1 kW 48 V to 12 V telecom quarter-brick fixed-frequency LLC with XDPP1100 digital controller

Using digital controller XDPP1100-Q024, OptiMOS™ 6 80 V ISC031N08NM6 with 3.3 mΩ max., OptiMOS™ 5 25 V IQE006NE2LM5 with 0.65 mΩ max., EiceDRIVER™ gate driver 2EDL803X-G3C, and 2DIB0410F ISOFACE™ dual-channel digital isolator

About this document

Feedback

Scope and purpose

This document presents the design and performance of a highly efficient 1 kW fixed-frequency LLC quarter-brick converter for 48 V intermediate bus converter applications. The reference board has an input voltage range of 42–60 V DC and output voltage range of 10–15 V DC, achieving a power density of 564 W/in^3 (34.6 W/cm^3) and 97.3 percent peak efficiency. The board is capable of providing 80 A output current without heatsinks. A higher power level is attainable if heatsinks are mounted. The board also achieves excellent EMI performance due to the soft-switching of the LLC converter.

The LLC quarter-brick converter incorporates a primary full-bridge with OptiMOS™ 6 80 V power MOSFET (ISC031N08NM6) with 3 mΩ max., and a secondary full-bridge with OptiMOS™ 5 25 V power MOSFET (IQE006NE2LM5) with 0.65 mΩ max. as synchronous rectifiers (SR). The superior characteristics of Infineon's power transistors result in very low losses and hence enable high power capability with enhanced efficiency and power density. Both the primary and secondary MOSFETs are driven by EiceDRIVER™ gate driver 2EDL8034-G3C in SON-10 3 mm × 3 mm package. Infineon 2DIB0410F ISOFACE dual-channel digital isolator with coreless technology provides high noise immunity and robust isolated communication to drive the primary gate drivers. Infineon's digital power controller XDPP1100-Q024, the industry's smallest digital controller with PMBus interface, is used in the design, providing utmost flexibility in efficiency optimization, soft-start implementation and enhanced protection.

The reference board follows the standard DOSA mechanical outline for high-current quarter-bricks. It is designed as a testing platform, with easy access to probe test points, and easy reworking/replacement of components.

Intended audience

This application note is intended for power supply design engineers.

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1 Introduction and design considerations

Intermediate-bus converters (IBCs) have been widely used in telecom, datacenters, servers, and other industrial applications. The trend in IBCs has been toward increased power density with optimized cost. High efficiency is a key factor in increasing power density, because heat dissipation must be minimized. Furthermore, higher efficiency directly reduces the ownership cost during the lifetime of the converter.

IBCs provide galvanic isolation and convert 48 V bus voltage to an intermediate low-level voltage to power the downstream point-of-load voltage regulators. The optimal IBC can be fully regulated, semi-regulated, or unregulated, depending on the system requirements for voltage variation range. Unregulated IBCs, also considered as DC transformers (DCX), typically achieve higher efficiency and higher power density, favorable in applications with narrow input voltage ranges. LLC resonant topology is a suitable candidate for unregulated intermediate bus conversion, which allows the converter to always operate at resonance, achieving optimal performance over the total load and voltage range.

This document describes the design and performance of a 1 kW fixed-frequency LLC quarter-brick converter. It is unregulated and has a conversion ratio of about 4:1. It operates from an input voltage range of 42–60 V DC to an output voltage range of 10–15 V DC. The reference board utilizes Infineon's advanced semiconductor technologies, which enables a power density of 564 W/in^3 (34.6 W/cm^3) and 97.3 percent peak efficiency. The board is capable of 80 A output current without heatsinks. Excellent EMI performance can be achieved due to the soft-switching of the LLC converter. The board follows the standard DOSA mechanical outline for high-current quarter-bricks.

OptiMOS™ 6 80 V MOSFET (ISC031N08NM6) is used in the primary full-bridge of the LLC quarter-brick converter. Infineon's OptiMOS™ 6 power MOSFETs utilize thin-wafer technology, offering next-generation, cutting-edge innovation, and best-in-class performance. Compared to alternative products, this family has reduced on-state resistance and improved figure-of-merit (FOM = $R_{DS(on)}$ × gate charge), allowing designers to increase efficiency and reduce system cost. [1]

OptiMOS™ 5 25 V MOSFET (IQE006NE2LM5) is used in the secondary full-bridge as SRs. This device comes in an innovative source-down PQFN 3.3 mm × 3.3 mm package, setting an industry benchmark in MOSFET performance. The source-down technology results in major reduction of $R_{DS(on)}$ by up to 30 percent compared to current technology. The thermal resistance between junction and case is significantly improved compared to the current PQFN packages. Reduced parasitics, improved PCB losses, as well as superior thermal performance, also add significant value to contemporary engineering designs. [2]

EiceDRIVER™ gate driver 2EDL8034G3C is used to drive both the primary and secondary MOSFETs. 2EDL8034G3C is a level-shift high-side low-side dual-channel driver with 4 A source and 6 A sink current capability. 2EDL8034's input pins support TTL logic levels independently of supply voltage. They are capable to withstand voltages from -10 V to 20 V, allowing the device to interface with a broad range of analog and digital controllers. The input stage features built-in hysteresis for enhanced noise immunity. The low-side and high-side gate drivers are independently controlled and matched to typical 2 ns between the turn on and turn of each other. [3]

Infineon's 2DIB0410F ISOFACE™ dual-channel digital isolator with coreless technology provides high noise immunity and robust isolated communication to drive the primary gate drivers. It provides 3 kV_{rms} isolation voltage and supports robust data rates up to 40 Mbps over a wide ambient operating temperature range (–40°C to +125°C). [4]

Infineon's digital power controller XDPP1100-Q024 is used in the design, providing utmost flexibility in efficiency optimization, soft-start implementation, and enhanced protection. XDPP1100-Q024 is the industry's smallest digital power controller with PMBus interface, offered in a 24-pin VQFN 4 mm × 4 mm package. The

device features many optimized power processing blocks and pre-programmed peripherals to enhance the performance of isolated DC-DC converters, reduce external components and minimize firmware development effort.

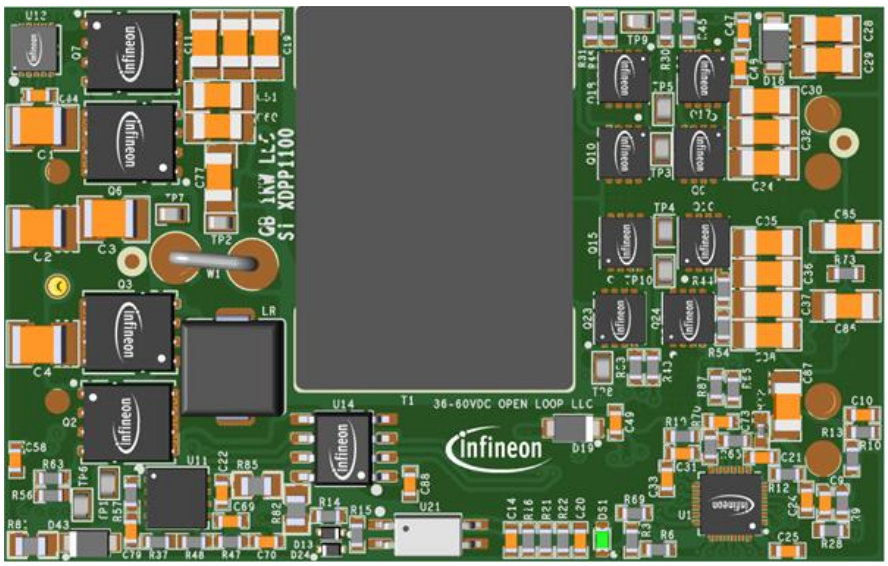
The controller also provides accurate telemetry and power management bus (PMBus 1.3) interface for system communication, advanced power conversion and monitoring. A combination of high-performance AFE, state machine-based digital control loop and an Arm® Cortex® M0 integrated in a single chip makes the XDPP1100 a highly integrated, fully programmable, and fastest-time-to-market technology for modern high-end power systems, employed in telecom infrastructure, 48 V server motherboards, datacenter and industrial 4.0 applications. [5]

Further details about the configuration and additional functionalities of this digital controller can be found in the XDPP1100 application note [6]. Infineon offers support tools such as a complementary XDPP1100 graphical user interface (GUI) that allows customers to configure and monitor key parameters for the XDPP1100. The XDPP1100 GUI tool is available to download in [7].

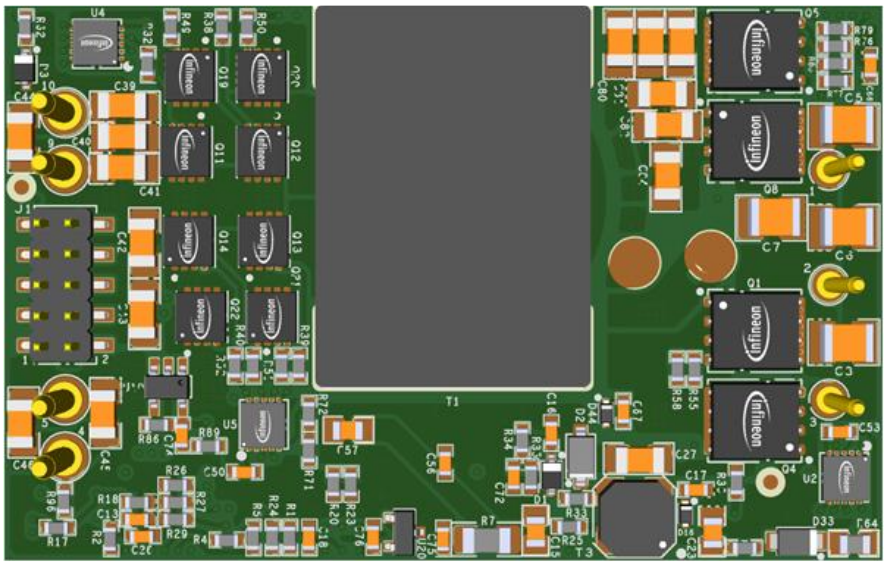
In addition, developers have full control of their application and firmware development process. Infineon enables designers to develop and compile their customized firmware in any commonly used Arm®-based development environment.

For further information on Infineon semiconductors see the Infineon website, as well as the Infineon evaluation board search tool, and the websites for the different implemented components:

- OptiMOS™ power MOSFETs
- Gate driver ICs
- XDP™ digital power controller
- ISOFACE™ digital isolator



Top view



Bottom view (flipped)

Figure 1 Infineon 1 kW fixed-frequency LLC quarter-brick converter reference board outline

1.1 System description

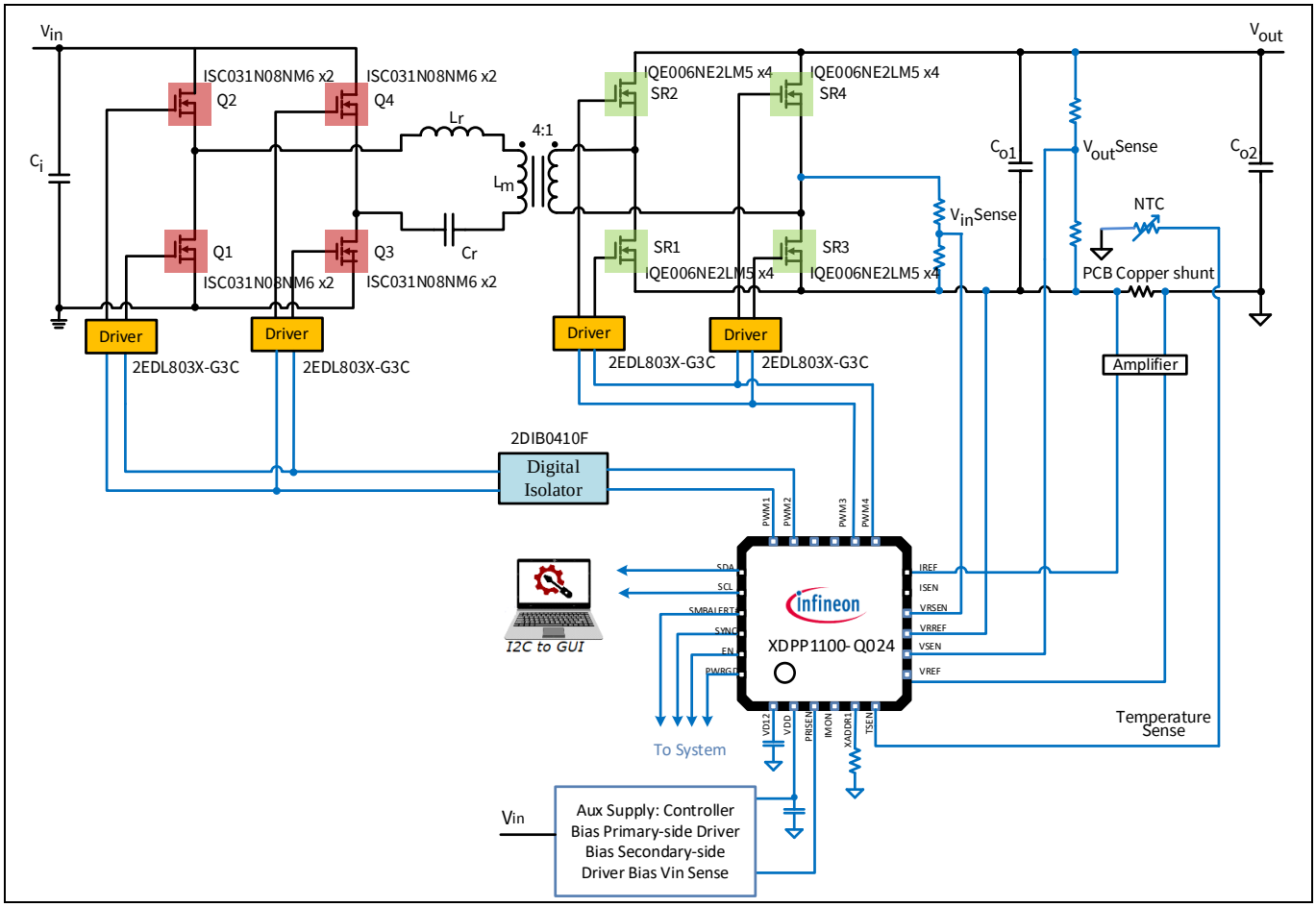


Figure 2 Infineon 1 kW fixed-frequency LLC quarter-brick converter – simplified block diagram

A block diagram of the LLC quarter-brick converter is shown in Figure 2. The converter consists of a primary full-bridge, a secondary full-bridge, a resonant inductor L_r, a resonant capacitor C_r and a 4:1 planar transformer. It has an input voltage range of 42–60 V DC and an output voltage range of 10–15 V DC. This converter is unregulated and operates at resonance with a fixed switching frequency. It achieves zero-voltage switching (ZVS) of all switches over the whole load and voltage range. The voltage stresses of primary FETs and secondary FETs equal the input voltage and output voltage, respectively, without ringing. Hence the 80 V MOSFET ISC031N08NM6 is used in the primary and the 25 V MOSFET IQE006NE2LM5 is used in the secondary. ISC031N08NM6 has an excellent FOM and superior switching performance. The low output capacitance reduces the required magnetizing current for ZVS operation in the LLC converter which lead to minimizing conduction losses. IQE006NE2LM5 has an industry-leading $R_{DS(on)}$, significantly lowering the conduction losses of SRs in the LLC converter. The reduced form factor (PQFN 3.3 mm × 3.3 mm footprint) enables more FETs to be paralleled in a given space, which further reduces conduction losses and offers superior thermal management.

The industry's smallest digital power controller XDPP1100-Q024 is used in the design to enhance the performance, reduce external components, and minimize firmware development effort. The XDPP1100-Q024 plays an important role in the fixed-frequency LLC quarter-brick converter. First, with the digital controller, the SR timing can be optimized for best efficiency. Second, the digital controller can easily implement a duty-cycle/frequency hybrid soft-start, which greatly reduces current stress during start-up. Third, the digital controller provides enhanced protections for the converter, including overvoltage protection (OVP),

undervoltage protection (UVP), overcurrent protection (OCP), and output short-circuit protection (SCP). The functions of the digital controller will be illustrated in detail in Sections 1.3, 1.4, and 1.5.

1.2 Design of resonant tank

The switching frequency f_{sw} is selected to be 310 kHz for optimal efficiency. With a fixed switching frequency, the LLC converter operates at resonance over the whole input voltage and load range. The voltage gain of the resonant tank is around 1. The design of the tank follows, as shown in Equation 1.

$$\frac{1}{2\pi\sqrt{(L_r+L_k)C_r}} = f_{sw}$$

Equation 1

As no regulation is required, the values of L_r and C_r are not so critical for operation as they would be in a regulated LLC converter. From the efficiency point of view, a small L_r is preferred, as a small L_r results in small core size and low core losses. On the other hand, a too-small L_r poses challenges for start-up and short circuit protection. A certain inductance is still needed to lower the current stress during start-up and limit the current rising rate for short-circuit protection. As a compromise, 85 nH inductor LP02-800-1S is selected in this design. Note that leakage inductance L_k of the transformer adds to the total resonant inductance. As a planar transformer is implemented in the design, it gives very low and highly repeatable leakage inductance (approximately 50 nH). Resonant capacitor C_r can be calculated from Equation 1. In practice, the exact value of C_r can be found by tuning the resonant waveforms. In this design, C_r is chosen to be 1.89 µF.

In order to achieve ZVS, magnetizing inductance L_m of the transformer needs to be small so that the magnetizing current is large enough to completely charge/discharge the output capacitance of primary FETs within the dead-time. Then the body-diode conducts and hence ZVS can be achieved. The switching transition is shown in Figure 3.

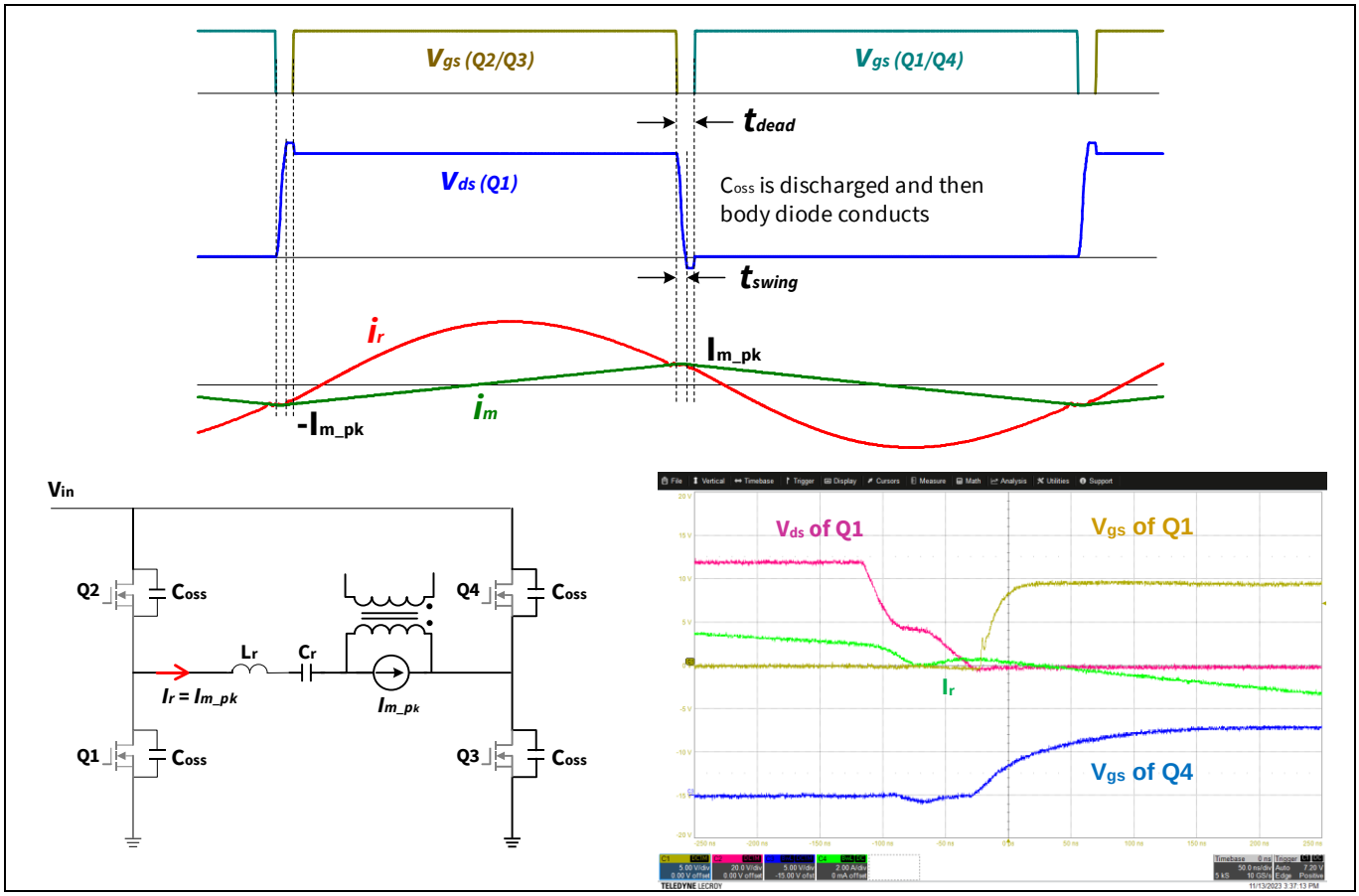


Figure 3 Switching transition

The calculation of maximum L_m for ZVS operation is provided from Equation 2 to Equation 5.

According to the magnetizing current waveform, I_{m_pk} can be calculated as follows:

$$nV_o = L_m \cdot \frac{2I_{m_{pk}}}{0.5T_{sw}}$$

Equation 2

Where, $I_{m\_pk} = \frac{nV_o}{4L_m \cdot f_{sw}}$

During the switching transition, C_{oss} is discharged/charged from V_{in} to zero by I_{m_pk} as follows:

$$I_{m\_pk} = 2m \cdot C_{ossAvg} \cdot \frac{V_{in}}{t_{swing}}$$

Equation 3

Where, $t_{swing} = \frac{2m \cdot C_{ossAvg} \cdot V_{in}}{I_{m\_pk}}$

The dead-time must be larger than V_{ds} swing time, so that body-diode can conduct to ensure ZVS.

$$t_{dead} > t_{swing}$$

Equation 4

Combining Equation 2 to Equation 4, the maximum L_m can be calculated by:

$$L_m < \frac{t_{dead} \cdot nV_o}{8m \cdot C_{ossAvg} \cdot f_{sw} \cdot V_{in}} = \frac{t_{dead}}{8m \cdot C_{ossAvg} \cdot f_{sw}}$$

Equation 5

Where it is assumed $nV_o = V_{in}$ for ~100 percent efficiency.

Where C_{ossAvg} is average output capacitance of each FET during voltage swing, and m is the number of FETs in parallel.

Note: As C_{oss} varies with drain-source voltage, the average value of C_{oss} during voltage swing should be used.

In this design, t_{dead} = 80 ns, f_{sw} = 310 kHz, m = 2, C_{ossAvg}≈ 1500 pF. According to Equation 5, L_m< 10.7 µH.

The selection of dead-time has some trade-off considerations. If the dead-time is too small, higher magnetizing current is needed to charge/discharge C_{oss}, increasing conduction losses. If the dead-time is too large, effective duty-cycle is reduced, increasing circulating losses without power delivery, especially in high-frequency designs.

In this design, dead-time is selected to be 80 ns. Two ISC031N08NM6 MOSFETs are used in parallel at the primary for lower conduction losses. The average C_{oss} of each ISC031N08NM6 during V_{ds} voltage swing from V_{in} to 0 is approximately 1500 pF, which can be found in Figure 4 from the datasheet of ISC031N08NM6. According to calculations from Equation 2 to Equation 5, L_m needs to be smaller than 10.7 µH. A magnetizing inductance of 9 µH is finally chosen in the design, which is obtained by adding two layers of polyimide film tape (5 mil gap) between the transformer cores.

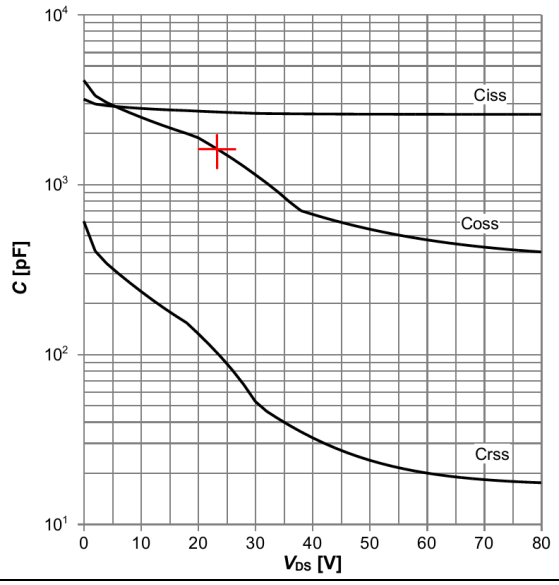


Figure 4 Capacitance curves of primary MOSFET ISC031N08NM6

The voltage gain curves of the resonant tank based on this design are plotted in Figure 5. It verifies that the voltage gain of the tank is around 1 across the whole load range, with quite a wide tolerance to switching frequency.

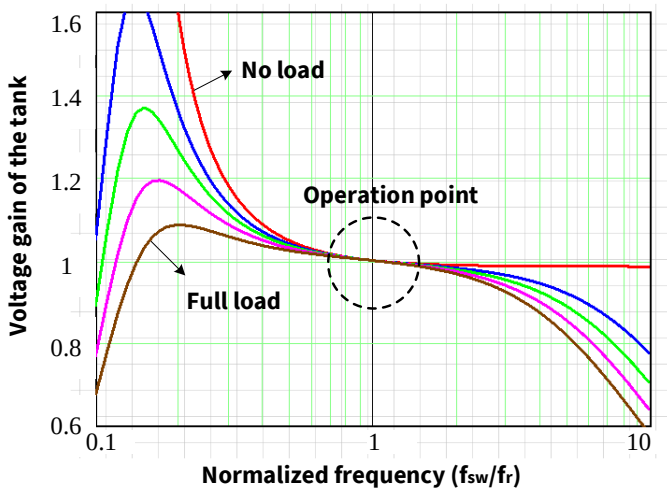


Figure 5 Voltage gain curves of the resonant tank in this fixed-frequency LLC converter

1.3 SR timing

The primary gate signals have 50 percent duty-cycle with dead-time. The secondary SR timing is critical for efficiency optimization. Typically, multiple SR FETs are used in parallel to minimize conduction losses. As multiple FETs are paralleled and driven by a single driver, the gate signals are rising/falling much slower than primary FETs. Then the SR gate falling edge must be earlier than the primary gate falling edge, to ensure that SRs can be turned off earlier than primary FETs. Furthermore, a certain blanking time (about 30 ns) is necessary between the real turn-off of the SRs (the point when V_{gs} falls below the gate threshold voltage) and the real turn-off the primary FETs, to make sure no negative currents flow through SRs. Besides, as an optocoupler is used to isolate the primary PWM signals from the secondary, the isolation delay of the optocoupler must be taken into account when the digital controller generates PWM signals. An ideal timing diagram of the fixed-frequency LLC converter is shown in Figure 6.

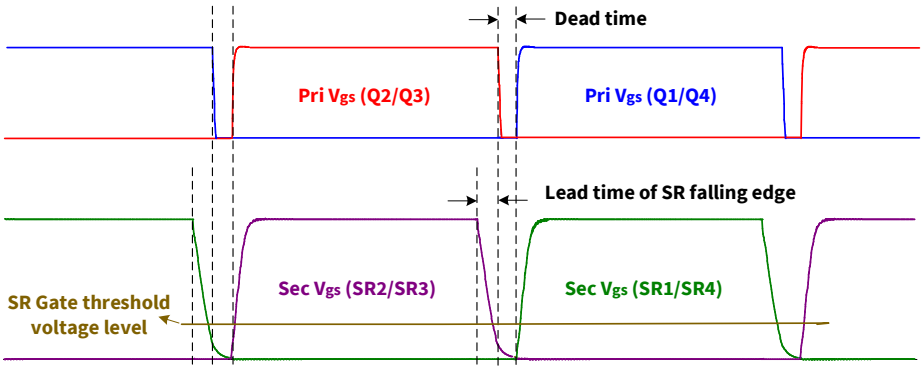


Figure 6 Ideal timing diagram of the fixed-frequency LLC quarter-brick converter

The use of Infineon's digital controller XDPP1100-Q024 can easily satisfy the above timing requirements in the LLC quarter-brick converter. XDPP1100 is highly flexible in PWM configuration. The rising-edge and falling-edge delay of each PWM can be programmed independently. Figure 7 shows the PMBus command in the GUI to

configure the rising and falling edge of the primary and secondary PWMs. The maximum delay time can be set to 318.75 ns with a resolution of 1.25 ns. The active PMWs are highlighted in color.

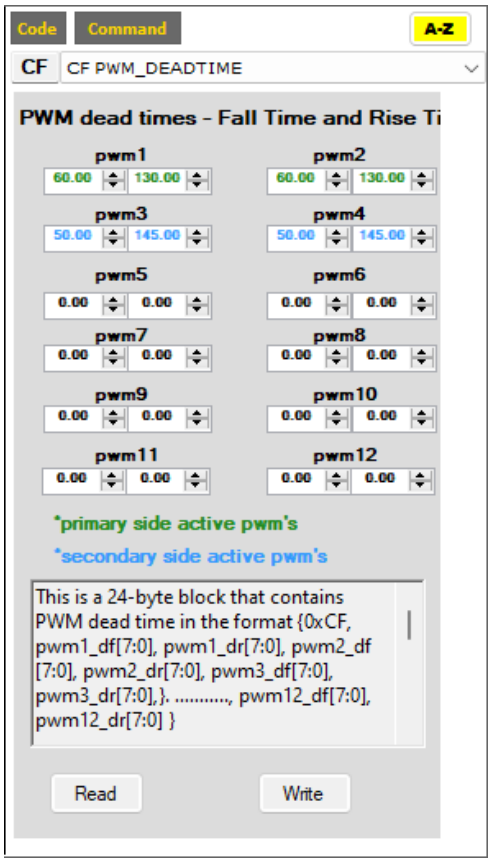


Figure 7 PWM rising-edge and falling-edge configuration in digital controller XDPP1100

1.4 Soft-start

Soft-start is needed to establish the output voltage progressively in order to prevent high current stress. One common method is to start up by sweeping the switching frequency from an initial high value down to the resonant point. The maximum switching frequency of the converter is limited by hardware (especially by the driving capability of the bias supply). If the allowed maximum frequency is not high enough (over 3–4 times the resonant frequency), a large inrush current can still occur, since the voltage gain is not low enough at the beginning.

Another method for soft-start is to ramp up the duty-cycle from 0 to nearly 50 percent (with dead-time) at resonant frequency. The LLC converter operates in PWM mode, and high initial inrush current can be avoided. As resonant inductance is typically small, the converter may still suffer from very high peak current when operating at resonant frequency, especially at start-up under harsh constant-current load conditions. High current stress may also cause large ringing on V_{ds} of the FETs in PWM-mode operation, increasing the voltage stress during start-up.

In this design, a duty-cycle/frequency hybrid soft-start is presented. The duty-cycle ramps up from 0 to nearly 50 percent (with dead-time) at a higher switching frequency (e.g., 500 kHz). Then duty-cycle is fixed at nearly 50 percent and switching frequency decreases gradually from the high value to the resonant frequency (310 kHz). As the converter operates in PWM mode at a higher switching frequency, the peak current can be reduced. The PWM sequence of the duty-cycle/frequency hybrid soft-start is shown in Figure 8.

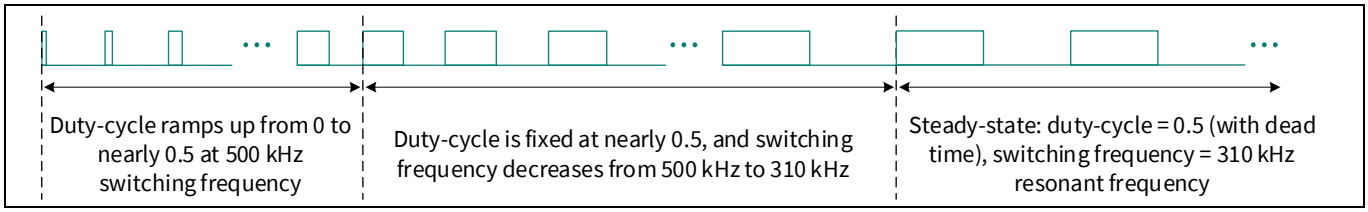


Figure 8 PWM sequence of the duty-cycle/frequency hybrid soft-start

With the XDPP1100-Q024 digital controller, the duty-cycle/frequency hybrid soft-start can be easily implemented. A customized firmware patch for the start-up procedure has been developed and can be loaded into the one-time programmable (OTP) memory. The start-up parameters, like the maximum switching frequency, duty-cycle ramp time, and frequency decrease time can be configured by the MFR PMBus command, which can be imported into the GUI using the “Load PMBus Spread Sheet” button. The PMBus spreadsheet can be found in the GUI installation folder.

1.5 Fault protections

The XDPP1100-Q024 digital controller has two 11-bit voltage-sense ADCs with 50 MHz sampling rate, one 9-bit current-sense (CS) ADC with 25 MHz clocking speed, and a 9-bit general-purpose telemetry ADC which consists of four channels and can be configured to digitize voltage, current, impedance, and temperature. These dedicated hardware peripherals of XDPP1100-Q024 make it possible to provide enhanced protections for the LLC quarter-brick converter.

The XDPP1100-Q024 controller is located on the secondary side and senses the input voltage, the output voltage, and the output current, as can be seen in Figure 2. The output voltage is sensed directly by resistor-dividers. The input voltage is sensed from the transformer secondary side at the switching node V_{rect} and computed based on the resistor-divider ratio and the transformer turns ratio. This eliminates the use of an isolated op-amp or other types of isolators for input voltage sensing. The output current is sensed through a PCB copper shunt with amplifier. The temperature of the PCB copper shunt is also sensed by an NTC thermistor and used for CS temperature compensation. The temperature compensation is to eliminate the copper resistance drift overtemperature to enable accurate output current telemetry across the full temperature range.

Three levels of OCP can be configured in the LLC quarter-brick converter through XDPP1100 GUI. The first-level OCP is provided by IOUT_OC_FAULT, which is based on the averaged output current after a low-pass filter. It has the slowest response, and so the fault threshold IOUT_OC_FAULT_LIMIT should be set lowest. The second-level OCP is provided by IOUT_OC_FAST_FAULT. It is based on the averaged output current but without the filter. It has a faster response and the fault threshold IOUT_OC_FAST_FAULT_LIMIT should be set higher than IOUT_OC_FAULT_LIMIT. The third-level OCP is provided by the registers for SCP. SCP fault trips when the sensed output current goes above the SCP threshold (isp0_scp_thresh) for a single ADC sample. It has the fastest response, and the SCP threshold should be set to the highest.

Besides the three-level OCP, the LLC quarter-brick converter also has output OVP/UVP and input OVP/UVP. The XDPP1100 fault detection is implemented in hardware (HW) and the fault response is managed by firmware (FW). The combination of HW and FW provides fast protection with flexible fault response. Further details about the configuration and additional functionalities of fault protections can be found in the XDPP1100 application note [6].

2 Power board information

2.1 Specifications

The specification of the 1 kW fixed-frequency LLC quarter-brick converter is shown in Table 1.

Table 1 Specifications

Parameter	Min.	Typ.	Max.	Unit
Input voltage range (V_{in})	42	48	60	V DC
V_{in} turn-on threshold	34	–	–	V
V_{in} turn-off threshold	32	–	–	V
Input current (at 100 percent load)	–	20	–	A
Output voltage range (V_{out})	10	12	15	V DC
Output current (I_{out})	–	80	–	A DC
Output power	–	960	1200	W
Output voltage ripple (peak-to-peak at full load, measured with 1800 µF tantalum capacitor)	–	–	400	mV
Dynamic load response (50 percent to 100 percent load-transient at 1 A/µs slew rate, measured with 1800 µF tantalum capacitor): • Output voltage deviation (peak-to-peak) • Settling time	–	–	 680 200	 mV µs
Recommended output capacitor	1000	–	10000	µF
Efficiency (V_{in} = 48 V DC) at 25°C: • 25 percent load • 50 percent load • 75 percent load • 100 percent load	–	 97.02 97.27 96.76 96.05	–	%
Switching frequency	–	310	–	kHz
Air flow	–	600	–	LFM
Operating temperature (ambient)	–40	–	50	°C

2.2 Schematics

Figure 9 and Figure 10 shows the schematics of the power stage and control circuit of the 1 kW fixed-frequency LLC quarter-brick converter. Two OptiMOS™ 6 80 V MOSFETs ISC031N08NM6 with 3.3 mΩ are used in parallel in the primary full-bridge and driven by a single 2EDL8034-G3C driver at each branch. Four OptiMOS™ 5 25 V MOSFETs IQE006NE2LM5 with 0.65 mΩ are used in parallel in the secondary full-bridge and driven by a single 2EDL8034-G3C driver at each branch.

The XDPP1100-Q024 digital controller is used for PWM generation and soft-start implementation as well as telemetry and protection. Voltage ADC VSEN/VREF is used for output voltage sense. The other voltage ADC VRSEN/VRREF is used for input voltage sense through the transformer secondary winding. A high-speed current

ADC ISEN/IREF is used for output CS. TSEN is used for temperature sense of the PCB copper shunt for CS temperature compensation.

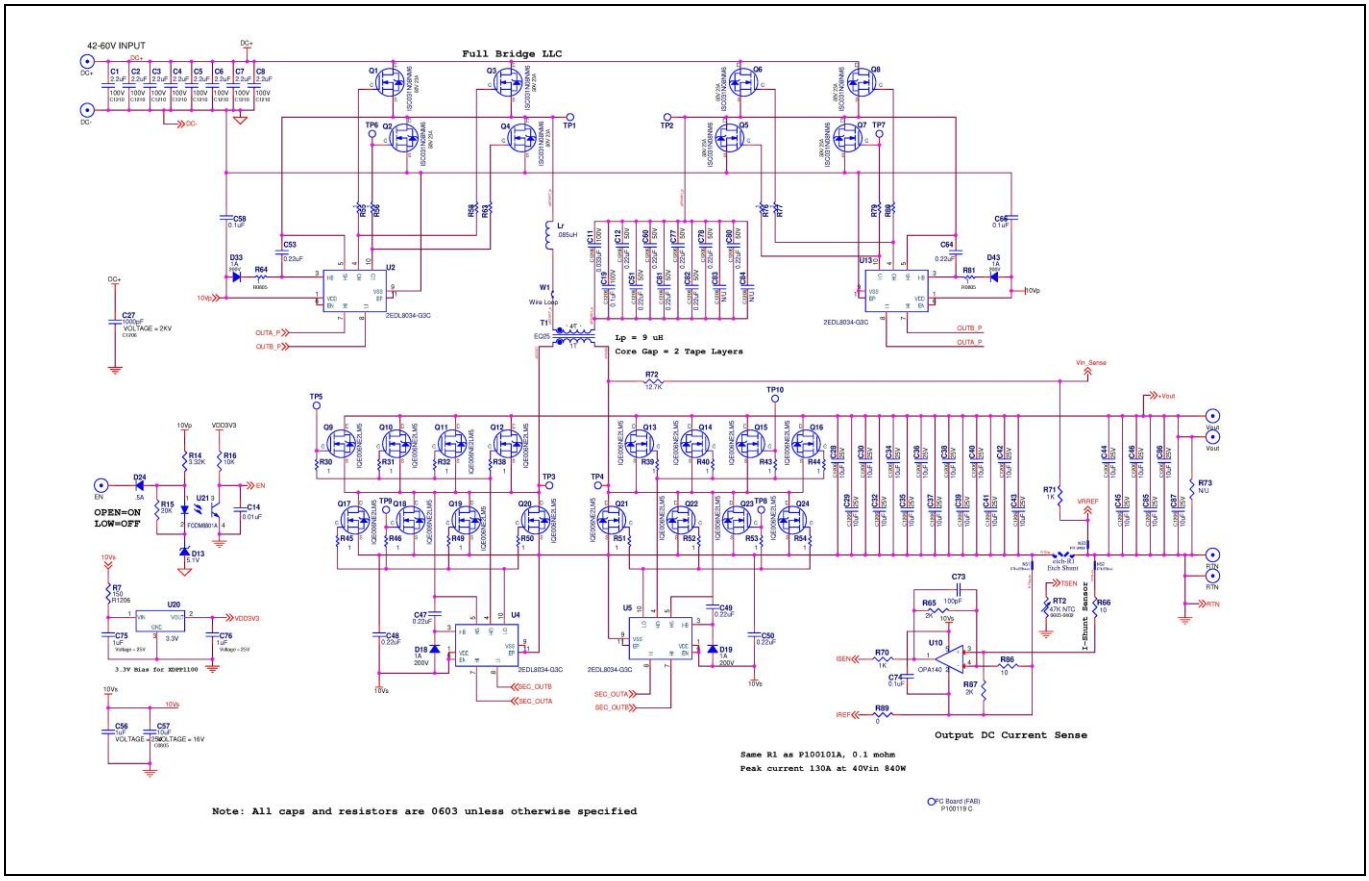


Figure 9 Power stage schematic

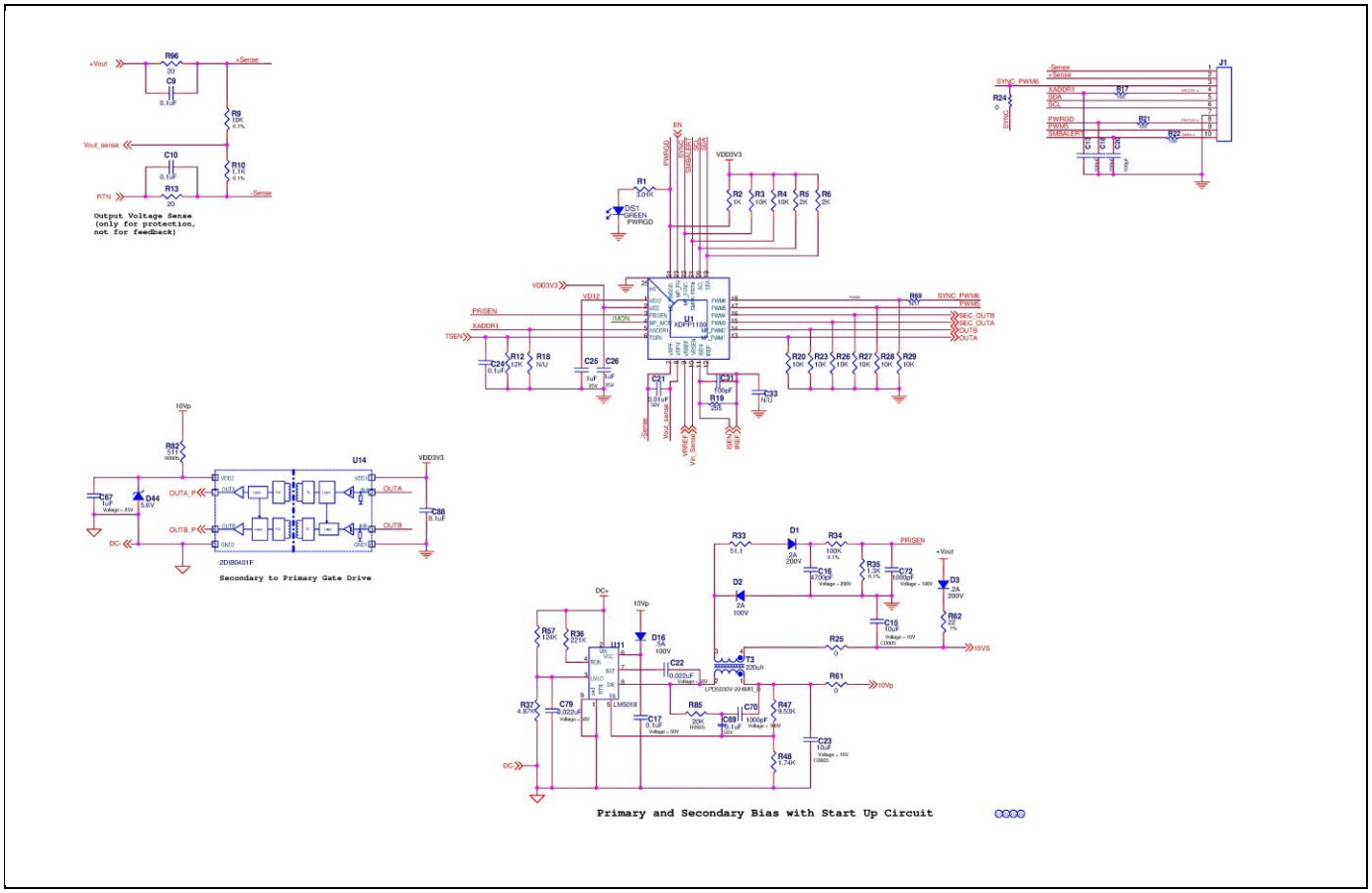


Figure 10 Control and bias circuit schematic

Figure 11 and Figure 12 give the top and bottom-side PCB reference drawings showing part locations for each component. Measurement test points are also highlighted in the reference drawings.

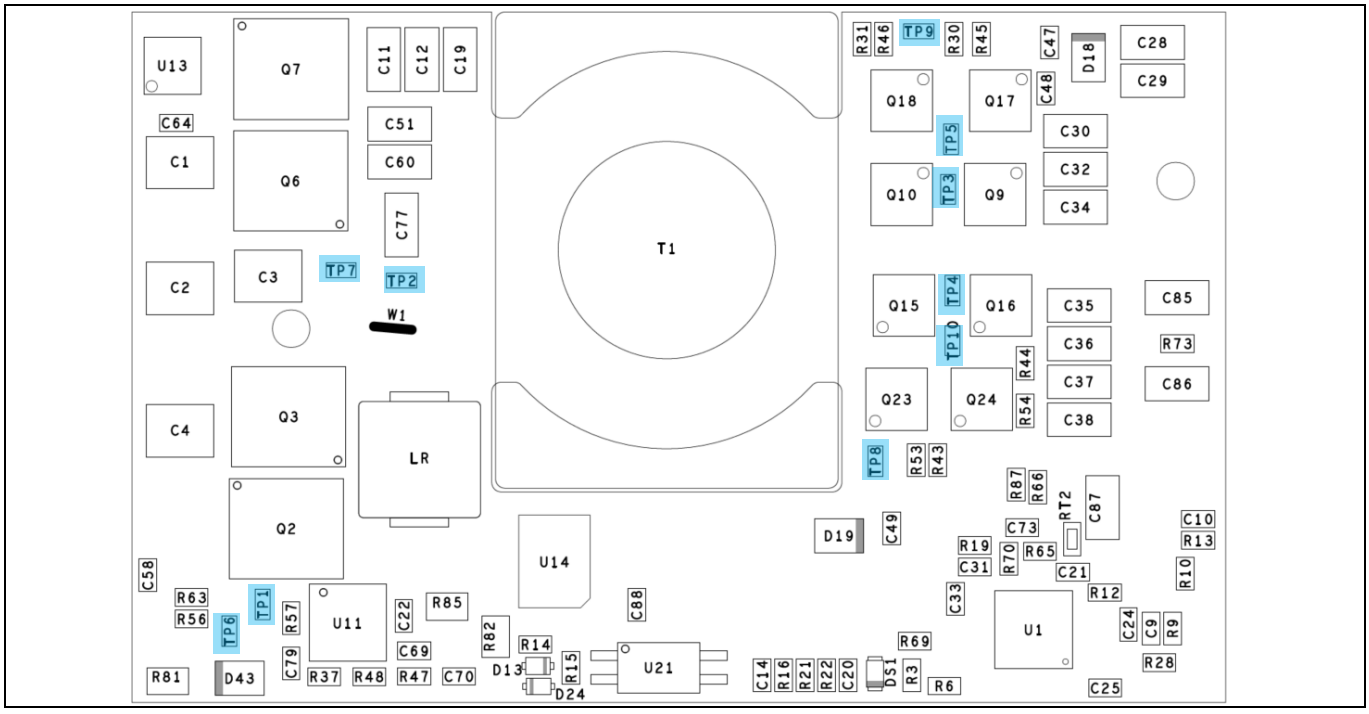


Figure 11 Assembly reference – top side of PCB

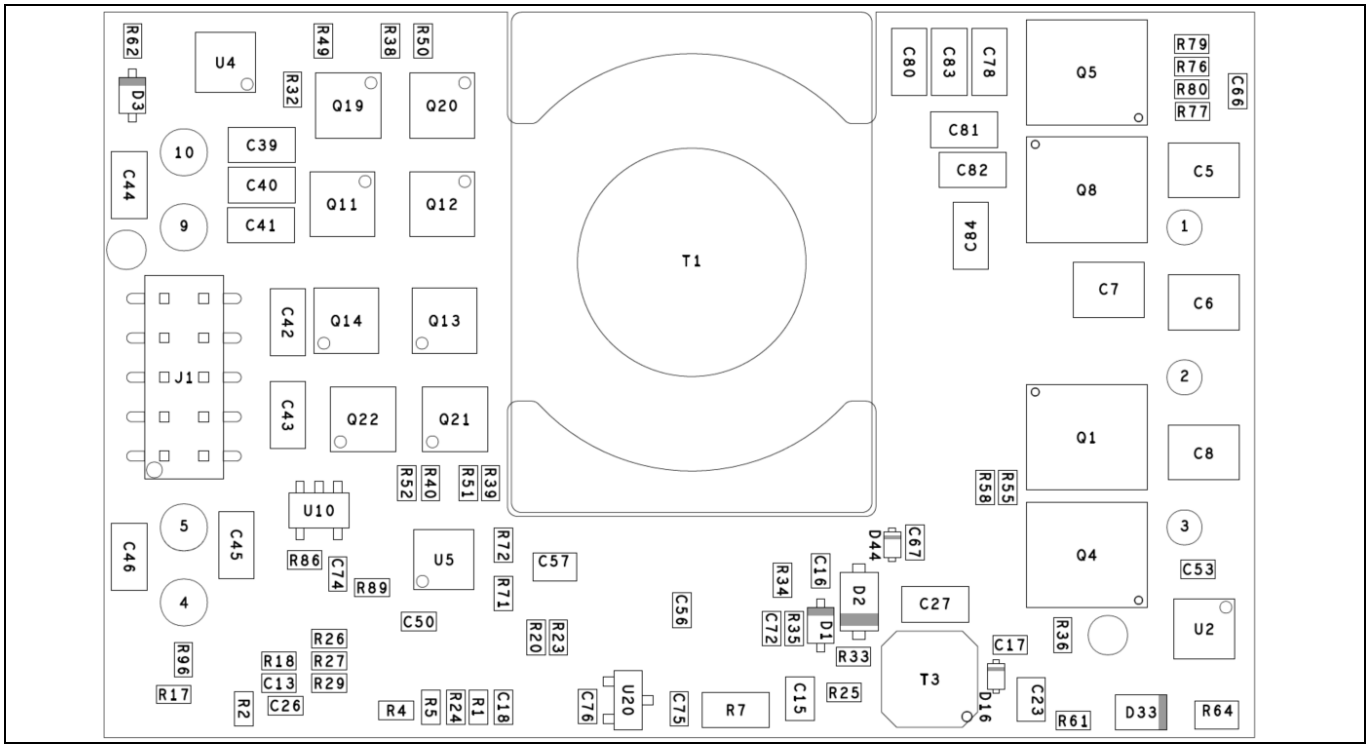


Figure 12 Assembly reference – bottom side of PCB

2.3 Transformer

The transformer has a conversion ratio of four primary turns to one secondary turn with a planar construction. The core geometry is an EQ25 and a plate with ferrite material ML27D. The primary winding is composed of four

PCB layers in series while the secondary winding is composed of ten PCB layers in parallel. The primary windings have been interleaved with the secondary windings for minimum leakage inductance and proximity losses. A detailed description of the construction can be seen in Figure 13.

In this design, a magnetizing inductance of 9 µH is needed for ZVS. Two layers of TestEquity TST22-0250 polyimide film tape (5 mil gap in total) have been added between the EQ25 core and the plate in order to obtain the required inductance.

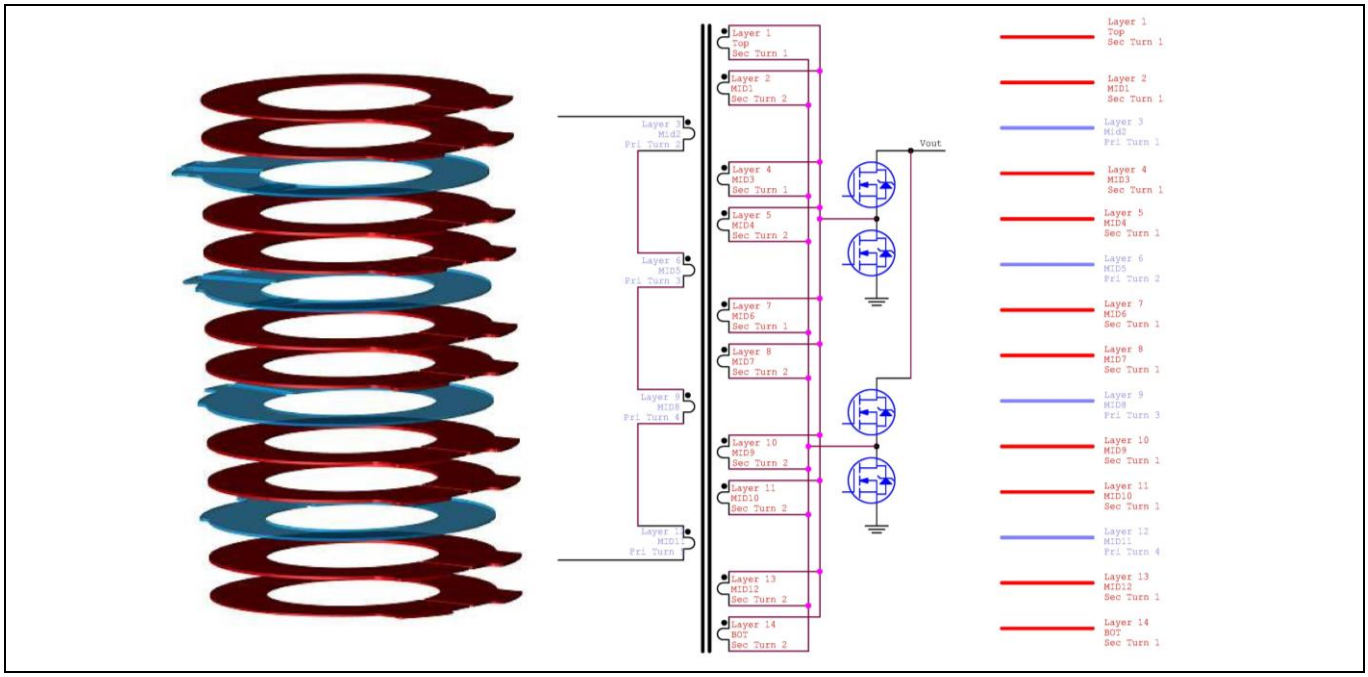


Figure 13 Planar transformer construction

2.4 Board layout

Figure 14 shows the placement of the component locations on the 1 kW fixed-frequency LLC quarter-brick converter. The outer dimensions of the board, designed without enclosure, are 2.30" × 1.45" × 0.51" (58.4 mm × 36.8 mm × 12.9 mm), which results in a power density in the range of 564 W/in^3 (34.6 W/cm^3). The PCB is fabricated from a 14-layer board. The internal layers are all 6 oz. copper, 8.23 mil (0.209 mm) thickness with the top and bottom layers at 4 oz. copper, 5.5 mil (0.140 mm) thickness. See Appendix for mechanical outline and bill of materials (Table 4) of the LLC quarter-brick converter.

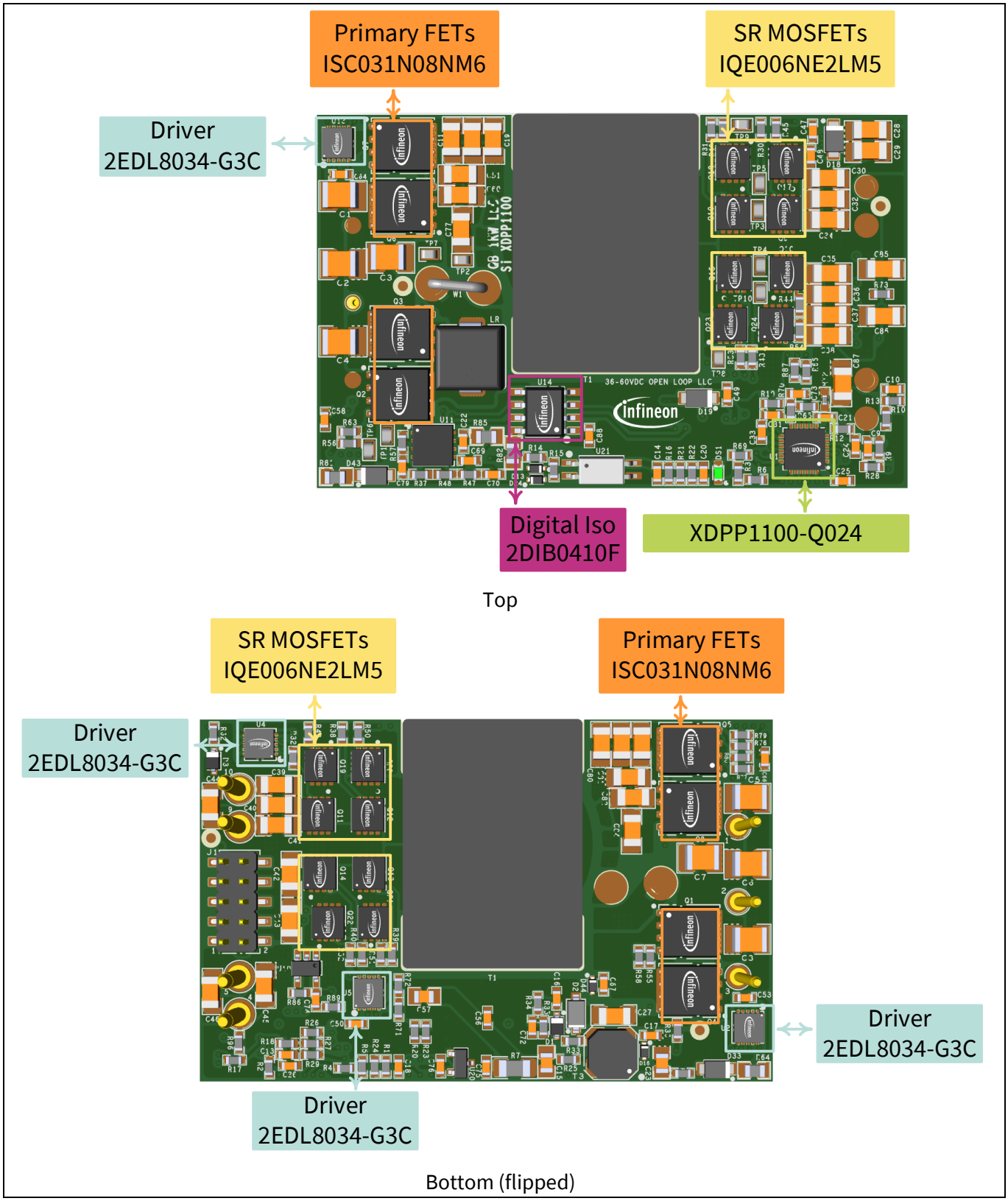


Figure 14 Placement of the different sections

2.5 Power loss analysis

The major sources of power losses are identified and calculated as in Table 2. At V_{in} = 48 V and I_{out} = 80 A, the estimated total power loss is 30.84 W. The measured power loss is 38.4 W. The loss breakdown chart is shown in Figure 15.

Table 2 Loss breakdown at V_{in} = 48 V and I_{out} = 80 A

Component	Type of loss	Individual loss	Cumulative loss
Primary MOSFETs	Conduction loss	2.70 W	3.82 W
	Body diode loss	0.29 W	
	Driving loss	0.83 W	
Secondary MOSFETs	Conduction loss	4.48 W	8.21 W
	Body diode loss	0.70 W	
	Driving loss	3.03 W	
Transformer	Conduction loss	7.40 W	8.77 W
	Core loss	1.37 W	
Resonant inductor	Conduction loss	0.13 W	1.23 W
	Core loss	1.10 W	
Resonant capacitor	–	–	0.17 W
Output capacitor	–	–	0.23 W
Auxiliary bias circuit	–	–	1.06 W
High current PCB traces and vias	–	–	7.35 W
Total losses	–	–	30.84 W

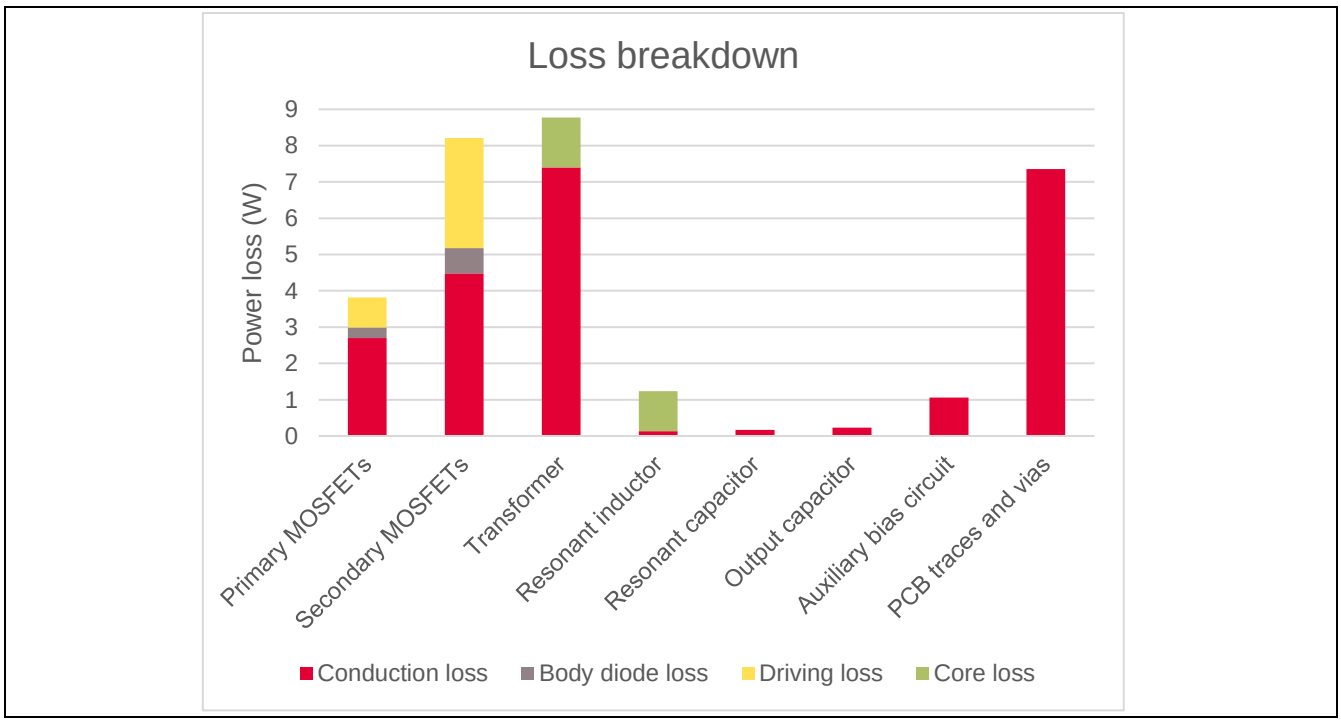


Figure 15 Power loss breakdown

2.6 Cooling solution and test setup

The quarter-brick test fixture is a test platform for the quarter-brick converter. It provides power connection terminals, communication and debugging ports, as well as a cooling fan. Figure 16 shows the schematic of the test fixture. It has an I²C connector for I²C and PMBus communication, and a SWD debugger port for FW debugging. The fan should be biased with external DC power supply, in the 5 V to 12 V range for different airflow. This bias is necessary to enable communication with the XDPP1100 to the USB dongle.

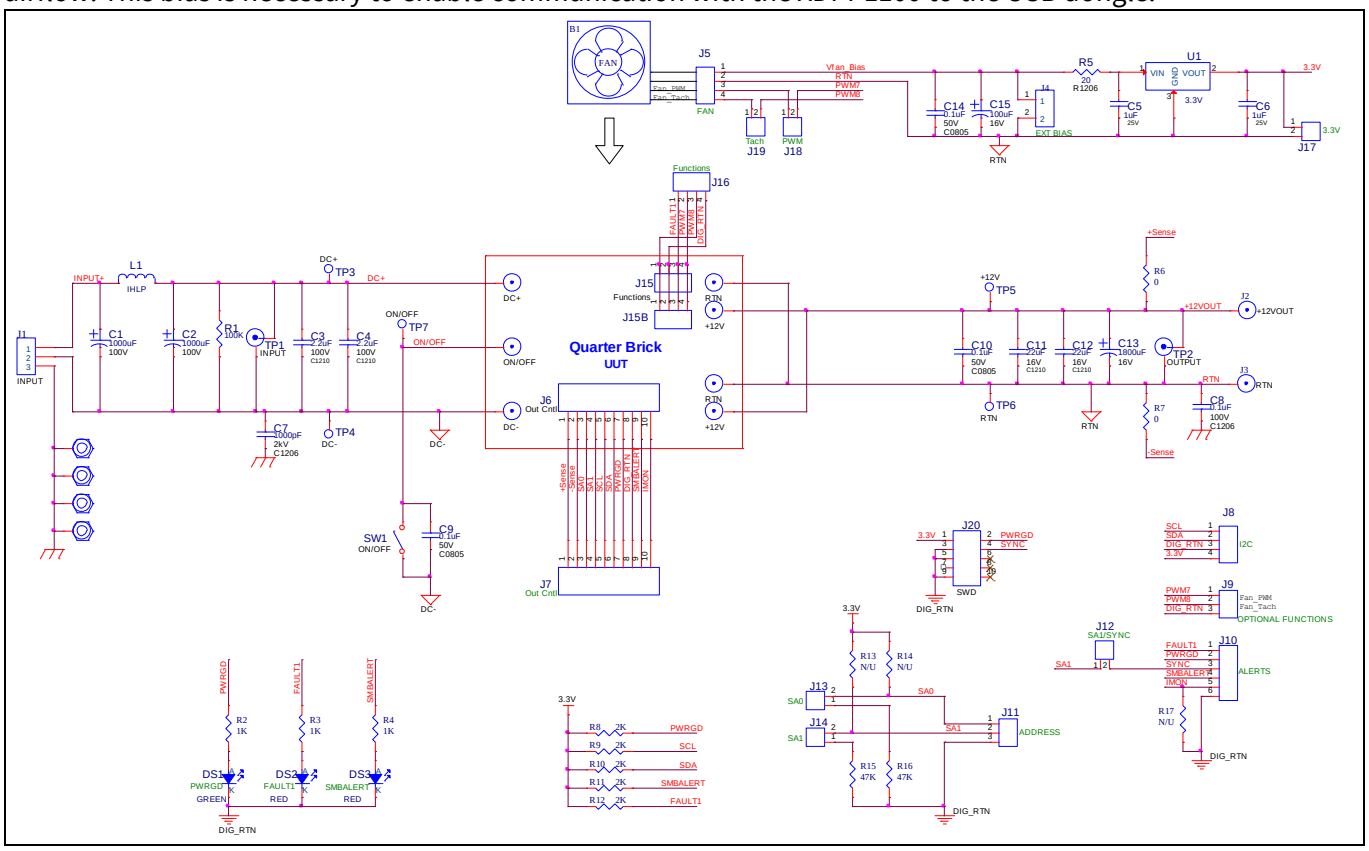


Figure 16 Test fixture schematic

The switch SW1 at the primary is the enable-switch to turn-on the quarter-brick. Ensure that the polarity of the enable-switch can be configured by PMBus command ON_OFF_CONFIG. If EN “active low” is preferred, the user should write PMBus command ON_OFF_CONFIG and choose the polarity to be “active low”. When “active low” is selected, the on/off label on the test fixture aligns with the actual on/off status. If “active high” is selected, the on/off label shows the opposite status.

A 3.3 V LDO regulator on the test fixture provides pull-up voltage to the SDA/SCL I²C communication bus when 5 V to 12 V is applied to the external bias connector.

Test setup for the 1 kW fixed-frequency LLC quarter-brick converter using the test fixture is shown in Figure 17.

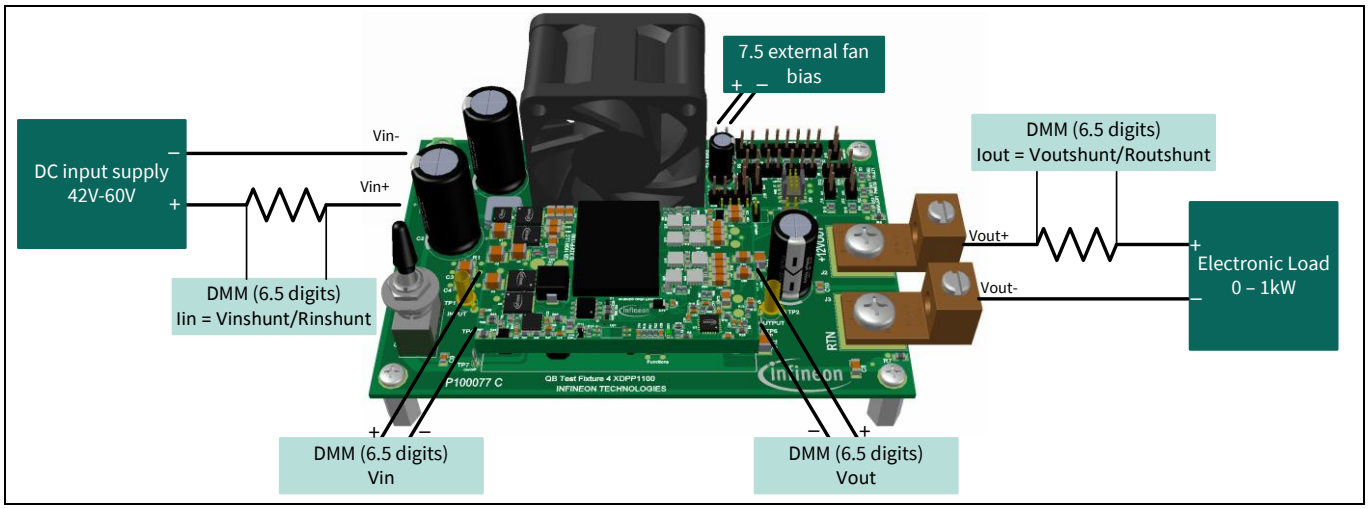


Figure 17 Test setup with test fixture

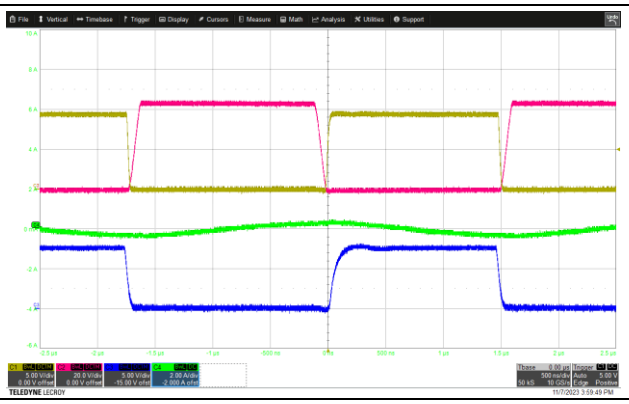
Necessary connections to operate the board:

1. Connect the quarter-brick to the test fixture. Make sure the DC input, 12 V output, and the signal connector J6 on the test fixture have good contact.
2. Connect the 48 V input power supply to J1.
3. Connect the load to J2 and J3.
4. Bias the fan with a 5–12 V DC power supply at J4 (EXT BIAS).
5. Connect the XDPP1100 USB dongle (USB007 revA) to J8. Find the direction by identifying the ground pin G (black wire). The blue wire of USB007 is not used.
6. Make sure the switch SW1 is in the off position.
7. Turn on the 48 V input power supply. A minimum of 35 V is required to enable the auxiliary power supply.
8. The secondary side voltage of auxiliary power supply (10VS) should provide a 10 V ± 1 V output.
9. This demo board comes with a default patch and configuration stored in OTP and can be turned on once the operation command is asserted from the XDPP1100 GUI.
10. In order to assert the operation command, open XDPP1100 GUI and click on “Auto populate”. The auto populate option is in the top-left corner just below the “file” option.
11. Write “ON” to PMBus command 0 × 01 operation and turn SW1 to the on position (sequence is not critical).

3 Experimental results

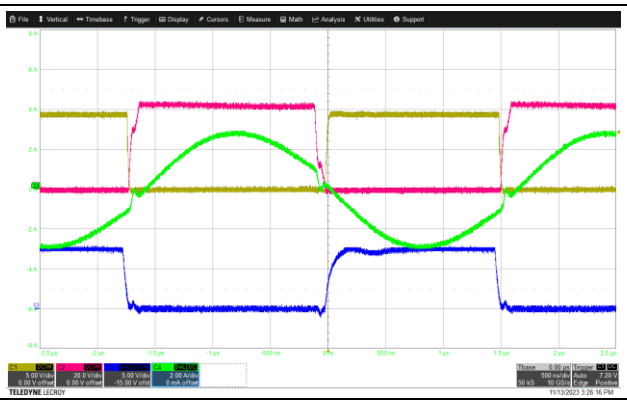
3.1 Steady-state waveforms

Figure 18 shows the key steady-state waveforms measured on the 1 kW FF LLC quarter-brick converter mounted to the Infineon test fixture. As can be seen, ZVS is achieved over a wide line and load range.



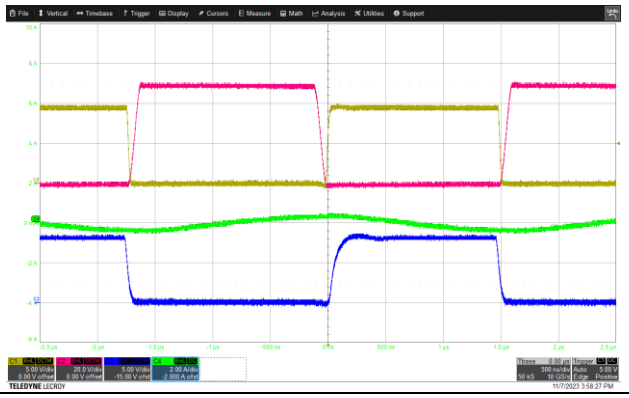
Ch.1= Primary Vgs(Q2) Ch.2= Primary Vds(Q2) Ch.3= Secondary Vgs(Q18) Ch.4= Resonant current(1:10)

Steady-state waveforms at V_{in} = 42 V and I_{out} = 0 A



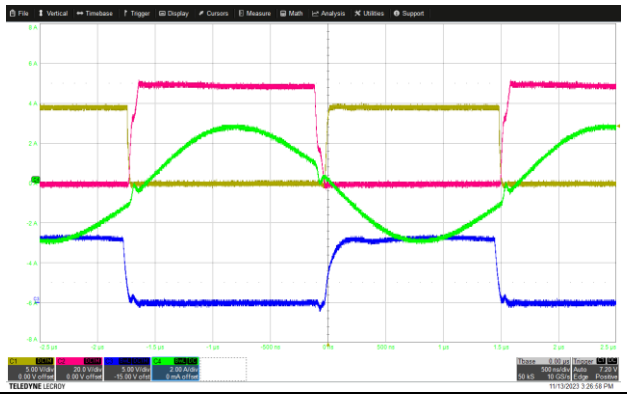
Ch.1= Primary Vgs(Q2) Ch.2= Primary Vds(Q2) Ch.3= Secondary Vgs(Q18) Ch.4= Resonant current(1:10)

Steady-state waveforms at V_{in} = 42 V and I_{out} = 80 A



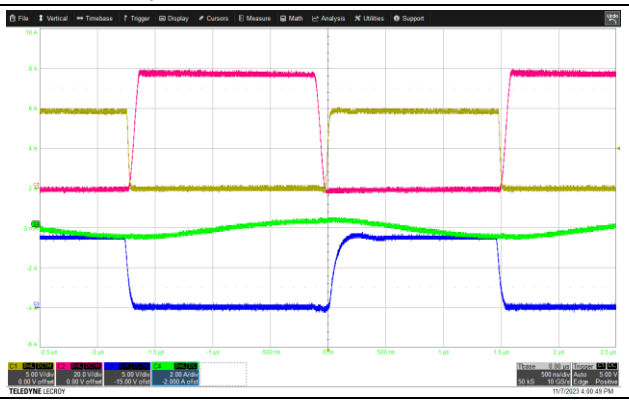
Ch.1= Primary Vgs(Q2) Ch.2= Primary Vds(Q2) Ch.3= Secondary Vgs(Q18) Ch.4= Resonant current(1:10)

Steady-state waveforms at V_{in} = 48 V and I_{out} = 0 A



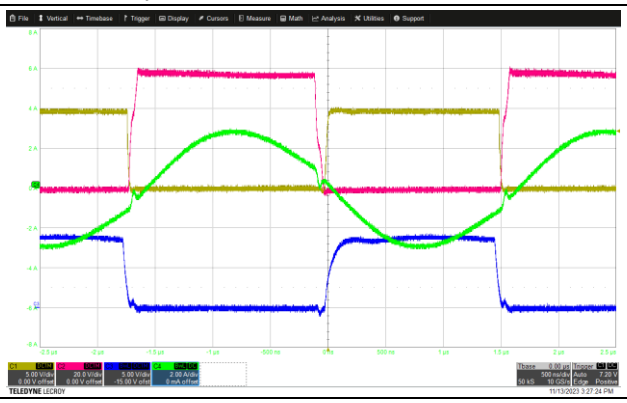
Ch.1= Primary Vgs(Q2) Ch.2= Primary Vds(Q2) Ch.3= Secondary Vgs(Q18) Ch.4= Resonant current(1:10)

Steady-state waveforms at V_{in} = 48 V and I_{out} = 80 A



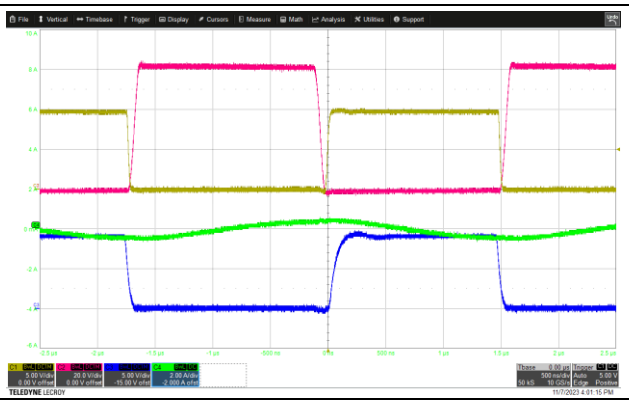
Ch.1= Primary Vgs(Q2) Ch.2= Primary Vds(Q2) Ch.3= Secondary Vgs(Q18) Ch.4= Resonant current(1:10)

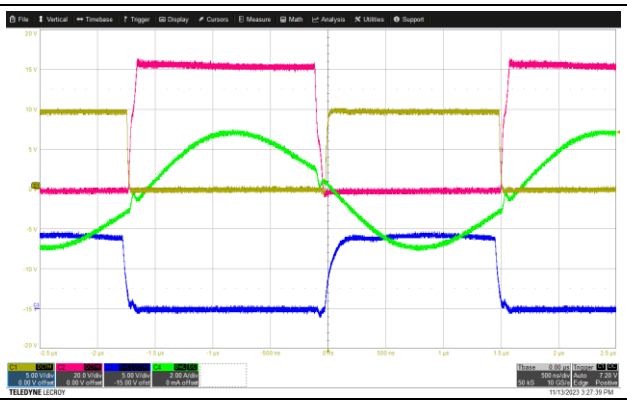
Steady-state waveforms at V_{in} = 56 V and I_{out} = 0 A



Ch.1= Primary Vgs(Q2) Ch.2= Primary Vds(Q2) Ch.3= Secondary Vgs(Q18) Ch.4= Resonant current(1:10)

Steady-state waveforms at V_{in} = 56 V and I_{out} = 80 A





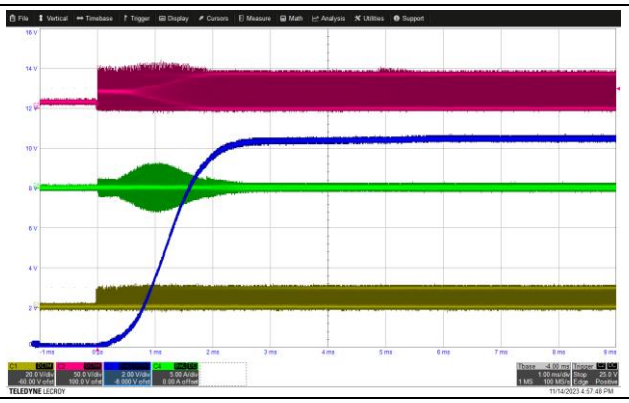
Ch.1= Primary Vgs(Q2) Ch.2= Primary Vds(Q2) Ch.3= Secondary Vgs(Q18) Ch.4= Resonant current(1:10)

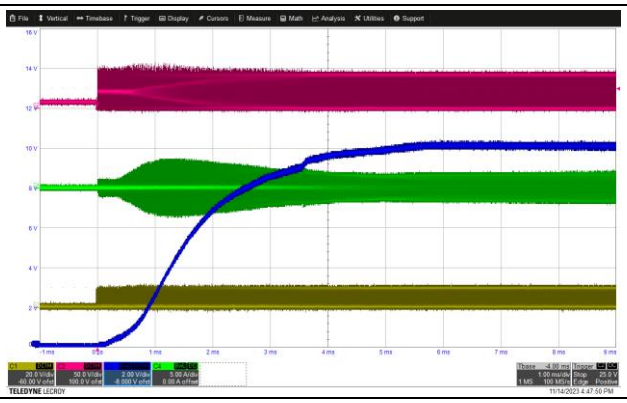
Steady-state waveforms at V_{in} = 60 V and I_{out} = 0 A	Steady-state waveforms at V_{in} = 60 V and I_{out} = 80 A

Figure 18 Steady-state waveforms

3.2 Start-up waveforms

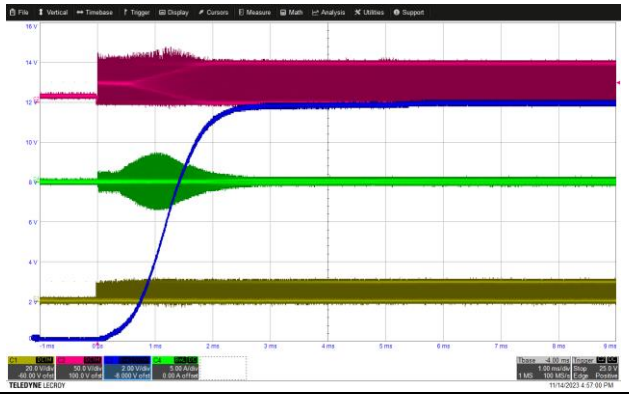
The duty-cycle/frequency hybrid soft-start over a wide line and load range has been tested. Figure 19 shows the soft-start waveforms measured under resistive load. Figure 20 shows the soft-start waveforms measured under constant-current load.

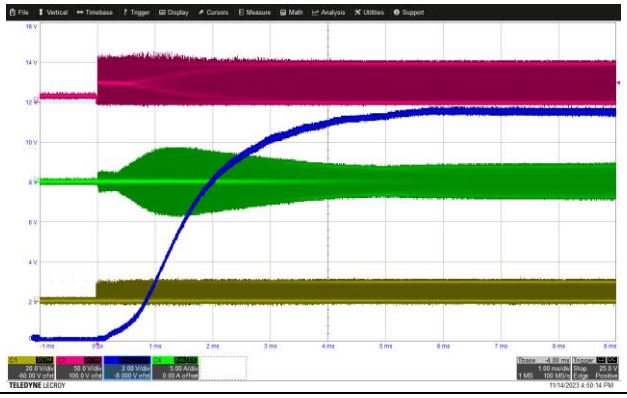




Ch.1= Primary Vgs(Q2) Ch.2= Primary Vds(Q2) Ch.3= Secondary Vgs(Q18) Ch.4= Resonant current(1:10)

Start-up waveforms at V_{in} = 36 V and I_{out} = 0 A	Start-up waveforms at V_{in} = 36 V and I_{out} = 80 A





Ch.1= Primary Vgs(Q2) Ch.2= Primary Vds(Q2) Ch.3= Secondary Vgs(Q18) Ch.4= Resonant current(1:10)

Start-up waveforms at V_{in} = 42 V and I_{out} = 0 A	Start-up waveforms at V_{in} = 42 V and I_{out} = 80 A

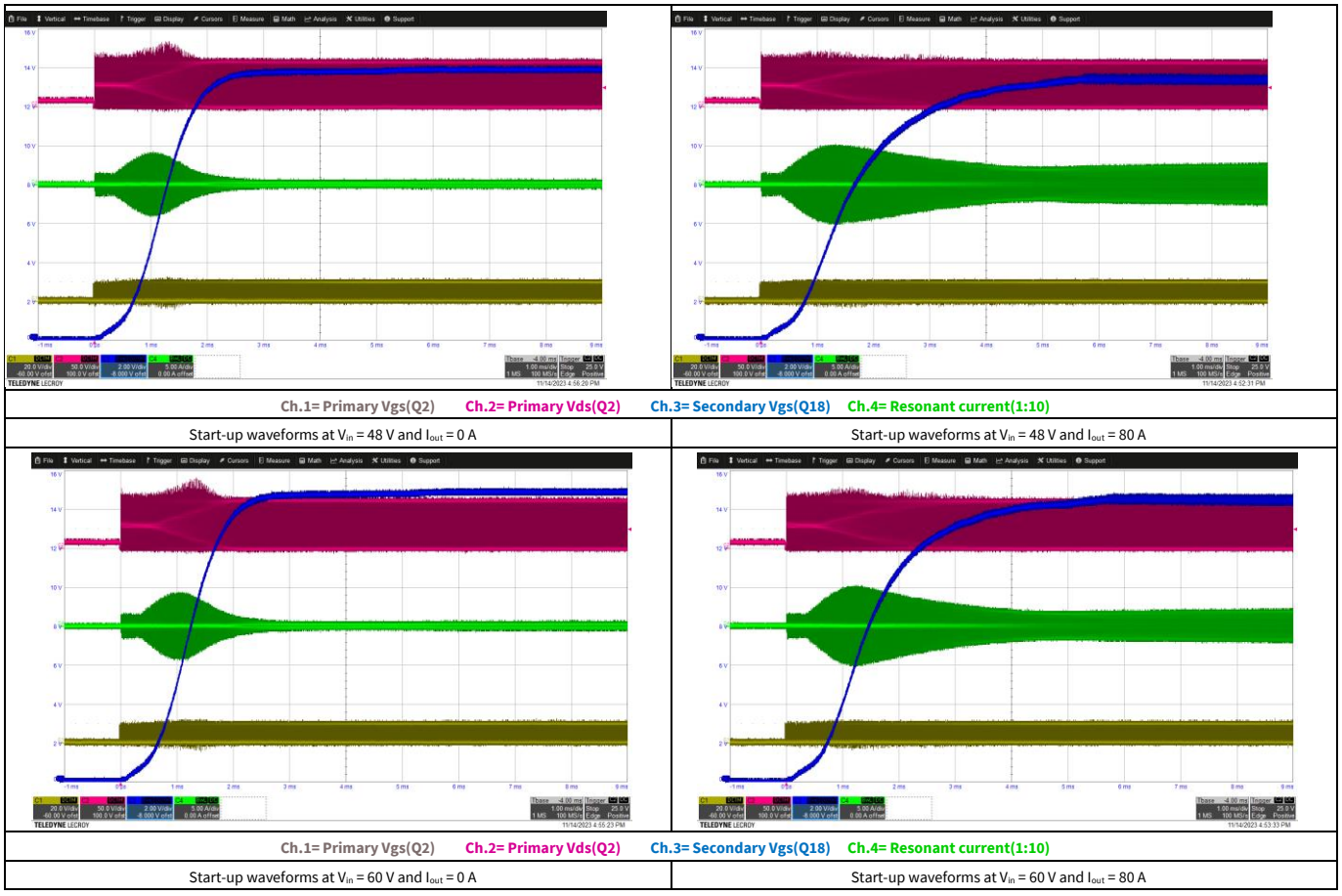
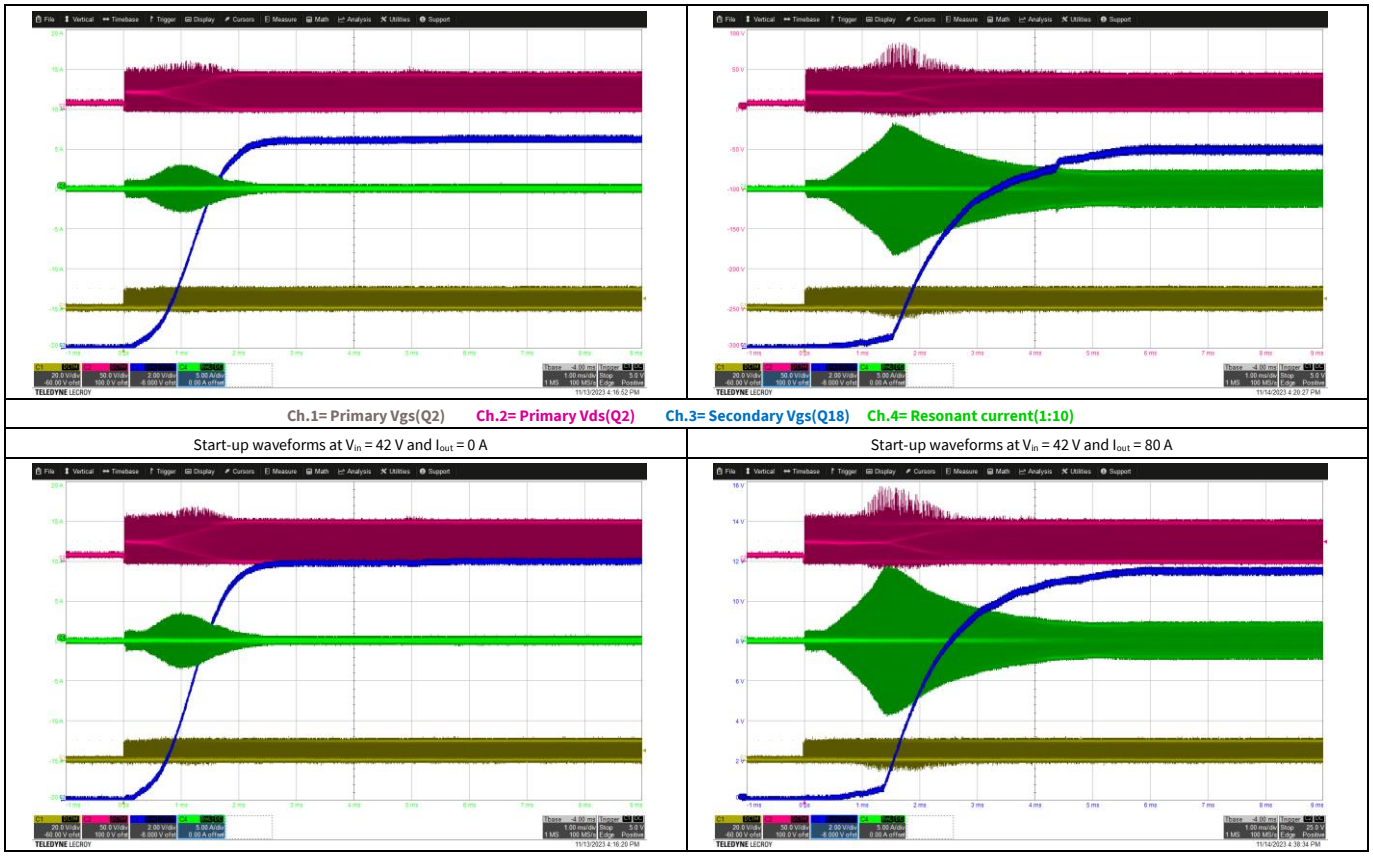


Figure 19 Start-up waveforms under resistive load



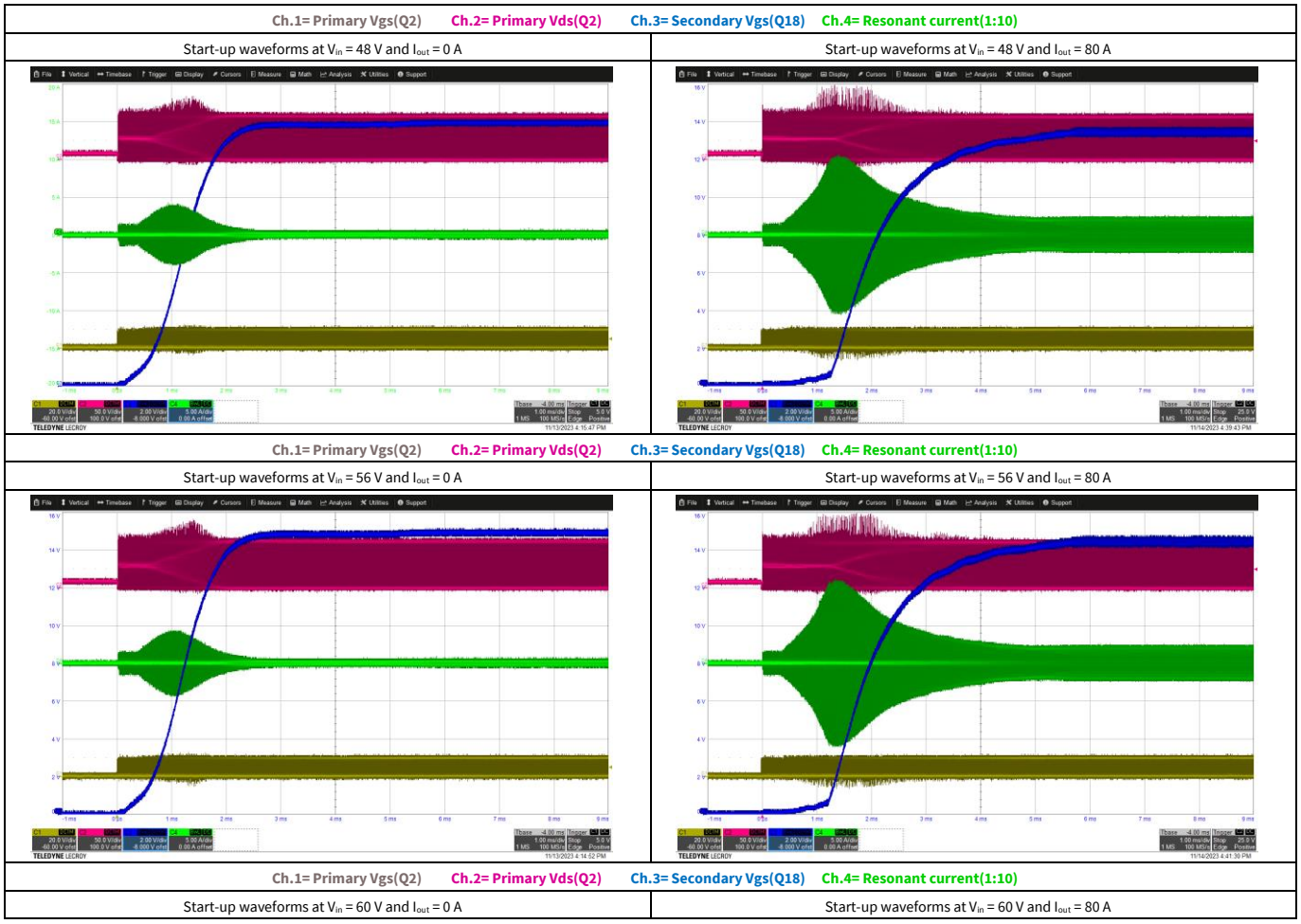
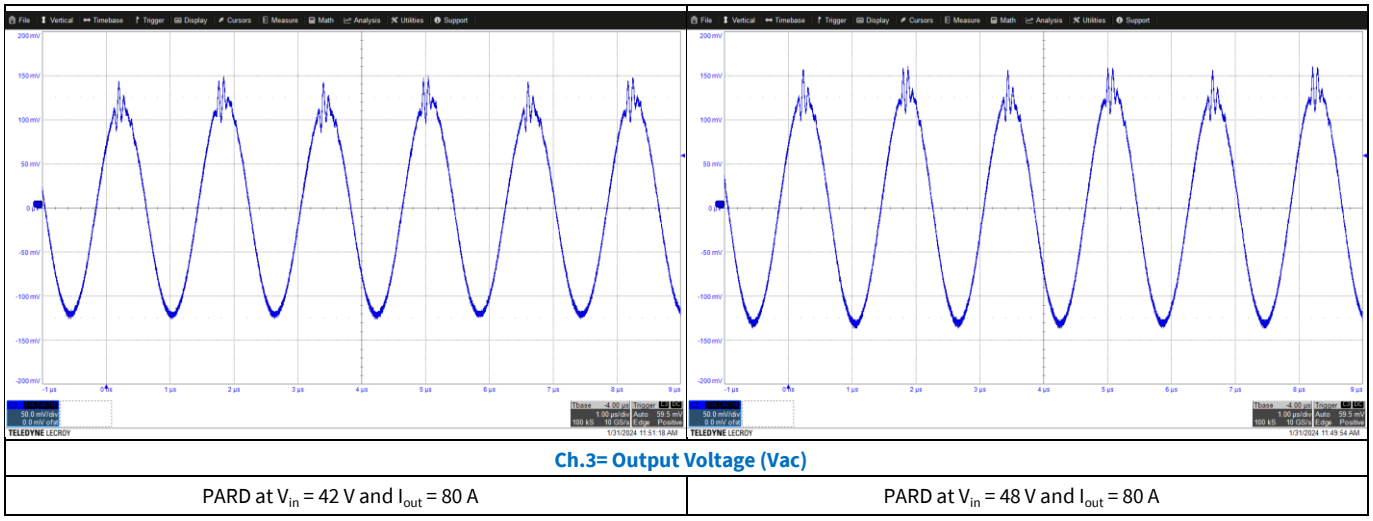
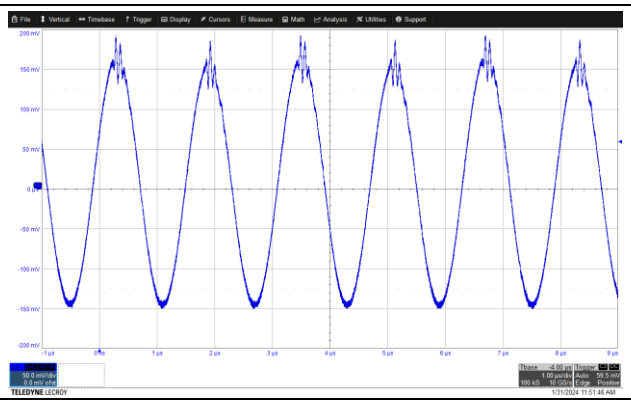


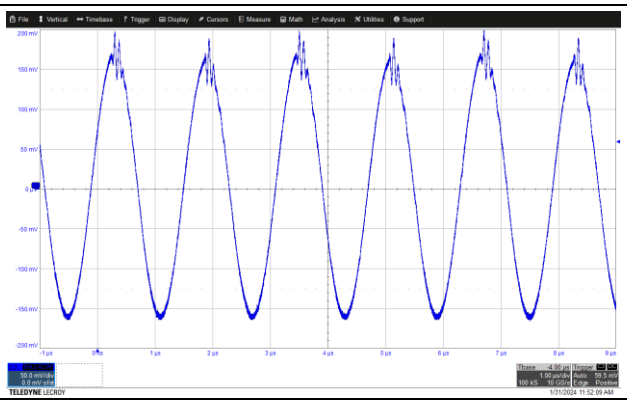
Figure 20 Start-up waveforms under constant-current load

3.3 Output PARD

Figure 21 shows the output periodic and random deviation (PARD) over a wide line and load range. The typical output PARD (peak-to-peak) is 280 mV at V_{in} = 48 V full load.







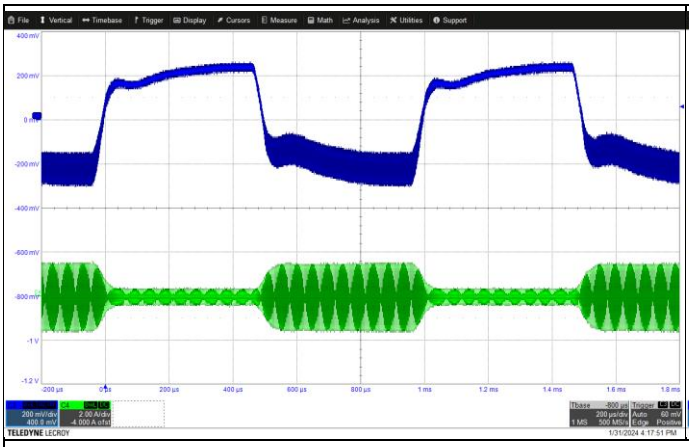
Ch.3= Output Voltage (Vac)

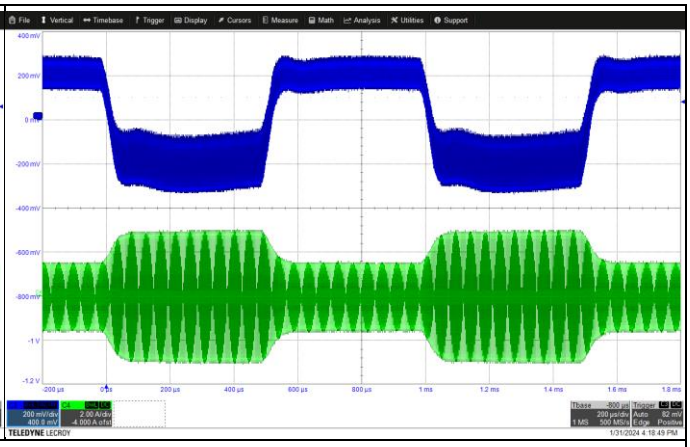
PARD at V_{in} = 56 V and I_{out} = 80 A	PARD at V_{in} = 60 V and I_{out} = 80 A

Figure 21 Output PARD waveforms

3.4 Load-transient response

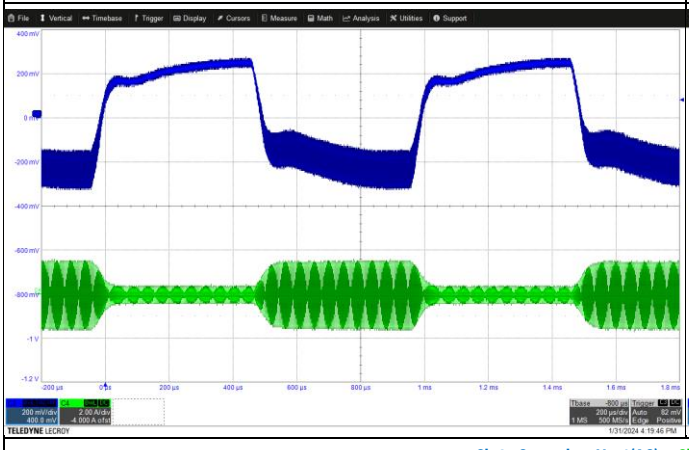
Figure 22 shows the output load-transient waveforms over a wide line and load range. Note that the converter is unregulated. The maximum output voltage deviation is 680 mV (transition from 50 percent load to 100 percent load at 1 A/µs slew rate).

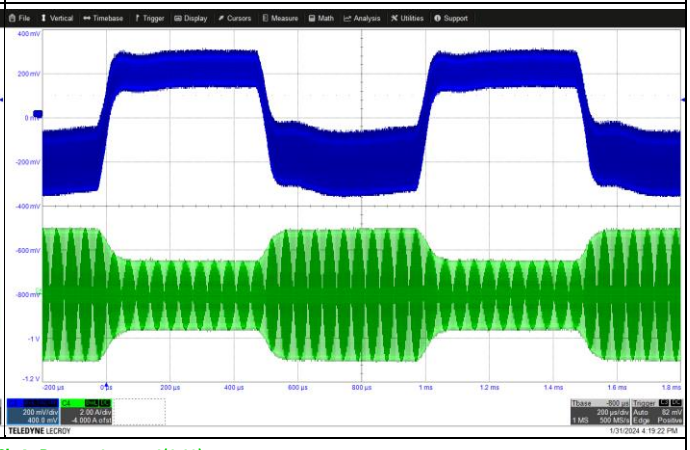




Ch.3= Secondary Vout(AC) Ch.4= Resonant current(1:10)

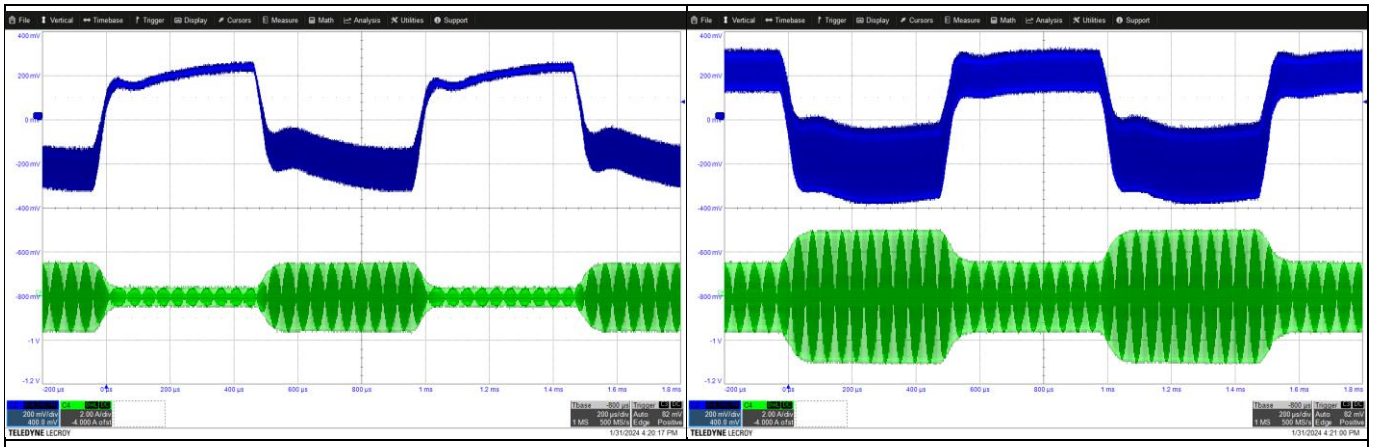
Transient waveforms at V_{in} = 42 V from I_{out} = 0A - 40 A with 1A/ µs	Transient waveforms at V_{in} = 42 V from I_{out} = 40A - 80 A with 1A/ µs





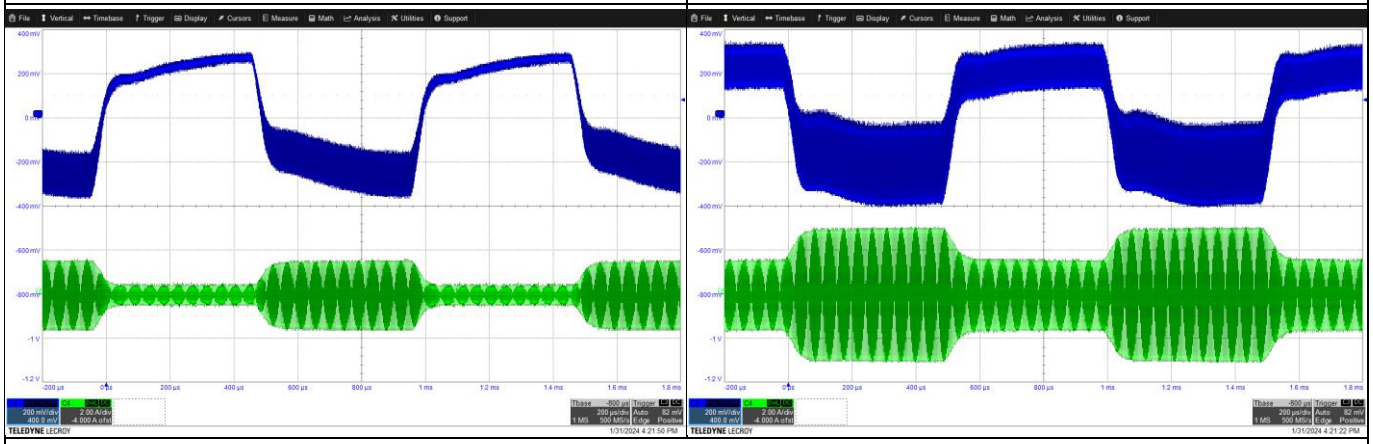
Ch.3= Secondary Vout(AC) Ch.4= Resonant current(1:10)

Transient waveforms at V_{in} = 48 V from I_{out} = 0A - 40 A with 1A/ µs	Transient waveforms at V_{in} = 48 V from I_{out} = 40A - 80 A with 1A/ µs



Ch.3= Secondary Vout(AC) Ch.4= Resonant current(1:10)

Transient waveforms at V_{in} = 56 V from I_{out} = 0A - 40 A with 1A/ µs	Transient waveforms at V_{in} = 56 V from I_{out} = 40A - 80 A with 1A/ µs



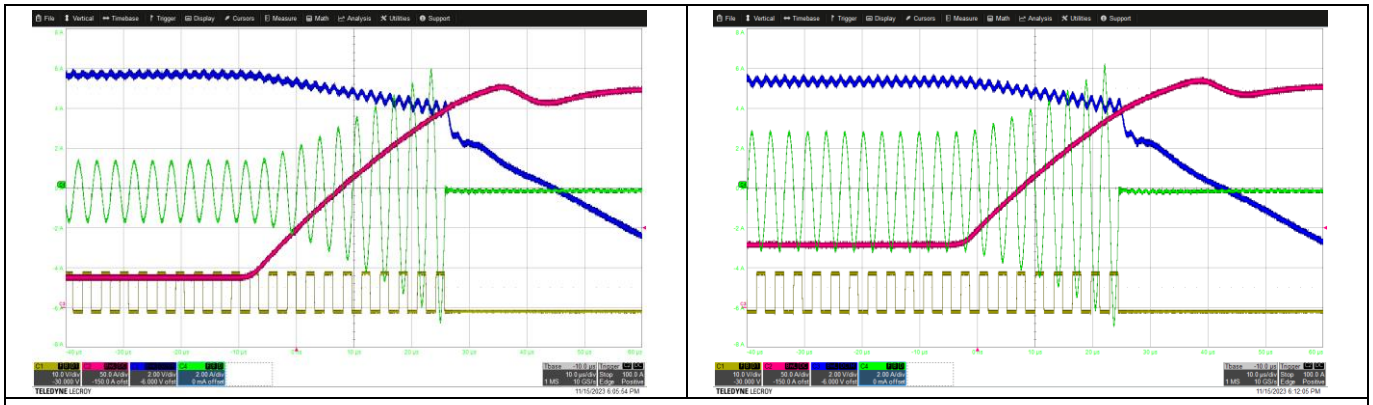
Ch.3= Secondary Vout(AC) Ch.4= Resonant current(1:10)

Transient waveforms at V_{in} = 60 V from I_{out} = 0A - 40 A with 1A/ µs	Transient waveforms at V_{in} = 60 V from I_{out} = 40A - 80 A with 1A/ µs

Figure 22 Load-transient waveforms

3.5 Output SCP

The output is shorted using a DC breaker in the test. Figure 23 shows the output SCP. The converter is protected by shutting off the PWMs when the secondary current through the PCB copper shunt goes over the SCP threshold. In the test, the SCP threshold is 90 A. The corresponding peak resonant current is about 37 A at the SCP threshold. Note that the output short-circuit current (the red waveform) is mostly provided by the large output capacitor on the fixture.



Ch.1= Primary Vgs(Q2) Ch.2= Output short-circuit current Ch.3= Output voltage Ch.4= Resonant current(1:10)

Output short-circuit occurs at V_{in} = 48 V and I_{out} = 40 A	Output short-circuit occurs at V_{in} = 48 V and I_{out} = 80 A

Figure 23 Output SCP

3.6 Efficiency

Table 3 shows the efficiency over a wide line and load range. The efficiency is measured under 600 FPM air flow. The efficiency curves are provided in Figure 24. The output voltage range across the load and applied input voltage are provided in Figure 25.

Table 3 Measured efficiency (percentage)

Output current	V_{in} = 42 V	V_{in} = 48 V	V_{in} = 56 V	V_{in} = 60 V
10 A	95.19	95.14	94.86	94.63
20 A	96.90	96.94	96.88	96.78
30 A	97.11	97.37	97.30	97.30
40 A	97.03	97.32	97.36	97.38
50 A	96.77	97.03	97.31	97.37
60 A	96.40	96.72	96.98	97.07
70 A	95.98	96.36	96.69	96.81
80 A	95.53	95.97	96.35	96.50

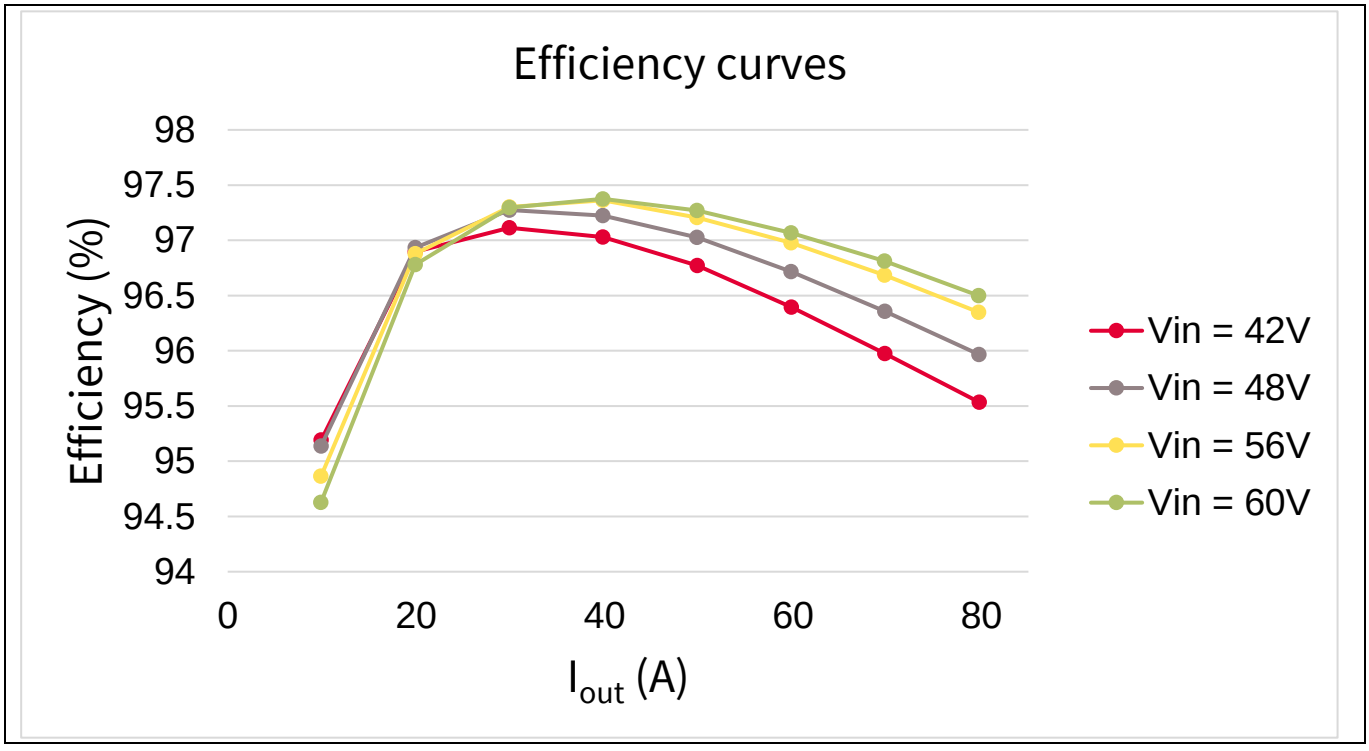


Figure 24 Efficiency graph over line and load range

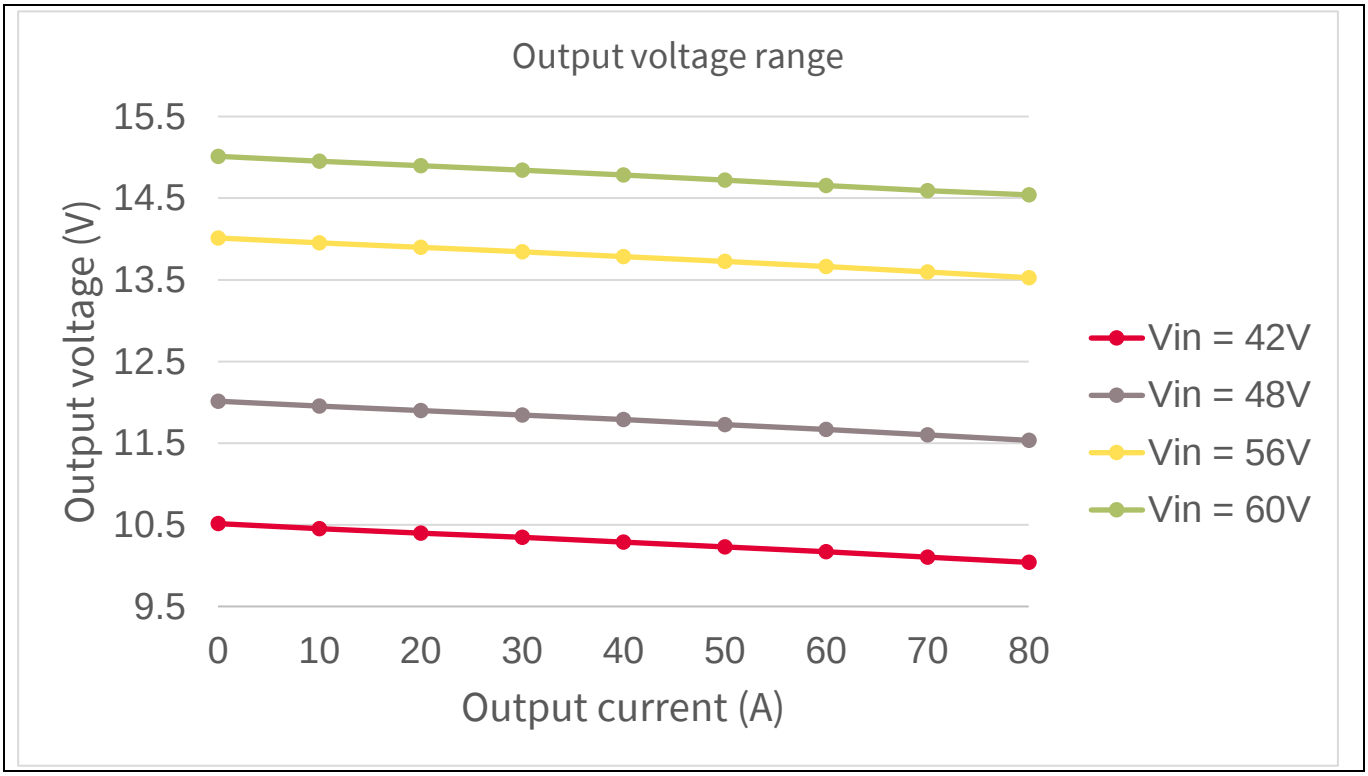


Figure 25 Output voltage across the load and input voltage

3.7 Thermal images

Figure 26 to Figure 29 shows the thermal images over a wide line and load range. The air flow is 600 FPM (with 7.5 V bias on the fan).

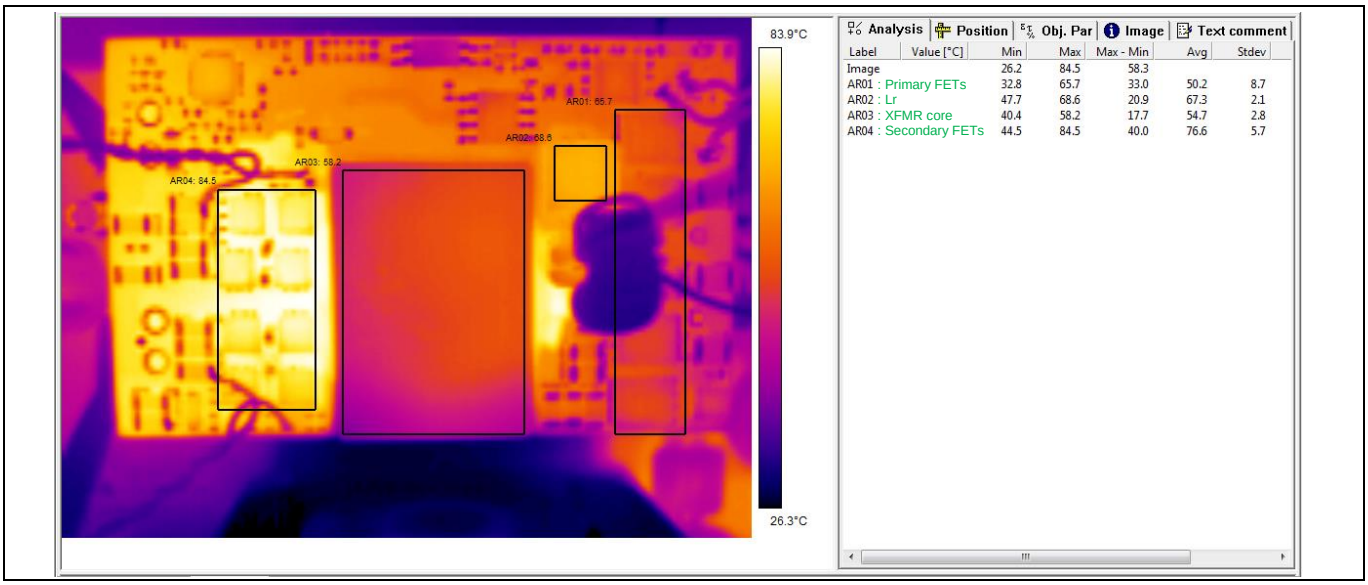


Figure 26 Thermal image taken at V_{in} = 42 V and I_{out} = 80 A

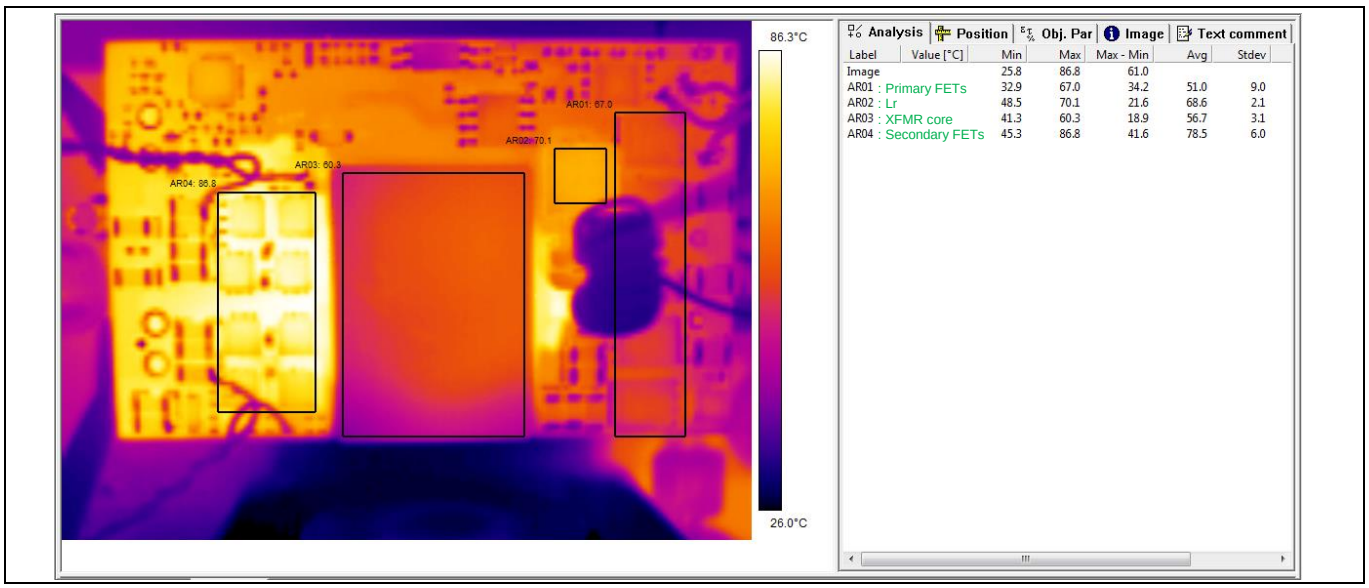


Figure 27 Thermal image taken at V_{in} = 48 V and I_{out} = 80 A

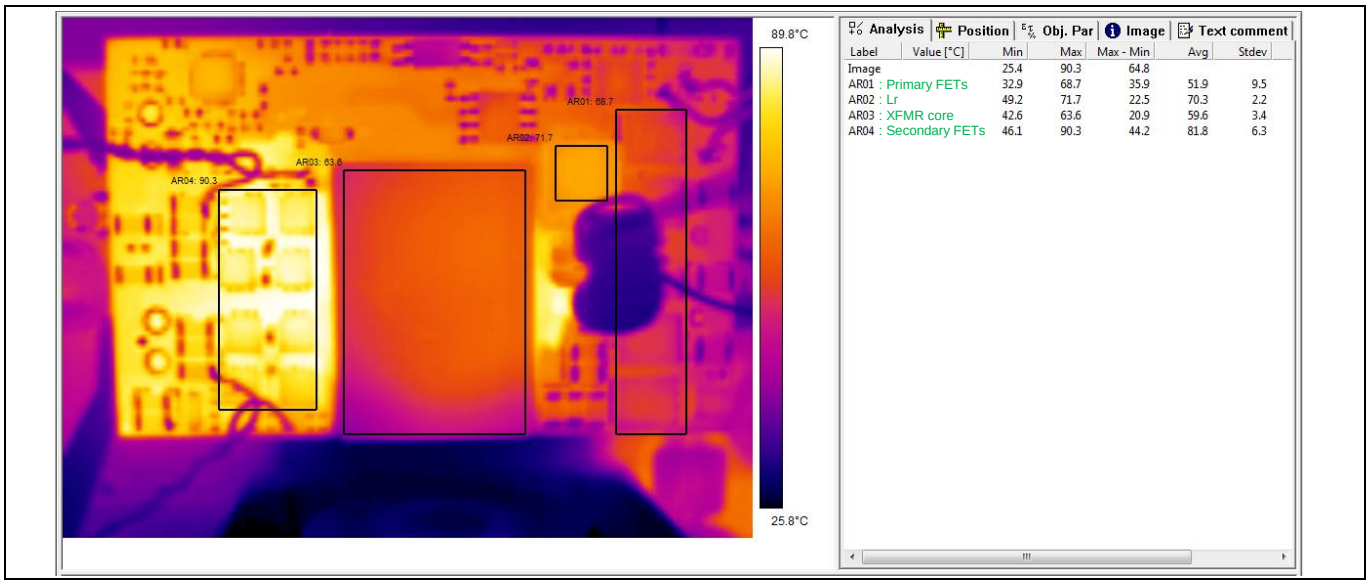


Figure 28 Thermal image taken at V_{in} = 56 V and I_{out} = 80 A

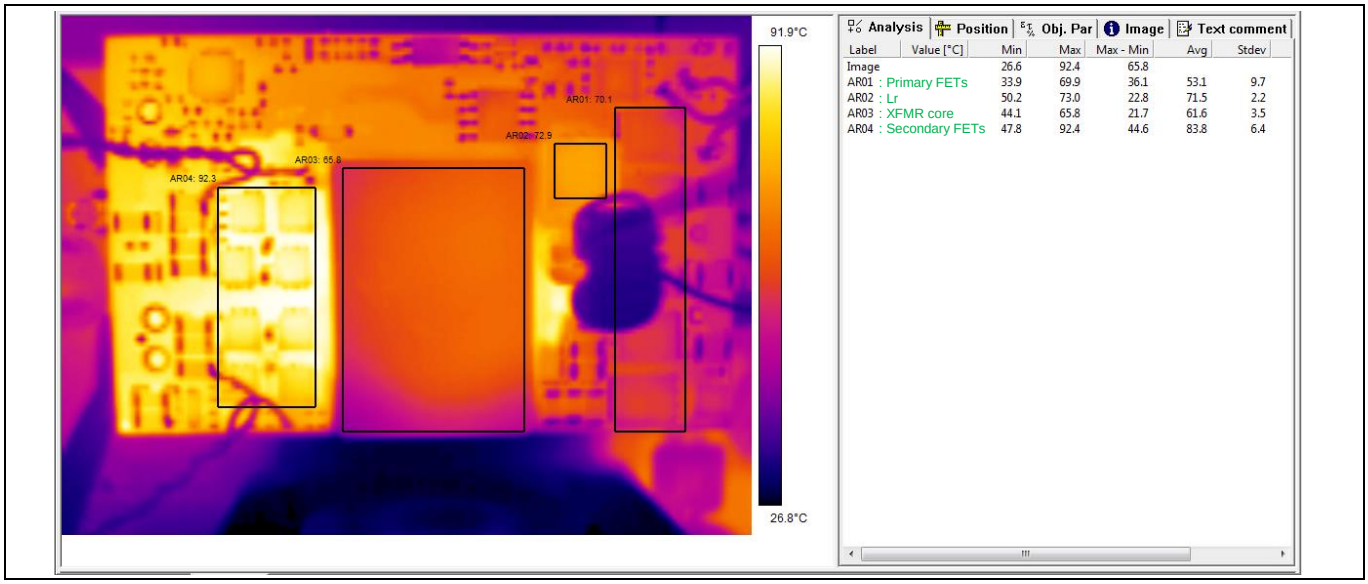


Figure 29 Thermal image taken at V_{in} = 60 V and I_{out} = 80 A

4 Summary

This document describes a complete Infineon solution for a 1 kW fixed-frequency LLC quarter-brick converter. The reference board has a standard DOSA-compliant quarter-brick footprint and achieves 97.3 percent peak efficiency and power density of 564 W/in^3 (34.6 W/cm^3), which are enabled by the outstanding performance of Infineon's semiconductor devices.

The primary OptiMOS™ 6 80 V MOSFET (ISC031N08NM6) has an excellent FOM and superior switching performance. The low output capacitance reduces the required magnetizing current for ZVS operation in the LLC converter, minimizing circulating losses. The secondary OptiMOS™ 5 25 V MOSFET (IQE006NE2LM5) has an industry-leading $R_{DS(on)}$, significantly lowering the conduction losses of SRs in the LLC converter. The reduced form factor (PQFN 3.3 mm × 3.3 mm footprint) enables more FETs to be paralleled in the same space, which further reduces conduction losses and offers superior thermal management. Both the primary and secondary FETs are driven by Infineon's 2EDL8034-G3C EiceDRIVER™ gate driver in SON-10 3 mm × 3 mm package. Infineon's 2DIB0410F ISOFACE™ dual-channel digital isolator with coreless technology provides high noise immunity and robust isolated communication to drive the primary gate drivers.

Infineon's digital power controller XDPP1100-Q024 plays an essential role in optimal PWM timing generation, duty-cycle/frequency hybrid soft-start implementation, and enhanced protection in the fixed-frequency LLC quarter-brick converter. The industry's smallest digital power controller offers many optimized power processing blocks and pre-programmed peripherals, which enhances the performance of isolated DC-DC converters, reduces external components, and minimizes firmware development effort.

5 Appendix

5.1 Mechanical outline

Figure 30 shows the mechanical outline for the 1 kW fixed-frequency LLC quarter-brick converter.

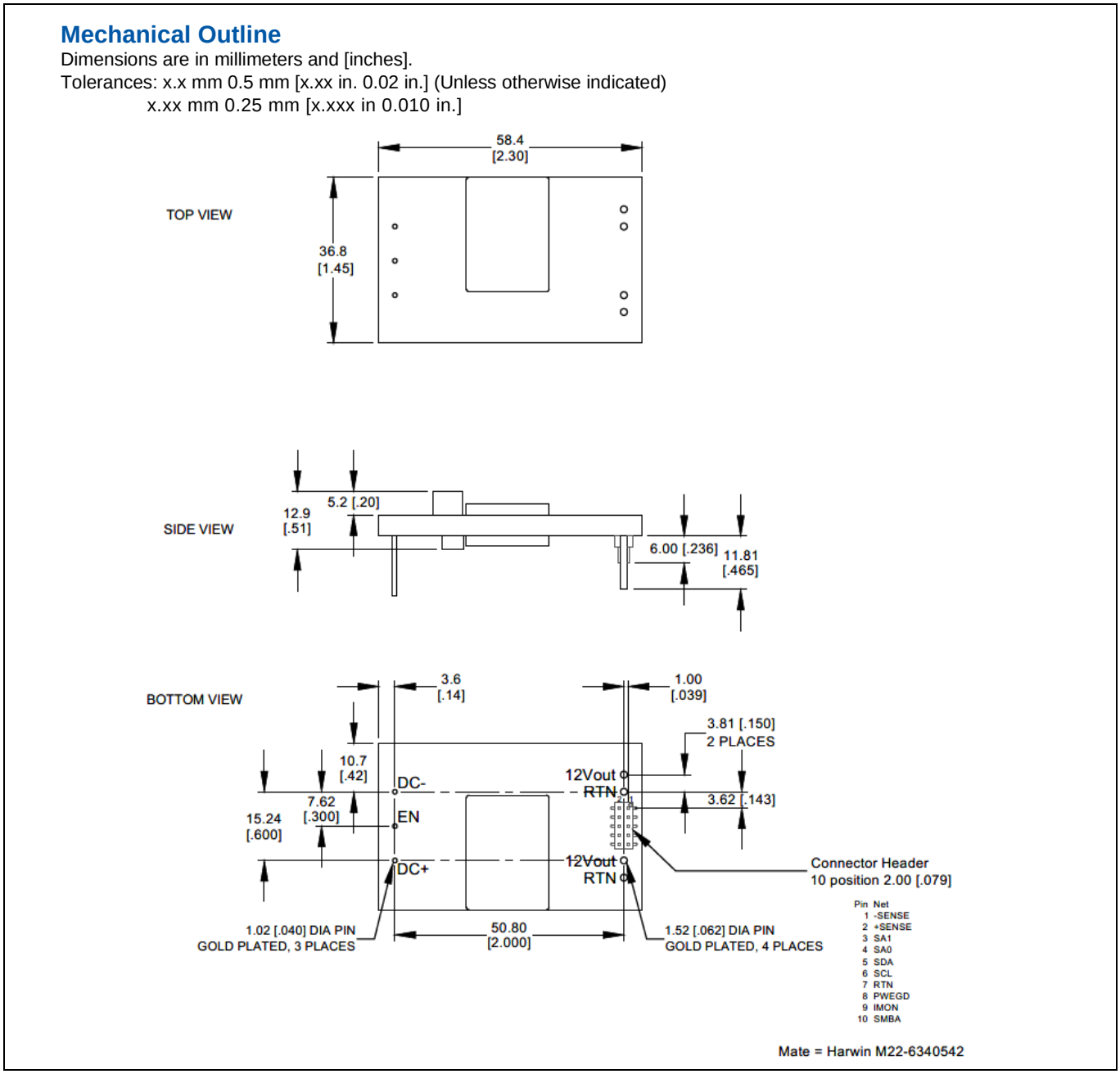


Figure 30 Mechanical outline

5.2 Bill of materials

Table 4 BOM

Item	Qty.	Ref.	Manufacturer	Part number
1	1	BRD1	–	P100119 C
2	8	C1, C2, C3, C4, C5, C6, C7, C8	TDK	C3225X7R2A225K230AM
3	9	C9, C10, C17, C24, C58, C66, C69, C74, C88	TDK	C1608X7R1H104K080AA
4	1	C11	TDK	C3216NP02A333J160
5	8	C12, C51, C60, C77, C78, C80, C81, C82	Murata	GRM31C5C1H224JE02L
6	5	C13, C18, C20, C31, C73	TDK	C1608C0G2A101K080AA
7	2	C14, C21	TDK	C1608X7R1H103K080AA
8	3	C15, C23, C57	Samsung	CL21B106KOQNNNE
9	1	C16	Kemet	C0603C472K2RACTU
10	1	C19	TDK	C3216C0G2A104J160AE
11	2	C22, C79	TDK	C1608X7R1H223K080AA
12	6	C25, C26, C56, C67, C75, C76	TDK	C1608X7R1E105K080AB
13	1	C27	Kemet	C1206C102JGRACTU
14	20	C28, C29, C30, C32, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C85, C86, C87	TDK	CGA5L1X8L1E106K160AC
15	1	C33	TDK	Not Used
16	6	C47, C48, C49, C50, C53, C64	TDK	C1608X7R1H224K080AB
17	2	C70, C72	TDK	C1608C0G2A102J080AA
18	2	C83, C84	–	Not Used
19	1	DS1	Würth	150060GS75000
20	2	D1, D3	On	BAS20HT1G
21	1	D2	On	MBR2H100SFT3G
22	1	D13	On	MM5Z5V1T1G
23	2	D16, D24	NXP	BAS516, 135
24	4	D18, D19, D33, D43	Toshiba	CRH01(TE85L, Q, M)
25	1	D44	ON	MM5Z5V6T1G
26	1	J1	Harwin	M22-5320505
27	1	Lr	ICE	LP02-800-1S
28	8	Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8	Infineon	ISC031N08NM6
29	16	Q9, Q10, Q11, Q12, Q13, Q14, Q15, Q16, Q17, Q18, Q19, Q20, Q21, Q22, Q23, Q24	Infineon	IQE006NE2LM5ATMA1
30	1	RT2	Murata	NCP15WB473F03RC
31	1	R1	Panasonic	ERJ-3EKF3011V
32	3	R2, R70, R71	Panasonic	ERJ-3EKF1001V
33	9	R3, R4, R16, R20, R23, R26, R27, R28, R29	Panasonic	ERJ-3EKF1002V

Item	Qty.	Ref.	Manufacturer	Part number
34	4	R5, R6, R65, R87	Panasonic	ERJ-3EKF2001V
35	1	R7	Panasonic	ERJ-8ENF1500V
36	1	R9	Panasonic	ERA-3AEB103V
37	1	R10	Panasonic	ERA-3AEB112V
38	1	R12	Panasonic	ERJ-3EKF1202V
39	2	R13, R96	Panasonic	ERJ-3EKF20R0V
40	1	R14	Panasonic	ERJ-3EKF3321V
41	1	R15	Panasonic	ERJ-3EKF2002V
42	3	R17, R21, R22	Panasonic	ERJ-3EKF1000V
43	3	R18, R69, R73	Panasonic	Not Used
44	1	R19	Panasonic	ERJ-3EKF2550V
45	4	R24, R25, R61, R89	Panasonic	ERJ-3GEY0R00V
46	24	R30, R31, R32, R38, R39, R40, R43, R44, R45, R46, R49, R50, R51, R52, R53, R54, R55, R56, R58, R63, R76, R77, R79, R80	Panasonic	ERJ-3RQF1R0V
47	1	R33	Panasonic	ERJ-3EKF51R1V
48	1	R34	Panasonic	ERA-3AEB104V
49	1	R35	Panasonic	ERA-3AEB132V
50	1	R36	Panasonic	ERJ-3EKF2213V
51	1	R37	Panasonic	ERJ-3EKF4871V
52	1	R47	Panasonic	ERJ-3EKF9531V
53	1	R48	Panasonic	ERJ-3EKF1741V
54	1	R57	Panasonic	ERJ-3EKF1243V
55	1	R62	Panasonic	ERJ-3EKF22R0V
56	2	R64, R81	Panasonic	ERJ-6RQF1R0V
57	2	R66, R86	Panasonic	ERJ-3EKF10R0V
58	1	R72	Panasonic	ERJ-3EKF1272V
59	1	R82	Panasonic	ERJ-6ENF5110V
60	1	R85	Panasonic	ERJ-6ENF2002V
61	10	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10	HARWIN	S2761-46R
62	1	T1	Proterial	EQ25-ML27D and PLT-ML27D
63	1	T3	Coilcraft	LPD5030V-224MR_B
64	1	U1	Infineon	XDPP1100-Q024
65	4	U2, U4, U5, U13	Infineon	2EDL8034-G3C
66	1	U10	TI	OPA140AIDBVT
67	1	U11	TI	LM5018SD/NOPB
68	1	U14	Infineon	2DIB0401F

Item	Qty.	Ref.	Manufacturer	Part number
69	1	U20	LT	LT1460KCS3-3.3#TRMPBF
70	1	U21	Fairchild	FODM8801A
71	1	W1	Belden	8019 000100
72	3	1, 2, 3	Mil Max	3104-3-00-15-00-00-08-0
73	4	4, 5, 9, 10	Mil Max	4357-0-00-15-00-00-03-0

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[5] Infineon Technologies AG: *Digital power controller XDPP1100,* Datasheet; Available online.

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Revision history

Document revision	Date	Description of changes
V 1.0	2020-09-30	First release
V 1.1	2020-10-30	Added power loss analysis
V 1.2	2024-02-01	Introduce EiceDRIVER™ gate driver 2EDL803X-G3C, and 2DIB0410F ISOFACE™ dual-channel digital isolator

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