XDPL8218 design guide

For high power factor flyback converter with constant voltage output

About this document

Scope and purpose

This document is a design guide using XDPL8218 as the control IC of the front-stage High Power Factor (HPF) flyback converter, which regulates the secondary output voltage supply to the second-stage Constant Current (CC) converter for LED lighting applications.

Intended audience

Power supply design engineers, field application engineers.

Table of contents

About this document **1**
Table of contents **1**
1 Introduction **3**
2 Design specifications **5**
3 Transformer design **6**
4 Flyback MOSFET and secondary main output diode selection **8**
5 CS resistor and GD pin-related design **10**
6 MOSFET maximum current cycle-by-cycle limit and start-up phase design **11**
7 HV pin-related design **14**
8 V_{CC} capacitance and output UVP design **15**
9 Output OVP-related design **17**
10 DC link filter and secondary main output capacitance **18**
11 Input voltage levels for start-up and protection **19**
12 ZCD pin-related design **20**
13 Secondary-side regulation FB circuit design **22**
14 Regulated mode parameters **26**
14.1 Digital notch filter 26
14.2 On-time limit and switching frequency limit (QRM1/DCM) 26
14.3 ABM FB voltage sensing and control 27
14.4 FB voltage mapping and mode transition 28
14.5 FB voltage maximum limit ramp 29
15 Other protection-related parameters **30**
15.1 V_{CC} OVP 30
15.2 Regulated mode V_{CC} UVP 30
15.3 IC over-temperature protection 30
15.4 Primary MOSFET over-current protection 30
15.5 Debug mode 31
16 PCB layout guide **32**

17 Parameter configuration list, set-up and procedures 33
17.1 Parameter configuration list 33
17.2 Parameter configuration set-up 34
17.3 Parameter configuration procedures 35
18 Fine-tuning guide 38
18.1 Input voltage-sensing parameter fine-tuning 38
18.2 QR valley switching parameter fine-tuning 39
18.3 Input power quality related parameter fine-tuning 41
19 Debugging guide 42
19.1 Pin signal debugging 42
19.2 Firmware status code read-out procedures with debug mode 45
20 References 46
Revision history 47

1 Introduction

XDPL8218 regulates Constant Voltage (CV) output of a HPF flyback converter, according to its feedback (FB) pin voltage signal, which is controlled by the secondary-side regulation FB circuit via an isolated optocoupler, as shown in **Figure 1**.

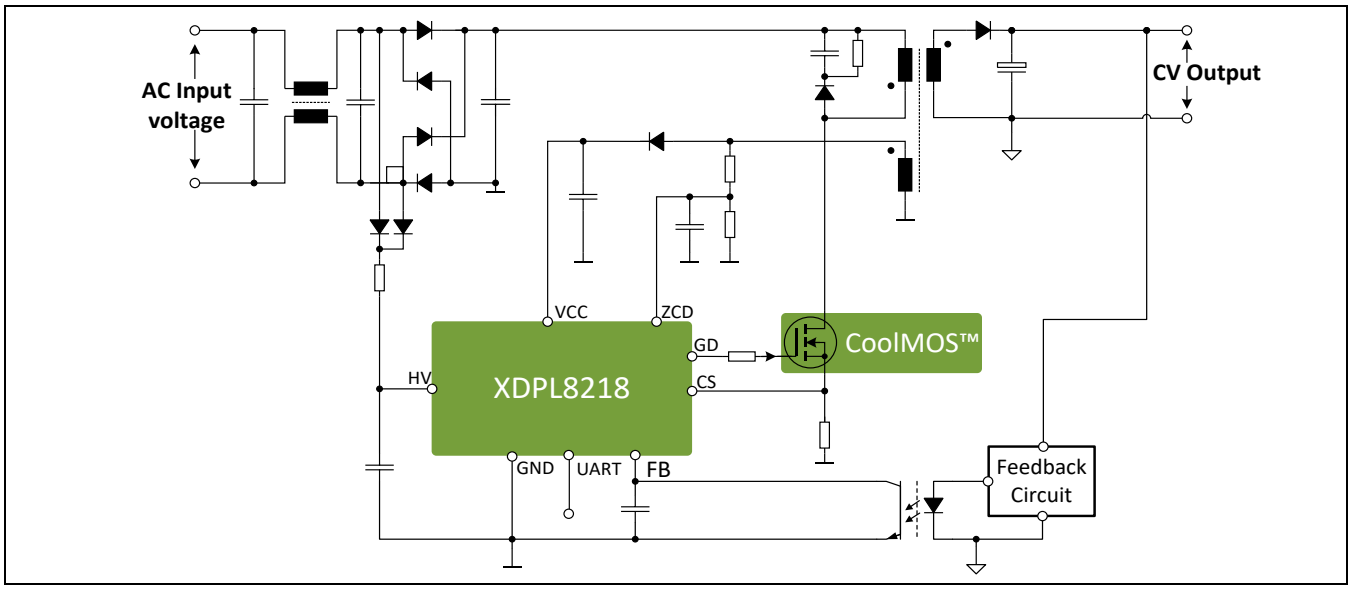


Figure 1 XDPL8218 flyback converter simplified circuitry with secondary-side regulated CV output

For LED lighting applications, XDPL8218 flyback CV output usually is converted to a CC output by a second-stage DC-DC switching or linear regulator.

XDPL8218 comes in a PG-DSO-8 package with eight pins, as shown in the datasheet [1]. The main functions of each pin are shown in **Table 1**.

Table 1 XDPL8218 pins assignment

Pin	Symbol	Type	Pin name and main functions
1	ZCD	Input	Zero Crossing Detection pin: • Transformer auxiliary winding ZCD via external resistor/divider • Sensing of the reflected input and output voltage signals from auxiliary winding via external resistors divider
2	FB	Input	Feedback pin: • Feedback voltage sensing for secondary-side output regulation
3	CS	Input	Current Sense pin: • Flyback MOSFET current sensing via external shunt resistor
4	GD	Output	Gate Drive pin: • Flyback MOSFET gate-drive control via external series resistor
5	HV	Input	High Voltage pin: • V_{CC} charging via its internal 600 V start-up cell during start-up and protection • Rectified AC input voltage sensing via external series resistor for line synchronization

Pin	Symbol	Type	Pin name and main functions
6	UART	Input /Output	Universal Asynchronous Receiver Transmitter pin: • Digital communication interface for IC parameter configuration
7	V_{CC}	Input	Voltage at Common Collector pin: • IC operating voltage supply and sensing
8	GND	–	Ground pin: • IC grounding

XDPL8218's IC parameters are configurable digitally via its UART interface, using Infineon's user-friendly Graphical User Interface (GUI) on a PC. This enables a lower Bill of Materials (BOM) and rapid engineering changes without the need for complex component design iterations.

Note: By default, the configurable parameters of a new XDPL8218 chip from Infineon are empty, so it is necessary to configure them before any application testing.

Figure 2 shows the XDPL8218 design guide document sectioning for each step of the recommended design flow.

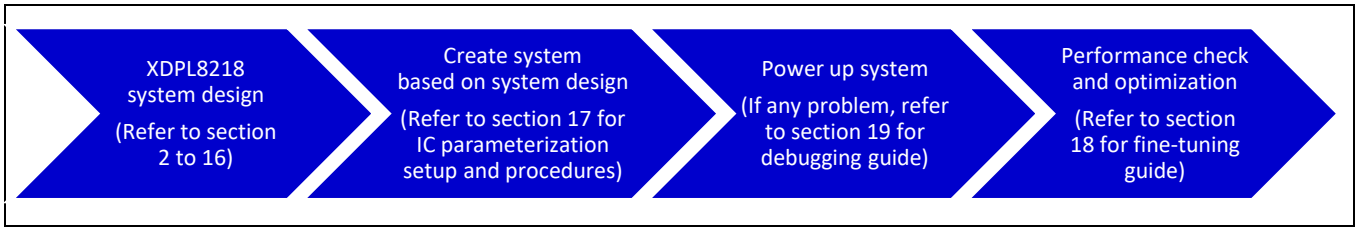


Figure 2 XDPL8218 design guide document sectioning for each step of the recommended design flow

2 Design specifications

A front-stage HPF flyback converter with CV output set-point $V_{out,setpoint}$ of 54 V (54 V/0.8 A) has been selected as a design example. The design specifications are shown in **Table 2**.

Table 2 Design specifications

Specification	Symbol	Value	Unit
Normal operational minimum AC input voltage	$V_{AC,min}$	90	V_{rms}
Normal operational maximum AC input voltage	$V_{AC,max}$	305	V_{rms}
Normal operational AC input frequency	F_{line}	47 ~ 63	Hz
Secondary-side regulated CV output set-point	$V_{out,setpoint}$	54	V
Steady-state output load current	I_{out}	0 ~ 800	mA
Steady-state full-load output power	$P_{out,full}$	43.2	W
Minimum efficiency at $P_{out,full}$	$\eta_{min,at,P,out,full}$	90	%
Target minimum switching frequency at $P_{out,full}$	$f_{sw,min,at,P,out,full}$	52	kHz

Note: $P_{out,full}$ of 43.2 W is defined in this design example, to be able to supply a second-stage CC converter which has minimum efficiency of 93 percent (or maximum 3.2 W loss) at full load, for a 40 W LED driver design.

Note: The recommended $f_{sw,min,at,P,out,full}$ is between 50 kHz and 65 kHz. In general, higher $f_{sw,min,at,P,out,full}$ value would result in a smaller flyback transformer with lower efficiency, while lower $f_{sw,min,at,P,out,full}$ value would result in a larger flyback transformer with higher efficiency.

3 Transformer design

To achieve both high efficiency and high power quality in QR Mode with first valley switching (QRM1), the flyback transformer primary main winding to secondary main winding turns ratio, N, should be high enough, but without exceeding the flyback MOSFET drain-source breakdown voltage $V_{(BR)DSS}$. Based on the $V_{AC,max}$ requirement of 305 V_{rms}, MOSFET **$V_{(BR)DSS}$ = 800 V** is selected for a good price to performance ratio.

To reduce transformer leakage inductance for low MOSFET voltage spike $V_{spike,FET}$, transformer design with sandwich construction as shown in **Figure 3** is highly recommended. Additionally, with the primary RCD snubber network deployed across the primary main winding (see **Figure 1**), $V_{spike,FET}$ can be estimated to be around 30 percent to 45 percent of $V_{AC,max}$ as a rule of thumb. In this design example, $V_{AC,max}$ is 305 V_{rms}, so we simply assume $V_{spike,FET}$ as an absolute number of 100 V, which is approximately 33 percent of $V_{AC,max}$.

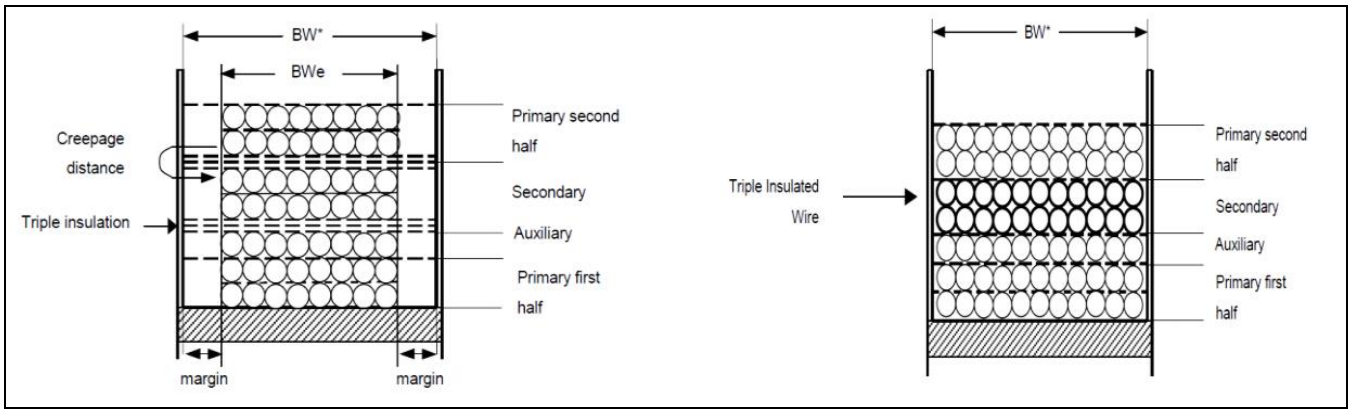


Figure 3 Transformer design with sandwich construction

For good reliability against input voltage surge, it is recommended to reserve a voltage margin $V_{margin,FET}$ of minimum 50 V from $V_{(BR)DSS}$. If XDPL8218 input Over-Voltage Protection (OVP) would be enabled later in **Section 10**, as a rule of thumb, $V_{margin,FET}$ should be at least 25 percent of $V_{AC,max}$, which is equivalent to 76.25 V based on $V_{AC,max}$ of 305 V_{rms}. In this design example, $V_{margin,FET}$ of 90 V is selected.

Based on the above, N can be defined as:

$$N \leq \frac{V_{(BR)DSS} - V_{AC,max(pk)} - V_{spike,FET} - V_{margin,FET}}{V_{out,setpoint} + V_d} \quad (1)$$

Where $V_{AC,max(pk)}$ is √2 times $V_{AC,max}$, and V_d is the secondary main output diode forward voltage.

Taking V_d = 0.7 V, N can then be calculated as:

$$N \leq \frac{800 - \sqrt{2} \cdot 305 - 100 - 90}{54 + 0.7} = 3.27$$

Based on the above, **N = 3.2** is selected.

The maximum primary peak current $I_{pri(pk),max}$ can then be defined and calculated as:

$$I_{pri(pk),max} \approx \frac{4 \cdot P_{out,full}}{\eta_{min,at,P,out,full}} \cdot \left[\frac{1}{N \cdot (V_{out,setpoint} + V_d)} + \frac{1}{V_{AC,min(pk)}}\right] \quad (2)$$

Where $V_{AC,min(pk)}$ is √2 times $V_{AC,min}$.

$$I_{pri(pk),max} \approx \frac{4 \cdot 43.2}{90\%} \cdot \left[\frac{1}{3.2 \cdot (54 + 0.7)} + \frac{1}{\sqrt{2} \cdot 90}\right]$$

$$\boldsymbol{I_{pri(pk),max} \approx 2.606\ A}$$

As a result, the primary main winding inductance L_p can be defined and calculated as:

$$L_p = \frac{V_{AC,min(pk)} \cdot N \cdot (V_{out,setpoint} + V_d)}{I_{pri(pk),max} \cdot f_{sw,min,at,P,out,full} \cdot [V_{AC,min(pk)} + N \cdot (V_{out,setpoint} + V_d)]} \quad (3)$$

$$L_p = \frac{\sqrt{2} \cdot 90 \cdot 3.2 \cdot (54 + 0.7)}{2.606 \cdot 52 \cdot 10^3 \cdot [\sqrt{2} \cdot 90 + 3.2 \cdot (54 + 0.7)]}$$

$$\boldsymbol{L_p = 544\ \mu H}$$

Based on core cross-sectional area, A_e = 120.1 mm² and saturation flux density at 100°C, $B_{sat(T=100°C)}$ = 0.41 Tesla for TDG PQ26/20 core with TPW33 material, the transformer primary main winding turns N_p can be defined as:

$$N_p \geq \frac{L_p \cdot I_{pri(pk),max}}{A_e \cdot B_{sat(T=100°C)} \cdot D_{f,Bsat}} \quad (4)$$

Where $D_{f,Bsat}$ is the derating factor to ensure the designed transformer maximum flux density B_{max} is below $B_{sat(T=100°C)}$ by a margin of (100 percent - $D_{f,Bsat}$) from saturation, and it is typical to set $D_{f,Bsat}$ in the range of 85 percent to 95 percent for a margin of 5 percent to 15 percent from transformer core saturation.

Taking $D_{f,Bsat}$ = 90 percent, N_p can then be calculated as:

$$N_p \geq \frac{544 \cdot 10^{-6} \cdot 2.606}{120.1 \cdot 10^{-6} \cdot 0.41 \cdot 90\%} = 31.99$$

Based on the above, **N_p = 32** is selected.

The transformer secondary main winding turns N_s can then be calculated as:

$$N_s = \frac{N_p}{N} = \frac{32}{3.2}$$

$$\boldsymbol{N_s = 10}$$

To ensure fast V_{CC} supply takeover from the primary auxiliary winding for avoiding IC reset during start-up, and also to be able to deliver peak gate-drive voltage $V_{GD,peak}$ of 12 V with high enough primary auxiliary winding V_{CC} supply during steady-state, the minimum primary auxiliary winding demagnetization voltage $V_{a,min}$ is therefore defined as 14 V. As a result, the recommended minimum primary auxiliary winding turns $N_{a,min}$ can be defined and calculated as:

$$N_{a,min} = \frac{V_{a,min} \cdot N_s}{(V_{out,setpoint} + V_d)} = \frac{14 \cdot 10}{(54 + 0.7)} = 2.56 \quad (5)$$

To ensure proper HV pin line synchronization, V_{CC} voltage should be lower than 19 V, the maximum auxiliary winding demagnetization voltage $V_{a,max}$ is therefore defined as 19 V. As a result, the recommended maximum primary auxiliary winding turns $N_{a,max}$ can be defined and calculated as:

$$N_{a,max} = \frac{V_{a,max} \cdot N_s}{(V_{out,setpoint} + V_d)} = \frac{19 \cdot 10}{(54 + 0.7)} = 3.47 \quad (6)$$

Based on the calculation results of equations (5) and (6), primary auxiliary winding turns **N_a = 3** is selected.

A secondary auxiliary winding is added to supply the operating voltage of the Secondary Side Regulation (SSR) FB circuit, since its op-amp or shunt regulator's maximum operating voltage is less than $V_{out,setpoint}$ of 54 V. The recommended minimum secondary auxiliary winding turns $N_{a,sec,min}$ and recommended maximum secondary auxiliary winding turns $N_{a,sec,max}$ can be defined respectively as per $N_{a,min}$ and $N_{a,max}$, as shown below:

$$N_{a,sec,min} = N_{a,min} = 2.56 \quad (7)$$

$$N_{a,sec,max} = N_{a,max} = 3.47 \quad (8)$$

Based on the calculation results of equations (7) and (8), secondary auxiliary winding turns **$N_{a,sec}$ = 3** is selected.

4 Flyback MOSFET and secondary main output diode selection

The CoolMOS™ P7 MOSFET series is the latest CoolMOS™ product family and targets customers looking for high performance and at the same time being price sensitive. Through optimizing key parameters (C_{oss}, E_{oss}, Q_g, C_{iss} and $V_{GS(th)}$); integrating Zener diode for ESD protection and other measures, this product family fully addresses market concerns in performance, ease-of-use, and price/performance ratio, delivering best-in-class performance with exceptional ease-of-use, while still not compromising on price/performance ratio. The 700 V and 800 V CoolMOS™ P7 series have been designed for flyback and could also be used in PFC topologies.

MOSFET drain-source breakdown voltage **$V_{(BR)DSS}$ = 800 V** is selected in this design example based on $V_{AC,max}$ of 305 V_{rms} and transformer design in **Section 3**.

Before selecting which MOSFET drain-source on-resistance at room temperature $R_{ds(on),25°C}$ is to be used, the maximum primary rms current $I_{pri(rms),max}$ has to be estimated based on:

$$I_{pri(rms),max} \approx I_{pri(pk),max} \cdot \sqrt{\frac{k}{3}} \quad (9)$$

Where k is a number obtained from the function curve in **Figure 4**, based on the variable factor of $\frac{V_{AC,min(pk)}}{N \cdot (V_{out,setpoint} + V_d)}$.

In this design example, the variable factor of $\frac{V_{AC,min(pk)}}{N \cdot (V_{out,setpoint} + V_d)}$ can be calculated as:

$$\frac{V_{AC,min(pk)}}{N \cdot (V_{out,setpoint} + V_d)} = \frac{\sqrt{2} \cdot 90}{3.2 \cdot (54 + 0.7)} = 0.727$$

Referring to the function curve in **Figure 4**, k = 0.31 is obtained.

Based on equation (9), $I_{pri(rms),max}$ can then be calculated as:

$$I_{pri(rms),max} \approx 2.606 \cdot \sqrt{\frac{0.31}{3}}$$

$$\boldsymbol{I_{pri(rms),max} \approx 0.838\ A}$$

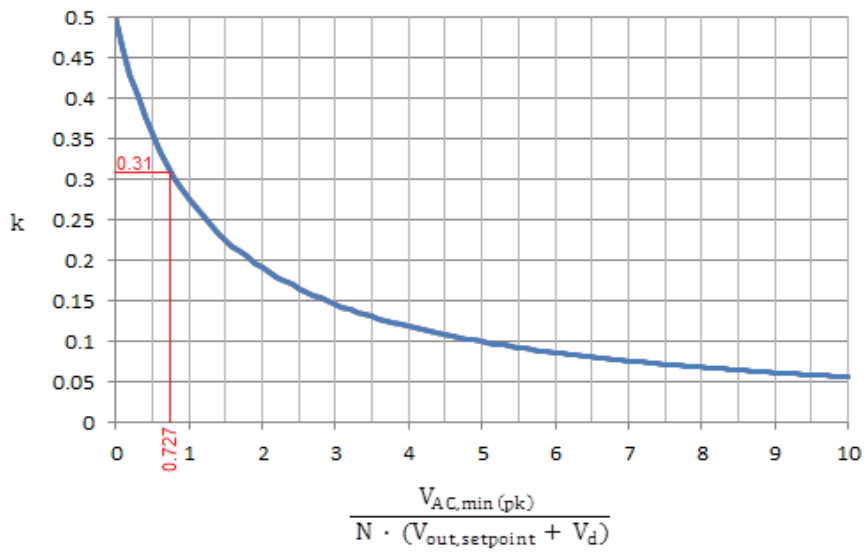


Figure 4 Function curve of k

The selectable MOSFET $R_{ds(on),25°C}$ can be defined as:

$$R_{ds(on),25°C} \leq \frac{m \cdot P_{out,full}}{I_{pri(rms),max}^{2} \cdot \Delta R_{ds(on),100°C}} \quad (10)$$

Where m is the desired ratio of MOSFET conduction loss over $P_{out,full}$ and $\Delta R_{ds(on),100°C}$ is the ratio of $\frac{R_{ds(on),100°C}}{R_{ds(on),25°C}}$.

It is typical to select m in the range of 0.025 to 0.03 and $\Delta R_{ds(on),100°C}$ in the range of 1.75 to 1.85. Taking m = 0.0275 and $\Delta R_{ds(on),100°C}$ = 1.8, $R_{ds(on),25°C}$ can then be calculated as:

$$R_{ds(on),25°C} \leq \frac{0.0275 \cdot 43.2}{0.838^{2} \cdot 1.8} = 0.94\ \Omega$$

Referring to the calculation results of equation (10) and **Table 3** below, **$R_{ds(on),25°C}$ = 900 mΩ** is selected.

To utilize the PCB as a heatsink for the MOSFET, **IPD80R900P7** with TO-252 (DPAK) package is selected.

Table 3 800 V CoolMOS™ P7 selection table

$R_{DS(on)}$ [mΩ]	TO -220	TO-220 FullPAK	TO-247	TO-252 (DPAK)	TO-251 (IPAK)	TO-251 (IPAK Short Lead)	SOT-223	TO-220 FullPAK narrow lead
280	IPP80R280P7	IPA80R280P7	IPW80R280P7	IPD80R280P7				IPAN80R280P7
360	IPP80R360P7	IPA80R360P7	IPW80R360P7	IPD80R360P7				IPAN80R360P7
450	IPP80R450P7	IPA80R450P7		IPD80R450P7				IPAN80R450P7
600	IPP80R600P7	IPA80R600P7		IPD80R600P7	IPU80R600P7	IPS80R600P7	IPN80R600P7	
750	IPP80R750P7	IPA80R750P7		IPD80R750P7	IPU80R750P7	IPS80R750P7	IPN80R750P7	
900/950	IPP80R900P7	IPA80R900P7		IPD80R900P7	IPU80R900P7	IPS80R900P7	IPN80R950P7	
1200	IPP80R1K2P7	IPA80R1K2P7		IPD80R1K2P7	IPU80R1K2P7	IPS80R1K2P7	IPN80R1K2P7	
1400	IPP80R1K4P7	IPA80R1K4P7		IPD80R1K4P7	IPU80R1K4P7	IPS80R1K4P7	IPN80R1K4P7	
2000				IPD80R2K0P7	IPU80R2K0P7	IPS80R2K0P7	IPN80R2K0P7	
2400				IPD80R2K4P7	IPU80R2K4P7	IPS80R2K4P7	IPN80R2K4P7	
3300				IPD80R3K3P7	IPU80R3K3P7		IPN80R3K3P7	
4500				IPD80R4K5P7	IPU80R4K5P7		IPN80R4K5P7	

For the secondary main output diode selection, it is necessary to first estimate the maximum reverse voltage $V_{r(diode),max}$ and maximum secondary main winding peak current $I_{sec(pk),max}$, based on:

$$V_{r(diode),max} = V_{spike,diode} + V_{out,setpoint} + \frac{V_{AC,max(pk)} + V_{margin,FET}}{N} \quad (11)$$

Where $V_{spike,diode}$ is the diode reverse voltage spike.

Assuming $V_{spike,diode} \approx 35\% \cdot \left(V_{out,setpoint} + \frac{V_{AC,max(pk)} + V_{margin,FET}}{N}\right)$,

$$V_{r(diode),max} \approx 135\% \cdot \left(V_{out,setpoint} + \frac{V_{AC,max(pk)} + V_{margin,FET}}{N}\right) = 135\% \cdot \left(54 + \frac{\sqrt{2} \cdot 305 + 90}{3.2}\right)$$

$$V_{r(diode),max} \approx 292.81\ V$$

$$I_{sec(pk),max} \approx I_{pri(pk),max} \cdot \frac{N_p}{N_s} = 2.606 \cdot \frac{32}{10} \quad (12)$$

$$I_{sec(pk),max} \approx 8.34\ A$$

Based on the above, a secondary main output diode with repetitive reverse voltage rating **V_{RRM} = 300 V** is selected. To minimize its switching and conduction losses, the selected diode also has the properties of hyper-fast recovery speed and low forward voltage drop at $I_{sec(pk),max}$.

Additionally, a RC secondary snubber network, e.g. 10 Ω resistor in series with 150 pF capacitor, is deployed across the secondary main output diode, to suppress the diode reverse voltage spike and the EMI.

5 CS resistor and GD pin-related design

Figure 5 shows the connections of the Current Sense (CS) resistor R_{CS}, gate resistor R_G and gate source resistor R_{GS}.

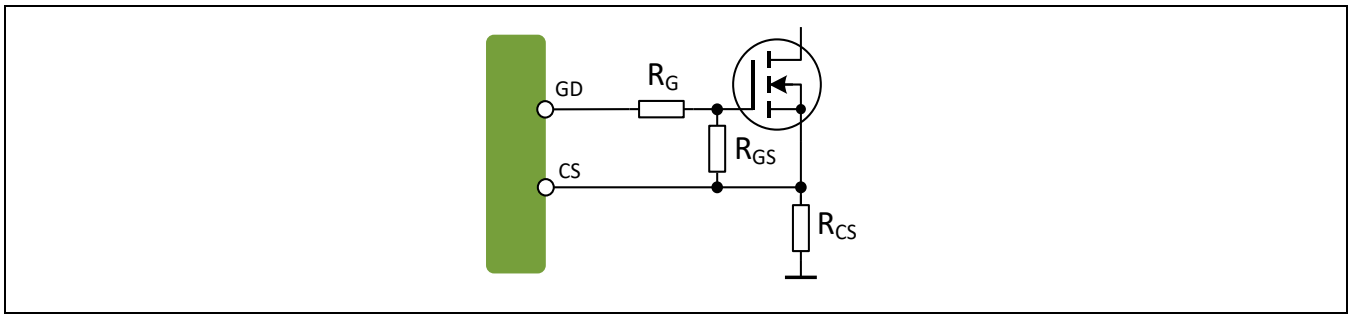


Figure 5 GD pin, CS pin, R_{CS}, R_G and R_{GS} connections

Based on the CS pin voltage across R_{CS}, the MOSFET current can be measured.

The recommended minimum CS resistor value $R_{CS,min}$ is defined and calculated as:

$$R_{CS,min} = \frac{0.45}{I_{pri(pk),max}} = \frac{0.45}{2.606} = 0.173\ \Omega \quad (13)$$

The recommended maximum CS resistor value $R_{CS,max}$ is defined and calculated as:

$$R_{CS,max} = \frac{0.54}{I_{pri(pk),max}} = \frac{0.54}{2.606} = 0.207\ \Omega \quad (14)$$

Based on the calculation results above, CS resistor **R_{CS} = 0.2 Ω** is selected in this design example.

R_G is to damp the gate-rise oscillaton, and R_{GS} is to ensure the MOSFET remains in an off-state when AC input is applied, with the IC not being activated yet. **R_G = 10 Ω** and **R_{GS} = 20 kΩ** are selected in this design example.

The gate-drive peak voltage $V_{GD,pk}$ is typically 12 V with sufficient V_{CC} voltage supply. To achieve a good balance of switching loss and EMI, the gate voltage rising slope can be controlled by configuring the gate driver peak source current parameter $I_{GD,pk}$ (configurable range: 30 mA to 180 mA). This saves two components (see $D_{fastoff}$, R_{slowon} in **Figure 6**), which are conventionally added for the same purpose.

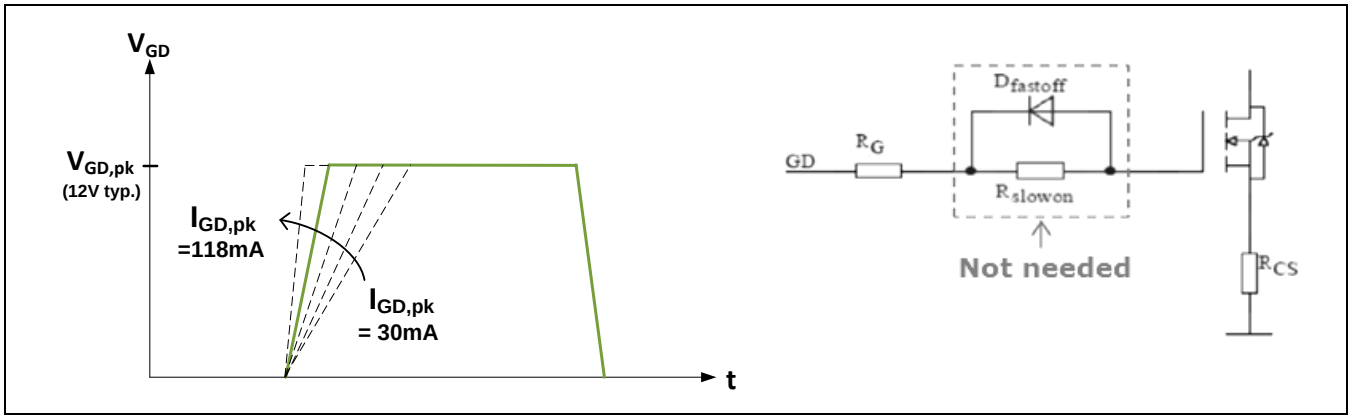


Figure 6 Gate-drive voltage rising slope control with $I_{GD,pk}$ parameterization for component saving

With the high-speed switching characteristics of CoolMOS™ P7 MOSFET, it is recommended to configure the $I_{GD,pk}$ parameter in the range of 30 mA to 49 mA.

As a result, **$I_{GD,pk}$ = 30 mA** is selected in this design example.

6 MOSFET maximum current cycle-by-cycle limit and start-up phase design

Under the single-fault condition of second-stage CC converter MOSFET drain and source pins being shorted, the connected output LEDs could clamp the flyback output voltage below its constant voltage regulation set-point.

To limit the flyback output power to the LEDs below 100 VA as per UL1310 requirements under such fault conditions, especially at high input voltage, XDPL8218 regulated mode features the CS pin voltage level 1 for MOSFET maximum current cycle-by-cycle limit $V_{OCP1}(V_{in})$, which is adaptive based on the estimated input voltage V_{in}, as shown in **Figure 7**.

*Note: Regulated mode is a controller operating state, which is entered after the start-up phase, to regulate the output based on the FB voltage mapping, as shown in **Figure 8**.*

*Note: The estimated input voltage V_{in} used for $V_{OCP1}(V_{in})$ adaptation is in rms value, which is assumed as 0.707 of estimated peak input voltage $V_{in,peak}$, regardless of whether actual input voltage is AC or DC. As the input voltage is estimated based on ZCD pin and CS pin switching signals, proper ZCD resistor selection (see **Section 12**) and R_{in} parameter fine-tuning (see **Section 18.1**) are needed.*

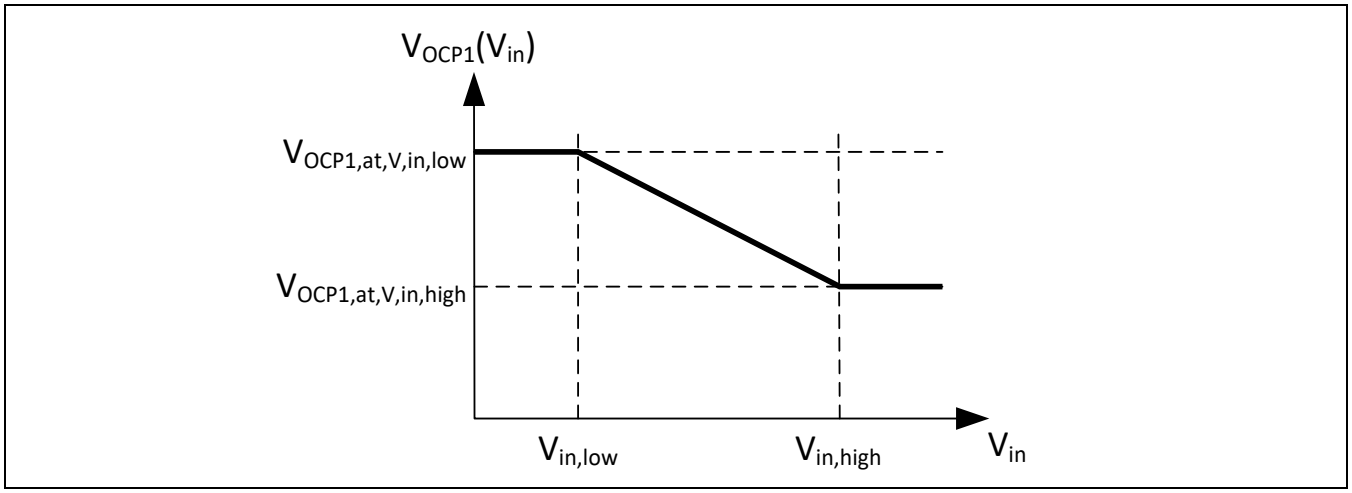


Figure 7 Regulated mode CS pin voltage level 1 for MOSFET maximum current cycle-by-cycle limit

$V_{OCP1,at,V,in,low}$ parameter defines the value of $V_{OCP1}(V_{in})$ variable when the estimated input voltage V_{in} is same as or lower than the lowest operational input voltage parameter $V_{in,low}$.

$V_{in,low}$ and $V_{OCP1,at,V,in,low}$ parameters can be defined and calculated as:

$$V_{in,low} = a \cdot V_{AC,min} \quad (15)$$

Where a is the ratio recommended to be between 0.9 and 0.95.

Taking a = 0.91,

$$V_{in,low} = 0.91 \cdot 90$$

$$\boldsymbol{V_{in,low} = 82\ V_{rms}}$$

$$V_{OCP1,at,V,in,low} = I_{pri(pk),max} \cdot R_{CS} \quad (16)$$

$$V_{OCP1,at,V,in,low} = 2.606 \cdot 0.2$$

$$V_{OCP1,at,V,in,low} = 0.52\ V$$

$V_{OCP1,at,V,in,high}$ parameter defines the value of $V_{OCP1}(V_{in})$ variable when the estimated input voltage V_{in} is the same as or higher than the highest operational input voltage parameter $V_{in,high}$. To better limit the maximum output power transfer to the LEDs under the fault condition mentioned above, $V_{OCP1,at,V,in,high}$ should be configured less than $V_{OCP1,at,V,in,low}$.

$V_{in,high}$ and $V_{OCP1,at,V,in,high}$ parameters can be defined and calculated as:

$$V_{in,high} = b \cdot V_{AC,max} \quad (17)$$

Where b is the ratio recommended to be between 1.05 and 1.10.

Taking b = 1.07,

$$V_{in,high} = 1.07 \cdot 305$$

$$V_{in,high} = 326\ V_{rms}$$

$$V_{OCP1,at,V,in,high} = c \cdot R_{CS} \cdot L_p \cdot {I_{pri(pk),max}}^2 \cdot f_{sw,min,at,P,out,full} \cdot \left[\frac{1}{V_{in,high(pk)}} + \frac{1}{N \cdot (V_{out,setpoint} + V_d)}\right] \quad (18)$$

Where $V_{in,high(pk)}$ is √2 times of $V_{in,high}$ and c is the ratio recommended to be between 1.05 and 1.15.

Taking c = 1.12,

$$V_{OCP1,at,V,in,high} = 1.12 \cdot 0.2 \cdot 544 \cdot 10^{-6} \cdot 2.606^2 \cdot 52 \cdot 10^3 \cdot \left[\frac{1}{\sqrt{2} \cdot 326} + \frac{1}{3.2 \cdot (54 + 0.7)}\right]$$

$$V_{OCP1,at,V,in,high} = 0.34\ V$$

Note: $V_{OCP1,at,V,in,high}$ parameter minimum configurable value is fixed as 0.34 V. If the calculation result of equation (18) is below 0.34 V, parameter setting of $V_{OCP1,at,Vin,high}$ = 0.34 V should be selected.

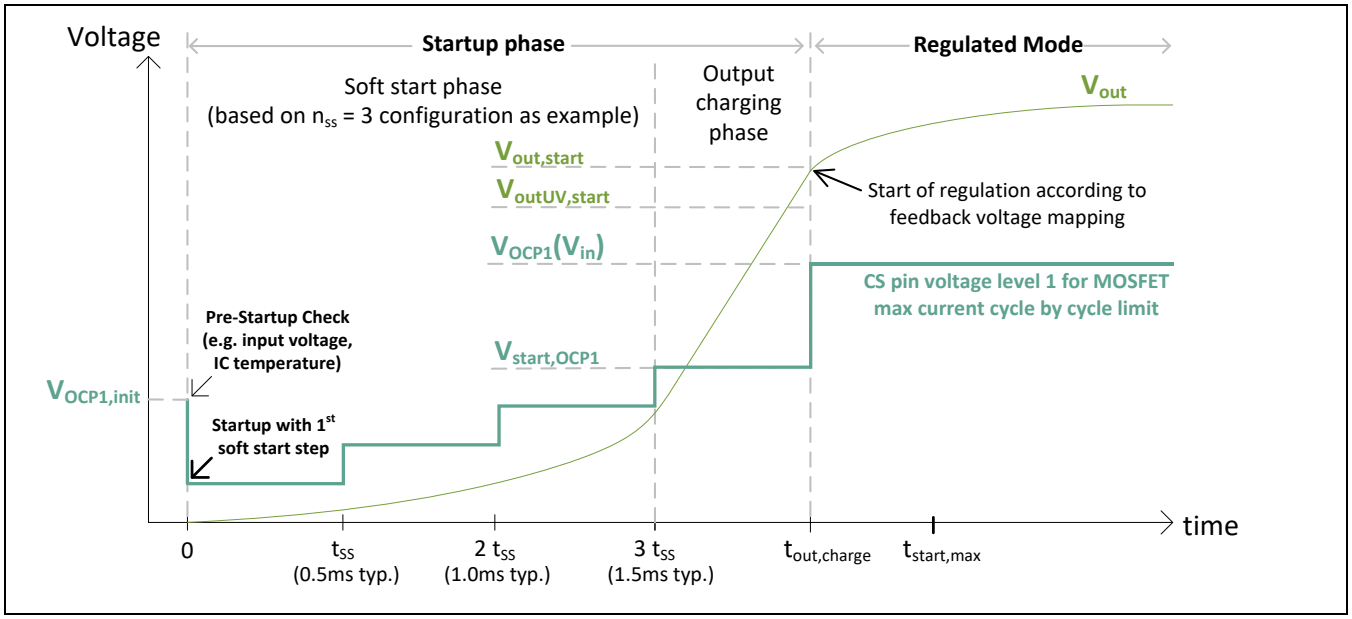


Figure 8 Pre-start-up check, start-up phase and regulated mode

Pre-start-up check ensures the estimated input voltage V_{in} and IC junction temperature T_j are within the configured protection limits before start-up, as shown in **Figure 8**. The parameter configurations of the input voltage levels and maximum T_j for start-up are covered in **Section 11** and **Section 15.3** respectively.

$V_{OCP1,init}$ parameter in **Figure 8** denotes the initial CS pin voltage level 1 for MOSFET current limit on the input voltage measurement pulse, during pre-start-up check. It can be defined and calculated as:

$$V_{OCP1,init} = \frac{d \cdot R_{CS} \cdot V_{in,high(pk)} \cdot t_{on,min,V,in,start,sense}}{L_p} \quad (19)$$

Where $t_{on,min,V,in,start,sense}$ is the minimum on-time for the pre-start-up input voltage measurement pulse and d is the ratio recommended to be between 1.2 and 1.3.

Take $t_{on,min,V,in,start,sense}$ = 1.38 µs, and d = 1.29,

$$V_{OCP1,init} = \frac{1.29 \cdot 0.2 \cdot \sqrt{2} \cdot 326 \cdot 1.38 \cdot 10^{-6}}{544 \cdot 10^{-6}}$$

$$\boldsymbol{V_{OCP1,init} = 0.3\ V}$$

Note: A typical leading-edge blanking time $t_{CS,LEB}$ of 480 ns applies on $V_{OCP1}(V_{in})$, $V_{OCP1,init}$ and $V_{start,OCP1}$.

The start-up phase consists of the soft-start phase and output charging phase. The soft-start phase is to minimize the component stress during start-up, while the output charging phase is to fast-charge the output voltage for fast V_{CC} self-supply takeover from the primary auxiliary winding.

During the soft-start phase, the switching frequency is fixed as 20 kHz. The MOSFET current is limited in the first soft-start step based on the CS pin maximum voltage limit of $V_{start,OCP1}/(n_{ss} + 1)$, where $V_{start,OCP1}$ is the parameter for the output charging phase CS pin maximum voltage limit, and n_{ss} is the parameter for the number of soft-start steps. The soft-start phase CS pin maximum voltage limit is increased by $V_{start,OCP1}/(nss + 1)$ after each soft-start step, and the typical duration of each soft-start step is 0.5 ms.

During the output charging phase, the output voltage is fast-charged with MOSFET switching pulses based on either the output charging phase CS pin maximum voltage limit of $V_{start,OCP1}$ or the maximum on-time in QRM. To exit the start-up phase and enter the regulated mode without triggering the start-up output UVP, the ZCD pin estimated output voltage V_{out} has to either reach the output charging voltage set-point of $V_{out,start}$ before the maximum allowable start-up phase duration of $t_{start,max}$ is reached, or reach at least the start-up output UVP level of $V_{outUV,start}$ at the timing of $t_{start,max}$.

It is generally recommended to set the n_{ss} parameter value between 2 and 4. In this design example, **n_{ss} = 3** parameter setting is selected, as shown in **Figure 8**.

To ensure fast V_{CC} self-supply takeover from the primary auxiliary winding, the $V_{start,OCP1}$ parameter is recommended to be configured as per $V_{OCP1,at,V,in,low}$. Hence, **$V_{start,OCP1}$ = 0.52 V** parameter setting is selected in this design example.

$V_{out,start}$ parameter can be defined and calculated as:

$$V_{out,start} = \frac{V_{a,start} \cdot N_s}{N_a} - V_d \quad (20)$$

Where $V_{a,start}$ is the desired primary auxiliary winding demagnetization voltage when output voltage is $V_{out,start}$.

$V_{a,start}$ is recommended to be between 8 V and 9 V. So, taking $V_{a,start}$ = 8.3 V,

$$V_{out,start} = \frac{8.3 \cdot 10}{3} - 0.7$$

$$\boldsymbol{V_{out,start} = 27\ V}$$

7 HV pin-related design

As shown in **Figure 9**, HV series resistor R_{HV} is connected from the HV pin to the cathodes of HV diode D_{HV1} and D_{HV2}, while bridge rectifier AC input should be applied across the D_{HV1} anode and D_{HV2} anode.

Additionally, a HV capacitor C_{HV} should also be connected between the HV pin and ground.

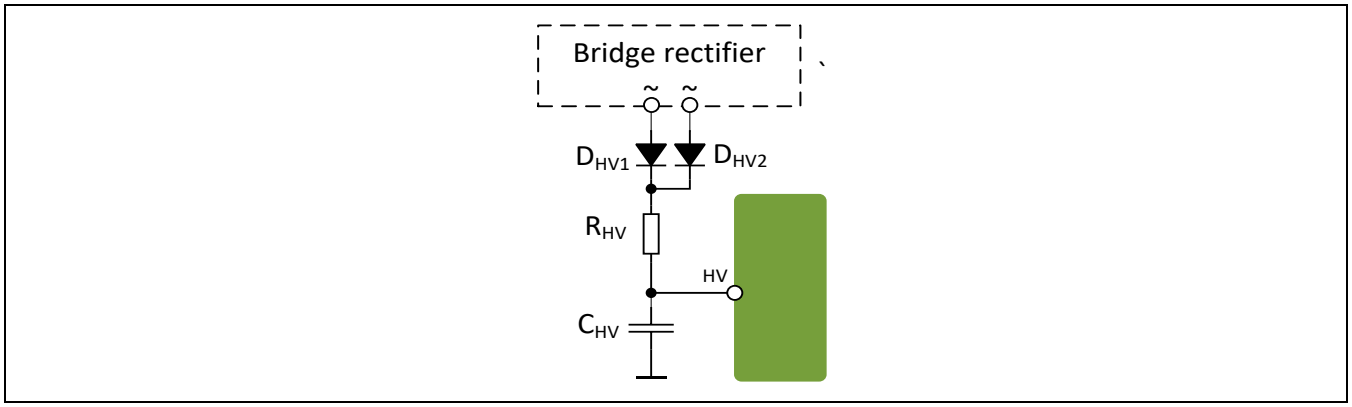


Figure 9 HV pin, R_{HV}, C_{HV}, D_{HV1} and D_{HV2} connections

The recommended minimum HV series resistor value $R_{HV,min}$ is defined and calculated as:

$$R_{HV,min} = \frac{V_{in,high(pk)}}{I_{HV,max}} \quad (21)$$

Where $I_{HV,max}$ is the HV pin maximum peak input current of 9.6 mA.

$$R_{HV,min} = \frac{\sqrt{2} \cdot 326}{9.6 \cdot 10^{-3}} = 48\ k\Omega$$

The recommended maximum HV series resistor value $R_{HV,max}$ is defined and calculated as:

$$R_{HV,max} = \frac{V_{AC,min(rect,avg)} - V_{VCCON,max}}{I_{HV,min(avg)}} \cdot \left[1 - \frac{2}{\pi} \cdot sin^{-1}\left(\frac{V_{VCCON,max}}{V_{AC,min(pk)}}\right)\right] \quad (22)$$

Where $V_{AC,min(rect,avg)}$ is the average value of the rectified $V_{AC,min}$, while $V_{VCCON,max}$ is the maximum V_{CC} turn-on voltage threshold of 22 V, and $I_{HV,min(avg)}$ is the recommended HV pin minimum average input current of 1 mA.

$$R_{HV,max} = \frac{0.9 \cdot 90 - 22}{1 \cdot 10^{-3}} \cdot \left[1 - \frac{2}{\pi} \cdot sin^{-1}\left(\frac{22}{\sqrt{2} \cdot 90}\right)\right]$$

$$R_{HV,max} = 52.5\ k\Omega$$

Based on the above, **R_{HV} = 52 kΩ** is selected in this design example.

The HV series resistor dielectric withstand voltage should be above the total of $V_{AC,max(pk)}$ and $V_{margin,FET}$ (see **Section 4** for their respective values), which is equivalent to 521.3 V. As an example, the selected R_{HV} = 52 kΩ in this design example can be formed using a 36 kΩ 0.5 W resistor (dielectric withstand of 350 V) in series with a 16 kΩ 0.25 W resistor (dielectric withstand of 200 V).

For better line synchronization stability against noise interference, C_{HV} shown in **Figure 9** is needed. In addition, C_{HV} also improves the surge and ESD capability of the HV pin.

C_{HV} = 1 nF is recommended and selected in this design example.

8 V_{CC} capacitance and output UVP design

To fulfill the Energy Star time-to-light requirement of 500 ms, the V_{CC} voltage maximum charging time for IC activation, $t_{VCCON,charge,max}$ should not exceed 350 ms. Therefore, the maximum V_{CC} capacitance $C_{VCC,max}$ can be defined and calculated as:

$$C_{VCC,max} = \frac{V_{AC,120(rect,avg)} - V_{VCCON,max}}{R_{HV} \cdot V_{VCCON,max}} \cdot t_{VCCON,charge,max} \cdot \left[1 - \frac{2}{\pi} \cdot sin^{-1}\left(\frac{V_{VCCON,max}}{V_{AC,120(pk)}}\right)\right] \quad (23)$$

Where $V_{VCCON,max}$ is the maximum V_{CC} turn-on threshold of 22 V, $V_{AC,120(rect,avg)}$ is the average value of rectified 120 V_{rms} AC input, and $V_{AC,120(pk)}$ is the peak value of 120 V_{rms} AC input.

$$C_{VCC,max} = \frac{0.9 \cdot 120 - 22}{52 \cdot 10^3 \cdot 22} \cdot 350 \cdot 10^{-3} \cdot \left[1 - \frac{2}{\pi} \cdot sin^{-1}\left(\frac{22}{\sqrt{2} \cdot 120}\right)\right] = 24.13\ \mu F$$

$t_{start,max}$ parameter refers to the maximum allowable duration of the start-up phase, which consists of the soft-start phase and output charging phase. It can be indirectly configured with V_{CC} capacitance parameter C_{VCC}, based on:

$$t_{start,max} = \frac{0.8 \cdot C_{VCC} \cdot (V_{VCCON} - V_{UVOFF})}{I_{IC,avg,est}} = \frac{0.8 \cdot C_{VCC} \cdot (20.5 - 6)}{12 \cdot 10^{-3}} = 967 \cdot C_{VCC} \quad (24)$$

Where V_{VCCON} is the typical V_{CC} turn-on voltage threshold of 20.5 V, V_{UVOFF} is the typical V_{CC} turn-off voltage threshold of 6 V and $I_{IC,avg,est}$ is the estimated IC current consumption of 12 mA.

For proper start-up, as shown in **Figure 10 (left)**, C_{VCC} has to be high enough to ensure its corresponding $t_{start,max}$ calculated from equation (24) is longer than $t_{out,charge}$, whch $t_{out,charge}$ is the time needed to charge the output voltage to the start-up output UVP level $V_{outUV,start}$ or higher.

Based on the considerations above, V_{CC} capacitor value and IC parameter setting of **C_{VCC} = 22 μF** are selected in this design example, which results in $t_{start,max}$ = 21.3 ms. In addition, a noise decoupling ceramic capacitor of **$C_{VCCdecouple}$ = 0.1 μF** with low ESR is added in parallel to C_{VCC}.

In the start-up phase, if the ZCD pin estimated output voltage V_{out} is lower than $V_{outUV,start}$ over a time-out period of $t_{start,max}$, the start-up output UVP is triggered. For instance, this could happen if the flyback output is shorted during the start-up, as shown in **Figure 10 (right)**. It is recommended to configure $V_{outUV,start}$ as $V_{out,start}$. Hence, **$V_{outUV,start}$ = 27 V** is selected in this design example.

The reaction of start-up output UVP is fixed as auto-restart and the auto-restart time is based on the $t_{auto,restart}$ parameter. **$t_{auto,restart}$ = 1.2 sec** setting is selected in this design example. Please note that $t_{auto,restart}$ is a common auto-restart time used for other system protections with auto-restart reaction.

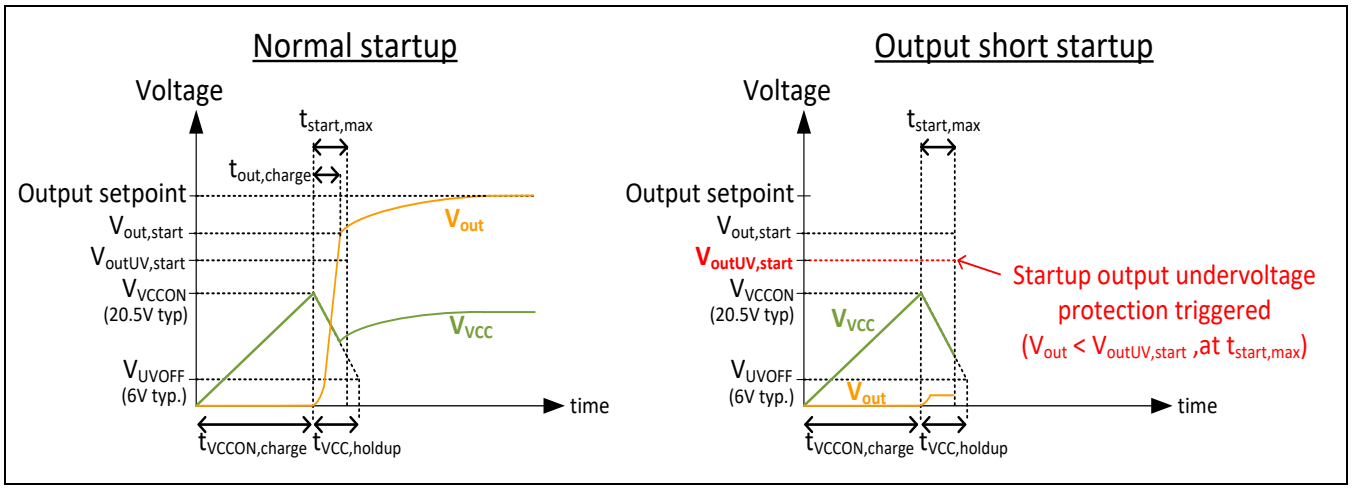


Figure 10 Normal start-up and start-up output UVP (short) waveforms

Under the single-fault condition of second-stage CC regulator MOSFET drain and source pins being shorted, the main output could be clamped by a low-output LED voltage, which could result in the flyback MOSFET continuously operating in the saturation region due to low V_{CC} and gate-drive voltages.

Hence, in this design example, **$EN_{UVP,Vout}$ = Enabled** parameter setting is selected to enable the regulated mode output UVP, which could be triggered if the ZCD pin estimated output voltage V_{out} is below the regulated mode output UVP level V_{outUV} for longer than a blanking time of $t_{VoutUV,blank}$, as shown in **Figure 11**.

V_{outUV} parameter can be defined and calculated as:

$$V_{outUV} = \frac{V_{a,UV} \cdot N_s}{N_a} - V_d \quad (25)$$

Where $V_{a,UV}$ is the desired primary auxiliary winding demagnetization voltage when output voltage is V_{outUV}.

$V_{a,UV}$ is recommended to be between 9.5 V and 10.5 V. So, taking $V_{a,UV}$ = 10.1 V,

$$V_{outUV} = \frac{10.1 \cdot 10}{3} - 0.7$$

$$\boldsymbol{V_{outUV} = 33\ V}$$

To prevent the regulated mode output UVP from being triggered by the output undershoot during input voltage step-down, e.g. from 277 V_{rms} to 120 V_{rms}, $t_{VoutUV,blank}$ is recommended to be at least 100 ms. Hence, **$t_{VoutUV,blank}$ = 500 ms** is selected in this design example.

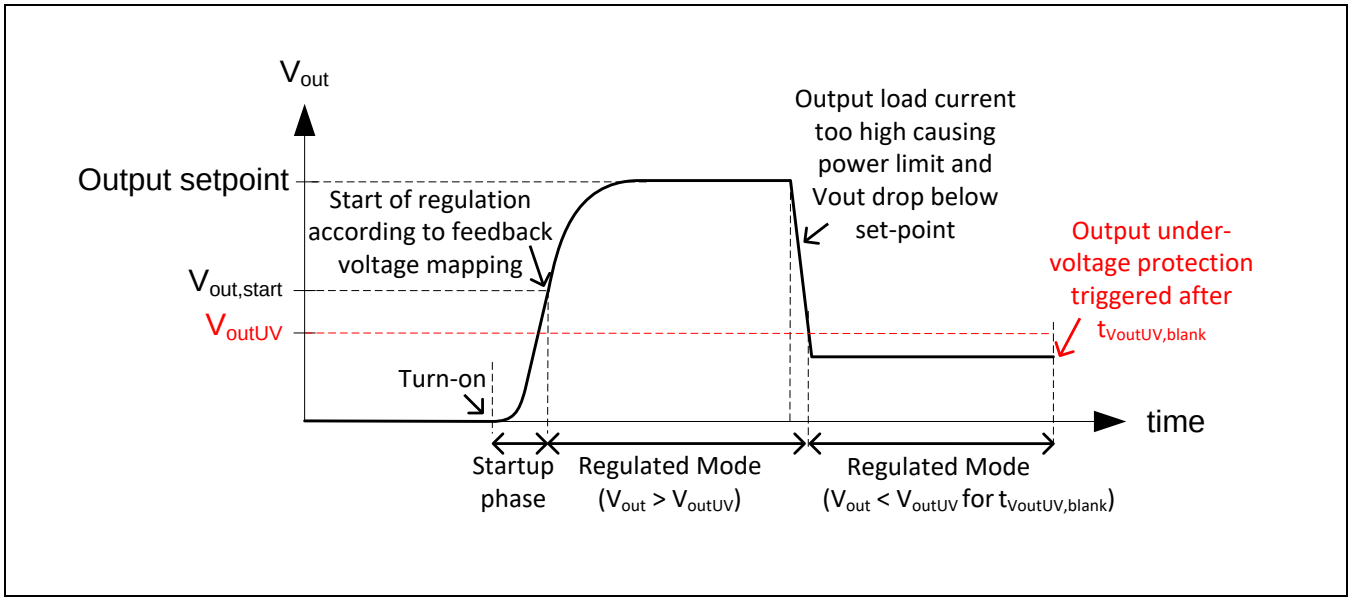


Figure 11 Regulated mode output UVP (based on ZCD pin voltage sensing)

The reaction of regulated mode output UVP is configurable to latch-mode or auto-restart, based on the $Reaction_{UVP,Vout}$ parameter. **$Reaction_{UVP,Vout}$ = Auto-Restart** is selected in this design example.

Note: The regulated mode output UVP is not active in Active Burst Mode (ABM).

9 Output OVP-related design

Under the single-fault condition of the FB pin open, the main output voltage would rise quickly above $V_{out,setpoint}$. As shown in **Figure 12**, the output OVP would be triggered when the ZCD pin estimated output voltage V_{out} is higher than the output OVP level V_{outOV} for longer than a blanking time.

Note: The output OVP blanking time is typically a quarter of the half sine wave period, e.g. 2.5 ms for F_{line} = 50 Hz with line synchronization established.

To prevent the output OVP from being triggered by the output overshoot during input voltage step-up, e.g. from 120 V_{rms} to 277 V_{rms}, the output OVP level V_{outOV} should be configured well above $V_{out,setpoint}$. Therefore, the V_{outOV} parameter can be defined and calculated as:

$$V_{outOV} \geq 120\% \cdot V_{out,setpoint} = 120\% \cdot 54 = 64.8\ V$$

Based on the above, **V_{outOV} = 65 V** is selected in this design example.

Considering the ZCD pin estimated output voltage protection accuracy is subjective to the the sampled signal accuracy, sampling delay, indirect sensing delay (e.g. output voltage cannot be estimated near AC input phase angle of 0 degrees and 180 degrees) and blanking time, the output capacitor voltage rating $V_{out,cap,rating}$ should be selected well above V_{outOV}. As a result, $V_{out,cap,rating}$ can be defined and calculated as:

$$V_{out,cap,rating} \geq \frac{V_{outOV}}{0.9} = \frac{65}{0.9} = 72.2\ V \quad (27)$$

Based on the above, **$V_{out,cap,rating}$ = 80 V** is selected in this design example.

Attention: It is mandatory to ensure that V_{outOV} is configured well below the actual output capacitor voltage rating $V_{out,cap,rating}$, while the $V_{out,cap,rating}$ is not exceeded in actual testing with all the necessary test conditions.

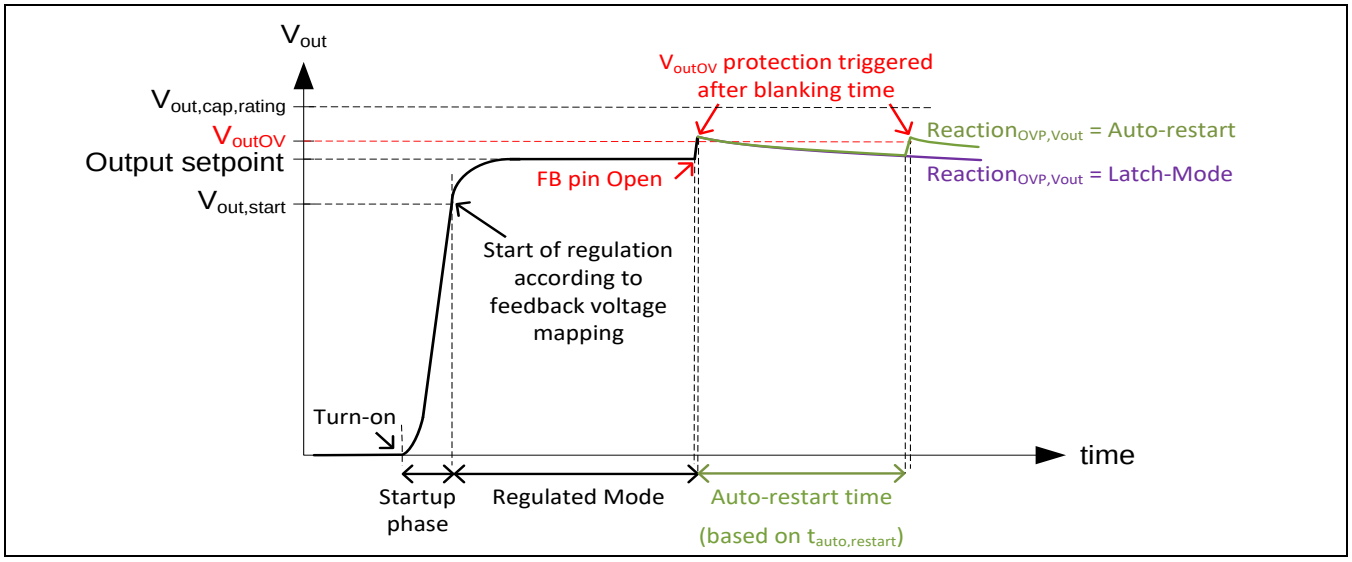


Figure 12 Output OVP (based on ZCD pin voltage sensing)

The reaction of output OVP is configurable to latch-mode or auto-restart, based on the $Reaction_{OVP,Vout}$ parameter. **$Reaction_{OVP,Vout}$ = Auto-Restart** is selected in this design example.

Note: The output OVP is not active in ABM.

10 DC link filter and secondary main output capacitance

$C_{DC,filter}$ denotes the DC link filter capacitor placed after the bridge rectifier. A higher $C_{DC,filter}$ value gives lower EMI but worse power quality, and vice versa.

Table 4 Recommended initial $C_{DC,filter}$ value

$V_{AC,min}$ (V)	Steady-state full-load output power $P_{out,full}$ (W)	Recommended initial $C_{DC,filter}$ (μF)
90 ~ 107	Less than 26	0.1
	26 ~ 35	0.15
	36 ~ 45	0.22
	Greater than 45	Greater than 0.22
Greater than or equal to 108	Less than 31	0.1
	31 ~ 40	0.15
	41 ~ 55	0.22
	Greater than 55	Greater than 0.22

Referring to **Table 4**, **initial $C_{DC,filter}$ = 0.22 μF** is selected in this design example. To improve the estimated input voltage V_{in} accuracy during pre-start-up check, it is also recommended to deploy DC link resistor **$R_{DC,filter}$ = 30 MΩ** in parallel with $C_{DC,filter}$, as shown in **Figure 13**.

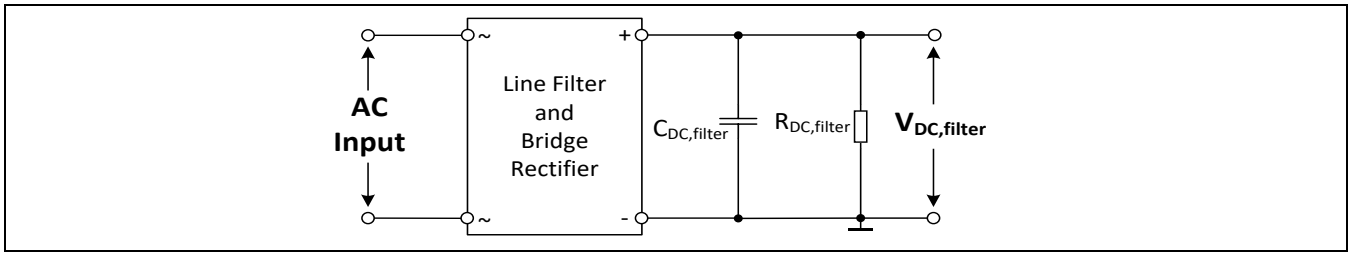


Figure 13 $C_{DC,filter}$ and $R_{DC,filter}$ across the DC link bus voltage

To compensate for the input current displacement caused by the $C_{DC,filter}$, the XDPL8218 enhanced Power Factor Correction (PFC) feature can be enabled by configuration of the compensation gain parameter named C_{EMI}. As a start, it can be configured as per the $C_{DC,filter}$ value. Hence, the **initial C_{EMI} = 0.22 μF** parameter setting is selected in this design example. Upon successful powering-up of the sytem, refer to **Section 18.3** for the fine-tuning guide.

$V_{ripple,out(pk-pk),max}$ denotes the maximum allowable secondary main output voltage peak-to-peak ripple level. Assuming the flyback output in this design example is connected to a second-stage CC buck regulator, which has a maximum LED voltage load $V_{LED,max}$ of 48 V and maximum allowable duty cycle $D_{buck,max}$ of 95 percent, $V_{ripple,out(pk-pk),max}$ can be defined and calculated as:

$$V_{ripple,out(pk-pk),max} = 2 \cdot \left(V_{out,setpoint} - \frac{V_{LED,max}}{D_{buck,max}}\right) = 2 \cdot \left(54 - \frac{48}{0.95}\right) = 6.95\ V \quad (28)$$

The secondary main output capacitor C_{out} value can then be defined and calculated as:

$$C_{out} \geq \frac{P_{out,full}}{2\pi \cdot F_{line,min} \cdot V_{ripple,out(pk-pk),max} \cdot V_{out,setpoint}} = \frac{43.2}{2\pi \cdot 47 \cdot 6.95 \cdot 54} = 390\ \mu F \quad (29)$$

Considering the tolerance of the electrolytic capacitor value, **C_{out} = 470 μF** is selected in this design example.

For lower EMI, low-ESR ceramic capacitors **$C_{out,lowESR1}$ = 1 μF** and **$C_{out,lowESR2}$ = 0.1 μF** are also added in parallel with C_{out}.

11 Input voltage levels for start-up and protection

$EN_{OVP,In}$ parameter refers to the enable switch for maximum input voltage start-up check and input OVP, based on $V_{in,start,max}$ and V_{inOV} levels, respectively. **$EN_{OVP,In}$ = Enabled** is selected in this design example.

$EN_{UVP,In}$ parameter refers to the enable switch for minimum input voltage start-up check and input UVP, based on $V_{in,start,min}$ and V_{inUV} levels, respectively. **$EN_{UVP,In}$ = Enabled** is selected in this design example.

*Note: The estimated input voltage V_{in} used for start-up check and protection is in rms value, which is assumed as 0.707 of estimated peak input voltage $V_{in,peak}$ regardless of whether actual input voltage is AC or DC. As the input voltage is estimated based on ZCD pin and CS pin switching signals, proper ZCD resistor selection (see **Section 12**) and R_{in} parameter fine-tuning (see **Section 18.1**) are needed.*

$V_{in,start,max}$ parameter refers to the maximum input voltage level setting for start-up, which is recommended to be configured as $V_{in,high}$. Hence, **$V_{in,start,max}$ = 326 V_{rms}** is selected in this design example. V_{inOV} parameter refers to the input OVP level setting, which is recommended to be:

$$V_{inOV} \geq V_{in,start,max} \cdot 107\% = 349\ V_{rms} \quad (30)$$

$V_{in,start,min}$ parameter refers to the minimum input voltage level setting for start-up, which is recommended to be configured as $V_{in,low}$. Hence, **$V_{in,start,min}$ = 82 V_{rms}** is selected in this design example. V_{inUV} parameter refers to the input UV (brown-out) protection level setting, which is recommended as:

$$V_{inUV} \leq V_{in,start,min} \cdot 93\% = 76\ V_{rms} \quad (31)$$

Based on the above, **V_{inOV} = 350 V_{rms}** and **V_{inUV} = 70 V_{rms}** are selected in this design example.

$EN_{VIN,ABM}$ refers to the enable switch for input voltage protections (based on V_{inOV} and V_{inUV}) in ABM.

If $EN_{VIN,ABM}$ is enabled, the enable switches for V_{inOV} and V_{inUV} protections in ABM are respectively based on $EN_{OVP,In}$ and $EN_{UVP,In}$. If $EN_{VIN,ABM}$ is disabled, both V_{inOV} and V_{inUV} protections are inactive in ABM.

In this design example, **$EN_{VIN,ABM}$ = Enabled** is selected.

Note: The reaction of V_{inOV} and V_{inUV} protections is auto-restart. A typical blanking time of either 10 half sine wave periods or 10 burst periods applies on V_{inOV} and V_{inUV} protections triggering.

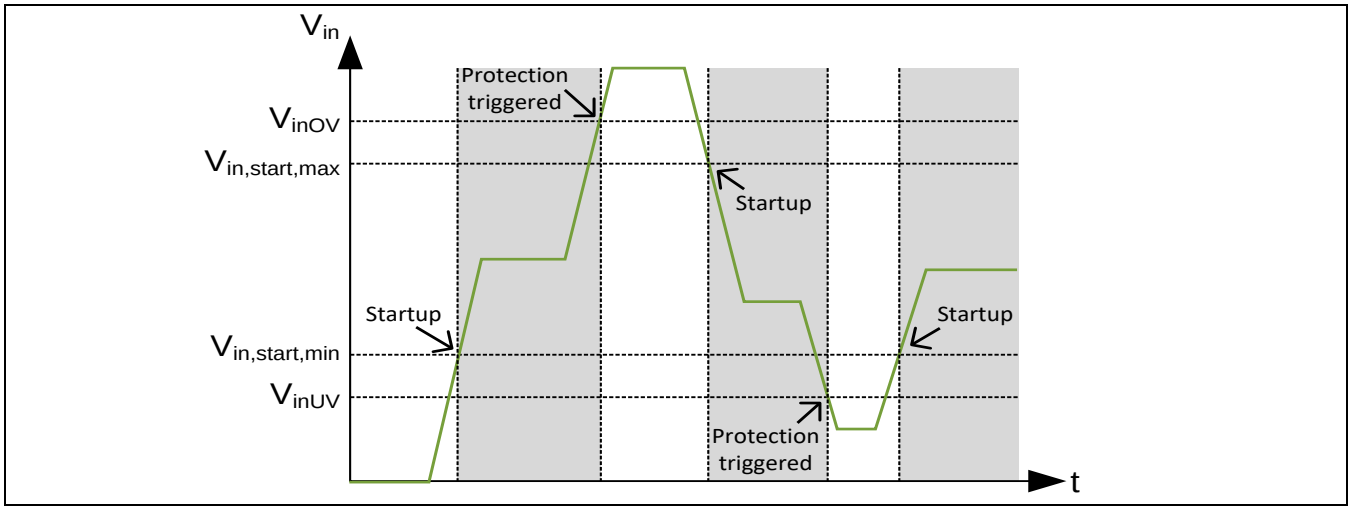


Figure 14 Input voltage levels for start-up and protection

12 ZCD pin-related design

ZCD pin filter capacitor C_{ZCD}, ZCD series resistor $R_{ZCD,1}$ and ZCD shunt resistor $R_{ZCD,2}$ are connected based on the connections shown in **Figure 15**.

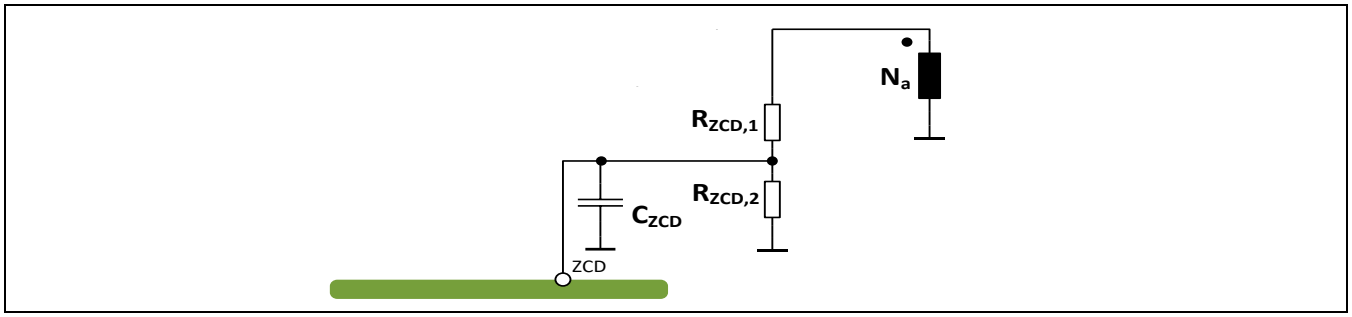


Figure 15 ZCD pin, C_{ZCD}, R_{ZCD1} and R_{ZCD2} connections

C_{ZCD} is mainly for ZCD pin noise-filtering, so a fixed value can generally be used for different designs. **C_{ZCD} = 47 pF** is selected in this design example.

*Note: QR first valley switching of the MOSFET drain voltage can be achieved with t_{ZCDPD} parameter fine-tuning based on **Section 18.2**. **Initial t_{ZCDPD} = 350 ns** can be used for powering-up of the system before the fine-tuning.*

Apart from zero crossing detection, the ZCD pin is also used to measure the reflected input voltage signal when the MOSFET is turned on, and to measure the reflected output voltage signal when the MOSFET is turned off afterward. Hence, it is important to select the correct $R_{ZCD,1}$ and $R_{ZCD,2}$ values, which can cover the necessary measurement range, not only for normal conditions but also for protected conditions.

The recommended minimum ZCD series resistance $R_{ZCD,1,min}$ and maximum ZCD series resistance $R_{ZCD,1,max}$ are defined as:

$$R_{ZCD,1,min} = -\frac{N_a}{I_{IV,max,VinOV} \cdot N_p} \cdot \left[V_{inOV(pk)} + \frac{V_{INPCLN,min} \cdot N \cdot (V_{outOV} + V_d)}{V_{ZCDSH,max,VoutOV}} \right] \quad (32)$$

$$R_{ZCD,1,max} = -\frac{N_a}{I_{IV,min,VinUV} \cdot N_p} \cdot \left[V_{inUV(pk)} - \Delta V_{in,HF,ripple,est} + \frac{V_{INPCLN,max} \cdot N \cdot (V_{outOV} + V_d)}{V_{ZCDSH,min,VoutOV}} \right] \quad (33)$$

Where:

$V_{inOV(pk)}$ and $V_{inUV(pk)}$ are respectively √2 times V_{inOV} and √2 times V_{inUV}.

$I_{IV,max,VinOV}$ and $I_{IV,min,VinUV}$ are respectively the recommended maximum ZCD pin negative clamping current for V_{inOV} sensing and minimum ZCD pin negative clamping current for V_{inUV} sensing.

$V_{ZCDSH,max,VoutOV}$ and $V_{ZCDSH,min,VoutOV}$ are respectively the recommended maximum and minimum ZCD pin voltage sensing levels for V_{outOV} sensing.

$V_{INPCLN,max}$ and $V_{INPCLN,min}$ are respectively the maximum and minimum ZCD pin negative clamping voltages.

$\Delta V_{in,HF,ripple,est}$ is the estimated difference between the $V_{inUV(pk)}$ level and the high-frequency ripple minimum voltage level at the peak of AC input half sine wave. As a rule of thumb, it can be assumed to be between 25 V and 30 V.

Taking $I_{IV,max,VinOV}$ = -3.1 mA, $I_{IV,min,VinUV}$ = -0.15 mA, $V_{ZCDSH,max,VoutOV}$ = 2.6 V, $V_{ZCDSH,min,VoutOV}$ = 2.35 V, $V_{INPCLN,max}$ = -0.22 V, $V_{INPCLN,min}$ = -0.14 V, and $\Delta V_{in,HF,ripple,est}$ = 27.5 V,

$$R_{ZCD,1,min} = -\frac{3}{-3.1 \cdot 10^{-3} \cdot 32} \cdot \left[\sqrt{2} \cdot 350 + \frac{-0.14 \cdot 3.2 \cdot (65 + 0.7)}{2.6}\right] = 14.6\ k\Omega$$

$$R_{ZCD,1,max} = -\frac{3}{-0.15 \cdot 10^{-3} \cdot 32} \cdot \left[\sqrt{2} \cdot 70 - 27.5 + \frac{-0.22 \cdot 3.2 \cdot (65 + 0.7)}{2.35}\right] = 32.4\ k\Omega$$

In general, it is recommended to select $R_{ZCD,1}$ to be closer to $R_{ZCD,1,max}$, for lower power dissipation. Hence, **$R_{ZCD,1}$ = 27 kΩ** is selected in this design example.

The recommended minimum ZCD shunt resistance $R_{ZCD,2,min}$ and maximum ZCD shunt resistance $R_{ZCD,2,max}$ are defined and calculated as:

$$R_{ZCD,2,min} = \frac{R_{ZCD,1} \cdot N_s \cdot V_{ZCDSH,min,VoutOV}}{N_a \cdot (V_{outOV} + V_d) - N_s \cdot V_{ZCDSH,min,VoutOV}} = \frac{27 \cdot 10^3 \cdot 10 \cdot 2.35}{3 \cdot (65 + 0.7) - 10 \cdot 2.35} = 3.65\ k\Omega \quad (34)$$

$$R_{ZCD,2,max} = \frac{R_{ZCD,1} \cdot N_s \cdot V_{ZCDSH,max,VoutOV}}{N_a \cdot (V_{outOV} + V_d) - N_s \cdot V_{ZCDSH,max,VoutOV}} = \frac{27 \cdot 10^3 \cdot 10 \cdot 2.6}{3 \cdot (65 + 0.7) - 10 \cdot 2.6} = 4.1\ k\Omega \quad (35)$$

Based on the above, **$R_{ZCD,2}$ = 3.9 kΩ** is selected in this design example.

When the AC input voltage decreases at full-load output, the DC link filter capacitor high-frequency peak-to-peak voltage ripple would increase, and this would also result in higher ripple on the ZCD pin negative clamping current, which is used for estimating input voltage V_{in}. Hence, for good V_{in} estimation via the ZCD pin, especially at input UVP level V_{inUV}, such a ripple effect should be minimized and compensated with proper configuration of $t_{on,max,at,V,in,low}$ and R_{in} parameters, respectively.

$t_{on,max,at,V,in,low}$ parameter denotes the maximum on-time at the lowest operational input voltage $V_{in,low}$. $t_{on,max,at,V,in,low}$ should be configured not too high, while being able to deliver the steady-state full-load output power $P_{out,full}$ at $V_{in,low}$. Therefore, $t_{on,max,at,V,in,low}$ can be defined and calculated as:

$$t_{on,max,at,V,in,low} = \frac{e \cdot L_p \cdot I_{pri(pk),max}}{\sqrt{2} \cdot V_{in,low}} \quad (36)$$

Where e is the ratio for margin on the maximum on-time, which is recommended to be between 1.2 and 1.25.

Taking e = 1.23,

$$t_{on,max,at,V,in,low} = \frac{1.23 \cdot 544 \cdot 10^{-6} \cdot 2.606}{\sqrt{2} \cdot 82}$$

$$\boldsymbol{t_{on,max,at,V,in,low} = 15\ \mu s}$$

R_{in} parameter is to compensate the DC link filter capacitor voltage ripple for accurate V_{in} measurement. As this parameter configuration is subjective to the line filter and the DC link filter capacitance design, parameter fine-tuning based on actual waveform measurement is required.

For powering up the board, the initial R_{in} parameter can be defined and calculated as:

$$Initial\ R_{in} = \frac{\Delta V_{in,HF,ripple,est}}{I_{pri(pk),max}} \quad (37)$$

$$Initial\ R_{in} = \frac{27.5}{2.606}$$

$$\boldsymbol{Initial\ R_{in} = 10.6\ \Omega}$$

Upon successful powering-up of the system, please refer to **Section 18.1** for the fine-tuning guide for the R_{in} parameter.

13 Secondary-side regulation FB circuit design

The FB pin filter capacitor C_{FB}, optocoupler and the SSR FB circuit are connected based on the connections shown in **Figure 16**.

The FB pin does not need any external pull-up as XDPL8218 has a fixed voltage reference V_{REF} of 2.428 V, which is internally connected to its FB pin via an internal pull-up resistor. The internal pull-up resistor value is configurable based on the $R_{FB,pull,up}$ parameter.

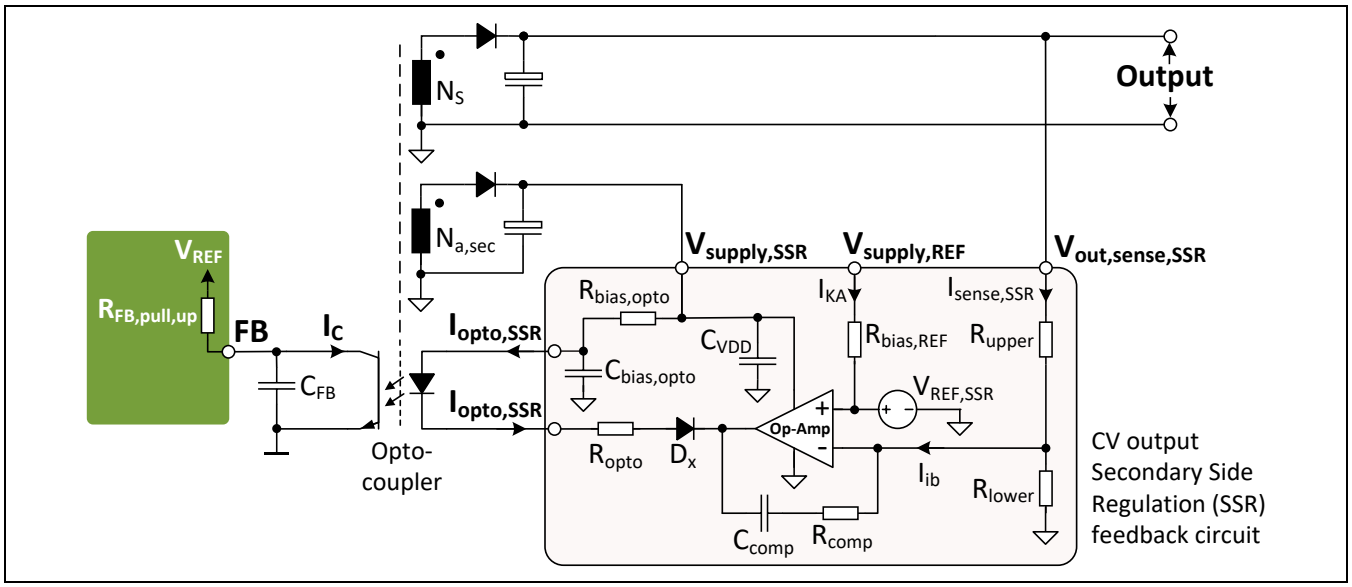


Figure 16 FB pin internal pull-up, C_{FB}, optocoupler and CV output SSR FB circuit connections

$V_{supply,SSR}$ from the secondary auxiliary winding rectified output is mainly used to supply the SSR circuit op-amp operational voltage V_{DD} and optocoupler LED current $I_{opto,SSR}$ via resistor $R_{bias,opto}$. For $V_{supply,SSR}$ noise decoupling, in this design example, a ceramic capacitor of **C_{VDD} = 100 nF** with low ESR is selected and placed near the op-amp V_{DD} pin.

As shown in **Figure 16**, the SSR op-amp non-inverting input should be connected to the SSR reference voltage $V_{REF,SSR}$, while the inverting input should be connected to a resistor/divider formed by R_{upper} and R_{lower} for output voltage sensing. In this design example, the selected op-amp part number is TSM103W, which has dual op-amps, and the non-inverting input of one op-amp is wired to a voltage reference $V_{REF,SSR}$ of 2.5 V internally.

$V_{supply,SSR}$ can be used as the SSR voltage reference supply $V_{supply,REF}$, to provide a minimum biasing current of $I_{KA,min}$ via voltage reference biasing resistor $R_{bias,REF}$, for generating the $V_{REF,SSR}$. However, in this design example, to minimize the standby loss, $V_{supply,REF}$ is not supplied by $V_{supply,SSR}$ based on $N_{a,sec}$ = 3, but by another rectified output with lower voltage, based on a partial secondary auxiliary winding turns number of **$N_{a,sec,partial}$ = 2**. Hence, the recommended maximum voltage reference biasing resistance $R_{bias,REF,max}$ can be defined and calculated as:

$$R_{bias,REF,max} = \frac{g}{I_{KA,min}} \cdot \left[(V_{out,setpoint} + V_d) \cdot \left(N_{a,sec,partial}/N_s\right) - V_{d,aux} - V_{REF,SSR}\right] \quad (38)$$

Where g is the ratio recommended to be between 0.75 and 0.85, and $V_{d,aux}$ is the auxiliary output diode forward voltage.

Taking g = 0.8, $V_{d,aux}$ = 0.5 V and $I_{KA,min}$ = 1 mA based on the selected op-amp datasheet,

$$R_{bias,REF,max} = \frac{0.8}{1 \cdot 10^{-3}} \cdot [(54 + 0.7) \cdot (2/10) - 0.5 - 2.5] = 6.35\ k\Omega$$

Based on the above, **$R_{bias,REF}$ = 6.2 kΩ** is selected in this design example.

To achieve accurate output voltage regulation based on $V_{out,setpoint}$, the op-amp input biasing current I_{ib} has to be much smaller than the output sensing upper resistor/divider current $I_{sense,SSR}$. As compared to using the conventional shunt regulator TL431, which has a maximum reference input current of 4 µA, the selected op-amp has a maximum input bias current of $I_{ib,max}$ = 0.2 µA, which results in much lower regulation offset error $ERR_{offset,ib}$ with the same level of $I_{sense,SSR}$.

Considering that $ERR_{offset,ib}$ is desired to be not more than 0.1 percent in this design example, the maximum output sensing upper divider resistance $R_{upper,max}$ can be de defined and calculated as:

$$R_{upper,max} = \frac{ERR_{offset,ib} \cdot (V_{out,setpoint} - V_{REF})}{I_{ib,max}} = \frac{0.1\% \cdot (54 - 2.5)}{0.2 \cdot 10^{-6}} = 257.5\ k\Omega \quad (39)$$

Since the ABM burst frequency is fixed based on the f_{burst} parameter for low audible noise, as a rule of thumb to achieve stable main output voltage at no-load, the R_{upper} selection should also ensure the output sensing resistor/divider power consumption is at least the power transfer of a single ABM pulse. Therefore, the $R_{upper,max}$ value can also be defined and calculated as:

$$R_{upper,max} = \frac{L_p \cdot V_{out,setpoint} \cdot (V_{out,setpoint} - V_{REF})}{V_{inOV}^2 \cdot t_{on,min,ABM}^2 \cdot f_{burst} \cdot \eta_{ABM}} \quad (40)$$

Where $t_{on,min,ABM}$ is the ABM minimum on-time parameter and η_{ABM} is the estimated power efficiency in ABM.

Take f_{burst} = 130 Hz, $t_{on,min,ABM}$ = 1 µs and assume η_{ABM} = 65 percent,

$$R_{upper,max} = \frac{544 \cdot 10^{-6} \cdot 54 \cdot (54 - 2.5)}{350^2 \cdot (1 \cdot 10^{-6})^2 \cdot 130 \cdot 65\%} = 146.15\ k\Omega$$

Based on the smaller $R_{upper,max}$ calculated from equation (39) and (40), the output sensing upper resistance R_{upper} should be selected near to $R_{upper,max}$ = 146.15 kΩ to achieve low standby power, so **R_{upper} = 127.5 kΩ** is selected in this design example.

The output sensing lower divider resistance R_{lower} can then be defined and calculated as:

$$R_{lower} = \frac{R_{upper} \cdot V_{REF}}{V_{out,setpoint} - V_{REF}} = \frac{127.5 \cdot 10^3 \cdot 2.5}{54 - 2.5} \quad (41)$$

$$\boldsymbol{R_{lower} \approx 6.2\ k\Omega}$$

For good control-loop stability, the FB pin internal pull-up resistance parameter $R_{FB,pull,up}$ should be configured not too high. On the other hand, for low standby power, $R_{FB,pull,up}$ should be configured not too low either. In a practical system, $R_{FB,pull,up}$ may be around 5 kΩ. Hence, **$R_{FB,pull,up}$ = 5.5 kΩ** is selected in this design example.

XDPL8218's internal ADC sampling point for the FB pin voltage signal is right after the GD pin signal becomes high for a period of $t_{CS,LEB}$ (480 ns typ.), to ensure a high Signal to Noise Ratio (SNR). The FB pin capacitor **C_{FB}** is mainly used to filter the switching-on MOSFET current ringing noise, which might not be fully damped after $t_{CS,LEB}$. As the frequency of such ringing noise is normally at least a few MHz and the ADC sampling frequency $f_{sampling,ADC}$ is a few kHz, the RC filter frequency $f_{RC,FB}$ formed by C_{FB} and $R_{FB,pull,up}$ is recommended to be in the range of 40 kHz to 100 kHz. Therefore, C_{FB} can be defined and calculated as:

$$C_{FB} = \frac{1}{2 \cdot \pi \cdot R_{FB,pull,up} \cdot f_{RC,FB}} \quad (42)$$

Taking $f_{RC,FB}$ = 60 kHz,

$$C_{FB} = \frac{1}{2 \cdot \pi \cdot 5.5 \cdot 10^3 \cdot 60 \cdot 10^3} = 482\ pF$$

Based on the commonly used ceramic capacitor value which is near to the calculated C_{FB} above, **C_{FB} = 470 pF** is selected in this design example.

The minimum power transfer of the system is reached when the filtered FB voltage level $V_{FB,filtered}$ is the same as or less than the $V_{FB,min}$ parameter. Hence, it is recommended to configure the minimum FB voltage $V_{FB,min}$ the same as $V_{CE,sat}$ based on the selected optocoupler datasheet. As a result, **$V_{FB,min}$ = 0.3 V** is selected in this design example.

Based on the minimum current transfer ratio CTR_{min} from the selected optocoupler datasheet, the total resistance of $R_{bias,opto}$ and R_{opto} can be defined as:

$$R_{bias,opto} + R_{opto} \leq h \cdot R_{FB,pull,up} \cdot CTR_{min} \cdot \left[\frac{(V_{out,setpoint}+V_d) \cdot N_{a,sec}/N_S - V_{d,aux} - V_{f,opto} - V_{dx}}{V_{REF}-V_{CE,sat}}\right] \quad (43)$$

Where h is the ratio recommended to be between 0.7 and 0.8 for compensating the secondary auxiliary winding rectified output voltage drop under no load at the main output, $V_{f,opto}$ is the optocoupler LED forward voltage, R_{opto} and V_{dx} are respectively the optocoupler series resistance and the forward voltage of D_x, as shown in **Figure 16**.

Taking CTR_{min} = 100 percent, h = 0.7, $V_{f,opto}$ = 1.1 V and V_{dx} = 0.5 V for the calculation,

$$R_{bias,opto} + R_{opto} \leq 0.7 \cdot 5.5 \cdot 10^3 \cdot 100\% \cdot \left[\frac{0.7 \cdot (54 + 0.7) \cdot 3/10 - 0.5 - 1.1-0.5}{2.428 - 0.3}\right]$$

$$R_{bias,opto} + R_{opto} \leq 16.98\ k\Omega$$

Based on the above, $R_{bias,opto}$ + R_{opto} = 16 kΩ is selected in this design example. $R_{bias,opto}$ is recommended to be at least 10 times lower than R_{opto}, so $R_{bias,opto,max}$, which denotes the maximum $R_{bias,opto}$ value, can then be defined and calculated as:

$$R_{bias,opto,max} = \frac{R_{bias,opto} + R_{opto}}{1.1} = 1.455\ k\Omega \quad (44)$$

The recommended maximum RC filter frequency $f_{RC,bias,opto,max}$ formed by $R_{bias,opto}$ and $C_{bias,opto}$ is $F_{line,min}$. Since $R_{bias,opto}$ with high resistance is generally cheaper than $C_{bias,opto}$ with high capacitance, $C_{bias,opto}$ nominal value is recommended not to exceed 4.7 µF. As a result, in this design example, **$C_{bias,opto}$ = 3.3 µF** is selected, while the minimum optocoupler biasing resistor value $R_{bias,opto,min}$ can be defined and calculated as:

$$R_{bias,opto,min} = \frac{1}{2 \cdot \pi \cdot C_{FB} \cdot f_{RC,bias,opto,max}} = \frac{1}{2 \cdot \pi \cdot 3.3 \cdot 10^{-6} \cdot 47} = 1\ k\Omega \quad (45)$$

Based on the $R_{bias,opto,max}$ and $R_{bias,opto,min}$ calculation results, and also $R_{bias,opto}$ + R_{opto} selection above, **$R_{bias,opto}$ = 1** kΩ and **R_{opto} = 15** kΩ are selected in this design example.

A type II FB compensation network is used in this design example. It consists of a resistor R_{comp} in series with C_{comp}, as shown In **Figure 16**. As a rule of thumb, the initial frequency of the pole at origin $f_{pole,origin}$ can be around 2 Hz to 3 Hz, while the initial frequency of the zero f_{zero} is suggested to be around 4 Hz to 8 Hz. As a result, the initial value of C_{comp} and R_{comp} for system powering-up can be defined and calculated as:

$$C_{comp} = \frac{1}{2 \cdot \pi \cdot R_{upper} \cdot f_{pole,origin}} \quad (46)$$

$$R_{comp} = \frac{1}{2 \cdot \pi \cdot C_{comp} \cdot f_{zero}} \quad (47)$$

Taking $f_{pole,origin}$ = 2.65 Hz and f_{zero} = 5 Hz,

$$C_{comp} = \frac{1}{2 \cdot \pi \cdot 127.5 \cdot 10^3 \cdot 2.65}$$

$$\boldsymbol{Initial\ C_{comp} = 470\ nF}$$

$$R_{comp} = \frac{1}{2 \cdot \pi \cdot 470 \cdot 10^{-9} \cdot 5}$$

$$\boldsymbol{Initial\ R_{comp} = 68\ k\Omega}$$

14 Regulated mode parameters

In regulated mode, XDPL8218 supports multi-mode operation consisting of QRM1, Discontinuous Conduction Mode (DCM) without valley switching, and ABM. The mode of operation and switching parameters are selected mainly based on the digitally filtered FB voltage $V_{FB,filtered}$ mapping. When the regulated mode is entered after the start-up phase, the filtered FB voltage maximum limit $V_{FB,filtered,max}$ ramp is applied initially on the voltage mapping, to prevent excessive output rise overshoot.

14.1 Digital notch filter

In QRM1 and DCM, a digital notch filter with quality factor of $N_{quality}$ is applied, to suppress the double line frequency component in $V_{FB,filtered}$, in order to achieve high power quality. To allow time for the notch filter convergence, the notch filter output is only taken as $V_{FB,filtered}$ for output regulation after every HV pin line synchronization has been established for a time-out, which is based on the $n_{notch,blank}$ parameter. A digital low pass filter is used for noise filtering whenever the digital notch filter output has not been taken as $V_{FB,filtered}$. The recommended $N_{quality}$ and $n_{notch,blank}$ parameter configuration from **Table 5** is selected in this design example.

In ABM, line synchronization and notch filter are disabled for power saving, so a digital low pass filter is applied.

Table 5 Notch filter parameter configuration

Parameter name	Recommended value	Unit
$N_{quality}$	1.6	–
$n_{notchblank}$	2	Number of AC input half sine wave period

14.2 On-time limit and switching frequency limit (QRM1/DCM)

The maximum on-time variable $t_{on,max}(V_{in})$ is dependent on the estimated input voltage V_{in}, as shown in **Figure 17**. When V_{in} is $V_{in,low}$, the maximum on-time is based on the $t_{on,max,at,V,in,low}$ parameter. When V_{in} is above $V_{in,low}$, the maximum on-time is reduced, to compensate for the increasing input voltage influence on the FB gain. When V_{in} is below $V_{in,low}$, the maximum on-time foldback can be configured based on the $P_{foldback,gain}$ parameter, for power limitation during brown-out.

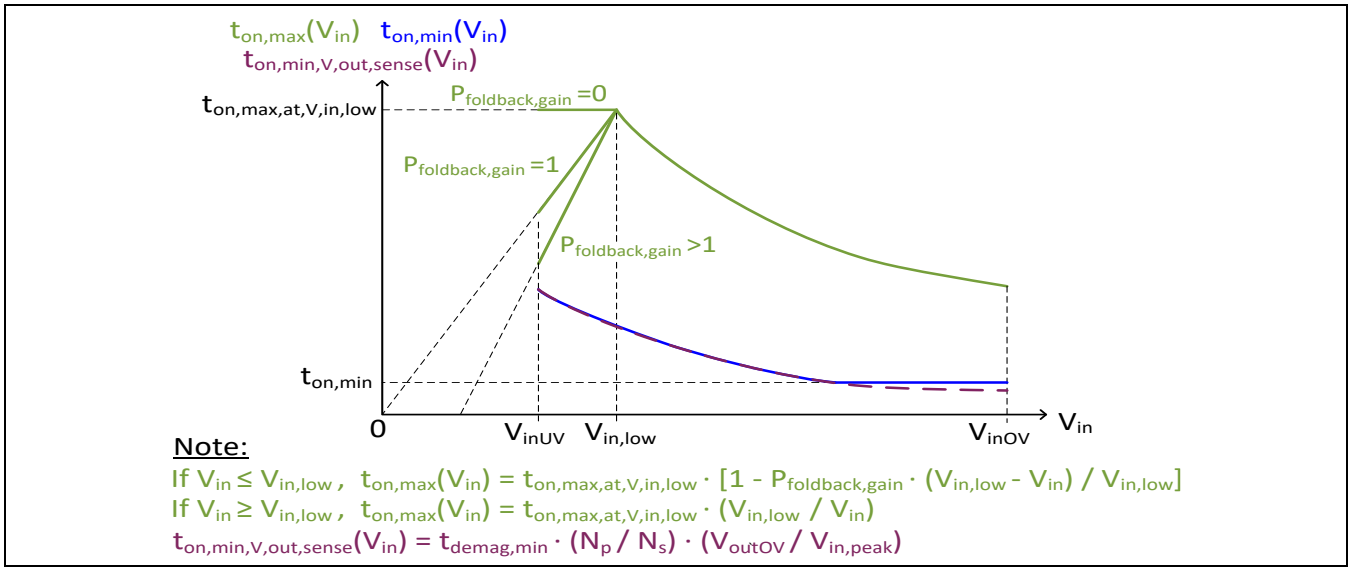


Figure 17 QRM1 and DCM on-time limits

In QRM1 and DCM, the minimum on-time variable $t_{on,min}(V_{in})$ is based on the $t_{on,min}$ parameter or $t_{on,min,V,out,sense}(V_{in})$ variable, whichever is higher. The $t_{on,min,V,out,sense}(V_{in})$ variable denotes the minimum on-time required for V_{outOV} sensing, which is dependent on V_{in} measurement and the $t_{min,demag}$ parameter (see the equation in **Figure 17**).

The recommended QRM1 and DCM on-time limit related parameter configuration from **Table 6** is selected in this design example.

Table 6 QRM1 and DCM on-time limit parameter configuration

Parameter name	Recommended value	Unit
$t_{on,max,at,V,in,low}$	Refer to calculation in **Section 12**	µs
$t_{on,min}$	1.38	µs
$t_{min,demag}$	4	µs
$P_{foldback,gain}$	1	–

In QRM1, the maximum switching frequency parameter $f_{sw,max}$ affects the number of first valley switching pulses over every AC input half sine wave period. To lower the input current total harmonic distortion (iTHD) at high input voltage and high output power, the number of first valley switching pulses can be reduced by lowering $f_{sw,max}$. However, please note that the efficiency could be reduced if the number of first valley switching pulses is reduced too much. As a start, it is recommended to use **$f_{sw,max}$ = 136 kHz** and fine-tune it later if necessary.

The minimum switching frequency parameter $f_{sw,min}$ is not configurable and is fixed as 20 kHz.

14.3 ABM FB voltage sensing and control

In ABM, the switching pulse on-time t_{on} and burst pulse number N_{ABM} are controlled based on $V_{FB,filtered}$ taken at the last pulse of the previous burst cycle, as shown in **Figure 18**. The ABM minimum on-time and minimum pulse number per burst are based on the $t_{on,min,ABM}$ and $n_{ABM,min}$ parameters, respectively.

During ABM burst pause, the controller enters sleep mode with the FB pin internal pull-up disabled, to reduce the power consumption. Before the next ABM burst pulse starts, the controller wakes up with the FB pin internal pull-up re-enabled. To avoid measuring the FB pin voltage spikes, which could present initially when the internal pull-up is re-enabled, the start of both ABM burst pulsing and FB pin voltage sampling is delayed upon the controller wake-up, based on the n_{wakeup} parameter.

The ABM switching period is based on $1/f_{sw,min}$ (50 µs typ.), while the the burst cycle period t_{ABM} is based on $1/f_{burst}$, as shown in **Figure 18**.

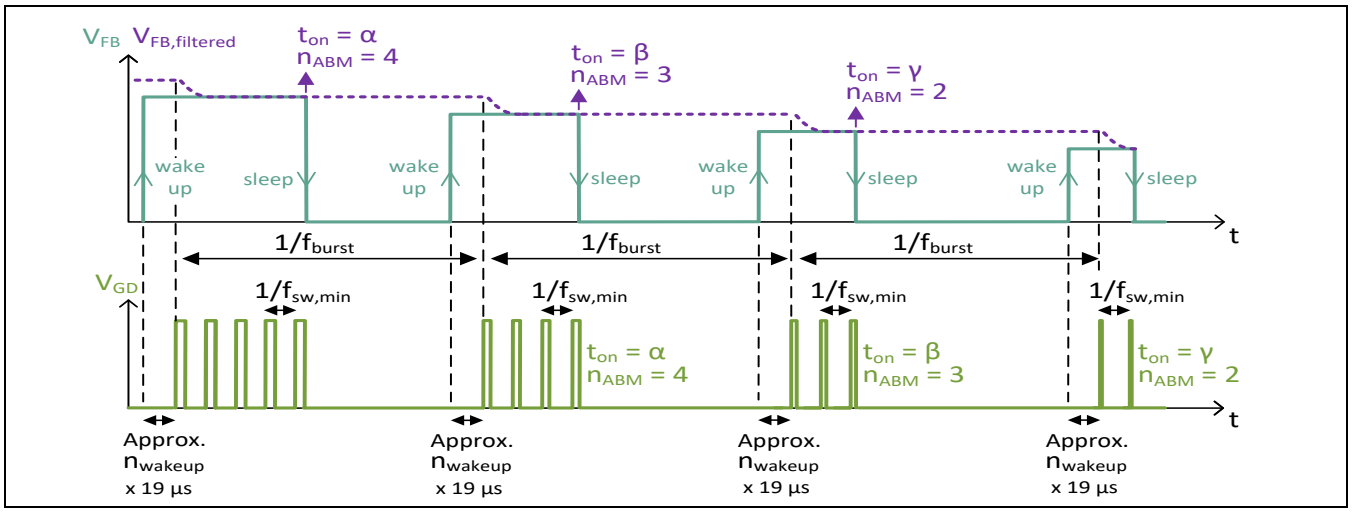


Figure 18 ABM t_{on} and n_{ABM} control based on $V_{FB,filtered}$ taken at the last pulse of the previous burst cycle

Referring to **Table 7**, the recommended parameter configuration for ABM FB voltage sensing and control is selected in this design example.

Table 7 Parameter configuration related to ABM FB voltage sensing and control

Parameter name	Recommended value	Unit
$n_{ABM,min}$	1	–
f_{burst}	130	Hz
$t_{on,min,ABM}$	1.00	µs
n_{wakeup}	5	Interval (each interval is around 19 µs)

14.4 FB voltage mapping and mode transition

In regulated mode, the multi-mode operation on-time t_{on}, switching period t_{sw} and ABM pulse number n_{ABM} are mapped to the filtered FB voltage $V_{FB,filtered}$, as shown in **Figure 19**.

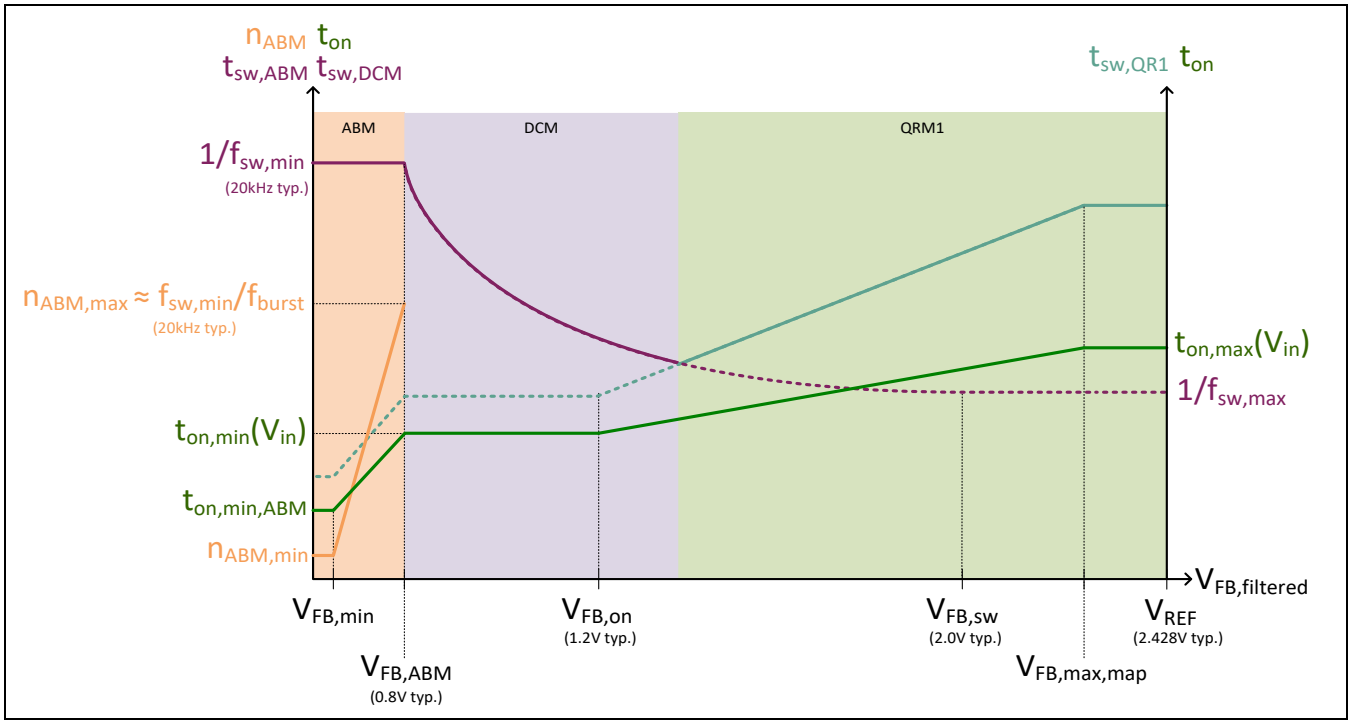


Figure 19 Multi-mode operation mapping based on filtered FB voltage $V_{FB,filtered}$

When $V_{FB,filtered}$ is the same as or higher than the $V_{FB,max,map}$ parameter, the power transfer is maximum, with the maximum switching frequency being limited to $f_{sw,max}$ and the on-time based on $t_{on,max}(V_{in})$ if the CS pin voltage does not exceed $V_{OCP1}(V_{in})$.

At maximum power transfer, the double line frequency ripple on the FB pin signal is high. With the notch filter enabled, such ripple can be suppressed in $V_{FB,filtered}$. Hence, $V_{FB,max,map}$ should be configured well below V_{REF}.

When $V_{FB,filtered}$ is the same as or lower than the $V_{FB,min}$ parameter, the power transfer is minimum, with ABM minimum on-time $t_{on,min,ABM}$ and ABM minimum pulse number $n_{ABM,min}$. As described in **Section 13**, $V_{FB,min}$ should be configured as per $V_{CE,sat}$ based on the optocoupler datasheet.

$V_{FB,ABM}$ parameter is the $V_{FB,filtered}$ threshold for the transition between ABM and DCM. To enter ABM from DCM, $V_{FB,filtered}$ needs to be below the $V_{FB,ABM}$ threshold, for a minimum time-out based on the $t_{ABM,blank}$ parameter. In ABM, if $V_{FB,filtered}$ rises above the $V_{FB,ABM}$ threshold, DCM is entered.

The on-time ramp increases from $t_{on,min}(V_{in})$ at $V_{FB,on}$, until $t_{on,max}(V_{in})$ is reached at $V_{FB,max,map}$.

Note: *$t_{on,min}(V_{in})$ and $t_{on,max}(V_{in})$ are the on-time limit variables, which are dependent on the estimated input voltage V_{in}. For more details, please refer to **Section 14.2**.*

The switching period ramp increases from $1/f_{sw,max}$ at $V_{FB,sw}$, until $1/f_{sw,min}$ is reached at $V_{FB,ABM}$. When the QR first valley switching period $t_{sw,QR1}$ is above this switching period ramp, QRM1 is entered. When $t_{sw,QR1}$ is below this switching period ramp, DCM is entered.

Note: *$f_{sw,max}$ and $f_{sw,min}$ are respectively the maximum and minimum switching frequency parameters.*

As shown in **Figure 19**, the typical values of $V_{FB,ABM}$, $V_{FB,on}$ and $V_{FB,sw}$ are fixed as 0.8 V, 1.2 V and 2.0 V, respectively.

Referring to **Table 8**, the recommended parameter configuration for FB voltage mapping and mode transition is selected in this design example.

Table 8 Parameter configuration related to FB voltage mapping and mode transition

Parameter name	Recommended value	Unit
$V_{FB,max,map}$	2.0	V
$V_{FB,min}$	$V_{CE,sat}$ (refer to optocoupler datasheet)	V
$t_{ABM,blank}$	6.5	Ms

14.5 FB voltage maximum limit ramp

Whenever the regulated mode is entered, the filtered FB voltage maximum limit $V_{FB,filtered,max}$ is ramped up from $V_{FB,limit,start}$ (1.2 V typ.) to V_{REF} (2.428 V typ.), with incremental voltage step based on the $V_{FB,limit,step}$ parameter and time step based on the half sine wave period.

As shown in **Figure 20**, when $V_{FB,filtered}$ is higher than $V_{FB,filtered,max}$ initially on entering regulated mode, the FB voltage mapping is based on $V_{FB,filtered,max}$ ramp, in order to prevent excessive output rise overshoot. When $V_{FB,filtered}$ gets lower than $V_{FB,filtered,max}$, the FB voltage mapping is then based on $V_{FB,filtered}$.

As a start, **$V_{FB,limit,step}$ = 800 mV** is generally recommended. It can be reduced later after successful powering-up of the system, if there is excessive output rise overshoot found during the start-up test.

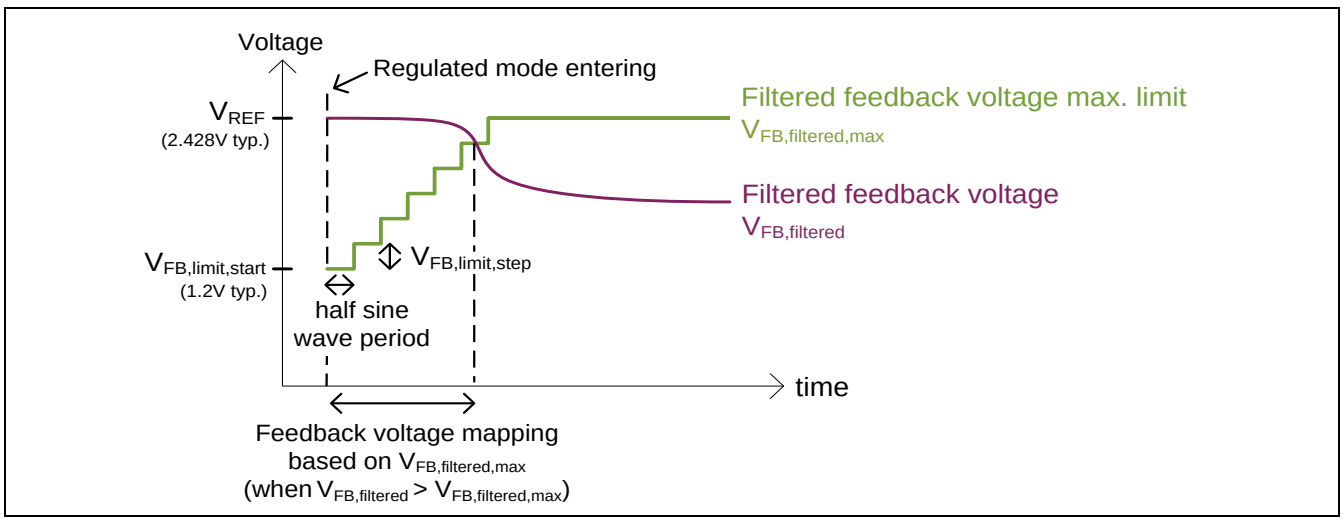


Figure 20 FB voltage maximum limit ramp when entering regulated mode

15 Other protection-related parameters

15.1 V_{CC} OVP

The V_{CC} Over Voltage Protection (OVP) reaction is configurable to latch-mode or auto-restart, based on the $Reaction_{VCC,OVP}$ parameter, while the V_{CC} OVP level is configurable based on the $V_{VCC,max}$ parameter.

$Reaction_{VCC,OVP}$ = Latch-Mode and **$V_{VCC,max}$ = 23 V** are recommended and selected in this design example. Based on $V_{VCC,max}$ = 23 V, V_{CC} capacitor voltage rating of 25 V is selected.

15.2 Regulated mode V_{CC} UVP

$EN_{VCC,UVP}$ parameter refers to the enable switch for the regulated mode V_{CC} Under Voltage Protection (UVP). The protection reaction is fixed as auto-restart and it is triggered when V_{CC} voltage is the same as or lower than regulated mode V_{CC} UVP $V_{VCC,min}$, for longer than a blanking period based on $t_{VCCUV,blank}$.

$EN_{VCC,UVP}$ = Enabled, **$V_{VCC,min}$ = 7.5 V** and **$t_{VCCUV,blank}$ = 1.5 ms** parameter settings are recommended and selected in this design example.

15.3 IC over-temperature protection

The IC over-temperature protection level is based on the $T_{critical}$ parameter. If $T_{critical}$ is configured above 119°C, the maximum switching frequency parameter $f_{sw,max}$ cannot be configured above 136.4 kHz. The protection reaction is fixed as auto-restart, while the maximum junction temperature for start-up/restart is fixed as 4°C below $T_{critical}$.

$T_{critical}$ = 119°C is recommended and selected in this design example.

Note: XDPL8218's lifetime is not guaranteed when operating junction temperature is above 125°C, which is possible if $T_{critical}$ is configured above 119°C, with temperature sensing tolerance of ± 6°C.

15.4 Primary MOSFET over-current protection

V_{OCP2} denotes the CS pin voltage level 2 for primary MOSFET over-current protection. Under the single-fault condition of shorted primary main winding, the primary MOSFET over-current protection is triggered when the CS pin voltage exceeds V_{OCP2} for longer than a blanking time based on the t_{CSOCP2} parameter.

t_{CSOCP2} = 240 ns is recommended and selected in this design example.

V_{OCP2} level is automatically selected based on the $V_{OCP1,at,V,in,low}$ setting, as shown in **Table 9**. In this design example, $V_{OCP1,at,V,in,low}$ = 0.52 V is selected, so V_{OCP2} = 0.8 V is applied. The protection reaction is fixed as auto-restart.

Table 9 Automatic V_{OCP2} level selection based on $V_{OCP1,at,V,in,low}$ parameter configuration

$V_{OCP1,at,V,in,low}$ configuration (V)	V_{OCP2} (V)
0.34 ~ 0.36	0.6
0.37 ~ 0.54	0.8
0.55 ~ 0.72	1.2
0.73 ~ 1.08	1.6

15.5 Debug mode

The parameter setting of **$Debug_{Mode}$ = Disabled** is selected in this design example. The $Debug_{Mode}$ parameter should only be enabled for debugging purposes. For more details on XDPL8218 debug mode, please refer to **Section 19.2**.

16 PCB layout guide

a) Minimize the circumference of the following high-current/high-frequency loop with traces which are short and wide (or with jumper wires which are short and thick).
- Power switch loop formed by DC link filter capacitor $C_{DC,filter}$, primary main winding, flyback MOSFET and CS resistor R_{CS}.
- Main output rectifier loop formed by secondary main winding, main output diode and main output capacitor.
- Auxiliary output rectifier loop formed by auxiliary winding, auxiliary output diode and auxiliary output capacitor.

b) Place each filter capacitor, V_{CC} noise decoupling capacitor $C_{VCCdecouple}$, ZCD pin filter capacitor C_{ZCD} and FB pin filter capacitor C_{FB} near to its designated pin and the GND pin of the controller.

c) Apply the following guide for star grounding.
- Connect ground signal traces of $C_{VCCdecouple}$, C_{ZCD}, $R_{ZCD,2}$, C_{FB}, the controller GND pin and the optocoupler emitter pin.
- Connect V_{CC} ground traces of the V_{CC} capacitor C_{VCC} and primary auxiliary winding.
- Connect the C_{HV} GND pin near to the ground pin of $C_{DC,filter}$.
- Connect the GND pin of each C_{VCC}, $C_{VCCdecouple}$, R_{CS} and bridge rectifier separately to a single point near $C_{DC,filter}$.

d) Ensure the high dv/dt traces from the MOSFET drain and GD pin are as far as possible from the FB pin and its connected trace.

e) Shield signal traces with ground traces or ground plane, which can help to reduce noise pick-up.

f) Always ensure appropriate safety clearances between the HV and LV nets.

17 Parameter configuration list, set-up and procedures

17.1 Parameter configuration list

Figure 21 shows the XDPL8218 parameter configuration list, with selected values based on the design examples from **Section 2** to **Section 15**. For another system design, the values in the list can be different.

For the IC parameter configuration set-up and procedures, please refer to **Section 17.2** and **Section 17.3**. For safety purposes, before powering up the board, it is important to ensure that the configured IC parameter values in the hardware configuration section in **Figure 21** are compatible with the actual system hardware dimensioning.

Hardware configuration		
N_p	32.000	
N_s	10.000	
N_a	3.000	
L_p	0.5440	mH
R_CS	0.200	ohm
R_ZCD_1	27.00	kohm
R_ZCD_2	3.90	kohm
C_VCC	22.00	uF
V_out_cap_rating	80	V
R_HV	52.00	kohm
I_GD_pk	30	mA
Startup		
n_ss	3	
V_out_start	27.0	V
V_start_OCP1	0.52	V
V_OCP1_init	0.300	V
Protections		
t_auto_restart	1.2	s
V_OCP1_at_V_in_low	0.52	V
V_OCP1_at_V_in_high	0.34	V
V_in_low	82.0	V
V_in_high	326.0	V
t_CSOCP2	240	ns
Reaction_OVP_Vout	Auto-Restart	
V_outOV	65.0	V
V_outUV_start	27.0	V
EN_UVP_Vout	Enabled	
Reaction_UVP_Vout	Auto-Restart	
V_outUV	33.0	V
t_VoutUV_blank	500.0	ms
EN_OVP_In	Enabled	
EN_UVP_In	Enabled	
EN_VIN_ABM	Enabled	
V_inOV	350.0	V
V_in_start_max	326.0	V
V_in_start_min	82.0	V
V_inUV	70.0	V
P_foldback_gain	1.00	
Reaction_VCC_OVP	Latch-Mode	
V_VCC_max	23.0	V
EN_VCC_UVP	Enabled	
V_VCC_min	7.5	V
t_VCCUV_blank	1.5	ms
T_critical	119	degreeC
Debug_Mode	Disabled	

Multimode		
R_FB_pull_up	5.5	kohm
N_quality	1.6	
n_notch_blank	2	
f_sw_max	136.0	kHz
t_on_min	1.38	us
t_min_demag	4.0	us
t_on_max_at_V_in_low	15.00	us
f_burst	130	Hz
n_ABM_min	1	
t_on_min_ABM	1.00	us
t_ABM_blank	6.50	ms
n_wakeup	5	
V_FB_max_map	2.000	V
V_FB_min	0.30	V
V_FB_limit_step	800.000	mV
Power factor correction		
C_EMI	0.2200	uF
Fine tuning		
t_ZCDPD	350	ns
R_in	10.60	ohm
User ID		
User_ID_A	0	

Figure 21 IC parameter configuration list with selected values based on design examples from Section 2 to Section 15

*Note: $User_{ID,A}$ parameter in **Figure 21** has no effect on the IC behavior and system performance. By default, the value of this parameter is set to zero. If necessary, it can be configured to store system information, such as parameter version, LED driver model, etc.*

17.2 Parameter configuration set-up

The tools needed for on-board XDPL8218 parameter configuration are listed in **Table 10**.

Table 10 Tools needed for XDPL8218 parameter configuration

Tool type	Tool name	Description	Ordering/Download link	Ordering/Download content
Hardware	.dp Interface Gen2	.dp Interface board	IF-BOARD.DP-GEN2	.dp Interface Gen2 x 1 USB cable x 1
Software	.dp Vision	GUI for parameter configuration of all .dp products	.dp Vision *Note:* *Please install .dp Vision before running the XDPL8218 .dp Vision folder setup file shown below.*	Latest version of the .dp Vision installer (*.exe)
	XDPL8218 parameter csv file	XDPL8218 parameter configuration file	XDPL8218 40W reference board homepage *Note:* *Please download the zipped package which contains the .dp Vision folder setup file (*.msi)*	Latest version of .dp Vision folder setup file (*.msi), which installs the following XDPL8218 40 W reference design engineering report (*.pdf) and parameter configuration file (*.csv), including images for the configuration file. XDPL8218 design guide (*.pdf)

Figure 22 shows the hardware set-up needed for the on-board XDPL8218 parameter configuration.

Note: Please ensure the board is not supplied with any voltage before connecting the programmable cable to the target XDPL8218 board. For parameter configuration on the XDPL8218 40 W reference design, please connect the programming cable to its configuration connector X2.

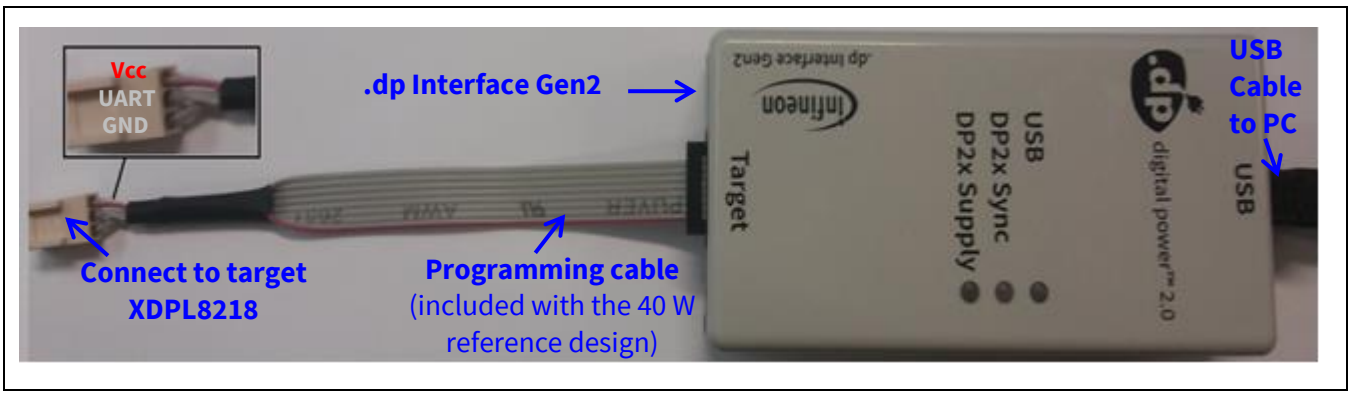


Figure 22 Hardware set-up for on-board XDPL8218 parameter configuration

17.3 Parameter configuration procedures

After the hardware connections for XDPL8218 configuration (see **Figure 22**) are done, please start the program by clicking the shortcut ".dp Vision" on the desktop.

Note: During the program start-up, if the system shows there is a newer version of .dp Vision, please follow the procedure and update accordingly. As the screenshots were taken based on .dp Vision version 2.0.9.1, it might look different for newer versions of .dp Vision.

A .dp Vision user manual is available by clicking [Help] >> [Help contents], to provide the detailed instructions on how to use this GUI for parameter configuration. Alternatively, the following simple guide is also available for quick and easy reference.

Open the XDPL8218 parameter configuration file (*.csv) from the default installation folder of the project add-on at ***C:\Users\<Username>\Infineon Technologies AG\.dp vision\Parameters***, as shown in **Figure 23**.

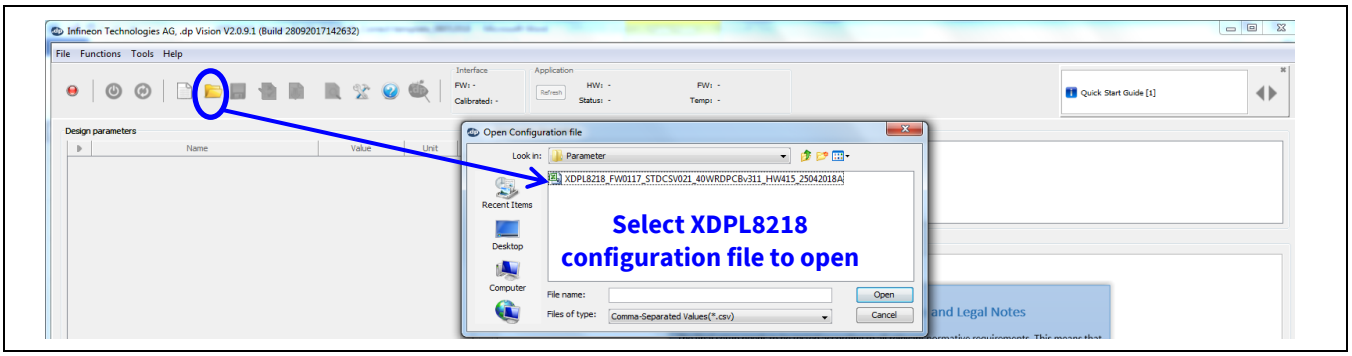


Figure 23 Opening the XDPL8218 parameter configuration file (*.csv) in .dp Vision

After opening the parameter csv file, a list of configurable parameters with default values based on the reference board design will be shown (see the box on the left in **Figure 24**). These default values can be changed for another board design, by referring to the design guide from **Section 2** to **Section 15** and the fine-tuning guide in **Section 18**.

If a parameter value is changed and no limit violation is found, the changed value itself will turn blue, like the example in **Figure 24** in which the R_{cs} parameter in the hardware configuration section has been changed from 0.2 Ω to 0.18 Ω. Otherwise, if an error is detected (e.g. exceeded min./max. value), the parameter value which caused the error will turn red and the message bar of .dp Vision (see the top right in **Figure 24**) will show an error message. If any error is not resolved, the user is not allowed to configure the IC with the changed value.

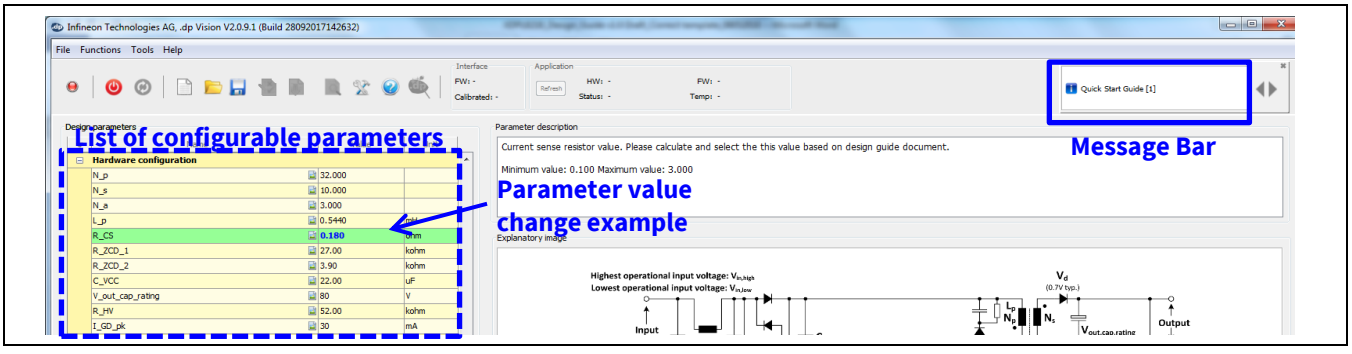


Figure 24 Changing parameter values of XDPL8218 configuration file in .dp Vision

Note: For safety and proper system functioning, it is important to ensure the hardware configuration section parameter values are compatible with the actual system hardware dimensioning.

There are two options available to configure the IC based on the list of parameter values shown in .dp Vision.

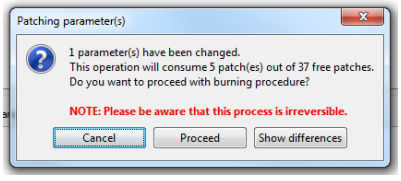
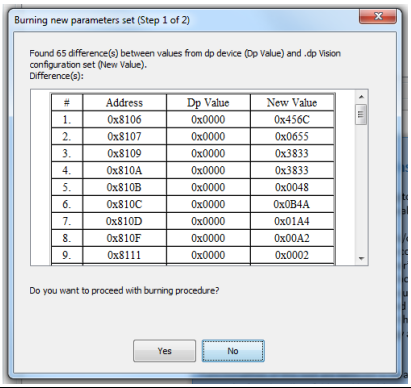
- Burn configuration

  It is important to note that the new XDPL8218 chip from Infineon does not contain any parameter configuration by default, so the user should first burn a full set of parameters on the new chip using this function, before any application testing. If the XDPL8218 chip on board has already been burned with a first full set of parameters in its One-Time Programmable (OTP) memory space, such as the XDPL8218 40 W reference board, any IC parameter value change on it with this option is considered as parameter patching. There are total 77 patchable OTP memory spaces.

  Each time the burn configuration function is executed, .dp Vision will detect if there is parameter value difference between the saved configuration file and the target XDPL8218. If a difference is detected, each burn configuration will consume a minimum of three patchable memory spaces. However, the process will be aborted if it requires more memory space than what is available on the target IC. In that case, the user will have to replace the XDPL8218 chip with a new one in order to burn the configuration.

  Table 11 shows the recommended procedures for using the burn configuration function in .dp Vision to burn a first full set of parameters or patch the parameters into the OTP memory.

Table 11 Burn configuration procedures

Step	Instruction
I	Open configuration file using .dp Vision (see example in **Figure 23**).
II	If necessary, change any parameter value (see example in **Figure 24**), then click [File] >> [Save] or [File] >> [Save as] to save the configuration file. Otherwise, proceed to step III.
III	Ensure that the primary supply voltages (e.g. AC input) to the board are switched off or disconnected, and the hardware connection for configuration is OK based on **Figure 22**.
IV	Click  to supply power and establish a connection to the target XDPL8218. After this step, XDPL8218 will be in configuration mode (with V_{CC} voltage for OTP programming at 7.5 V ± 0.15 V) and the device status  should change to .
V	Click  to burn the configuration to the target XDPL8218. After this step, you should see a pop-up window, which is similar to one of those below.  OR 
VI	Click “Proceed” or “Yes” to burn/patch the configuration. After this step, a pop-up window should show that the burning/patching is successful.
VII	Click “OK” on the pop-up window, then disconnect the programming cable from the XDPL8218 configuration connector and test the application, if needed.

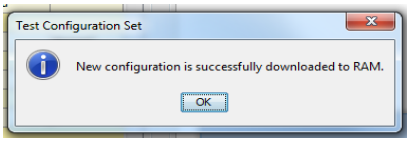
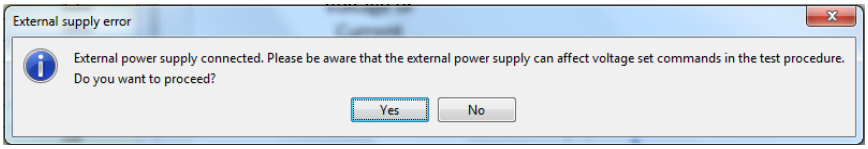
– Test configuration

This function will download the parameter values from the list in .dp Vision into the XDPL8218 RAM, followed by an automatic IC start-up, for application testing with the new configuration.

Unlike using the burn configuration, parameter configuration with this option is not permanent because the loaded RAM contents will be lost once the IC supply voltage is turned off, but the advantage of using this option is that it does not consume OTP memory space, thus there is no limit on the number of parameter value changes.

Table 12 shows the recommended procedures for using test configuration functions in .dp Vision to load the new parameter values to the RAM and test the application with the new configuration.

Table 12 Test configuration procedures

Step	Instruction
I	Open the configuration file using .dp Vision (see example in **Figure 23**).
II	Ensure that the primary supply voltages (e.g. AC input) to the board are switched off and the hardware connection for configuration is OK based on **Figure 22**.
III	If necessary, change any parameter value (see example in **Figure 24**). Otherwise, proceed to step IV.
IV	Click  to supply power and establish a connection to the target XDPL8218. After this step, XDPL8218 will be in configuration mode and the device status  should change to .
V	Ensure the board test set-up (e.g. output load) is OK, then apply the AC input to the board. After this step, the board does not start up because XDPL8218 is still in configuration mode.
VI	Click  to test the new configuration with the target XDPL8218.
VII	If the IC automatically starts up with the new configuration, you should see a pop-up window like the one shown below. Click “OK” to proceed.  *Note: If there is any protection being triggered after step VI, the pop-up window would show that the test configuration is unsuccessful instead; please refer **Section 19.2** for firmware status code read-out in debug mode.*
VIII	To test another configuration change, repeat steps II to VII. If the following message box appears in between the steps, click “Yes” to proceed.  Otherwise, turn off the AC input and disconnect the programming cable from the XDPL8218 configuration connector.

Note: If any error occurs during the burn configuration or test configuration procedures, please refer to the message bar of .dp Vision for the error description. For more details, please refer to the .dp Vision user manual.

18 Fine-tuning guide

This section presents guidelines for how to fine-tune the value of a few essential XDPL8218 parameters, based on the actual measurement waveform or data.

18.1 Input voltage-sensing parameter fine-tuning

When the primary MOSFET is switched on, the XDPL8218 measures the current flowing out of the ZCD pin $-I_{IV}$, to estimate the DC link filter capacitor voltage $V_{DC,filter}$.

Ideally, $V_{DC,filter}$ should be a low-frequency (e.g. typically 100 Hz ~ 120 Hz) rectified sinusoidal waveform, as shown in **Figure 25**, where the peak value of $V_{DC,filter}$ is equal to AC input peak value $V_{in,peak}$, and the estimated input voltage V_{in} in rms value is assumed to be 0.707 times $V_{in,peak}$. However, due to the input line filter impedance and the filter capacitor ESR, the actual $V_{DC,filter}$ has high switching frequency ripple (in the kHz range) over the low-frequency sinusoidal waveform, whose ripple peak-to-peak voltage level varies based on the peak current being drawn by the transformer primary main winding. Step III of **Table 13** shows an example of the actual $V_{DC,filter}$ waveform.

To improve the input voltage estimation accuracy, R_{in} parameter fine-tuning is important for the IC to estimate the correct $V_{in,peak}$ by compensating such switching frequency ripples, which appears in $-I_{IV}$ measurements as well.

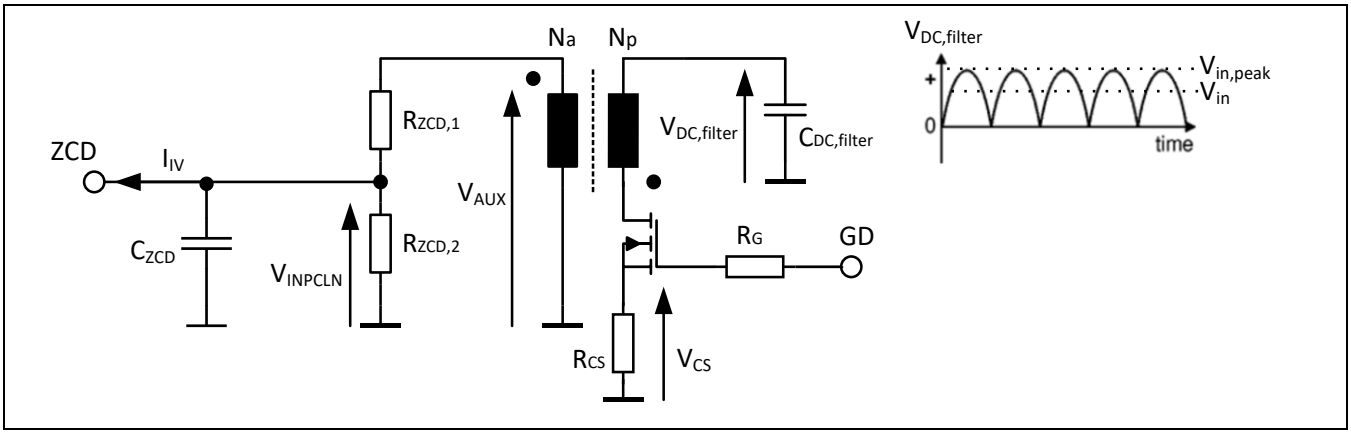
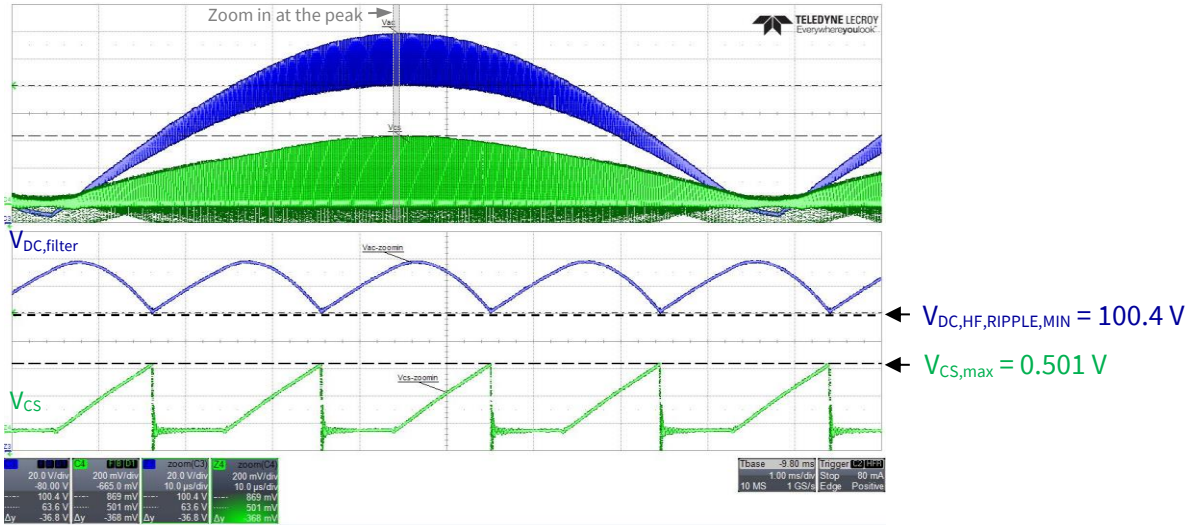


Figure 25 $-I_{IV}$ measurement for input voltage sensing

Table 13 shows the recommended procedures for R_{in} parameter fine-tuning.

Table 13 Recommended procedures for R_{in} parameter fine-tuning

Step	Instruction
I	Apply two voltage probes on the board, which respectively measure the waveform of the DC link filter capacitor voltage $V_{DC,filter}$ and CS pin voltage V_{CS}.
II	Ensure the target XDPL8218 has already been burned with at least a first full set of parameters. Power up the board with normal operational minimum AC input voltage $V_{AC,min}$ and full load output. If it cannot be powered up, retry by burning the input UVP to enable switch parameter $EN_{UVP,In}$ as “Disabled” (if it was not before) or refer **Section 19** for the debugging guide.
III	Capture the voltage waveform with a time base of 1 ms and zoom into the peak voltage for measuring the minimum level of the $V_{DC,filter}$ high-frequency voltage ripple ($V_{DC,HF,RIPPLE,MIN}$) and the maximum level of V_{CS} ($V_{CS,max}$). Below is an example of a waveform captured on the 40 W reference design with $V_{AC,min}$ = 90 V_{rms}, F_{line} = 60 Hz and full-load output (I_{out} = 0.8 A).

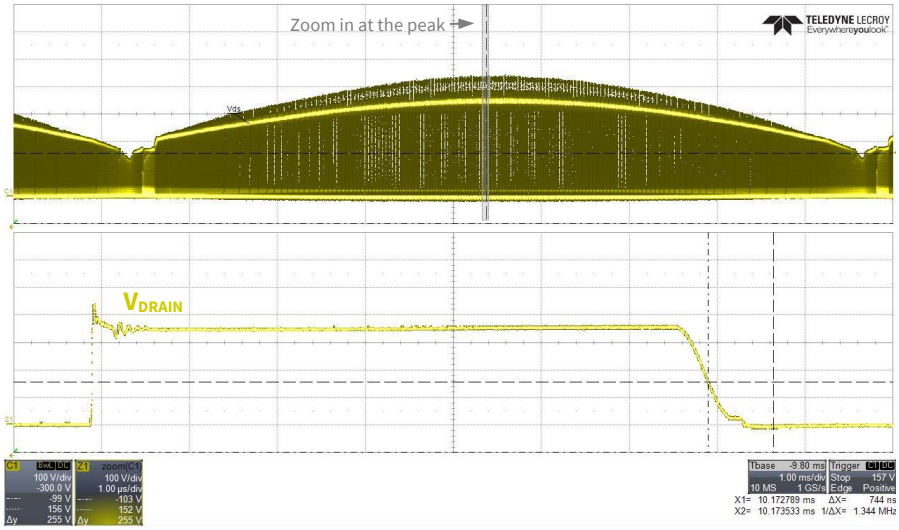
	
IV	Turn off the AC input. Calculate R1 with the equation below and voltage measurements from step III: $R1 = R_{CS} \cdot \left(\frac{\sqrt{2} \cdot V_{AC,min} - V_{DC,HF,RIPPLE,MIN}}{V_{CS,max}} \right)$, based on full load output Calculation example based on 40 W reference design with $V_{AC,min}$ = 90 V_{rms}, F_{line} = 60 Hz and full-load output (I_{out} = 0.8 A): $R1 = 0.2 \cdot \left(\frac{\sqrt{2} \cdot 90 - 100.4}{0.501} \right) = 10.73\ \Omega$
V	Repeat step III to obtain another measurement of $V_{DC,HF,RIPPLE,MIN}$ and $V_{CS,max}$ based on 33 percent load.
VI	Turn off the AC input. Calculate R2 with the equation below and voltage measurements from step V: $R2 = R_{CS} \cdot \left(\frac{\sqrt{2} \cdot V_{AC,min} - V_{DC,HF,RIPPLE,MIN}}{V_{CS,max}} \right)$, based on 33 percent load output Calculation example based on 40 W reference design with $V_{AC,min}$ = 90 V_{rms}, F_{line} = 60 Hz and 33 percent load output (I_{out} = 0.265 A): $R2 = 0.2 \cdot \left(\frac{\sqrt{2} \cdot 90 - 116.6}{0.281} \right) = 7.59\ \Omega$
VII	Calculate the fine-tuned R_{in} parameter value with the following equation: $Fine\ tuned\ R_{in} = 0.5 \cdot (R1 + R2) + R_{ds(on),25°C} + R_{dc,pri,winding} + R_{CS}$ Where $R_{ds(on),25°C}$ is the MOSFET drain-source on-resistance at 25°C, and $R_{dc,pri,winding}$ is the primary main winding DC resistance. Calculation example based on 40 W reference design: $Fine\ tuned\ R_{in} = 0.5 \cdot (10.73 + 7.59) + 0.9 + 0.265 + 0.2$ $\boldsymbol{Fine\ tuned\ R_{in} \approx 10.5\ \Omega}$
VIII	Use the burn configuration in .dp Vision to patch the R_{in} parameter with the value from step VII and also enable the $EN_{UVP,In}$ parameter (if it was set to “Disabled” before). Then, verify the AC input UVP accuracy at full load and low load.

18.2 QR valley switching parameter fine-tuning

Unlike conventional analog solutions which achieve QR valley switching by introducing an external hardware delay on the zero-crossing signal with the ZCD pin capacitor, the XDPL8218 ZCD pin capacitor is mainly used for noise filtering only. Therefore, a fixed capacitor value, e.g. 47 pF, can be used across designs of different power classes. To achieve QRM1, the XDPL8218 dynamically measures the resonant period and delays the MOSFET switch-on by a quarter of the resonant period after zero-crossing of the primary auxiliary winding voltage.

t_{ZCDPD} parameter fine-tuning is, however, necessary to compensate for XDPL8218 internal propagation delay in ZCD and also external delay caused by the noise-filtering capacitor at the ZCD pin. **Table 14** shows the recommended procedures for t_{ZCDPD} parameter fine-tuning.

Table 14 Recommended procedures for t_{ZCDPD} parameter fine-tuning

Step	Instruction
I	Apply a differential probe on the board to measure the flyback MOSFET drain voltage waveform.
II	Set the t_{ZCDPD} parameter to 0 and use the test configuration function in .dp Vision to power up the board with low AC input voltage, e.g. 120 V_{rms}, and full-load output. If the board cannot be powered up, please refer to **Section 19** for the debugging guide.
III	Capture the waveform with a 1 ms time base and zoom into the voltage peak with a 1 µs time base.
IV	Place a horizontal cursor at the highest possible level which crosses two points on the resonance part of the waveform (see a and b below), and measure the time between them (t_{a-b}). In the example below, which is based on the 40 W reference design, t_{a-b} is measured to be approximately 744 ns. 
V	Set the t_{ZCDPD} parameter as approximately half of t_{a-b} and burn the configuration with .dp Vision.
VI	Disconnect the programming cable after burning, then power up the board and the flyback MOSFET drain voltage waveform should be switching at the QRM1 (see example below based on the 40 W reference design with **fine-tuned t_{ZCDPD} = 370 ns**). 

18.3 Input power quality related parameter fine-tuning

The enhanced PFC feature can be enabled by configuring the C_{EMI} parameter above zero and fine-tuning the value to compensate for the current displacement effect, which is mainly caused by the DC link filter capacitor. A higher C_{EMI} parameter value gives higher compensation and vice versa.

The recommended starting value of the C_{EMI} parameter is the value of the DC link filter capacitor $C_{DC,filter}$ placed after the bridge rectifier. If necessary, fine-tune the C_{EMI} parameter using the test configuration function in .dp Vision, to achieve the optimized power factor and iTHD. For example with the XDPL8218 40W reference design, the initial C_{EMI} based on $C_{DC,filter}$ is 0.22 μF for powering up of the board, and **fine-tuned C_{EMI} = 0.2 μF** parameter is then selected for performance optimization.

In QRM1, the maximum switching frequency parameter $f_{sw,max}$ affects the number of first valley switching pulses over every AC input half sine wave period. To lower the iTHD at high input voltage and high output power, the number of first valley switching pulses can be reduced by lowering $f_{sw,max}$. However, please note that the efficiency could be reduced if the number of first valley switching pulses is reduced.

19 Debugging guide

This section presents guidelines for system debugging if the board has any problems with powering up or shutting down during testing.

19.1 Pin signal debugging

Scenario I: V_{CC} voltage stays above V_{CC} turn-off threshold (6 V typ.) and the UART pin signal toggles every 0.4 sec for a duration of $t_{auto,restart}$ before every restart. See an example in **Figure 26**.

This scenario means a protection with auto-restart reaction has been triggered. It is recommended to activate the XDPL8218 debug mode for firmware status code read-out in this case, to know exactly which protection has been triggered. For more details on the XDPL8218 debug mode, please refer **Section 19.2**.

*Note: As shown in **Figure 26**, the actual auto-restart time of a protection with auto-restart time is typically longer than the configured $t_{auto,restart}$ value, due to an additional time of $t_{VCCON,recharge}$ needed for V_{CC} recharging to V_{CC} turn-on threshold (20.5 V typ.) before every restart.*

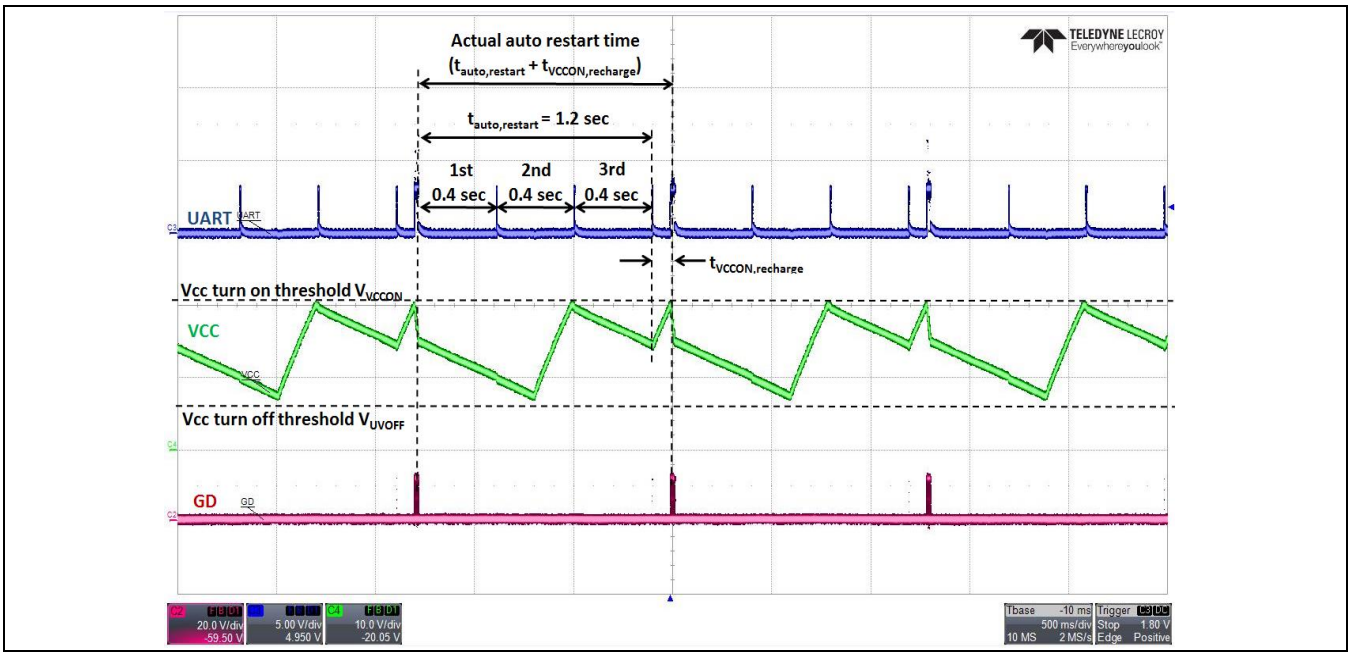


Figure 26 Scenario I waveform example (protection with auto-restart reaction)

Scenario II: V_{CC} stays above V_{CC} turn-off threshold (6 V typ.) and the UART pin always stays low. See an example in **Figure 27**.

This scenario means a protection with latch-mode reaction has been triggered. It is recommended to activate the XDPL8218 debug mode for firmware status code read-out in this case, to know exactly which protection has been triggered. For more details on the XDPL8218 debug mode, please refer to **Section 19.2**.

As there are only a few system protections in which the reaction can be configured to latch-mode, an alternative debugging option could be to identify which system protection with latch-mode reaction, after its reaction is configured to auto-restart, would cause the triggered protection waveform change from scenario II to scenario I.

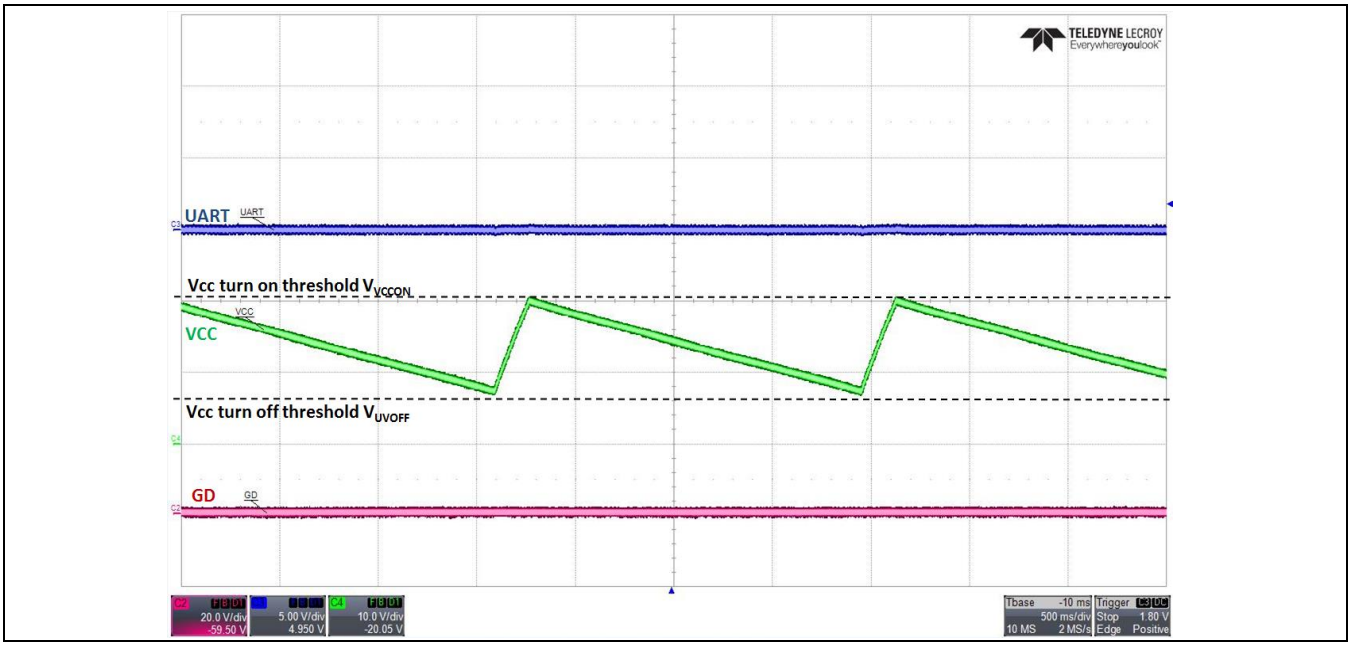


Figure 27 Scenario II waveform example (protection with latch-mode reaction)

Scenario III: V_{CC} hits V_{CC} turn-off threshold (6 V typ.) and followed by GD pin signal switching restarts after every V_{CC} recharge to V_{CC} turn-on threshold (20.5 V typ.). See an example in **Figure 28**.

This scenario means the V_{CC} Under Voltage Lockout (UVLO) protection has been triggered, which is likely caused by either one of the following:

- Issue(s) with V_{CC} supply circuit or/and start-up related parameter.
- Debug mode enabled, plus any protection triggering. For more details on the XDPL8218 debug mode, please refer **Section 19.2**.

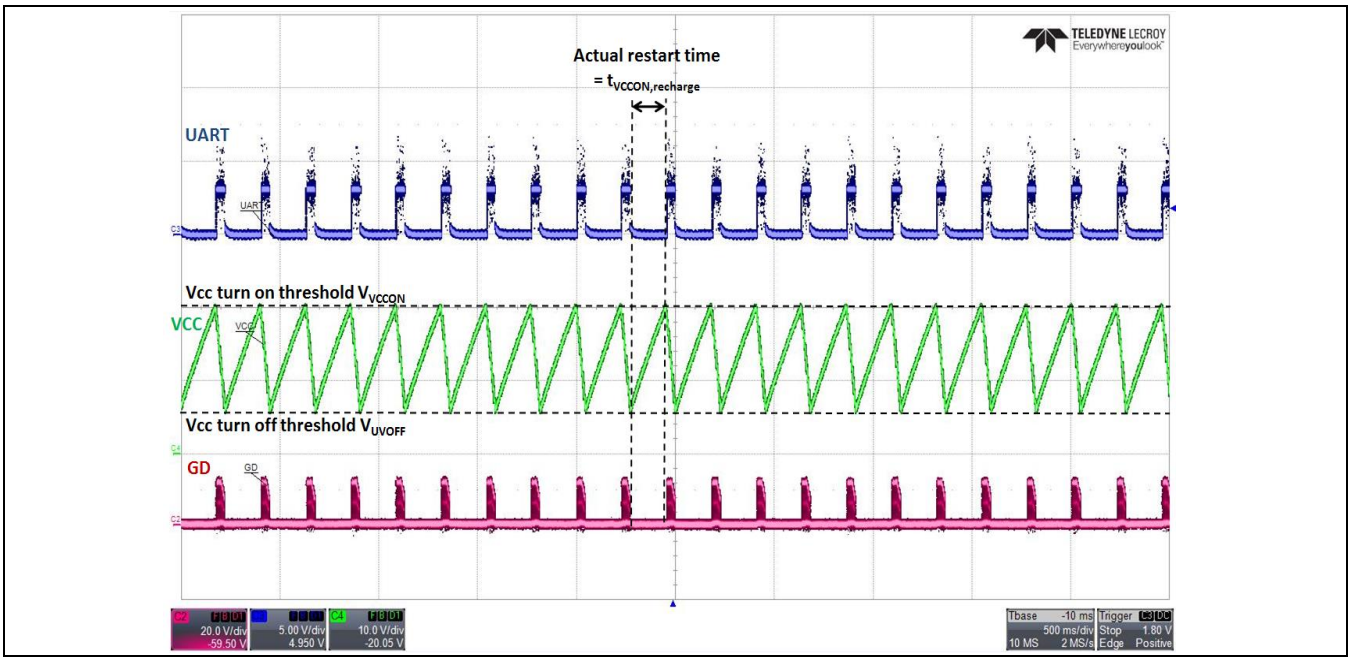


Figure 28 Scenario III waveform example (V_{CC} UVLO protection)

Scenario IV: V_{CC} repeatedly hits V_{CC} turn-off threshold (6 V typ.) and the GD pin signal always stays low despite V_{CC} recharge to the turn-on threshold (20.5 V typ.). See an example in **Figure 29**.

This scenario means the configuration mode has likely been entered due to no parameter at start-up. To avoid this, please burn the first full set of parameters to the XDPL8218 chip.

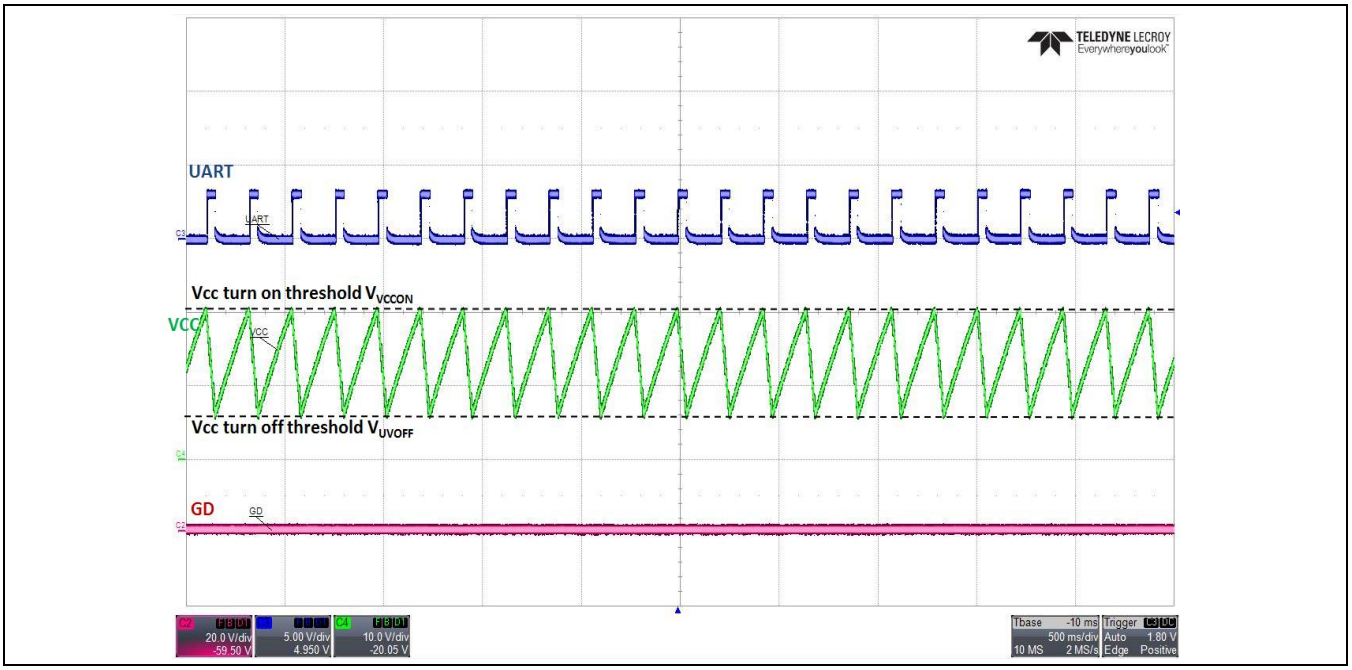


Figure 29 Scenario IV waveform example (configuration mode entered with no parameter at start-up)

Scenario V: V_{CC} stays constant at approximately 7.5 V and the UART pin signal stays mostly high (see an example in **Figure 30**).

This scenario means the configuration mode has been entered due to IC activation by .dp Interface Gen2 before AC input is applied. To avoid this, disconnect the .dp Interface Gen2 before AC input is applied.

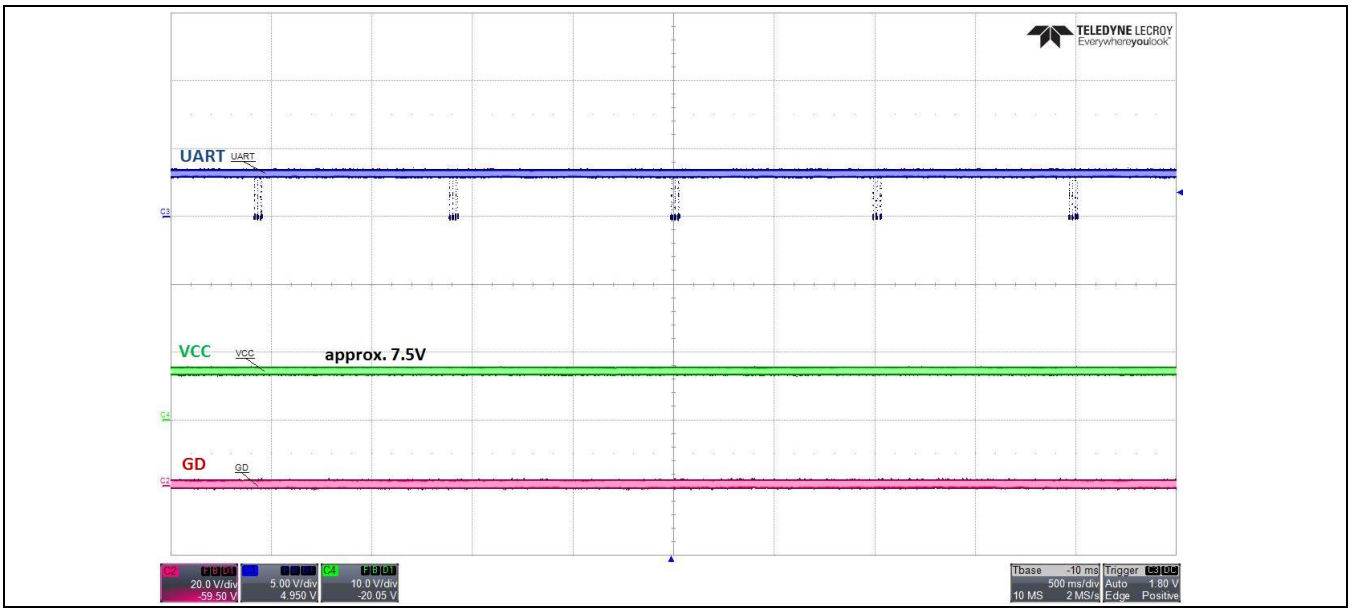


Figure 30 Scenario V waveform (configuration mode entering due to IC activation by .dp Interface Gen2 voltage supply, before AC input is applied)

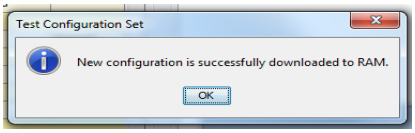
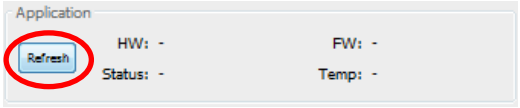
19.2 Firmware status code read-out procedures with debug mode

For further debugging, the XDPL8218 debug mode can be activated to read out the firmware status code, to identify which protection has been triggered.

Table 15 shows the recommended procedures for firmware status code read-out in debug mode.

*Note: $Debug_{Mode}$ parameter should only be enabled for debugging purposes along with the configuration set-up connection shown in **Figure 22**. For stand-alone board testing without connecting the .dp Interface Gen2, please ensure the $Debug_{Mode}$ parameter is set to disabled.*

Table 15 Procedures for firmware status code read-out in debug mode

Step	Instruction
I	Open the configuration file (see the example in **Figure 23**) used in the system which has the problem of powering up or shutting down, then set the $Debug_{Mode}$ parameter to “Enabled”.
II	Ensure that the AC input to the board is switched off and that the hardware connection for configuration is OK based on **Figure 22**, plus a low-ESR ceramic capacitor of 1 nF soldered across the UART pin and ground for noise decoupling.
III	Click  to supply power and establish connection to the target XDPL8218. After this step, the XDPL8218 will be in configuration mode and the device status  should change to .
IV	Supply the board with AC input and output conditions, which trigger the problem. After this step, the board does not start up because XDPL8218 is still in configuration mode.
V	Click  to test the configuration with the target XDPL8218. After this step, the IC will automatically start up in debug mode and you should see a pop-up window like the one shown below.  If any protection is triggered, the IC’s GD pin will stop switching and the output will stay low.
VI	Click “OK” in the pop-up window.
VII	Click the “Refresh” button in the .dp Vision application section and switch off the AC input. After this step, the firmware status code is read out. If any protection has been triggered after step V, the status code will show a value in red. Otherwise, it will show 0x0000 in black. 
VIII	Hover the mouse over the status code and the description of the status code will be shown. For example, 0x0040 means input UVP has been triggered.
IX	Apply the necessary counter-measure or repeat the steps above to debug again. Otherwise, ensure the AC input is switched off before disconnecting the programming cable from the XDPL8218 board.

20 References

[1] XDPL8218 datasheet

[2] REF-XDPL8218-U40W engineering report

Revision history

Document version	Date of release	Description of changes
V 1.0	2018-06-06	Initial version

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