How to design SMPS to Pass Common Mode Lightning Surge Test

Power Management & Supply



Never stop thinking.

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1 Introduction

Lightning surge is the most common source of overstresses. Overstresses in the form of overvoltage and overcurrent can happen in consumer equipments which contain tuner receiver like TV set, recordable DVD player etc, as it is exposed to the lightning strikes through the antenna and the AC line. Consumer equipment makers in general perform lightning surge test on their products before going into volume production. It is to ensure that the equipment can not be interrupted during operation or even damaged by the lightning surge. This application note is intended to advise the designer of switched mode power supply (SMPS) circuit in consumer equipments on how to properly design SMPS to avoid the disruptive influence and the damaging effect of the overstress by the lightning.

2 Overview of Lightning Surge Test Standards

Currently prevailing standards for the lightning surge test are the European standard IEC61000-4-5 and the Japanese standard JEC210/212. Table 1 shows the differences between the two standards.

Ref. Standard	JEC210/212	IEC61000-4-5
Test Voltage	7kV or special	0.5, 1, 2, 4kV or special
Pulse Waveform & output impedance Z	Open-circuit output voltage characteristic : Surge voltage waveform : 1.2/50 µs Output impedance, Z : not defined; some equipments use 6 Ω If the surge voltage is 30kV, it can generate 5kA short-circuit current (30kV/6Ω). Short-circuit output current characteristics : Surge current waveform : 8/20µs (refer to fig. 1) Output impedance, Z : not defined; some equipments use 5 Ω If the required surge current is 6kA, it needs to generate 30kV output voltage (6kA x 5Ω).	Open-circuit output voltage characteristic : Surge voltage waveform : 1.2/50 µs Output impedance, Z : 2 Ω If the surge voltage is 15kV, it can generate 7.5kA short-circuit current (15kV/2Ω). Short-circuit output current characteristics : Surge current waveform : 8/20µs (refer to fig.1) Output impedance, Z : 2 Ω If the required surge current is 7.5kA, it needs to generate 15kV output voltage (7.5kA x 2Ω).
Coupling to AC Lines (Power testing)	Not defined.	Differential mode : 18uF Common mode : 10 Ω + 9µF

Table 1 JEC standard vs IEC standard

The lightning testing current wave shape is defined in Figure 1. For an 8x20µs waveform, T1 = 8µs and T2 = 20µs. In general, surge voltage of ±2kV up to ±16kV, with increasing step of ±2kV, is applied across AC line as well as across one of the AC line and the chassis ground of the equipment under test (EUT), ie. L-N, L-G and N-G. The SMPS in the EUT, which is directly exposed to the surge power, must be undamaged and continue to operate properly after the surge is applied. Most of the equipment makers used JEC210/212 standard until early 1990 when IEC61000-4-5 was implemented. The IEC standard since then becomes very common.

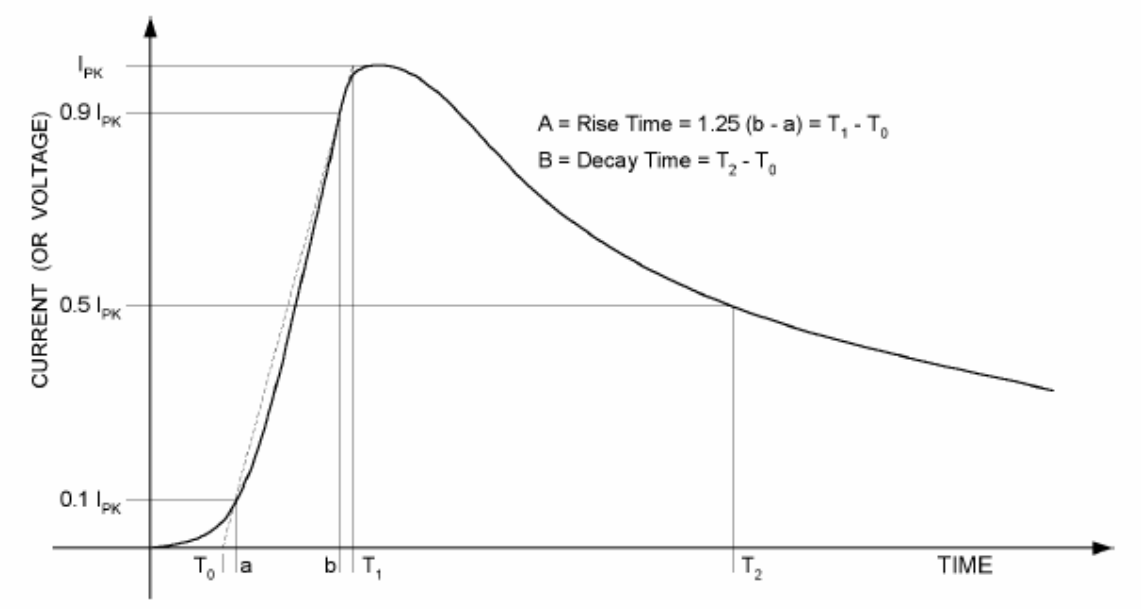

Figure 1 Lightning Pulse Waveform

3 Test Set-up

Figure 2 shows the complete lightning surge test setup. The LCD TV with the external SMPS adapter is used as the EUT. The lightning surge generator is an ideal voltage source with the specified waveform which is connected to its output ports with the known fixed resistance as in Table 1. It as well as the SMPS adapter gets the AC power from the isolation transformer. For the differential surge test, the surge voltage is applied across the AC lines of the SMPS adapter, whereas for the common mode surge test, it is applied across one of the AC line and the equipment's ground connection at the tuner's input socket of the TV-set. The number of strikes is 5 at each voltage step (2kV to 16kV) and at each polarity.

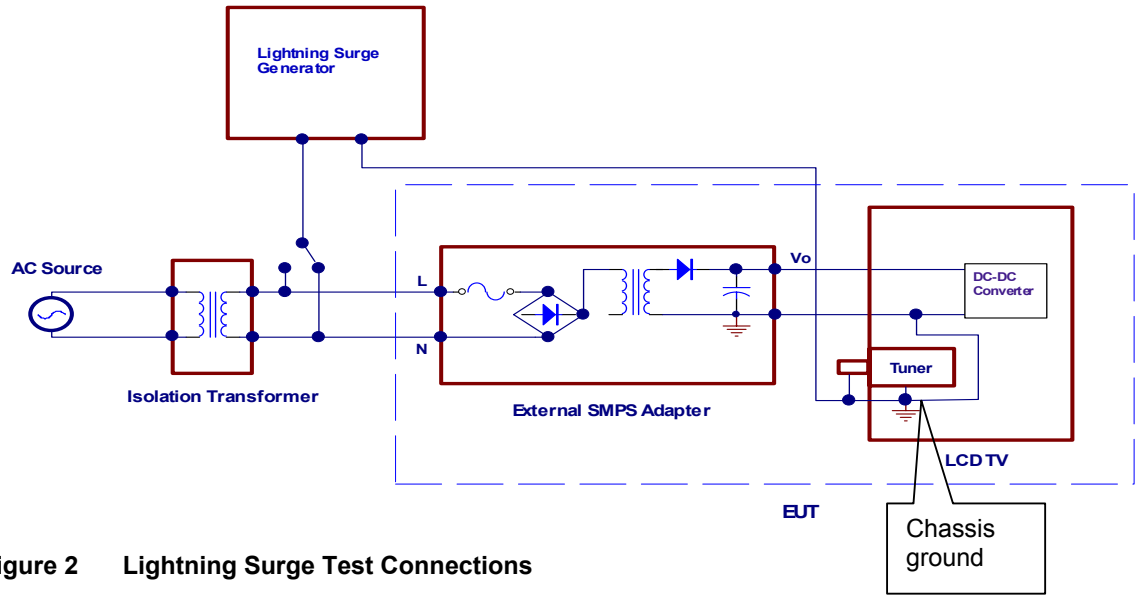

Figure 2 Lightning Surge Test Connections

4 How is IC interferenced by lightning surge voltage

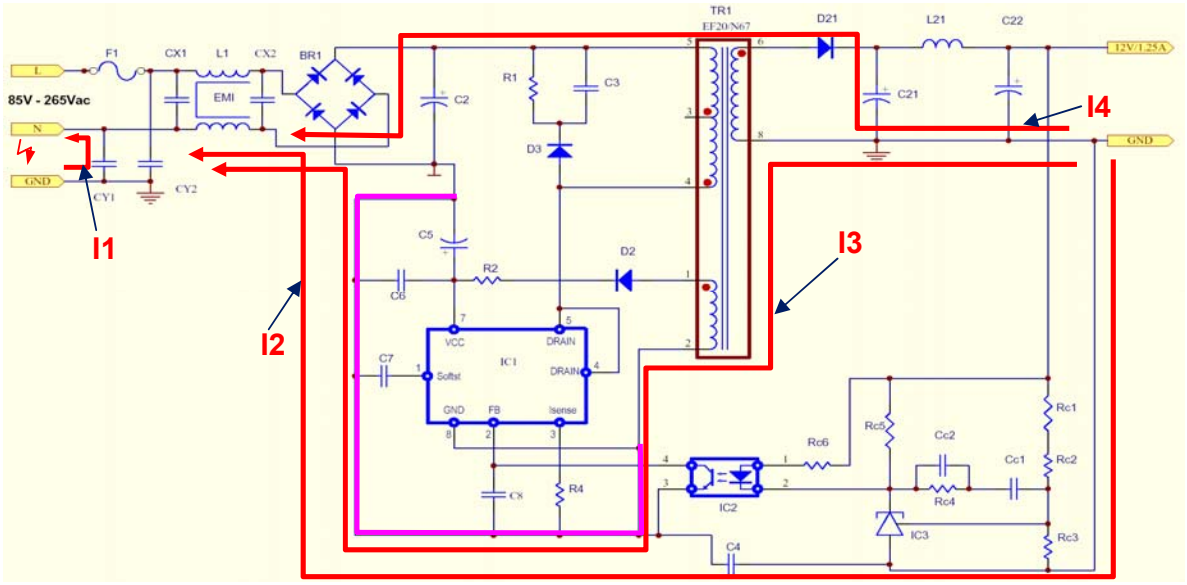

Figure 3 Circuit example of the SMPS under Test

Figure 3 shows a circuit example which is under lightning surge test. The circuit is a flyback converter with CoolSET-F3 PWM controller. The surge signal is across between neutral and earth ground. Possible surge current paths, I_1, I_2 and I_3 are shown in the diagram. I_1 is the current which is passing through safety Y capacitor CY1 between Neutral and Earth. In general I_1 is limited before bridge rectifier and not observed by PWM IC. I2 is the current which is passing through EMI capacitor C4, and I3 is the current which is passing through transformer from secondary GND (earth) to primary GND. I2 and I3 may influence IC GND potential depending on PCB design as shown in Figure 4. I4 is the current which is also passing through transformer but from secondary GND (earth) to primary bulk positive. I4 will influence IC as well if IC has the pins to directly connecting to high voltage bulk positive.

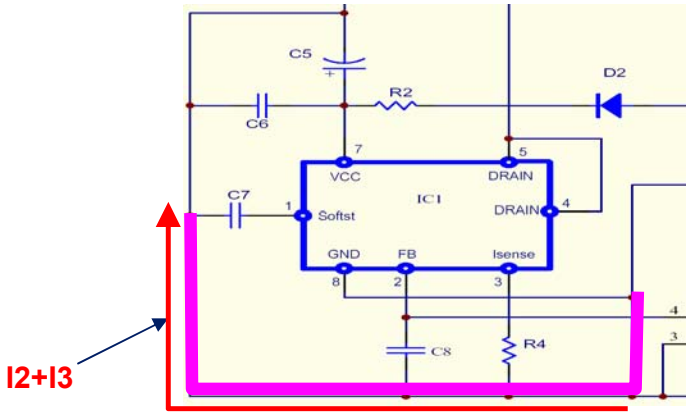

Figure 4 Surge current on the IC GND

Assuming Z is the impedance of PCB track in pink colour, then the voltage across IC pin 1 (Softs) and Pin 8 (GND) is:

$$V_{Softs_GND} = V_{C7} + Z \cdot (I_2 + I_3) \quad (1)$$

Where, V_{C7} is voltage across soft start capacitor C7. it can be considered as constant voltage during lightning surge. From equation (1), it can be seen that IC observes a noisy voltage caused by I2 and I3. The similar effect also occurs on the IC Pin voltage of FB to GND, Vcc to GND and Isense to GND. Depending on how

high the noisy voltage become, IC may enter into fault condition such as protection mode or even be damaged.

5 SMPS Design consideration under lightning surge Test

5.1 PCB primary GND design

From the section 4, it can be seen that IC pins may observe the noisy signal which are highly dependent on PCB design. So the guideline for PCB design is to divert I2 and I3 to other path which is not observed by IC. “Star” connection is highly recommended for the following GND which have to be separated and connected together in bulk capacitor negative pin as shown in Figure 5.

- small signal IC GND,
- high current CS GND,
- input bridge rectifier GND,
- MOSFET Heatsink
- Y capacitor GND (if Y capacitor is connected between transformer primary GND and secondary GND
- Transformer auxiliary winding GND

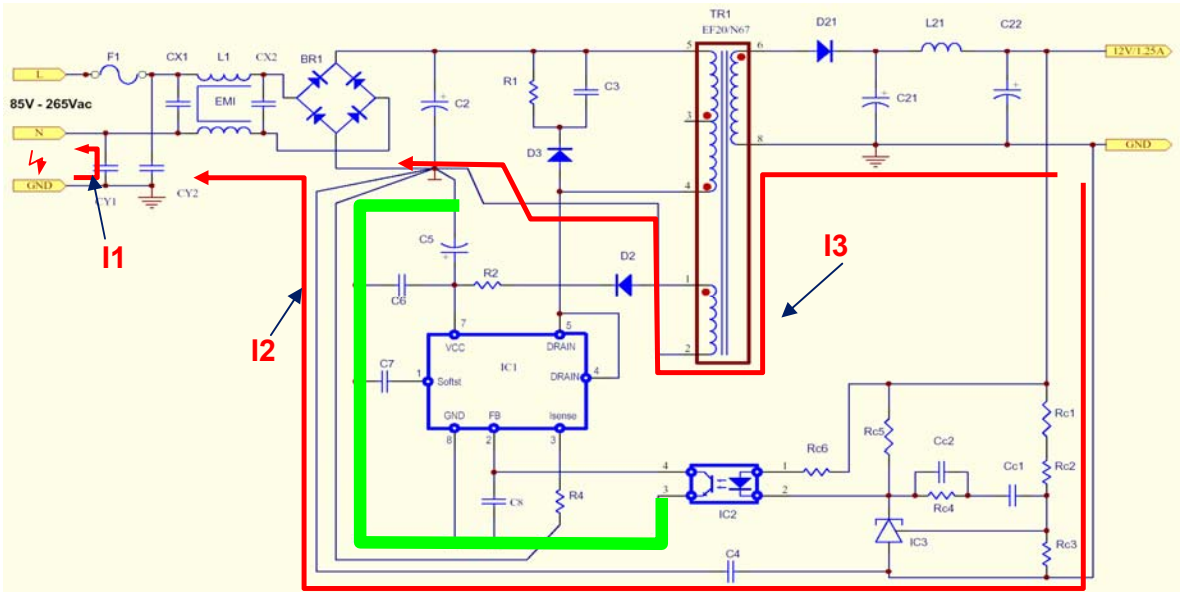

Figure 5 Star connection for primary GND

With the properly star connection as in Figure 5, I2 and I3 will not pass through the PCB track in green colour and IC voltage between pins will not observe noisy signal any more.

Although the above star connection is preferred for lightning surge immunity, some GND tracks **ares** not able to apply this rule due to other concern. One example is transformer auxiliary winding GND in the case of ICEXQS01 Quasi-resonant flyback controller. In this Quasi-resonant controller, auxiliary winding is not only for IC Vcc supply but also to sense minimum MOSFET drain-source voltage for Quasi-resonant operation (and also call zero crossing sensing). In some cases auxiliary winding GND has to connect directly to IC GND pin due to too low signal to noise ratio during normal operation, and then I3 can not be avoided to

influence the IC Pins during lightning. In such circumstance, one way to improve lightning noise immunity is to design the PCB track for auxiliary winding GND as thick as possible, in order to have low impedance Z.

5.2 Y capacitor between primary GND and secondary GND (Earth)

The function of the Y capacitor C4 in Figure 5 is to bypass EMI noise. Instead of primary ground, sometimes C4 can be connected to bulk capacitor positive pin for the same EMI purpose. With doing that, lightning surge current I2 is diverted to bulk positive and will not influence IC GND any more. However, if this is not possible due to other concern and C4 has to be connected to primary GND, the above star connection has to be applied.

5.3 Transformer design

5.3.1 Insulation voltage

I3 current amplitude is dependant on transformer insulation. If transformer insulation is lower than lightning surge voltage, short time breakdown between primary and secondary will occur and very high surge current will be generated. Besides that IC is interferenced by such high surge current, secondary rectifier diode will also experience high voltage stress during short breakdown time and be damaged. So transformer insulation voltage is suggested to be higher than lightning test voltage.

5.3.2 Transformer shielding

Transformer shielding may also help to reduce the parasitic capacitance between primary and secondary. One example is shown in Figure 6 which is from a multiple outputs SMPS design.

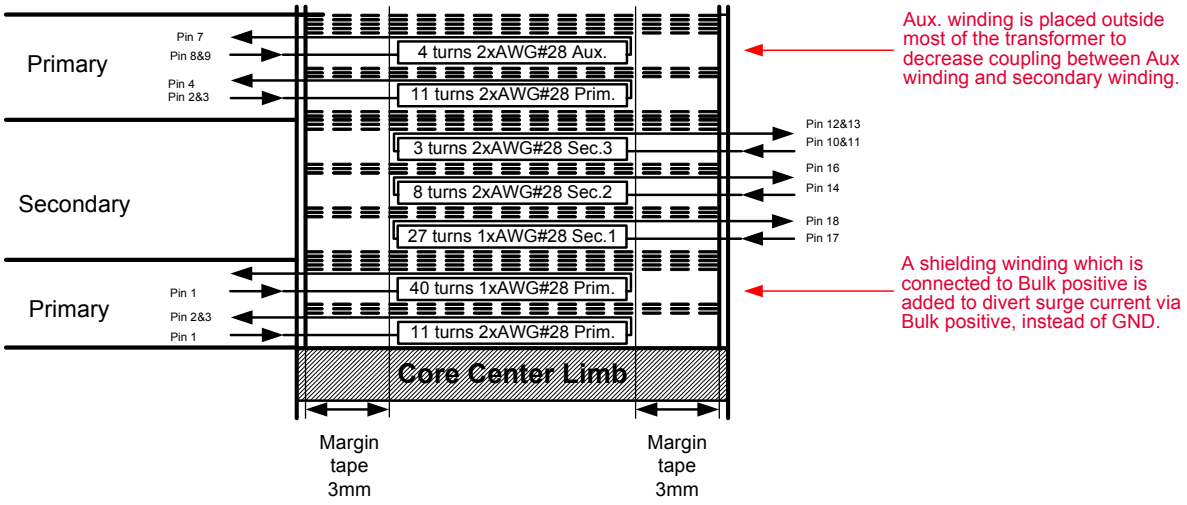

Figure 6 transformer winding design with shielding layer

In Figure 6, the shielding layer is inserted between primary and secondary and connected to bulk capacitor positive. Because shielding layer is much closer to secondary side, the parasitic capacitance between secondary GND to shielding layer is higher compared to secondary GND to Auxiliary winding. So during lightning surge test, the surge current is more likely via shielding layer going into bulk positive instead of primary GND which may influence IC GND.

5.4 Others

5.4.1 Pin filtering capacitor

Most of IC pins has a filtering capacitor to reject the RF noise caused by lightning surge. This capacitor should be also located as close as possible to IC pin for better performance.

5.4.2 High voltage pin for startup cell

Some ICs such as ICE3A(B)S02 which have startup cell integrated. As the shown in Figure 3, the lightning surge current may also go through bulk capacitor positive. If the startup cell pin is directly connected to positive directly, the lightning noise will be radiated as transmitter from the PCB track which is connected startup cell with bulk capacitor positive. So it is necessary to keep this track as thin as possible and enough clearance from other small signal tracks. If it is not possible, a 100kΩ resistor can be connected between bulk capacitor positive and startup cell pin.

6 Summary

To design SMPS with lightning surge immunity, the following items have to be

- Grounding
  - star connections must be applied
  - AUX GND, signal GND use separate tracks to IC GND
  - IC GND, Current sense resistor GND, Bridge Rectifier GND, MOSFET heatsink GND, and Y1 capacitor GND (if Y1 connected to primary GND) use separate tracks and connect together at Bulk Cap negative.
- Y1 Capacitor
  - Y1 cap can be connected to bulk capacitor positive instead of primary GND if possible.
- Transformer structure
  - High insulation voltage
  - Aux winding can be placed at the outmost of the transformer for better performance
  - Shielding winding can also be added for better performance
- Others
  - The filter capacitor should be across IC Pin and IC GND Pin as near as possible.
  - HV pin tracks should be thinner and it **must** be placed far from other signal tracks.

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