Design guidelines for MERUS™ IRS2452BM Class D amplifier IC

About this document

Scope and purpose

This document provides a detailed functional description and design guidelines for the MERUS™ IRS2452BM Class D amplifier control IC.

Intended audience

This document is intended for power electronics engineers, technicians, and developers of Class D audio systems interested in evaluating the functionality and implementation of Infineon's MERUS™ IRS2452BM audio controller.

Key points

- Explains the functional operation and design methodology of a two-channel Class D amplifier control IC for high-voltage audio systems
- Describes PWM modulator options, input configurations, and control loop design for self-oscillating and clock-synchronized operation
- Details protection schemes including overcurrent, overtemperature, undervoltage, and configurable shutdown behaviors
- Provides guidelines for dead-time selection, power supply design, and bootstrap implementation to ensure stable operation
- Outlines PCB layout, grounding, and thermal considerations critical for reliable and low-noise Class D amplifier designs

About this product family

Product family

MERUS™ multilevel Class D audio amplifiers with their unique five-level modulation offer 10x less power dissipation, better approximation of the sound signal, and uncompromised audio performance with the possibility to use only ferrite beads for the output filtering. The integrated DSP option also minimizes the overall system cost.

Target applications

- Constant voltage distribution systems (100 Vrms/70 Vrms)
- Installation systems
- Paging systems
- Pro audio systems
- High power, low impedance systems

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1 General description

The IRS2452BM is a two-channel Class D audio amplifier driver rated at 400 V with integrated pulse-width modulator (PWM) and overcurrent protection. Combined with four external MOSFETs and passive components, the IRS2452BM forms a high voltage two channel analog input Class D amplifier. The versatile structure of the analog input section with an error amplifier and a PWM comparator offer flexibility for implementing different types of PWM modulator schemes.

Loss-less current sensing utilizes the $R_{DS(on)}$ of the MOSFETs. The protection control logic monitors the status of the power supplies and load current through each MOSFET.

With the convenience of a half bridge configuration, the differential input analog PWM modulator and protection logic interface are floated from the main power supply.

The IRS2452BM is equipped with start-up click noise reduction to suppress unwanted audible noise during PWM start-up and shutdown. A 7 mm × 7 mm PQFN package enhances the benefits realized by a small size Class D topology.

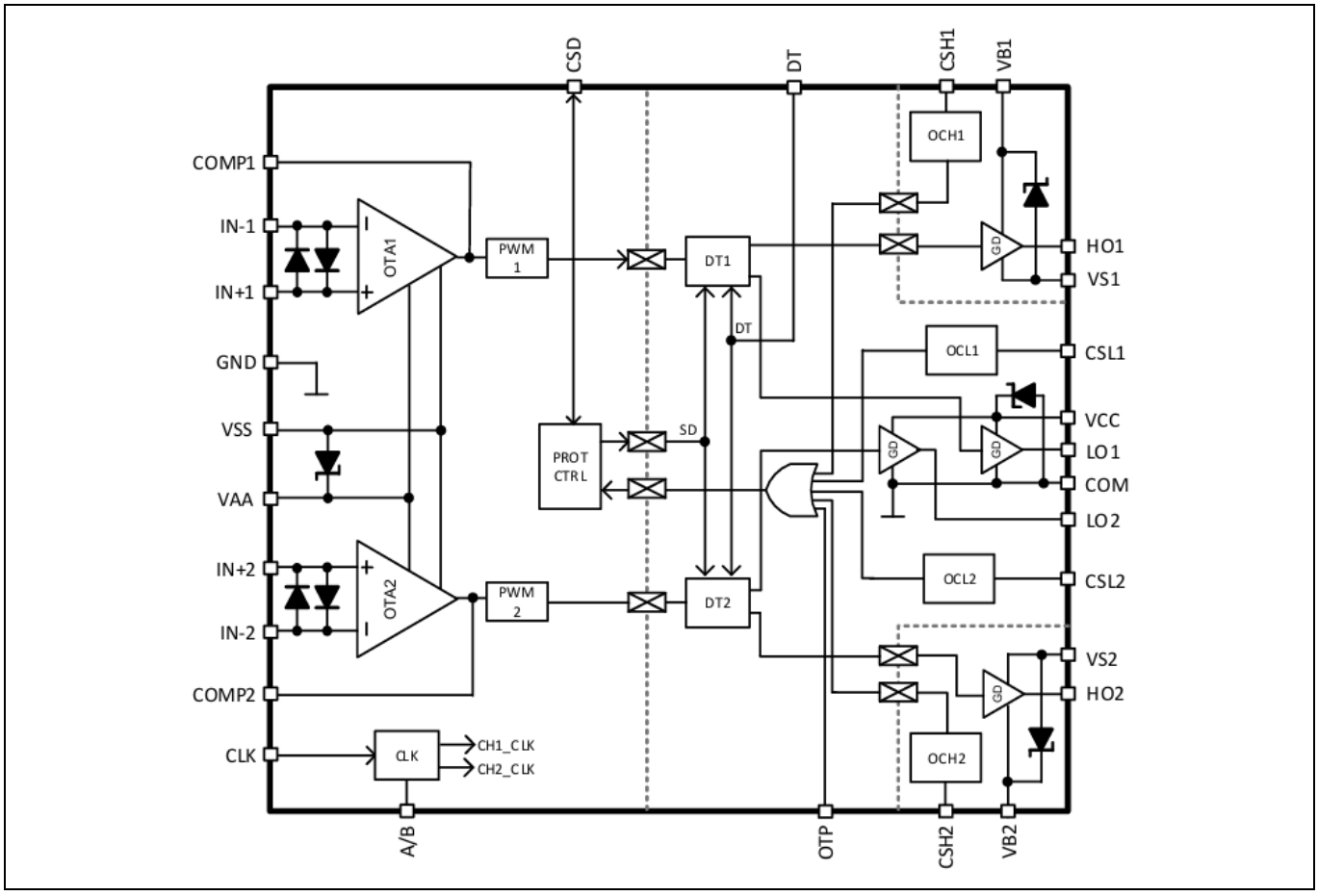


Figure 1 IRS2452BM functional block diagram

2 Typical application topology

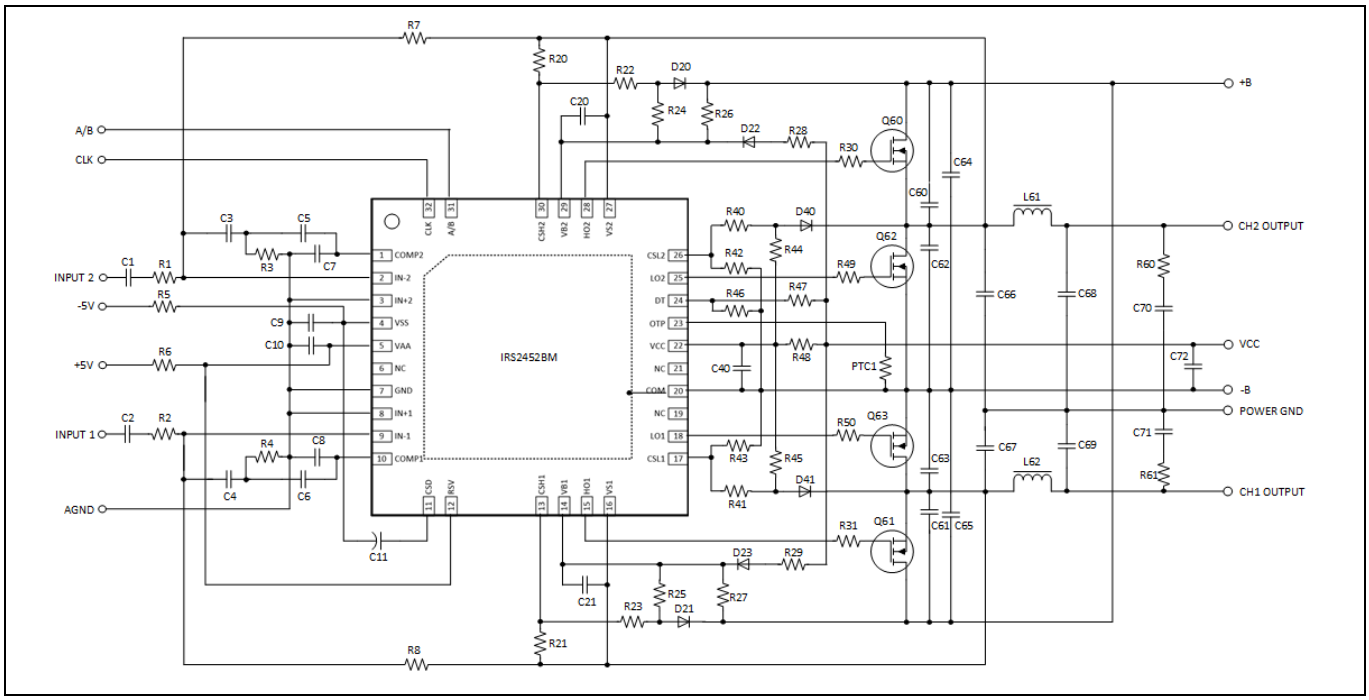


Figure 2 IRS2452BM typical application topology

3 PWM modulator design

The open access front-end structure of the IRS2452BM offers multiple ways to implement a PWM modulator. The following explanations are based on a typical application circuit with self-oscillating PWM topology shown in Figure 2. For further information on the design, see the IRAUDAMP23 reference design [1].

3.1 Input section

3.1.1 Unbalanced input

The audio input stage forms an inverting error amplifier. The voltage gain of the amplifier (G_V) is determined by the ratio between input resistor (R_{IN}) and feedback resistor (R_{FB}).

$$G_V = \frac{R_{FB}}{R_{IN}}$$

Equation 1

As the feedback resistor (R_{FB}) is part of an integrator time constant, which determines the switching frequency, changing the overall voltage gain by R_{IN} is simpler and therefore recommended. Note that the input impedance of the amplifier is equal to the input resistor R_{IN}.

A DC blocking capacitor (C3) should be connected in series with R_{IN} to minimize the DC offset voltage in the output. An electrolytic capacitor is recommended. A ceramic capacitor is not recommended due to potential distortion. Reducing the DC offset is essential to minimize the audible noise during power-ON and -OFF.

The connection of the non-inverting input IN+ is a reference for the error amplifier, which is crucial for audio performance. Connect IN+ to the signal reference ground in the system, which should have the same potential as the negative terminal of the speaker output.

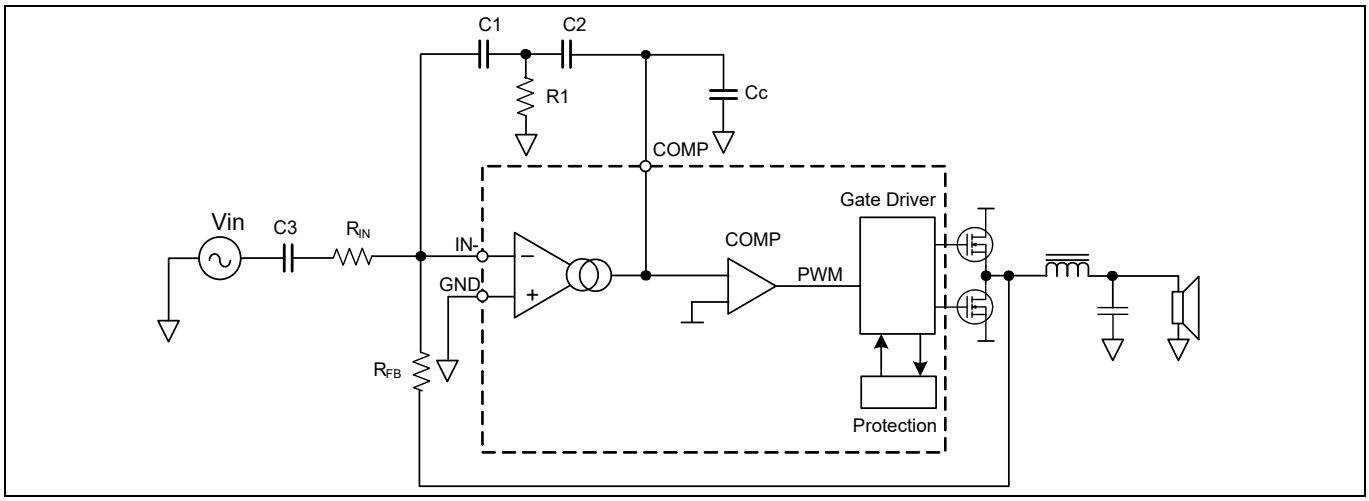


Figure 3 IRS2452BM typical control loop design

3.1.2 Differential input

Figure 4 shows an example of a differential input configuration. This design is useful in a single supply configuration. Use $R_{IN1} = R_{IN2}$, $R_{FB1} = R_{FB2}$, C3 = C4.

Voltage gain is given by a ratio between R_{IN} and R_{FB}.

$$G_V = \frac{R_{FB}}{R_{IN}}$$

Equation 2

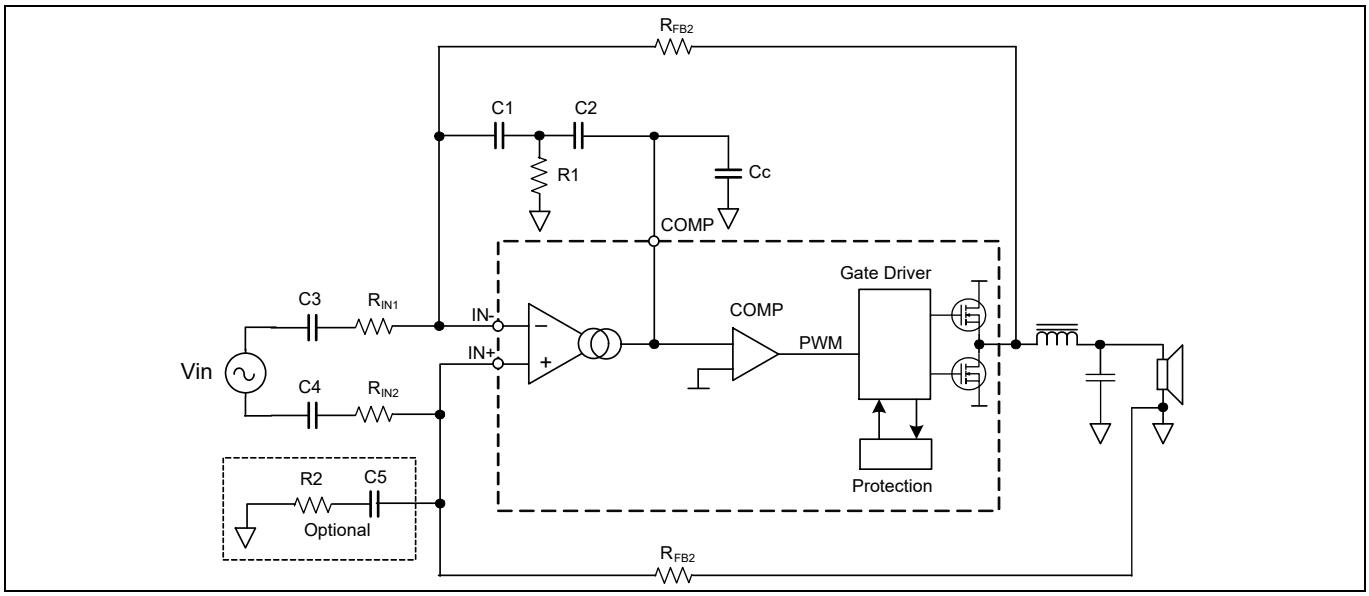


Figure 4 Differential input

Although component values in the feedback network are balanced between inverting and non-inverting inputs, the integration capacitor path in the non-inverting input creates an imbalance at high frequencies, causing slightly higher distortion compared to an unbalanced input configuration. To improve the total harmonic distortion (THD) degradations, place an optional RC network R2 = R1 and C5 = C1.

3.1.3 Operational transconductance amplifier (OTA)

The front-end error amplifier of the IRS2452BM features an operational transconductance amplifier (OTA), which is designed to obtain optimal audio performance. The OTA outputs current to the COMP pin, unlike a voltage output in an operational amplifier (OPA).

The inverting and non-inverting inputs have clamping diodes to improve recovery from clipping as well as ensuring stable start up. The OTA output COMP is internally connected to the PWM comparator with a threshold of (VAA-VSS)/2.

For stable operation of the OTA, a compensation capacitor Cc of minimum 2.2 nF is required. The OTA shuts down when V_{CSD} < Vth2.

3.1.4 Pop-less startup

The IRS2452BM has a unique feature that minimizes the audible click noise at start and stop. When the control shutdown (CSD) pin is between Vth1 and Vth2 during start up, an internal closed loop around the OTA enables an oscillation that generates voltages at COMP and IN-, bringing them to steady state values. It runs at around 1 MHz, independent from the switching oscillation.

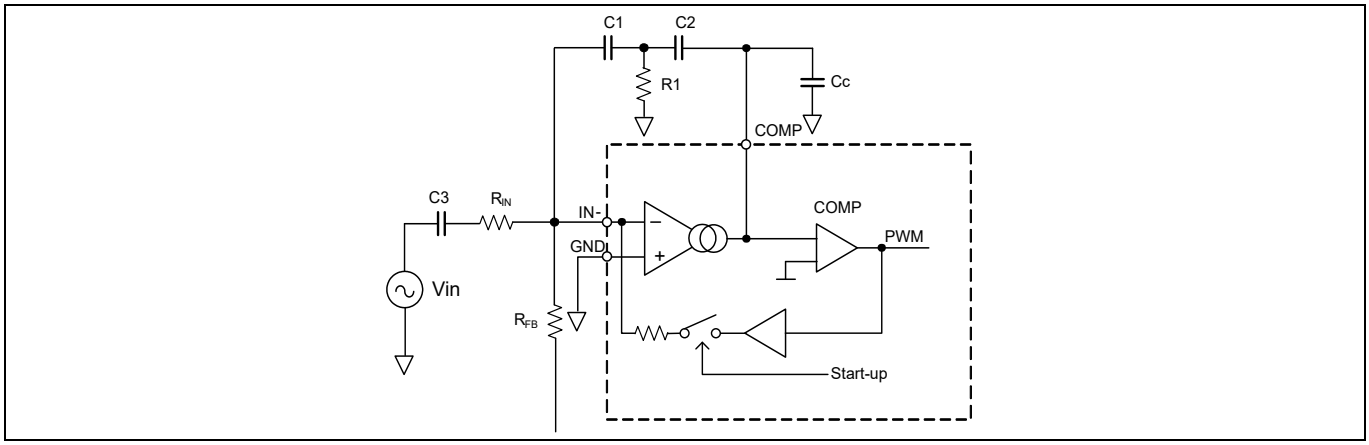


Figure 5 Audible click noise elimination

As a result, all capacitive components connected to COMP and IN- pins, such as C1, C2, C3, and Cc in Figure 5, are pre-charged to their steady state values during the startup sequence. This allows instant settling of PWM operation.

To utilize the click noise reduction function, the following conditions must be met:

- The CSD pin has slow enough ramp up from Vth1 to Vth2 such that the voltages in the capacitors can settle to their target values
- The high-side bootstrap power supply needs to be charged up prior to starting oscillation
- The audio input has to be zero
- For the internal local loop to override external feedback during the startup period, the DC offset at the speaker output prior to shutdown release has to satisfy the following condition:

$$DCoffset < 30\mu A \times R_{FB}$$

Equation 3

For minimum click noise, it is recommended not to start synchronous clock during the pop-less startup period.

3.2 Control loop design

The IRS2452BM allows to choose from numerous ways of PWM modulator implementations. In this section, all the explanations are based on typical application circuits of a self-oscillating PWM.

3.3 PWM frequency

Choosing an idling switching frequency entails making a trade-off between many aspects. At lower switching frequencies, the conduction losses in the MOSFET stage increases due to higher inductor ripple current. The output carrier leakage in the speaker output increases. At higher switching frequency, the efficiency degrades due to higher switching losses. Higher switching frequency supports wider audio bandwidth. The reduced inductor ripple current slows down the zero-voltage switching (ZVS) operation. Therefore, increasing the minimum dead-time required for efficient idling operation. For these reasons, 325 kHz is chosen as a typical design example in the IRAUDAMP23 [1] evaluation board.

Self-oscillating frequency is determined mainly by the following (Figure 4).

- Integration capacitors (C1 and C2)
- Integration resistor (R1)
- Propagation delay in the gate driver
- Feedback resistor (R_{FB})
- Duty cycle

Note that the nature of a self-oscillating PWM is for the switching frequency to decrease as the PWM modulation deviates from idling.

Table 1 summarizes suggested values of components for a given target self-oscillating frequency. The front-end operational transconductance amplifier (OTA) output has limited voltage and current compliances. This set of component values ensures that OTA operates within its linear region for optimal THD+N performance. In case, the target frequency is somewhere in between the frequencies listed in Table 1, then adjust the frequency by tuning R1.

Table 1 External component values vs. self-oscillation frequency

Target self-oscillation frequency (kHz)	C1 = C2 (nF)	CC (nF)	R1 (Ω)
400	3.3	2.2	131
350	3.3	2.2	97
300	3.3	2.2	78
250	3.3	2.2	69
200	3.3	2.2	64

3.4 Clock synchronization

In the PWM control loop design example, the self-oscillating frequency can be set and synchronized to an external clock. Through the internal RC network, the clock signal from clock (CLK) pin injects periodic pulsating charges into the integrator, forcing oscillation to lock up to the clock frequency. To maximize audio performance, the self-running frequency should be 10% higher than the clock frequency.

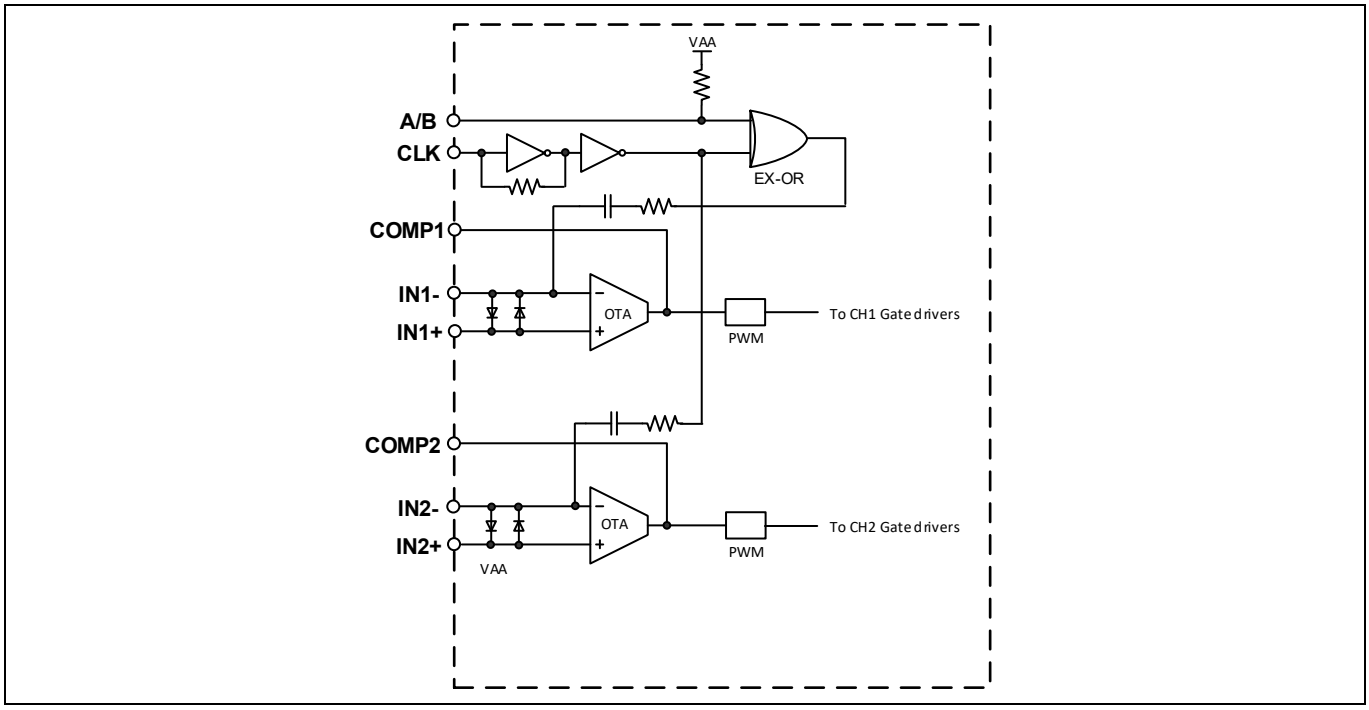


Figure 6 Clock synchronization

The CLK pin receives a clock signal referenced to GND. The input threshold is set for 3.3 V logic. The external clock should be 50% duty cycle. The A/B pin changes the clock phase for CH1. The threshold is in between VAA and GND. When A/B pin is pulled to VAA, CH1 and CH2 clocking is in-phase. When A/B pin is pulled to GND or VSS, CH1 and CH2 are out-of-phase.

Figure 7 shows the clock synchronization lock range of the IRS2452BM as a function of output duty cycle, at the supply voltage of ±148.3 V. The self-oscillating frequency follows a naturally parabolic shape, peaking near the natural self-oscillating frequency at 50% duty cycle, and tapering toward the duty cycle extremes. This is an inherent characteristic of the self-oscillating PWM topology. The upper and lower locking frequency boundaries define the range of external clock frequencies to which the IC can successfully synchronize. An external clock signal must fall between these two boundary curves at the operating duty cycle to achieve lock. The design example is based on a 325 kHz self-oscillating frequency. At 50% duty cycle, the lock range spans roughly 290 kHz to 380 kHz, providing approximately ±10% to 15% capture range around the natural oscillating frequency.

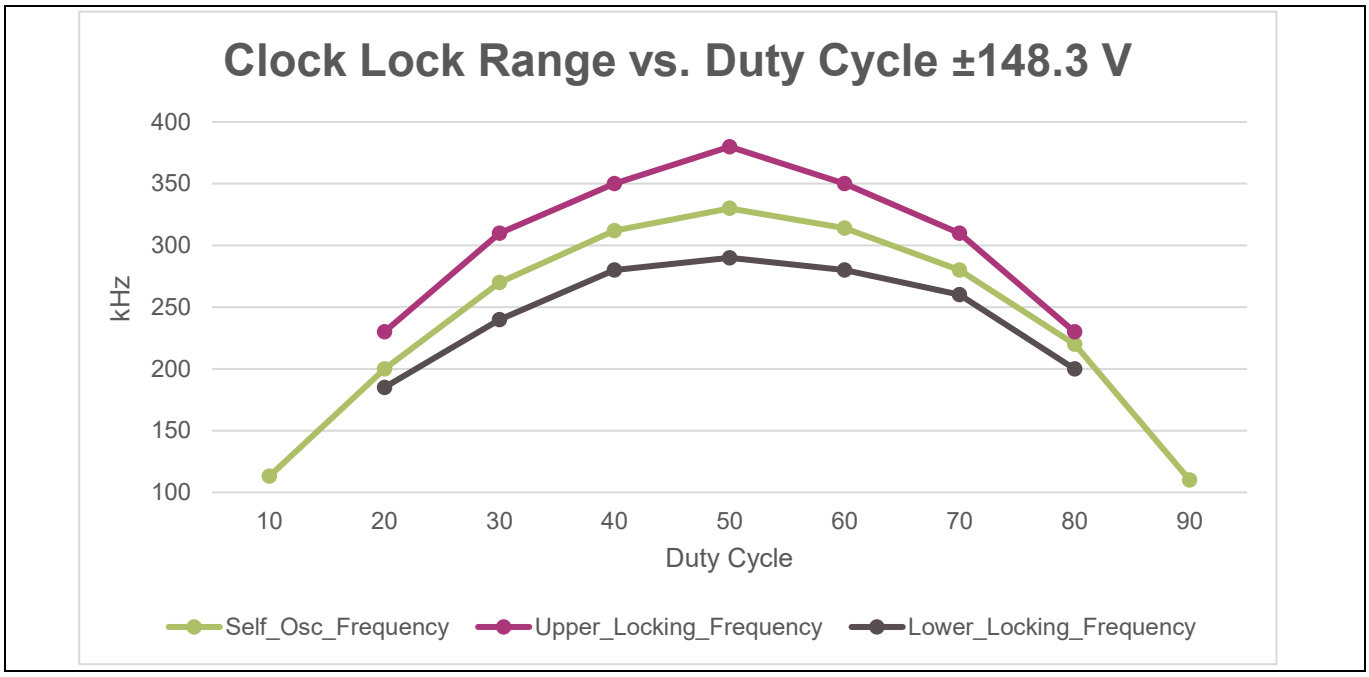


Figure 7 Typical lock range to external clock

3.5 Output low pass filter (LPF)

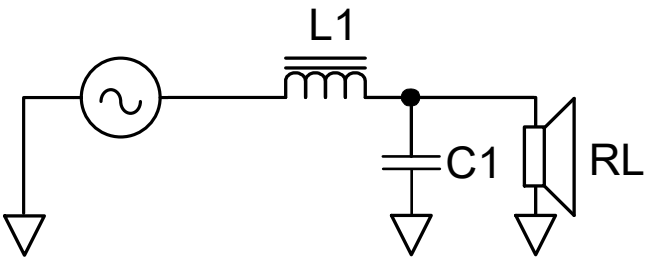
The output low pass filter (LPF) demodulates the amplified audio signal, which is necessary for efficient operation of a Class D amplifier. Therefore, selecting the right components is critical for both audio and system efficiency.

A typical output LPF uses a second order Butterworth LC filter designed to achieve maximum flat frequency response up to a corner frequency with nominal load impedance. Figure 8 shows how to calculate the component values for a load impedance. The corner frequency should be set according to the bandwidth requirement. A corner frequency of 40 kHz would be a good tradeoff point between 20 kHz bandwidth, inductor ripple current, and inductance. Note that the higher the corner frequency, the higher the switching carrier leakage, and the lower the corner frequency, the bigger the inductor size.

The inductance of the inductor changes with load current bias, which causes distortion in audio output. Core saturation increases the inductor ripple significantly, which could trigger the overcurrent protection immediately. Use an inductor with a saturation point that is higher than the peak load current. Consider the I_{RMS} rating of an inductor for temperature rise condition with 1/8 rated power and peak current for maximum load current.

Use a capacitor that meets the AC voltage ratings at the highest audio frequency output. Use a film capacitor with lower series inductance structure type. Ceramic capacitors could add audio distortion from the strong bias voltage dependency in capacitance; this is especially demonstrated in high dielectric coefficient ceramic capacitors such as Y5V.

3 PWM modulator design



$$L_n = \frac{1.414 \times R_L}{2 \times \pi \times f_C}$$

$$C_n = \frac{0.707}{2 \times \pi \times f_C \times R_L}$$

Figure 8 Output LPF design

4 Operational mode

The CSD pin determines the operational mode of the IRS2452BM as shown in Figure 9. The OTA has three operational modes: cut off, local oscillation, and normal operation; while the gate driver section has two modes: shutdown and normal operation.

When V_{CSD} < Vth2, the IC is in shutdown mode and the OTA is cut off. When Vth2 < V_{CSD} < Vth1, the high-side output (HO) and low-side output (LO) are still in shutdown mode. The OTA is activated and starts local oscillation for pop-less start-up, which pre-biases all the capacitive components in the error amplifier. When V_{CSD} > Vth1, the shutdown is released and PWM operation starts.

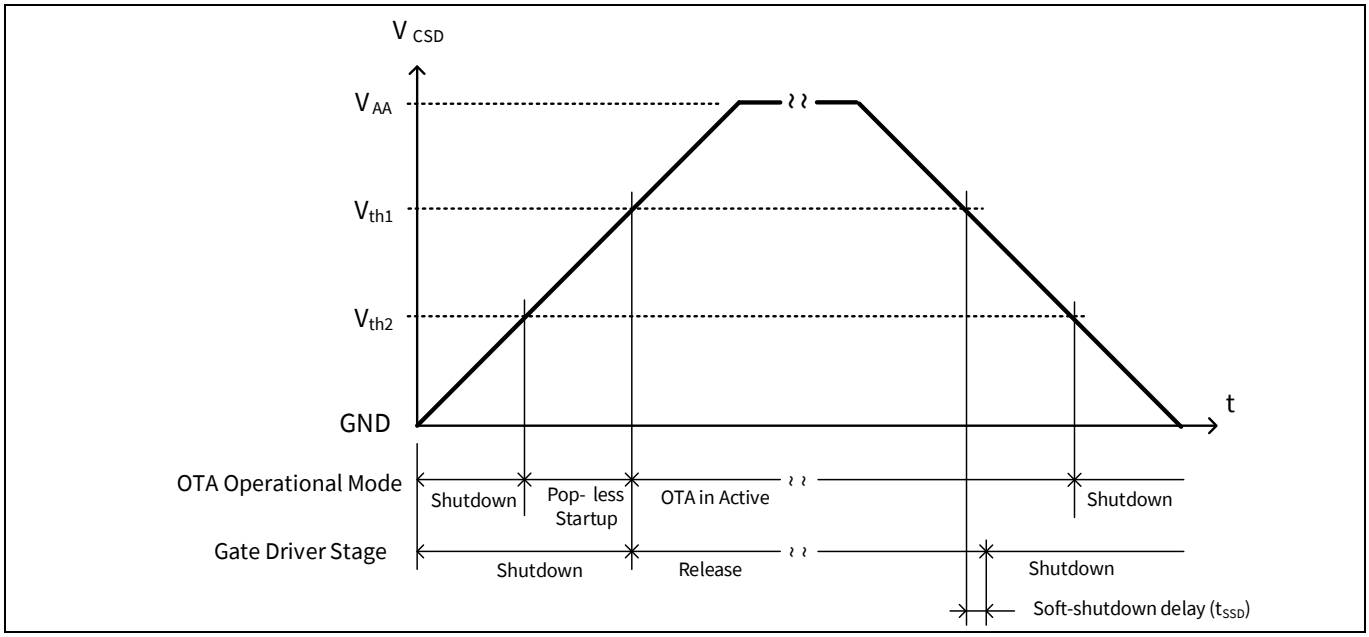


Figure 9 V_{CSD} and operational mode

4.1 Self-oscillation start-up condition

Ensure that the IRS2452BM meets the following conditions for pop-less startup to work properly.

- All the control power supplies (VAA, VSS, VCC, and VBS) are above the undervoltage lockout thresholds
- The CSD pin voltage should be over the Vth1 threshold

$$|i_{IN}| < |i_{FB}|$$

Equation 4

Where,

$$i_{IN} = \frac{V_{IN}}{R_{IN}}, i_{FB} = \frac{V_{+B}}{R_{FB}}$$

Equation 5

- The duration of the CSD voltage transitioning from Vth2 to Vth1 is long enough to pre-charge the input and integration capacitors around OTA section

5 Dead-time setting

5.1 Determining required dead-time.

Dead-time is the blanking period inserted between high-side and low-side ON duration. Dead-time serves two purposes: to prevent shoot-through at any time and to ensure zero-voltage switching (ZVS) at idling.

The internal dead-time generation block allows to select the optimum dead-time from a range of preset values. An external voltage divider selects a preset dead-time through the dead-time (DT) pin voltage. The selectable dead-time setting prevents incoming noise modulating the switching timing, which is critical to the audio performance.

An effective dead-time in MOSFET gate bias voltage differs from the dead-time specified in the device datasheet. The dead-time value in the datasheet is defined as the time period between the beginning of transition on one side of the output to the other side as shown in Figure 10. The fall time of the MOSFET gate voltage must be subtracted from the dead-time value in the datasheet to determine the effective dead-time of a Class D audio amplifier.

Effective dead-time = Dead-time in datasheet – tf (MOSFET fall time)

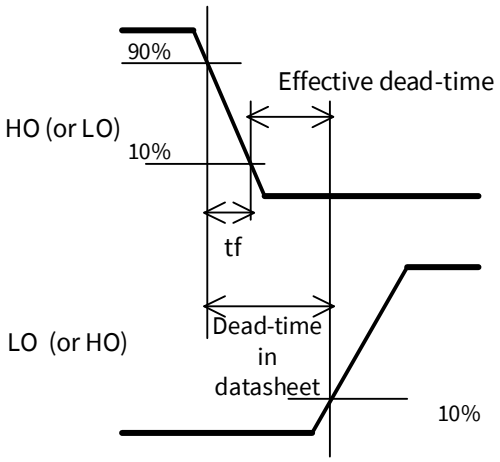


Figure 10 Effective dead-time

A longer dead-time period is required for a MOSFET with a larger gate charge value because of the longer tf. Negative values of effective dead-time cause excessive heat dissipation in the MOSFETs, leading to potential damage so it should always be avoided. Therefore, effective dead-time determines the minimum dead-time a design can take.

In practical design, efficient operation at idling is important to minimize idling power loss. Setting a dead-time for zero-voltage switching (ZVS) operation ensures minimum idling power consumption. A time duration required to complete the voltage transition (t_{ZVS}) is a function of output inductor current, total MOSFET output capacitance in VS node, C_o, and output inductance in the LC LPF.

$$t_{ZVS} = 8 \times C_O \times f_{SW} \times L$$

Equation 6

5 Dead-time setting

Where,

C_o = Total capacitance in VS node = 2 × Coss, use time constant equivalent Coss

f_{sw} = PWM frequency

L = Output inductor inductance

Select a dead-time window such that the minimum effective dead-time is longer than t_{ZVS}.

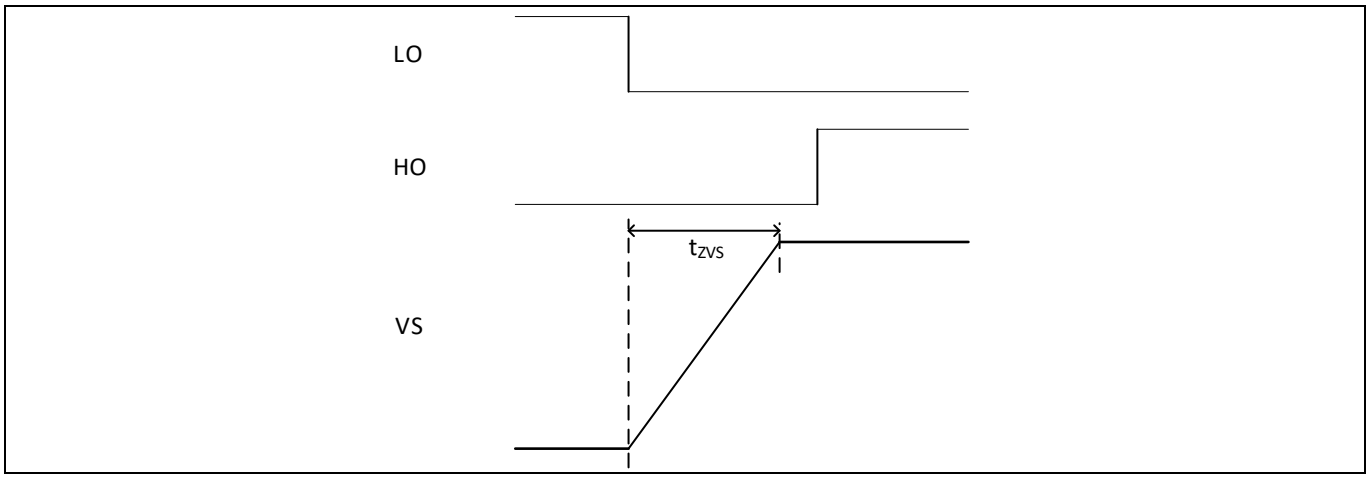


Figure 11 ZVS during dead-time

5.2 Programming dead-time

The IRS2452BM selects the dead-time from a range of preset dead-time values based on the voltage applied at the DT pin. An internal comparator translates the DT input to a predetermined dead-time by comparing the input with internal reference voltages. These internal reference voltages are set in the IC through a resistive voltage divider using V_{CC}. The relationship between the operation mode and the voltage at DT pin is illustrated in Figure 12.

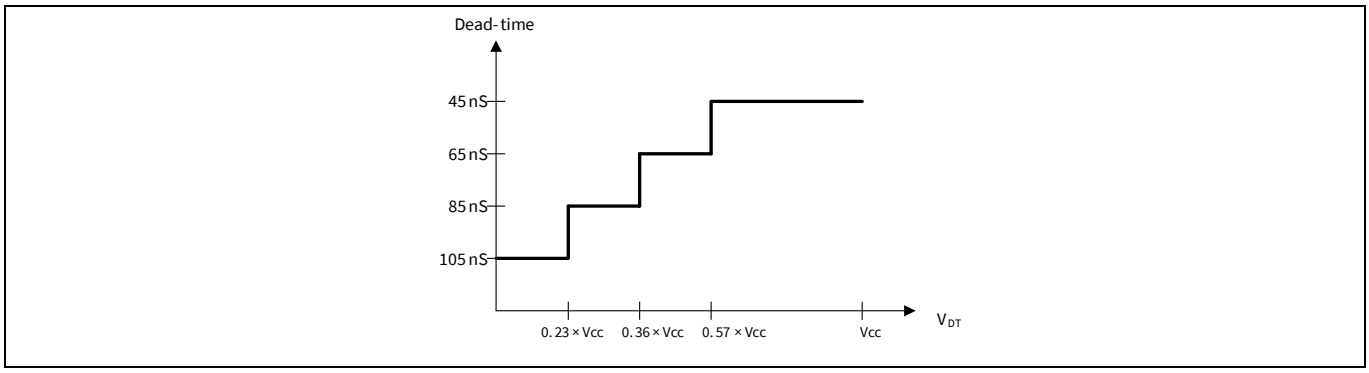


Figure 12 Dead-time vs. VDT

Table 2 recommends pairs of resistor values used in the voltage divider for selecting dead-time. Resistors with up to 5% tolerance are acceptable when using these values.

5 Dead-time setting

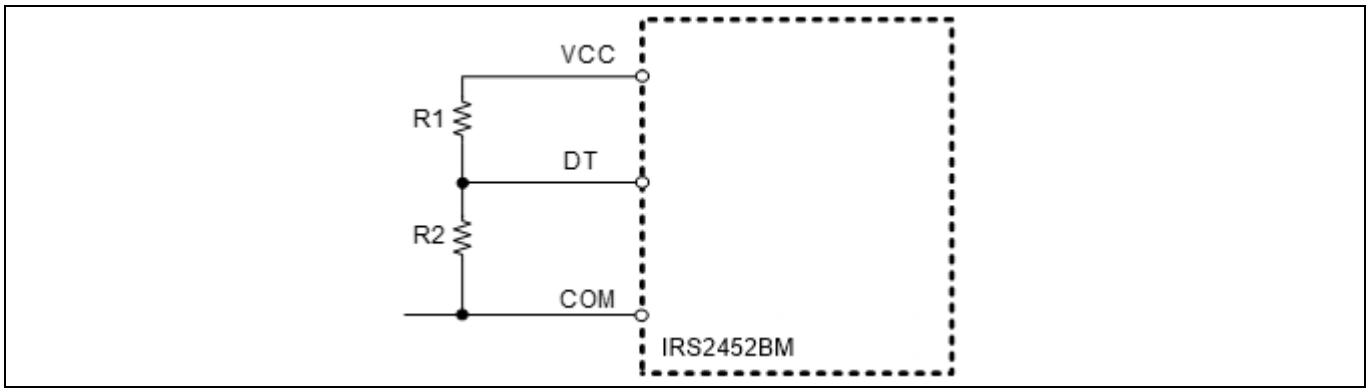


Figure 13 External voltage divider for DT pin

Table 2 Recommended resistor values for dead-time selection

Dead-time mode	R1	R2	DT voltage
DT1	<10k	Open	Vcc
DT2	5.6 kΩ	4.7 kΩ	0.46 × Vcc
DT3	8.2 kΩ	3.3 kΩ	0.29 × Vcc
DT4	Open	<10 k	COM

6 Adding gate drive buffer

The built-in gate driver with 0.5 A to 0.6 A output can drive a MOSFET with Qg < 20 nC. To drive a MOSFET with a larger Qg, it is recommended to use a gate drive buffer to boost the output current. Due to the overcurrent sensing monitoring the V_{DS} when the MOSFET is on, the propagation delay in the gate buffer needs to be less than 50 ns to prevent false triggering.

Figure 14 shows how to add a buffer using bipolar junction transistors (BJTs).

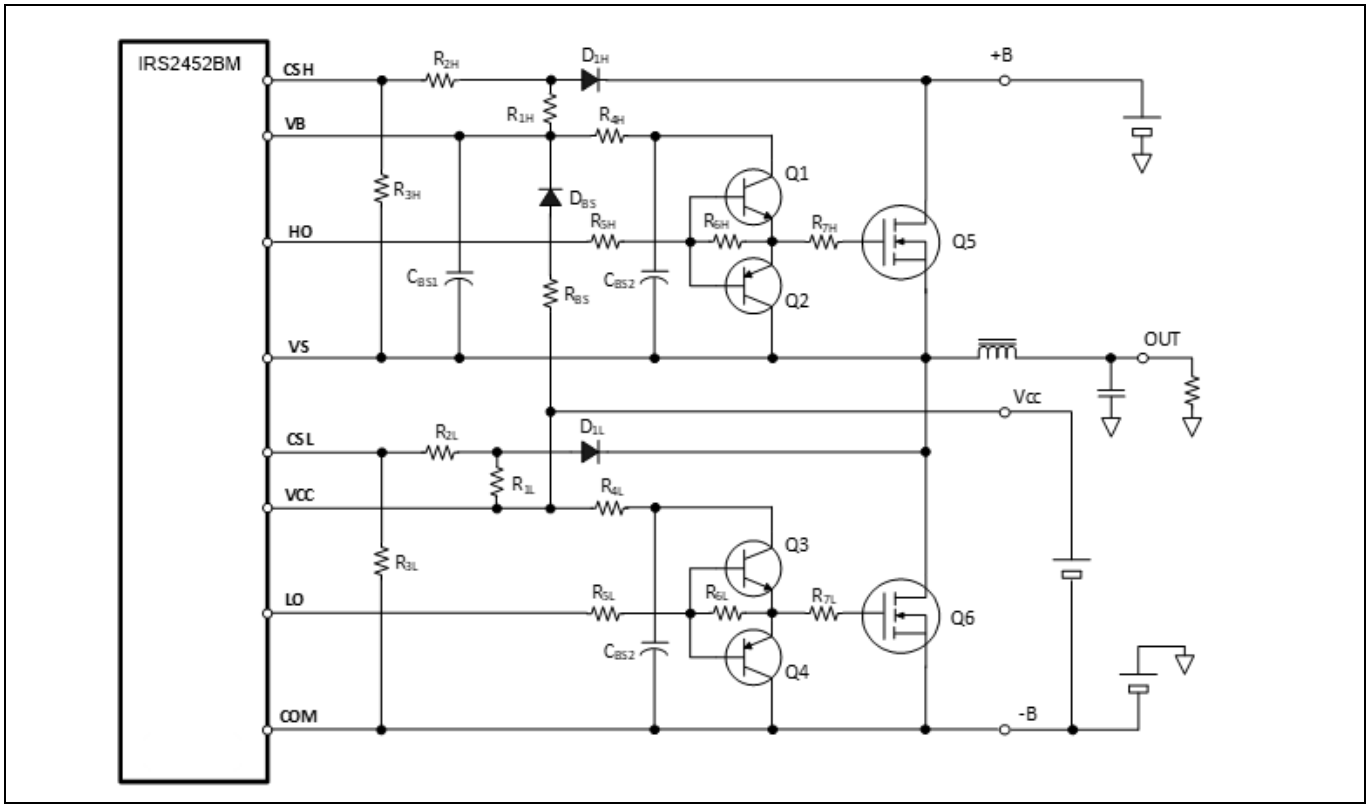


Figure 14 IRS2452BM with gate drive buffer

7 Protections

7.1 Protection control

The internal protection control block dictates the operational mode, normal, or shutdown, using the input of the CSD pin. In shutdown mode, the IC forces LO and HO to output 0 V with respect to COM and VS respectively to turn off the power MOSFETs.

The CSD pin provides the following functions:

- Power up delay timer
- Self-reset timer
- Shutdown input
- Latched protection configuration
- Shutdown status output (host I/F)

Note: The CSD pin of one IRS2452BM IC cannot be tied with another IRS2452BM directly.

Table 3 shows the operating status of the protection features.

CSD recycle: CSD pin voltage discharges down to Vth2 and charges back to VAA, if the CSD pin is configured as self-reset protection.

Table 3 Events and actions of CSD and FAULT

Event	CSD	FAULT
UVCC, rising edge	Recycle	L until CSD > Vth1
UVCC, falling edge	NA	NA
UVAA, rising edge	NA	L at VAA<UVAA
UVAA, falling edge	NA	L at VAA<UVAA
UVBS, rising edge	NA	NA
UVBS, falling edge	NA	NA
Overcurrent protection	Keep recycling until OCP is reset	Held L until OCP is reset
OTP input	Keep recycling until OTP is reset	Held L until OTP is reset

7 Protections

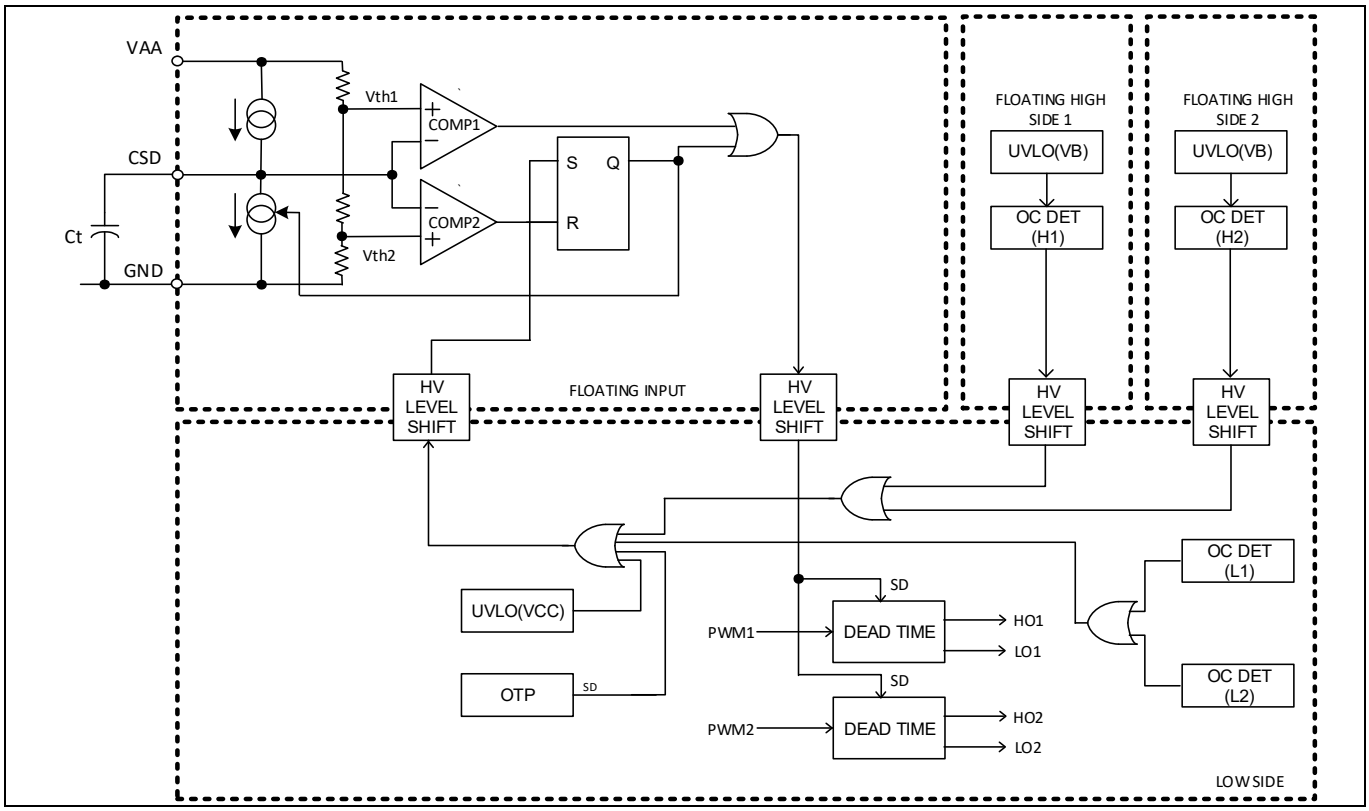


Figure 15 Protection functional block diagram

7.1.1 Self-reset protection

Attaching a capacitor between CSD and VSS configures the IRS2452BM self-rest protection mode. Upon an OCP event, the CSD pin discharges the external capacitor voltage (V_{CSD}), down to the lower threshold (Vth2) to reset the internal shutdown latch. Then, the CSD pin begins to charge the external capacitor (Ct) in an attempt to resume operation. Once the voltage of the CSD pin rises above the upper threshold (Vth1), the IC resumes normal operation.

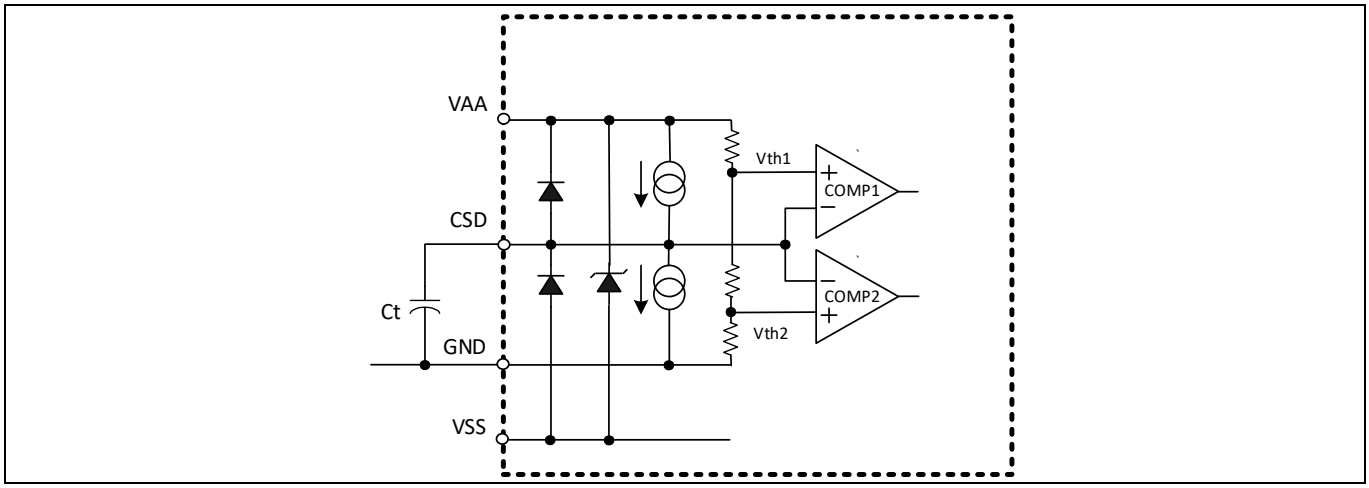


Figure 16 Self-reset protection configuration

7.1.2 Designing Ct

The external timing capacitor (Ct) programs self-reset timings, t_{RESET} and t_{SU}.

- The t_{RESET} is the time that elapses from when the IC enters the shutdown mode to the time when the IC resumes operation. The t_{RESET} should be long enough to avoid over heating the MOSFETs from the repetitive sequence of shutting down and resuming operation during overcurrent conditions. In most applications, the minimum recommended time for t_{RESET} is 0.1 seconds
- The t_{SU} is the time between powering up the IC in shutdown mode to the moment the IC releases shutdown to begin normal operation

The Ct determines t_{RESET} and t_{SU} as shown in the following equations:

$$t_{RESET} = \frac{Ct \times V_{AA}}{1.1 \times I_{CSD}} \text{[seconds]}$$

Equation 7

$$t_{SU} = \frac{Ct \times V_{AA}}{0.7 \times I_{CSD}} \text{[seconds]}$$

Equation 8

Where,

I_{CSD} = Charge/discharge current at the CSD pin

V_{AA} = the input supply voltage with respect to GND

7.1.3 Shutdown input

During normal operation, pulling the CSD pin below the upper threshold (Vth1) forces the IC into shutdown mode. Figure 17 shows how to add an external discharging path to shutdown the PWM.

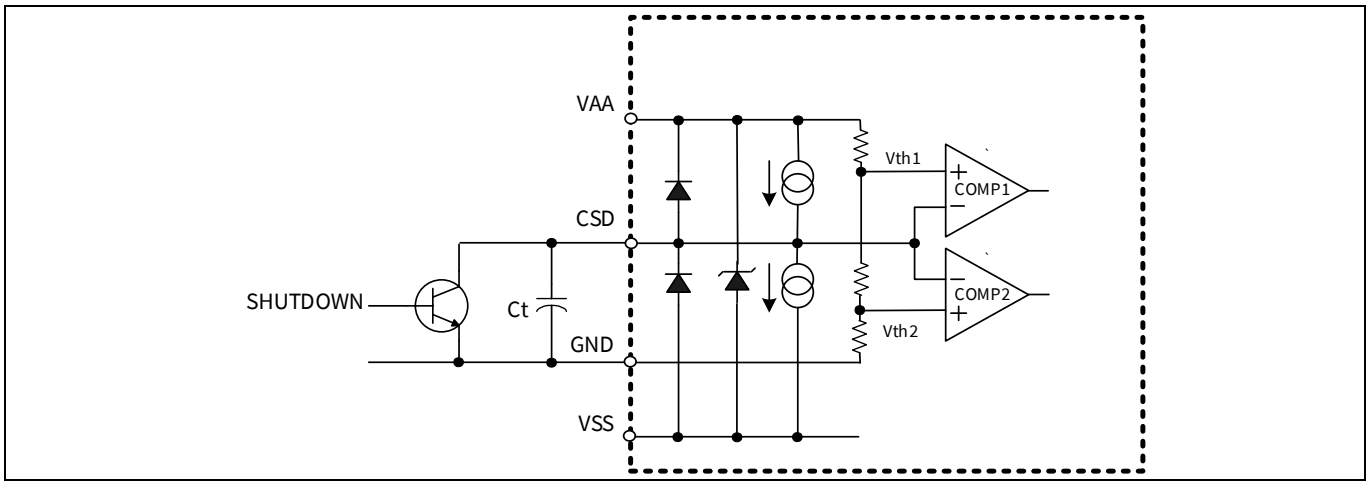


Figure 17 Shutdown input

7.1.4 Latched protection

Connecting CSD to VAA through a 10 kΩ or less configures the latched protection mode. The internal shutdown latch stays in shutdown mode after overcurrent is detected. An external reset switch brings CSD below the lower threshold (Vth2) for a minimum of 200 ns and resets the latch. At first power up, a reset signal to the CSD pin is required to release the IC from shutdown mode.

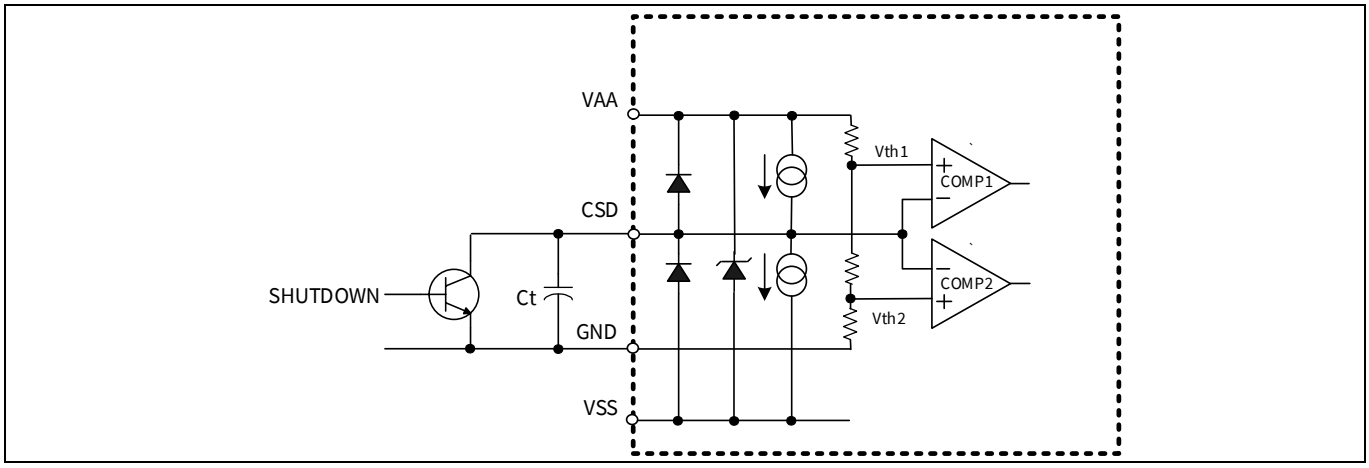


Figure 18 Latched protection with reset input

7.1.5 Interfacing with system controller

The IRS2452BM can communicate with an external system controller through a simple interfacing circuit as shown in Figure 19. A generic PNP transistor (U1) detects the sink current at the CSD pin during protection event and outputs a shutdown flag signal to an external system controller. Another generic NPN transistor (U2) can then reset the internal protection logic by pulling the CSD voltage below the lower threshold (Vth2). After the first power-up sequence, a reset signal to the CSD pin is required to release the IC from shutdown mode.

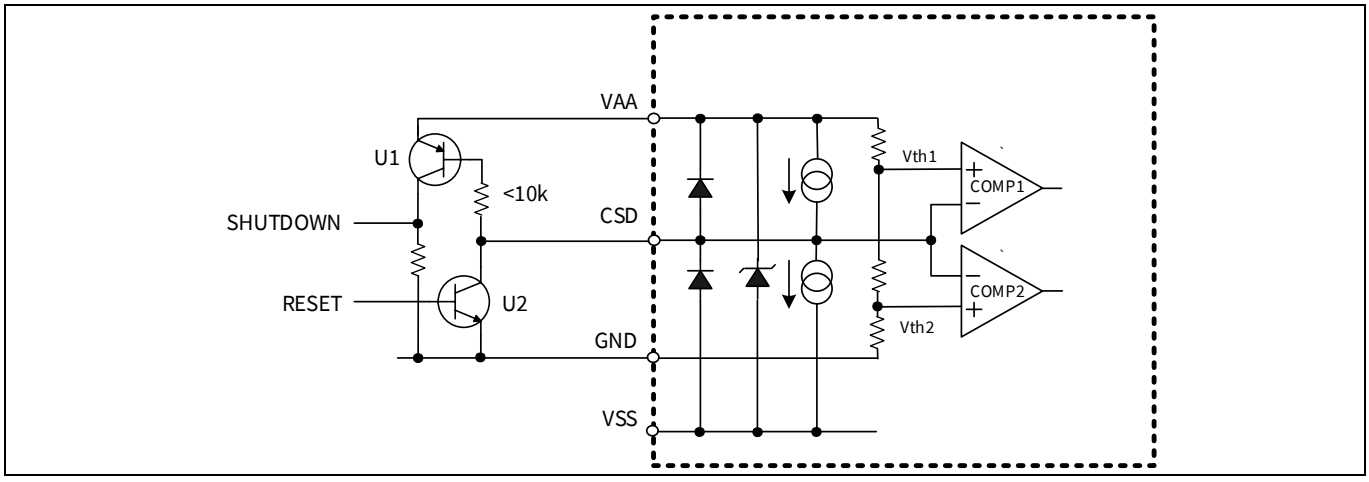


Figure 19 Interfacing CSD with system controller

7.2 Overcurrent protection (OCP)

The IRS2452BM features overcurrent protection to protect the external power MOSFETs during abnormal load conditions. Figure 20 shows the overcurrent protection timing chart. As soon as either the high-side or low-side current sensing block detects overcurrent, the following sequence will occur:

1. Shutdown latch flips its logic state from normal operational mode to shutdown mode
2. Low-side and high-side MOSFETs go into an off state condition
3. CSD pin starts discharging the external capacitor (Ct)
4. When the voltage across Ct falls below the lower threshold (Vth2), the internal shutdown latch resets to normal mode
5. CSD pin starts charging the external capacitor (Ct)
6. V_{CSD} goes above the upper threshold (Vth1), the logic on COMP1 toggles and the IC resumes operation

Figure 20 summarizes the above sequence. As long as the overcurrent condition exists, the IC will repeat the overcurrent protection sequence at a repetitive rate set by the CSD capacitor.

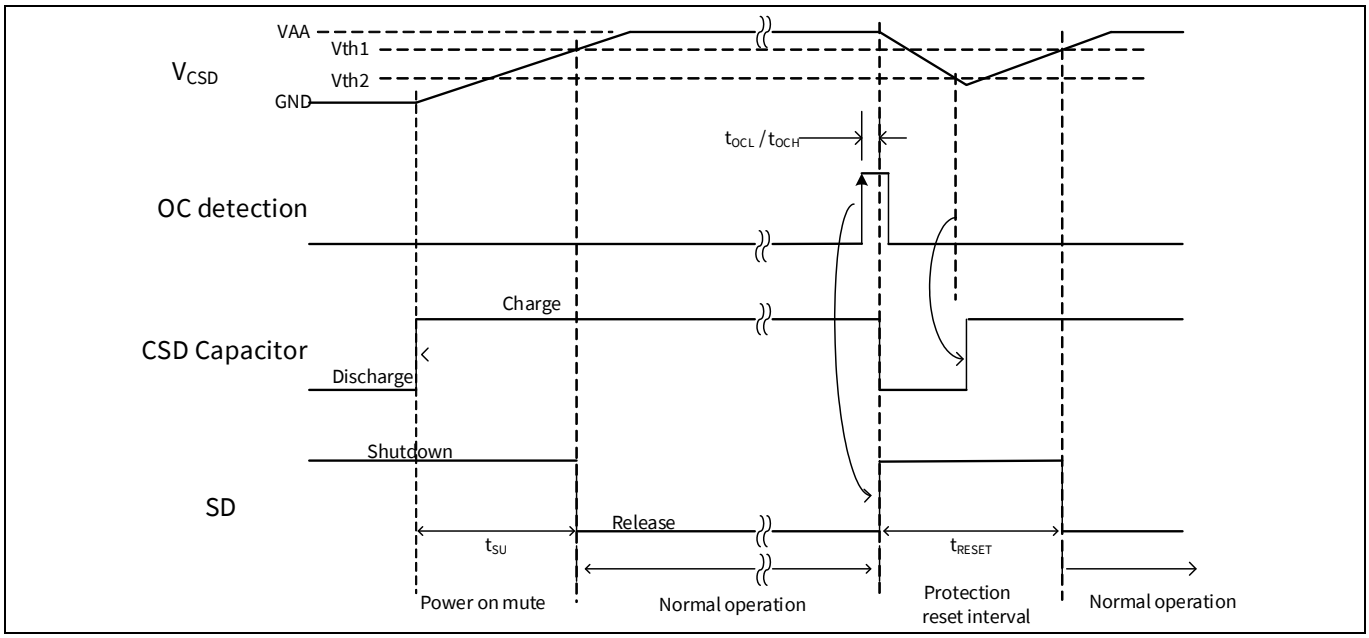


Figure 20 Overcurrent protection timing chart

7.2.1 Programming OCP trip level

In a Class D audio amplifier, the direction of the load current alternates with the audio input signal. An overcurrent condition can therefore occur during either a positive current cycle or a negative current cycle. The IRS2452BM uses the $R_{DS(on)}$ of the output MOSFETs as current sensing resistors. If the measured current exceeds a predetermined threshold, the OCP block outputs a signal to the protection block, forcing HO and LO low and protecting the MOSFETs. The IRS2452BM provides an identical overcurrent sensing signal to both high-side and low-side MOSFETs.

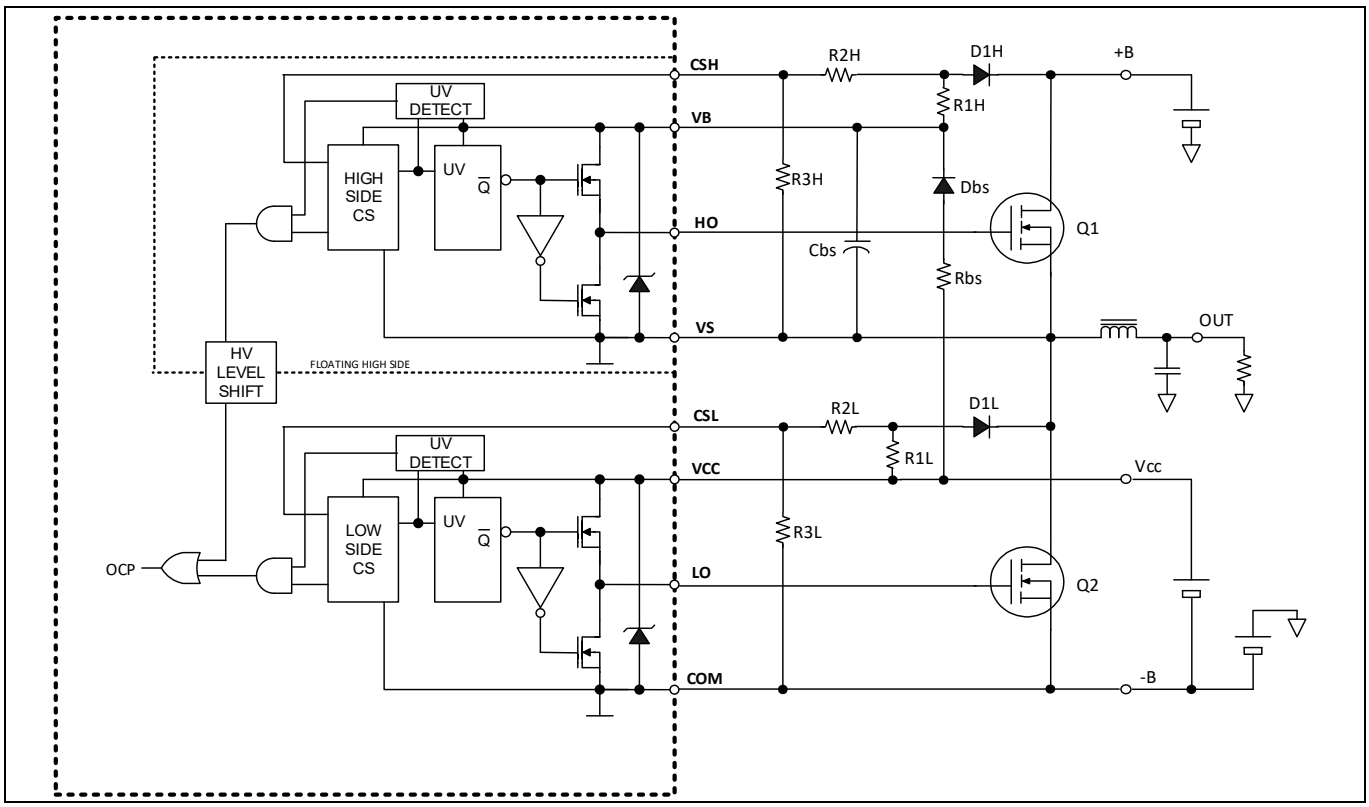


Figure 21 Bidirectional overcurrent protection

7.2.2 Overcurrent sensing

Overcurrent sensing block monitors the load condition and shuts down switching operation if the load current exceeds the preset trip level. Current sensing uses the drain to source voltage (V_{DS}) across the MOSFET during the turn on period via CSH and CSL pins. To avoid false triggering the OCP due to switching rings, a blanking interval is inserted right after HO or LO turn-on for 500 ns max.

An external diode (D1) blocks the high voltage from the drain of the MOSFET from feeding into the CSL/CSH pin while the MOSFET is off. A 10 kΩ resistor (R1), forward biases D1.

The detection thresholds of the OCP, Vth_{OCL}, and Vth_{OCH} are internally fixed at typical 1.2 V. An external resistive divider, R2 and R3, set the threshold. Due to a forward voltage drop of $V_{F(D1)}$ across the D1, the minimum threshold required for high-side overcurrent protection therefore is Vth_{OCL} or Vth_{OCH} minus $V_{F(D1)}$, which is typically 0.6 V.

$$V_{CSH} = \frac{R3}{R2+R3} \times \left(V_{DS} + V_{F(D1)}\right)$$

Equation 9 Sensing voltage for high side CSH pin

Where,

V_{DS} = Drain to source voltage of the high-side MOSFET during on state

$V_{F(D1)}$ = Forward drop voltage of D1

As the V_{DS} is the product of drain current I_D and $R_{DS(on)}$ of the high side MOSFET. V_{CSH} can be rewritten as:

$$V_{CSH} = \frac{R3}{R2+R3} \times \left(R_{DS(on)} \times I_D + V_{F(D1)}\right)$$

Equation 10

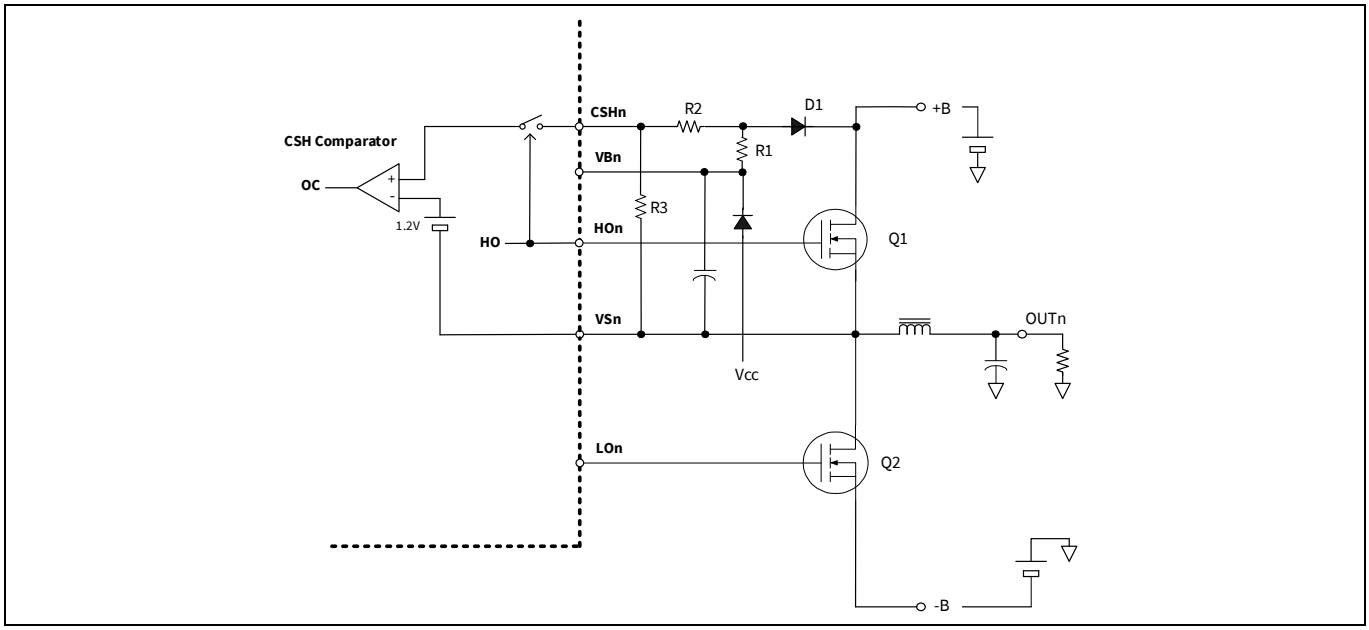


Figure 22 Programming high-side current threshold

7 Protections

A OCP trip point of $R_{DS(on)}$ based current sensing changes according to the junction temperature (T_J) of the sensing MOSFET. The OCP threshold reduces at higher T_J. Therefore, consider operating T_J and set a threshold not to trigger within normal operating conditions. The current sensing in the IRS2452BM is designed to handle output inductor core saturation. Setting a trip threshold above the output inductor saturation current is to set the OCP threshold at the inductor saturation point.

In the following example, the overcurrent protection level is set to trip at 30 A using a MOSFET with an $R_{DS(on)}$ = 100 mΩ. The component values of R2 and R3 can be calculated using the following formula:

Let R2 + R3=10 kΩ.

$$R_3 = 10\ k\Omega \times \frac{Vth_{OCH}}{V_{DS}+V_F}$$

Equation 11

Where,

Vth_{OCL} = 1.2 V

V_F = Forward voltage of reverse blocking diode D1 = 0.6 V

$V_{DS@ID=30\ A}$ = Voltage drop across the high side MOSFET when the MOSFET current is 30 A

Therefore, $V_{DS@ID=30A} = I_D \times R_{DS(on)}$ = 30 A x 100 mΩ = 3 V

Based on the formulas above, closest resistor values in E12 series are R2 = 6.8 kΩ and R3 = 3.3 kΩ.

7.2.3 Choosing the reverse blocking diode

The CSL and CSH sensing diodes require a reverse voltage higher than the supply voltage between +B and –B. The reverse recovery time must be less than 100 ns. A diode such as the MURA140T3G, rated at 400 V, t_{rr} = 65 ns high-speed switching diode or equivalent fits well.

7.3 Overtemperature protection (OTP) input

The overtemperature protection (OTP) input uses an external PTC thermistor or thermostat to monitor the temperature of the MOSFET. The OTP pin sources a 0.6 mA internal current to the external thermal sensor. Overtemperature protection activates when the voltage at any of OTP input pins reaches higher than 2.8 V that makes the typical threshold sensor resistance 4.7 kΩ.

The OTP pin of IRS2452BM is designed for connecting a PTC thermistor with characteristics shown in Figure 24. Recommended PTC thermistor includes PRF15xx471QB1RC, PRF18xx471QB1RB, or PRF21xx471QB1RA series (Murata Electronics) or similar. A mechanical thermostat switch or a thermostat IC with open drain output, such as LM26 (Texas Instruments), can also be used as a temperature sensor for better accuracy as shown in Figure 25.

7 Protections

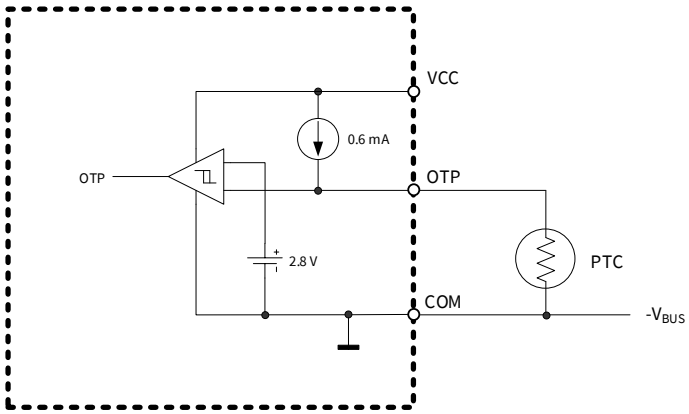


Figure 23 Overtemperature protection (OTP) input structure

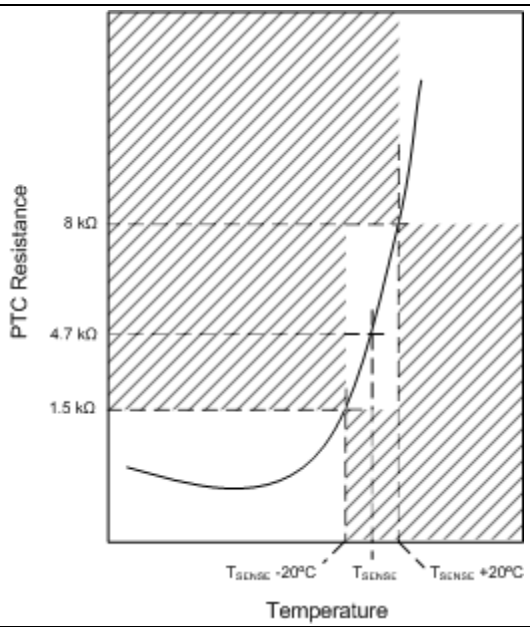


Figure 24 Recommended PTC sensor characteristics

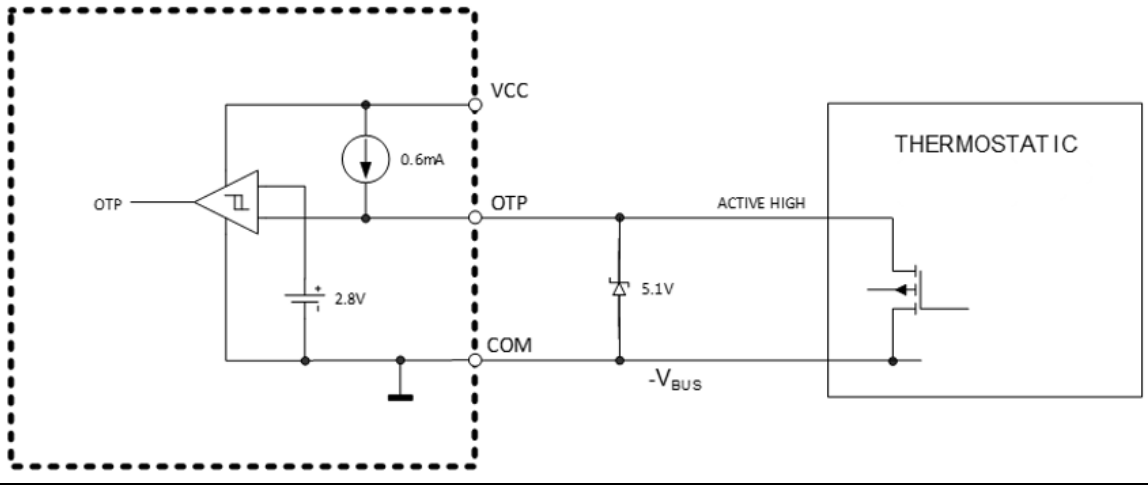


Figure 25 OTP pin with thermostat IC

7.4 Undervoltage protection (UVP)

To prevent a partial on state of the external MOSFET, undervoltage protection monitors the low-side and high-side gate bias supplies, VCC, and VB. When VCC is below UVLO, both high- and low-side MOSFETs are turned off. When the high-side supply V_{BS} is below the UVLO threshold, the high-side output is disabled, while the low-side works normally.

8 Power supply design

8.1 Supplying VAA and VSS

VAA and VSS are supply voltages at the front-end of the analog section, therefore, they are noise sensitive. For best audio performance, use regulated power supplies for VAA and VSS.

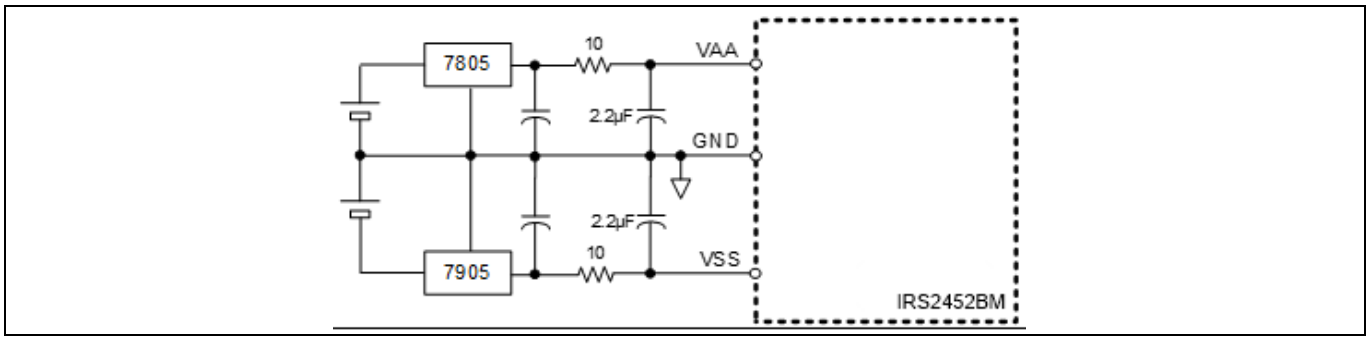


Figure 26 Supplying VAA and VSS with external voltage regulators

When switched mode regulators are used as power supply voltages for VAA and VSS, place a two-stage R-C noise filter in the supply lines as shown in Figure 27.

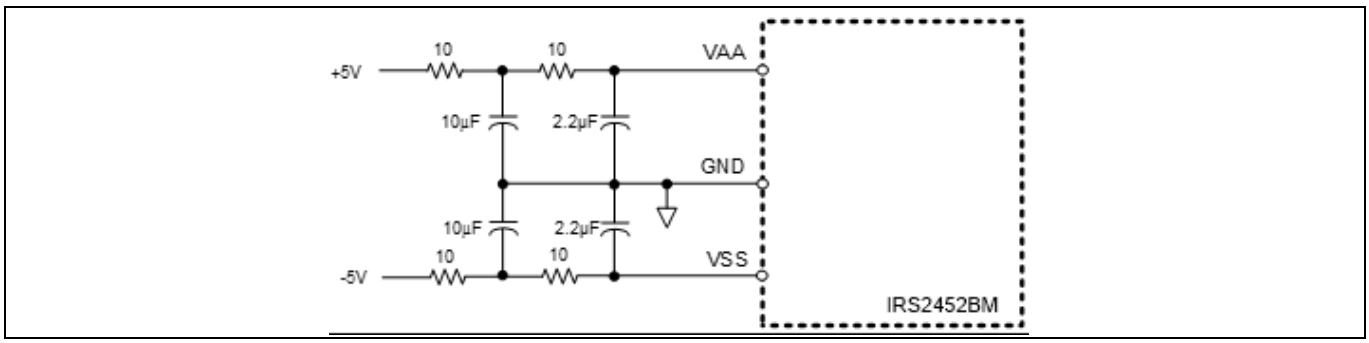


Figure 27 Supplying VAA and VSS from switched mode power supply

8.2 Supplying VCC and VB

Figure 28 shows the recommended power supply configuration for gate driver power supplies. The gate driver stage has four power supply inputs:

- VB1-VS1: CH1 high side gate drive supply
- VB2-VS2: CH2 high side gate drive supply
- VCC-COM: CH1-2 low side gate drive supply

The low-side power supply (VCC) feeds the internal gate drive logic and low-side gate driver. To protect VCC from switching noise generated by the VS node, it is recommended to insert a few ohms of RVBS in the bootstrap charging path.

The high-side driver requires a floating supply VBn referenced to the respective switching node VSn where the source of the output MOSFET is connected. A charge pump method (floating bootstrap power supply) eliminates the need for a floating power supply and therefore, it is used in the typical application circuit. The floating bootstrap power supply charges the bootstrap capacitor (C_{BS}) from the low-side power supply VCC during the low-side MOSFET ON period. When the high-side MOSFET is ON, the diode cuts off and floats the VBS supply. CBS retains its VB supply voltage for the rest of the high-side ON duration.

R_{BS1} and R_{BS2} reduce switching noise triggered by Qrr of the bootstrap diodes, D_{BS1} and D_{BS2}. R_{VCC} filters out switching noise from the bootstrap charge pump. These optional filtering resistors are effective to achieve the best audio performance in higher power applications (>100 W).

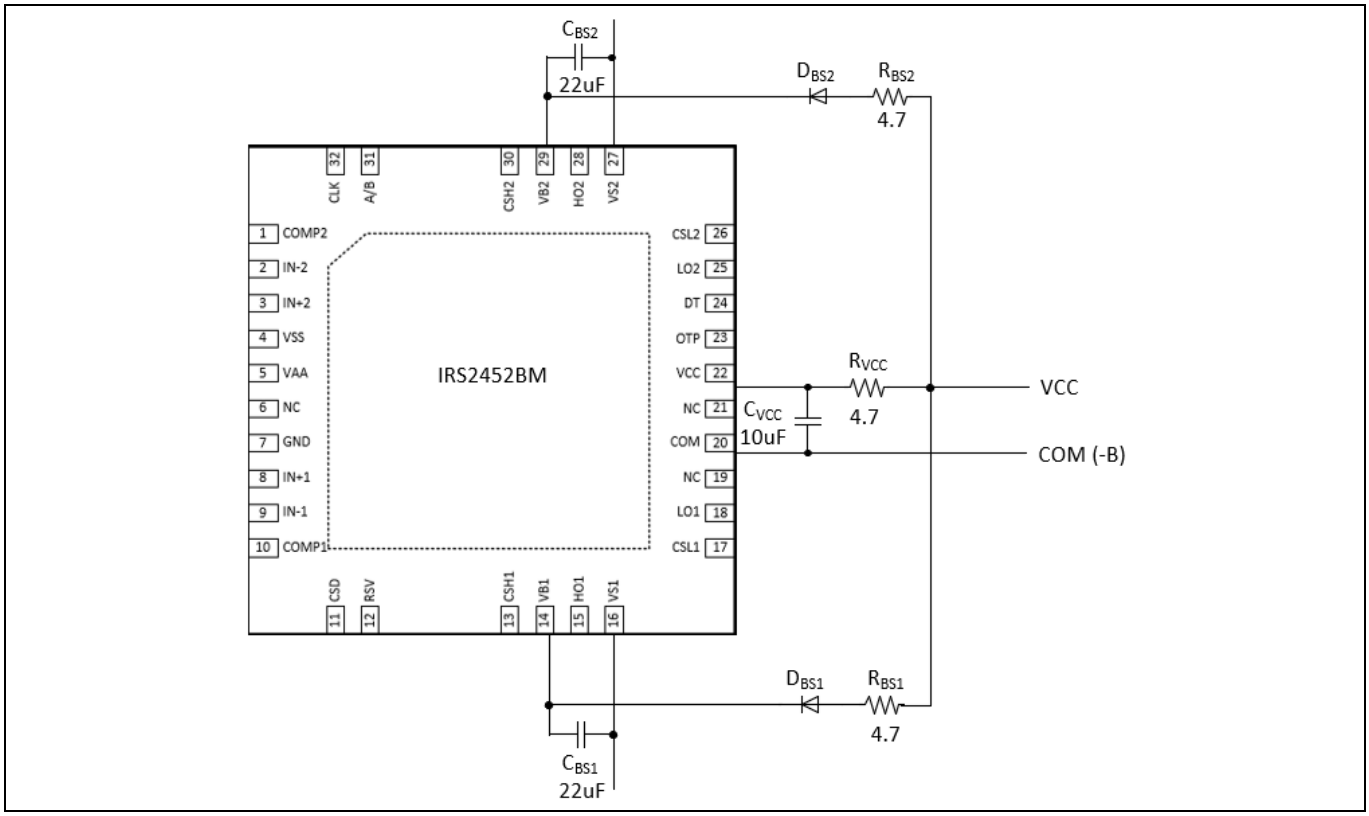


Figure 28 Recommended power supply configuration for gate driver stage

8.3 Bottom pad connection

The exposed bottom pad in the MLPQ 32L package where the IC die rests has the same voltage potential as COM. However, it is not directly connected internally. The pad may be tied to COM with short distance trace(s), or floated. Do not use the bottom pad as the low side power supply return path.

8.4 Designing high-side bootstrap power supply

The high-side driver requires a floating supply VBn referring to the respective switching node VSn where the source of the MOSFET is connected. A charge pump method (floating bootstrap power supply) eliminates the need for a floating power supply and therefore, it is used in the typical application circuit.

8.4.1 Floating bootstrap power supply

The floating bootstrap power supply charges the bootstrap capacitor (C_{BS}) from the low-side power supply (VCC) during the low-side MOSFET ON period. When the high-side MOSFET is ON, the charging diode turns off to float the VBS supply. C_{BS} retains its voltage as a floating power supply referenced to VS. Before C_{BS} discharges and VBS crosses the undervoltage lock out threshold UVBS, the next charging cycle should start by turning on the low-side MOSFET.

Figure 29 depicts the low-side MOSFET ON state. I_1 turns off the high-side MOSFET first, then I_2 turns on the low-side MOSFET. As soon as the switching node VS reaches the negative supply (–B), the bootstrap diode (D_{BS}) turns on and starts charging C_{BS} with current I_3 from VCC. Note that VBS = VCC – (forward drop voltage of D_{BS}).

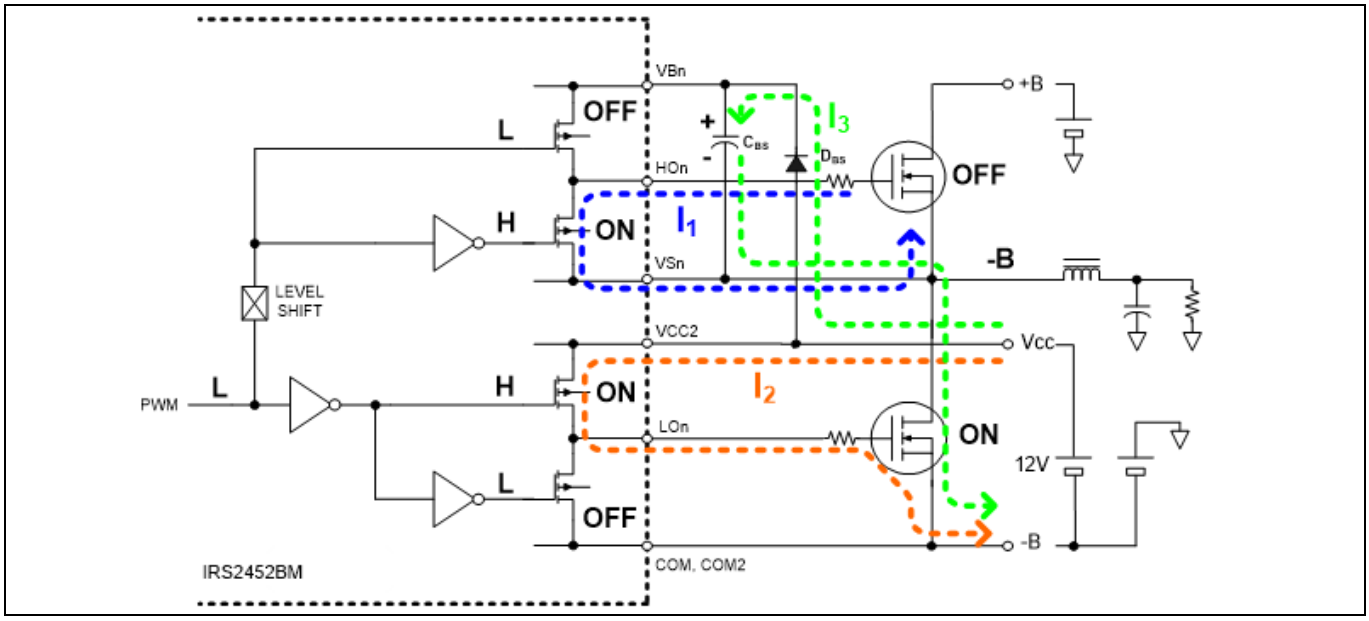


Figure 29 Charging VBS: Low-side ON period

After the low-side conduction period, I4 in Figure 30 turns off the low-side MOSFET. Then I5 turns on the high-side MOSFET, increasing VS up to +B. As long as the high side is ON, the bootstrap diode (D_{BS}) isolates the floating power supply VBS.

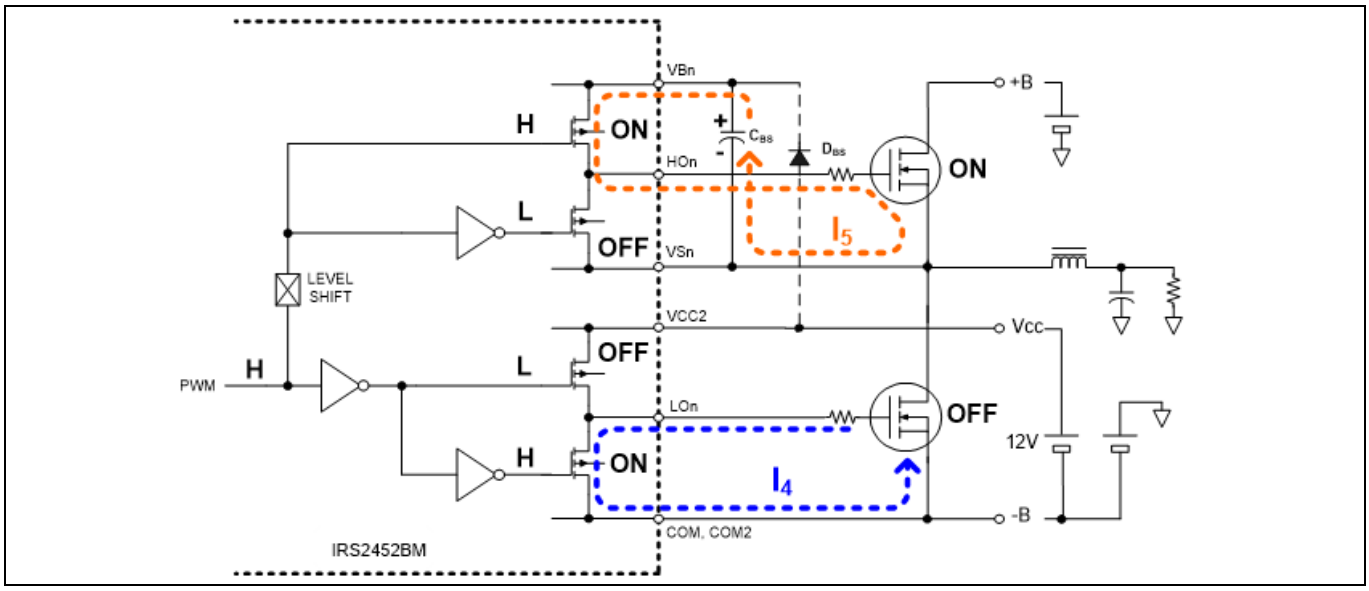


Figure 30 High-side ON period

8.4.2 Choosing bootstrap capacitance

During the high side on period, the bootstrap capacitor (C_{BS}) holds the high-side supply voltage. Quiescent current (I_{QBS}) in the high-side gate driver, precharges the resistor, and I_{R1} a current through high-side current sensing resistor R1 discharge the C_{BS} (Figure 32). The I_{QBS} and I_{R1} are the most significant contributors and the others are negligible.

The minimum bootstrap capacitance is determined as follows:

$$C_{BS} >> \frac{(I_{QBS}+I_{R1})\cdot t_{ON}}{VCC-1.5-UVBS}$$

Equation 12

Where,

C_{BS} = Floating bootstrap capacitance (F)

I_{QBS} = High-side quiescent current (A)

I_{R1} = High-side current sensing bias current (A)

t_{ON} = Longest high-side MOSFET conduction time (s)

VCC = Low-side power supply voltage (V)

UVBS = High-side undervoltage lockout threshold (V)

1.5 = Voltage drop in the bootstrap charging diode (D_{BS})

Often the IRS2452BM uses hard clipping condition. The continuous high-side ON duration could endure as long as it is half of the lowest audio frequency, tens of milliseconds. A typical application uses a 22 µF C_{BS} to support low audio frequency clipping. Since the bootstrap capacitor sees the VCC supply voltage, a ceramic capacitor (X7R, X5R, or X5S type) or aluminum electrolytic capacitor with 25 V or higher voltage rating is recommended.

8 Power supply design

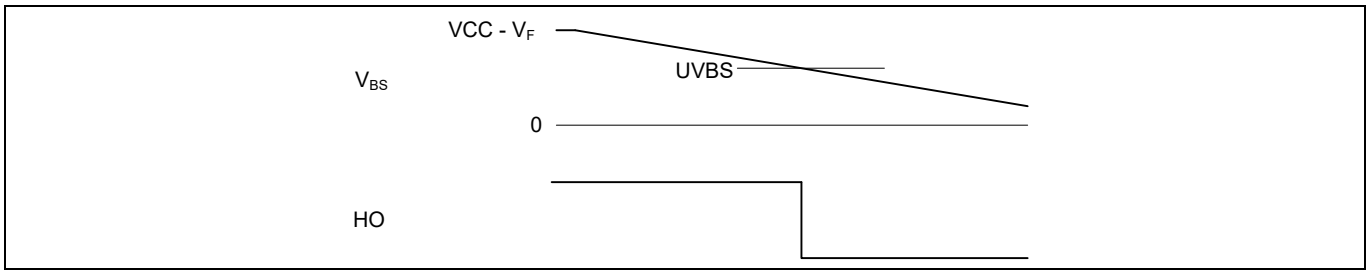


Figure 31 V_{BS} discharging

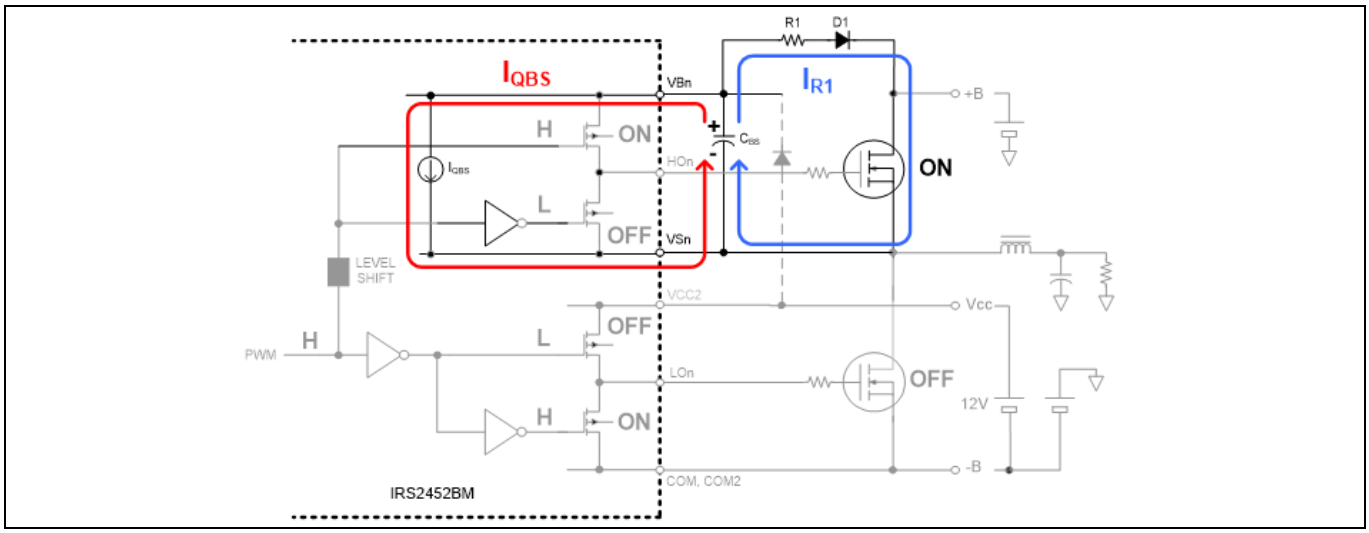


Figure 32 C_{BS} discharging during high-side ON period

8.4.3 Choosing bootstrap diode

Use a bootstrap charging diode with voltage rating of 1.5 x the maximum bus voltage. To charge the bootstrap capacitor in a very short low-side ON period with a high PWM modulation ratio, a fast recovery diode type (trr < 50 nS) is recommended.

8.4.4 Charging V_{BS} prior to start

For proper start-up in a self-oscillating PWM configuration, precharging the bootstrap supply V_{BS} prior to PWM start-up ensures that the oscillation can start with either high-side or low-side first. A charging resistor R_{CHARGE}, inserted between the positive supply bus and VB, charges C_{BS} prior to switching as shown in Figure 33. The minimum resistance of R_{CHARGE} is limited by the maximum continuous ON duration of the high side MOSFET. When the high-side MOSFET is on, R_{CHARGE} drains the bootstrap power supply together with the quiescent current I_{QBS} so it reduces holding up time.

The maximum resistance of R_{CHARGE} is limited by the current charge capability of the resistor during startup:

$$I_{CHARGE} > I_{QBS}$$

Equation 13

8 Power supply design

Where,

I_{CHARGE} = Current through R_{CHARGE}

I_{QBS} = High-side supply quiescent current, 1 mA

The pre-charging current flows into the speaker load. A balancing resistor ($R_{BALANCE}$) and a dummy load (R_{DUMMY}) reduces the DC current flows in to the load.

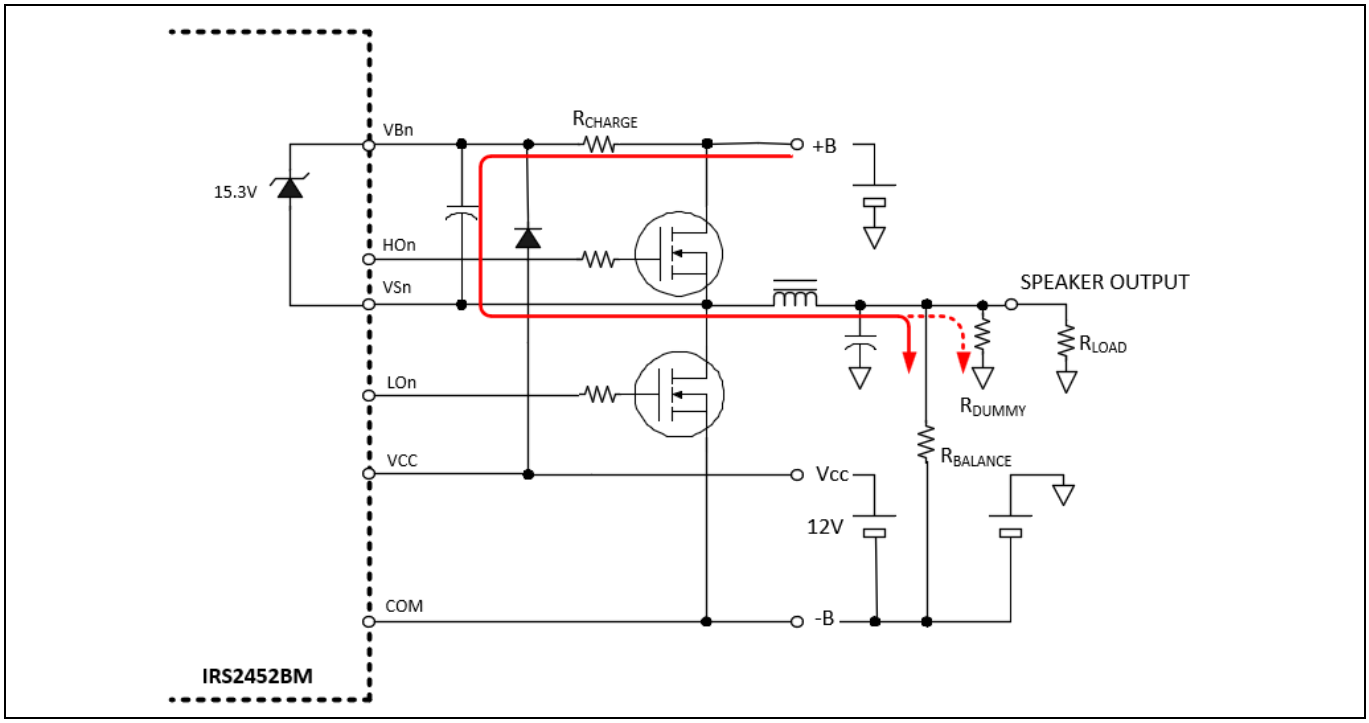


Figure 33 Pre-charging bootstrap supply

8.5 Start-up/power-down sequence

The protection control block in the IRS2452BM monitors the status of V_{AA} and V_{CC} to ensure that both voltage supplies are above their respective undervoltage lockout (UVLO) thresholds before beginning normal operation. If either V_{AA} or V_{CC} is below the undervoltage threshold, LO and HO are disabled in shutdown mode until both V_{AA} and V_{CC} rise above their voltage thresholds.

As soon as V_{AA} or V_{CC} falls below its UVLO threshold, protection logic in the IRS2452BM turns off LO and HO, shutting off the power MOSFETs.

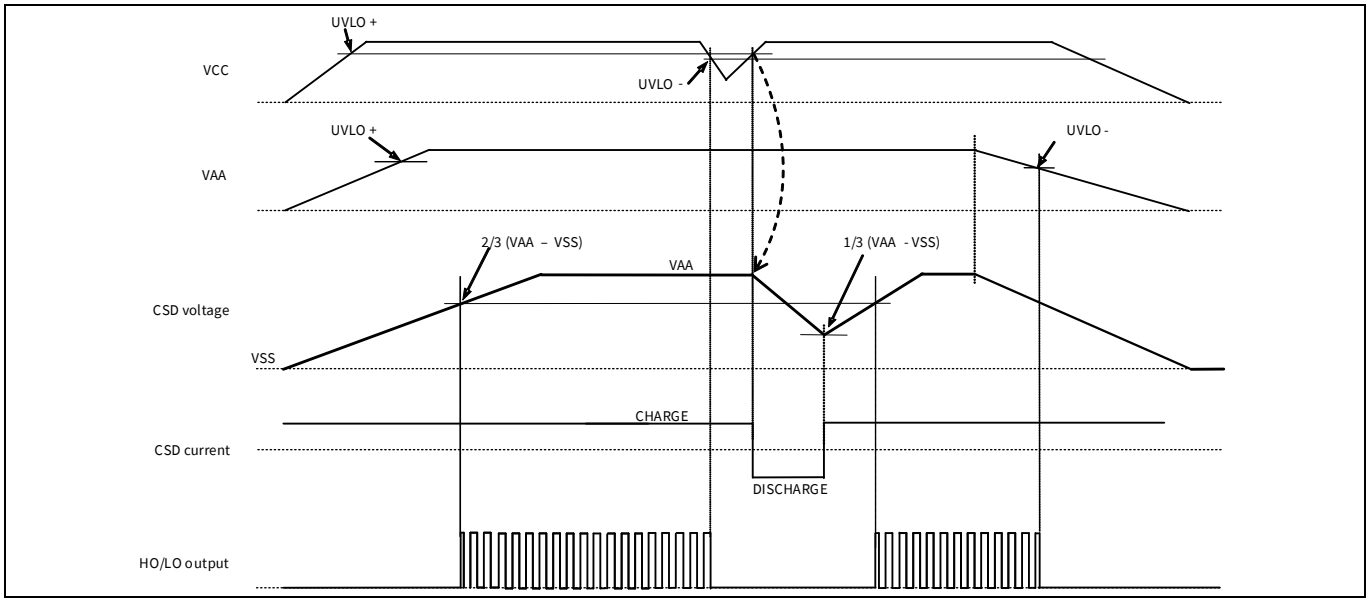


Figure 34 IRS2452BM UVLO timing chart

8.6 Power supply decoupling

Due to the analog circuitry in the IRS2452BM, careful attention must be given to decoupling the power supplies for proper operation of the IC. Ceramic capacitors (minimum of 0.1 µF) or aluminum capacitors (minimum of 1 µF) should be placed close to the power supply pins of the IC on the board. Due to large capacitance variations, Y5V dielectric or similar type ceramic capacitors are not recommended.

See the application note AN-978 [2] for general design considerations of a high voltage gate driver IC.

9 Board layout considerations

The reliability of products in the PQFN package is subject to the board mounting process. The soldering process is critical. See the application note AN-1170 [3] audio IC board mounting application note for specific footprint design and soldering methods.

9.1 Board layout plan

There are functional blocks that generate noise and there are functional blocks that are sensitive to noise. The PCB designer should identify them and find out the best component placement based on these facts as well as mechanical and thermal requirements.

Noise sensitive functions:

- The audio input circuitry, especially IN+ and IN-
- Clock input

Noise generating functions:

- Gate driver stage, especially VB, CSH, and VS
- MOSFET stage

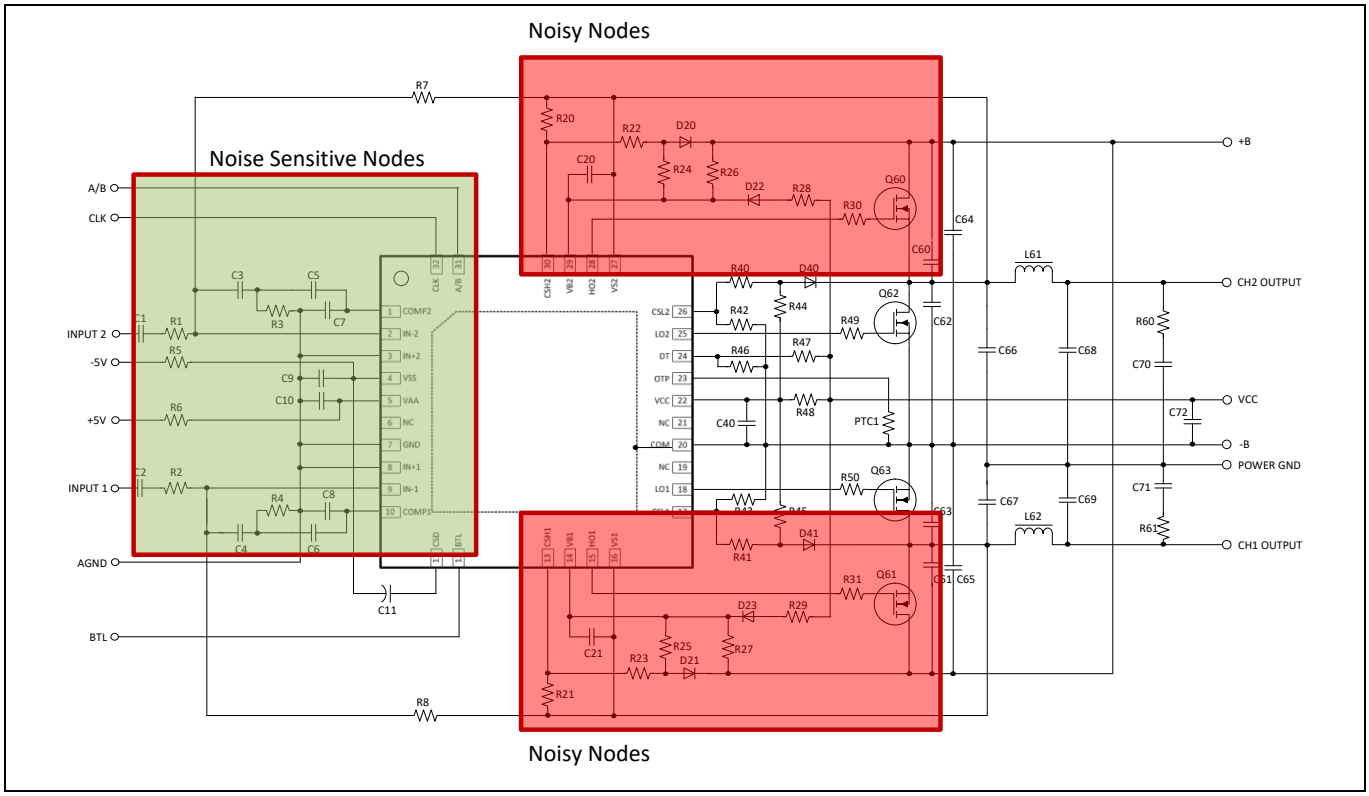


Figure 35 Noise mapping of IRS2452BM application

It is important to properly locate the ground planes to obtain good audio performance. As each functional block within refers to different potentials, it is recommended to apply three reference potentials, analog, gate drive, and power grounds.

Figure 36 is a PCB layout example used with the IRAUDAMP23 [1] reference design. Note that there is no overlap between the input GND plane and the noisy switching nodes: VS1, VS2, and high side components. Stray

inductance in the VS connection is less influential than +B and –B so prioritize these power supply traces. Prioritize +B to –B power traces for minimum impedance.

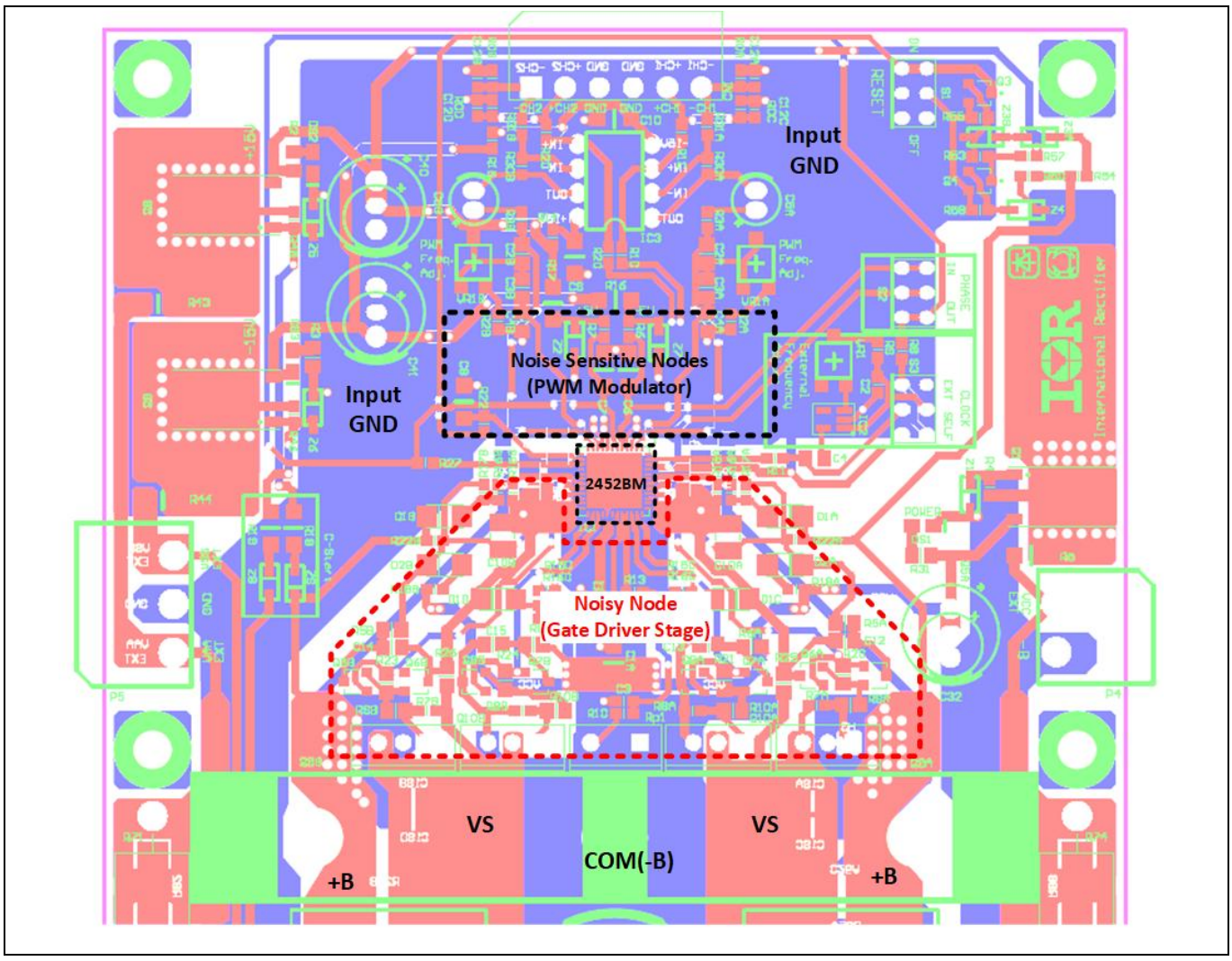


Figure 36 Noise mapping of IRS2452BM PCB design example

9.2 Analog ground

The input analog section is referenced to the signal ground, or GND, which should be a quiet reference node for the audio input signal. The peripheral circuits in the floating input section such as CSD and COM pins refer to this ground. These nodes should all be separated from the switching stages of the system. To prevent potential capacitive coupling to the switching nodes, use a ground plane only in this part of the circuit. Do not share the signal ground plane with the gate driver or power stages unless there is a dedicated layer for the GND plane.

9.3 Gate driver reference

The gate driver stage of the IRS2452BM is located between pins 13 and 30 and is referenced to the negative bus voltage, COM. This is the substrate of the IC and acts as ground. Although the negative bus is a noisy node in the system, both of the gate drivers refer to this node. Therefore, it is important to shield the gate drive stages with the negative bus voltage so that all the noise currents due to stray capacitances flow back to the power supply without degrading the signal ground.

9.4 Power ground

Power ground is the ground connection that closes the loops of the bus capacitors and inductor ripple current circuits. Separate the power ground and input signal grounds from each other as much as possible to avoid common stray impedances.

Figure 37 illustrates how to lay out reference planes. The power GND plane should include a negative bus capacitor. The power reference plane should include Vcc. Also, use distinctly different symbols for the different grounds.

For further board layout information, see AN-1135 [4], PCB Layout with IR Class D audio gate drivers.

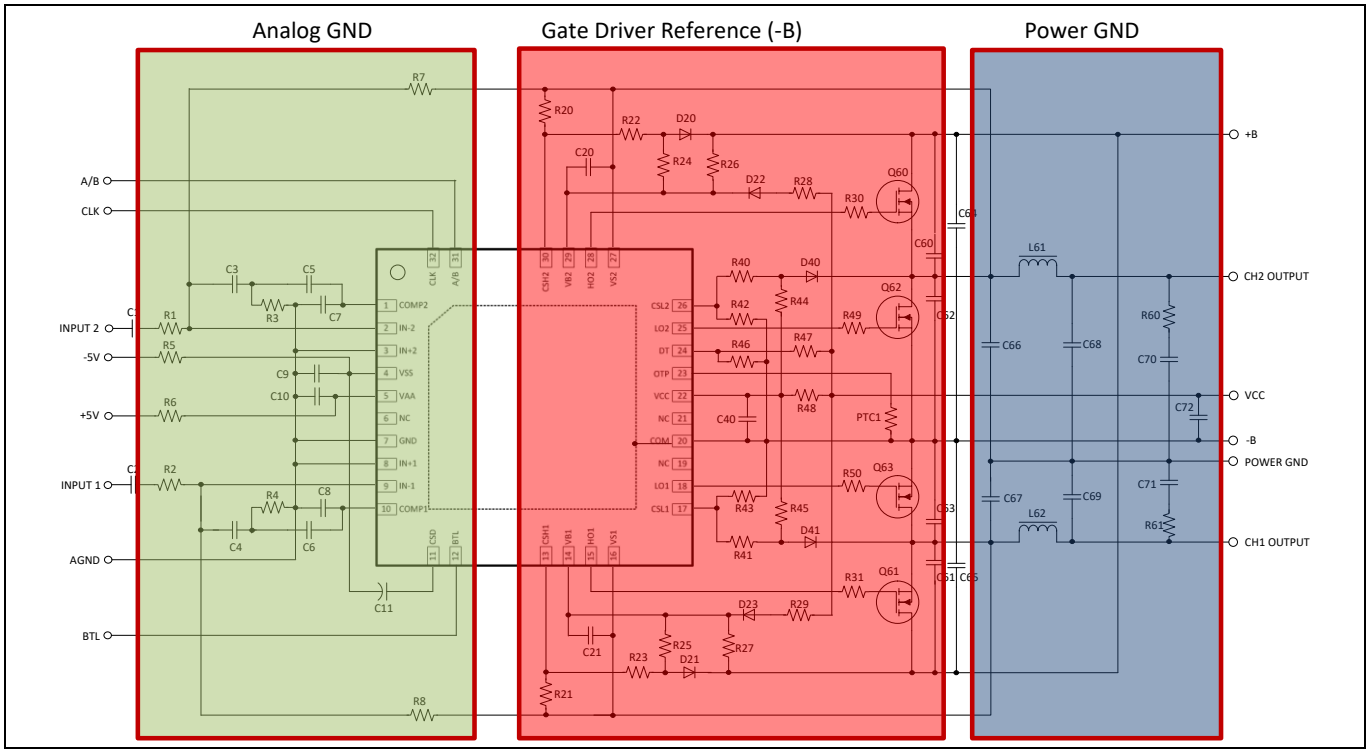


Figure 37 Applying ground planes

10 Thermal considerations

The major power dissipation of the IRS2452BM comes from the high-voltage level-shifter inside and is proportional to the high-voltage bias voltage to the VS nodes and the PWM frequency.

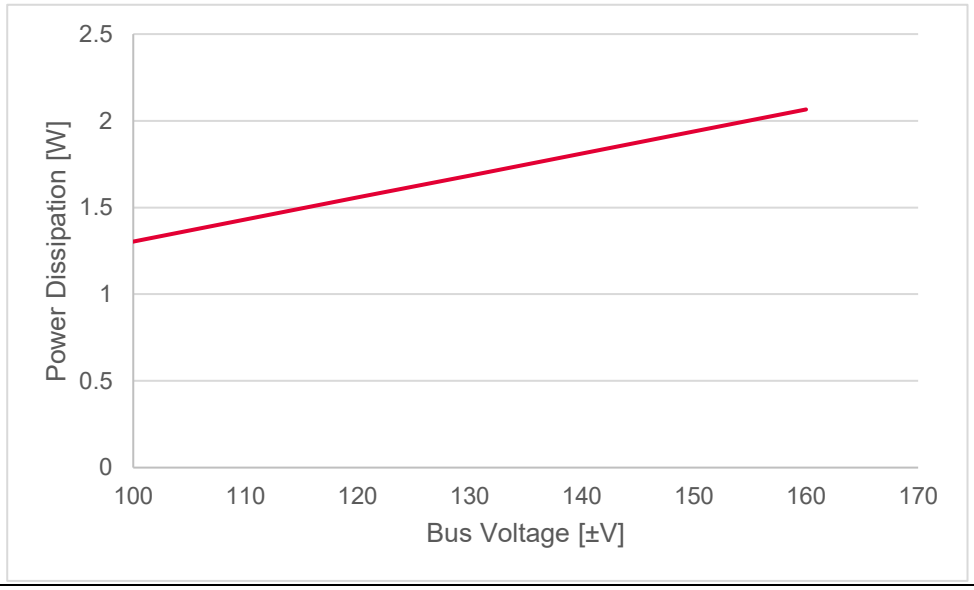


Figure 38 Supply voltage vs. power dissipation at 325 kHz

Figure 39 shows operational supply voltage ranges that meet Tc < 100°C on the IRAUDAMP23 [1] board operating at 325 kHz PWM frequency.

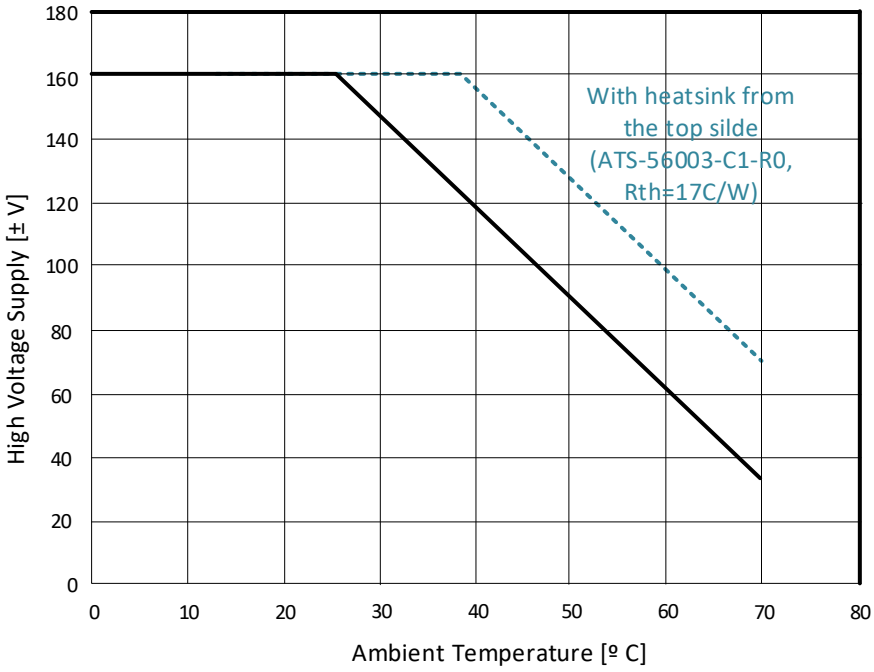


Figure 39 Ambient temperature vs. high-voltage supply voltage for Tc < 100°C

11 Related resources

- Webpage: Discrete MERUS™ Class D audio amplifier ICs
- IRS2452BM datasheet
- Infineon Developer Community: MERUS™ Class D forum
- User guide: REF_AUDIO_SiC_2kW Class D audio reference board with CoolSiC™ 400 V transistors and MERUS™ IRS2452BM audio IC
- User guide: IRAUDAMP23 500 W x 2 channel constant voltage Class D audio amplifier using the IRS2452BM

References

[1] Infineon Technologies AG: *UG_1811_PL88_1812_191445 – 500 W x 2 channel constant voltage Class D audio amplifier using the IRS2452BM*; Available online

[2] Infineon Technologies AG: *AN-978 – HV floating MOS-gate driver ICs*; Available online

[3] Infineon Technologies AG: *AN-1170 – Audio power quad flat no-lead (PQFN) board mounting*; Available online

[4] Infineon Technologies AG: *AN-1135 – PCB layout with IR Class D audio gate drivers*; Available online

Abbreviations and acronyms

Table 4 Abbreviations and acronyms

Abbreviation/symbol	Expansion
BJT	Bipolar junction transistor
C_{BS}	Bootstrap capacitor
CSD	Control and shutdown
Ct	Timing capacitor
DC	Direct current
DT	Dead-time
G_V	Voltage gain
HO	High-side output
IC	Integrated circuit
I_{QBS}	Quiescent current
IRMS	Root mean square current
LC	Inductor-capacitor
LO	Low-side output
LPF	Low pass filter
OPA	Operational amplifier
OTA	Operational transconductance amplifier
OCP	Overcurrent protection
OTP	Overtemperature protection
PQFN	Plastic quad flat no-lead
PWM	Pulse-width modulation
PTC	Positive temperature coefficient
RC	Resistor-capacitor
$R_{DS(on)}$	On-state resistance
THD	Total harmonic distortion
THD+N	Total harmonic distortion + noise
UVLO	Undervoltage lockout
UVP	Undervoltage protection
V_{BS}	Bootstrap supply voltage
VCC	Low-side gate drive supply voltage
V_{DS}	Drain-to-source voltage
VF	Forward voltage
VS	Switching node voltage
ZVS	Zero-voltage switching

Revision history

Document revision	Date	Description of changes
V 1.0	2026-06-01	Initial release

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Edition: 2026-06-01

Published by
Infineon Technologies AG
Am Campeon 1-15
85579 Neubiberg, Germany

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AN222011

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