XDPL8210 design guide

For high power factor flyback converter with dimmable constant current output

About this document

Scope and purpose

This document is a design guide using XDPL8210 as the control IC of the High Power Factor (HPF) Flyback converter, which has a dimmable Constant Current (CC) output based on Primary-Side Regulation (PSR), for LED lighting applications. It also includes a design guide on pairing XDPL8210 with a dimming interface IC named CDM10VD, to achieve 0–10 V dimming with dim-to-off option, while isolating the connected dimmer not only from the primary-side circuitry, but also from the LED load-connected circuitry.

Intended audience

Power supply design engineers, field application engineers.

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1 Introduction

XDPL8210 regulates the CC output of a HPF Flyback converter, based on PSR. The secondary-side circuitry and optocoupler used for output regulation can therefore be omitted.

Figure 1 shows the simplified circuitry for non-dimming application.

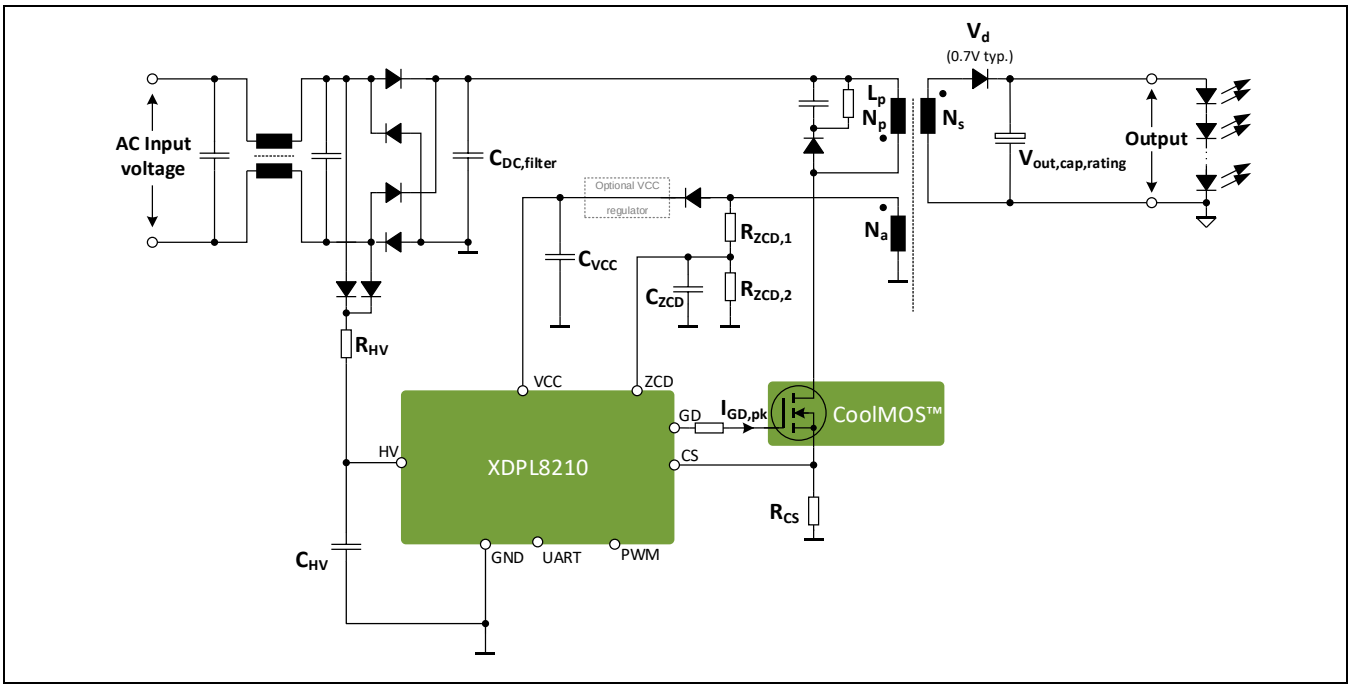


Figure 1 Simplified circuitry for non-dimming application

Figure 2 shows the simplified circuitry for 0–10 V dimming application, which uses a device called CDM10VD plus an optocoupler for transmitting the dimming signal to the XDPL8210 PWM pin, while isolating the connected dimmer not only from the primary-side circuitry, but also from the LED load-connected circuitry.

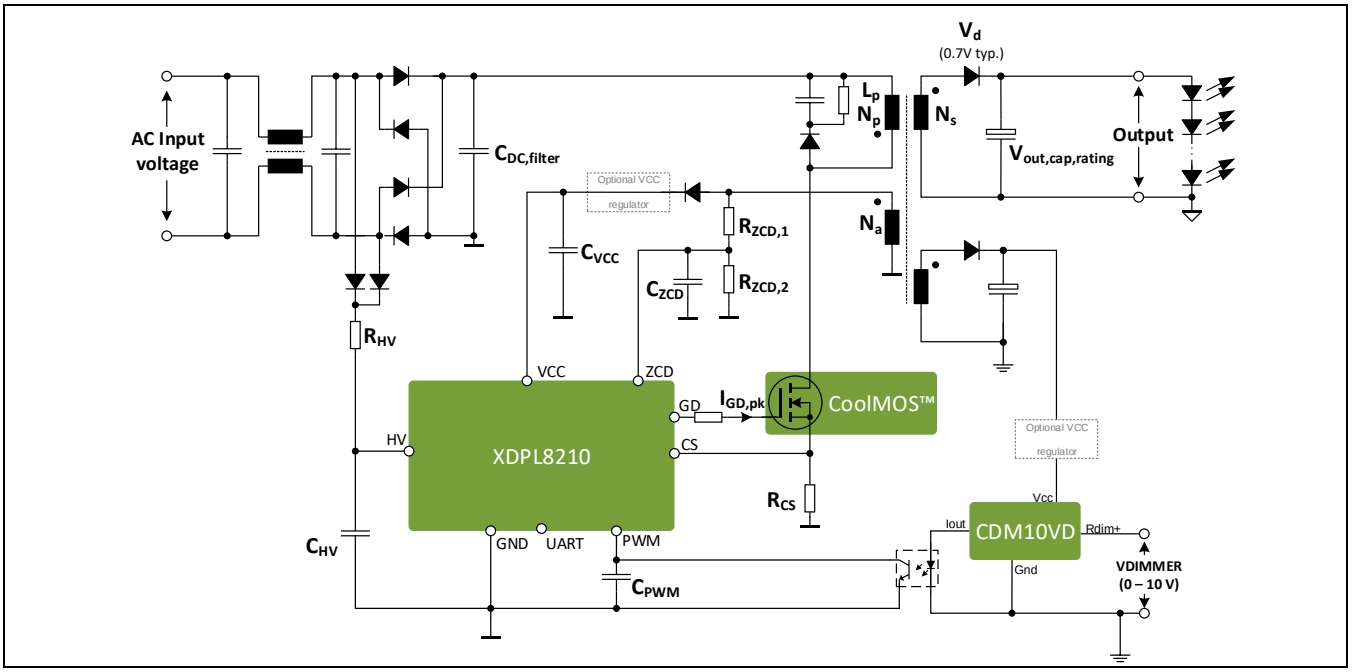


Figure 2 Simplified circuitry for 0–10 V dimming application

*Note: CDM10VD is a device which transmits analog voltage-based signals from a 0–10 V dimmer or potentiometer to the dimming or PWM input of a lighting controller IC in the form of a 5 mA current-based PWM signal to drive an external isolated optocoupler. It replaces many components in a traditional solution and reduces the Bill of Materials (BOM) and PCB space significantly. For more details about CDM10VD, please visit the **Infineon website**.*

Figure 3 shows the simplified circuitry for the wireless or DALI dimming application, which typically has a microcontroller for transmitting the PWM dimming signal to the XDPL8210 PWM pin.

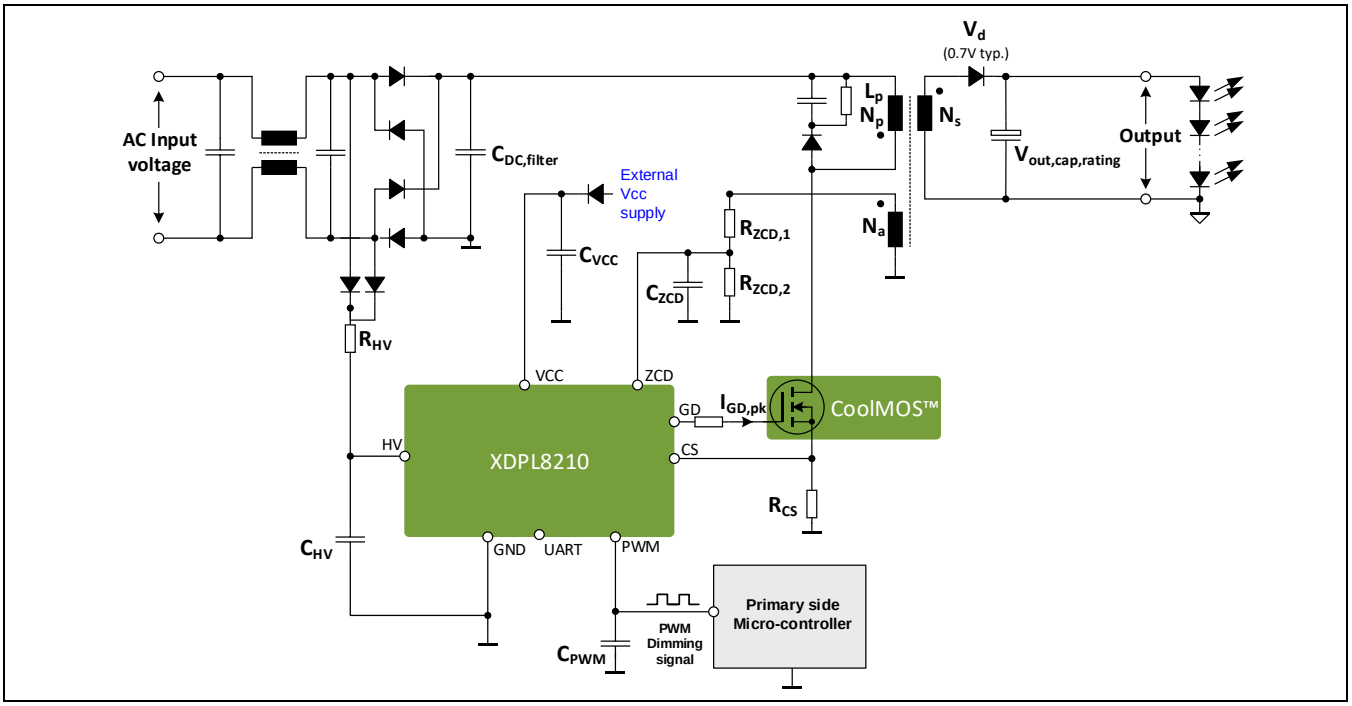


Figure 3 Simplified circuitry for wireless or DALI dimming application

XDPL8210 comes in a PG-DSO-8 package with eight pins, as shown in the datasheet [1]. The main functions of each pin are shown in **Table 1**.

Table 1 XDPL8210 pins assignment

Pin	Symbol	Type	Pin name and main functions
1	ZCD	Input	Zero Crossing Detection pin: • Transformer auxiliary winding ZCD via external resistor-divider • Sensing of the reflected input and output voltage signals from auxiliary winding via external resistor-divider
2	PWM	Input	Pulse Width Modulation pin: • Dimming signal input pin
3	CS	Input	Current Sense pin: • Flyback MOSFET current sensing via external shunt resistor
4	GD	Output	Gate Drive pin: • Flyback MOSFET gate-drive control via external series resistor

Pin	Symbol	Type	Pin name and main functions
5	HV	Input	High Voltage pin: • V_{CC} charging via its internal 600 V start-up cell during start-up and protection • Rectified AC input voltage sensing via external series resistor for line synchronization
6	UART	Input /Output	Universal Asynchronous Receiver Transmitter pin: • Digital communication interface for IC parameter configuration
7	V_{CC}	Input	Voltage at Common Collector pin: • IC operating voltage supply and sensing
8	GND	–	Ground pin: • IC grounding

XDPL8210's IC parameters are configurable digitally via its UART interface, using Infineon's user-friendly Graphical User Interface (GUI) on a PC. This enables a lower BOM and rapid engineering changes without the need for complex component design iterations.

Note: By default, the configurable parameters of a new XDPL8210 chip from Infineon are empty, so it is necessary to configure them before any application testing.

Figure 4 shows the XDPL8210 design guide document sectioning for each step of the recommended design flow.

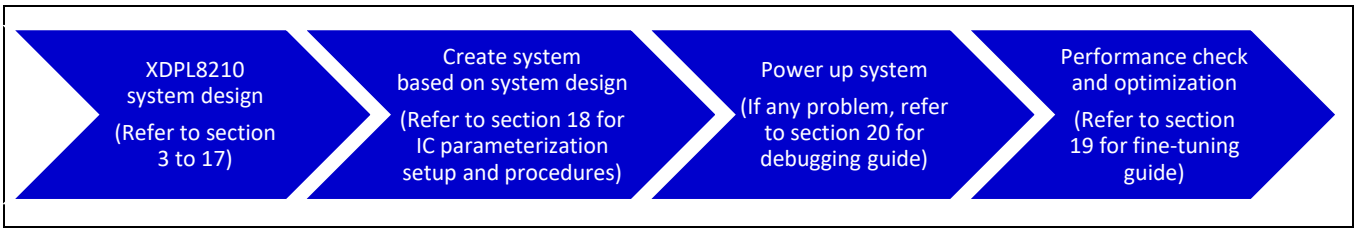


Figure 4 Recommended design flow I (referring to design guide document sections)

Apart from referring to the design guide document (see **Section 3** to **Section 17**), the XDPL8210 system design step can also be done by using the Microsoft Excel-based design tool, as shown in **Figure 5**.

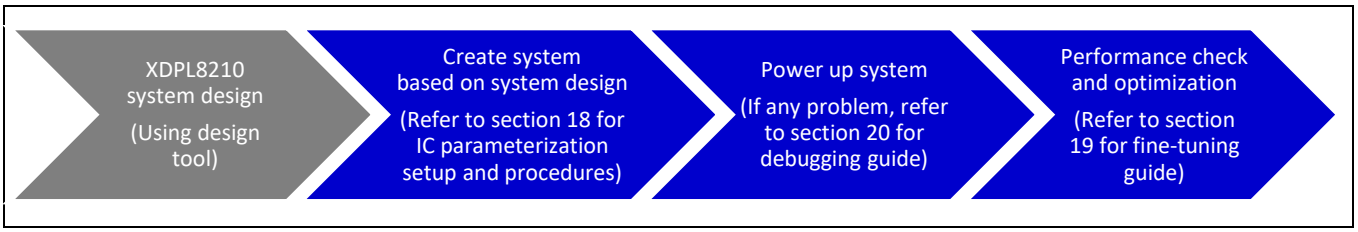


Figure 5 Recommended design flow II (using Excel tool and referring to design guide document sections)

2 Design specifications

A HPF Flyback converter with the following design specifications (see **Table 2**) and operating window has been selected as a design example.

Table 2 Design specifications

Specification	Symbol	Value	Unit
Normal operational minimum AC input voltage	$V_{AC,min}$	90	V_{rms}
Normal operational maximum AC input voltage	$V_{AC,max}$	305	V_{rms}
Normal operational AC input frequency	F_{line}	47 ~ 63	Hz
Steady-state maximum output current set-point	$I_{out,full}$	830	mA
Steady-state minimum output current set-point	$I_{out,min}$	41.5	mA
Dimmer voltage (analog)	V_{DIMMER}	0 ~ 10	V
Dimming curve	C_{DIM}	Linear	–
Dim-to-off	$EN_{DIM,TO,OFF}$	Yes	–
Steady-state maximum output LED load voltage	$V_{LED,max}$	54	V
Steady-state maximum output LED power	$P_{out,full}$	35	W
Steady-state minimum LED load voltage at V_{DIMMER} = 10 V (non-dimmed)	$V_{LED,min,non-dimmed}$	18	V
Steady-state minimum LED load voltage at $I_{out,min}$	$V_{LED,min,at,I,out,min}$	14	V
Steady-state minimum LED load voltage at V_{DIMMER} = 0 V (fully dimmed)	$V_{LED,min,fully-dimmed}$	13	V
Minimum efficiency at $P_{out,full}$	$\eta_{min,at,P,out,full}$	90	%
Target minimum switching frequency at $P_{out,full}$	$f_{sw,min,at,P,out,full}$	52.5	kHz

Note: The recommended $f_{sw,min,at,P,out,full}$ is between 50 kHz and 65 kHz. In general, a higher $f_{sw,min,at,P,out,full}$ value would result in a smaller Flyback transformer with lower efficiency, while a lower $f_{sw,min,at,P,out,full}$ value would result in a larger Flyback transformer with higher efficiency.

3 Output set-points and dimming related parameters design

Based on the design specifications in **Table 2**, the desired operating window shown in **Figure 6** can be achieved by configuring:

- Steady-state maximum output current set-point, **$I_{out,full}$ = 830 mA**
- Steady-state maximum output power limit set-point, **$P_{out,set}$ = 35 W**
- Steady-state minimum output current set-point, **$I_{out,min}$ = 41.5 mA**

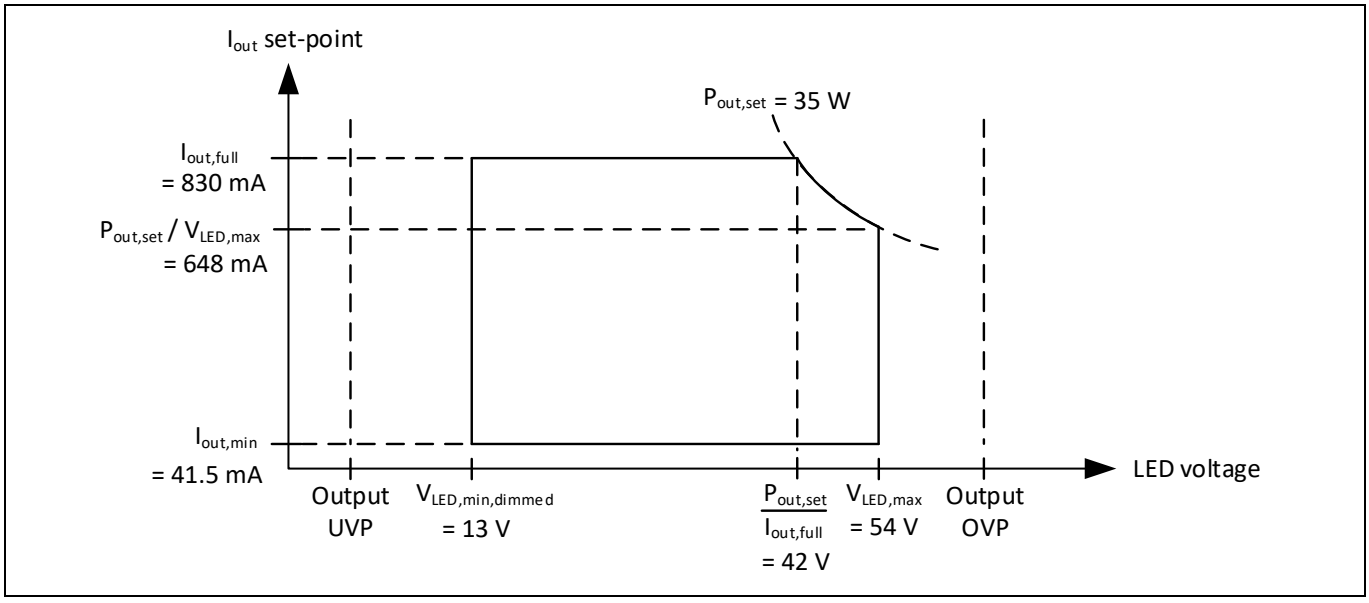


Figure 6 Operating window

Note: If the maximum output power limit is not desired in the operating window, $P_{out,set}$ can be configured above the multiplication of $V_{LED,max}$ and $I_{out,full}$.

Based on the design specifications in **Table 2**, the dimming-type parameter setting of **DIM_{type} = Dim (to off)** is selected, which activates the PWM duty-cycle level for entering dim-to-off $D_{DIM,off}$ and PWM duty-cycle level for exiting dim-to-off $D_{DIM,on}$, as shown in **Figure 7**.

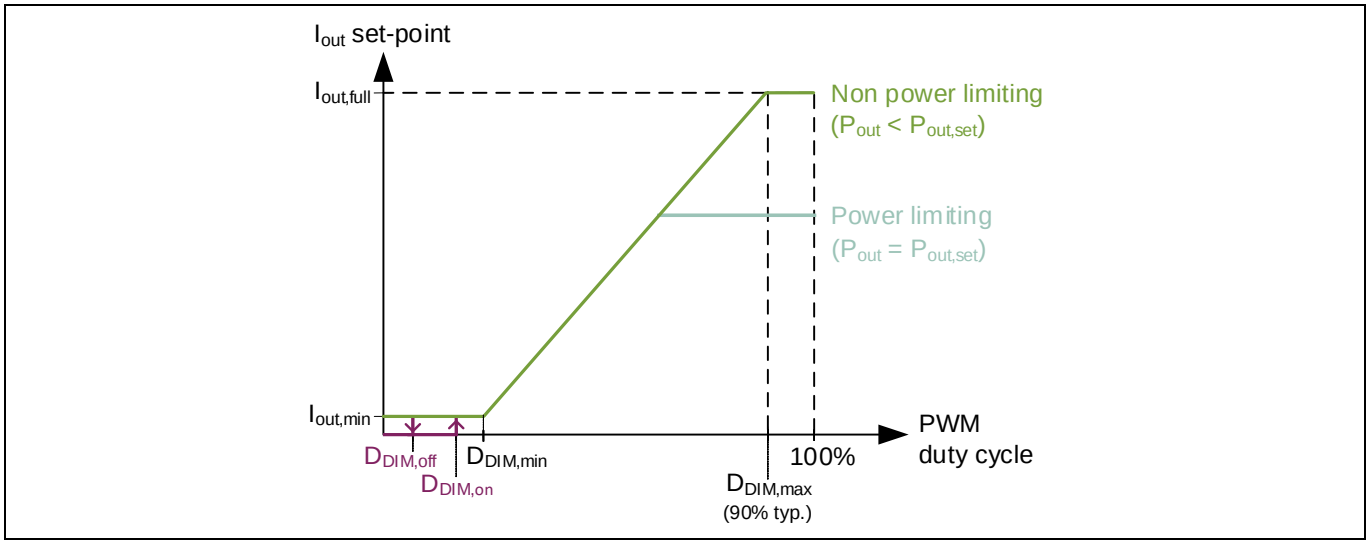


Figure 7 Output set-point based on measured PWM duty-cycle levels

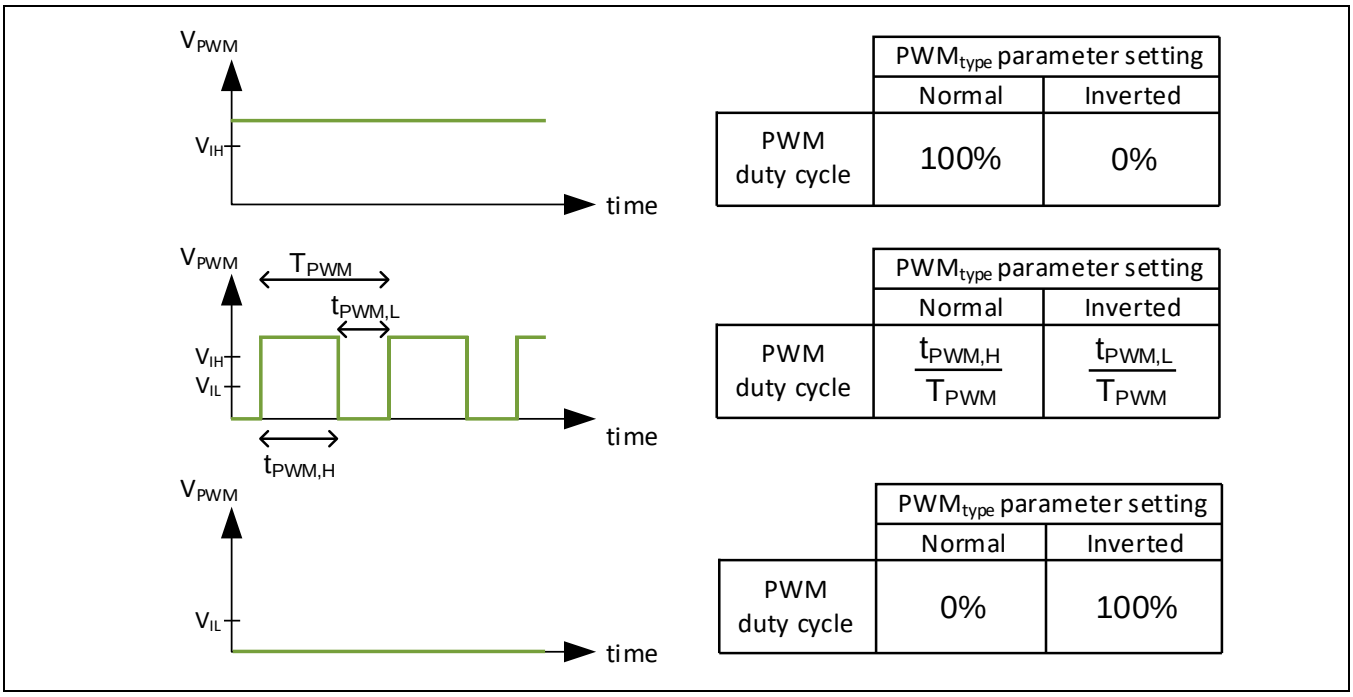
Note: If dimming operation is desired but without dim-to-off, the DIM_{type} parameter can be configured as "Dim (without off)" to deactivate $D_{DIM,off}$ and $D_{DIM,on}$.

Note: If non-dimming operation is desired, the DIM_{type} parameter can be configured as "Non-dim".

When using an optocoupler plus a device called CDM10VD to convert the 0–10 V dimmer voltage into PWM for transmission to the XDPL8210 PWM pin (see **Figure 2**), the PWM pin internal pull-up resistor should be enabled by configuring the $PWM_{R,pull,up}$ parameter between 2.25 kΩ and 30 kΩ. With lower pull-up resistance, the PWM duty cycle accuracy generated by the optocoupler is better with shorter voltage rise time, hence **$PWM_{R,pull,up}$ = 2.25 kΩ** is selected.

Based on the circuit operation In **Figure 2**, in which the output current and 0–10 V dimmer voltage are proportionate to the PWM pin voltage duty cycle based on an inverted PWM-type signal, the PWM-type parameter setting of **PWM_{type} = Inverted** shown in **Figure 8** is therefore selected in this design example.

The PWM period T_{PWM} should be fixed in the range from 0.5 ms to 2 ms. T_{PWM} generated by CDM10VD is typically 1 ms with ±5% tolerance. Therefore, in this design example, the maximum PWM frequency parameter setting of **$f_{PWM,max}$ = 1050 Hz** and minimum PWM frequency setting of **$f_{PWM,min}$ = 950 Hz** are selected.



	PWM_{type} parameter setting	
	Normal	Inverted
PWM duty cycle	100%	0%

	PWM_{type} parameter setting	
	Normal	Inverted
PWM duty cycle	$\frac{t_{PWM,H}}{T_{PWM}}$	$\frac{t_{PWM,L}}{T_{PWM}}$

	PWM_{type} parameter setting	
	Normal	Inverted
PWM duty cycle	0%	100%

Figure 8 PWM duty-cycle measurement based on PWM-type parameter setting (normal/inverted)

*Note: If the PWM pin is supplied with an active voltage signal, for example with the circuitry in **Figure 3**, PWM_{type} parameter can be configured as "Normal", while the $PWM_{R,pull,up}$ parameter can be configured as "Disabled".*

Either a linear or quadratic dimming curve can be configured based on the C_{DIM} parameter, as shown in **Figure 9**. Based on the design specifications in **Table 2**, the parameter setting of **C_{DIM} = Linear** is selected.

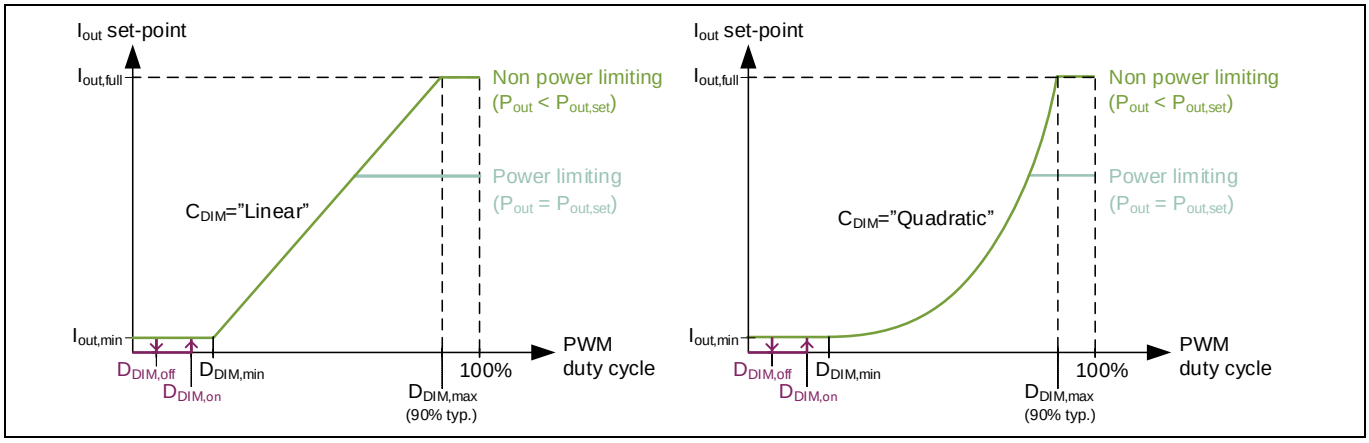


Figure 9 Output set-point based on selected dimming curve and measured PWM duty-cycle levels

Figure 10 shows the relationship between the PWM duty cycle and 0–10 V dimmer voltage, based on the CDM10VD datasheet. For example, the PWM duty-cycle level for maximum output current $D_{DIM,max}$ = 90 percent is reached when the dimmer voltage V_{DIMMER} is 8.52 V.

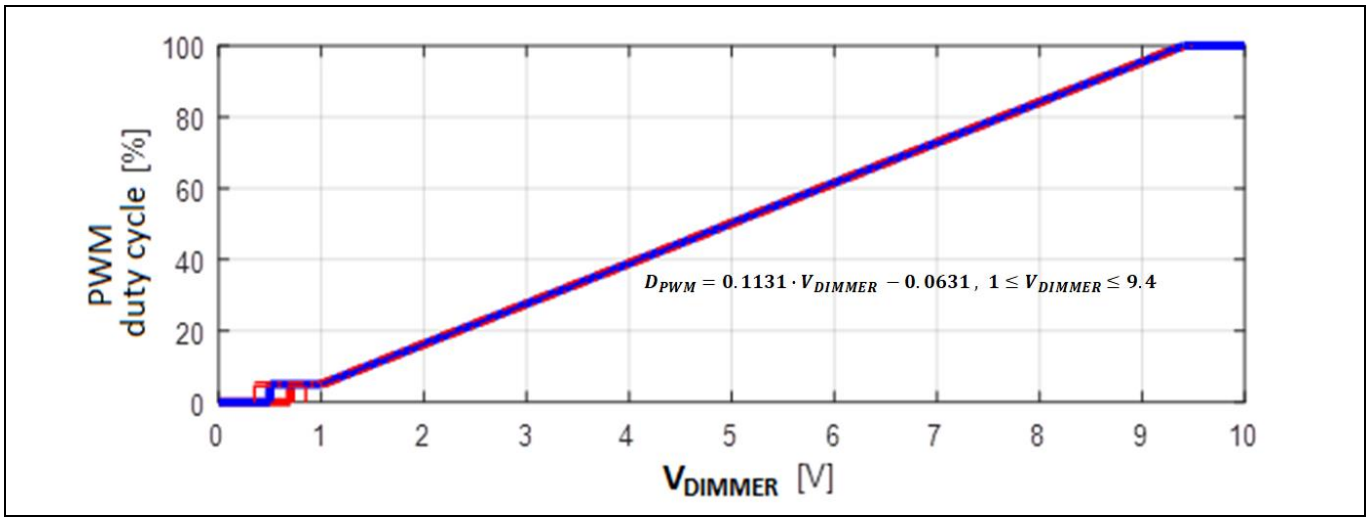


Figure 10 PWM duty cycle generated by CDM10VD based on 0–10 V dimmer voltage

By referring to **Figure 10**, $D_{DIM,min}$, $D_{DIM,on}$ and $D_{DIM,off}$ parameter values can be defined respectively according to the desired dimmer voltage for minimum output current $V_{DIM,min}$, the desired dimmer voltage for exiting dim-to-off $V_{DIM,on}$ and the desired dimmer voltage for entering dim-to-off $V_{DIM,off}$.

Taking $V_{DIM,min}$ = 1.88 V, $V_{DIM,on}$ = 1.53 V and $V_{DIM,off}$ = 1.44 V, parameter values of **$D_{DIM,min}$ = 15 percent**, **$D_{DIM,on}$ = 11 percent**, and **$D_{DIM,off}$ = 10 percent** are selected in this design example.

To achieve good light quality, PWM duty-cycle jittering is suppressed by configuring the PWM duty hysteresis parameter **$PWM_{Duty,hyst}$ = 0.1 percent**.

4 Transformer design

To achieve both high efficiency and high power quality in QR mode with first valley switching (QRM1), the Flyback transformer primary main winding to secondary main winding turns ratio, N, should be high enough, but without exceeding the Flyback MOSFET drain-source breakdown voltage $V_{(BR)DSS}$. Based on the $V_{AC,max}$ requirement of 305 V_{rms}, MOSFET **$V_{(BR)DSS}$ = 800 V** is selected for a good price-to-performance ratio.

To reduce transformer leakage inductance for low MOSFET voltage spike $V_{spike,FET}$, transformer design with sandwich construction as shown in **Figure 11** is recommended. Additionally, with the primary RCD snubber network deployed across the primary main winding (see **Figure 1**), $V_{spike,FET}$ can be estimated to be around 30 percent to 45 percent of $V_{AC,max}$ as a rule of thumb. In this design example, $V_{AC,max}$ is 305 V_{rms}, so we simply assume $V_{spike,FET}$ as an absolute number of 100 V, which is approximately 33 percent of $V_{AC,max}$.

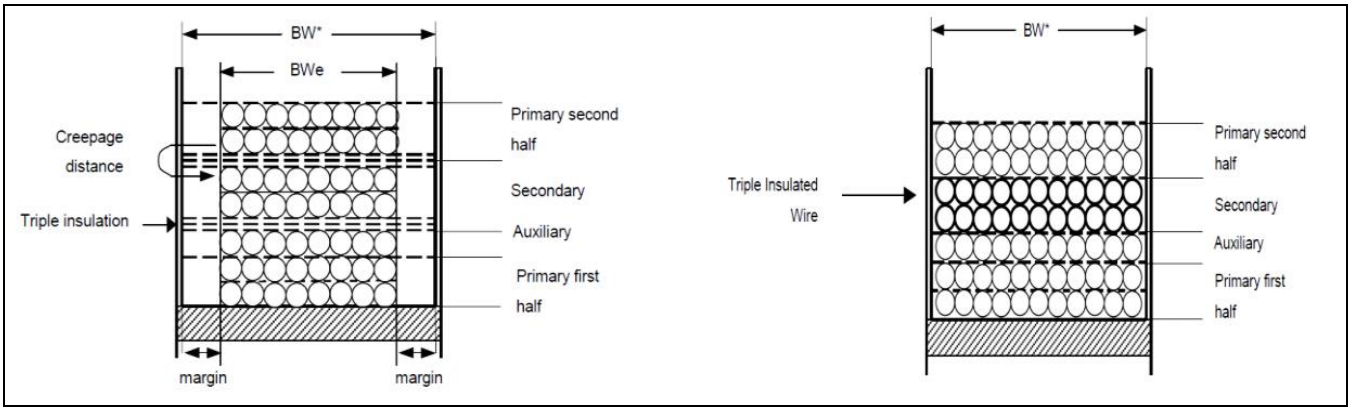


Figure 11 Transformer design with sandwich construction

For good reliability against input voltage surge and output open-load condition, it is recommended to reserve a voltage margin $V_{margin,FET}$ of minimum 50 V from $V_{(BR)DSS}$. If XDPL8210 input Over-Voltage Protection (OVP) would be enabled later in **Section 12**, as a rule of thumb, $V_{margin,FET}$ should be at least 25 percent of $V_{AC,max}$, which is equivalent to 76.25 V based on $V_{AC,max}$ of 305 V_{rms}. In this design example, $V_{margin,FET}$ of 80 V is selected.

Based on the above, N can be defined as:

$$N \leq \frac{V_{(BR)DSS} - V_{AC,max(pk)} - V_{spike,FET} - V_{margin,FET}}{V_{LED,max} + V_d} \quad (1)$$

Where $V_{AC,max(pk)}$ is √2 times $V_{AC,max}$, and V_d is the secondary main output diode forward voltage.

Taking V_d = 0.7 V, N can then be calculated as:

$$N \leq \frac{800 - \sqrt{2} \cdot 305 - 100 - 80}{54 + 0.7} = 3.46$$

Based on the above, **N = 3.4** is selected.

The maximum primary peak current $I_{pri(pk),max}$ is reached at the LED load voltage of $V_{LED,at,I,pri(pk),max}$.

$I_{pri(pk),max}$ and $V_{LED,at,I,pri(pk),max}$ can be defined and calculated as:

$$V_{LED,at,I,pri(pk),max} = \frac{P_{out,full}}{I_{out,full}} = \frac{35}{0.83} = 42.17\ V \quad (2)$$

$$I_{pri(pk),max} \approx \frac{4 \cdot P_{out,full}}{\eta_{min,at,P,out,full}} \cdot \left[\frac{1}{N \cdot (V_{LED,at,I,pri(pk),max} + V_d)} + \frac{1}{V_{AC,min(pk)}}\right] \quad (3)$$

Where $V_{AC,min(pk)}$ is √2 times $V_{AC,min}$.

$$I_{pri(pk),max} \approx \frac{4 \cdot 35}{90\%} \cdot \left[\frac{1}{3.4 \cdot (42.17 + 0.7)} + \frac{1}{\sqrt{2} \cdot 90}\right]$$

$$\boldsymbol{I_{pri(pk),max} \approx 2.289\ A}$$

As a result, the primary main winding inductance L_p can be defined and calculated as:

$$L_p = \frac{V_{AC,min(pk)} \cdot N \cdot (V_{LED,at,I,pri(pk),max} + V_d)}{I_{pri(pk),max} \cdot f_{sw,min,at,P,out,full} \cdot [V_{AC,min(pk)} + N \cdot (V_{LED,at,I,pri(pk),max} + V_d)]} \quad (4)$$

$$L_p = \frac{\sqrt{2} \cdot 90 \cdot 3.4 \cdot (42.17 + 0.7)}{2.289 \cdot 52.5 \cdot 10^3 \cdot [\sqrt{2} \cdot 90 + 3.4 \cdot (42.17 + 0.7)]}$$

$$\boldsymbol{L_p = 566\ \mu H}$$

Based on core cross-sectional area, A_e = 62 mm^2 and saturation flux density at 100°C, $B_{sat(T=100°C)}$ = 0.41. Tesla for TDG PQ20/20 core with TPW33 material, the transformer primary main winding turns N_p can be defined as:

$$N_p \geq \frac{L_p \cdot I_{pri(pk),max}}{A_e \cdot B_{sat(T=100°C)} \cdot D_{f,Bsat}} \quad (5)$$

Where $D_{f,Bsat}$ is the derating factor to ensure the designed transformer maximum flux density B_{max} is below $B_{sat(T=100°C)}$ by a margin of (100 percent - $D_{f,Bsat}$) from saturation, and it is typical to set $D_{f,Bsat}$ in the range of 85 percent to 95 percent for a margin of 5 percent to 15 percent from transformer core saturation.

Taking $D_{f,Bsat}$ = 88 percent, N_p can then be calculated as:

$$N_p \geq \frac{566 \cdot 10^{-6} \cdot 2.289}{62 \cdot 10^{-6} \cdot 0.41 \cdot 88\%} = 57.9$$

Based on the above, **N_p = 58** is selected.

The transformer secondary main winding turns N_s can then be calculated as:

$$N_s = \frac{N_p}{N} = \frac{58}{3.4}$$

$$\boldsymbol{N_s = 17}$$

To ensure fast XDPL8210 V_{CC} supply takeover from the primary auxiliary winding for avoiding IC reset during start-up, and also to be able to deliver peak gate-drive voltage $V_{GD,peak}$ of 10 V with high enough primary auxiliary winding V_{CC} supply during steady-state, the minimum primary auxiliary winding demagnetization voltage $V_{a,min}$ is therefore defined as 12 V. As a result, the recommended minimum primary auxiliary winding turns $N_{a,min}$ can be defined and calculated as:

$$N_{a,min} = \frac{V_{a,min} \cdot N_s}{(V_{LED,min,fully-dimmed} + V_d)} = \frac{12 \cdot 17}{(13 + 0.7)} = 14.89 \quad (6)$$

Based on the above, **N_a = 15** is selected.

A secondary auxiliary winding is added to supply CDM10VD operating voltage. The recommended minimum secondary auxiliary winding turns $N_{a,sec,min}$ can be defined based on $N_{a,min}$, as shown below:

$$N_{a,sec,min} = N_{a,min} = 14.89 \quad (7)$$

Based on the above, **$N_{a,sec}$ = 15** is selected.

5 Flyback MOSFET and secondary main output diode selection

The CoolMOS™ P7 MOSFET series is the latest CoolMOS™ product family and targets customers looking for high performance and at the same time being price sensitive. Through optimizing key parameters (C_{oss}, E_{oss}, Q_g, C_{iss} and $V_{GS(th)}$) and integrating a Zener diode for ESD protection and other measures, this product family fully addresses market concerns in performance, ease-of-use, and price/performance ratio, delivering best-in-class performance with exceptional ease-of-use, while still not compromising on price/performance ratio. The 700 V and 800 V CoolMOS™ P7 series have been designed for Flyback and could also be used in Power Factor Correction (PFC) topologies.

MOSFET drain-source breakdown voltage **$V_{(BR)DSS}$ = 800 V** is selected in this design example based on $V_{AC,max}$ of 305 V_{rms} and transformer design in **Section 4**.

Before selecting which MOSFET drain-source on-resistance at room temperature $R_{ds(on),25°C}$ is to be used, the maximum primary rms current $I_{pri(rms),max}$ has to be estimated based on:

$$I_{pri(rms),max} \approx I_{pri(pk),max} \cdot \sqrt{\frac{k}{3}} \quad (8)$$

Where k is a number obtained from the function curve in **Figure 12**, based on the variable factor of $\frac{V_{AC,min(pk)}}{N \cdot (V_{LED,at,I,pri(pk),max} + V_d)}$.

In this design example, the variable factor of $\frac{V_{AC,min(pk)}}{N \cdot (V_{LED,at,I,pri(pk),max} + V_d)}$ can be calculated as:

$$\frac{V_{AC,min(pk)}}{N \cdot (V_{LED,at,I,pri(pk),max} + V_d)} = \frac{\sqrt{2} \cdot 90}{3.4 \cdot (42.17 + 0.7)} = 0.873$$

Referring to the function curve in **Figure 12**, k = 0.29 is obtained.

Based on equation (8), $I_{pri(rms),max}$ can then be calculated as:

$$I_{pri(rms),max} \approx 2.289 \cdot \sqrt{\frac{0.29}{3}}$$

$$\boldsymbol{I_{pri(rms),max} \approx 0.712\ A}$$

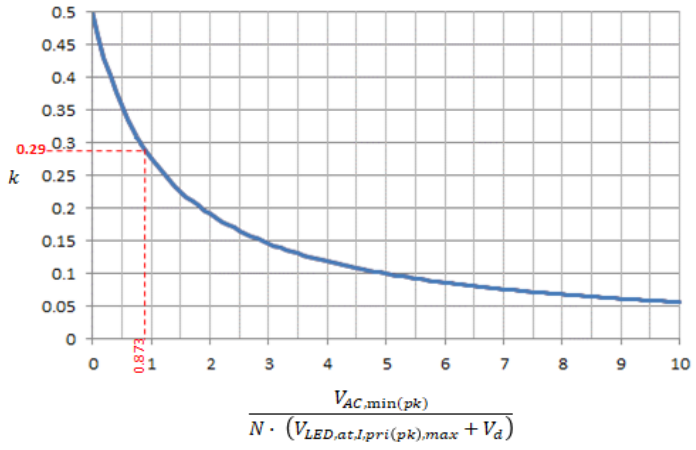


Figure 12 Function curve of k

The selectable MOSFET $R_{ds(on),25°C}$ can be defined as:

$$R_{ds(on),25°C} \leq \frac{m \cdot P_{out,full}}{I_{pri(rms),max}^{2} \cdot \Delta R_{ds(on),100°C}} \quad (9)$$

Where m is the desired ratio of MOSFET conduction loss over $P_{out,full}$ and $\Delta R_{ds(on),100°C}$ is the ratio of $\frac{R_{ds(on),100°C}}{R_{ds(on),25°C}}$.

It is typical to select m in the range of 0.025 to 0.03 and $\Delta R_{ds(on),100°C}$ in the range of 1.75 to 1.85. Taking m = 0.025 and $\Delta R_{ds(on),100°C}$ = 1.8, $R_{ds(on),25°C}$ can then be calculated as:

$$R_{ds(on),25°C} \leq \frac{0.025 \cdot 35}{0.712^{2} \cdot 1.8} = 0.96\ \Omega$$

Referring to the calculation results of equation (9) and **Table 3** below, **$R_{ds(on),25°C}$ = 900 mΩ** is selected.

To utilize the PCB as a heatsink for the MOSFET, **IPN80R900P7** with SOT-223 package is selected from **Table 3**.

Table 3 800 V CoolMOS™ P7 selection table

$R_{DS(on)}$ [mΩ]	TO -220	TO-220 FullPAK	TO-247	TO-252 (DPAK)	TO-251 (IPAK)	TO-251 (IPAK Short Lead)	SOT-223	TO-220 FullPAK narrow lead	ThinPAK 5x6
280	IPP80R280P7	IPA80R280P7	IPW80R280P7	IPD80R280P7				IPAN80R280P7	
360	IPP80R360P7	IPA80R360P7	IPW80R360P7	IPD80R360P7				IPAN80R360P7	
450	IPP80R450P7	IPA80R450P7		IPD80R450P7				IPAN80R450P7	
600	IPP80R600P7	IPA80R600P7		IPD80R600P7	IPU80R600P7	IPS80R600P7	IPN80R600P7		IPLK80R600P7
750	IPP80R750P7	IPA80R750P7		IPD80R750P7	IPU80R750P7	IPS80R750P7	IPN80R750P7		IPLK80R750P7
900	IPP80R900P7	IPA80R900P7		IPD80R900P7	IPU80R900P7	IPS80R900P7	IPN80R900P7		IPLK80R900P7
1200	IPP80R1K2P7	IPA80R1K2P7		IPD80R1K2P7	IPU80R1K2P7	IPS80R1K2P7	IPN80R1K2P7		IPLK80R1K2P7
1400	IPP80R1K4P7	IPA80R1K4P7		IPD80R1K4P7	IPU80R1K4P7	IPS80R1K4P7	IPN80R1K4P7		IPLK80R1K4P7
2000				IPD80R2K0P7	IPU80R2K0P7	IPS80R2K0P7	IPN80R2K0P7		IPLK80R2K0P7
2400				IPD80R2K4P7	IPU80R2K4P7	IPS80R2K4P7	IPN80R2K4P7		
3300				IPD80R3K3P7	IPU80R3K3P7		IPN80R3K3P7		
4500				IPD80R4K5P7	IPU80R4K5P7		IPN80R4K5P7		

For the secondary main output diode selection, it is necessary to first estimate the maximum reverse voltage $V_{r(diode),max}$ and maximum secondary main winding peak current $I_{sec(pk),max}$, based on:

$$V_{r(diode),max} = V_{spike,diode} + V_{LED,max} + \frac{V_{AC,max(pk)} + V_{margin,FET}}{N} \quad (10)$$

Where $V_{spike,diode}$ is the diode reverse voltage spike.

Assuming $V_{spike,diode} \approx 35\% \cdot \left(V_{LED,max} + \frac{V_{AC,max(pk)} + V_{margin,FET}}{N}\right)$,

$$V_{r(diode),max} \approx 135\% \cdot \left(V_{LED,max} + \frac{V_{AC,max(pk)} + V_{margin,FET}}{N}\right) = 135\% \cdot \left(54 + \frac{\sqrt{2} \cdot 305 + 80}{3.4}\right)$$

$$V_{r(diode),max} \approx 275.9\ V$$

$$I_{sec(pk),max} \approx I_{pri(pk),max} \cdot \frac{N_p}{N_s} = 2.289 \cdot \frac{58}{17} \quad (11)$$

$$I_{sec(pk),max} \approx 7.81\ A$$

Based on the above, a secondary main output diode with repetitive reverse voltage rating **V_{RRM} = 300 V** is selected. To minimize its switching and conduction losses, the selected diode also has the properties of hyper-fast recovery speed and low forward voltage drop at $I_{sec(pk),max}$.

If necessary, a RC secondary snubber network, e.g. 10 Ω resistor in series with 150 pF capacitor, can be deployed across the secondary main output diode, to suppress the diode reverse voltage spike and the EMI.

6 CS resistor and GD pin-related design

Figure 13 shows the connections of the CS resistor R_{CS}, gate resistor R_G and gate-source resistor R_{GS}.

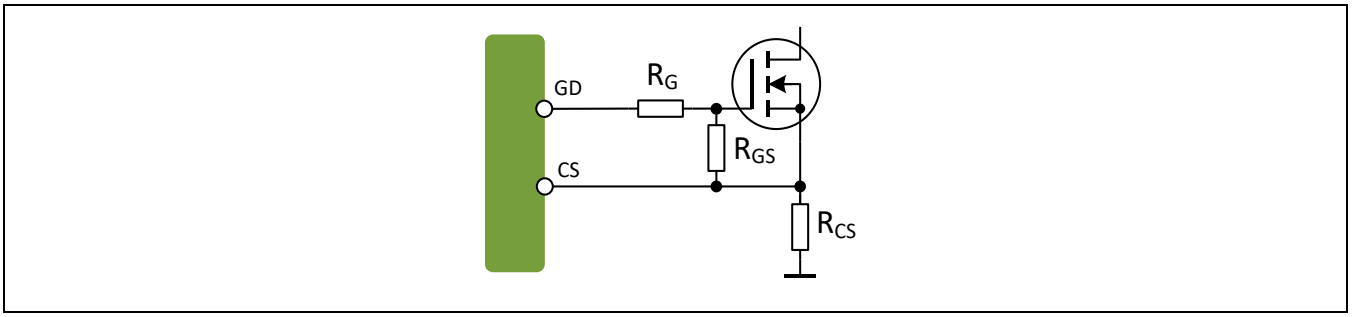


Figure 13 GD pin, CS pin, R_{CS}, R_G and R_{GS} connections

Based on the CS pin voltage across R_{CS}, the MOSFET current can be measured.

The recommended minimum CS resistor value $R_{CS,min}$ is defined and calculated as:

$$R_{CS,min} = \frac{0.45}{I_{pri(pk),max}} = \frac{0.45}{2.289} = 0.197\ \Omega \quad (12)$$

The recommended maximum CS resistor value $R_{CS,max}$ is defined and calculated as:

$$R_{CS,max} = \frac{0.54}{I_{pri(pk),max}} = \frac{0.54}{2.289} = 0.236\ \Omega \quad (13)$$

Based on the calculation results above, CS resistor **R_{CS} = 0.22 Ω** is selected in this design example.

R_G is to damp the gate-rise oscillaton, and R_{GS} is to ensure the MOSFET remains in an off-state when AC input is applied, with the IC not being activated yet. **R_G = 10 Ω** and **R_{GS} = 20 kΩ** are selected in this design example.

The gate-drive peak voltage $V_{GD,pk}$ is typically 12 V with sufficient V_{CC} voltage supply. To achieve a good balance of switching loss and EMI, the gate voltage rising slope can be controlled by configuring the gate-driver peak-source current parameter $I_{GD,pk}$ (configurable range: 30 mA to 180 mA). This saves two components (see $D_{fastoff}$, R_{slowon} in **Figure 14**), which are conventionally added for the same purpose.

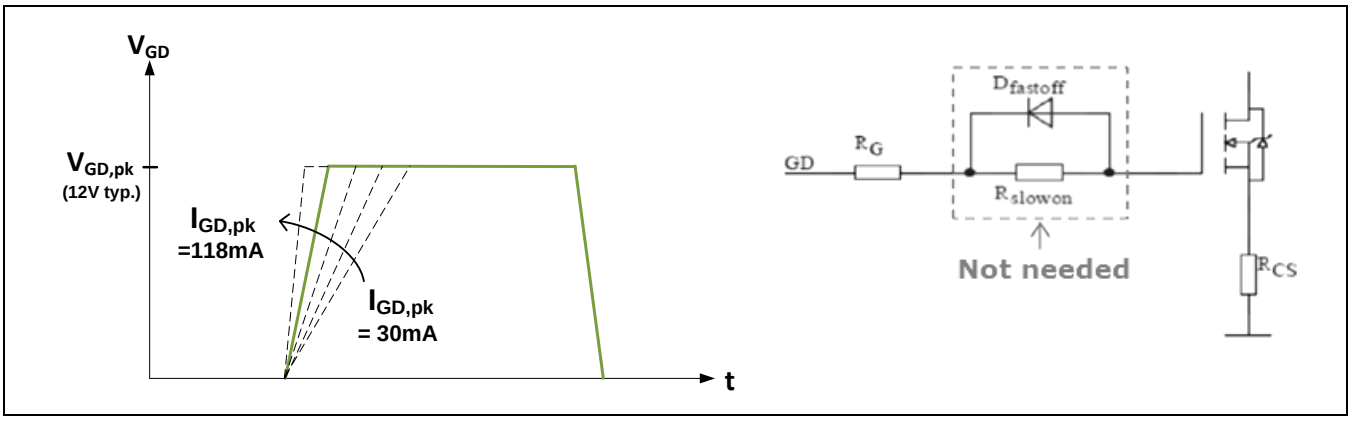


Figure 14 Gate-drive voltage rising slope control with $I_{GD,pk}$ parameterization for component saving

With the high-speed switching characteristics of the CoolMOS™ P7 MOSFET, it is recommended to configure the $I_{GD,pk}$ parameter in the range of 30 mA to 49 mA.

As a result, **$I_{GD,pk}$ = 30 mA** is selected in this design example.

7 MOSFET maximum current cycle-by-cycle limit and start-up phase design

To avoid transformer core saturation, XDPL8210 regulated mode features the CS pin voltage level 1 for MOSFET maximum current cycle-by-cycle limit V_{OCP1}.

*Note: Regulated mode is a controller operating state, which is entered after the start-up phase, to regulate the output current based on the target set-point (see **Figure 15**).*

$$V_{OCP1} = I_{pri(pk),max} \cdot R_{CS} \quad (14)$$

$$V_{OCP1} = 2.289 \cdot 0.22$$

$$\boldsymbol{V_{OCP1} = 0.50\ V}$$

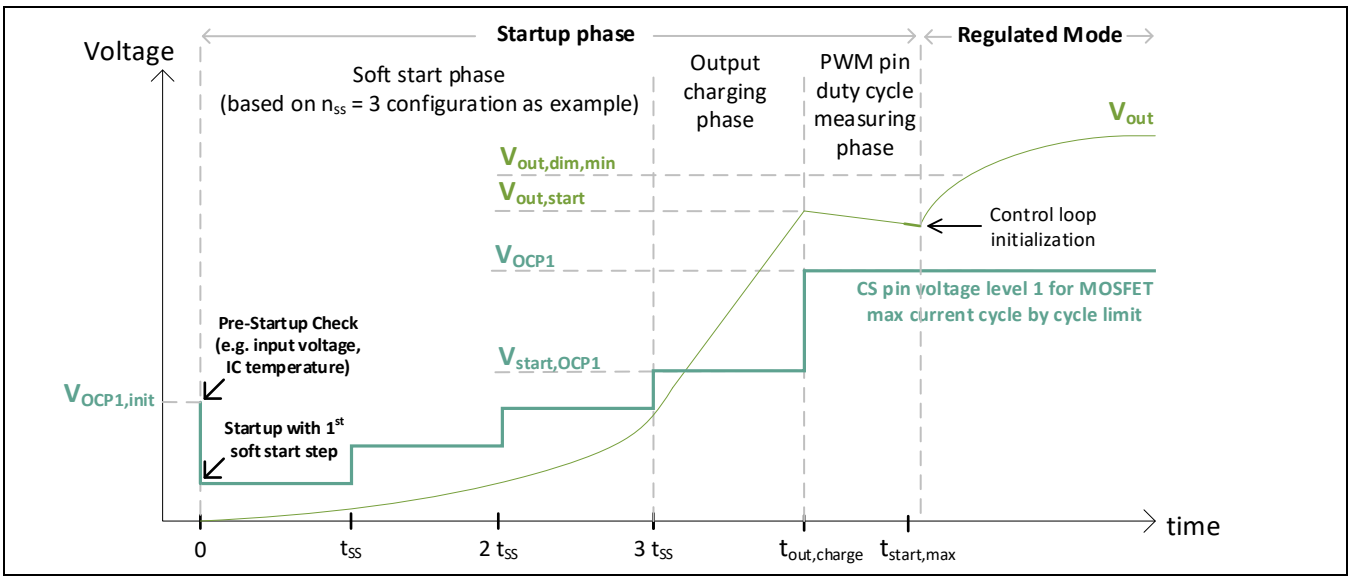


Figure 15 Start-up phase with soft-start step n_{ss} = 3

Pre-start-up check ensures the estimated input voltage V_{in} and IC junction temperature T_j are within the configured protection limits before start-up, as shown in **Figure 15**. The parameter configurations of the input voltage levels and maximum T_j for start-up are covered in **Section 12** and **Section 16.2** respectively.

The $V_{OCP1,init}$ parameter in **Figure 15** denotes the initial CS pin voltage level 1 for MOSFET current limit on the input voltage measurement pulse, during pre-start-up check. It can be defined and calculated as:

$$V_{OCP1,init} = Max\left\{\frac{a \cdot R_{CS} \cdot V_{AC,max(pk)} \cdot t_{on,min,V,in,start,sense}}{L_p},\ 0.3\right\} \quad (15)$$

Where $V_{AC,max(pk)}$ is √2 times $V_{AC,max}$, $t_{on,min,V,in,start,sense}$ is the minimum on-time for the pre-start-up input voltage measurement pulse and a is the ratio recommended to be between 1.2 and 1.3.

Take $t_{on,min,V,in,start,sense}$ = 1.38 µs, and a = 1.3,

$$V_{OCP1,init} = Max\left\{\frac{1.3 \cdot 0.22 \cdot \sqrt{2} \cdot 305 \cdot 1.38 \cdot 10^{-6}}{566 \cdot 10^{-6}}, 0.3\right\}$$

$$\boldsymbol{V_{OCP1,init} = 0.3\ V}$$

Note: A typical leading-edge blanking time $t_{CS,LEB}$ of 480 ns applies on V_{OCP1}, $V_{OCP1,init}$ and $V_{start,OCP1}$.

The start-up phase consists of the soft-start phase, output charging phase and PWM duty-cycle measuring phase.

The soft-start phase is to minimize the component stress during start-up. The output charging phase is to fast-charge the output voltage for fast V_{CC} voltage self-supply takeover from the primary auxiliary winding, while the PWM duty-cycle measuring phase is to determine the regulated mode output current set-point.

During the soft-start phase, the switching frequency is fixed at 26.9 kHz. The MOSFET current is limited in the first soft-start step based on CS pin maximum voltage limit of $V_{start,OCP1}/(n_{ss} + 1)$, where $V_{start,OCP1}$ is the parameter for the output charging phase CS pin maximum voltage limit and n_{ss} is the parameter for the number of soft-start steps. The soft-start phase CS pin maximum voltage limit is increased by $V_{start,OCP1}/(n_{ss} + 1)$ after each soft-start step until $V_{start,OCP1}$ is reached, and the typical duration of each soft-start step t_{ss} is $3.2/n_{ss}$ ms or 0.5 ms, whichever is lower.

It is recommended to configure the n_{ss} parameter with a higher value, so that during dim-to-off operation, the secondary main output voltage charging is minimized to keep the LEDs in the off-state, by transferring most of the soft-start phase transformer demagnetization energy to the secondary auxiliary winding output for supplying the CDM10VD operating voltage. Therefore, in this design example, **n_{ss} = 20** parameter setting is selected, which results in t_{ss} of 3.2/20 = 0.16 ms.

To ensure fast V_{CC} self-supply takeover from the primary auxiliary winding, the $V_{start,OCP1}$ parameter is recommended to be configured as per V_{OCP1}. Hence, **$V_{start,OCP1}$ = 0.50 V** parameter setting is selected in this design example.

During the output charging phase, the output voltage is fast-charged with MOSFET switching pulses based on either the output charging phase CS pin maximum voltage limit of $V_{start,OCP1}$ or the maximum on-time of $t_{on,max}$ in QRM1.

In this design example, the fully dimmed condition refers to the dim-to-off condition, so $V_{LED,min,fully\text{-}dimmed}$ = 13 V from **Table 2** can also denote the minimum LED turn-on threshold. To ensure no flicker during start-up and no light during dim-to-off, $V_{out,start}$ should be below $V_{LED,min,fully\text{-}dimmed}$ by sufficient margin. Therefore, $V_{out,start}$ can be defined and calculated as:

$$V_{out,start} = b \cdot V_{LED,min,fully-dimmed} \quad (16)$$

Where b is the ratio, which is recommended to be between 0.8 and 0.85.

Taking b = 0.81,

$$V_{out,start} = 0.81 \cdot 13$$

$$\boldsymbol{V_{out,start} = 10.5\ V}$$

For proper start-up without triggering the start-up output Under-Voltage Protection (UVP) as shown in **Figure 15**, the ZCD pin estimated output voltage V_{out} has to reach the output charging voltage set-point parameter $V_{out,start}$ before the maximum allowable start-up phase duration of $t_{start,max}$ is reached (see **Section 10** for details).

8 HV pin-related design

As shown in **Figure 16**, HV series resistor R_{HV} is connected from the HV pin to the cathodes of HV diode D_{HV1} and D_{HV2}, while bridge rectifier AC input should be applied across the D_{HV1} anode and D_{HV2} anode.

Additionally, a HV capacitor C_{HV} should also be connected between the HV pin and ground.

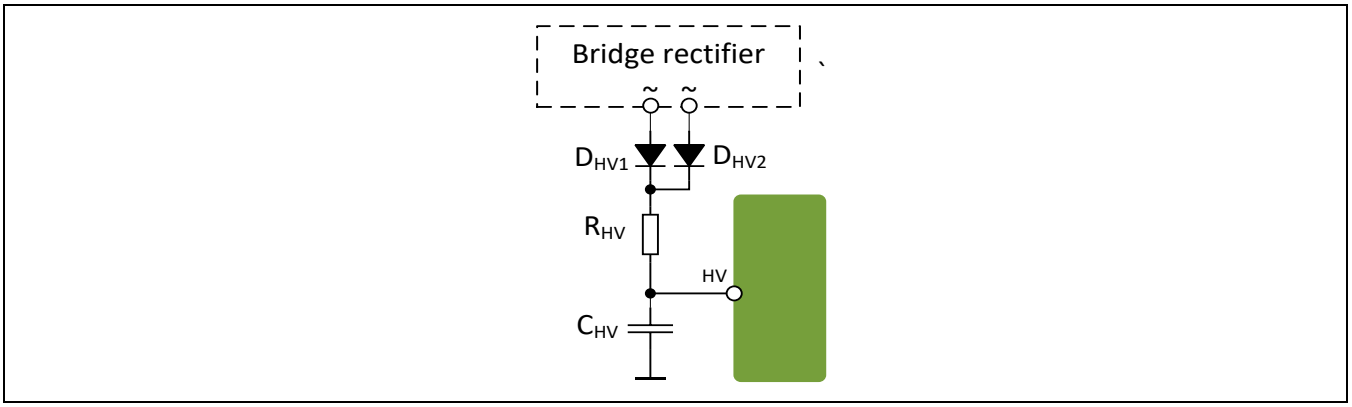


Figure 16 HV pin, R_{HV}, C_{HV}, D_{HV1} and D_{HV2} connections

The recommended minimum HV series resistor value $R_{HV,min}$ is defined and calculated as:

$$R_{HV,min} = \frac{d \cdot V_{AC,max(pk)}}{I_{HV,max}} \quad (17)$$

Where $V_{AC,max(pk)}$ is √2 times $V_{AC,max}$, $I_{HV,max}$ is the HV pin maximum peak input current of 9.6 mA, and d is the ratio recommended to be between 1.05 and 1.1.

Taking d = 1.075,

$$R_{HV,min} = \frac{1.075 \cdot \sqrt{2} \cdot 305}{9.6 \cdot 10^{-3}} = 48.3\ k\Omega$$

The recommended maximum HV series resistor value $R_{HV,max}$ is defined and calculated as:

$$R_{HV,max} = \frac{V_{AC,min(rect,avg)} - V_{VCCON,max}}{I_{HV,min(avg)}} \cdot \left[1 - \frac{2}{\pi} \cdot sin^{-1}\left(\frac{V_{VCCON,max}}{V_{AC,min(pk)}}\right)\right] \quad (18)$$

Where $V_{AC,min(rect,avg)}$ is the average value of the rectified $V_{AC,min}$, while $V_{VCCON,max}$ is the maximum V_{CC} turn-on voltage threshold of 22 V, and $I_{HV,min(avg)}$ is the recommended HV pin minimum average input current of 1 mA.

$$R_{HV,max} = \frac{0.9 \cdot 90 - 22}{1 \cdot 10^{-3}} \cdot \left[1 - \frac{2}{\pi} \cdot sin^{-1}\left(\frac{22}{\sqrt{2} \cdot 90}\right)\right]$$

$$R_{HV,max} = 52.5\ k\Omega$$

Based on the above, **R_{HV} = 52 kΩ** is selected in this design example.

The HV series resistor dielectric withstand voltage should be above the total of $V_{AC,max(pk)}$ and $V_{margin,FET}$ (see **Section 4** for their respective values), which is equivalent to 511.3 V. As an example, the selected R_{HV} = 52 kΩ in this design example can be formed using three resistors in series, with the power rating of 0.25 W and dielectric withstand rating of 200 V for each resistor.

For better line synchronization stability against noise interference, C_{HV} shown in **Figure 16** is needed. In addition, C_{HV} also improves the surge and ESD capability of the HV pin.

C_{HV} = 1 nF is recommended and selected in this design example.

9 DC-link filter and secondary main output capacitance

$C_{DC,filter}$ denotes the DC-link filter capacitor placed after the bridge rectifier. A higher $C_{DC,filter}$ value gives lower EMI but worse power quality, and vice versa.

Table 4 Recommended initial $C_{DC,filter}$ value

$V_{AC,min}$ (V)	Steady-state full-load output power $P_{out,full}$ (W)	Recommended initial $C_{DC,filter}$ (μF)
90 ~ 107	Less than 26	0.1
	26 ~ 35	0.15
	35 ~ 44	0.22
	Greater than 45	Greater than 0.22
Greater than or equal to 108	Less than 31	0.1
	31 ~ 40	0.15
	40 ~ 55	0.22
	Greater than 55	Greater than 0.22

Referring to **Table 4**, initial $C_{DC,filter}$ value of 0.15 μF or 0.22 μF can be selected. In this design example, **initial $C_{DC,filter}$ = 0.22 μF** is selected. To improve the estimated input voltage V_{in} accuracy during pre-start-up check, it is also recommended to deploy a high-ohmic DC-link resistor in parallel with $C_{DC,filter}$, as shown in **Figure 17**.

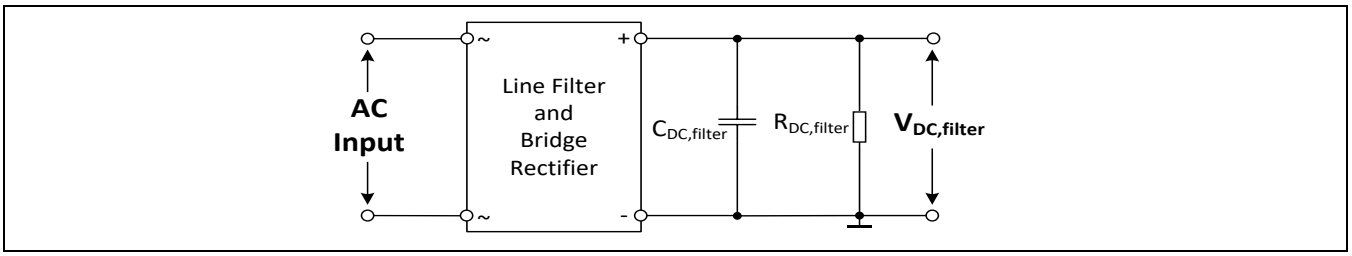


Figure 17 $C_{DC,filter}$ and $R_{DC,filter}$ across the DC-link bus voltage

To compensate for the input current displacement caused by the $C_{DC,filter}$, the XDPL8210 enhanced PFC feature can be enabled by configuration of the compensation gain parameter named C_{EMI}. As a start, it can be configured as per the $C_{DC,filter}$ value. Hence, the **initial C_{EMI} = 0.22 μF** parameter setting is selected in this design example. Upon successful powering-up of the sytem, refer to **Section 19.4** for the fine-tuning guide.

The secondary main output capacitor C_{out} value can be defined and calculated as:

$$C_{out} \geq \frac{\sqrt{\left(\frac{I_{out,full}}{\Delta I_{out}}\right)^2 - 1}}{4 \cdot \pi \cdot F_{line} \cdot R_{d,min}} \quad (19)$$

Where ΔI_{out} is the maximum output ripple current and $R_{d,min}$ is the minimum LED dynamic resistance at $I_{out,full}$. In this design example, $V_{LED,min,non\text{-}dimmed}$ is 18 V, which is normally formed by six LEDs in series. Assuming each LED has a dynamic resistance at $I_{out,full}$ of 1 Ω, then $R_{d,min}$ is 6 Ω.

Taking F_{line} = 50 Hz and ΔI_{out} = 0.249 A (equivalent to 30 percent of $I_{out,full}$), C_{out} can then be calculated as:

$$C_{out} \geq \frac{\sqrt{\left(\frac{0.83}{0.249}\right)^2 - 1}}{4 \cdot \pi \cdot 50 \cdot 6} = 843\ \mu F$$

Considering the electrolytic capacitance tolerance, **C_{out} = 940 μF** is selected in this design example. For lower EMI, low-ESR ceramic capacitors **$C_{out,lowESR1}$ = 1 μF** and **$C_{out,lowESR2}$ = 0.1 μF** are also added in parallel with C_{out}.

10 V_{CC} capacitance and output UVP design

To fulfill the Energy Star time-to-light requirement of 500 ms, the V_{CC} voltage maximum charging time for IC activation, $t_{VCCON,charge,max}$ is recommended to be 250 ms. Therefore, the maximum V_{CC} capacitance $C_{VCC,max}$ can be defined and calculated as:

$$C_{VCC,max} = \frac{V_{AC,120(rect,avg)} - V_{VCCON,max}}{R_{HV} \cdot V_{VCCON,max}} \cdot t_{VCCON,charge,max} \cdot \left[1 - \frac{2}{\pi} \cdot sin^{-1}\left(\frac{V_{VCCON,max}}{V_{AC,120(pk)}}\right)\right] \quad (20)$$

Where $V_{VCCON,max}$ is the maximum V_{CC} turn-on threshold of 22 V, $V_{AC,120(rect,avg)}$ is the average value of rectified 120 V_{rms} AC input, and $V_{AC,120(pk)}$ is the peak value of 120 V_{rms} AC input.

$$C_{VCC,max} = \frac{0.9 \cdot 120 - 22}{52 \cdot 10^3 \cdot 22} \cdot 250 \cdot 10^{-3} \cdot \left[1 - \frac{2}{\pi} \cdot sin^{-1}\left(\frac{22}{\sqrt{2} \cdot 120}\right)\right] = 17.23\ \mu F$$

The $t_{start,max}$ parameter refers to the maximum allowable duration of the start-up phase, which consists of the soft-start phase and output charging phase. It can be indirectly configured with V_{CC} capacitance parameter C_{VCC}, based on:

$$t_{start,max} = \frac{0.8 \cdot C_{VCC} \cdot (V_{VCCON} - V_{UVOFF})}{I_{IC,avg,est}} = \frac{0.8 \cdot C_{VCC} \cdot (20.5 - 6)}{12 \cdot 10^{-3}} = 967 \cdot C_{VCC} \quad (21)$$

Where V_{VCCON} is the typical V_{CC} turn-on voltage threshold of 20.5 V, V_{UVOFF} is the typical V_{CC} turn-off voltage threshold of 6 V and $I_{IC,avg,est}$ is the estimated IC current consumption of 12 mA.

For proper start-up, as shown in **Figure 18 (left)**, C_{VCC} has to be high enough to ensure its corresponding $t_{start,max}$ calculated from equation (21) is longer than $t_{out,charge}$, which $t_{out,charge}$ is the time needed to charge the output voltage to the output charging phase voltage set-point $V_{out,,start}$.

Based on the considerations above, V_{CC} capacitor value and IC parameter setting of **C_{VCC} = 15 μF** is selected in this design example, which results in $t_{start,max}$ = 14.5 ms. In addition, a noise decoupling ceramic capacitor of **$C_{VCCdecouple}$ = 0.1 μF** with low ESR is added in parallel to C_{VCC}.

In the start-up phase, if the ZCD pin estimated output voltage V_{out} is lower than $V_{out,start}$ over a time-out period of $t_{start,max}$, the start-up output UVP is triggered. For instance, this could happen if the Flyback output is shorted during the start-up, as shown in **Figure 18 (right)**.

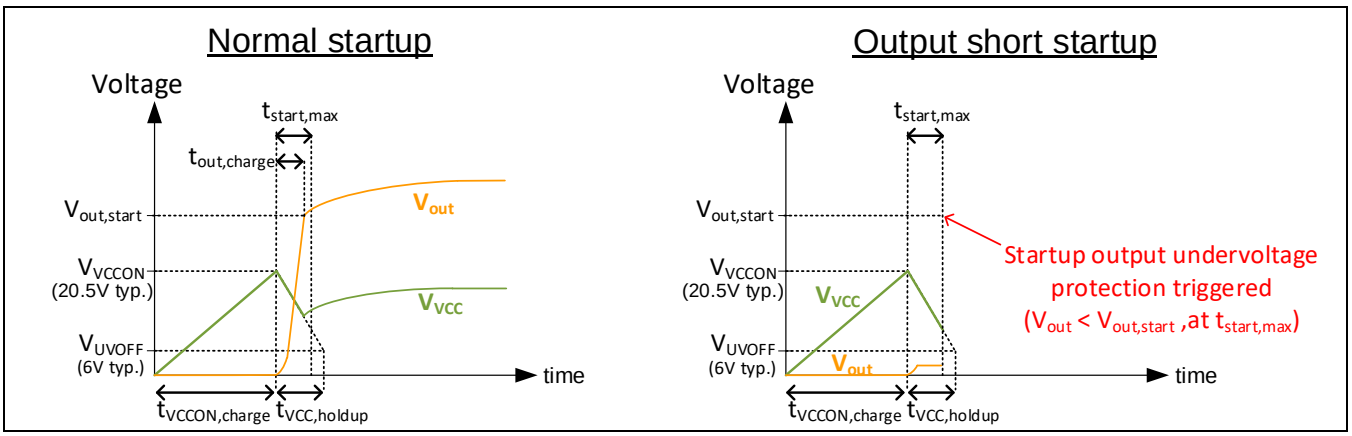


Figure 18 Normal start-up and start-up output UVP (short) waveforms

Additionally, the regulated mode output UVP can be triggered if the ZCD pin estimated output voltage V_{out} is below the regulated mode output UVP level V_{outUV} for longer than a blanking time of $t_{VoutUV,blank}$, as shown in **Figure 19**. $t_{VoutUV,blank}$ is recommended to be at least 40 ms. Hence, **$t_{VoutUV,blank}$ = 40 ms** is selected in this design example.

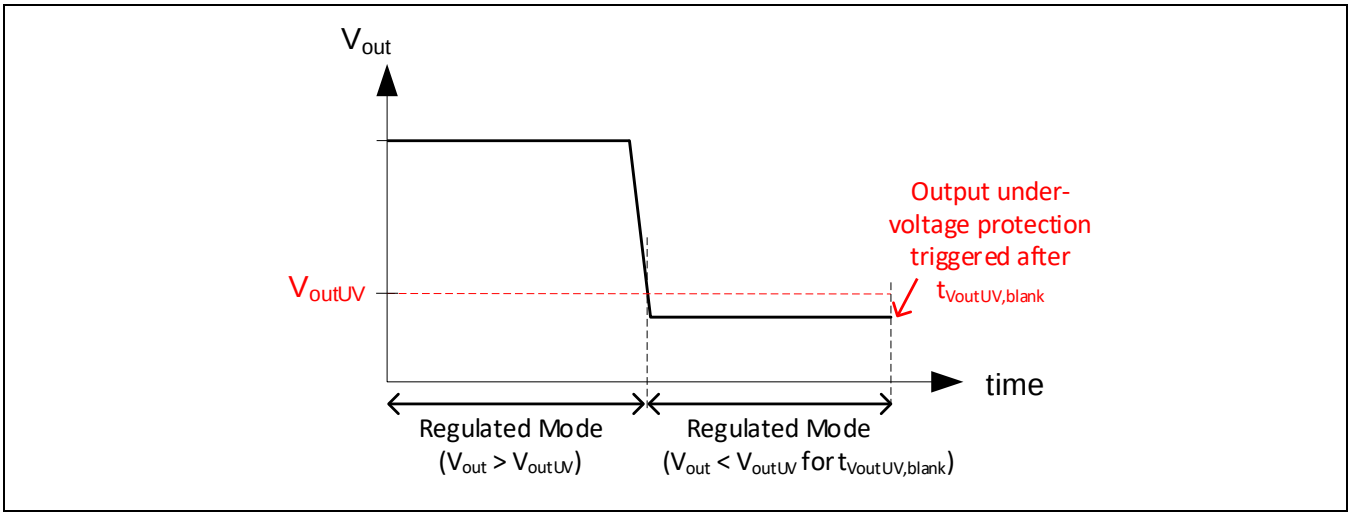


Figure 19 Regulated mode output UVP (based on ZCD pin voltage sensing)

V_{outUV} setting can be indirectly configured based on:

$$V_{outUV} = 0.5 \cdot V_{out,dm,min} \quad (22)$$

Where $V_{LED,min,fully\text{-}dimmed}$ is a configurable parameter which is recommended to be in the range of 90 percent to 100 percent of $V_{LED,min,fully\text{-}dimmed}$. Taking **$V_{out,dim,min}$ = 12 V** (which is 92 percent of $V_{LED,min,fully\text{-}dimmed}$) in this design example, the resulting V_{outUV} based on equation (22) would be 6 V.

The reaction of both start-up output UVP and regulated mode output UVP is fixed as auto-restart, and the auto-restart time is based on the $t_{auto,restart}$ parameter. **$t_{auto,restart}$ = 1.6 s** setting is selected in this design example. Please note that $t_{auto,restart}$ is a common auto-restart time used for other system protections with auto-restart reaction.

11 Output OVP-related and bleeder design

In case of output open, the output voltage may rise to a high level. The output OVP would be triggered when the ZCD pin estimated output voltage V_{out} is higher than the output OVP level V_{outOV} for longer than the blanking time.

In QRM1 and DCM, the blanking time is typically a quarter of the half-sine-wave period, e.g. 2.5 ms for F_{line} = 50 Hz with line synchronization established. In ABM, the blanking time is configurable based on the $t_{VoutOV,blank,ABM}$ parameter.

The V_{outOV} parameter can be defined and calculated as:

$$V_{outOV} \geq \frac{V_{LED,max}}{0.95} = \frac{54}{0.95} = 56.84\,V \quad (23)$$

Based on the above, **V_{outOV} = 56.9 V** setting is selected in this design example.

Considering the ZCD pin estimated output voltage protection accuracy is subject to the the sampled signal accuracy, sampling delay, indirect sensing delay (e.g. output voltage cannot be estimated near AC input phase angle of 0 degrees and 180 degrees) and blanking time, the output capacitor voltage rating $V_{out,cap,rating}$ should be selected well above V_{outOV}. As a result, $V_{out,cap,rating}$ can be defined and calculated as:

$$V_{out,cap,rating} \geq \frac{V_{outOV}}{0.85} = \frac{56.9}{0.85} = 66.9\,V \quad (24)$$

Based on the above, **$V_{out,cap,rating}$ = 80 V** setting is selected in this design example.

Attention: ***It is mandatory to ensure that V_{outOV} is configured well below the actual output capacitor voltage rating $V_{out,cap,rating}$, while the $V_{out,cap,rating}$ is not exceeded in actual testing with all the necessary test conditions.***

The reaction of output OVP is configurable to latch-mode or auto-restart, based on the $Reaction_{OVP,Vout}$ parameter. **$Reaction_{OVP,Vout}$ = Auto-Restart** setting is selected in this design example.

To have lower output open-load voltage during auto-restart, as shown in **Figure 20**, the adaptive output OVP can be enabled with the $EN_{adaptive,OVP,Vout}$ parameter. **$EN_{adaptive,OVP,Vout}$ = Enabled** setting is selected in this design example.

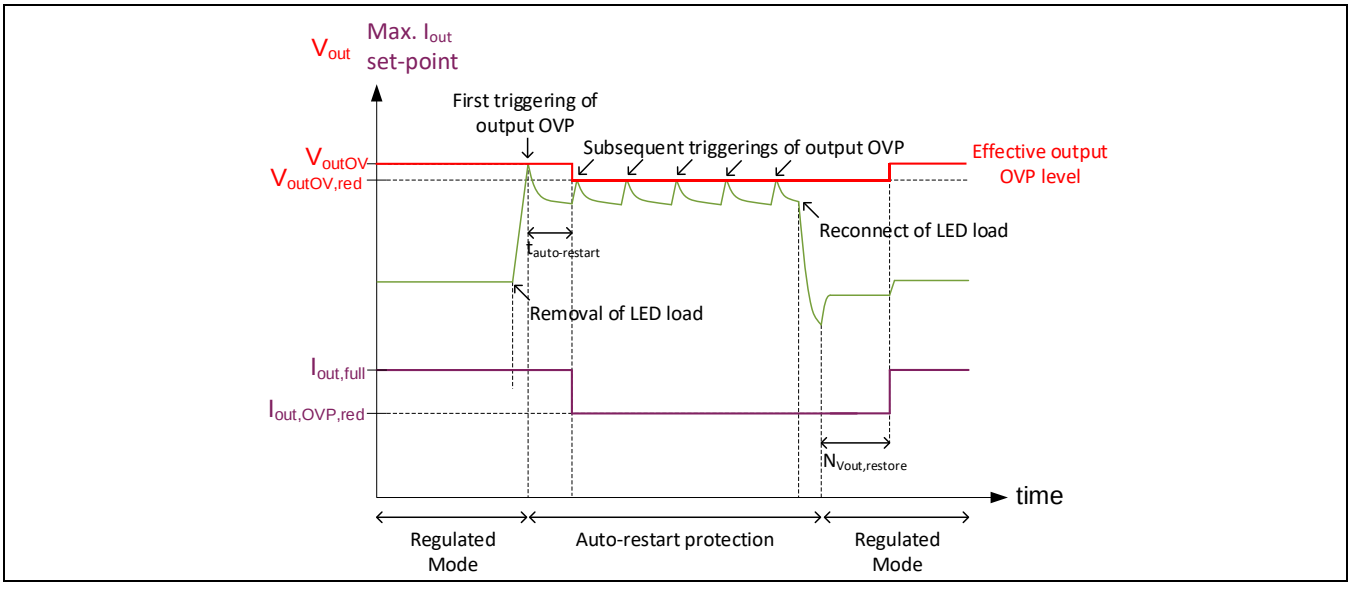


Figure 20 Output over-voltage protection and recovery waveform ($EN_{adaptive,OVP,Vout}$ = Enabled)

Upon triggering the enabled adaptive output OVP for the first time, the protection level is reduced from V_{outOV} to $V_{outOV,red}$ and the output current set-point maximum limit is reduced from $I_{out,full}$ to $I_{out,OVP,red}$. For a successful output recovery, the estimated output voltage V_{out} upon auto-restart has to be lower than $V_{outOV,red}$ for a number of half-sine-wave periods based on the $N_{Vout,restore}$ parameter, in order to restore the protection level and the output current set-point maximum limit to V_{outOV} and $I_{out,full}$, respectively.

$I_{out,OVP,red}$ can be defined and calculated as:

$$I_{out,OVP,red} \geq I_{out,dim,min} = 41.5\ mA \quad (25)$$

Based on the above, the **$I_{out,OVP,red}$ = 41.5 mA** setting is selected in this design example.

$V_{outOV,red}$ can be defined as:

$$V_{outOV,red} = \frac{V_{LED,max,at,I,out,OVP,red}}{0.95} \quad (26)$$

Where $V_{LED,max,at,I,out,OVP,red}$ denotes the steady-state maximum LED load voltage at $I_{out,OVP,red}$.

By estimating $V_{LED,max,at,I,out,OVP,red}$ equal to 90 percent of $V_{LED,max}$, which is 48.6 V based on this design example, $V_{outOV,red}$ can then be calculated as:

$$V_{outOV,red} = \frac{48.6}{0.95} = 51.2\ V$$

Based on the above, **$V_{outOV,red}$ = 51.2 V** setting is selected in this design example.

$N_{Vout,restore}$ can be defined and calculated as:

$$N_{Vout,restore} \geq \frac{4 \cdot F_{line,max} \cdot C_{out} \cdot (V_{LED,max,at,I,out,OVP,red} - V_{out,start})}{I_{out,OVP,red}} = \frac{4 \cdot 63 \cdot 940 \cdot 10^{-6}\ (51.2 - 10.5)}{41.5 \cdot 10^{-3}} = 232 \quad (27)$$

Based on the above, **$N_{Vout,restore}$ = 500** setting is selected in this design example.

If the adaptive output OVP is not desired, it can be disabled with the $EN_{adaptive,OVP,Vout}$ parameter, as shown in **Figure 21**.

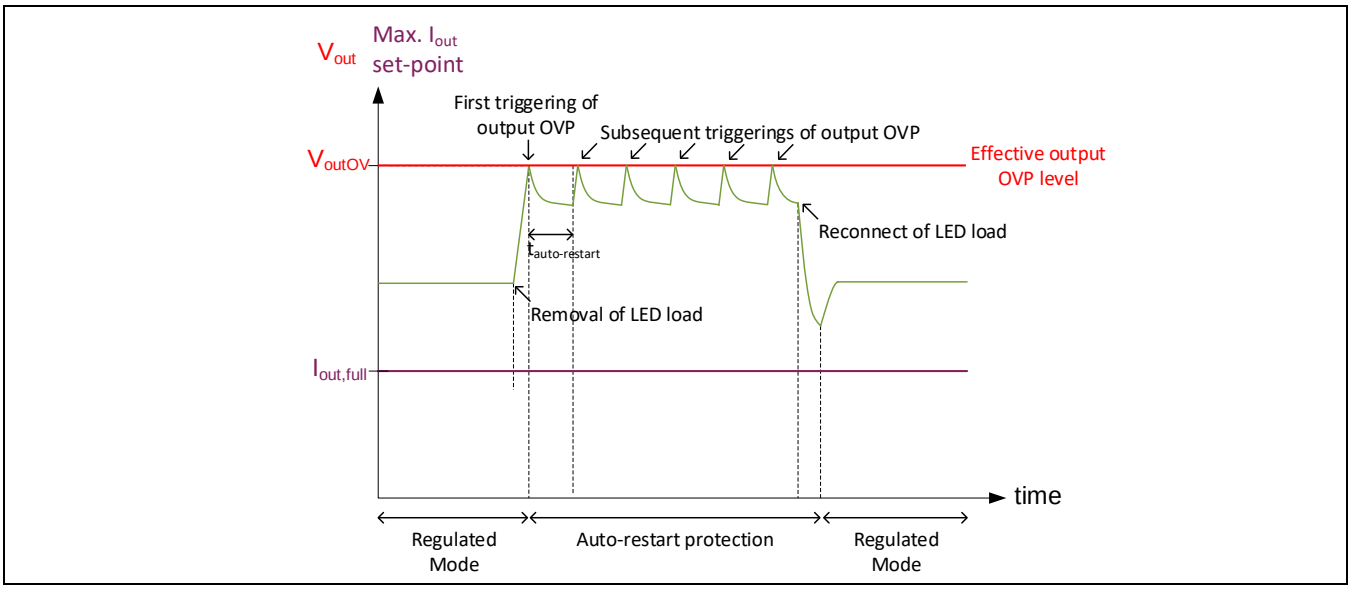


Figure 21 Output OVP and recovery waveform ($EN_{adaptive,OVP,Vout}$ = Disabled)

In this design example, despite the output OVP setting of V_{outOV} = 56.9 V, the actual output OVP level of first triggering could exceed 60 V, since the ZCD pin estimated output voltage protection accuracy is subject to the

sampled signal accuracy, sampling delay, indirect sensing delay (e.g. output voltage cannot be estimated near AC input phase angle of 0 degrees and 180 degrees) and blanking time. With the adaptive output OVP enabled and adaptive output OVP setting of $V_{outOV,red}$ = 51.2 V, the actual output OVP level of the subsequent triggerings can then be controlled to be less than 60 V.

To meet the safety standard UL1310 (Class 2), a single pulse exceeding 60 V on the output should be less than 200 ms. Therefore, an active bleeder is deployed in this design example (see **Figure 22**), so that the output voltage can be discharged quickly to less than 60 V after the first output OVP triggering.

When the Flyback converter is switching, C13, D9, D10 and C6 builds up Q4 gate voltage to ZD3 reverse voltage, so that Q4 is on and Q5 is off, to disable the bleeding. When the Flyback converter is not switching e.g. after first output OVP triggering, R22 discharges the Q4 gate voltage so that Q4 is off and Q5 is on, to enable the bleeding. R23 is to pull up Q5 gate voltage to ZD5 reverse voltage and also to limit the current.

To ensure low standby power, the active bleeder should be disabled during dim-to-off. In **Figure 22**, the active bleeding is disabled when output voltage is less than the ZD4 reverse voltage, V_{ZD4}. To sink ZD4 leakage current, R28 = 1 MΩ is added. In this design example, **V_{ZD4} = 18 V** is selected, so that the active bleeder is always disabled when the output voltage is maintained below $V_{LED,min,fully\text{-}dimmed}$ of 13 V during dim-to-off. A weak and passive bleeding resistor $R_{bleed,passive}$ is however necessary to ensure the output voltage is below $V_{LED,min,fully\text{-}dimmed}$. In this design example, **$R_{bleed,passive}$ = 200 kΩ** is selected.

The active bleeder discharge resistor value $R_{bleed,active}$ can be defined as:

$$R_{bleed,active} \geq -\frac{t_{discharge}}{\ln\left(\frac{v_1}{v_0}\right)\cdot C_{out}} \quad (28)$$

Where v_1 is the output voltage after discharge, v_0 is the output voltage before discharge, and $t_{discharge}$ is the discharge time. Considering there is a delay from output OVP triggering until the active bleeder starts discharging, $t_{discharge}$ = 120 ms is selected in this design example.

Taking v_1 = 90 percent of v_0, $R_{bleed,active}$ can then be calculated as:

$$R_{bleed,active} \leq -\frac{0.12}{\ln(0.9)\cdot 940\cdot 10^{-6}} = 1210\ \Omega$$

Based on the above, **$R_{bleed,active}$ = 1000** Ω is selected in this design example.

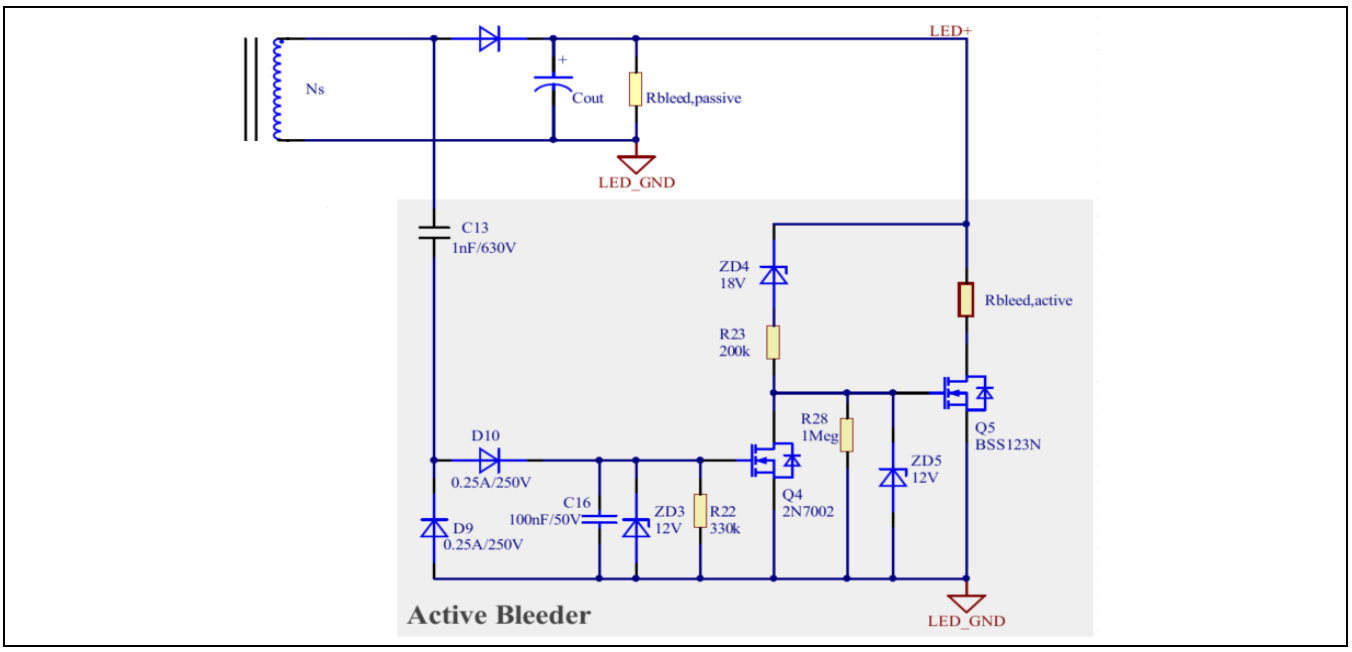


Figure 22 Passive bleeder and active bleeder circuit

12 Input voltage levels for start-up and protection

The $EN_{OVP,In}$ parameter refers to the enable switch for maximum input voltage start-up check and input OVP, based on $V_{in,start,max}$ and V_{inOV} levels, respectively. **$EN_{OVP,In}$ = Enabled** is selected in this design example.

The $EN_{UVP,In}$ parameter refers to the enable switch for minimum input voltage start-up check and input UVP, based on $V_{in,start,min}$ and V_{inUV} levels, respectively. **$EN_{UVP,In}$ = Enabled** is selected in this design example.

*Note: The estimated input voltage V_{in} used for start-up check and protection is in rms value, which is assumed as 0.707 of estimated peak input voltage $V_{in,peak}$. As the input voltage is estimated based on ZCD pin and CS pin switching signals, proper ZCD resistor selection (see **Section 13**) and R_{in} parameter fine-tuning (see **Section 19.1**) are needed.*

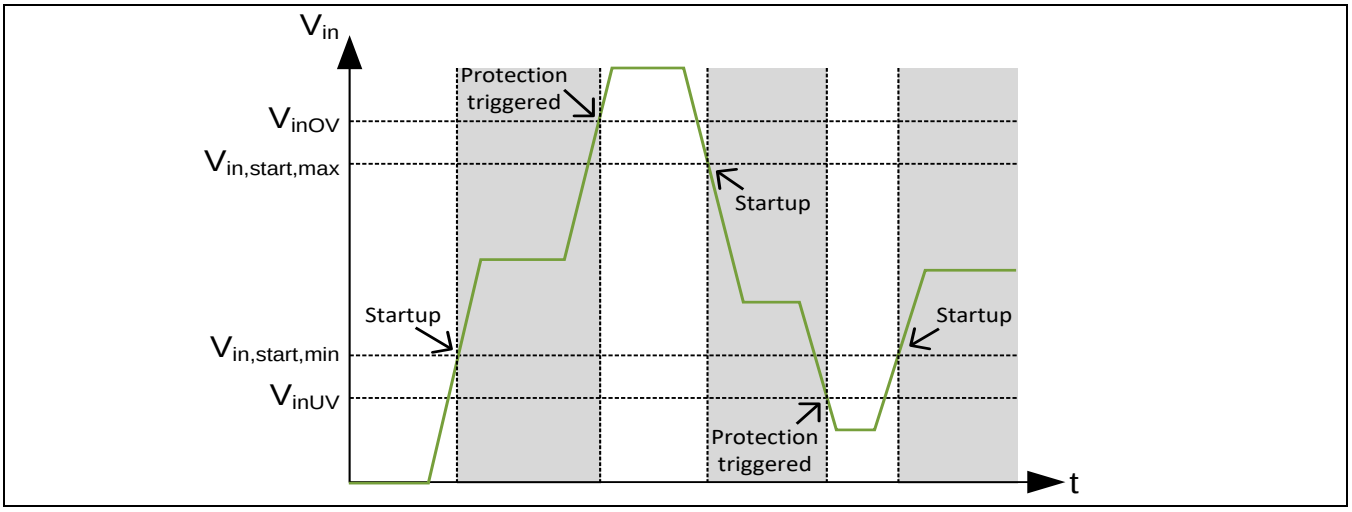


Figure 23 Input voltage levels for start-up and protection

The $V_{in,start,max}$ parameter refers to the maximum input voltage level setting for start-up, which can be defined and calculated as:

$$V_{in,start,max} = e \cdot V_{AC,max} \quad (29)$$

Where e is the ratio recommended to be between 1.05 and 1.10.

Taking e = 1.07,

$$V_{in,start,max} = 1.07 \cdot 305$$

$$\boldsymbol{V_{in,start,max} = 326\ V_{rms}}$$

The V_{inOV} parameter refers to the input OVP level setting, which is recommended as:

$$V_{inOV} \geq V_{in,start,max} \cdot 107\% = 349\ V_{rms} \quad (30)$$

Based on the above, **V_{inOV} = 352 V_{rms}** is selected in this design example.

Note: The reaction of $V_{in,start,max}$ and V_{inOV} protections is auto-restart. A typical blanking time of 1 half-sine-wave period applies on V_{inOV} protection triggering.

The $V_{in,start,min}$ parameter refers to the minimum input voltage level setting for start-up, which can be defined and calculated as:

$$V_{in,start,min} = g \cdot V_{AC,min} \quad (31)$$

Where g is the ratio recommended to be between 0.9 and 0.95.

Taking g = 0.9,

$$V_{in,start,min} = 0.9 \cdot 90$$

$$\boldsymbol{V_{in,start,min} = 81\ V_{rms}}$$

The V_{inUV} parameter refers to the input UV (brown-out) protection level setting, which is recommended as:

$$V_{inUV} \leq V_{in,start,min} \cdot 93\% = 75\ V_{rms} \quad (32)$$

Based on the above, **V_{inUV} = 63 V_{rms}** is selected in this design example.

Note: The reaction of $V_{in,start,min}$ and V_{inUV} protections is auto-restart. A typical blanking time of 10 half-sine-wave periods applies on V_{inUV} protection triggering.

13 ZCD pin-related design

ZCD pin filter capacitor C_{ZCD}, ZCD series resistor $R_{ZCD,1}$ and ZCD shunt resistor $R_{ZCD,2}$ are connected as shown in **Figure 24**.

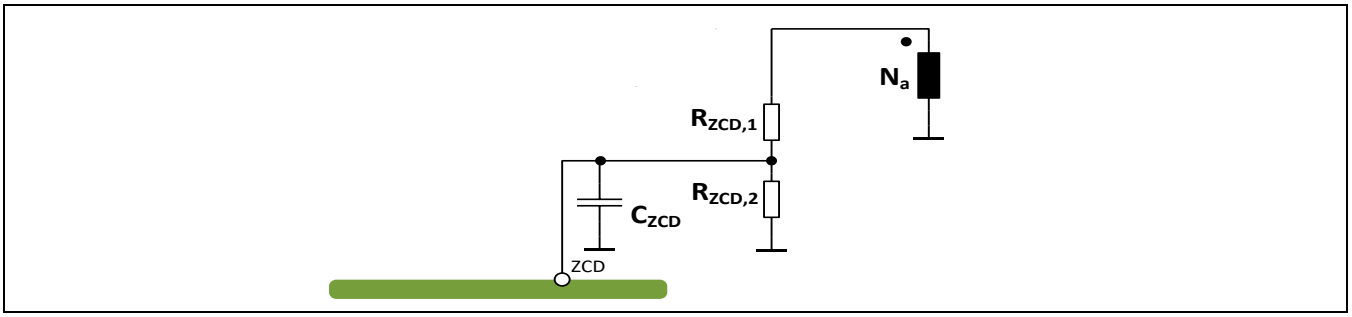


Figure 24 ZCD pin, C_{ZCD}, R_{ZCD1} and R_{ZCD2} connections

C_{ZCD} is mainly for ZCD pin noise-filtering, so a fixed value can generally be used for different designs. **C_{ZCD} = 47 pF** is selected in this design example.

*Note: QR first valley switching of the MOSFET drain voltage can be achieved with t_{ZCDPD} parameter fine-tuning based on **Section 19.2**. **Initial t_{ZCDPD} = 350 ns** can be used for powering-up of the system before the fine-tuning.*

Apart from zero crossing detection, the ZCD pin is also used to measure the reflected input voltage signal when the MOSFET is turned on, and to measure the reflected output voltage signal when the MOSFET is turned off afterward. Hence, it is important to select the correct $R_{ZCD,1}$ and $R_{ZCD,2}$ values, which can cover the necessary measurement range, not only for normal conditions but also for protected conditions.

The recommended minimum ZCD series resistance $R_{ZCD,1,min}$ and maximum ZCD series resistance $R_{ZCD,1,max}$ are defined as:

$$R_{ZCD,1,min} = -\frac{N_a}{I_{IV,max,VinOV} \cdot N_p} \cdot \left[V_{inOV(pk)} + \frac{V_{INPCLN,min} \cdot N \cdot (V_{outOV} + V_d)}{V_{ZCDSH,max,VoutOV}} \right] \quad (33)$$

$$R_{ZCD,1,max} = -\frac{N_a}{I_{IV,min,VinUV} \cdot N_p} \cdot \left[V_{inUV(pk)} - \Delta V_{in,HF,ripple,est} + \frac{V_{INPCLN,max} \cdot N \cdot (V_{outOV} + V_d)}{V_{ZCDSH,min,VoutOV}} \right] \quad (34)$$

Where:

$V_{inOV(pk)}$ and $V_{inUV(pk)}$ are respectively √2 times V_{inOV} and √2 times V_{inUV}.

$I_{IV,max,VinOV}$ and $I_{IV,min,VinUV}$ are respectively the recommended maximum ZCD pin negative clamping current for V_{inOV} sensing and the minimum ZCD pin negative clamping current for V_{inUV} sensing.

$V_{ZCDSH,max,VoutOV}$ and $V_{ZCDSH,min,VoutOV}$ are respectively the recommended maximum and minimum ZCD pin voltage sensing levels for V_{outOV} sensing.

$V_{INPCLN,max}$ and $V_{INPCLN,min}$ are respectively the maximum and minimum ZCD pin negative clamping voltages.

$\Delta V_{in,HF,ripple,est}$ is the estimated difference between the $V_{inUV(pk)}$ level and the high-frequency ripple minimum voltage level at the peak of AC input half-sine-wave. As a rule of thumb, it can be assumed to be between 25 V and 30 V.

Taking $I_{IV,max,VinOV}$ = -3.1 mA, $I_{IV,min,VinUV}$ = -0.15 mA, $V_{ZCDSH,max,VoutOV}$ = 2.6 V, $V_{ZCDSH,min,VoutOV}$ = 2.35 V, $V_{INPCLN,max}$ = -0.22 V, $V_{INPCLN,min}$ = -0.14 V, and $\Delta V_{in,HF,ripple,est}$ = 27.5 V,

$$R_{ZCD,1,min} = -\frac{15}{-3.1 \cdot 10^{-3} \cdot 58} \cdot \left[\sqrt{2} \cdot 352 + \frac{-0.14 \cdot 3.4 \cdot (56.9 + 0.7)}{2.6}\right] = 40.6\ k\Omega$$

$$R_{ZCD,1,max} = -\frac{15}{-0.15 \cdot 10^{-3} \cdot 58} \cdot \left[\sqrt{2} \cdot 62 - 27.5 + \frac{-0.22 \cdot 3.4 \cdot (56.9 + 0.7)}{2.35}\right] = 72.1\ k\Omega$$

It is recommended to choose an R_{ZCD1} value which is around or above the mean value of $R_{ZCD,1,min}$ and $R_{ZCD,1,max}$. Therefore, **$R_{ZCD,1}$ = 56.2 kΩ** is selected in this design example.

The recommended minimum ZCD shunt resistance $R_{ZCD,2,min}$ and maximum ZCD shunt resistance $R_{ZCD,2,max}$ are defined and calculated as:

$$R_{ZCD,2,min} = \frac{R_{ZCD,1} \cdot N_s \cdot V_{ZCDSH,min,VoutOV}}{N_a \cdot (V_{outOV} + V_d) - N_s \cdot V_{ZCDSH,min,VoutOV}} = \frac{56.2 \cdot 10^3 \cdot 17 \cdot 2.35}{15 \cdot (56.9 + 0.7) - 10 \cdot 2.35} = 2.67\ k\Omega \quad (35)$$

$$R_{ZCD,2,max} = \frac{R_{ZCD,1} \cdot N_s \cdot V_{ZCDSH,max,VoutOV}}{N_a \cdot (V_{outOV} + V_d) - N_s \cdot V_{ZCDSH,max,VoutOV}} = \frac{56.2 \cdot 10^3 \cdot 17 \cdot 2.6}{15 \cdot (56.9 + 0.7) - 10 \cdot 2.6} = 2.96\ k\Omega \quad (36)$$

Based on the above, **$R_{ZCD,2}$ = 2.7 kΩ** is selected in this design example.

When the AC input voltage decreases at full-load output, the DC-link filter capacitor high-frequency peak-to-peak voltage ripple would increase, and this would also result in higher ripple on the ZCD pin negative clamping current, which is used for estimating input voltage V_{in}. Hence, for good V_{in} estimation via the ZCD pin, especially at input UVP level V_{inUV}, such a ripple effect should be minimized and compensated with proper configuration of $t_{on,max}$ and R_{in} parameters, respectively.

$t_{on,max}$ parameter denotes the maximum on-time. $t_{on,max}$ should be configured not too high, while being able to deliver the steady-state full-load output power $P_{out,full}$ at $V_{in,start,min}$. As such, the maximum output power can also be reduced during brown-out, to protect the primary components such as the Flyback MOSFET from overheating. Therefore, $t_{on,max}$ can be defined and calculated as:

$$t_{on,max} = \frac{e \cdot L_p \cdot I_{pri(pk),max}}{\sqrt{2} \cdot V_{in,start,min}} \quad (37)$$

Where e is the ratio for margin on the maximum on-time, which is recommended to be between 1.0 and 1.05.

Taking e = 1.02,

$$t_{on,max} = \frac{1.02 \cdot 566 \cdot 10^{-6} \cdot 2.289}{\sqrt{2} \cdot 81}$$

$$\boldsymbol{t_{on,max,at,V,in,low} = 11.5\ \mu s}$$

R_{in} parameter is to compensate for the DC-link filter capacitor voltage ripple for accurate V_{in} measurement. As this parameter configuration is subject to the line filter and the DC-link filter capacitance design, parameter fine-tuning based on actual waveform measurement is required.

For powering up the board, the initial R_{in} parameter can be defined and calculated as:

$$Initial\ R_{in} = \frac{\Delta V_{in,HF,ripple,est}}{I_{pri(pk),max}} \quad (38)$$

$$Initial\ R_{in} = \frac{27.5}{2.289}$$

$$\boldsymbol{Initial\ R_{in} = 12.0\ \Omega}$$

Upon successful powering-up of the system, please refer to **Section 19.1** for the fine-tuning guide for the R_{in} parameter.

14 Multimode-related parameters

In regulated mode, there are three different switching modes, which are QRM1, Discontinuous Conduction Mode (DCM) without valley switching, and Active Burst Mode (ABM). The integrated primary-side control loop selects the switching mode depending on the operating condition.

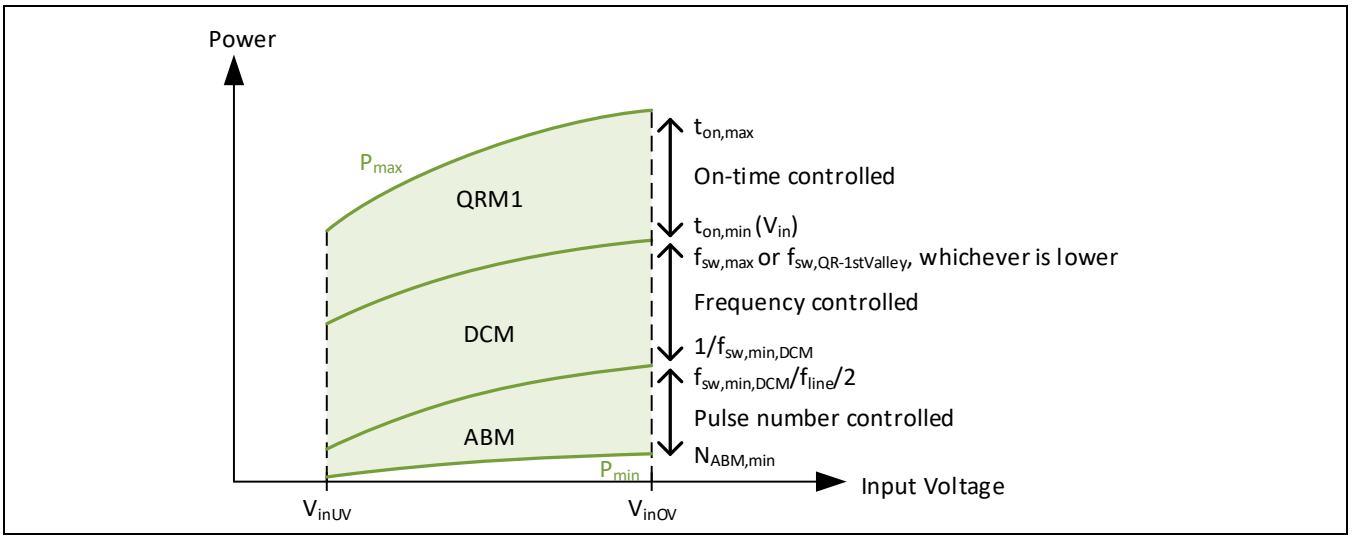


Figure 25 Multimode operation scheme

14.1 ABM enable switch

The EN_{ABM} parameter refers to the enable switch for ABM. For a dimming application that has $I_{out,min}$ not more than 10 percent of $I_{out,full}$, the EN_{ABM} parameter should be enabled. In this design example, $I_{out,min}$ is 5 percent of $I_{out,full}$, so the **EN_{ABM} = Enabled** setting is selected.

14.2 On-time limit and switching frequency limit

The minimum on-time variable $t_{on,min}(V_{in})$ is based on the $t_{on,min}$ parameter or $t_{on,min,V,out,sense}(V_{in})$ variable, whichever is higher. The $t_{on,min,V,out,sense}(V_{in})$ variable denotes the minimum on-time required for V_{out} sensing, which is dependent on V_{in} measurement and the $t_{min,demag}$ parameter (see the equation in **Figure 26**).

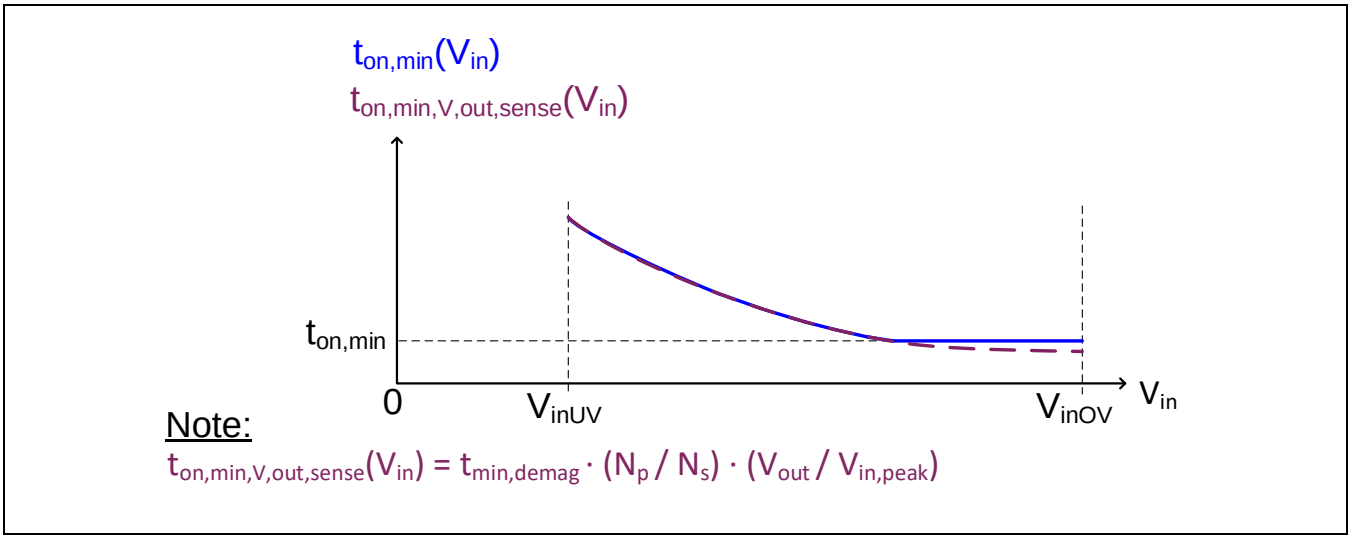


Figure 26 Minimum on-time depending on the estimated input voltage

The recommended on-time limit related parameter configuration from **Table 5** is selected in this design example.

Table 5 On-time limit parameter configuration

Parameter name	Recommended value	Unit
$t_{on,max}$	Refer to calculation in **Section 13**	µs
$t_{on,min}$	2.0	µs
$t_{min,demag}$	3.0	µs

In QRM1, the maximum switching frequency parameter $f_{sw,max}$ affects the number of first valley switching pulses over every AC input half-sine-wave period. To lower the input current Total Harmonic Distortion (iTHD) at high input voltage and high output power, the number of first valley switching pulses can be reduced by lowering $f_{sw,max}$. However, please note that the efficiency could be reduced if the number of first valley switching pulses is reduced too much. As a start, it is recommended to use **$f_{sw,max}$ = 70 kHz** and fine-tune it later if necessary.

To achieve good EMI and light quality in DCM without valley switching, the maximum switching frequency can be modulated, based on the modulation attenuation parameter $N_{DCM,mod,gain}$. However, please note that the input power quality could be degraded by the modulation. As a start, it is recommended to use **$N_{DCM,mod,gain}$ = 16** and fine-tune it later if necessary.

The minimum switching frequency parameter setting of **$f_{sw,min,DCM}$ = 20 kHz** is recommended and selected in this design example.

14.3 ABM minimum pulse number

The minimum ABM pulse number parameter $N_{ABM,min}$ can be defined and calculated as:

$$N_{ABM,min} = \frac{V_{LED,min,at,I,out,min} \cdot I_{out,min} \cdot L_p}{2 \cdot h \cdot f_{line,max} \cdot {V_{AC,max}}^2 \cdot {t_{on,min}}^2} \quad (39)$$

Where $V_{LED,min,at,I,out,min}$ is the minimum LED voltage at $I_{out,min}$ and h is the ratio recommended to be between 0.6 and 0.7.

Taking $V_{LED,min,at,I,out,min}$ = 14 V and h = 0.63,

$$N_{ABM,min} = \frac{14 \cdot 41.5 \cdot 10^{-3} \cdot 566 \cdot 10^{-6}}{2 \cdot 0.63 \cdot 63 \cdot 305^2 \cdot (2 \cdot 10^{-6})^2} = 11.1$$

Based on the above and $N_{ABM,min}$ should be an integer, **$N_{ABM,min}$ = 11** parameter setting is selected.

Note: The $N_{ABM,min}$ parameter setting cannot be less than 4.

14.4 Control-loop initialization

When the regulated mode is entered initially after the start-up phase, the control loop is initialized. To ensure a fast and smooth start-up with minimal output current overshoot, XDPL8210 features an adaptive control loop switching parameter initialization depending on the EN_{ABM} parameter and estimated input voltage V_{in}:

- If ABM is enabled with the EN_{ABM} parameter, ABM is selected as the initial switching mode for the control loop. The initial controlled ABM switching pulse number $N_{ABM,init}$ is scaled between $N_{ABM,min}$ and $N_{ABM,init,VinUV}$ parameters, depending on V_{in}.
- If ABM is disabled with the EN_{ABM} parameter, DCM is selected as the initial switching mode for the control loop. The initial controlled DCM switching frequency number $f_{DCM,init}$ is scaled between $f_{sw,min,DCM}$ parameter and $f_{DCM,init,VinUV}$ (20 kHz typ.), depending on V_{in}.

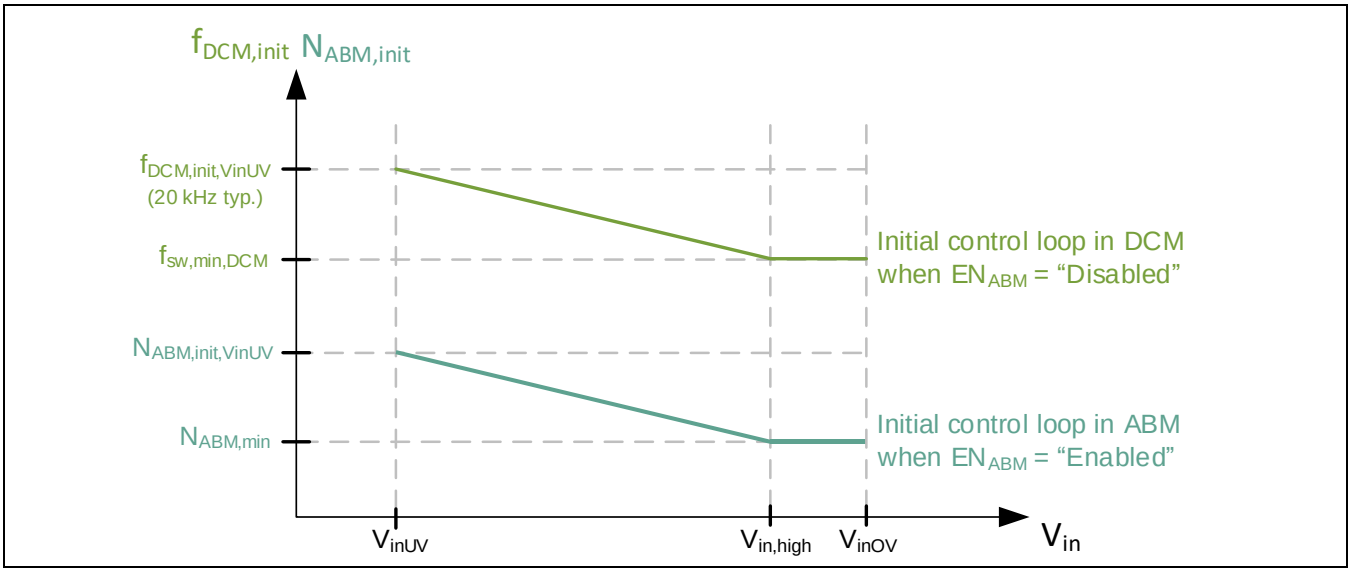


Figure 27 Minimum on-time depending on the estimated input voltage

$V_{in,high}$ in **Figure 27** refers to the high input voltage parameter. With the EN_{ABM} parameter enabled in this design example, $N_{ABM,init} = N_{ABM,min}$ is applied when the estimated input voltage V_{in} is $V_{in,high}$ or more.

$V_{in,high}$ can be defined and calculated as:

$$V_{in,high} = \frac{V_{AC,max}}{k} \quad (40)$$

Where k is the ratio recommended to be between 1.05 and 1.1.

Taking k = 1.1,

$$V_{in,high} = \frac{305}{1.1}$$

$$\boldsymbol{V_{in,high} = 277\ V_{rms}}$$

$N_{ABM,init,VinUV}$ in **Figure 27** refers to the initial ABM pulse number when the estimated input voltage V_{in} is V_{inUV}. $N_{ABM,init,VinUV}$ can be defined as:

$$N_{ABM,init,VinUV} = N_{ABM,min} \cdot \left(\frac{V_{in,high}}{V_{in,start,min}}\right)^2 \cdot \left[\frac{t_{on,min}}{t_{on,min}(V_{in,start,min})}\right]^2 \quad (41)$$

Where $t_{on,min}(V_{in,start,min})$ is the minimum on-time at $V_{in,start,min}$, which can be defined and calculated as:

$$t_{on,min}(V_{in,start,min}) = Max\left\{t_{min,demag} \cdot \left(\frac{N_p}{N_s}\right) \cdot \left(\frac{V_{LED,min,at,I,out,min}}{\sqrt{2} \cdot V_{in,start,min}}\right),\ t_{on,min}\right\} \quad (42)$$

$$t_{on,min}(V_{in,start,min}) = Max\left\{3 \cdot 10^{-6} \cdot \left(\frac{58}{17}\right) \cdot \left(\frac{14}{\sqrt{2} \cdot 80}\right),\ 2 \cdot 10^{-6}\right\} = Max\{1.27 \cdot 10^{-6},\ 2 \cdot 10^{-6}\} = 2\ \mu s$$

Taking $t_{on,min}(V_{in,start,min}) = 2\ \mu s$ into equation (41), $N_{ABM,init,VinUV}$ can be calculated as:

$$N_{ABM,init,VinUV} = 11 \cdot \left(\frac{277}{80}\right)^2 \cdot \left[\frac{2 \cdot 10^{-6}}{2 \cdot 10^{-6}}\right]^2 = 131.9$$

Based on the above and $N_{ABM,init,VinUV}$ should be an integer, **$N_{ABM,init,VinUV}$ = 132** parameter setting is selected.

Note: The $N_{ABM,min}$ parameter maximum configurable limit is $f_{sw,min,DCM}/80 + 20$. In this design example, $f_{sw,min,DCM}$ is 20 kHz, so the resulting $N_{ABM,min}$ parameter maximum configurable limit is 270.

14.5 Control-loop response

The XDPL8210 uses a Proportional-Integral (PI) regulator as the control loop for its primary-side output current regulation, thus the control-loop response is determined by the proportional gain parameter (K_P) and integral gain parameter (K_I) of the PI regulator. For each switching mode, the control-loop response is determined by each dedicated set of K_P and K_I parameters.

In ABM, the PI regulator will be active only if the absolute error is higher than a threshold which is defined by the multiplication of the $ABM_{thrs,multiplier}$ parameter and the ABM first pulse averaging output current over the ABM cycle period.

The recommended on-time limit related parameter configuration from **Table 6** is selected in this design example.

Table 6 Control-loop response parameter configuration

Parameter name	Recommended value	Unit
$K_{P,QRM}$	512	–
$K_{I,QRM}$	32	–
$K_{P,DCM}$	2048	–
$K_{I,DCM}$	512	–
$K_{P,ABM}$	128	–
$K_{I,ABM}$	32	–
$ABM_{thrs,multiplier}$	3.00	–

If necessary, the control-loop response can be improved by adjusting these parameter values but it is important to be aware of the possible side-effects. **Table 7** shows the effects of increasing the value of K_P and K_I respectively.

Table 7 Effects of increasing the values of K_P and K_I

Parameter	Output rise time	Output overshoot	Output settling time	Output stability
K_P	Decrease	Increase	Small change	Degrade
K_I	Decrease	Increase	Increase	Degrade

15 V_{CC} supply-related and dimming circuit design

In this design example, the transformer primary and secondary auxiliary winding are designed to supply the V_{CC} of XDPL8210 and CDM10VD, respectively. Based on the winding turns ratio selected in in **Section 4**, the maximum primary auxiliary winding demagnetization voltage $V_{a,max}$ and the maximum secondary auxiliary winding demagnetization voltage $V_{a,sec,max}$ can be defined and calculated based on:

$$V_{a,max} = \left(V_{LED,max} + V_d\right) \cdot \frac{N_a}{N_s} = (54 + 0.7) \cdot \frac{15}{17} = 48.3\ V \quad (43)$$

$$V_{a,sec,max} = \left(V_{LED,max} + V_d\right) \cdot \frac{N_{a,sec}}{N_s} = (54 + 0.7) \cdot \frac{15}{17} = 48.3\ V \quad (44)$$

As the calculated $V_{a,max}$ exceeds 22 V, a voltage regulator circuit for XDPL8210 V_{CC} supply is deployed, as shown in **Figure 28**, and the **VCC_{SUPPLY} = "Wide"** parameter setting is therefore selected.

*Note: If the calculated $V_{a,max}$ is 22 V or below, the voltage regulator circuit in **Figure 28** can be bypassed and the VCC_{SUPPLY} = "Narrow" parameter setting can then be selected. However, it is mandatory to ensure its V_{CC} absolute maximum rating of 26 V is not exceeded in actual testing with all the necessary test conditions, such as the output open test.*

Note: If V_{CC} supply is not supplied from the primary auxiliary winding, the VCC_{SUPPLY} = "External" parameter setting should be selected.

As the calculated $V_{a,sec,max}$ exceeds 22 V, a voltage regulator circuit for CDM10VD V_{CC} supply is also deployed, as shown in **Figure 28**.

Note: If the calculated $V_{a,sec,max}$ is 22 V or below, the voltage regulator circuit for CDM10VD V_{CC} can be omitted. However, it is mandatory to ensure its V_{CC} absolute maximum rating of 26 V is not exceeded in actual testing with all the necessary test conditions, such as the output open test.

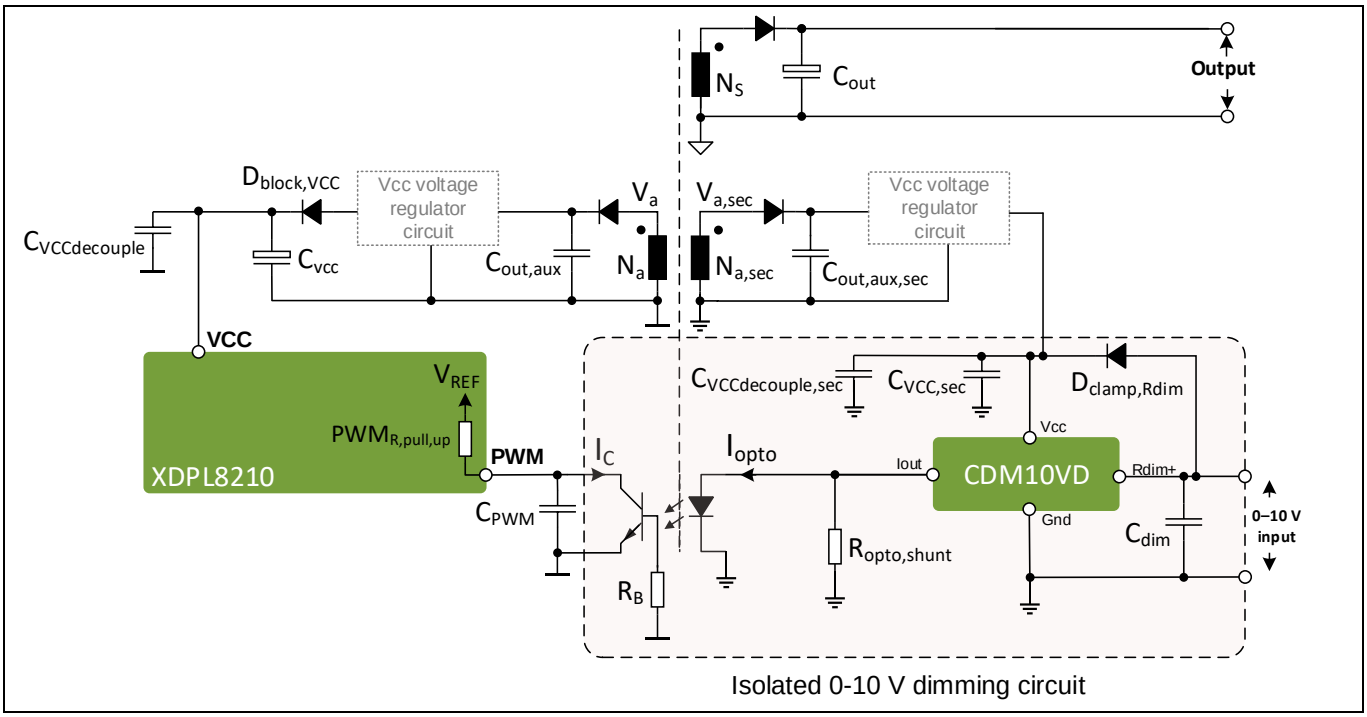


Figure 28 V_{CC} supply and isolated 0–10 V dimming circuit

The primary auxiliary output capacitor $C_{out,aux}$ dimensioning is important to hold up the V_{CC} voltage, especially during ABM. The recommended minimum primary auxiliary output capacitor value $C_{out,aux,min}$ can be defined as:

$$C_{out,aux,min} = \frac{I_{IC,avg,est} \cdot \left(\frac{1}{2 \cdot F_{line,min}} - \frac{N_{ABM,min}}{f_{sw,min,DCM}}\right)}{\left(V_{LED,min,at,I,out,min} + V_d\right) \cdot \left(\frac{N_a}{N_s}\right) - V_{a,UVOFF}} - C_{VCC} \quad (45)$$

Where $V_{a,UVOFF}$ is the estimated primary auxiliary winding demagnetization voltage when XDPL8210 V_{CC} reaches IC turn-off threshold.

Taking $V_{a,UVOFF}$ = 9 V, $C_{out,aux,min}$ can be calculated as:

$$C_{out,aux,min} = \frac{12 \cdot 10^{-3} \cdot \left(\frac{1}{2 \cdot 47} - \frac{11}{20 \cdot 10^3}\right)}{(14+0.7) \cdot \left(\frac{15}{17}\right) - 9} - 15 = 15.5\ \mu F$$

Based on the above, **$C_{out,aux}$ = 22 µF** is selected.

The secondary auxiliary output capacitor $C_{out,aux,sec}$ and the CDM10VD V_{CC} capacitor $C_{VCC,sec}$ dimensionings are important to hold up the V_{CC} voltage, especially for the PWM duty-cycle measuring phase during dim-to-off. For proper dim-to-off exiting, it is recommended to use a ceramic capacitor, which has low ESR for both $C_{out,aux,sec}$ and $C_{VCC,sec}$. **$C_{out,aux,sec}$ = 4.7 µF** and **$C_{VCC,sec}$ = 4.7 µF** are recommended and selected in this design example.

A noise decoupling ceramic capacitor of **$C_{VCCdecouple,sec}$ = 0.1 µF** with low ESR is added in parallel to $C_{VCC,sec}$. In addition, **C_{PWM} = 100 pF** and **C_{dim} = 22 nF** are added for noise filtering on the XDPL8210 PWM pin and CDM10VD R_{dim+} pin respectively.

$D_{clamp,Rdim}$ is connected from the R_{dim+} pin to the V_{CC} pin to ensure the voltage level at the R_{dim+} pin does not exceed its maximum voltage rating of V_{CC} + 0.7 V, in case of an active voltage source (e.g. DC power supply) being applied to it for testing or productive use. For productive use with only a passive voltage source (e.g. potentiometer, current sink dimmer) it can be connected to the R_{dim+} pin, and $D_{clamp,Rdim}$ can be omitted. It is highly recommended to use a low-leakage Schottky diode for $D_{clamp,Rdim}$ for high accuracy of the dimmer voltage measurement on the R_{dim+} pin. In this design example, **$D_{clamp,Rdim}$ with V_F = 0.42 V, V_R = 30 V and I_R = 10 µA** is selected.

The **optocoupler with photo-transistor output and base connection** shown in **Figure 28** is recommended and selected in this design example, to have faster switching response with the base resistor R_B connected, for more accurate PWM duty-cycle sensing by XDPL8210. **R_B = 300 kΩ** is recommended and selected in this design example. $R_{opto,shunt}$ is optional, to discharge the opto-diode residual forward voltage after the falling edge of I_{opto}. In this design example, **$R_{opto,shunt}$ = 47 kΩ** is selected.

Figure 29 and **Figure 30** show a BJT-based V_{CC} regulator circuit and depletion MOSFET-based V_{CC} regulator circuit respectively.

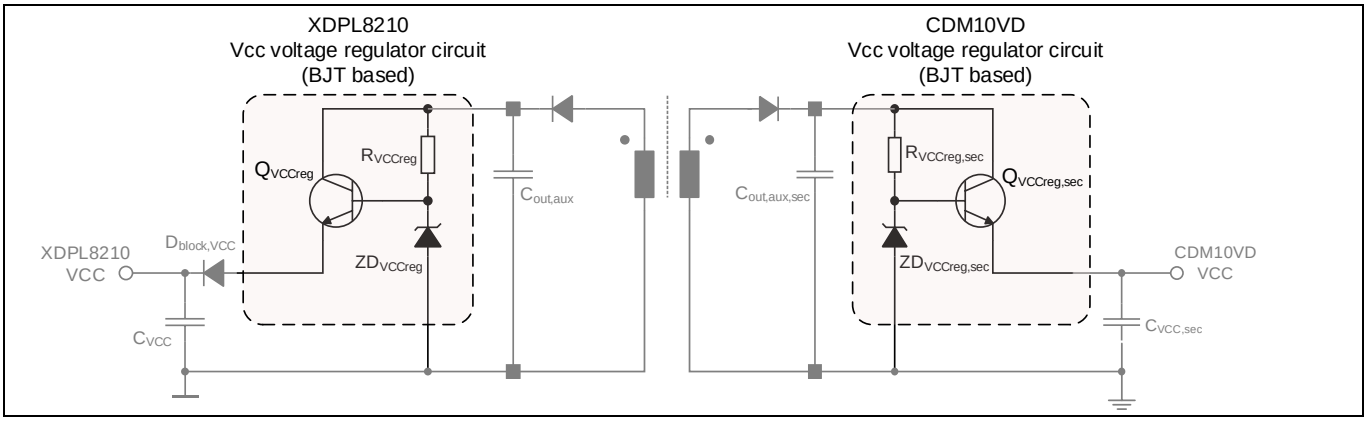


Figure 29 V_{CC} voltage regulator circuit (BJT based)

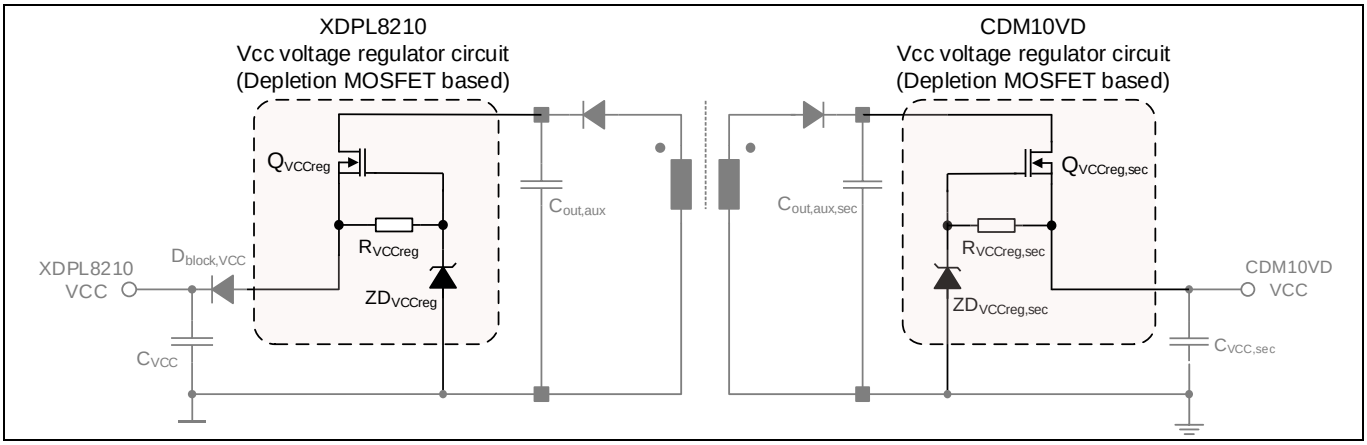


Figure 30 V_{cc} voltage regulator circuit (depletion MOSFET based)

The depletion MOSFET-based V_{CC} regulator circuit has lower losses than the BJT-based V_{CC} regulator circuit, especially when the difference between primary auxiliary output voltage and ZD_{VCCreg} reverse voltage increases.

$D_{block,Vcc}$ is to block the HV pin current from flowing into the V_{CC} voltage regulator circuit, during start-up and auto-restart.

16 Other protection-related parameters

16.1 Regulated mode peak output OCP

When the $EN_{Iout,max,peak}$ parameter is enabled, the regulated mode peak output Over-Current Protection (OCP) is triggered when the estimated average output current per switching cycle is above $I_{out,max,peak}$ for a longer period than the $t_{Iout,max,peak,blank}$ parameter. $I_{out,max,peak}$ is recommended to be at least 2.25 times the $I_{out,full}$, which is at least 1867.5 mA for this design example.

In this design example, **$EN_{Iout,max,peak}$ = Enabled**, **$I_{out,max,peak}$ = 2100 mA** and **$t_{Iout,max,peak,blank}$ = 1 ms** parameter settings are selected.

The reaction of this protection is fixed as auto-restart. The auto-restart speed is configurable based on the $Speed_{OCP,Iout}$ parameter:

- If $Speed_{OCP,Iout}$ is configured as “fast”, the auto-restart time is approximately 0.4 s.
- If $Speed_{OCP,Iout}$ is configured as “slow”, the auto-restart time is based on the configurable $t_{auto,restart}$ parameter.

In this design example, the **$Speed_{OCP,Iout}$ = fast** parameter setting is selected.

16.2 IC over-temperature protection

The IC over-temperature protection level is based on the $T_{critical}$ parameter. Its protection reaction is fixed as auto-restart, while the maximum junction temperature for start-up/restart is fixed as 4°C below $T_{critical}$.

$T_{critical}$ = 119°C is recommended and selected in this design example.

16.3 Debug mode

The parameter setting of **$Debug_{Mode}$ = Disabled** is selected in this design example. The $Debug_{Mode}$ parameter should only be enabled for debugging purposes. For more details on XDPL8210 debug mode, please refer to **Section 20.1**.

17 PCB layout guide

a) Minimize the circumference of the following high-current/high-frequency loops with traces which are short and wide (or with jumper wires which are short and thick):
   - power switch loop formed by DC-link filter capacitor $C_{DC,filter}$, primary main winding, Flyback MOSFET and CS resistor R_{CS}
   - main output rectifier loop formed by secondary main winding, main output diode and main output capacitor
   - auxiliary output rectifier loop formed by auxiliary winding, auxiliary output diode and auxiliary output capacitor.

b) Place each filter capacitor, V_{CC} noise decoupling capacitor $C_{VCCdecouple}$, ZCD pin filter capacitor C_{ZCD} and PWM pin filter capacitor C_{PWM} near to its designated pin and the GND pin of the controller.

c) Apply the following guide for star grounding:
   - Connect ground signal traces of $C_{VCCdecouple}$, C_{ZCD}, $R_{ZCD,2}$, C_{PWM}, the controller GND pin and the optocoupler emitter pin.
   - Connect V_{CC} ground traces of the V_{CC} capacitor C_{VCC} and primary auxiliary winding.
   - Connect the C_{HV} GND pin near to the ground pin of $C_{DC,filter}$.
   - Connect the GND pin of each C_{VCC}, $C_{VCCdecouple}$, R_{CS} and bridge rectifier separately to a single point near $C_{DC,filter}$.

d) Ensure the high dv/dt traces from the MOSFET drain and GD pin are as far as possible from the PWM pin and its connected trace.

e) Shield signal traces with ground traces or ground plane, which can help to reduce noise pick-up.

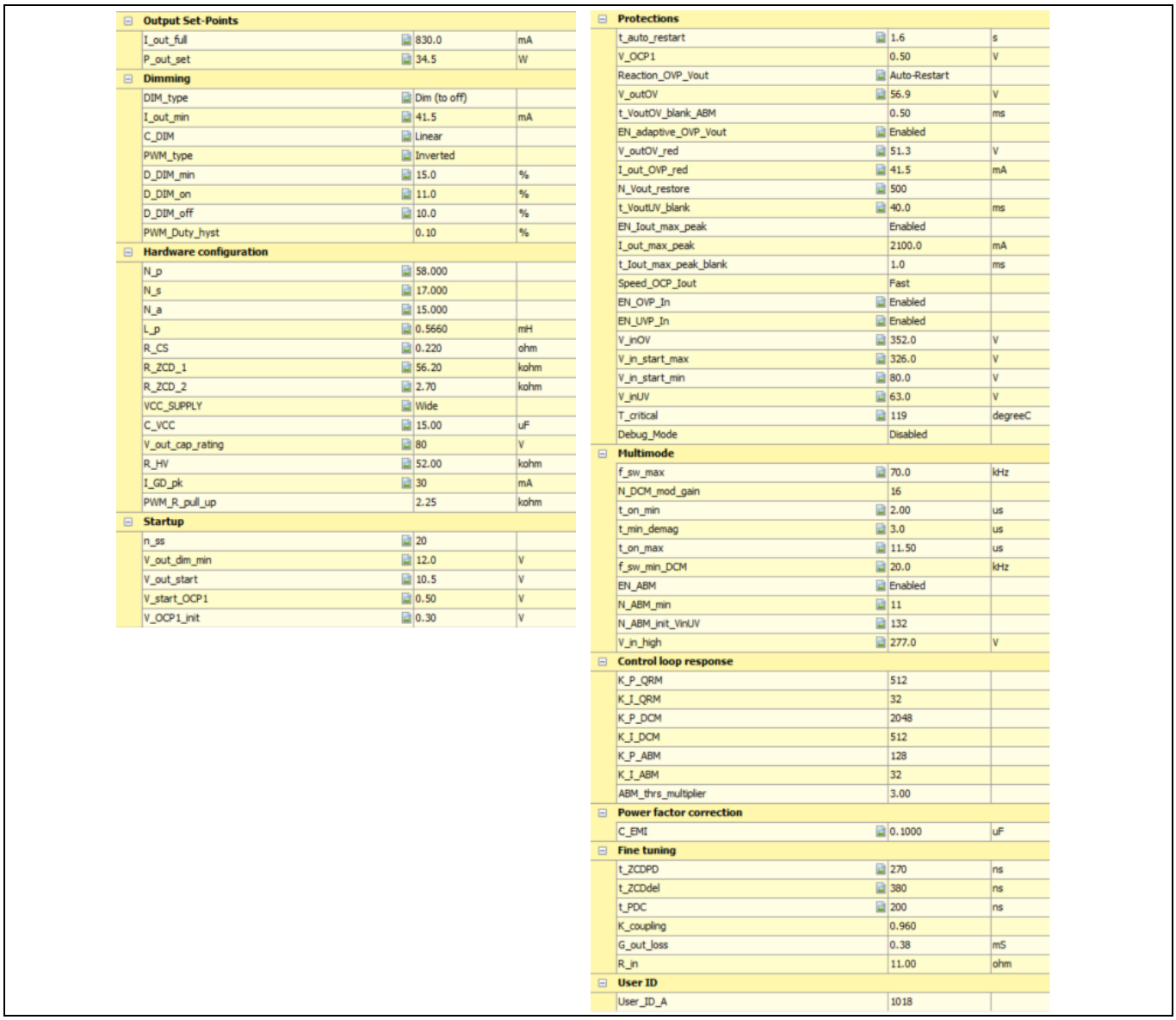
f) Always ensure appropriate safety clearances between the HV and LV nets.

18 Parameter configuration list, set-up and procedures

18.1 Parameter configuration list

Figure 31 shows the XDPL8210 parameter configuration list, with selected values based on the design examples from **Section 2** to **Section 16**. For another system design, the values in the list might be different.

For the IC parameter configuration set-up and procedures, please refer to **Section 18.2** and **Section 18.3**. For safety purposes, before powering up the board, it is important to ensure that the configured IC parameter values in the hardware configuration section in **Figure 31** are compatible with the actual system hardware dimensioning.



Output Set-Points		
I_out_full	830.0	mA
P_out_set	34.5	W
Dimming		
DIM_type	Dim (to off)	
I_out_min	41.5	mA
C_DIM	Linear	
PWM_type	Inverted	
D_DIM_min	15.0	%
D_DIM_on	11.0	%
D_DIM_off	10.0	%
PWM_Duty_hyst	0.10	%
Hardware configuration		
N_p	58.000	
N_s	17.000	
N_a	15.000	
L_p	0.5660	mH
R_CS	0.220	ohm
R_ZCD_1	56.20	kohm
R_ZCD_2	2.70	kohm
VCC_SUPPLY	Wide	
C_VCC	15.00	uF
V_out_cap_rating	80	V
R_HV	52.00	kohm
I_GD_pk	30	mA
PWM_R_pull_up	2.25	kohm
Startup		
n_ss	20	
V_out_dim_min	12.0	V
V_out_start	10.5	V
V_start_OCP1	0.50	V
V_OCP1_init	0.30	V

Protections		
t_auto_restart	1.6	s
V_OCP1	0.50	V
Reaction_OVP_Vout	Auto-Restart	
V_outOV	56.9	V
t_VoutOV_blank_ABM	0.50	ms
EN_adaptive_OVP_Vout	Enabled	
V_outOV_red	51.3	V
I_out_OVP_red	41.5	mA
N_Vout_restore	500	
t_VoutUV_blank	40.0	ms
EN_Iout_max_peak	Enabled	
I_out_max_peak	2100.0	mA
t_Iout_max_peak_blank	1.0	ms
Speed_OCP_Iout	Fast	
EN_OVP_In	Enabled	
EN_UVP_In	Enabled	
V_inOV	352.0	V
V_in_start_max	326.0	V
V_in_start_min	80.0	V
V_inUV	63.0	V
T_critical	119	degreeC
Debug_Mode	Disabled	
Multimode		
f_sw_max	70.0	kHz
N_DCM_mod_gain	16	
t_on_min	2.00	us
t_min_demag	3.0	us
t_on_max	11.50	us
f_sw_min_DCM	20.0	kHz
EN_ABM	Enabled	
N_ABM_min	11	
N_ABM_init_VinUV	132	
V_in_high	277.0	V
Control loop response		
K_P_QRM	512	
K_I_QRM	32	
K_P_DCM	2048	
K_I_DCM	512	
K_P_ABM	128	
K_I_ABM	32	
ABM_thrs_multiplier	3.00	
Power factor correction		
C_EMI	0.1000	uF
Fine tuning		
t_ZCDPD	270	ns
t_ZCDdel	380	ns
t_PDC	200	ns
K_coupling	0.960	
G_out_loss	0.38	mS
R_in	11.00	ohm
User ID		
User_ID_A	1018	

Figure 31 IC parameter configuration list with selected values based on design examples from Section 2 to Section 16

*Note: The $User_{ID,A}$ parameter in **Figure 31** has no effect on the IC behavior and system performance. By default, the value of this parameter is set to zero. If necessary, it can be configured to store system information, such as parameter version, LED driver model, etc.*

18.2 Parameter configuration set-up

The tools needed for on-board XDPL8210 parameter configuration are listed in **Table 8**.

Table 8 Tools needed for XDPL8210 parameter configuration

Tool type	Tool name	Description	Ordering/Download link	Ordering/Download content
Hardware	.dp Interface Gen2	.dp Interface board	**IF-BOARD.DP-GEN2**	.dp Interface Gen2 x 1 USB cable x 1
Software	.dp Vision	GUI for parameter configuration of all .dp products	**Infineon Toolbox** *Note:* *Please install .dp Vision before running the XDPL8210 .dp Vision folder set-up file shown below.*	Latest version of the .dp Vision installer (*.exe)
	XDPL8210 parameter csv file	XDPL8210 parameter configuration file	**XDPL8210 35W reference board homepage** *Note:* *Please download the zipped package which contains the .dp Vision folder setup file (*.msi).*	Latest version of .dp Vision folder setup file (*.msi), which installs the following: XDPL8210 35 W reference design engineering report (*.pdf) and parameter configuration file (*.csv), including images for the configuration file. XDPL8210 design guide (*.pdf)

Figure 32 shows the hardware set-up needed for the on-board XDPL8210 parameter configuration.

Note: Please ensure the board is not supplied with any voltage before connecting the programmable cable to the target XDPL8210 board. For parameter configuration on the XDPL8210 35 W reference design, please connect the programming cable to its configuration connector X2.

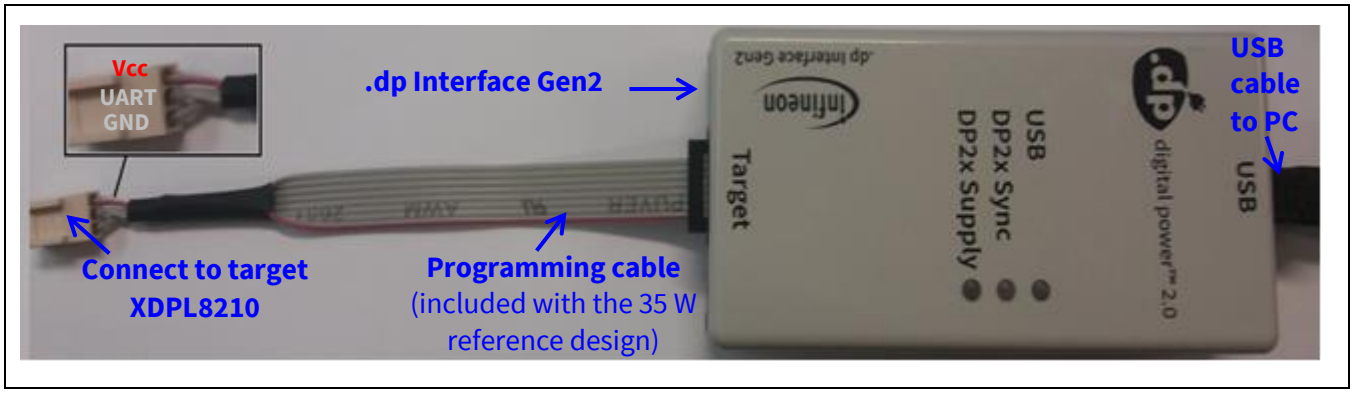


Figure 32 Hardware set-up for on-board XDPL8210 parameter configuration

18.3 Parameter configuration procedures

After the hardware connections for XDPL8210 configuration (see **Figure 32**) are done, please start the program by clicking the shortcut ".dp Vision" on the desktop.

Note: During the program start-up, if the system shows there is a newer version of .dp Vision, please follow the procedure and update accordingly. As the screenshots were taken based on .dp Vision version 2.0.9.4, it might look different for newer versions of .dp Vision.

A .dp Vision user manual is available by clicking [Help] >> [Help contents], to provide detailed instructions on how to use this GUI for parameter configuration. Alternatively, the following simple guide is also available for quick and easy reference.

Open the XDPL8210 parameter configuration file (*.csv) from the default installation folder at ***C:\Users\<Username>\Infineon Technologies AG\.dp vision\Parameters***, as shown in **Figure 33**.

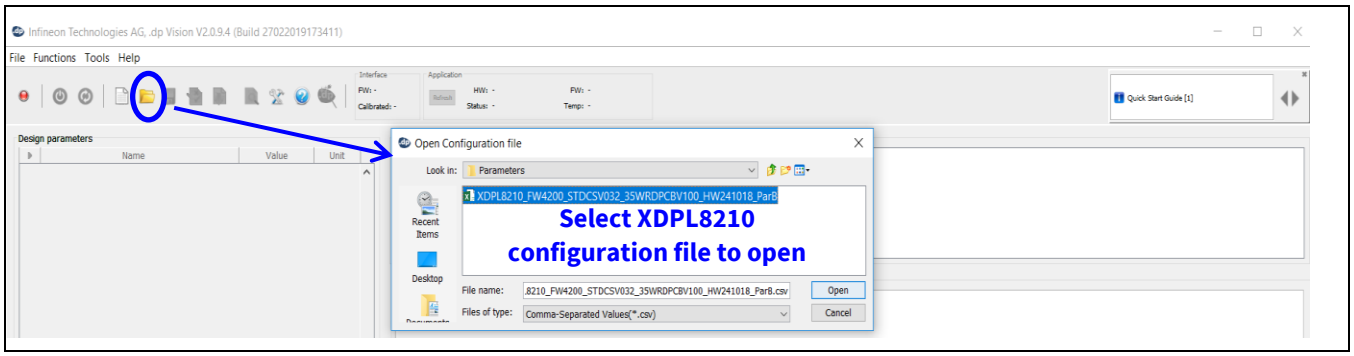


Figure 33 Opening the XDPL8210 parameter configuration file (*.csv) in .dp Vision

After opening the parameter csv file, a list of configurable parameters with default values based on the reference board design will be shown (see the box on the left in **Figure 34**). These default values can be changed for another board design, by referring to the design guide from **Section 2** to **Section 17** and the fine-tuning guide in **Section 19.4**.

If a parameter value is changed and no limit violation is found, the changed value itself will turn blue, like the example in **Figure 34** which the $I_{out,full}$ parameter in the hardware configuration section has been changed from 830 mA to 800 mA. Otherwise, if an error is detected (e.g. exceeded min./max. value), the parameter value which caused the error will turn red and the message bar of .dp Vision (see the top right in **Figure 34**) will show an error message. If any error is not resolved, the user is not allowed to configure the IC with the changed value.

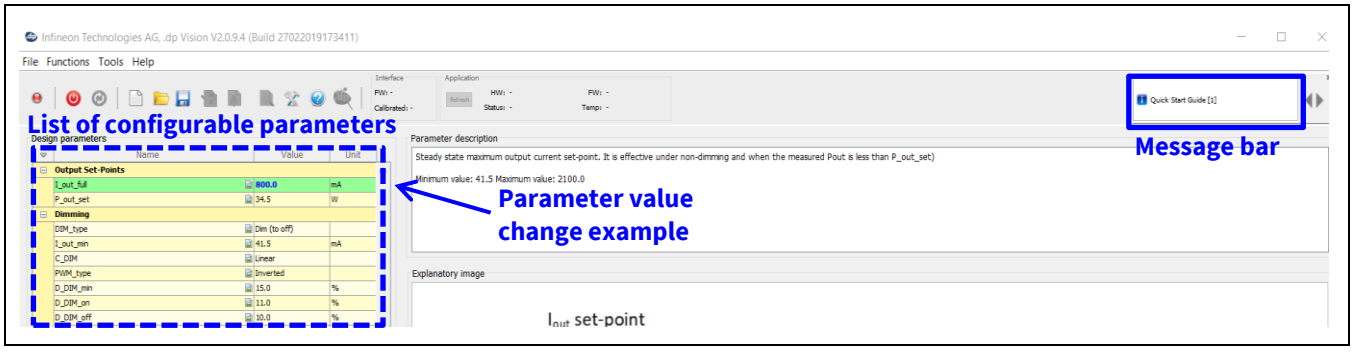


Figure 34 Changing parameter values of XDPL8210 configuration file in .dp Vision

Note: For safety and proper system functioning, it is important to ensure the hardware configuration section parameter values are compatible with the actual system hardware dimensioning.

There are two options available to configure the IC based on the list of parameter values shown in .dp Vision.

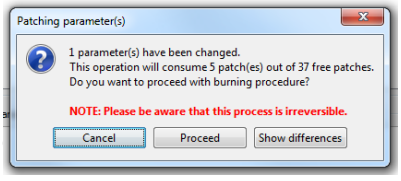
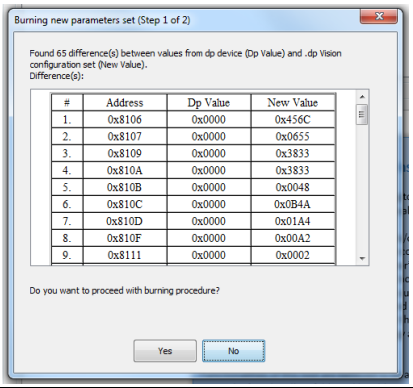
- Burn configuration

  It is important to note that the new XDPL8210 chip from Infineon does not contain any parameter configuration by default, so the user should first burn a full set of parameters on the new chip using this function, before any application testing. If the XDPL8210 chip on board has already been burned with a first full set of parameters in its One-Time Programmable (OTP) memory space, such as the XDPL8210 35 W reference board, any IC parameter value change on it with this option is considered as parameter patching. There are a total of 77 patchable OTP memory spaces.

  Each time the burn configuration function is executed, .dp Vision will detect if there is parameter value difference between the saved configuration file and the target XDPL8210. If a difference is detected, each burn configuration will consume a minimum of three patchable memory spaces. However, the process will be aborted if it requires more memory space than what is available on the target IC. In that case, the user will have to replace the XDPL8210 chip with a new one in order to burn the configuration.

  Table 9 shows the recommended procedures for using the burn configuration function in .dp Vision to burn a first full set of parameters or patch the parameters into the OTP memory.

Table 9 Burn configuration procedures

Step	Instruction
I	Open configuration file using .dp Vision (see example in **Figure 33**).
II	If necessary, change any parameter value (see example in **Figure 34**), then click [File] >> [Save] or [File] >> [Save as] to save the configuration file. Otherwise, proceed to step III.
III	Ensure that the primary supply voltages (e.g. AC input) to the board are switched off or disconnected, and the hardware connection for configuration is OK based on **Figure 32**.
IV	Click  to supply power and establish a connection to the target XDPL8210. After this step, XDPL8210 will be in configuration mode (with V_{CC} voltage for OTP programming at 7.5 V ± 0.15 V) and the device status  should change to .
V	Click  to burn the configuration to the target XDPL8210. After this step, you should see a pop-up window, which is similar to one of those below.  
VI	Click “Proceed” or “Yes” to burn/patch the configuration. After this step, a pop-up window should show that the burning/patching is successful.
VII	Click “OK” on the pop-up window, then disconnect the programming cable from the XDPL8210 configuration connector and test the application, if needed.

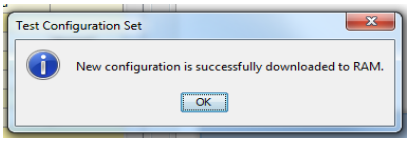
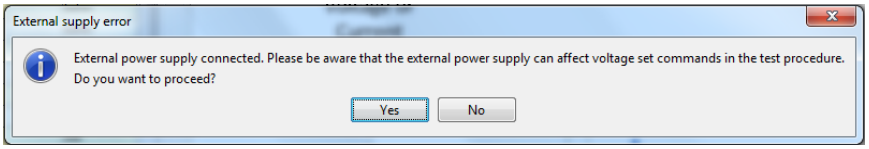
– Test configuration

This function will download the parameter values from the list in .dp Vision into the XDPL8210 RAM, followed by an automatic IC start-up, for application testing with the new configuration.

Unlike using the burn configuration, parameter configuration with this option is not permanent because the loaded RAM contents will be lost once the IC supply voltage is turned off, but the advantage of using this option is that it does not consume OTP memory space, thus there is no limit on the number of parameter value changes.

Table 10 shows the recommended procedures for using test configuration functions in .dp Vision to load the new parameter values to the RAM and test the application with the new configuration.

Table 10 Test configuration procedures

Step	Instruction
I	Open the configuration file using .dp Vision (see example in **Figure 33**).
II	Ensure that the primary supply voltages (e.g. AC input) to the board are switched off and the hardware connection for configuration is OK based on **Figure 32**.
III	If necessary, change any parameter values (see example in **Figure 34**). Otherwise, proceed to step IV.
IV	Click  to supply power and establish a connection to the target XDPL8210. After this step, XDPL8210 will be in configuration mode and the device status  should change to .
V	Ensure the board test set-up (e.g. output load) is OK, then apply the AC input to the board. After this step, the board does not start up because XDPL8210 is still in configuration mode.
VI	Click  to test the new configuration with the target XDPL8210.
VII	If the IC automatically starts up with the new configuration, you should see a pop-up window like the one shown below. Click “OK” to proceed.  *Note: If there is any protection being triggered after step VI, the pop-up window would show that the test configuration is unsuccessful instead; please refer **Section 20.1** for firmware status code read-out in debug mode.*
VIII	To test another configuration change, repeat steps II to VII. If the following message box appears in between the steps, click “Yes” to proceed.  Otherwise, turn off the AC input and disconnect the programming cable from the XDPL8210 configuration connector.

Note: If any error occurs during the burn configuration or test configuration procedures, please refer to the message bar of .dp Vision for the error description. For more details, please refer to the .dp Vision user manual.

19 Fine-tuning guide

This section presents guidelines for how to fine-tune the value of a few essential XDPL8210 parameters, based on the actual measurement waveform or data.

19.1 Input voltage-sensing parameter fine-tuning

When the primary MOSFET is switched on, the XDPL8210 measures the current flowing out of the ZCD pin $-I_{IV}$, to estimate the DC-link filter capacitor voltage $V_{DC,filter}$.

Ideally, $V_{DC,filter}$ should be a low-frequency (e.g. typically 100 Hz ~ 120 Hz) rectified sinusoidal waveform, as shown in **Figure 35**, where the peak value of $V_{DC,filter}$ is equal to AC input peak value $V_{in,peak}$, and the estimated input voltage V_{in} in rms value is assumed to be 0.707 times $V_{in,peak}$. However, due to the input line filter impedance and the filter capacitor ESR, the actual $V_{DC,filter}$ has high switching frequency ripple (in the kHz range) over the low-frequency sinusoidal waveform, whose ripple peak-to-peak voltage level varies based on the peak current being drawn by the transformer primary main winding. Step III of **Table 11** shows an example of the actual $V_{DC,filter}$ waveform.

To improve the input voltage estimation accuracy, R_{in} parameter fine-tuning is important for the IC to estimate the correct $V_{in,peak}$ by compensating for such switching frequency ripples, which appears in $-I_{IV}$ measurements as well.

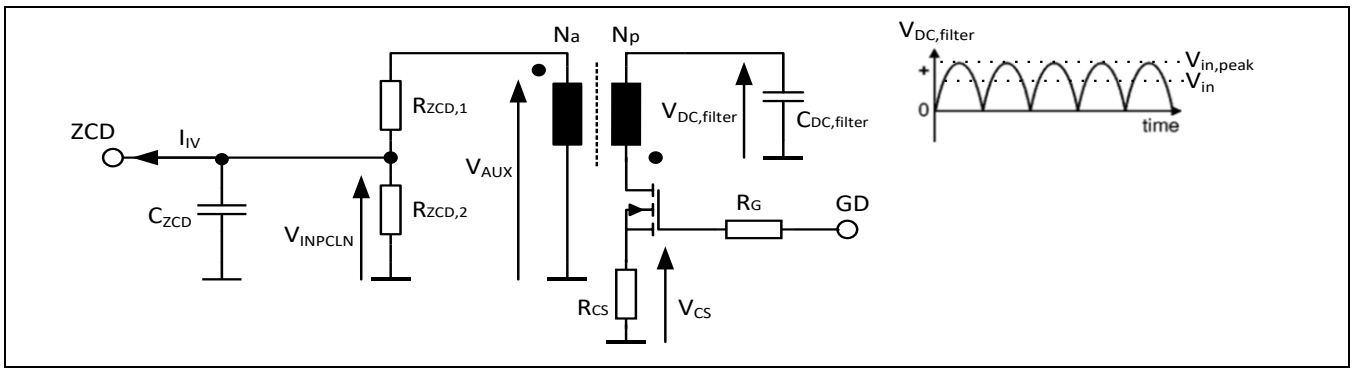
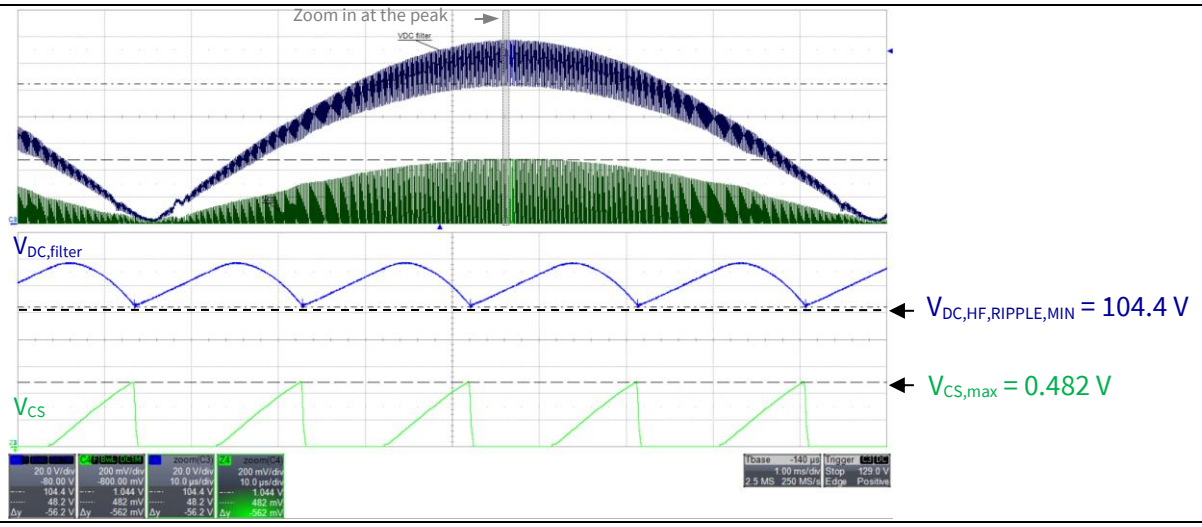


Figure 35 $-I_{IV}$ measurement for input voltage sensing

Table 11 shows the recommended procedures for R_{in} parameter fine-tuning.

Table 11 Recommended procedures for R_{in} parameter fine-tuning

Step	Instruction
I	Apply two voltage probes on the board, which respectively measure the waveform of the DC-link filter capacitor voltage $V_{DC,filter}$ and CS pin voltage V_{CS}.
II	Ensure the target XDPL8210 has already been burned with at least a first full set of parameters. Power up the board with normal operational minimum AC input voltage $V_{AC,min}$ and full-load output. If it cannot be powered up, retry by burning the input UVP to enable switch parameter $EN_{UVP,In}$ as "Disabled" (if it was not before) or refer to **Section 19.4** for the debugging guide.
III	Capture the voltage waveform with a time base of 1 ms and zoom into the peak voltage for measuring the minimum level of the $V_{DC,filter}$ high-frequency voltage ripple ($V_{DC,HF,RIPPLE,MIN}$) and the maximum level of V_{CS} ($V_{CS,max}$). Below is an example of a waveform captured on the 35 W reference design with $V_{AC,min}$ = 90 V_{rms}, F_{line} = 60 Hz and LED load voltage at around $V_{LED,at,I,pri(pk),max}$ = 42.17 V, under non-dimming condition.

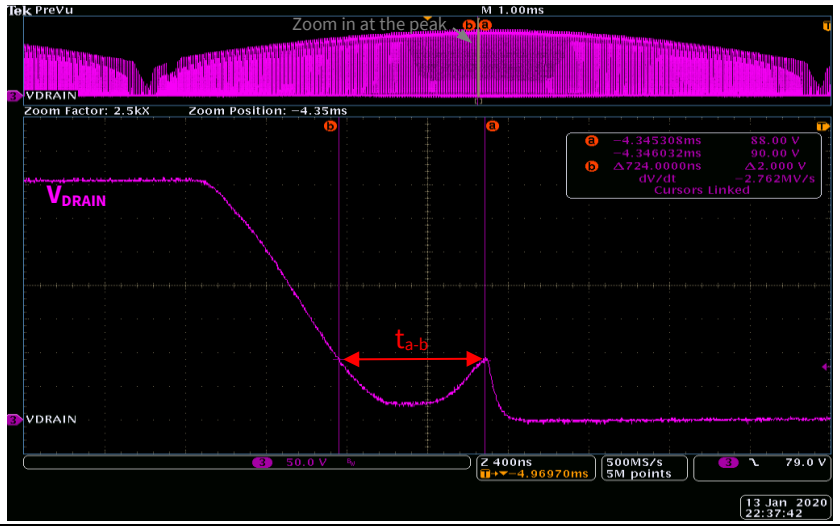
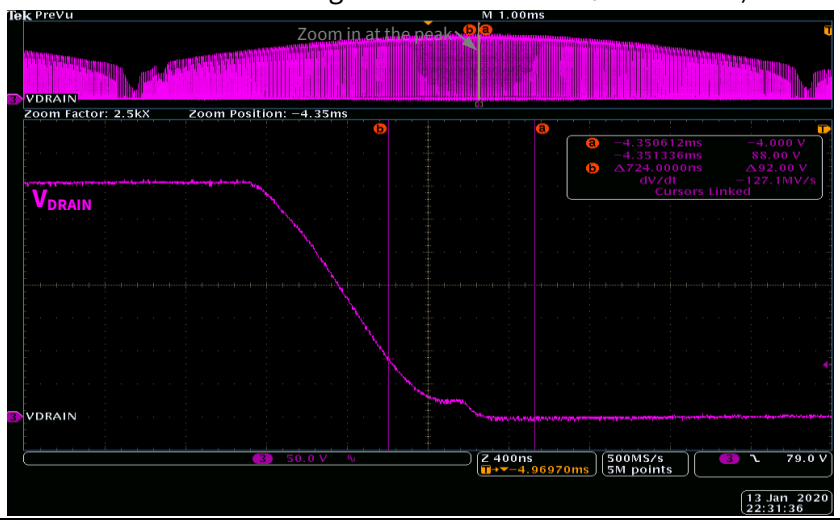
	
IV	Turn off the AC input. Calculate R1 with the equation below and voltage measurements from step III: $R1 = R_{CS} \cdot \left(\frac{\sqrt{2} \cdot V_{AC,min} - V_{DC,HF,RIPPLE,MIN}}{V_{CS,max}} \right)$, based on $V_{LED,at,I,pri(pk),max}$ and non-dimming. Calculation example based on 35 W reference design with $V_{AC,min}$ = 90 V_{rms}, F_{line} = 60 Hz and LED load voltage at around $V_{LED,at,I,pri(pk),max}$ = 42.17 V, under non-dimming condition. $R1 = 0.22 \cdot \left(\frac{\sqrt{2} \cdot 90 - 104.4}{0.482} \right) = 10.43\ \Omega$
V	Repeat step III to obtain another measurement of $V_{DC,HF,RIPPLE,MIN}$ and $V_{CS,max}$ based on $V_{LED,min,non-dimmed}$.
VI	Turn off the AC input. Calculate R2 with the equation below and voltage measurements from step V: $R2 = R_{CS} \cdot \left(\frac{\sqrt{2} \cdot V_{AC,min} - V_{DC,HF,RIPPLE,MIN}}{V_{CS,max}} \right)$, based on $V_{LED,min,non-dimmed}$ and non-dimming. Calculation example based on 35 W reference design with $V_{AC,min}$ = 90 V_{rms}, F_{line} = 60 Hz and LED load voltage at around $V_{LED,min,non-dimmed}$ = 18 V, under non-dimming condition. $R2 = 0.2 \cdot \left(\frac{\sqrt{2} \cdot 90 - 114.6}{0.326} \right) = 8.54\ \Omega$
VII	Calculate the fine-tuned R_{in} parameter value with the following equation: $Fine\ tuned\ R_{in} = 0.5 \cdot (R1 + R2) + R_{ds(on),25°C} + R_{dc,pri,winding} + R_{CS}$ Where $R_{ds(on),25°C}$ is the MOSFET drain-source on-resistance at 25°C, and $R_{dc,pri,winding}$ is the primary main winding DC resistance. Calculation example based on 35 W reference design: $Fine\ tuned\ R_{in} = 0.5 \cdot (10.43 + 8.54) + 0.9 + 0.4 + 0.22$ $\boldsymbol{Fine\ tuned\ R_{in} \approx 11.0\ \Omega}$
VIII	Use the burn configuration in .dp Vision to patch the R_{in} parameter with the value from step VII and also enable the $EN_{UVP,In}$ parameter (if it was set to “Disabled” before). Then, verify the AC input UVP accuracy at full load and low load.

19.2 QR valley switching parameter fine-tuning

Unlike conventional analog solutions which achieve QR valley switching by introducing an external hardware delay on the zero-crossing signal with the ZCD pin capacitor, the XDPL8210 ZCD pin capacitor is mainly used for noise filtering only. Therefore, a fixed capacitor value, e.g. 47 pF, can be used across different power classes. To achieve QR valley switching, the XDPL8210 dynamically measures the resonant period and delays the MOSFET switch-on by a quarter of the resonant period after zero-crossing of the primary auxiliary winding voltage.

t_{ZCDPD} parameter fine-tuning is, however, necessary to compensate for XDPL8210 internal propagation delay in ZCD and also external delay caused by the noise-filtering capacitor at the ZCD pin. **Table 12** shows the recommended procedures for t_{ZCDPD} parameter fine-tuning.

Table 12 Recommended procedures for t_{ZCDPD} parameter fine-tuning

Step	Instruction
I	Apply a differential probe on the board to measure the Flyback MOSFET drain voltage waveform.
II	Set the t_{ZCDPD} parameter to 0 and use the test configuration function in .dp Vision to power up the board with low AC input voltage, e.g. 120 V_{rms}, and full-load output. If the board cannot be powered up, please refer to **Section 19.4** for the debugging guide.
III	Capture the waveform with a 1 ms time base and zoom into the voltage peak.
IV	Place a horizontal cursor at the highest possible level which crosses two points on the resonance part of the waveform (see a and b below), and measure the time between them (t_{a-b}). In the example below, which is based on the 35 W reference design, t_{a-b} is measured to be approximately 720 ns. 
V	Set the t_{ZCDPD} parameter as approximately half of t_{a-b} and burn the configuration with .dp Vision.
VI	Disconnect the programming cable after burning, then power up the board and the Flyback MOSFET drain voltage waveform should be switching at the first valley (see example below based on the 35 W reference design with **fine-tuned t_{ZCDPD} = 360 ns**). 

19.3 Output current regulation parameters fine-tuning

Please note that QR valley switching parameter (t_{ZCDPD}) fine-tuning in **Section 19.2** should be done before output regulation parameters fine-tuning.

The t_{PDC} parameter is used to compensate for the propagation delay from one end of the XDPL8210 GD pin gate pulse until the MOSFET drain current reaches zero, so that the accurate primary peak current can be estimated for better output regulation against input voltage variation.

The t_{zcddel} parameter is used to compensate for the propagation delay from one end of the XDPL8210 GD pin gate pulse until the ZCD pin voltage polarity change from negative to positive. The recommended initial t_{zcddel} is defined and calculated as:

$$Initial\ t_{zcddel} = t_{PDC} + \frac{C_{zcd} \cdot R_{zcd1} \cdot R_{zcd2}}{R_{zcd1} + R_{zcd2}} = t_{PDC} + \frac{47 \cdot 10^{-12} \cdot 56.2 \cdot 10^{3} \cdot 2.7 \cdot 10^{3}}{56.2 \cdot 10^{3} + 2.7 \cdot 10^{3}} \quad (46)$$

$$\boldsymbol{Initial\ t_{zcddel} = t_{PDC} + 120\ ns}$$

The $G_{out,loss}$ parameter is used to compensate for the output current reduction at minimum output current set-point. The recommended initial $G_{out,loss}$ is 0.

The $K_{coupling}$ parameter is to compensate for the non-ideal transformer primary-to-secondary peak current transfer ratio, so that the actual output current measurement matches the maximum output current set-point parameter, $I_{out,full}$. The recommended initial $K_{coupling}$ is 1.

Table 13 shows the recommended procedures for t_{PDC} parameter fine-tuning.

Table 13 Recommended procedures for t_{PDC}, t_{zcddel}, $K_{coupling}$ and $G_{out,loss}$ parameters fine-tuning

Step	Instruction
I	Calculate the corresponding initial t_{zcddel} values to be used for the t_{PDC} parameter fine-tuning. Based on equation (46), using the 35 W reference design as example, the corresponding initial t_{zcddel} values for t_{PDC} values of 150, 200, 250, 300 and 350 ns would be 270, 320, 370, 420 and 470 ns respectively.
II	Test the configuration using .dp Vision with the parameter $G_{out,loss}$ = 0 mS, $K_{coupling}$ = 1, t_{PDC} = 150 ns and the corresponding initial t_{zcddel} value calculated from step I (e.g. t_{zcddel} = 270 ns with t_{PDC} = 150 ns in this design example), to power up the board for non-dimmed output current measurement under the different conditions shown below: • Maximum AC input voltage ($V_{AC,max}$) and non power-limiting maximum LED voltage ($V_{LED,at,I,pri(pk),max}$) • Minimum AC input voltage ($V_{AC,min}$) and non power-limiting maximum LED voltage ($V_{LED,at,I,pri(pk),max}$) • Maximum AC input voltage (V_{AC_max}) and non-dimmed minimum LED voltage ($V_{LED,min,non-dimmed}$) • Minimum AC input voltage (V_{AC_min}) and non-dimmed minimum LED voltage ($V_{LED,min,non-dimmed}$) In this design example, $V_{AC,max}$ = 305 V_{rms}, $V_{AC,min}$ = 90 V_{rms}, $V_{LED,at,I,pri(pk),max}$ = 42.17 V and $V_{LED,min,non-dimmed}$ = 18 V are applied for the measurement. Please ensure there is no voltage probe connected to the board during the measurement. If it cannot be powered up in any condition above, please refer to **Section 20** for a debugging guide.
III	Calculate the total line, load regulation percentage based on the following equation: $\Delta I_{out,full} = \pm \left(\frac{I_{out,full,max} - I_{out,full,min}}{I_{out,full,max} + I_{full,min}} \times 100\ percent \right)$ Where: $I_{out,full,min}$ is the minimum full output current measured in the different conditions shown in step II. $I_{out,full,max}$ is the maximum full output current measured in the different conditions shown in step II.

IV	Repeat steps II to III with another four sets of t_{PDC} and initial t_{zcddel} from step I, to identify the set of t_{PDC} and initial t_{zcddel} which gives the lowest $\Delta I_{out,full}$. Take the 35 W reference design as an example, **t_{PDC} = 200 ns** and **initial t_{zcddel} = 320 ns** are selected.
V	Calculate $K_{coupling}$ based on the following equation: $K_{coupling} = 2 - \frac{2 \times I_{out,full}}{I_{out,full,max} + I_{out,full,min}}$ Where: $I_{out,full,max}$ is the maximum full output current measured in step II with the selected set of t_{PDC} and initial t_{zcddel} values from step IV. $I_{out,full,min}$ is the minimum full output current measured in step II with the selected set of t_{PDC} and initial t_{zcddel} values from step IV. $I_{out,full}$ is the full output current set-point in the XDPL8210 configuration. Taking the 35 W reference design as an example, **$K_{coupling}$ = 0.96** is calculated and selected.
VI	To optimize the line regulation at minimum output current set-point $I_{out,min}$, t_{zcddel} can be fine-tuned based on its initial value +20 ns per step. In this design example, the **fine tuned t_{zcddel} = 380 ns** is selected. For non-dimming application, this step can be skipped.
VII	Test the configuration using .dp Vision with the parameter $G_{out,loss}$ = 0 mS, $K_{coupling}$ value selected from step V, t_{PDC} value selected from step IV and t_{zcddel} value selected from step VI, to measure the load regulation at minimum output current set-point $I_{out,min}$, including: • $\Delta I_{out,min,at,V,AC,max}$ which denotes the output current change at maximum AC input voltage, when LED load voltage is changed from the maximum LED voltage $V_{LED,max,at,I,out,min}$ to the minimum LED voltage $V_{LED,min,at,I,out,min}$ at $I_{out,min}$. • $\Delta I_{out,min,at,V,AC,min}$ which denotes the output current change at minimum AC input voltage, when LED load voltage is changed from maximum LED voltage $V_{LED,max,at,I,out,min}$ to the minimum LED voltage $V_{LED,min,at,I,out,min}$ at $I_{out,min}$. In this design example, $V_{AC,max}$ = 305 V_{rms}, $V_{AC,min}$ = 90 V_{rms}, $V_{LED,max,I,out,min}$ = 42 V and $V_{LED,min,at,I,out,min}$ = 14 V are applied for the measurement. Please ensure there is no voltage probe connected to the board during the measurement. For non-dimming application, this step can be skipped.
VIII	Calculate $G_{out,loss}$ based on the following equation: $G_{out,loss} = \frac{\Delta I_{out,min,at,VAC,max} + \Delta I_{out,min,at,VAC,min}}{2 \cdot (V_{LED,max,at,I,out,min} - V_{LED,min,at,I,out,min})}$ Take the 35 W reference design as an example, **$G_{out,loss}$ = 0.38 mS** is calculated and selected. For non-dimming application, this step can be skipped.
IX	If necessary, fine-tune the minimum output current set-point $I_{out,min}$ to compensate for the offset between the actual typical minimum output current and the set-point. For example, if the actual typical minimum output current is 2 mA higher than the set-point, then $I_{out,min}$ parameter can be reduced by 2 mA. For non-dimming application, this step can be skipped.

19.4 Input power quality-related parameter fine-tuning

The enhanced PFC feature can be enabled by configuring the C_{EMI} parameter above zero and fine-tuning the value to compensate for the current displacement effect, which is mainly caused by the DC-link filter capacitor. A higher C_{EMI} parameter value gives higher compensation and vice versa.

The recommended starting value of the C_{EMI} parameter is the value of the DC-link filter capacitor $C_{DC,filter}$ placed after the bridge rectifier. If necessary, fine-tune the C_{EMI} parameter using the test configuration function in .dp Vision, to achieve the optimized power factor and iTHD. For example with the XDPL8210 35 W reference design,

the initial C_{EMI} based on $C_{DC,filter}$ is 0.22 μF for powering up of the board, and the **fine-tuned C_{EMI} = 0.1 μF** parameter is then selected for performance optimization.

In QRM1, the maximum switching frequency parameter $f_{sw,max}$ affects the number of first valley switching pulses over every AC input half-sine-wave period. To lower the iTHD at high input voltage and high output power, the number of first valley switching pulses can be reduced by lowering $f_{sw,max}$. However, please note that the efficiency could be reduced if the number of first valley switching pulses is reduced.

20 Debugging guide

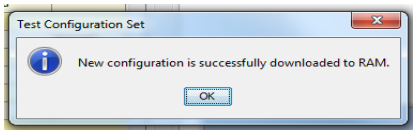
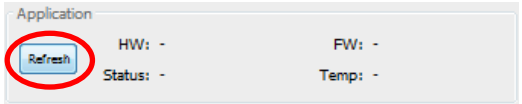
This section presents guidelines for system debugging if the board has any problems with powering up or shutting down during testing.

20.1 Firmware status code read-out procedures with debug mode

For further debugging, the XDPL8210 debug mode can be activated to read out the firmware status code, to identify which protection has been triggered. **Table 14** shows the recommended procedures for firmware status code read-out in debug mode.

*Note: The $Debug_{Mode}$ parameter should only be enabled for debugging purposes along with the configuration set-up connection shown in **Figure 32**. For stand-alone board testing without connecting the .dp Interface Gen2, please ensure the $Debug_{Mode}$ parameter is set to Disabled.*

Table 14 Procedures for firmware status code read-out in debug mode

Step	Instruction
I	Open the configuration file (see the example in **Figure 33**) used in the system which has the problem of powering up or shutting down, then set the $Debug_{Mode}$ parameter to “Enabled”.
II	Ensure that the AC input to the board is switched off and that the hardware connection for configuration is OK based on **Figure 32**, plus a low-ESR ceramic capacitor of 1 nF soldered across the UART pin and ground for noise decoupling.
III	Click  to supply power and establish connection to the target XDPL8210. After this step, the XDPL8210 will be in configuration mode and the device status  should change to .
IV	Supply the board with AC input and output conditions, which trigger the problem. After this step, the board does not start up because XDPL8210 is still in configuration mode.
V	Click  to test the configuration with the target XDPL8210. After this step, the IC will automatically start up in debug mode and you should see a pop-up window like the one shown below.  If any protection is triggered, the IC’s GD pin will stop switching and the output will stay low.
VI	Click “OK” in the pop-up window.
VII	Click the “Refresh” button in the .dp Vision application section and switch off the AC input. After this step, the firmware status code is read out. If any protection has been triggered after step V, the status code will show a value in red. Otherwise, it will show 0x0000 in black. 
VIII	Hover the mouse over the status code and the description of the status code will be shown. For example, 0x0040 means input UVP has been triggered.
IX	Apply the necessary counter-measure or repeat the steps above to debug again. Otherwise, ensure the AC input is switched off before disconnecting the programming cable from the XDPL8210 board.

21 References

[1] XDPL8210 datasheet

[2] REF-XDPL8210-U35W engineering report

Revision history

Document version	Date of release	Description of changes
V1.0	2019-07-07	Initial version
V1.1	2020-02-13	Recommend C_{dim} value changed from 220 nF to 22 nF
V1.2	2021-07-01	Removed DC input related text Updated .dp Vision download link
V1.3	2022-08-09	Corrected text from "A_e = 120.1 mm²" to "A_e = 62 mm²" in **Section 4** Corrected text from "PQ26/20" to "PQ20/20" in **Section 4** Updated link to CDM10VD in **Section 1** Updated links in the **References Section**

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Edition 2022-08-09

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
DG_2001_PL21_2002_115501

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