Design guide for adaptor with XDP™ digital power XDPS21081

About this document

Scope and purpose

This is a design guide to help customers design a 65 W USB-PD adaptor with Infineon's latest ZVS digital controller XDP™ digital power **XDPS21081**. It provides guidelines for power stage design, IC parameter settings, PCB layout and .dp Vision GUI usage.

Intended audience

This document is intended for power supply engineers who need to design adaptors with Infineon's digital control ZVS IC, XDP™ digital power **XDPS21081**. It also provides an insight into making a highly efficient transformer design with understanding of the loss mechanism.

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1 Abstract

Infineon's digital controller XDP™ digital power **XDPS21081** is a multiple-mode zero voltage switching (ZVS) controller for a flyback converter, QR operation for low-line input, forced quasi-resonant (FQR) ZVS operation for high-line input. This design guide provides information on the ZVS principle of the flyback converter as well as related parameter settings. It gives a step-by-step design for power stage components with given specifications of a typical 65 W USB-PD adaptor design. The design equation can also be extended to other power ratings. Installation and usage of a graphical user interface (GUI) – .dp Vision – are covered, and customers will learn how to set IC parameters through the digital interface.

2 Introduction

2.1 IC introduction

The **XDPS21081** [1] is a ZVS flyback current mode controller with built-in HV start-up cell. The start-up cell makes the IC power supply much more efficient and flexible during no-load operation. The DSP in the controller is like the brain of the chip, making the controller much smarter than a conventional mixed-signal hardware chip. The IC selects the most efficient operation mode depending on line input. For low-line input, it enables QR mode, and natural quasi-ZVS is achieved without current injection, reducing power loss. For high-line input, it transfers to FQR ZVS mode, implemented by self-generated resonant oscillation. With medium or light load, it enables frequency reduction mode and configurable burst mode power to get the best efficiency across line and load regulation. In addition, a one-time programmable (OTP) unit is integrated to provide a wide set of programmable parameters to ease the design-in phase.

2.2 Pin configuration and description

The pin configuration is shown in **Figure 1** and **Table 1**.

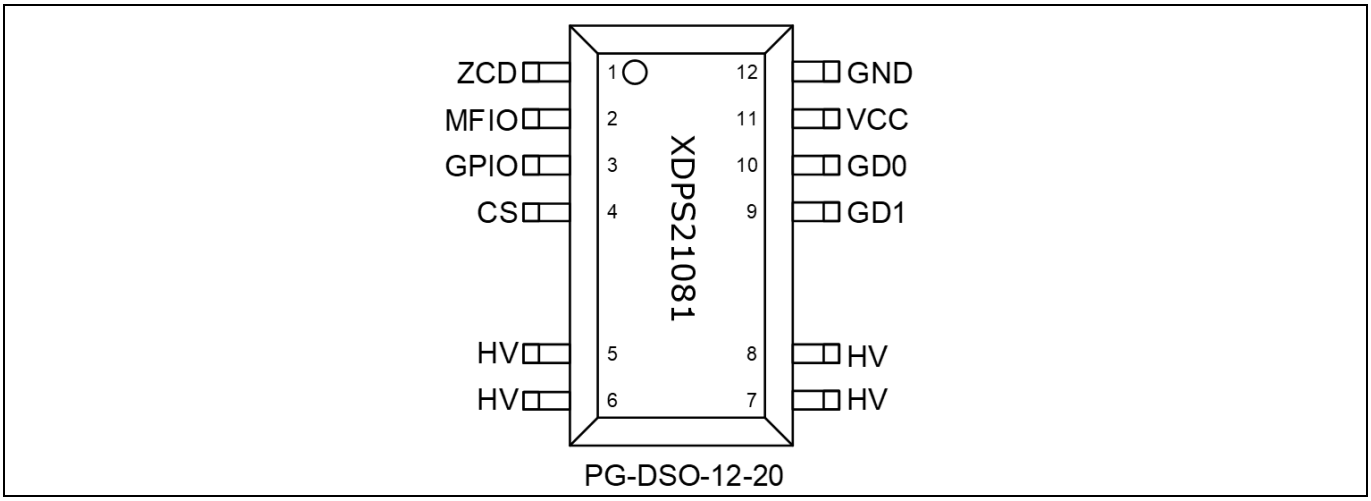


Figure 1 Pin configuration

Table 1 Pin definitions and functions

Symbol	Pin	Type	Function
ZCD	1	I	**Zero crossing detection** The ZCD pin is connected to an auxiliary winding for zero crossing detection, positive pin voltage measurement and also to insert V_{CS} offset based on output voltage.
MFIO	2	I	**Multifunctional input output** The MFIO pin is connected to an optocoupler that provides an amplified error signal for PWM mode operation.
GPIO	3	IO	**Digital general-purpose input output** The GPIO pin provides a UART interface until brown-in. It is switched to weak pull-down mode, and UART function is disabled during normal operation.
CS	4	I	**Current sense** The CS pin is connected via a resistor in series to an external shunt resistor and the source of the power MOSFET.
HV	5, 6, 7, 8	I	**High voltage input** The HV pin is connected to the rectified bulk voltage. An internally connected 600 V HV start-up cell is used for initial V_{CC} charge. Brown-in and brown-out detection are also provided.
GD1	9	I	**FQR ZVS signal gate driver output** The GD1 pin provides a gate driver pulse signal to initiate FQR ZVS mode operation.
GD0	10	O	**Gate driver output** Output for directly driving the main power MOSFET.
V_{CC}	11	I	**Positive voltage supply** IC power supply.
GND	12	O	**Power and signal ground**

2.3 Product highlights

- Integrated 600 V start-up cell for fast start-up and direct bus voltage sensing
- Adaptive CS compensation for USB-PD
- FFR mode
- High-precision line and load regulation
- Primary-side output overvoltage protection (OVP)
- Supports lowest no-load standby power
- One-pin UART interface for configuration

2.4 Simplified application diagram

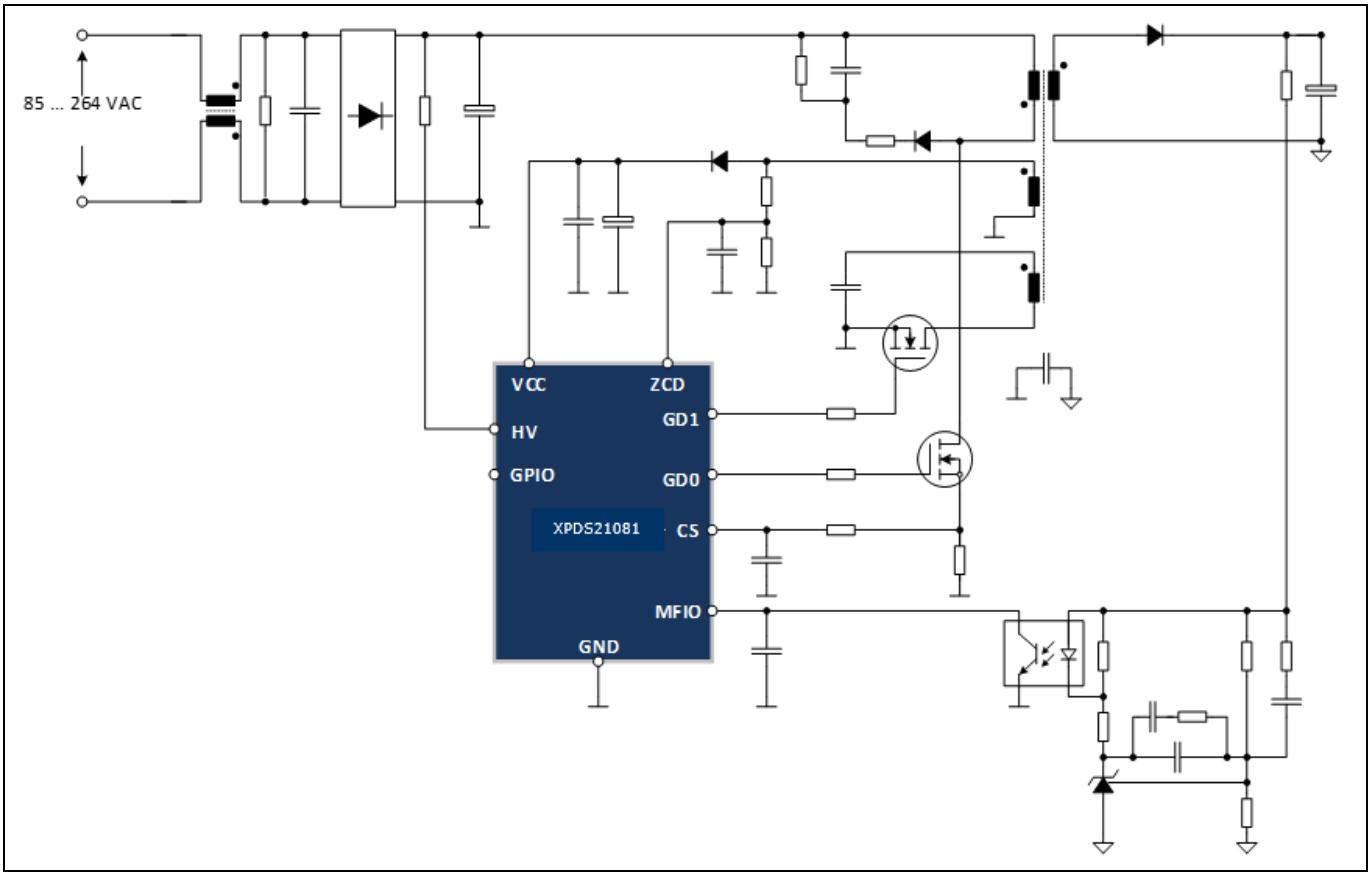


Figure 2 Simplified application diagram

2.5 ZVS principles

Figure 3 shows the typical PWM sequences and related key waveforms for the ZVS flyback.

After the primary MOSFET turns off at t_0, the synchronous rectifier (SR) MOSFET will turn-on, delayed by a short blanking time. At t_1, the SR MOSFET turns off when the demagnetizing current ideally goes to zero, then the magnetizing inductance L_p and C_{eqv} will oscillate. The voltage of the primary MOSFET will oscillate from $V_{bulk+Vref}$ to $V_{bulk-Vref}$. If the auxiliary MOSFET is turned on at t_2, the resonant peak of the primary MOSFET will mean the magnetizing current is zero, then the $i_{_mag}$ will build up as negative. During this controlled ZVS on-time, the V_{DS} of the primary MOSFET is clamped to $V_{bulk+Vref}$. Once the peak current reaches $i_{_zvs_pk}$, the aux MOSFET is turned off, and because this current is stored in the magnetizing inductance and in the reverse direction, it will continue to flow in this direction and discharge the energy stored in C_{eqv}. This time duration in the IC is controlled by the $t_{ZVSdead}$ parameter, which is configurable. So at t_4, the drain voltage of the primary MOSFET reaches its minimum, and turns on the primary MOSFET, which reduces the turn-on losses significantly, which is almost ZVS. As seen in the diagram, the energy is proportional to V_{bulk}, and so is the ZVS on-time.

ZVS pulse insertion is based on nano-DSP core and memory info. The IC knows the next switching cycle period and ZVS dead-time and ZVS pulse on-time, so the switching period minus these two parts will decide the ZVS pulse starting point, assuming the IC main gate turn-on time is also fixed. When the CS signal reaches the current command, the main gate off-point can also be decided.

Introduction

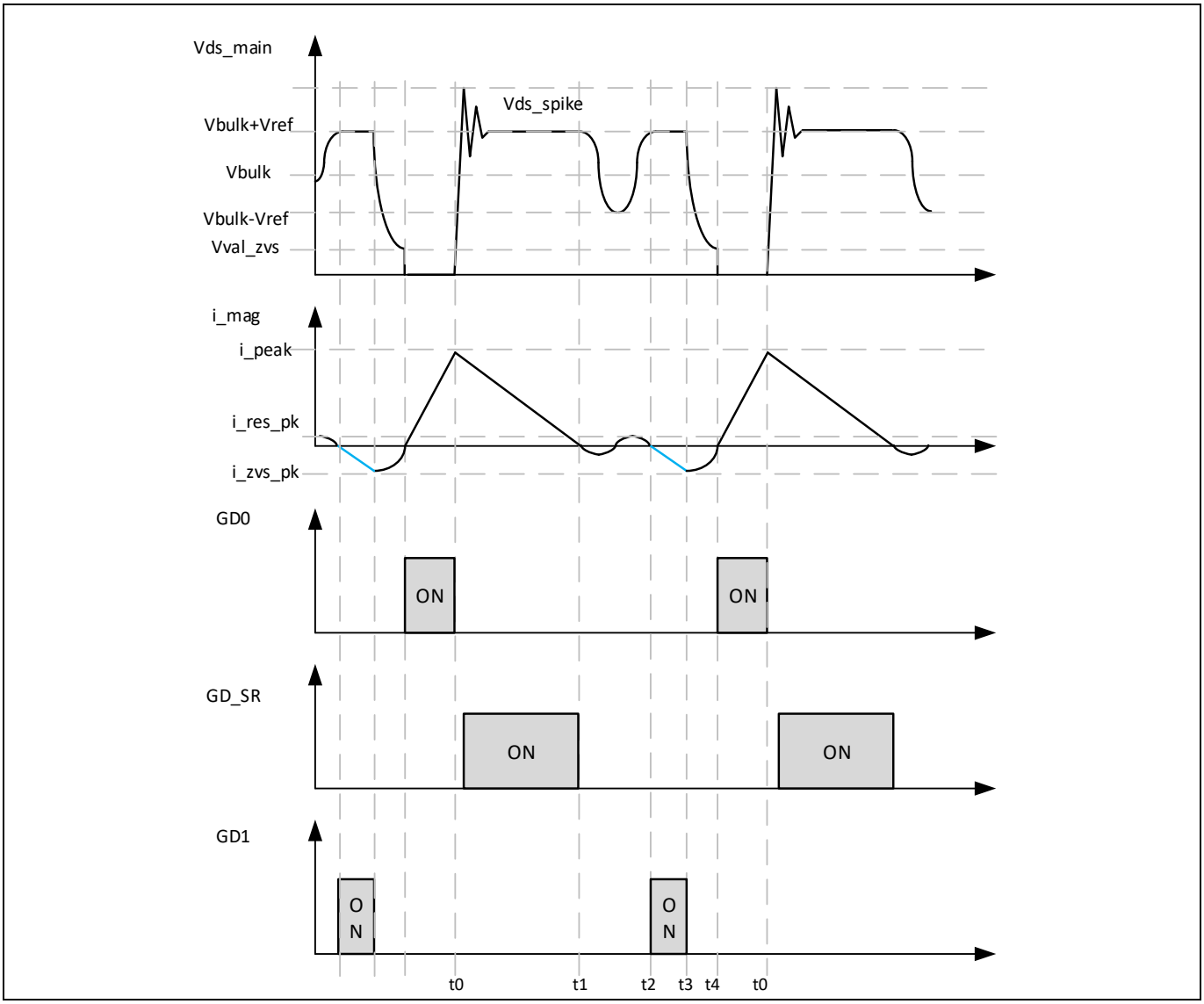


Figure 3 ZVS principles

3 Flyback power stage design

3.1 65 W adaptor system specifications

Table 2 shows the simplified system specs for the nominal 65 W adaptor. Only the key specs are included here to dimension the power train components such as the bulk capacitor, transformer and MOSFETs.

Table 2 65 W adaptor system specifications

Descriptions	Symbol	Value	Unit	Test conditions
Input AC voltage	V AC	90 to 264	V AC	
Input AC frequency	f_{line}	50/60	Hz	
Output voltage	V_{out}	5/9/12/15/20	V	
Output voltage ripple	ΔV_{out}	150	mV	From 5 V to 20 V under steady-state load
Nominal output current	I_{outnom}	3 3.25	A A	3 A for voltage below 20 V 3.25 A for 20 V output

3.2 Bulk capacitor selection

Figure 4 shows the typical waveforms after the rectification bridge with a large bulk capacitor. T1 is the conduction period of the rectifier bridge diode. During this timeframe, input AC voltage will charge the bulk capacitor, and the rest of the time is the discharging of the bulk capacitor. The difference between the energy stored in the bulk capacitor is equal to the output power times (T2 to T1).

The conducting period can be calculated using the following equation:

$$T_1 = T_2 \times \frac{\frac{\pi}{2} - sin^{-1}\frac{V_{bulkmin}}{V_{pk}}}{\pi} \quad (1)$$

Where T2 is the period of the rectified sine waveform, i.e. $T_{line}/2$, V_{pk} is the AC peak input voltage, and $V_{bulkmin}$ is the minimum voltage of the bulk capacitor.

The energy discharged from the bulk capacitor during the rectifier off-period is:

$$C_{energy} = 0.5 \times C_{bulk}\left(V_{pk}^2 - V_{bulkmin}^2\right) \quad (2)$$

This energy should be equal to the input power times of the off-period, so we get the following equation:

$$P_{out} \div \eta \times (T_2 - T_1) = C_{energy} \quad (3)$$

Using equations(1), (2)(1) and(3), with given line frequency and AC input voltage, either the value of the bulk capacitor or the minimum bulk voltage can be calculated once one variable is fixed.

Here we choose C_{bulk} 120 µF as an example, with the given power requirement in **Table 2**, giving the minimum bulk voltage shown in **Table 3**.

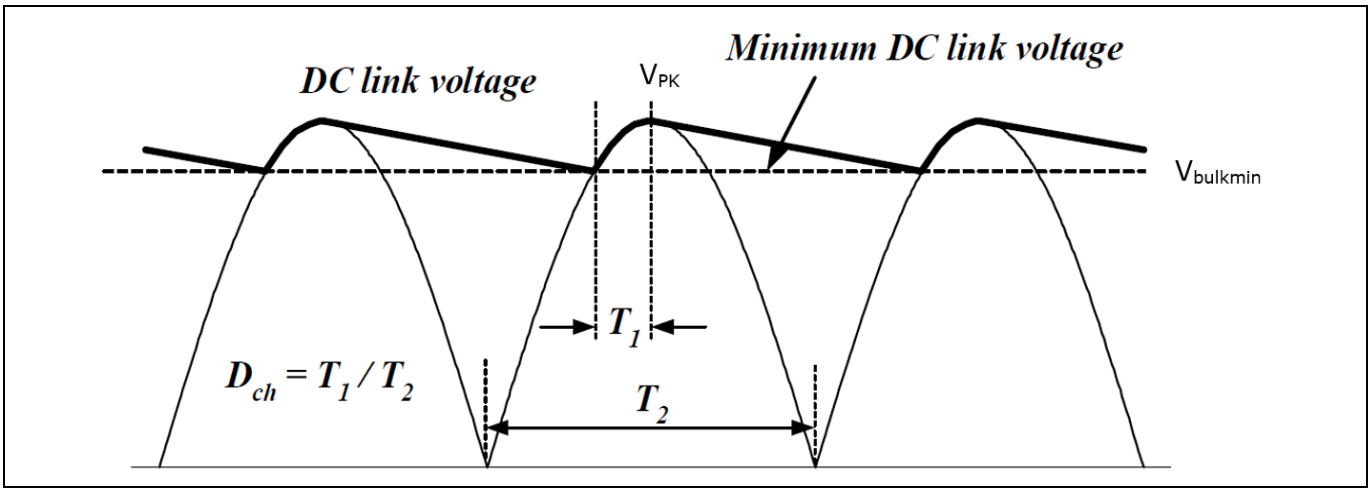


Figure 4 Bulk capacitor voltage after rectification

Table 3 V_{bulk} minimum voltage at max. load

V_{in} (V AC)	Freq. (Hz)	V_{out} (DC)	I_{out} (A)	P_{out} (W)	Eff. η	$V_{bulkmin}$ (DC)
90	47	20	3.25	65	0.94	85

Using 120 µF for the bulk capacitor value, the minimum V_{bulk} 85 V appears at 90 V AC/47 Hz with 3.25 A loading.

3.3 Transformer design

Now, with the minimum bulk capacitor voltage information at different AC-line/frequency and output power, we will be able to design the transformer of the flyback converter. According to the **XDPS21081** operation scheme, the system will operate at QR/boundary mode at low-line (90 V AC/47 Hz) at maximum 65 W. Since the gate drive signal is only available when zero crossing (ZC) is detected, during overload condition, the on-time will be increased and also the off-time, so switching frequency will be reduced. The transformer design will need to guarantee that flux density B_{max} is below saturation level while the wire size only caters for nominal power to handle the thermal issue.

Reference [2] shows how to design the inductance in critical mode operation. The relevant equations are (4) and (5).

$$L_p \cdot i_{pk} \left(\frac{1}{V_{bulk}} + \frac{1}{V_{refl}} \right) + 0.5 \cdot T_r = \frac{1}{f_{sw}} \quad (4)$$

$$0.5 \cdot L_p \cdot i_{pk}^2 \cdot f_{sw} \cdot \eta = P_{out} \quad (5)$$

Table 4 shows the calculated inductance will be 200 µH, and primary-side peak current is 3.05 A at 20 V/3.25 A output.

Table 4 Calculated inductance and peak current

F_{sw} (kHz)	T_r (µs)	V_{ref} (V DC)	V_{bulk} (V DC)	P_{out} (W)	η	L_p (µH)	I_{pk} (A)
75	1.6	112	85	65	0.94	200	3.05

Flyback power stage design

The next thing to do is decide the transformer turns based on the selected core shape/material, B_{max}. Core loss and copper loss are the main considerations here.

$$B_{max} = \frac{L_p \cdot i_{pk}}{N \cdot A_e} \quad (6)$$

Equation (6) shows the delta flux density or peak flux in DCM, where N is the primary turns of the transformer, and A_e is the effective flux area of the core.

Table 5 shows the peak current and maximum flux density under maximum load based on the selected PQ20/16 core.

Table 5 Peak current and B_{max} under different output voltages

V_{in} (AC)	P_{out} (W)	V_{out} (V)	V_{bulk} (V DC)	I_{pk} (A)	L_p (µH)	N_p	A_e (mm²)	B_{max} (T)
90	65	20	85	3.05	200	28	62	0.34

3.4 Output capacitor selection

One consideration when selecting the output capacitor value is based on the ripple requirement. The required ripple is 150 mV. The ripple has two parts: one is the current charge to the output capacitor; the other is dominated by the ESR of the capacitor. **Figure 5** shows the current charge output capacitor for the flyback converter.

Part 1 voltage ripple is calculated using the following equation:

$$\Delta V_{o_1} = \frac{\Delta Q}{C} = \frac{(Ipk_{sec} - I_o)^2 * I_o * T_{sw}}{Ipk_sec^2 * C} \quad (7)$$

Part 2 voltage ripple is calculated using the following equation:

$$\Delta V_{o_2} = esr \cdot I_{ac} = esr \cdot \sqrt{i_{pk}^2 - i_o^2} \quad (8)$$

Total output voltage ripple is the sum of ΔV_{o_1}+ ΔV_{o_2}.

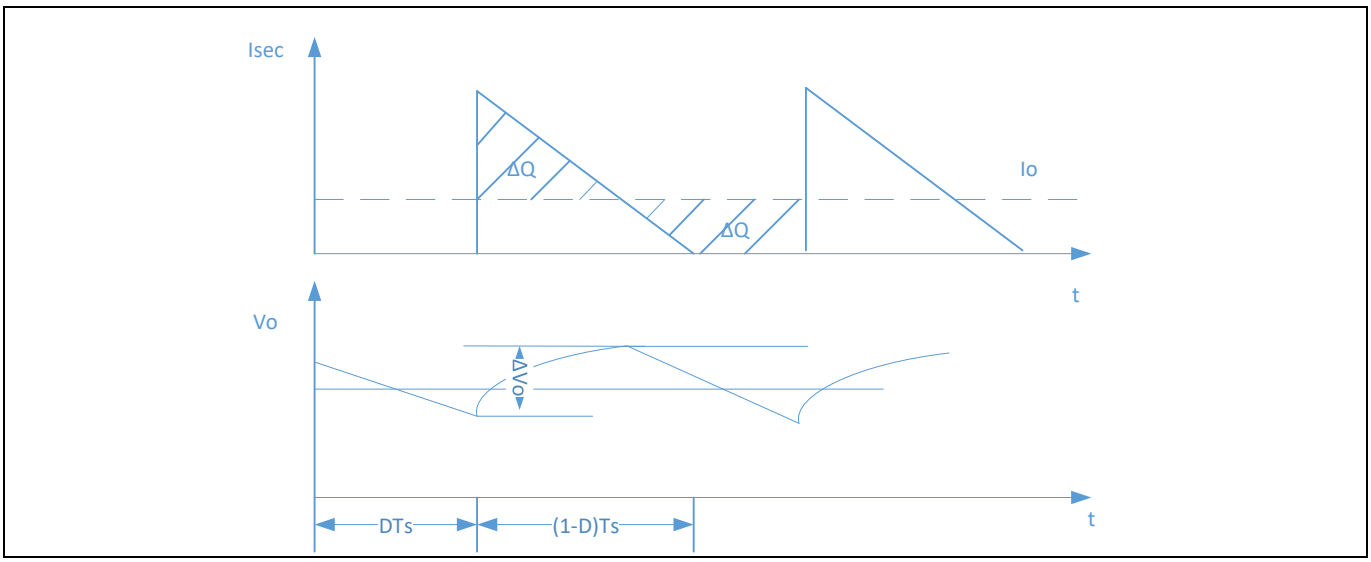


Figure 5 Output voltage ripple

Table 6 Output ripple calculation under 20 V/3.25 A

ΔV_{o_spec} (mV)	I_{pk_sec} (A)	T_{sw} (µS)	C (µF)	ΔV_{o_1} (mV)	ESR (mΩ)	I_{out} (A)	I AC (A)	ΔV_{o_2} (mV)
150	3.05 x 5.6	13.33	1222	23	More than 5	3.25	16.77	More than 84

Table 6 shows the total ripple is (23 + 84) = 107 mV, which meets the requirements. The selected output capacitors are polymer capacitors plus multiple-layer ceramic capacitors, two 470 µF/25 V polymer capacitors and six 47 µF/25 V multiple-layer ceramic capacitors.

3.5 MOSFET selection

3.5.1 Primary MOSFET

The superjunction MOSFET is the popular, HV discrete component used nowadays in AC-DC conversion. The latest **CoolMOS™ P7** [3] technology shows the best Q_G x $R_{DS(on)}$ figure-of-merit (FOM), and fast turn-off speed, which reduces the turn-off losses, so it is best suited to this design.

Based on the transformer design, the turns ratio is 5.6, so we can estimate the maximum voltage stress of the primary MOSFET based on the following equation. Derating is the most important consideration when selecting MOSFETs.

$$V_{ds} = V_{in} + V_{clamp}$$

So the maximum voltage rating during steady-state happens with maximum input RMS AC voltage, i.e. 264 V AC.

V_{DS} = 264 x 1.414 + V_{clamp}, with a 600 V MOSFET; the V_{clamp} should be kept below 227 V DC. This means properly dimensioning the snubber circuit is important, because the ZVS topology shown here will still have a turn-off spike caused by the energy in the leakage inductance.

The other selection consideration for the primary MOSFET is its $R_{DS(on)}$ value; usually conduction loss is the main concern at low-line, which is the worst case. A low $R_{DS(on)}$ MOSFET is preferred, but this means greater C_{oss}, and it also means more turn-on losses at high-line for conventional hard-switching or even QR flyback. With ZVS technology, we now can choose a low $R_{DS(on)}$ MOSFET to optimize the conduction losses while maintaining low losses at high-line.

As already known, different MOSFETs have different $R_{DS(on)}$ and Q_{oss} combinations, and Q_{oss} will need certain energy from the auxiliary winding to discharge it. Again, it is a trade-off between the losses gained and dissipated in term of system optimization.

Let us estimate the losses stored in the MOSFET junction capacitor at 230 V AC, considering the reflection voltage 112 V DC; the plateau of the primary MOSFET V_{DS} will be 230 x 1.414 + 112 = 437 V DC, while from the IPL60R185C7 datasheet C_{oss} curve, we find that from 400 V DC to 40 V DC, the E_{oss} change is (2.7 – 1.1) µJ, with 120 kHz switching frequency, which means power loss is E_{oss} x F_{sw} = 1.6 x 120 = 192 mW. We notice that from 40 V DC to zero, the E_{oss} is around 1.1 µJ, which means 132 mW is needed to discharge from 40 V to zero. So when considering efficiency, the optimum turn-on point for the primary MOSFET is not really zero voltage; it should be around 40~50 V DC for CoolMOS™.

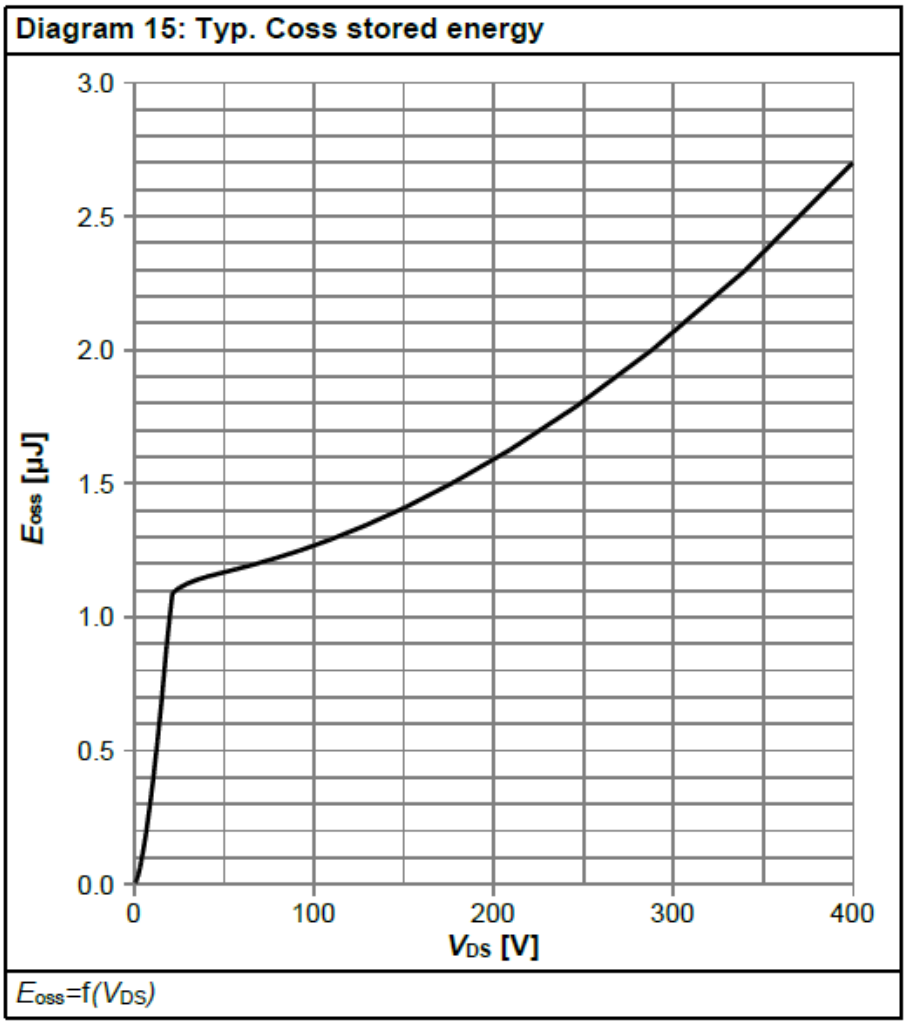


Figure 6 E_{oss} curve of IPL60R185C7

Based on these considerations, **IPL60R185C7** is chosen.

The conduction losses of the primary MOSFET at 20 V output and 3.25 A loading at 100°C junction temperature are:

$$P_{cond} = i_{rms}^2 \cdot R_{dson} = \left(\sqrt{D/3} \cdot i_{pk}\right)^2 \cdot R_{dson} = \left(\sqrt{0.53/3} \cdot 3.05\right)^2 \cdot 0.25 = 0.414W$$

3.5.2 ZVS MOSFET

The transformer has one additional winding at the primary. This winding provides the energy to discharge the primary MOSFET's equivalent C_{oss} by controlling the on-time of the ZVS MOSFET. The designed transformer has $N_{pz} = N_p:N_{ZVS} = 28:2$ turns ratio, so similarly the V_{DS} stress of this MOSFET can be calculated with $V_{inmax}/N_{pz} + V_{ZVS}$ = 374 V/14 + 8 V = 34.7 V. Considering the voltage spike, the voltage rating should be at least 60 V. Because this MOSFET only handles low energy, a small-signal MOSFET can be chosen. Here we choose **BSL606SN**.

3.5.3 SR MOSFET

The secondary-side SR MOSFET selected is the OptiMOS™ 5 series, considering the best FOM_{gd} and FOM_{oss}.

Based on the turns ratio N_{ps} = 28:5, the MOSFET rating will be 374 V/5.6 + 20 = 86.8 V. Due to the ZVS turns on the primary side, hardly any spike is seen at the output SR MOSFET in ZVS mode. So 100 V rating is chosen. Here we choose **BSC0802LS**.

The RMS current in the secondary SR MOSFET is: $i_{rms} = \sqrt{D_{off}/3} \cdot i_{pksec} = \sqrt{\frac{0.41}{3}} \cdot 3.05 \cdot 5.6 = 6.31A$

The conduction loss of the SR MOSFET is: $i_{rms}^2 \cdot R_{DS(on)} = 6.31^2 \cdot 0.0032\ \Omega = 0.127$ W

3.5.4 SR IC selection

When the ZVS pulse is turned on, the SR V_{DS} will also drop below zero voltage. It will tend to mistrigger the V_{DS} direct sensing SR IC, as shown in **Figure 7**. While using the voltage balance SR IC as shown in **Figure 8**, due to the SR arming function, there is no mis-triggering of the SR gate. For SR IC with direct sensing without arming function, the minimum on-time needs to be set to minimum, e.g., 50 ns, and the minimum on-time should be shorter than the primary ZVS on-time, otherwise shoot-through between primary and secondary will happen as soon as the primary main MOS turns on, then the primary MOS could be damaged. Here, it is worth mentioning CYPD3184, which is V_{DS} direct sensing SR IC plus PD protocol. Each time CYPD3184 drives the SR MOS, it will calculate the product of V_{DS}*T_{off} first, and it drives the SR MOS only if the calculated V_{DS}*T_{off} exceeds the setting threshold, so it can avoid mis-triggering the SR gate. Any other SR IC feature with calculation of V_{DS}*T_{off} is highly recommended.

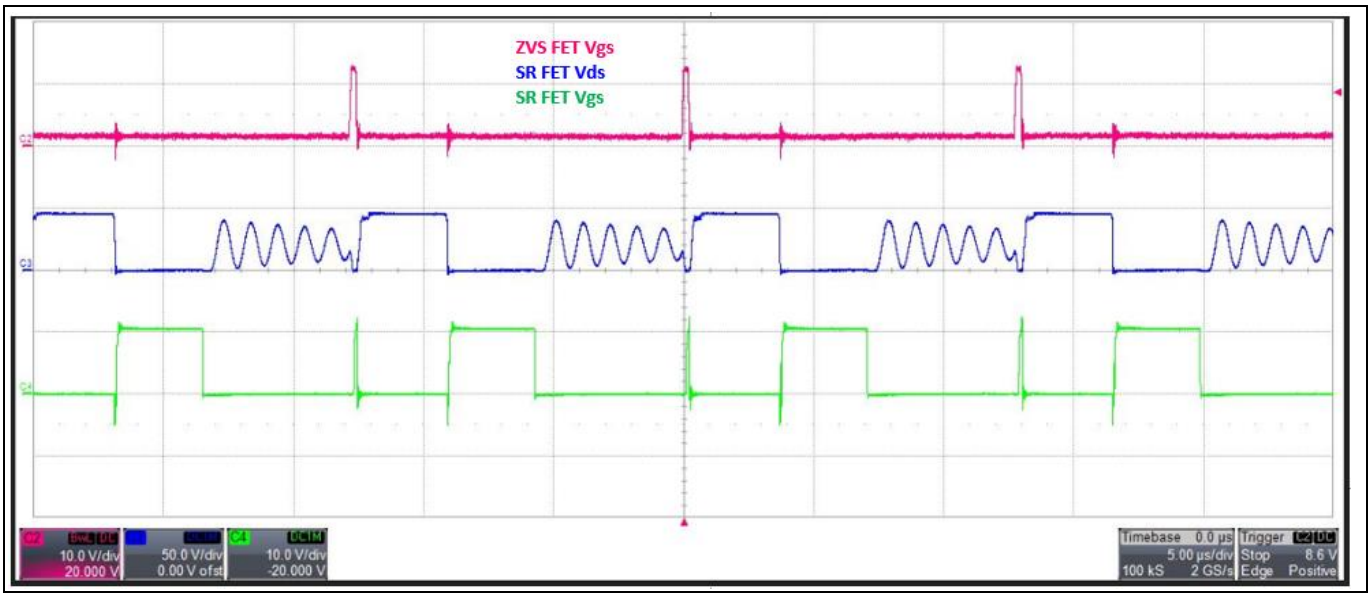


Figure 7 SR gate signal wit$_{ds}$ direct sensing SR controller

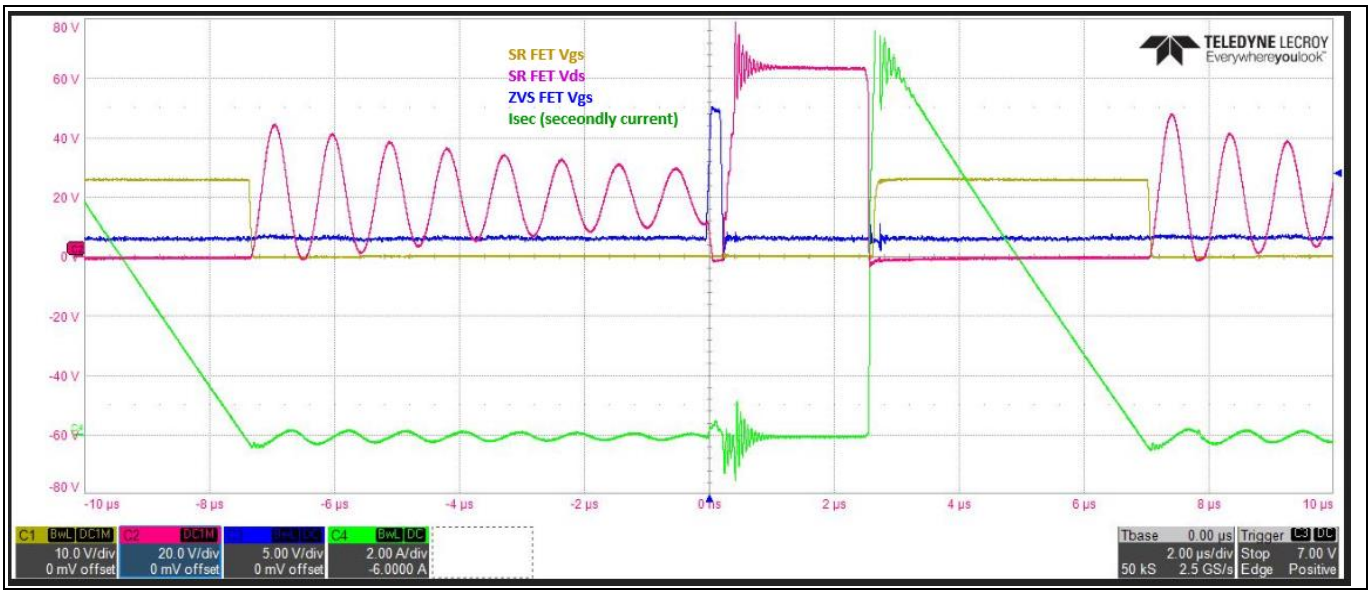


Figure 8 SR gate signal with voltage-second balance SR controller

3.6 Snubber circuit design

When the primary MOSFET turns off, the energy stored in leakage inductance will cause significant ringing at the drain node. This ringing must be clamped to keep the MOSFET within a safe operating range. A Zener clamp circuit as shown in **Figure 9** is chosen, as it has high efficiency at light load since the Zener clamp will never conduct, so there is no residual resistor loss compared to an RCD snubber. This is the snubber circuit used in the 65 W demo board. In general, the energy that goes into the snubber circuit is leakage inductance stored energy. Depending on the D1 type, the losses will be different. Due to the reverse recovery characteristic, the current entering the clamp capacitor can return to the output side, and part of the energy is recovered to the input or output.

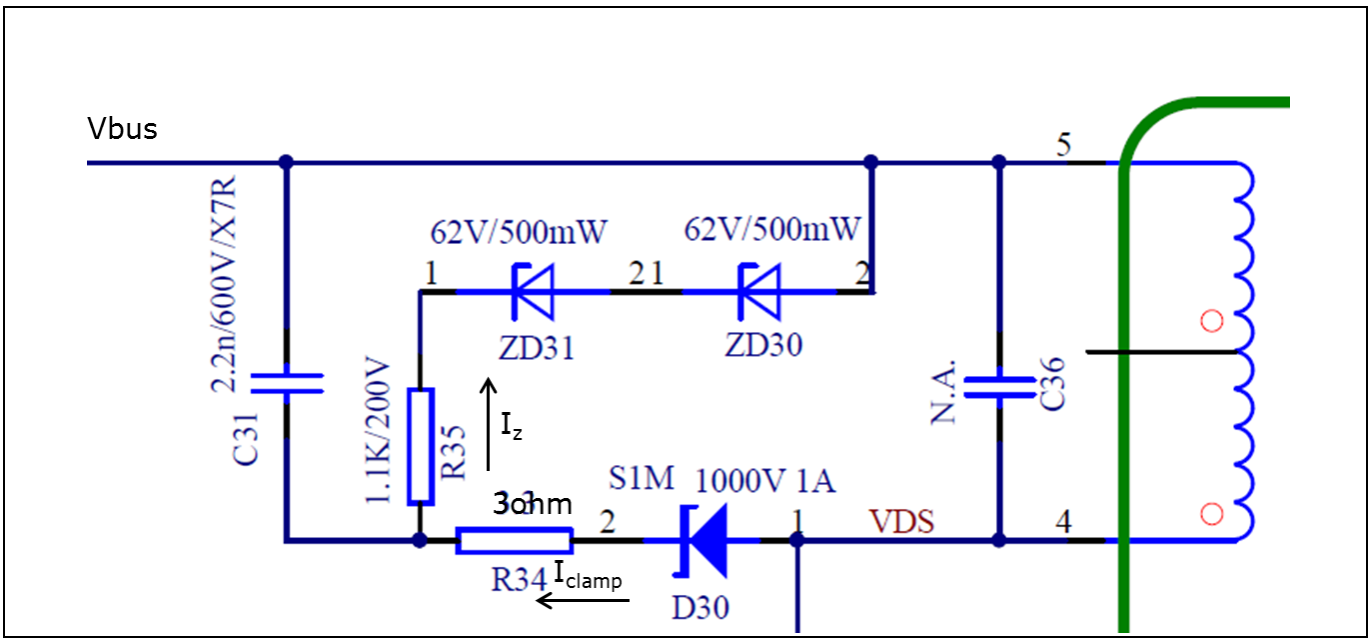


Figure 9 Snubber circuit

Flyback power stage design

Figure 10 and **Figure 11** show the snubber current and clamp voltage waveforms when the MOSFET turns off.

In reality, there is reverse recovery of the snubber diode, as shown in **Figure 10**, which means not all the current into the snubber capacitors is lost; the longer the recovery, the lower the losses that can be achieved.

Table 7 shows the calculation results of energy entering the snubber tank during turn-off, which is around 1.16 W. **Figure 10** also clearly shows that after the snubber diode current goes in the negative direction, the clamp voltage begins to decay.

This means not all the energy into the tank is lost, and the clamp voltage returns to the steady-state. Because the current returns to negative, the only way for this current path is to flow out of the dot terminal of the secondary-side transformer and partially to the output. So this energy is not fully dissipated.

Table 8 shows the losses in the Zener clamp, based on the measured waveforms. The power loss is calculated using 0.5 x I_z x V_{Zener_clamp} x duration x F_{sw}. It shows only 21 mW is dissipated in the Zener diode.

Table 7 Energy entering the snubber tank

V_{clamp_bottom} (V)	V_{clamp_peak} (V)	C_{clamp} (nF)	F_{sw} (kHz)	$P_{enter_snubber}$ (W)
123	151	2.2	137	1.16

Table 8 Power loss in the Zener diode

I_{Zener} (mA)	V_{Zener_clamp} (V)	Time (ns)	F_{sw} (kHz)	$P_{Zener_dissipate}$ (mW)
23	130	105	137	21

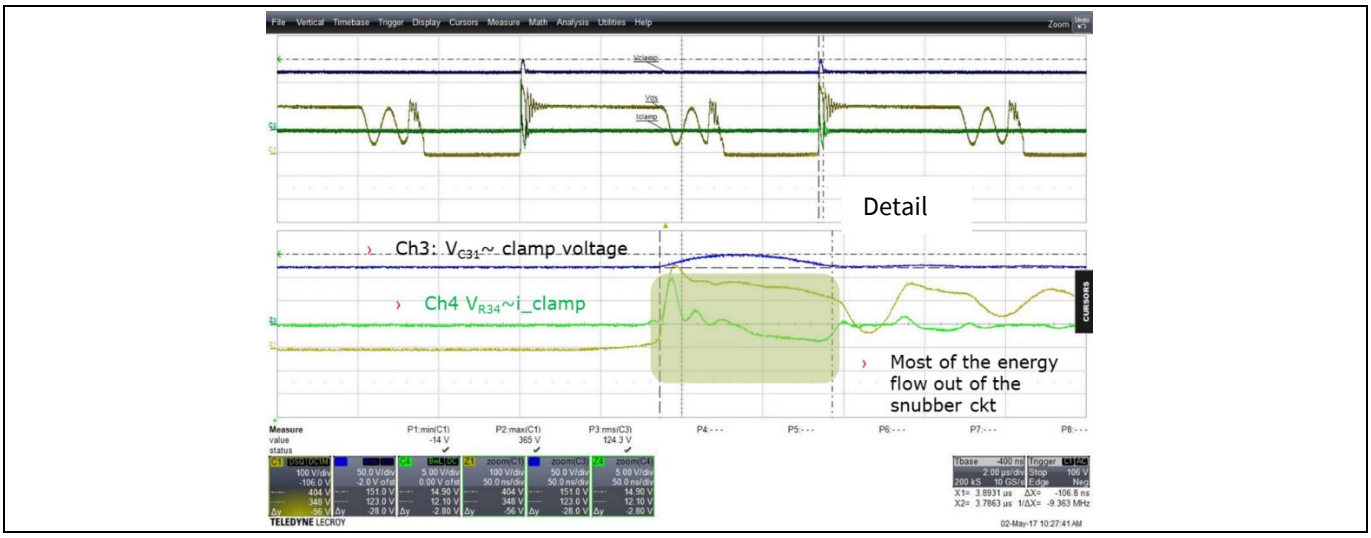


Figure 10 Snubber waveforms

Flyback power stage design



Figure 11 Snubber waveforms

4 Control diagram

Figure 12 shows the control diagram of **XDPS21081**.

The secondary-side control feedback signal feeds into the MFIO pin through the optocoupler, and this signal is sampled after leading-edge blanking (LEB) time every switching cycle and converted into a digital number by an 8-bit ADC, which takes around 1 µs. Based on this MFIO value, frequency and peak current will be picked up from the frequency law reference table. This value will be compared to the CS limit to see if maximum power is reached. If yes, after 31.3 ms blanking time, the IC will enter overload protection (OLP).

If not, the digital CS signal will be taken away from the V_{CS} offset, PDC correction, and feed into the 8-bit DAC to convert back to an analog signal. It compares with the CS shunt resistor to form the classical current mode control.

The V_{CS} offset value is calculated based on output voltage, which means the maximum usable current command will be different for variable output voltage, and therefore it will have different output power. For calculation details please refer to 5.2.2.

The propagation delay correction is to compensate for propagation delay influenced by the slew rate of the CS signal. For example, PDC = V_{in}/L_p x T_{delay}, where V_{bulk} is the bulk capacitor voltage, L_p is main inductance, and T_{delay} includes both IC internal (~100 ns) and external MOSFET turn-off delay. The detailed calculation can be found in 5.6.

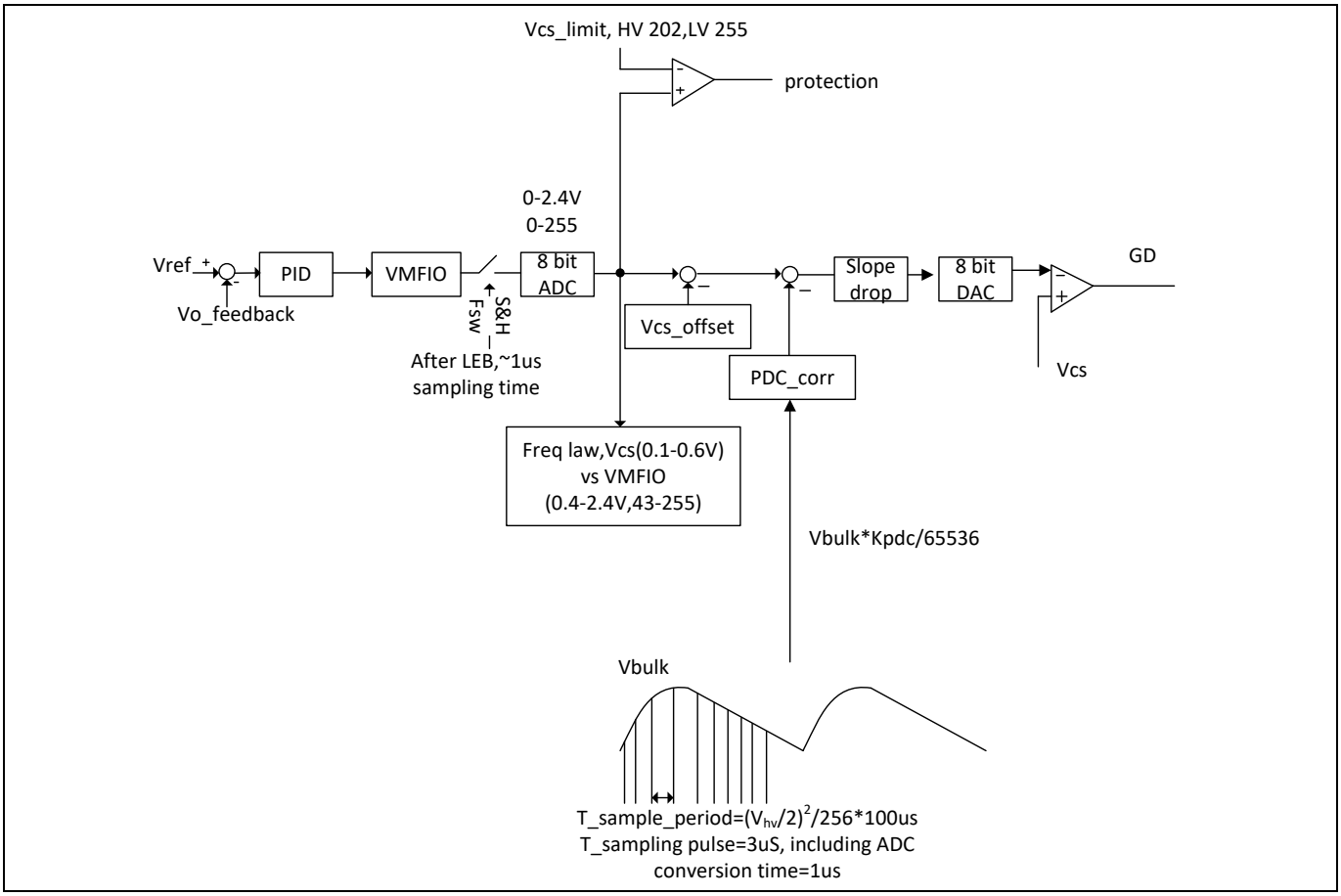


Figure 12 Overall control diagram

5 IC parameter settings

5.1 HV pin-related parameters and functions

The HV pin provides the start-up and bulk capacitor voltage sensing. The sensed voltage information will provide input power estimation and ZVS on-time adjustment. The brown-in/out function is also based on the HV pin, but on the current level.

The internal 600 V depletion start-up cell provides the charging current to the V_{CC} pin.

The charging current is calculated as $i_{hv}(t) = \frac{V_{bulk} - V_{cc}(t)}{R_{hv}}$, so it can be seen with a fixed HV pin external resistor, and the charging current will change proportionally with input AC-line voltage.

The start-up delay time needed is the time spent charging the V_{CC} capacitor before reaching the V_{CCon} threshold 20.5 V. $t_{delay} = C_{vcc} \cdot \frac{Vcc_{on}}{i_{hv} - i_{lk}}$, i_{lk} is the HV pin leakage current before power-up, stated in the datasheet specifications, typically ~10 µA.

When the V_{CC} is above 9 V, if the current flowing into the HV pin is greater than 1.156 mA, the IC starts switching. If the current is below 0.443 mA, the IC will stop switching after 1.06 ms.

So based on this current limit and the 100 kΩ HV pin resistor, we will see the brown-in voltage is $V_{brownin}$ = I_{hvbi} x R_{hv} + I_{hvbi} x 1.49 = 1.156 mA x (100 kΩ + 1.49 kΩ) = 117.32 V DC.

The brown-out voltage is $V_{brownout}$ = I_{hvbo} x R_{hv} + I_{hvbo} x 0.99 = 0.443 mA x (100 kΩ + 0.99 kΩ) = 44.7 V DC.

The other functions of V_{bulk} are used to tune the ZVS on-time and input power estimation. The current flow into the HV pin is not enough to get the voltage information, as it is also decided by the external HV pin resistor.

5.2 ZCD pin-related settings and functions

5.2.1 Output OVP function

The ZCD pin provides zero crossing detection in DCM and output voltage sensing during off-time. This pin's negative voltage is clamped to -0.2 V during the primary MOSFET's on-time.

$$V_{zcd} = \frac{N_{aux}}{N_s} \cdot \frac{R_l}{R_h + R_l} \cdot V_o < Vo_{ovpthr} \quad (9)$$

$$i_{zcd} = \frac{-0.2 + \frac{N_{aux}}{N_p} V_{bulkmax}}{R_h} \leq 3.5mA \quad (10)$$

R_h determines the current flowing out of the ZCD pin, based on designed N_{aux} and N_s. R_h will be selected first based on the current limit of the ZCD pin. Once R_h is chosen, based on the OVP requirement and V_{ZCD} OVP threshold, R_l can be calculated.

Based on N_{aux} = 5, N_p = 28, $V_{bulkmax}$ = 374 V, from equation (10), R_h is greater than or equal to 19.02 kΩ, and here we choose 39 kΩ.

The next thing is to decide the value of R_l based on equation (9) and the OVP requirement, N_s = 5, R_h = 39 kΩ, $V_{outovpthr}$ = 2.75 V, V_{outovp} = 21.7 V, R_l = 5.6 kΩ.

To filter noise at the ZCD pin, a small capacitor such as 10 pF can be paralleled to the low-side resistor.

5.2.2 V_{CS} offset based on V_{ZCD}

Figure 13 shows the V_{CS} offset based on V_{ZCD}, while the ZCD voltage corresponds to the output voltage. The purpose of this compensation is to reduce the current command for different output voltages, so the maximum allowed power can be reduced. This feature is especially important for variable-output voltage applications when the system is dimensioned at full power at the highest voltage. So the power can be reduced at lower output voltages to meet limited power supply (LPS) requirements.

ZCD pin voltage is from 1.2 V to 2.8 V, with the gain 1.5; this voltage is converted to the digital value internally with an 8-bit ADC.

The calculation procedure is to decide the zero point of V_{ZCD}; above this threshold, there is no compensation.

Second, based on the targeted compensation value, calculate K_{vcs_offset}.

The output voltage:

$$Vzcd_{zeropoint} = \frac{Rl}{Rl + Rh} * \frac{Naux}{Ns} * Vo_zero_point \quad (11)$$

Here we choose $V_{o_zero_point}$ = 13.5 V, with known R_l = 5.6 kΩ, R_h = 39 kΩ, N_{aux} = 5, N_s = 5, $V_{ZCDzeropoint}$ = 1.7 V.

The digital number $V_{ZCD_dig_zeropoint}$ = ($V_{ZCDzeropoint}$ – 1.2) x 1.5/2.4 x 255 = 79; this parameter can be set in the .dp Vision GUI.

Next is to decide the target compensation value, e.g., 53 mV at V_{ZCD} = 1.2 V, so the compensated digital value of V_{CS_dig} = 53 mV/0.4 V x 255 = 34, then K_{vcs_offset} = V_{CS_dig}/(0-$V_{ZCDzeropoint}$) x 65535 = 28240, and this slew rate is also a configurable parameter in the .dp Vision GUI.

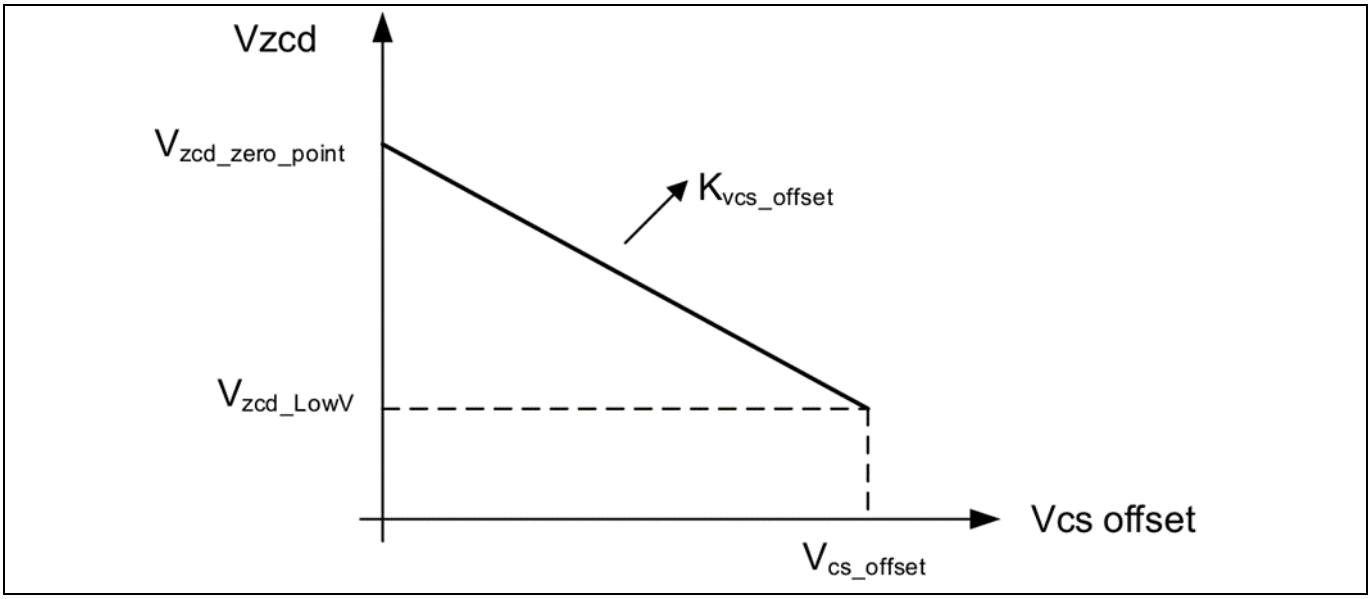


Figure 13 V_{CS_offset} compensation based on V_{ZCD} voltage

5.3 Gate driver related settings and functions

The two gate drivers are double-loop controlled, with external current loop and internal voltage loop. The default sourcing current is 35 mA (GD0), 118 mA (GD1) and 10.5 V clamp. The sink capability of the internal discharge path is limited by internal equivalent resistance less than or equal to 6.5 Ω, so the maximum sink current is 10.5 V/6.5 Ω = 1.6 A if there is no external serial resistor adopted.

IC parameter settings

Unlike the conventional voltage source-based driver, only one gate resistor is needed to limit the sink current. Generally a 10 Ω or lower gate resistor is used, and this should be tuned based on switch-off losses versus turn-off speed.

GD0 is the gate driver for the primary main MOSFET. GD1 is for the ZVS MOSFET.

There are two configurable parameters that can tune ZVS MOSFET on-time. Tuning this parameter is necessary since the parasitic capacitor varies with different C_{oss} of the primary MOSFET, SR MOSFET and parasitic coupling capacitor of the transformer.

$$\boldsymbol{t_{GD1on} = \left(V_{bulk} * \frac{K_{zvson}}{65535}\frac{1}{V} + 2\right) * 15.8ns + (2.34V - V_{zcd}) * \frac{K_{zvson_{vout}}}{65535} * \frac{1}{V} * 15.8ns} \quad (12)$$

V_{bulk} is measured through the HV pin and reflects bulk input voltage. V_{zcd} reflects power supply output voltage V_{out} and is proportional to V_{out}. According to equation (12), ZVS MOS on-time t_{GD1on} is proportional to V_{bulk} and reverse proportional to V_{out}.

The energy stored in the magnetizing inductance needed to discharge the equivalent capacitor energy of the primary MOSFET is like this:

$$0.5 \cdot L_p \cdot i_{neg}^2 > 0.5 \cdot C_{eqv} \cdot V_{ds}^2 \quad (13)$$

$$i_{zvs_pk} = \frac{N_p}{N_{zvs}} \cdot \frac{V_{zvs}}{L_p} \cdot t_{GD1on} \quad (14)$$

Required dead-time is:

$$t_{ZVSdead} = \frac{Q_{oss}}{i_{zvs_pk}} \quad (15)$$

There is also a configurable parameter $t_{ZVSdead}$ that can be tuned for required dead-times based on system parameters.

5.4 MFIO pin-related parameters

The MFIO pin provides the feedback information for the IC. Based on the voltage measured at the MFIO pin, the IC will check the reference table to get the desired frequency or frequency band and current limit command. The MFIO pin represents the loading directly, so the IC can also choose the operation mode (QR/FQR ZVS, DCM, burst mode) based on the MFIO voltage level.

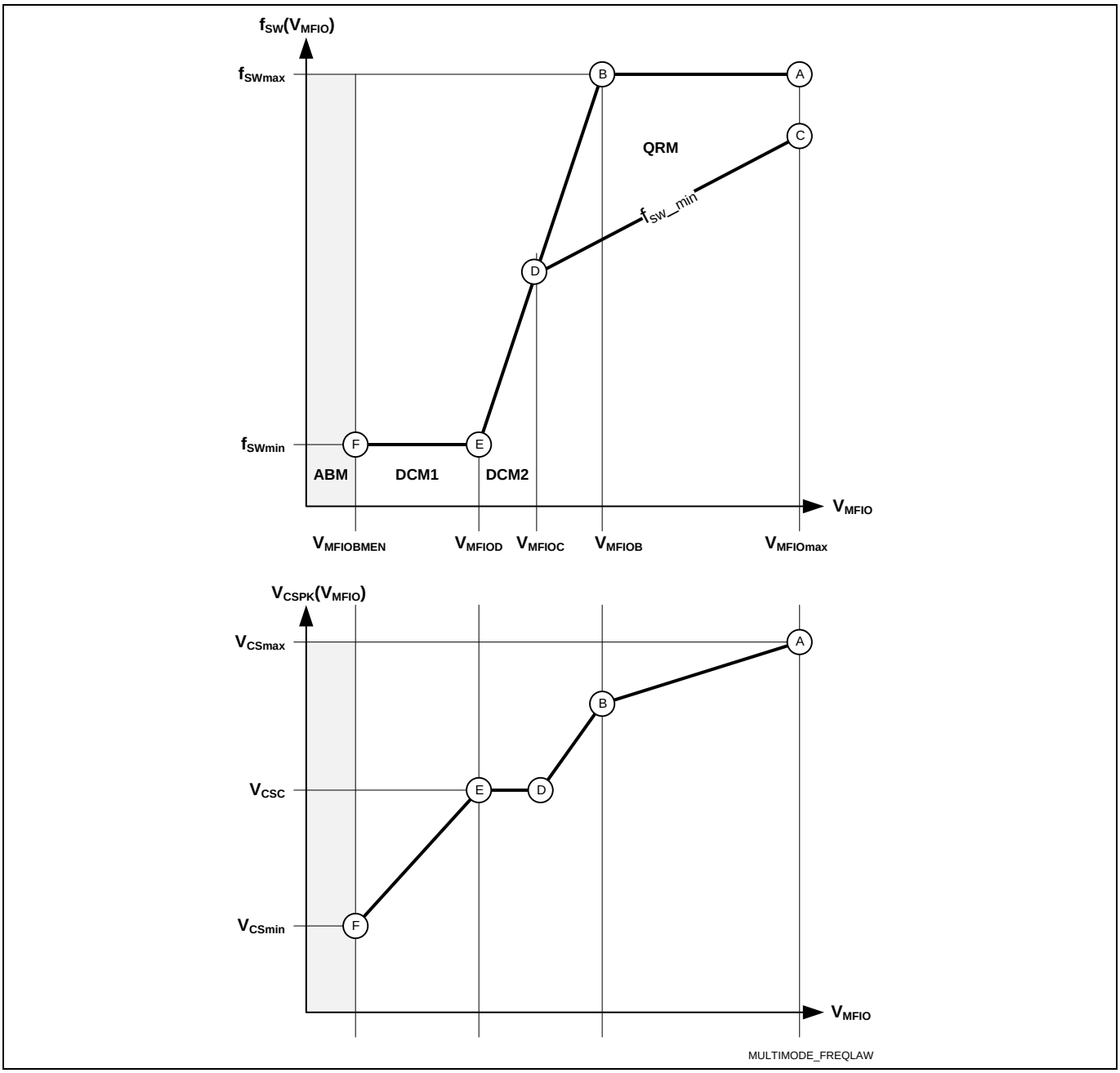


Figure 14 Frequency law configuration

5.5 V_{CC} pin-related parameters

V_{CC} provides the operating voltage of the IC and also has undervoltage lockout (UVLO) protection when V_{CC} drops below 7.2 V. Brown-in is activated when V_{CC} is above 9 V.

V_{CC} also has a V_{CC} OVP function, 21.8 V (typ.).

5.6 CS pin-related parameters

The CS pin's main functions are current mode control and overcurrent protection (OCP). For the current command, it is influenced by propagation delay compensation (PDC), V_{CS_offset}, and these parameters can be tuned according to different system dimensions.

IC parameter settings

The current command is given by equation(16):

$$CS_OCP1LVL = (Ipk) - PDC_Correction - Vcsoffset \quad (16)$$

$$PDC_Correction = INT(2^{-16} * PDC_{FACTOR} * Vbulk + PDCOFFSET) \quad (17)$$

Where PDC_{FACTOR} and PDC_{OFFSET} are two configurable parameters using .dp Vision – propagation delay-related parameters.

$$PDC_{FACTOR} = \frac{R_{CS} \cdot t_{PD}}{L_p \cdot V_{CSlsb8}} \cdot (2^{16} - 1) \quad (18)$$

$PDC_{FACTOR} = \frac{R_{CS} \cdot t_{PD}}{L_p \cdot V_{CSlsb8}} \cdot (2^{16} - 1) = \frac{0.135ohm \cdot 352ns}{200\mu H \cdot 2.34mV} \cdot 65535 = 6654$

Actually, the default PDC_{FACTOR} for XDPS21081 is 9000, default PDC_{OFFSET} is 0, so PDC_correction = 9000 x 85 V/65535 +0 = 9 bits, each bit is 2.34 mV, so PDC-induced V_{CS} reduction is 2.34 mV x 9 = 21 mV.

Where R_{CS} is the current sense resistor, t_{pd} is the propagation delay, which includes internal comparator delay and external turn-off delay, L_p is the main inductance value, and V_{CSlsb8} is the DAC lsb of the CS signal.

As maximum V_{CS} at low-line is 0.4 V, so R_{CS} = (400 mV – 21 mV)/I_{pk} = 0.232 V/3.05 A = 0.125 Ω.
As we see in the calculation procedure, the PDC calculation is influenced by R_{CS}, which is unknown before we get the final R_{CS} value, and also the propagation delay needs to be calibrated. And peak current calculations are also influenced by the efficiency assumption, etc., so R_{CS} would be tuned slightly to tailor it to a real design based on real test results. In the 65 W reference board, R_{CS} = 0.135 Ω is chosen.

6 Burst mode operation

To maintain efficiency at light load, the IC needs to keep the system working in burst mode. **XPDS21081** will stop the core engine and reduce power consumption depending on feedback voltage, which reflects load signal. **Table 9** shows the burst mode entry level. Different MFIO voltage means different peak current based on frequency.

Table 9 Burst mode entry level per V_{ZCD}

Burst mode entry threshold	Symbol	Min.	Typ.	Max.	Unit
	$V_{MFIOBMEN}$	0.175	0.209	0.242	V

Burst mode operation power is defined as follows:

$$P_{bst} = 0.5 * L_p * I_{pk}^2 * F_{bst} \quad (19)$$

Based on default V_{CS} in burst mode 78 mV, the peak current is 78 mV/0.135 Ω = 0.578 A, f_{bst} = 23 kHz. With known inductance, the burst mode power can be calculated.

7 Tips on PCB layout

In principle, there are two key switching loops, which need to be as small as possible. One is from bulk capacitor V+ to transformer winding to Q30 to R_{sense} to bulk capacitor V-. The other is the secondary-side rectification loop from the secondary transformer winding to the output filter capacitor and Q100 SR MOSFET.

For **XDPS21081** ground connection, star ground to bulk capacitor negative V- is necessary. The ZCD winding's ground should connect to filtering capacitor C50 first, then all other pins' grounds should tie to this IC's ground first before connecting to C50's ground.

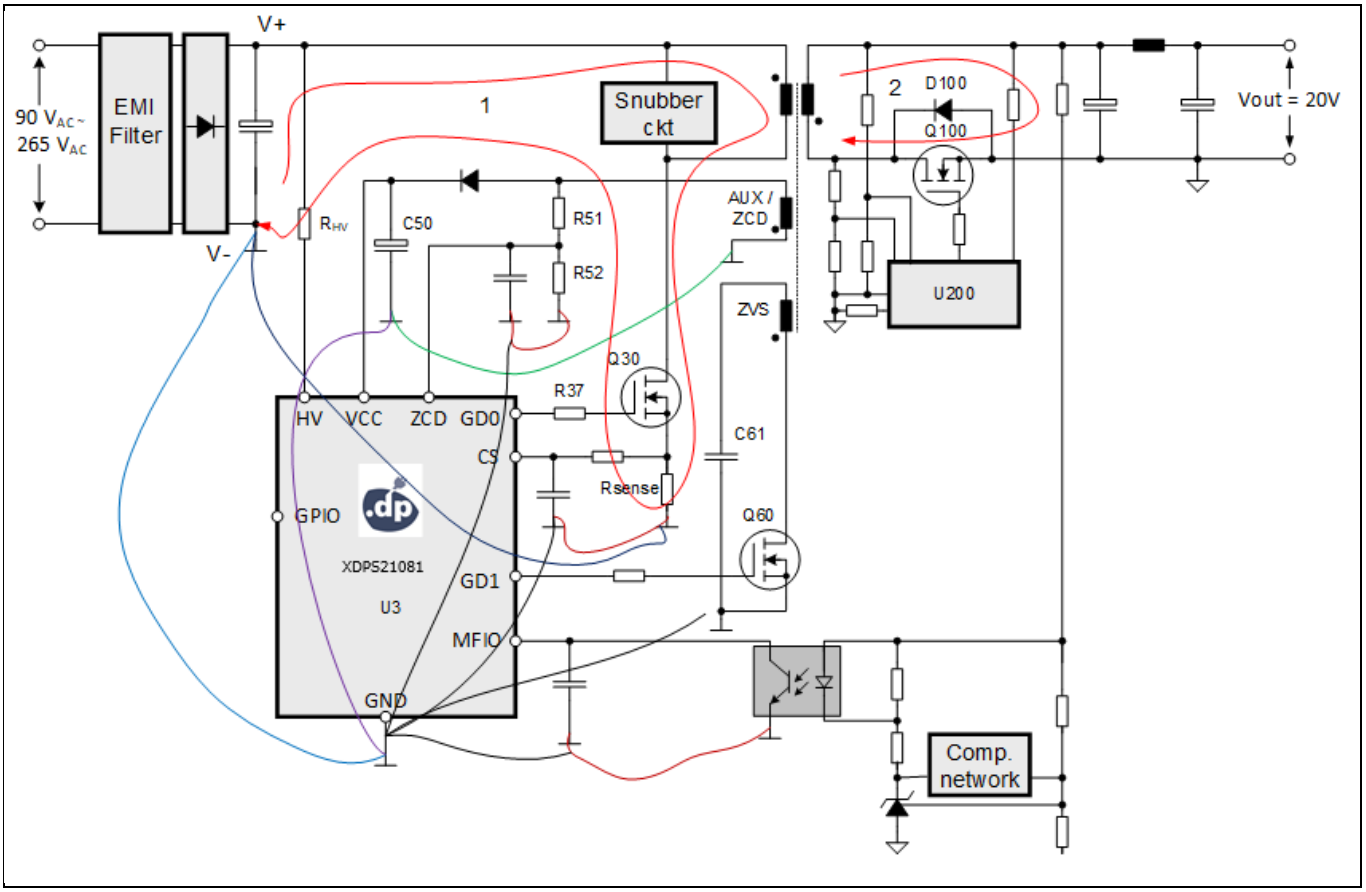


Figure 15 System layout recommendation

8 Usage of .dp Vision

8.1 Installation of .dp Vision

Customers can install the user interface .dp Vision on their own computer, following the installation instructions.

1) Install the latest .dp Vision_2.0.9.4 from the folder (double-click “dpVision_2.0.9.4.msi”).
2) Connect the IFX IDP21081 sample to the **dpIFGen2** interface board using V_{CC}, UART and GND pins.



Figure 16 dpIFGen2 interface board (side view)

3) Connect the **dpIFGen2** interface board using the USB cable provided to the laptop USB port and open the .dp Vision GUI by double-clicking on “dpVision.exe” or the icon shown below.



Figure 17 .dp Vision icon

Usage of .dp Vision

4) Open “XDPS21081_with_assistant_trials_rev1.07.csv” using menu → File → Open → browse to folder →\.....\.dpVision\Parameters.

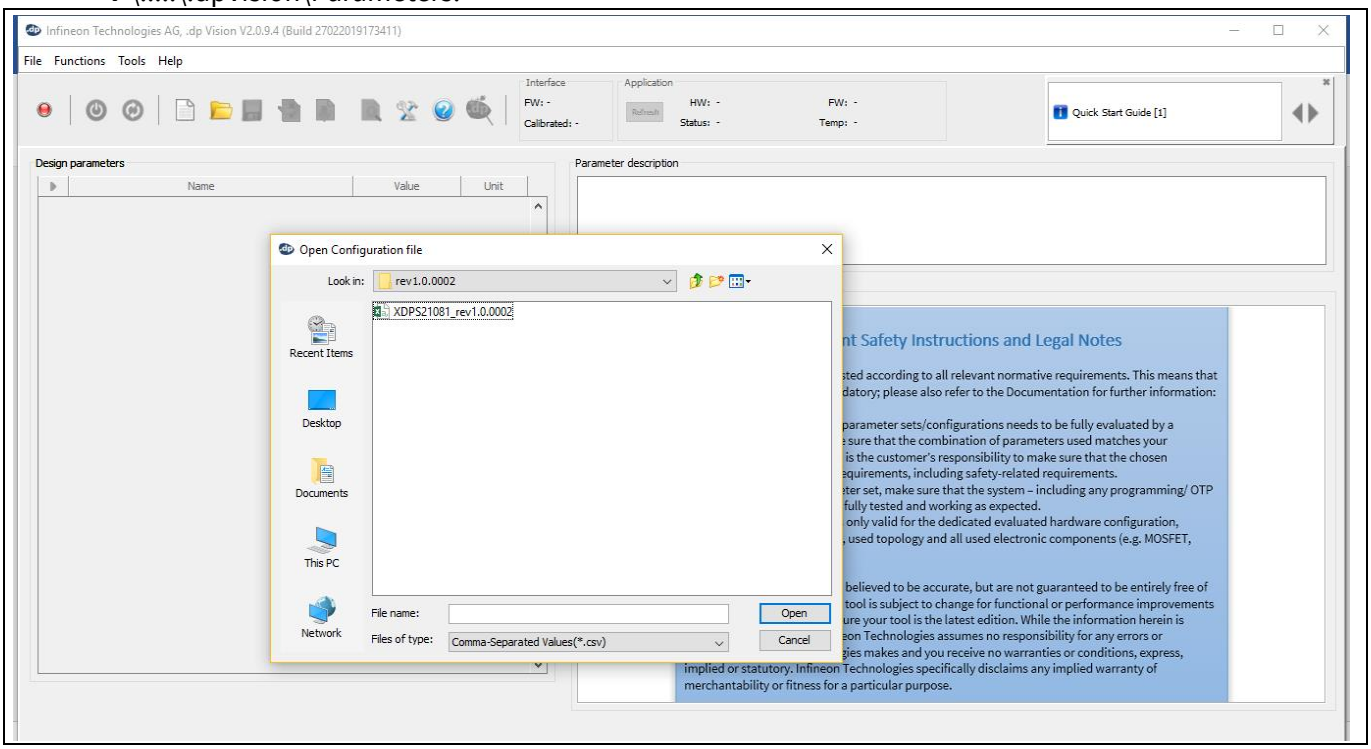


Figure 18 Power device on/off button and device status

5) Press the power device on/off button → device status should turn green.

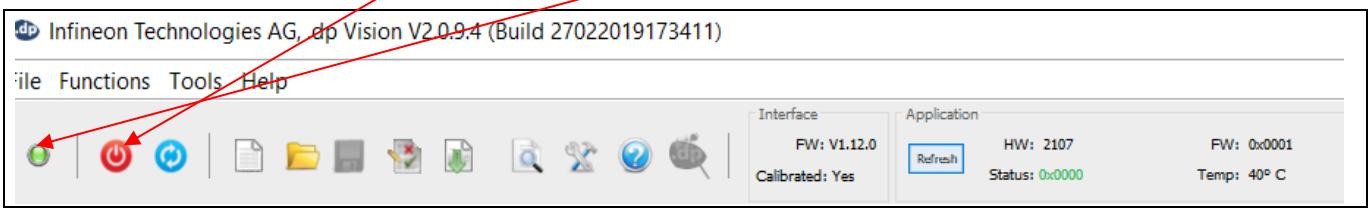
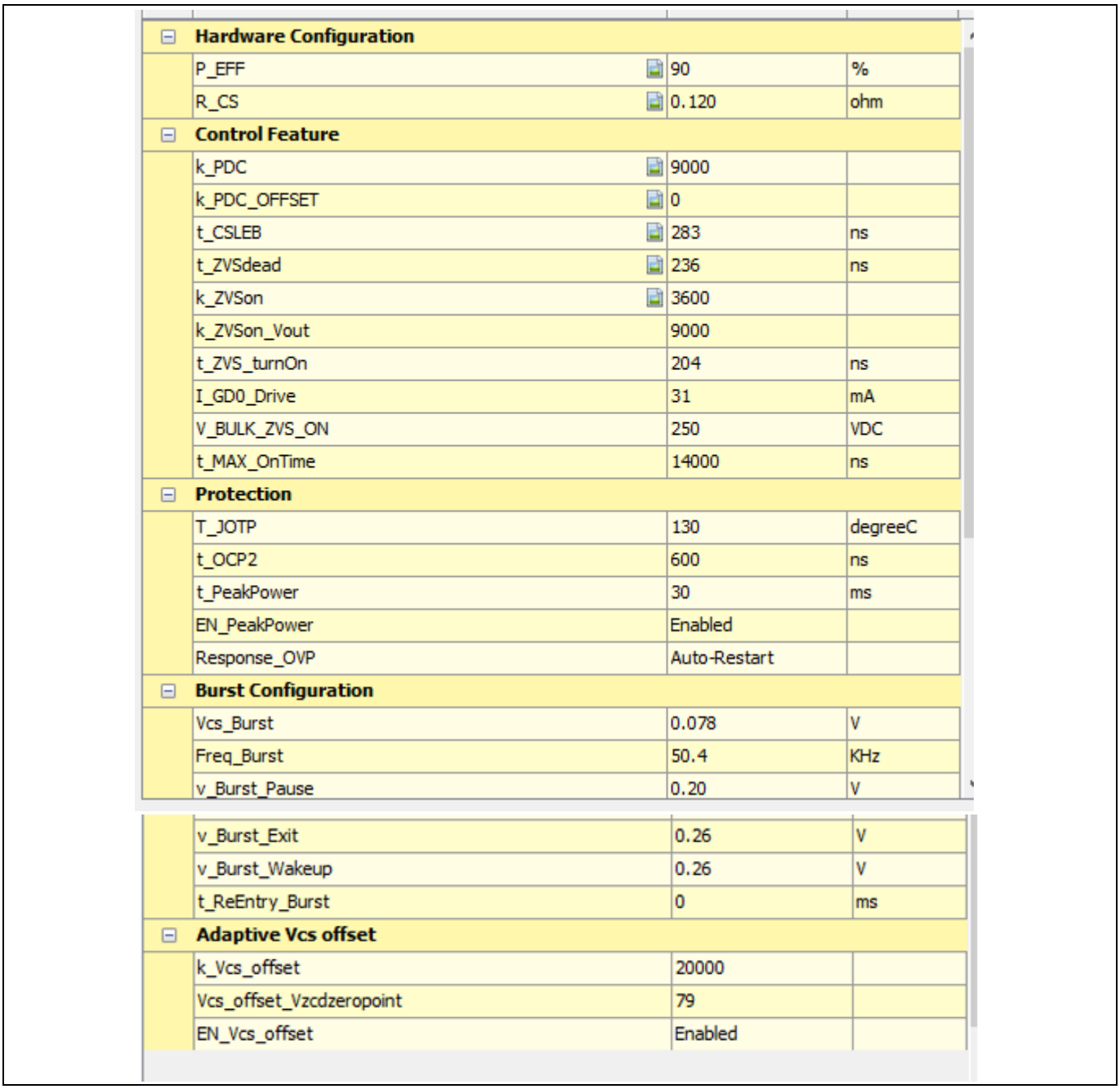


Figure 19 Power device on/off button and device status

6) Press the “Test Configuration Set” button and the parameter values are loaded in the XDPS21081 sample and the application firmware starts running.

Usage of .dp Vision

7) Change the parameters under the “Value” field.



Hardware Configuration			
	P_EFF	90	%
	R_CS	0.120	ohm
Control Feature			
	k_PDC	9000	
	k_PDC_OFFSET	0	
	t_CSLEB	283	ns
	t_ZVSdead	236	ns
	k_ZVSon	3600	
	k_ZVSon_Vout	9000	
	t_ZVS_turnOn	204	ns
	I_GD0_Drive	31	mA
	V_BULK_ZVS_ON	250	VDC
	t_MAX_OnTime	14000	ns
Protection			
	T_JOTP	130	degreeC
	t_OCP2	600	ns
	t_PeakPower	30	ms
	EN_PeakPower	Enabled	
	Response_OVP	Auto-Restart	
Burst Configuration			
	Vcs_Burst	0.078	V
	Freq_Burst	50.4	KHz
	v_Burst_Pause	0.20	V
	v_Burst_Exit	0.26	V
	v_Burst_Wakeup	0.26	V
	t_ReEntry_Burst	0	ms
Adaptive Vcs offset			
	k_Vcs_offset	20000	
	Vcs_offset_Vzcdzeropoint	79	
	EN_Vcs_offset	Enabled	

Figure 20 Value field

Usage of .dp Vision

8) Changing the parameters will activate the “Save Configuration Set” button. Save the configuration and again press the power on/off button and click on “Test Configuration Set”, which will load the new configuration set into the chip’s RAM area. Click on “Functions/Burn Configuration Set”, which will burn the new configuration set into OTP memory.

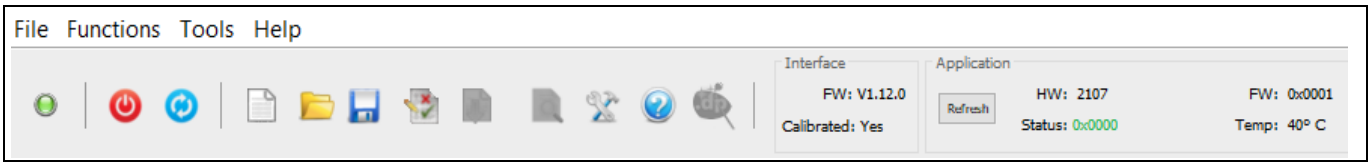


Figure 21 “Save Configuration Set” button

9) For details of setting parameters with .dp Vision, please press “Help” for the.dp Vision user manual.

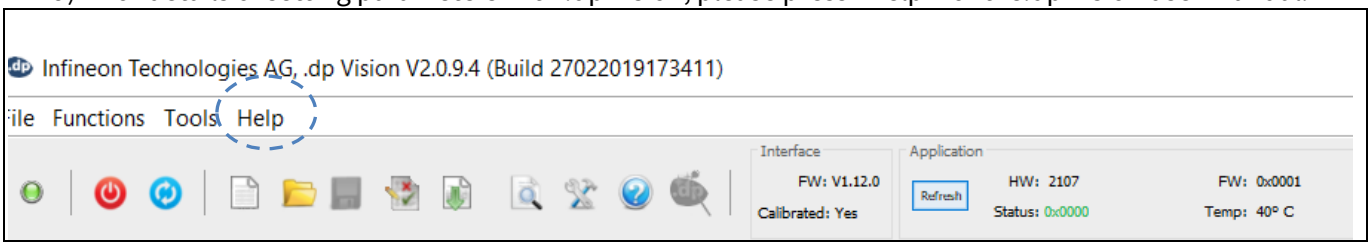


Figure 22 “Help” button

8.2 Parameter setting with .dp Vision

Table 10 lists all the parameters configurable by customers through .dp Vision. The setting of the major parameters has been explained in detail in this design guide. The description of each parameter together with an explanatory image will be displayed by clicking on each parameter name. In addition, a user manual can be obtained via the “Help” button.

Usage of .dp Vision

Table 10 Configurable parameters

Feature	Parameter	Default	Description
Propagation delay compensation for peak current control	k_PDC	9000 d	Propagation delay compensation factor
	k_PDC_OFFSET	0 d	Propagation delay compensation offset
LEB	t_{CSLEB}	283 ns	Blanking filter at CS pin to avoid erroneous turn-off of GD0 due to leading-edge spike at GD0 turn-on
ZVS dead-time	$t_{ZVSdead}$	236 ns	Dead-time between end of ZVS pulse at GD1 and start of GD0
ZVS pulse length factor	k_{ZVSon}	3600	ZVS pulse length factor per bulk voltage
	k_{ZVSon_vout}	9000	ZVS pulse length factor per output voltage
ZVS gate turn-on point	T_{zvs_turnon}	204 ns	Turn-on of the ZVS gate after zero crossing detected
Gate driver capability	$I_{_GD0_drive}$	35 mA	Sourcing current of gate driver 0
ZVS enable voltage	$V_{BULK_ZVS_ON}$	250 V DC	Above this voltage, ZVS gate is allowed to turn-on
	t_{MAX_OnTime}	140000 ns	
Protections	T_{JOTP}	130°C	Internal overtemperature detection level
	t_{ocp2}	600 ns	Blanking time for OCP2 of V_{CS} signal
	$t_{peakpower}$	30 ms	Blanking time for OLP
	En_OLP	Enabled	To enable or disable OLP
	Response_OVP	Auto restart	Protection mode for OVP, configurable for AR or latch
Burst mode parameters	*Vcs_bst*	0.078 V	Burst mode current limit
	Freq_bst	50.4 kHz	Burst mode frequency
	V_bst_pause	0.2 V	Pause threshold at MFIO pin during on-phase in burst mode operation
	V_bst_exit	0.26 V	Burst mode exit voltage at MFIO pin
	V_bst_wakeup	0.26 V	Burst mode wake-up voltage at MFIO pin
	T_reentry_bst	0 ms	Minimum time to re-enter burst mode
Adaptive V_{CS} offset	$K_V_{CS_offset}$	20000	Gradient for compensation curve
	$V_{CS_offset}_V_{zcdzeropoint}$	79	ZCD voltage level (digital value) without V_{CS} offset
	$En_V_{CS_offset}$	Enabled	To enable or disable V_{CS_offset} compensation

9 References

[1] XDPS21081 1.0 datasheet

[2] Design tips for flyback converters using the quasi-resonant PWM controller ICE2QS01, **http://www.infineon.com/dgdl/ANPS0005-ICE2QS01-V11-14122011.pdf?fileId=db3a30432f91014f012fb9a251d750c4**

[3] Robert W. Erickson, *Fundamentals of Power Electronics*, second edition, Springer, 2001

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