ICE1PCS01

ICE1PCS01 Based Boost Type CCM PFC Design Guide – Control Loop Modeling

Power Management & Supply

Never stop thinking.

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ICE1PCS01

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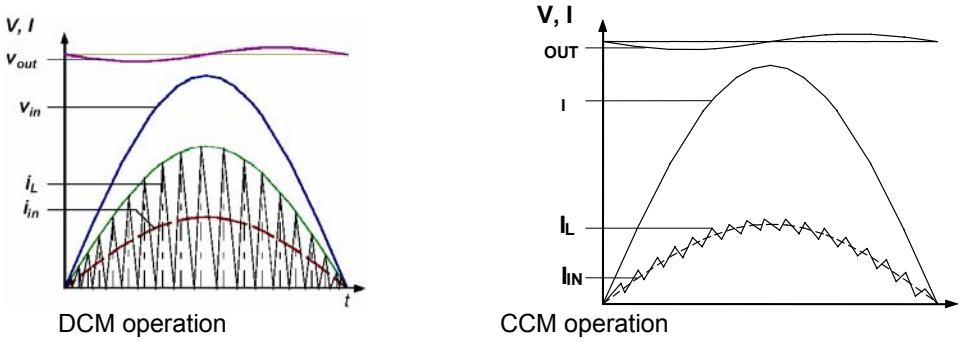
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Abstract

A new continuous conduction mode (CCM) PFC controller, named ICE1PCS01, is developed based on a new control scheme. Compared to the conventional PFC solution, the new IC does not need the direct sine-wave sensing reference signal from the AC mains. Average current control is implemented to achieve the unity power factor. This application note provides a model and a tool for evaluating and improving the control loop characteristics of ICE1PCS01-based PFC pre-regulators in boost topology. The goal is not only to ensure a narrow bandwidth in order to achieve a high Power Factor, but also to have enough phase margin so as to make sure the system is stable over a large range of operating conditions. The design example is demonstrated as well.

1 Introduction

Traditional diode rectifiers used in front of the electronic equipment draw pulsed current from the utility line, which deteriorates the line voltage, produce radiated and conducted electromagnetic interference, leads to poor utilization of the capacity of the power sources. In compliance with IEC 61000-3-2 harmonic regulation, active power factor correction (PFC) circuit is getting more and more attention in recent years. For low power up to 200W, discontinuous conduction mode (DCM) PFC is popular due to its lower cost. Furthermore, there is only one control loop, i.e. voltage loop, in its transferring control blocks. The design is easy and simple for DCM operation. However, due to its inherent high current ripple, DCM is seldom to be used for high power applications. In high power applications, continuous conduction mode (CCM) PFC is more attractive.



DCM operation CCM operation

Figure 1 DCM and CCM PFC principle

In the conventional CCM topology, there are two control loops called voltage loop and current loop in its transfer function. Because of this, the control circuit of CCM is complicated and the Pin count of CCM PFC controllers is often high. New CCM PFC controller, named ICE1PCS01, is developed to simplified and cost down the design. It has only 8 pins. Moreover, numerous protection features are integrated according to Failure Mode Effect Analysis (FMEA). The typical application of the new PFC controller, named ICE1PCS01, is shown in Figure 2. It has only 8 pins and there is no direct sin-wave sensing signal fed into the IC.

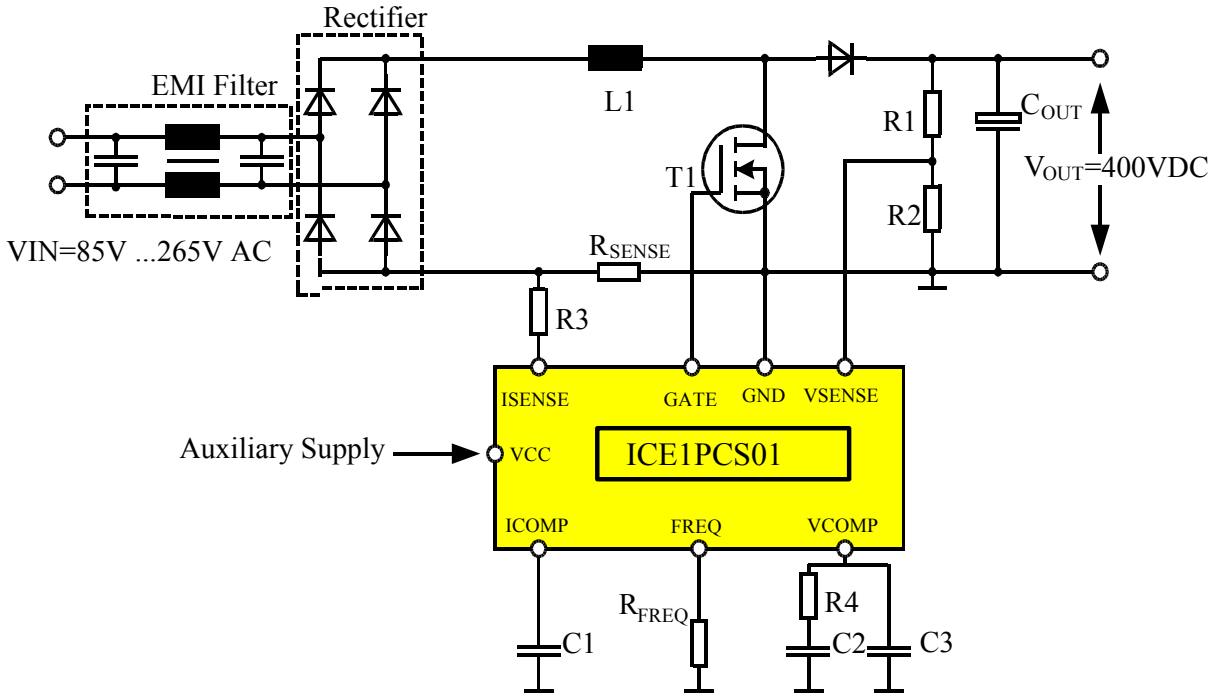


Figure 2 Typical application circuit of ICE1PCS01

In this application note, the control loop compensation design of ICE1PCS01 based boost topology CCM PFC is described in detail.

2 How to achieve PFC function without sinusoidal reference sensing

2.1 Boost converter modeling

Figure 3 shows the inductor current waveform for boost converter operating in continuous conduction mode.

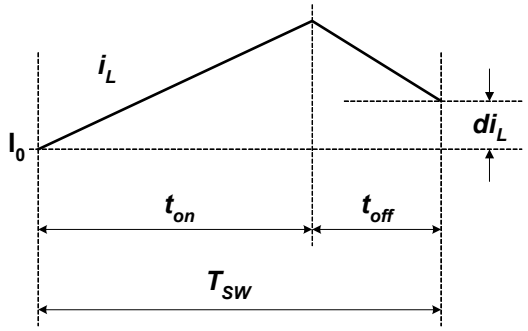


Figure 3 inductor current waveform of boost converter operating in CCM mode

assuming Vin is boost converter input DC voltage, Vout is the boost converter output voltage, L is the boost choke inductance, ton is the on time duration in one switching cycle, toff is the off time duration in one switching cycle, doff is the off time duty cycle and Tsw is the time duration in one switching cycle.

During “on” interval,

$$\frac{di_L}{dt} = \frac{V_{in}}{L} \tag{1}$$

During “off” interval,

$$\frac{di_L}{dt} = \frac{V_{in} - V_{out}}{L} \tag{2}$$

And then the boost inductor current variation after one switching cycle is:

$$di_L = \frac{V_{in}}{L} \cdot t_{on} + \frac{V_{in} - V_{out}}{L} \cdot t_{off} = \frac{V_{in} - V_{out} \cdot d_{off}}{L} \cdot T_{SW} \tag{3}$$

The instant boost inductor current after n switching cycle is:

$$i_{L_n} = i_{L_n-1} + \frac{V_{in_n} - V_{out_n} \cdot d_{off_n}}{L} \cdot T_{SW} \tag{4}$$

2.2 PFC IC control principle with boost topology

PFC IC control block is inserted in boost converter as shown in Figure 4.

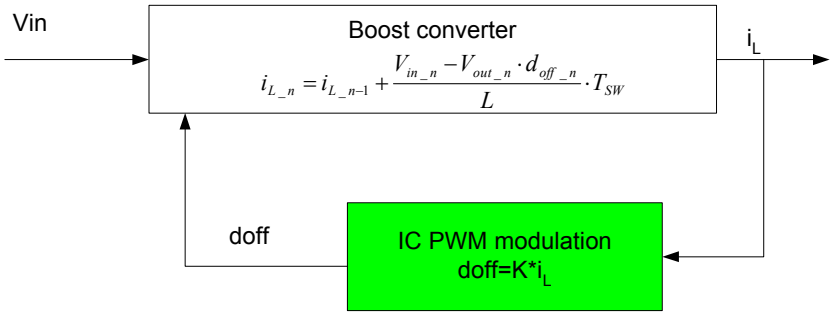


Figure 4 PFC current loop principle

IC senses boost inductor average current, and calculate the off duty cycle to be proportional to inductor current, and then send such off duty cycle back to boost converter. The negative feedback loop can be seen from Figure 4. A small disturb increasing on i_L will result in a little bit increasing on off duty cycle. The increasing off duty cycle will lead to decreasing of i_L after processing by boost converter. In the stead state,

$$V_{in} = V_{out} \cdot d_{off} = V_{out} \cdot K \cdot i_L \quad (5)$$

Where, K is the modulation gain defined by IC. It can be seen that boost inductor current shape follows AC input voltage and it is how PFC function to be achieved.

In the following sections, detail mathematical analysis of current loop and voltage loop will be described and the transfer function for each block is given in order to design IC external compensation network components.

3 Current Loop Regulation and Transfer Function

The detail block diagram of current loop for ICE1PCS01 is shown in the Figure 5. The boost converter stage K_{boost} is elaborated in S-plane.

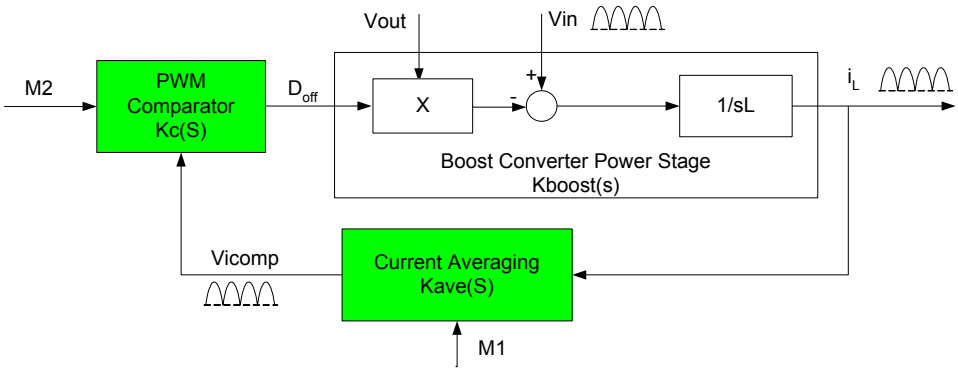


Figure 5 Block diagram of current loop

3.1 Current Averaging Circuit

IC sense the boost inductor current via shunt resistor Rsense as shown in Figure 2. The sensing signal is sent to Isense Pin. As the voltage in Isense Pin is negative signal together with switching ripple, IC need to do signal averaging and convert the polarity to positive for following PWM modulation blocks. The output of averaging block is Vicomp voltage at Icomp Pin. the block diagram of current averaging block is shown in Figure 6.

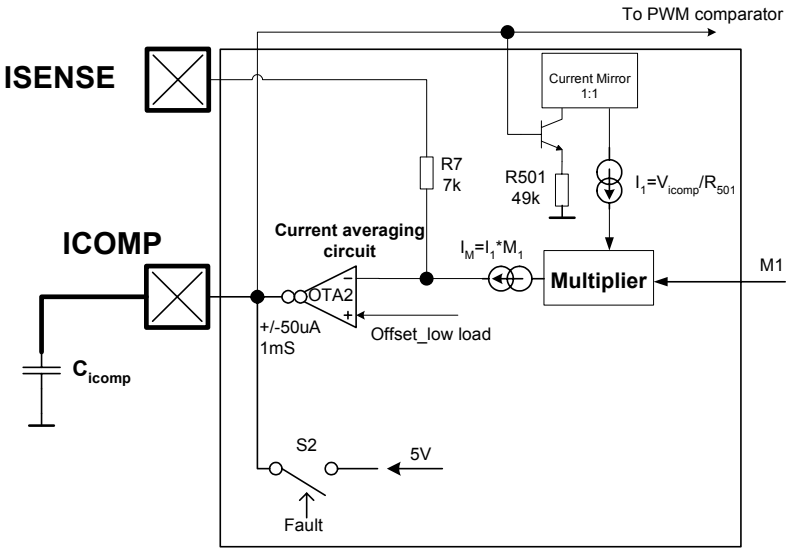


Figure 6 current averaging block diagram

The transfer function of averaging circuit block can be derived as below.

$$K_{AVE}(s) = \frac{V_{icomp}}{i_L} = \frac{\frac{K_1 R_{sense}}{M_1}}{1 + s \cdot \frac{K_1 C_{icomp}}{M_1 g_{OTA2}}} \quad (6)$$

where, K_1 is a ratio between R501 and R7 which is equal to 7, C_{icomp} is the capacitor at Icomp Pin, g_{OTA2} is the trans-conductance of the error amplifier of OTA2 for current averaging, typical 1.1mS as shown in Datasheet, M1 is the variable controlled by voltage loop.

The function of the averaging circuit is to filter out the switching current ripple. So the corner frequency of the averaging circuit f_{AVE} must be lower than the switching frequency f_{SW}. Then,

$$C_{icomp} \geq \frac{g_{OTA2} M_1}{K_1 \cdot 2\pi f_{AVE}} \quad (7)$$

3.2 PWM comparator block

The averaged Vicomp signal is sent to PWM comparator block and compared with internal triangular ramp signal to derive duty cycle. The timing diagram of this block is shown in Figure 7.

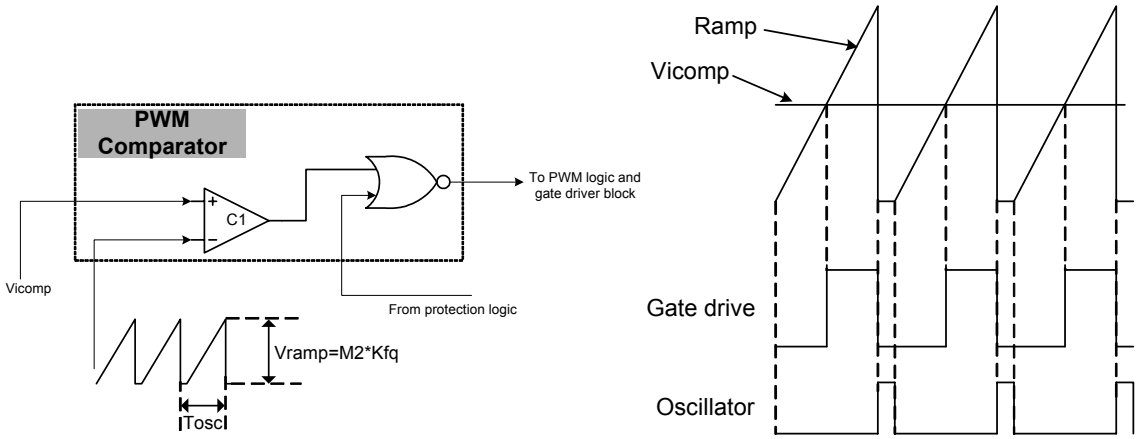


Figure 7 The block diagram and timing sequence of PWM comparator block

The operating principle is explained as following. Gate output is in “low” state in the beginning of the each cycle. Gate output is turned to “high” at the intersection of the triangular ramp signal and Vicomp signal. Gate output is turned to “low” by oscillator synchronous signal. Based on the operating principle, the transfer function of $K_C(s)$ is:

$$K_C(s) = \frac{d_{off}}{V_{icomp}} = \frac{1}{K_{FQ} M_2} \quad (8)$$

Where, K_{FQ} is a design constant which is equal to 9.183, M_2 is the variable controlled by voltage loop.

3.3 Boost converter stage

The transfer function of boost converter stage $K_{Boost}(s)$ can be obtain via State-Space Averaging method. Combining equation (1) and (2) by state –space averaging,

$$\frac{di_L}{dt} = \frac{V_{in}}{L} d_{on} + \frac{V_{in} - V_{out}}{L} d_{off} = \frac{V_{in} - V_{out} d_{off}}{L} \quad (9)$$

Make Laplace transformation for equation (9) with assuming Vin and Vout are constant for current loop analysis,

$$i_L(s) = (V_{in} - V_{out} d_{off}(s)) \frac{1}{sL} \quad (10)$$

The equation (10) has been described in current loop block diagram in Figure 5. **Although Vin is not physically sensed by circuit, the input sinusoidal signal is presented in transfer functions only if boost topology is applied.**

3.4 Open loop transfer function gain for current loop

The open loop gain of current regulation loop is:

$$G_C(s) = K_{AVE}(s) K_C(s) \frac{V_{out}}{sL} = \frac{\frac{K_1 R_{sense} V_{out}}{K_{FQ} M_1 M_2 L}}{s(1 + s \cdot \frac{K_1 C_{icomp}}{M_1 g_{OTA2}})} \quad (11)$$

The selected C_{icomp} must also meet the requirement that the cross over frequency of the current loop f_C is much lower than the switching frequency f_{SW}.

3.5 Steady state solution of I_L

Solving the current loop in Figure 5,

$$i_L(s) = (V_{in} - V_{out} d_{off}(s)) \frac{1}{sL} = (V_{in} - V_{out} K_C(s) K_{AVE}(s) i_L(s)) \frac{1}{sL}$$

$$i_L(s) = \frac{\frac{V_{in}}{sL}}{1 + \frac{V_{out} K_C(s) K_{AVE}(s)}{sL}} = \frac{\frac{V_{in}}{sL}}{1 + G_C(s)} \quad (12)$$

For AC line frequency which is much lower than f_C, then $G_C(s)>>1$,

$$i_L(s) = \frac{\frac{V_{in}}{sL}}{1 + G_C(s)} \approx \frac{\frac{V_{in}}{sL}}{G_C(s)} = \frac{\frac{K_{FQ} M_1 M_2 V_{in}}{K_1 R_{sense} V_{out}}}{1 + s \cdot \frac{K_1 C_{icomp}}{M_1 g_{OTA2}}} \quad (13)$$

For AC line frequency which is also much lower than f_{AVE}, then the steady state I_L can be derived as

$$I_L = \frac{K_{FQ} M_1 M_2 V_{in}}{K_1 R_{sense} V_{out}} \quad (14)$$

from the above steady state solution of I_L, it can be seen that the choke current I_L is always following input voltage V_{in}. This is how PFC function is achieved.

4 Voltage Loop Compensation

The control loop block diagram for ICE1PCS01 based CCM PFC is shown in Figure 8 and Figure 9. There are four blocks in the loop. IC PWM Modulator $G_2(s)$ has been discussed in above Section 3. the rest of them are Error Amplifier $G_1(s)$, nonlinear block $G_{NON}(s)$, boost converter output stage $G_3(s)$ and Feedback Sensing $G_4(s)$.

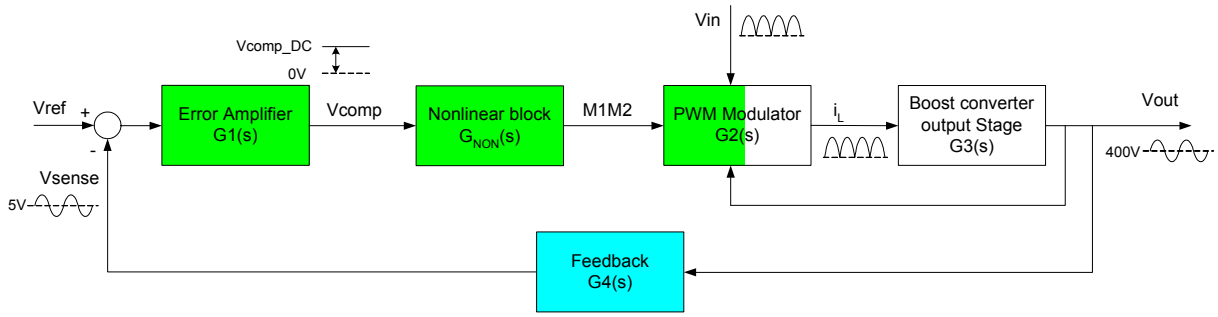


Figure 8 Large signal modeling of voltage loop

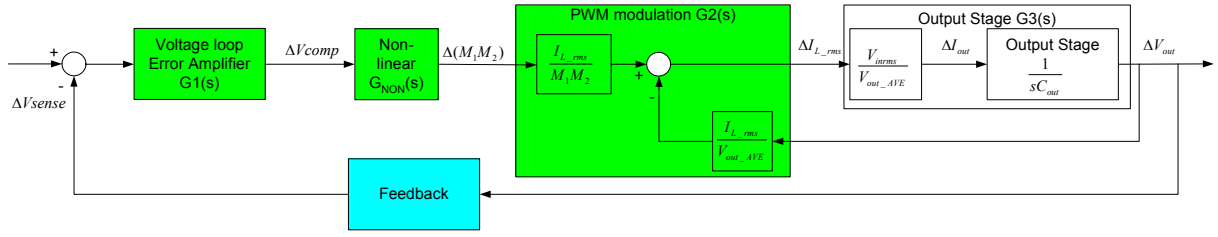


Figure 9 Small signal modeling of voltage loop

4.1 Boost converter output stage $G_3(s)$

Boost converter output stage is described as influencing of variation on i_L to bulk output voltage Vout. The transfer function of power stage, $G_3(s)$, is separated to two stages as:

$$G_3(s) = \frac{\Delta V_{out}}{\Delta I_{L_rms}} = \frac{\Delta V_{out}}{\Delta I_{out}} \cdot \frac{\Delta I_{out}}{\Delta I_{L_rms}} \tag{15}$$

where V_{out} is the DC output voltage, I_{out} the DC output current and I_{L_rms} is the boost inductor current.

4.1.1 ΔV_{out} / ΔI_{out}

Under the above assumption, the power stage can be modeled as illustrated in Figure 10: a controlled current source (with a shunt resistor Re) that drives the output bulk capacitor C_{out} and the load resistance Rout (= Vout / Iout). The zero due to the ESR associated with C_{out} is far beyond the crossover frequency thus it is neglected.

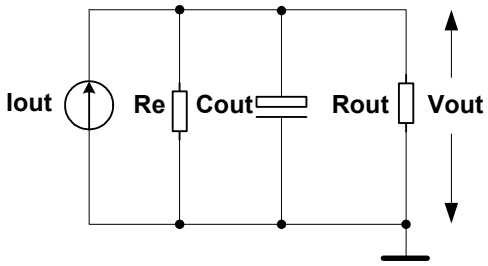


Figure 10 Power stage modeling

A few algebraic manipulations would show that the shunt resistor Re always equals the DC load resistance Rout, thus it changes depending on the power delivered by the system. There are two kinds of load in the application. Two cases will give a different result in case of resistive load or constant power load. For purely resistive load, the AC load resistance equals Ro. In case of constant power load like additional isolated PWM DC/DC converter, the AC load resistance is equal to -Ro (if the DC bus decreases, the current demanded of the PFC increases. hence the negative sign is shown.). As a result, the parallel combination with Re tends to infinity and the two resistances cancel. The current source drives only the output capacitor. The result is summarized as below:

$$\frac{\Delta V_{out}}{\Delta I_{out}} = \begin{cases} \dfrac{R_{out}}{2(1+s\cdot\dfrac{R_{out}C_{out}}{2})} & \text{Resistive Load} \\ \dfrac{1}{sC_{out}} & \text{Constant Power Load} \end{cases} \quad (16)$$

In this application note, the calculation is only carried out for constant power load situation

4.1.2 ΔI_{out} / ΔI_{L_rms}

The current source Iout can be characterized with the following considerations as shown in Figure 11. The low frequency component of the boost diode current is found by averaging the discharge portion of the inductor current over a given switching cycle. The low frequency current, averaged over a mains half-cycle yields the DC output current Iout:

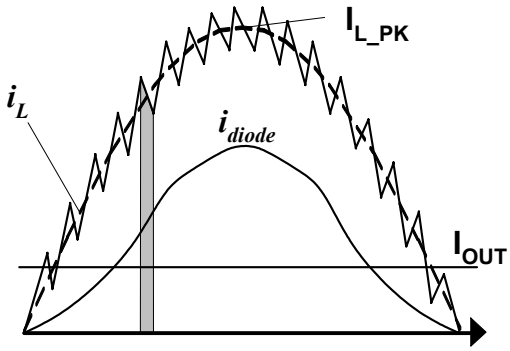


Figure 11 The simplification and characterization for I_{out} / I_{L_rms}

$$I_{out} = \frac{1}{\pi}\int_0^{\pi}(1-D_{on})I_{L_PK}Sin\alpha d\alpha = \frac{2V_{inrms}I_{L_rms}}{\pi V_{out_AVE}}\int_0^{\pi}(Sin\alpha)^2 d\alpha = \frac{V_{inrms}I_{L_rms}}{V_{out_AVE}} \quad (17)$$

So,

$$\frac{\Delta I_{out}}{\Delta I_{L_rms}} = \frac{V_{inrms}}{V_{out_AVE}} \quad (18)$$

where, Don is the switch duty cycle; α is the instantaneous phase angle of the mains voltage, Vinrms is the input RMS voltage value, I_{L_PK} is choke current sinewave peak value and V_{out_AVE} is the averaging bulk DC output voltage.

In case of constant power load, the transfer function of $G_3(s)$ is:

$$G_3(s) = \frac{\Delta V_{out}}{\Delta I_{L_rms}} = \frac{\Delta V_{out}}{\Delta I_{out}} \cdot \frac{\Delta I_{out}}{\Delta I_{L_rms}} = \frac{V_{inrms}}{V_{out_AVE}} \cdot \frac{1}{sC_{out}} \quad (19)$$

4.2 Small signal transfer function of $\Delta V_{out}/\Delta(M_1M_2)$ for voltage loop analysis

There is a internal feedback from Vout to $G_2(s)$. this inner loop has to be solved to obtain the transfer function of $\Delta V_{out}/\Delta(M1M2)$. Rewrite the equation (14) at input voltage RMS point:

$$I_{L_rms} = \frac{K_{FQ}M_1M_2V_{inrms}}{K_1R_{sense}V_{out}} \quad (20)$$

making a perturbation on I_{L_rms}, (M_1M_2), V_{out}, then

$$\Delta I_{L_rms} = \frac{I_{L_rms}}{M_1M_2}\Delta(M_1M_2) - \frac{I_{L_rms}}{V_{out_AVE}}\Delta V_{out} \quad (21)$$

replacing ΔI_{L_rms} by $\Delta V_{out}/G_3(s)$ according to voltage loop block diagram,

$$\frac{\Delta V_{out}}{G_3(s)} = \frac{I_{L_rms}}{M_1M_2}\Delta(M_1M_2) - \frac{I_{L_rms}}{V_{out_AVE}}\Delta V_{out} \quad (22)$$

then the transfer function of dV_{out}/dV_{comp} is

$$G_{23}(s) = \frac{\Delta V_{out}}{\Delta(M_1M_2)} = \frac{\frac{V_{out_AVE}}{M_1M_2}}{\frac{V_{out_AVE}^2 C_{out}}{I_{L_rms}V_{inrms}}s+1} = \frac{\frac{V_{out_AVE}}{M_1M_2}}{\frac{K_1R_{sense}V_{out_AVE}^3 C_{out}}{K_{FQ}M_1M_2V_{inrms}^2}s+1} \quad (23)$$

With $f_{23} = \frac{1}{2\pi\frac{K_1R_{sense}V_{out_AVE}^3 C_{out}}{K_{FQ}M_1M_2V_{inrms}^2}}$,

$$G_{23}(s) = \frac{\Delta V_{out}}{\Delta(M_1M_2)} = \frac{\frac{V_{out_AVE}}{M_1M_2}}{1+\frac{s}{2\pi f_{23}}} \quad (24)$$

4.3 Nonlinear block $G_{NON}(s)$

The Vcomp voltage is sent to nonlinear gain block. The output of nonlinear is two internal variables, M1 and M2. The two variables are used to define boost choke current amplitude I_L as in equation (14). The characteristic of nonlinear gain block is shown in Table 1 and Figure 12. The small signal gain between Δ(M1*M2) and ΔVcomp can be derived as well at different operating point.

Vcomp	M1	M2	M1*M2
0	0.048	1.330E-02	6.384E-04
1.5	0.048	1.330E-02	6.384E-04
1.85	0.0517	1.920E-02	9.926E-04
2	0.0551	3.860E-02	2.127E-03
2.5	0.101	1.790E-01	1.808E-02
3	0.184	3.350E-01	6.164E-02
3.5	0.316	5.080E-01	1.605E-01
4	0.477	7.160E-01	3.415E-01
4.5	0.629	9.830E-01	6.183E-01
5	0.752	1.368E+00	1.029E+00
5.5	0.846	1.879E+00	1.590E+00
5.6	0.888	1.968E+00	1.748E+00
6	0.906	1.982E+00	1.796E+00
6.5	0.906	1.987E+00	1.800E+00
7	0.906	1.987E+00	1.800E+00

Table 1 nonlinear block characteristic data

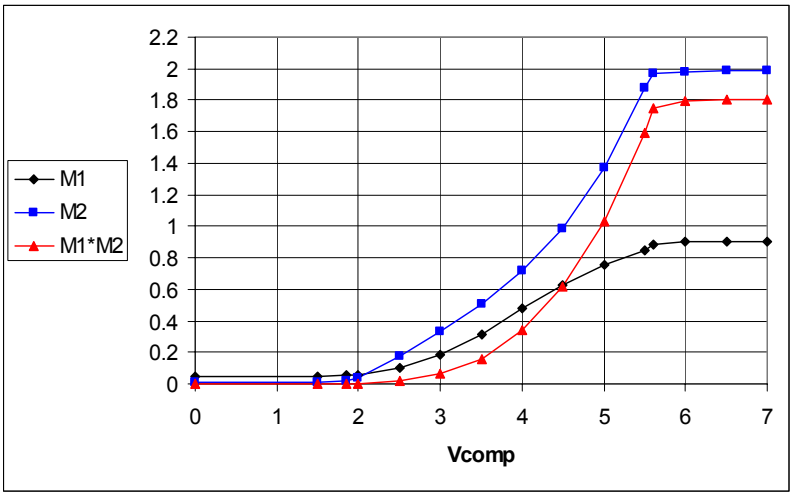


Figure 12 The characteristics of nonlinear block

4.4 Error Amplifier compensation $G_1(s)$

The circuit of error amplifier compensation circuit is shown in Figure 13. The sensing voltage Vsense is compared to internal reference voltage 5V typical. The difference between Vsense and internal reference is sent to transconductance error amplifier and converted to a current source to charge or discharge the RC components in Vcomp Pin.

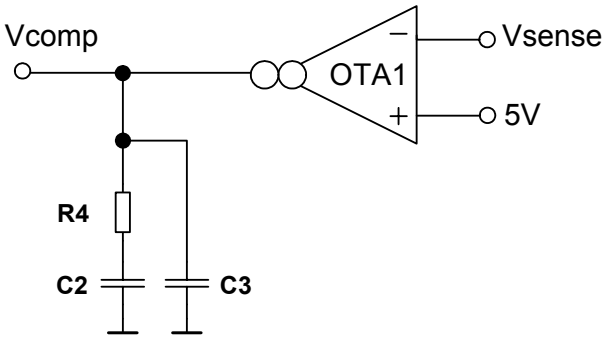


Figure 13 Error Amplifier compensation $G_1(s)$

The transfer function is:

$$G_1(s) = \frac{\Delta V_{comp}}{\Delta V_{sense}} = \frac{\Delta V_{comp}}{\Delta I_{OTA1}} \cdot \frac{\Delta I_{OTA1}}{\Delta V_{sense}} = \frac{1 + sR_4C_2}{(C_2 + C_3)s(1 + s\frac{R_4C_2C_3}{C_2 + C_3})} \cdot g_{OTA1} \quad (25)$$

where, g_{OTA1} is the trans-conductance of OTA1, 42uS typically for ICE1PCS01.

With $f_{CZ} = \frac{1}{2\pi R_4 C_2}$ and $f_{CP} = \frac{1}{2\pi \frac{R_4C_2C_3}{C_2 + C_3}}$,

$$G_1(s) = \frac{g_{OTA1}(1 + s/2\pi f_{CZ})}{(C_2 + C_3)s(1 + s/2\pi f_{CP})} \quad (26)$$

The pole and zero are to regulate the overall voltage loop with the cross-over frequency below 100Hz and create the phase margin for the loop stability.

4.5 Feedback $G_4(s)$

The Feedback block is a simple voltage divider to monitor the bulk capacitor output voltage. The circuit is shown in Figure 14.

$$G_4(s) = \frac{\Delta V_{sense}}{\Delta V_{out}} = \frac{R_2}{R_1 + R_2} \quad (27)$$

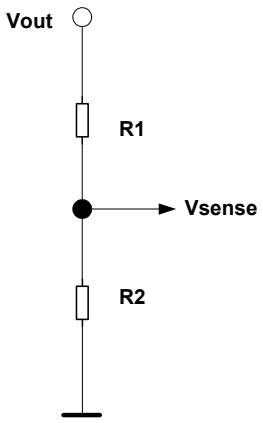


Figure 14 bulk voltage sensing divider

4.6 Overall Open Loop Transfer Function $G_V(s)$

With combining all of the blocks above, the overall open loop gain for voltage loop is equal to:

$$G_V(s) = G_1(s)G_{NON}(s)G_{23}(s)G_4(s) \quad (28)$$

Due to PF requirement, inherent PFC dynamic voltage loop compensation is always implemented with low bandwidth in order not to make the response for $2*f_L$ ripple. For example, for 50Hz AC line input, PFC voltage loop bandwidth is normally set below 20Hz. The compensation circuit R4, C2 and C3 are used to optimize the loop gain and phase margin.

4.7 Enhance dynamic response

As mentioned in Section 4.6, the inherent low bandwidth of voltage loop in PFC application will lead to slow response in case of sudden load step and result in large output overshoot or drop. Enhance dynamic response feature is integrated in ICE1PCS01 to have a fast response in the case of load step. The voltage loop with including enhance dynamic response block is shown in Figure 15.

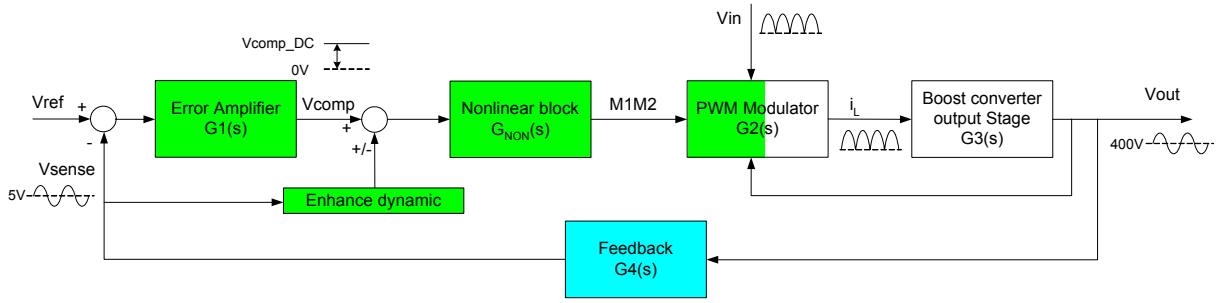


Figure 15 voltage loop block diagram including enhance dynamic response

When Vsense voltage variation is within -5% to +5% of nominal value, there is no function of enhance dynamic response block. However, when Vsense variation is out of such +/-5% range, enhance block will add offset voltage on top of Vcomp voltage to influence the current amplitude.

For Vsense variation < -5% of nominal value, the offset voltage is +2V maximum. For Vsense variation > +5% of nominal value, the offset voltage is -4V minimum. The timing diagram of enhance dynamic response operation is shown in Figure 16 with sudden load jump situation. It can be seen that during enhance dynamic operation, the high current of boost choke is delivered for fast response. Within half sinusoidal period, when Vsense operating around the boundary of -5% threshold, the first part of boost choke current follows high amplitude profile due to enhance mode offset and the rest of boost choke current come back to low amplitude profile without enhance mode offset. When Vsense voltage is pulled back within +/-5% range, enhance dynamic offset disappear and boost choke current waveform will stay as perfect sinusoidal shape.

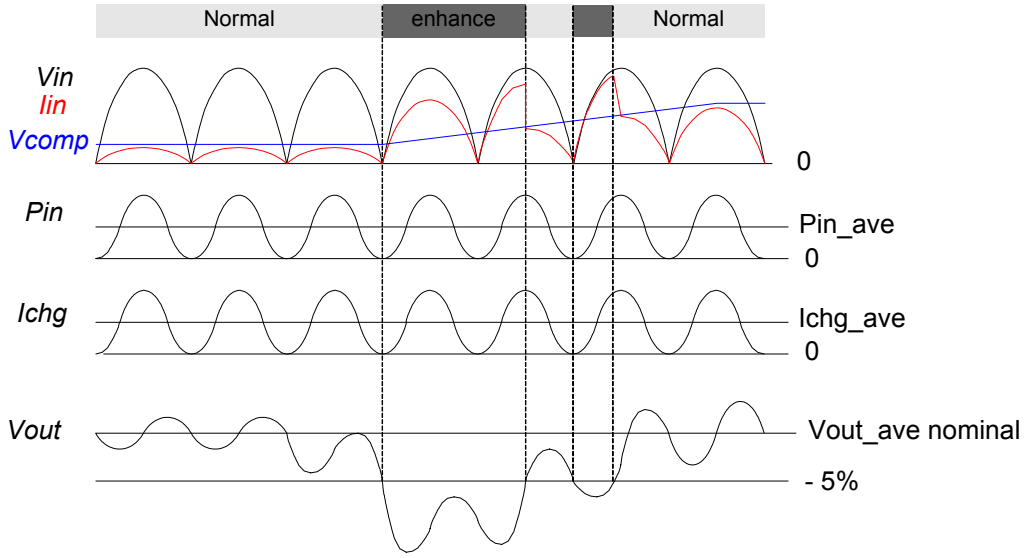


Figure 16 timing diagram for enhance dynamic operation

5 Design Example

Assuming a 300W application with universal input AC voltage 85~265VAC,

constant power load
efficiency=88%
Vout=400VDC
Cout=220uF/450V
f_{SW}=125kHz
Rsense=0.1ohm
Boost choke inductance L=1.2mH
Vsense divider: R1=390kohm*2=780kohm, R2=10kohm

5.1 Vcomp and M1, M2 value at full load condition

(1) 85VAC:

RMS AC input current under full load:

$$I_{L_rms_85} = \frac{P_{out}}{\eta \cdot V_{inrms_85}} = \frac{300}{0.88 \cdot 85} = 4.01A \tag{29}$$

From equation (14),

$$M_1 M_2\big|_{85VAC} = \frac{I_{L_rms_85} K_1 R_{sense} V_{out}}{K_{FQ} V_{inrms_85}} = \frac{4.01 \cdot 7 \cdot 0.1 \cdot 400}{9.183 \cdot 85} = 1.438 \tag{30}$$

From table 1 and Figure 12, it can be obtained

Vcomp	M1	M2	M1*M2
5	0.752	1.368E+00	1.029E+00
5.5	0.846	1.879E+00	1.590E+00

With Linear approximation:

$$V_{comp_85} = V_{comp_1} + \frac{M_1 M_2\big|_{85VAC} - M_1 M_2\big|_{Vcomp_1}}{M_1 M_2\big|_{Vcomp_2} - M_1 M_2\big|_{Vcomp_1}} \cdot (V_{comp_2} - V_{comp_1})$$

$$V_{comp_85} = 5 + \frac{1.438 - 1.029}{1.59 - 1.029} \cdot (5.5 - 5) = 5.365V \tag{31}$$

$$M_1\big|_{85VAC} = M_{1_1} + \frac{M_{1_2} - M_{1_1}}{V_{comp_2} - V_{comp_1}} \cdot (V_{comp_85} - V_{comp_1})$$

$$M_1\big|_{85VAC} = 0.752 + \frac{0.846 - 0.752}{5.5 - 5} \cdot (5.365 - 5) = 0.821 \tag{32}$$

$$M_2\big|_{85VAC} = M_{2_1} + \frac{M_{2_2} - M_{2_1}}{V_{comp_2} - V_{comp_1}} \cdot (V_{comp_85} - V_{comp_1})$$

$$M_2\big|_{85VAC} = 1.368 + \frac{1.879 - 1.368}{5.5 - 5} \cdot (5.365 - 5) = 1.741 \tag{33}$$

The small signal gain of nonlinear block is

$$G_{NON}(s)\big|_{85VAC} = \frac{M_1M_2\big|_{Vcomp_2} - M_1M_2\big|_{Vcomp_1}}{V_{comp_2} - V_{comp_1}} = \frac{1.590 - 1.029}{5.5 - 5} = 1.122 \quad (34)$$

The inherent pole of f_{23} is

$$f_{23}\big|_{85VAC} = \frac{1}{2\pi \frac{K_1 R_{sense} V_{out_AVE}{}^3 C_{out}}{K_{FQ} \cdot (M_1M_2)\big|_{85VAC} \cdot V_{inrms_85}{}^2}} = 1.5406Hz \quad (35)$$

(2) 265VAC

RMS AC input current under full load:

$$I_{L_rms_265} = \frac{P_{out}}{\eta \cdot V_{inrms_265}} = \frac{300}{0.88 \cdot 265} = 1.286A \quad (36)$$

From equation (14),

$$M_1M_2\big|_{265VAC} = \frac{I_{L_rms_265} K_1 R_{sense} V_{out}}{K_{FQ} V_{inrms_265}} = \frac{1.286 \cdot 7 \cdot 0.1 \cdot 400}{9.183 \cdot 265} = 0.148 \quad (37)$$

From table 1 and Figure 12, it can be obtained

Vcomp	M1	M2	M1*M2
3	0.184	3.350E-01	6.164E-02
3.5	0.316	5.080E-01	1.605E-01

With Linear approximation:

$$V_{comp_265} = V_{comp_1} + \frac{M_1M_2\big|_{265VAC} - M_1M_2\big|_{Vcomp_1}}{M_1M_2\big|_{Vcomp_2} - M_1M_2\big|_{Vcomp_1}} \cdot (V_{comp_2} - V_{comp_1})$$
$$V_{comp_265} = 3 + \frac{0.148 - 0.06164}{0.1605 - 0.06164} \cdot (3.5 - 3) = 3.437V \quad (38)$$

$$M_1\big|_{265VAC} = M_{1_1} + \frac{M_{1_2} - M_{1_1}}{V_{comp_2} - V_{comp_1}} \cdot (V_{comp_265} - V_{comp_1})$$
$$M_1\big|_{265VAC} = 0.184 + \frac{0.316 - 0.184}{3.5 - 3} \cdot (3.437 - 3) = 0.299 \quad (39)$$

$$M_2\big|_{265VAC} = M_{2_1} + \frac{M_{2_2} - M_{2_1}}{V_{comp_2} - V_{comp_1}} \cdot (V_{comp_265} - V_{comp_1})$$
$$M_2\big|_{265VAC} = 0.335 + \frac{0.508 - 0.335}{3.5 - 3} \cdot (3.437 - 3) = 0.486 \quad (40)$$

The small signal gain of nonlinear block is

$$G_{NON}(s)\big|_{265VAC} = \frac{M_1M_2\big|_{Vcomp_2} - M_1M_2\big|_{Vcomp_1}}{V_{comp_2} - V_{comp_1}} = \frac{0.1605 - 0.06164}{3.5 - 3} = 0.198 \quad (41)$$

The inherent pole of f_{23} is

$$f_{23}\big|_{265VAC} = \frac{1}{2\pi \frac{K_1 R_{sense} V_{out_AVE}{}^3 C_{out}}{K_{FQ} \cdot (M_1 M_2)\big|_{265VAC} \cdot V_{inrms_265}{}^2}} = 1.5412Hz \quad (42)$$

5.2 Current Averaging Circuit

With g_{OTA2}=1.1mS from Datasheet, M1@85VAC, and assuming f_{AVE}=24kHz which is 5 times less than switching frequency 125kHz, then

$$C_{icomp} \geq \frac{g_{OTA2} M_1\big|_{85VAC}}{K_1 \cdot 2\pi f_{AVE}} = \frac{1.1E-3 \cdot 0.821}{7 \cdot 2\pi \cdot 24E3} = 0.86nF \quad (43)$$

Select C_{icomp}=1nF

5.3 Current Loop Regulation

Insert M1 and M2 value in equation (11). The amplitude and phase angle of $G_C(s)$ is shown in Figure 17 to verify the stability of current loop and the requirement of f_C less than switching frequency.

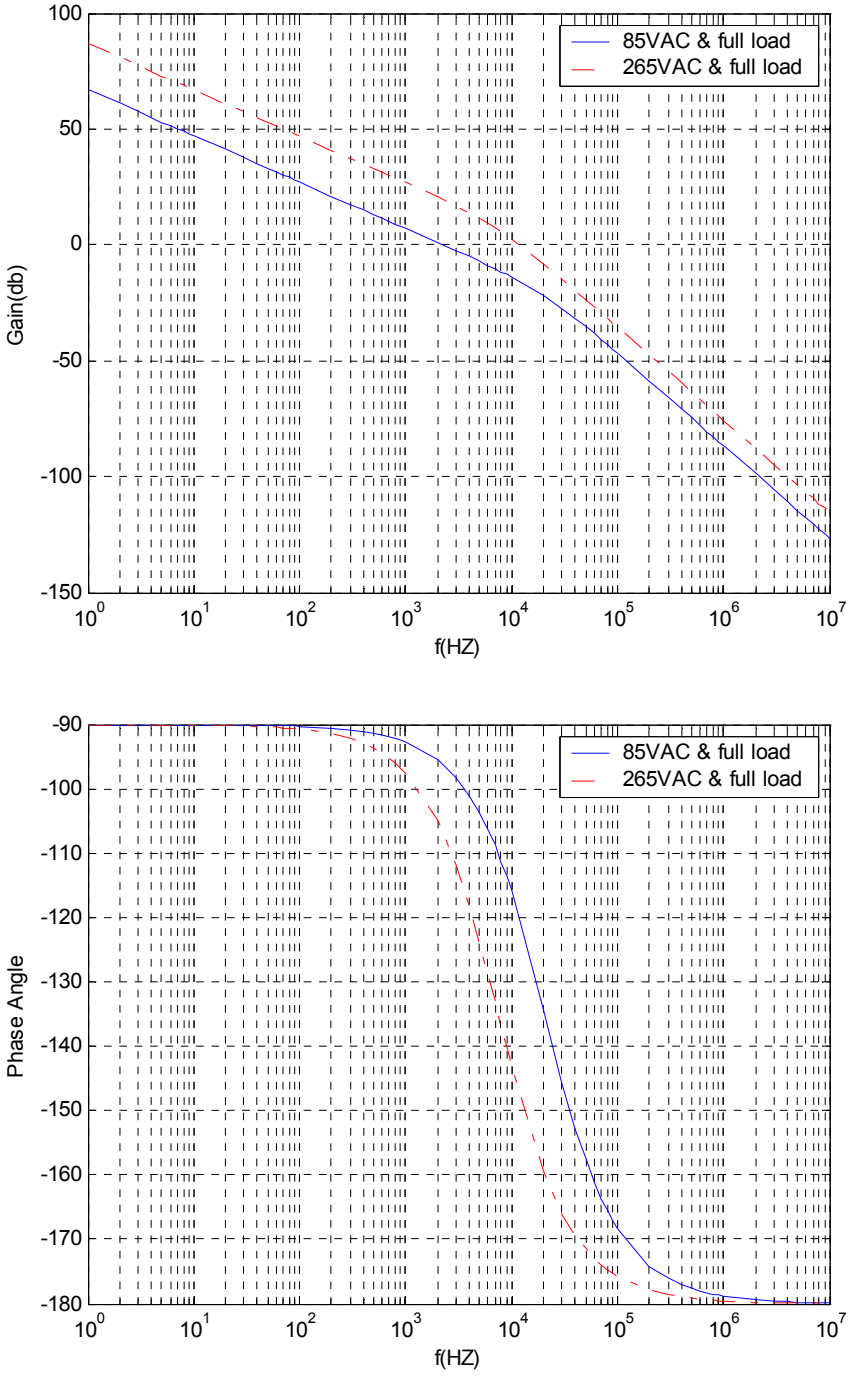


Figure 17 The bode plot and phase angle for current loop

The cross over frequency and phase margin are 2kHz and 85º for 85VAC, and 11kHz and 35º for 265VAC.

5.4 Voltage Loop Regulation

From the above sections, it can be obtained:

$$G_1(s) = \frac{\Delta V_{comp}}{\Delta V_{sense}} = \frac{g_{OTA1}(1 + s/2\pi f_{CZ})}{(C_2 + C_3)s(1 + s/2\pi f_{CP})} \quad (44)$$

$$G_{NON}(s) = \frac{\Delta(M_1 M_2)}{\Delta V_{comp}} \quad (45)$$

$$G_{23}(s) = \frac{\Delta V_{out}}{\Delta(M_1 M_2)} = \frac{\frac{V_{out_AVE}}{M_1 M_2}}{1 + \frac{s}{2\pi f_{23}}} \quad (46)$$

$$G_4(s) = \frac{\Delta V_{sense}}{\Delta V_{out}} = \frac{R_2}{R_1 + R_2} = \frac{5}{400} = 0.0125 \quad (47)$$

The open loop gain for voltage loop is to times all above factors together as:

$$G_V(s) = G_1(s) G_{NON}(s) G_{23}(s) G_4(s)$$

$G_1(s)$ is used to provide enough phase margin and also limit the bandwidth below 20HZ. R4, C2 and C3 can be chosen as required. f_{CZ} normally select to be compensate the pole in $G_{23}(s)$. f_{CP} normally select to be 40~70Hz in order to fast put down the gain amplitude and reject the high frequency interference. In this example f_{23} is equal to 1.5406Hz at 85VAC and full load and 1.5412Hz at 265VAC and full load respectively. So the initial target is: f_{CZ} is chosen to be close to 1.5Hz, and f_{CP} is chosen to be 50Hz.

C2 and C3 is calculated to obtain Gv(s) cross over frequency around 10Hz. The gain amplitude of $G_{NON}*G_{23}*G_4$ in 85VAC and full load is shown in Figure 18. It can be seen that at f=10Hz, the gain is about -4.52dB. So G1 should provide the gain +4.52dB at f=10Hz. Considering that C2>>C3 due to fcz<fcp and 10Hz>>1Hz=f_{CZ}, then

$$G_1(10Hz) = \frac{g_{OTA1} \, 10Hz/1Hz}{C_2 \cdot 2\pi \cdot 10Hz} = +4.52dB$$

$$C_2 = \frac{42 \cdot 10^{-6} \cdot \frac{10Hz}{1Hz}}{10^{4.52/20} \cdot 2\pi \cdot 10Hz} = 3.97\mu F \quad (48)$$

3.97uF is not common for ceramic type capacitor. So select C_2=1uF, then f_{CZ} is recalculated as:

$$G_1(10Hz) = \frac{g_{OTA1}\sqrt{1+(10Hz/f_{CZ})^2}}{C_2 \cdot 2\pi \cdot 10Hz} = +4.52dB$$

$$f_{CZ} = \frac{10Hz}{\sqrt{\left(\frac{1\mu F \cdot 10^{4.52/20} \cdot 2\pi \cdot 10Hz}{42 \cdot 10^{-6}}\right)^2 - 1}} = 4.33Hz \quad (49)$$

according to $f_{CZ} = \frac{1}{2\pi R_4 C_2} = 4.33Hz$ then

$$R_4 = \frac{1}{2\pi \cdot 4.33Hz \cdot C_2} = 36.8k\Omega \quad (50)$$

select R4=33kΩ, and $f_{CP} = \frac{1}{2\pi \frac{R_4 C_2 C_3}{C_2 + C_3}} \approx \frac{1}{2\pi R_4 C_3} = 50Hz$

$$C_3 = \frac{1}{2\pi \cdot 50Hz \cdot R_4} = 96.5nF \quad (51)$$

select C3=100nF

The gain amplitude and phase angle of overall voltage loop $G_V(s)$ at 85VAC and 265VAC in full load condition is shown in Figure 18 and Figure 19. At 85VAC, the cross over frequency f_V is around 8.5Hz and the phase margin is about 62°. At 265VAC, the cross over frequency f_V is around 14Hz and the phase margin is about 63°.

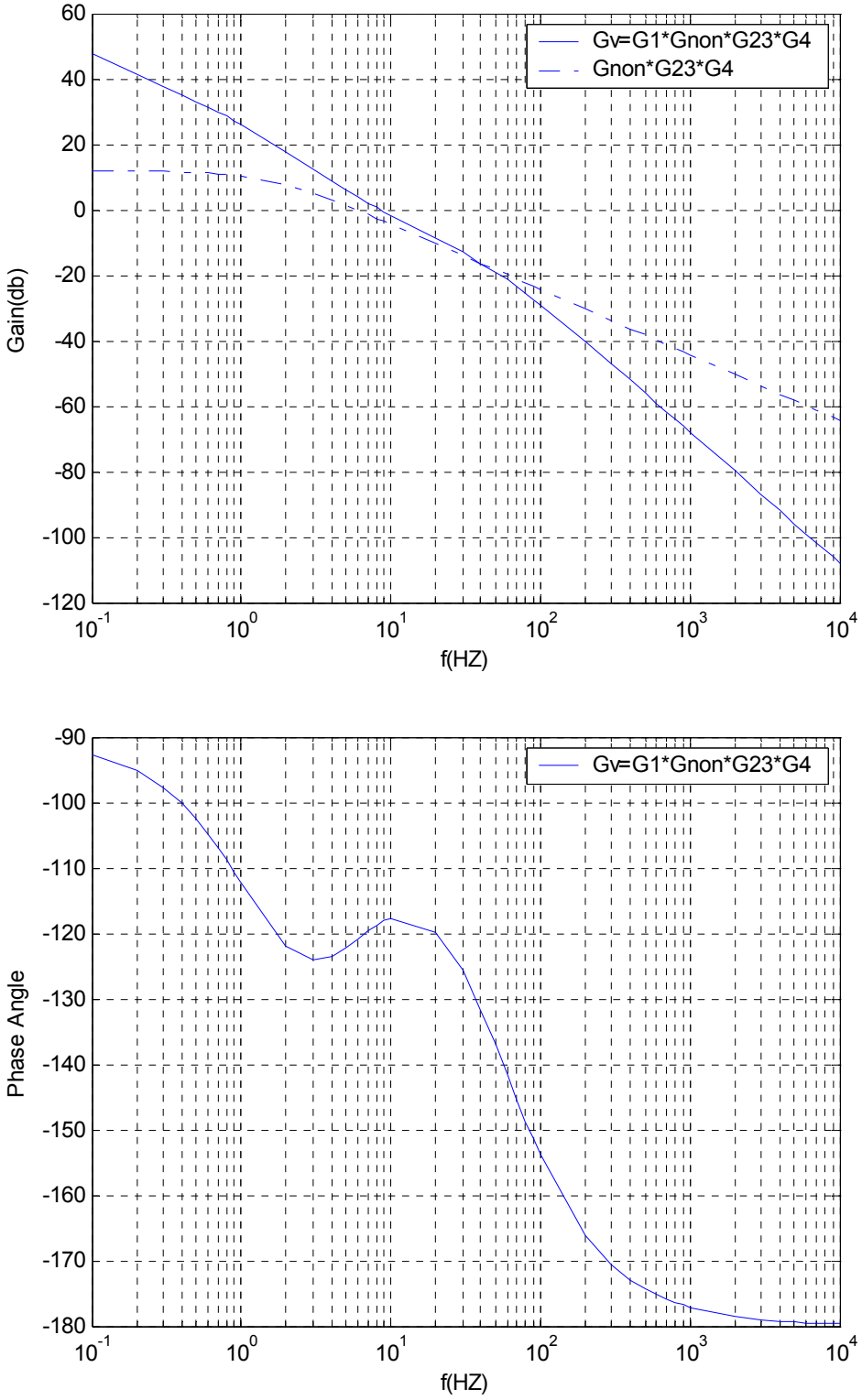


Figure 18 the bode plot and phase angle for voltage loop at 85VAC and full load

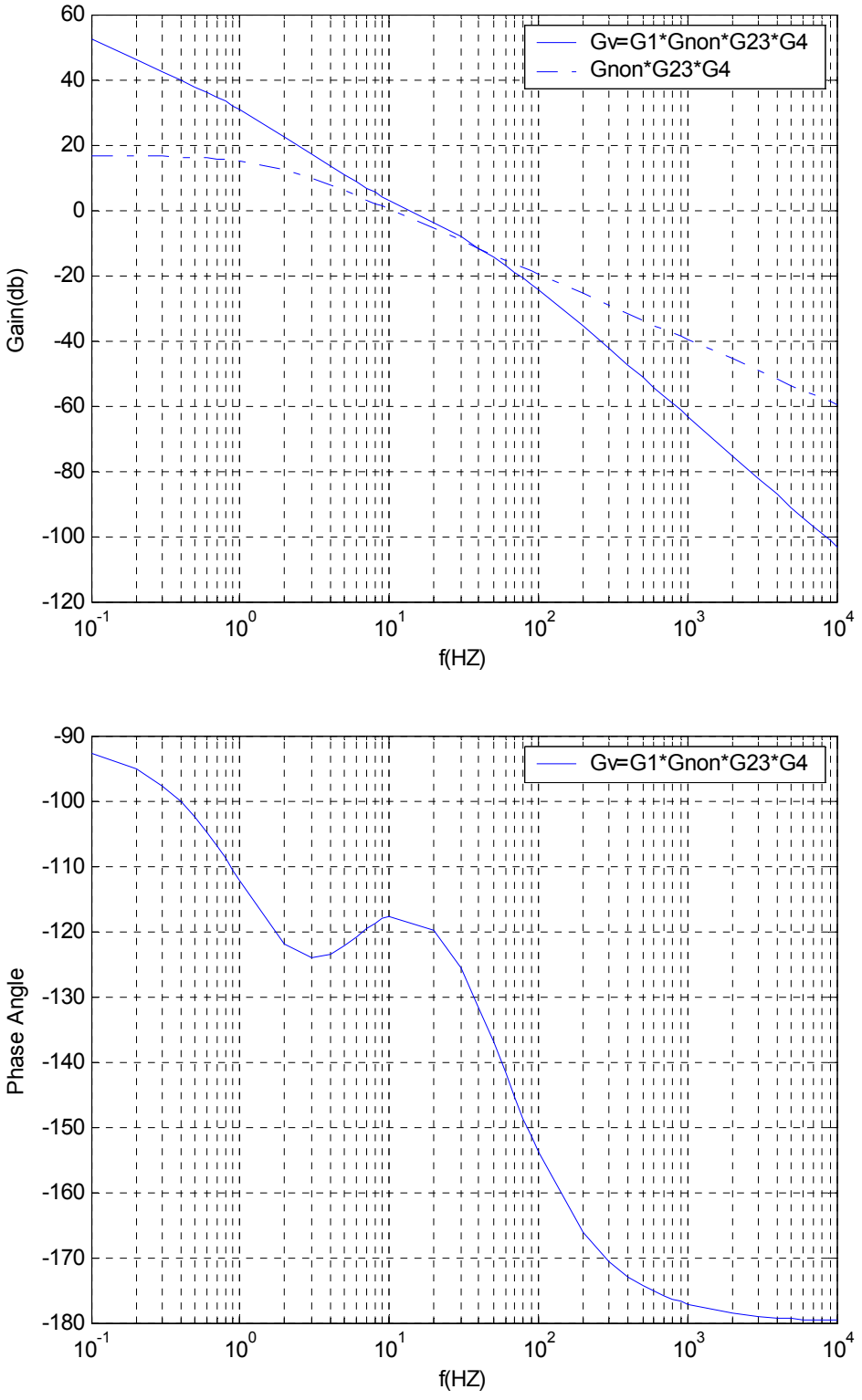


Figure 19 The bode plot and phase angle for voltage loop at 265VAC and full load

References

[1] Infineon Technologies: ICE1PCS01 - Standalone Power Factor Correction Controller in Continuous Conduction Mode; Preliminary datasheet; Infineon Technologies; Munich; Germany; Sept. 2002.

[2] Luo Junyang, Jeoh Meng Kiat, Huang Heng Cheong, A New Continuous Conduction Mode PFC IC With Average Current Mode Control, PEDS 2003; pp. 1110-1114, Nov 2003.

[3] Luo Junyang, Jeoh Meng Kiat, Yew Ming Lik, 300W CCM PFC Evaluation Board with ICE1PCS01, CoolMOS™ and SiC Diode thinQ!™, Application note, Infineon Technologies, Munich, Germany, Oct. 2003.