BCR601 linear LED controller IC with Active Headroom Control

Design guide for a linear LED controller IC with feedback loop to primary side

BCR601

About this document

Scope and purpose

This document presents a step-by-step design guide for a 60 V linear LED controller. Features include Active Headroom Control (AHC), precision current ripple suppression, over-voltage-, over-temperature- and hot plug protection. The IC is available in a PG-DSO-8 package.

Active headroom control is the realization of feedback to the primary side. It is an architecture that allows a linear LED controller to achieve maximum system efficiency by actively adjusting the AC-DC feedback loop to apply minimum voltage headroom on the output. By adjusting, and controlling a minimum necessary voltage across the LED array and linear pass element (transistor) on the output, system efficiency is optimized, and component temperatures are reduced. BCR601 enables the design of light drivers. A light driver supports a varying number of LED strings with different numbers and types of LEDs with one BCR601 architecture.

Intended audience

This document is intended for anyone wishing to design high-performance linear LED driver solutions with improved efficiency compared to common linear LED controllers. Primary side power converters usually consist of a power factor correction (PFC) and/or Flyback solution such as the XDPL8218. Output voltage regulation is achieved by the feedback (adjustment) from the secondary side (BCR601) controlling the PWM controller on the primary side.

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1 Introduction

This section gives an overview about key elements of a BCR601 LED system.

1.1 Product highlights

This section lists most important features of BCR601

- BCR601 supply voltage operating range 8 V to 60 V
- Supports use of NPN bipolar transistors and NMOSFETs
- 100 Hz/120 Hz supply voltage ripple suppression by highly effective current control loop
- Supports an opto-coupler feedback loop to primary side minimizing power losses
- Highly efficient internal direct feedback generation to primary controller (AHC)
- Over-temperature protection
- 3 percent analog dimming of LED current by a resistor R_{set} or DC voltage at the *MFIO* pin
- 8-pin PG-DSO-8 package
- LED short circuit protection
- Hot-plug capability
- Over-voltage protection (OVP)

1.2 Pin configuration

This section defines the purpose of every pin of the IC.

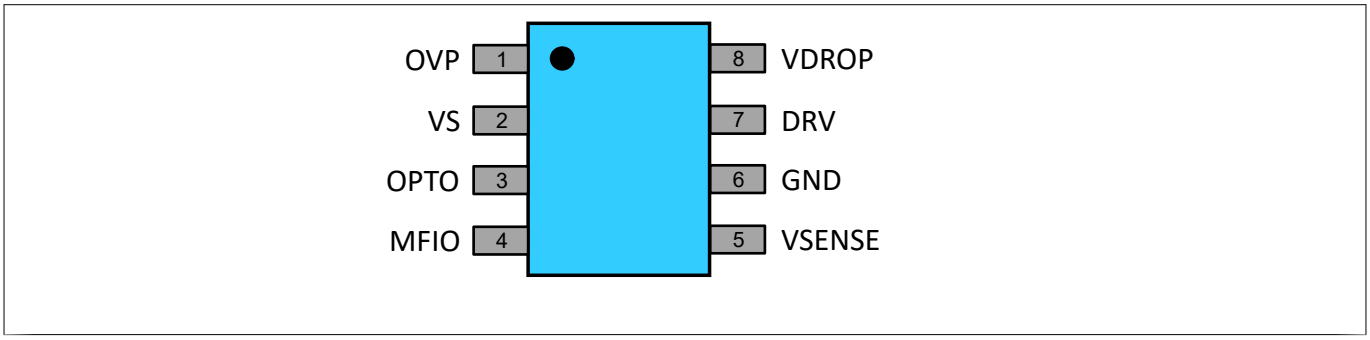


Figure 1 PG-DSO-8 pin out

Table 1 Pin configuration

Pin no.	Pin name	Pin type	Function
1	*OVP*	Input	Supply voltage measurement for over-voltage protection
2	*VS*	Input	Supply voltage
3	*OPTO*	Output	Output to control the opto-coupler current
4	*MFIO*	Input	Multifunctional IO for resistive and DC voltage dimming
5	*VSENSE*	Input	Measurement of V_{sense} voltage
6	*GND*	GND	IC ground
7	*DRV*	Output	Driver output to control base or gate of the external transistor
8	*VDROP*	Input	Measurement of V_{DROP} voltage

1.3 BCR601 theory of operation

This section describes applications using the BCR601 linear LED controller with active headroom control (AHC) .

The BCR601 is a linear LED controller IC typically found on the secondary side of an AC-DC power supply with a voltage output. The BCR601 controls a linear pass element such as a MOSFET or BJT transistor that is placed in series with the LED array. Feedback from the BCR601 to the primary side of the power converter adjusts the voltage headroom across the LED array optimizing efficiency. The following sections describes in detail the features and design requirements of the BCR601.

Typical target applications:

- LED driver

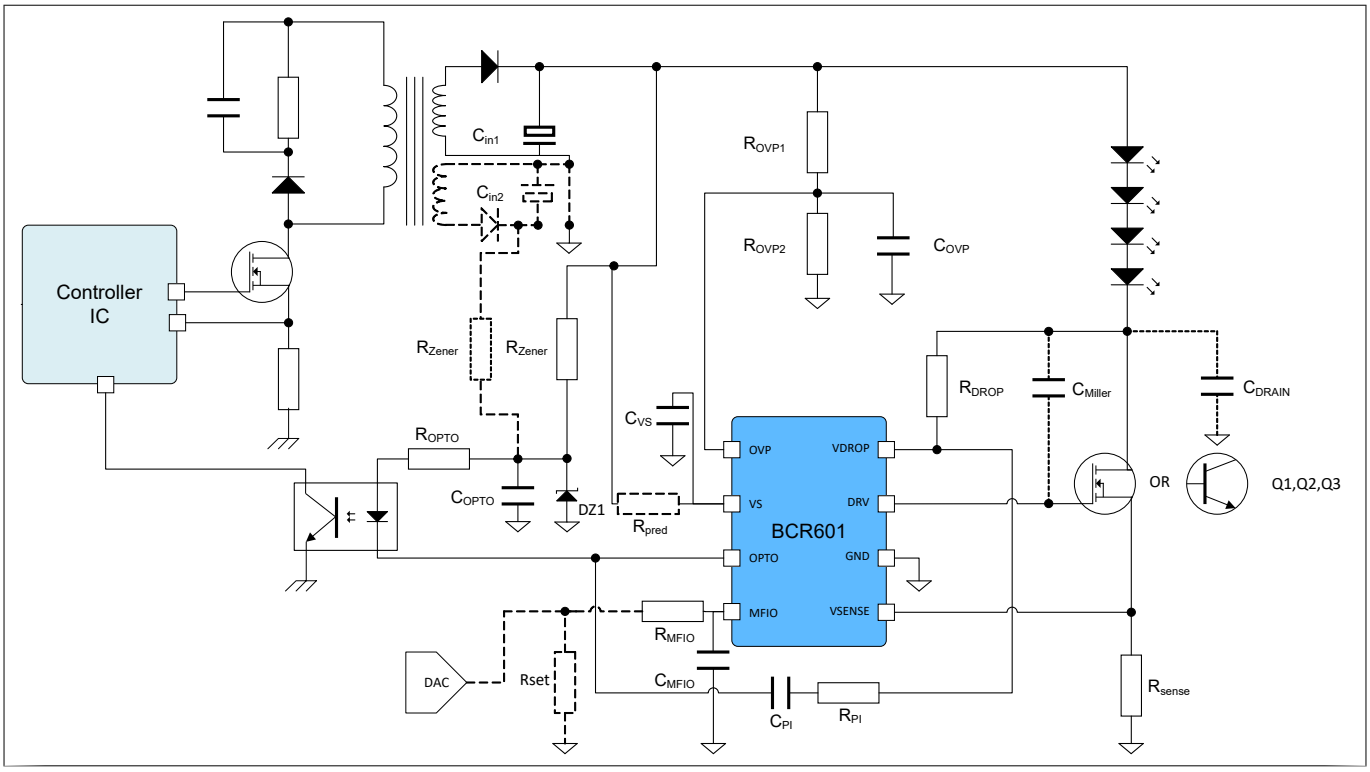


Figure 2 BCR601 typical application with AC-DC converter

1.4 Internal block diagram

This section shows the simplified internal block diagram of the BCR601.

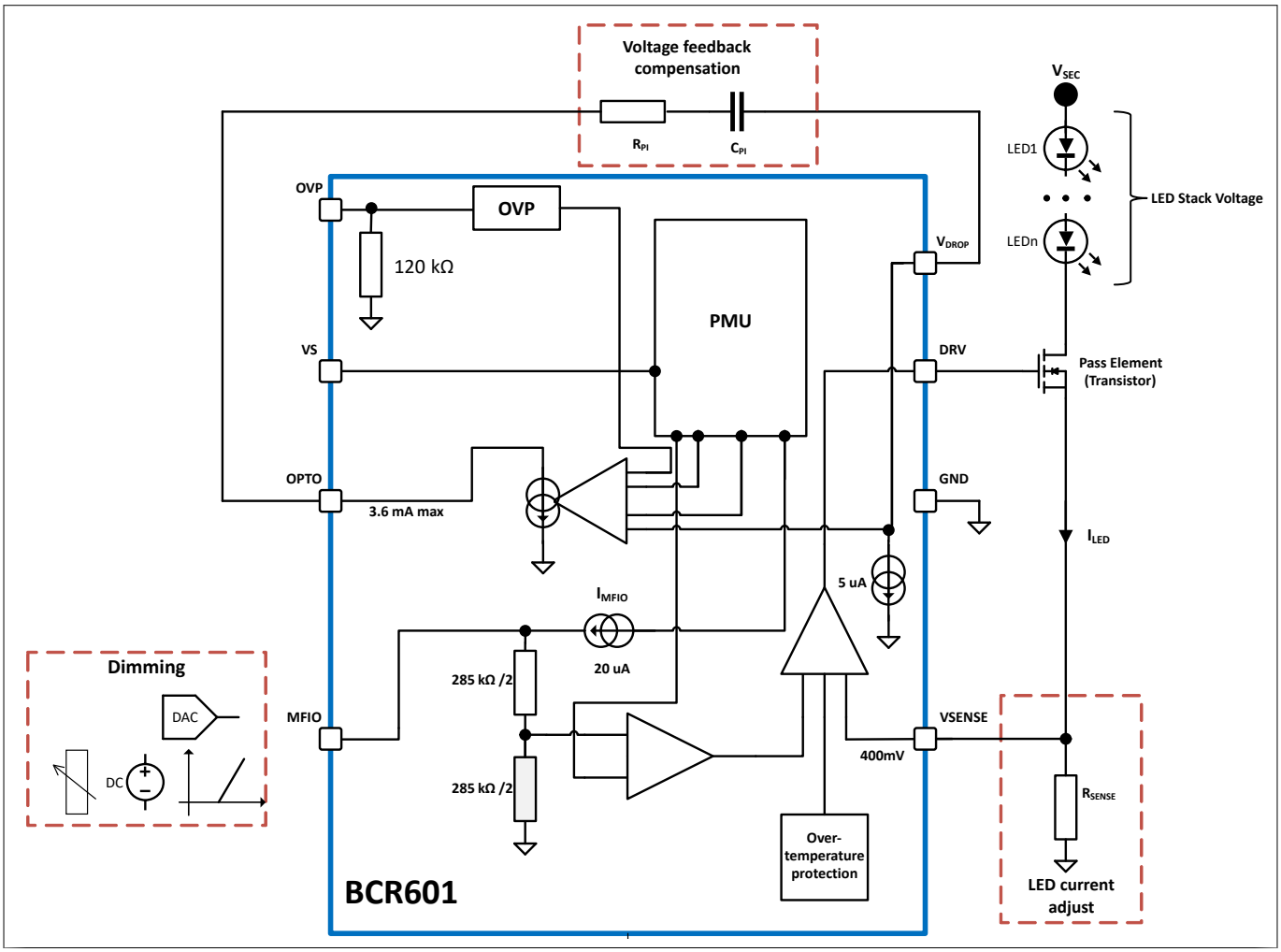


Figure 3 BCR601 top level block diagram

2 BCR601 detailed description

This section describes features and requirements for a fully functional and power optimized system configuration for BCR601.

The BCR601 is a single-channel linear LED controller with Active Headroom Control (AHC). It is used in LED lighting systems where a wide input voltage (up to 60 V) is required and efficiency optimization is desired. LEDs can vary their forward voltage considerably due to current density (forward current), and LED temperature. These two characteristics coupled with LED forward voltage drop variations due to the types of LEDs used forces the designer to ensure the voltage across the LED array and pass elements is large enough to satisfy all design requirements. The greater the difference between the LED array voltage and the input voltage to the linear pass element, the greater the power loss and temperature of the system. The BCR601 is an intelligent linear driver that actively adjust the over-head voltage to a minimum under all operating conditions.

Figure 3 illustrates a simplified internal block diagram of the BCR601 IC.

The BCR601 detailed description section of the BCR601 design document guides the designer how to use and optimize the BCR601 IC; topics include:

Optimization of the current and the voltage feedback loops

- Active Headroom Control (AHC) voltage feedback to the primary-side regulation,
  - Parameter settings of the analog PI controller via resistors and capacitors,
  - Tuning of the opto-coupler current to exploit the whole range of I_{OPTO} current and enable a failure-free operation over the whole range of current transfer ratios of the opto-coupler used including aging
- LED array current control and regulation via a calculated current sense resistor value for the system target current
- Optional tuning of the current loop in case of usage of highly amplifying Darlington-BJTs

Power loss optimization and protections of BCR601 and of the system.

- Minimizing the IC power consumption
- Minimizing voltage headroom across power transistor
- Configurable over-voltage protection tailored to the input voltage

Notable electrical specifications for the power transistor (pass element):

- Input capacitor value
- Threshold voltage
- In case of BJT current amplification

2.1 Setting LED target current

This section describes how to configure the target current of the application.

LED maximum current is configured via the current sense shunt resistor connected between pin *VSENSE* and ground.

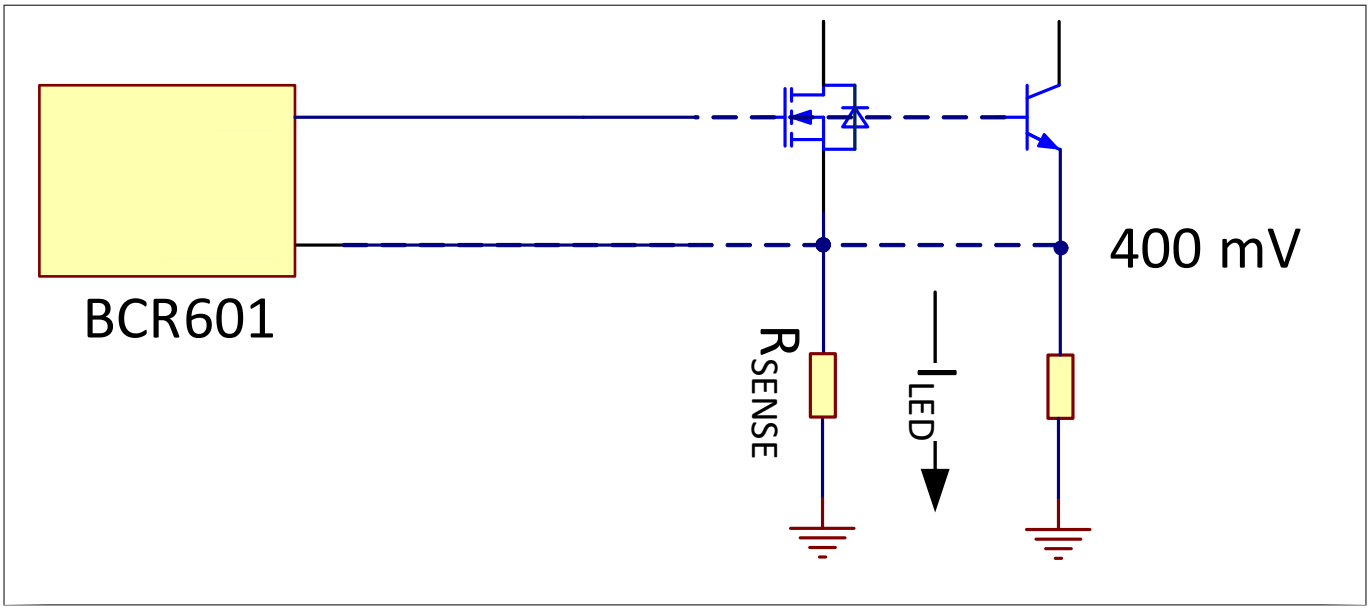


Figure 4 100 percent LED current set-point

Figure 4 illustrates current sense measurement using the BCR601. At 100 percent LED current output (non-dimming) the BCR601 regulates the current through the LED array so that the voltage drop over the shunt resistor is 400 mV. During dimming a fraction of the 400 mV regulation point is used and the final value depends on percentage of dimming.

The value of the series current sense resistor (R_{SENSE}) is determined by the formula:

$$R_{\mathrm{SENSE}} = \frac{400\ \mathrm{mV}}{I_{\mathrm{LED}}}$$

Equation 1 R_{SENSE} configuration

2.2 BCR601 dimming

This section describes means and aspects of dimming in a BCR601 system.

BCR601 LED driver systems can be dimmed by:

- Dimming by means of pin *MFIO*
  - Applying a DC signal between 0 V and 4 V (analog dimming)
  - Connecting a series resistor R_{SET} between pin *MFIO* and ground

2.2.1 BCR601 analog dimming

This section describes the means of dimming by applying a DC voltage to pin *MFIO*.

DC dimming is continuously increasing from the minimum dimming level at V_{MFIO} = 0.18 V up to the no dimming level starting at V_{MFIO} = 3.3 V.

For further information please refer to the datasheet.

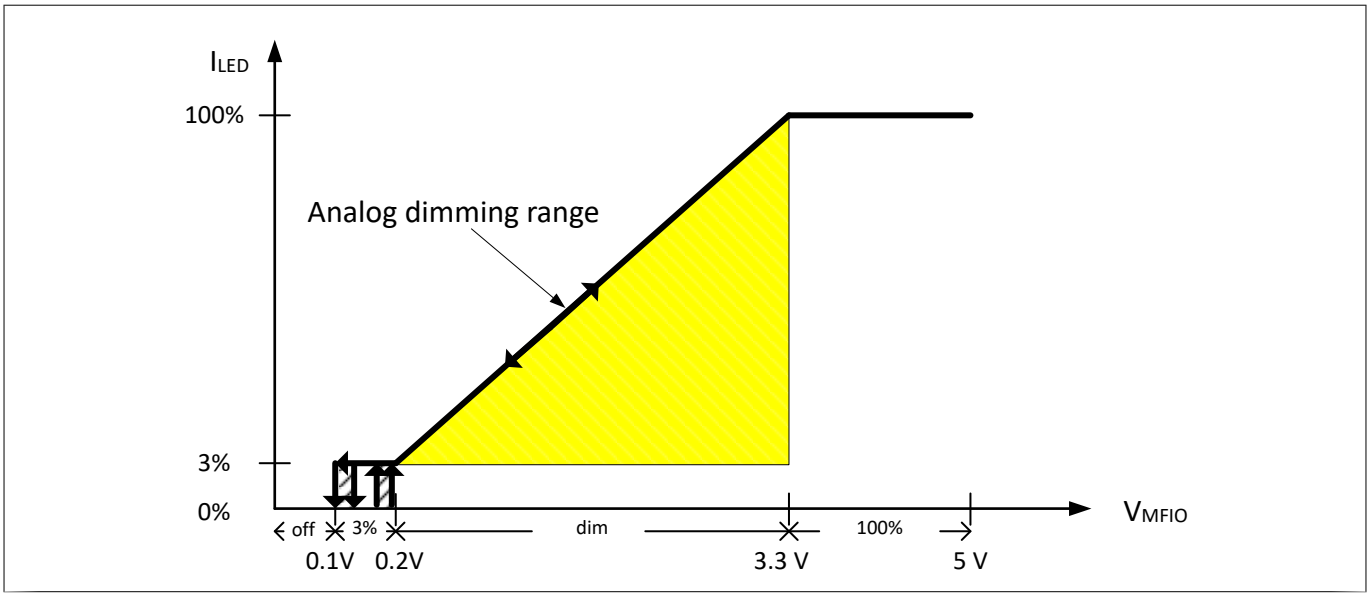
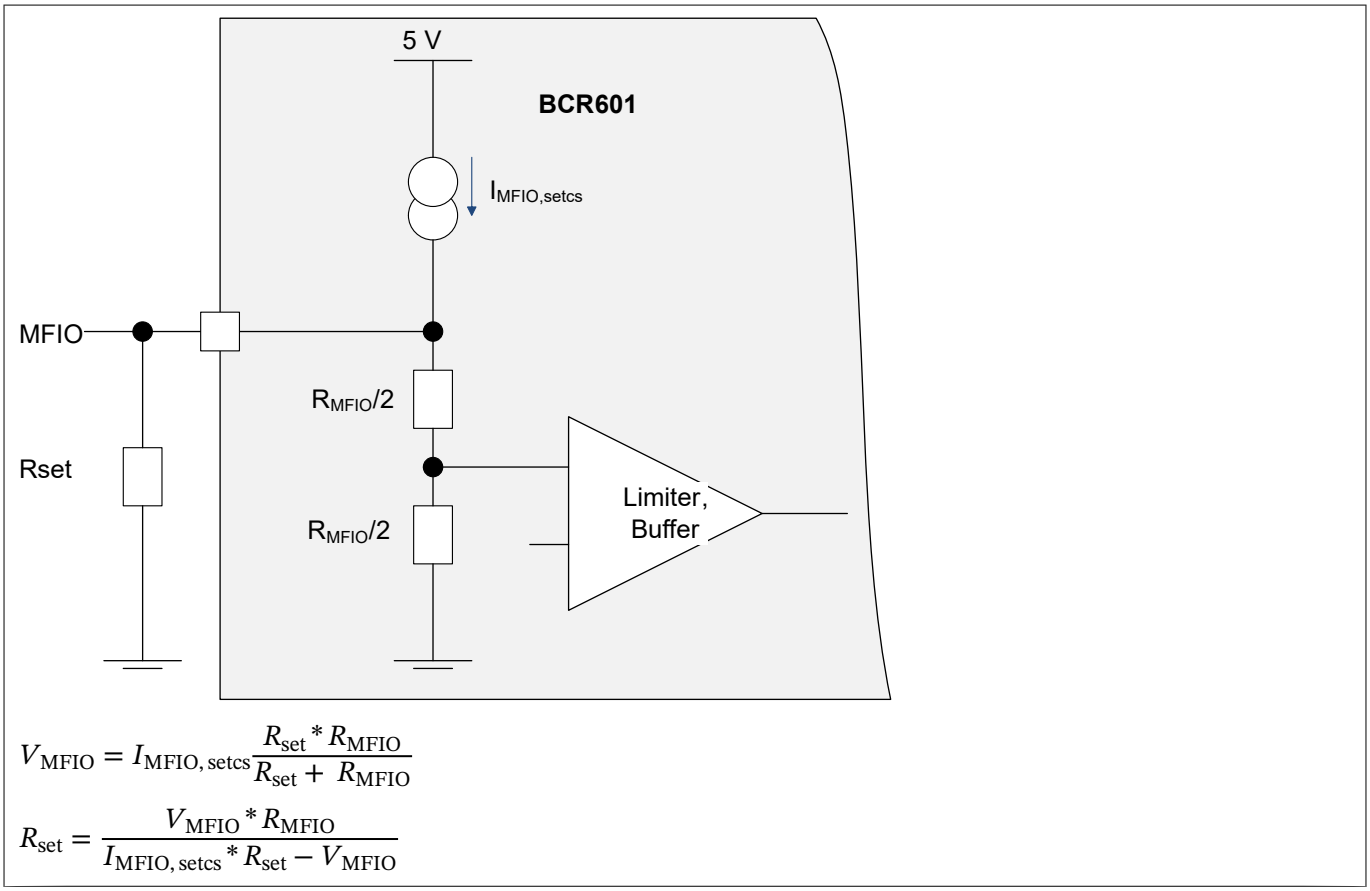


Figure 5 DC dimming curve

2.2.2 Resistor dimming

This section describes dimming to a fixed dimming value using an external resistor R_{set}.



$$V_{MFIO} = I_{MFIO,\,setcs} \frac{R_{set} * R_{MFIO}}{R_{set} + R_{MFIO}}$$

$$R_{set} = \frac{V_{MFIO} * R_{MFIO}}{I_{MFIO,\,setcs} * R_{set} - V_{MFIO}}$$

Figure 6 R_{set} dimensioning for resistor dimming

Figure 7 describes the correlation between R_{set} and the effective value for V_{MFIO}. Typical values to be used in the formula are:

- $R_{MFIO,typical}$ = 285 kΩ
- $I_{MFIO,setcs,typical}$ = 20 µA

Figure 7 illustrates the correlation between R_{set} and the voltage level seen at V_{MFIO}.

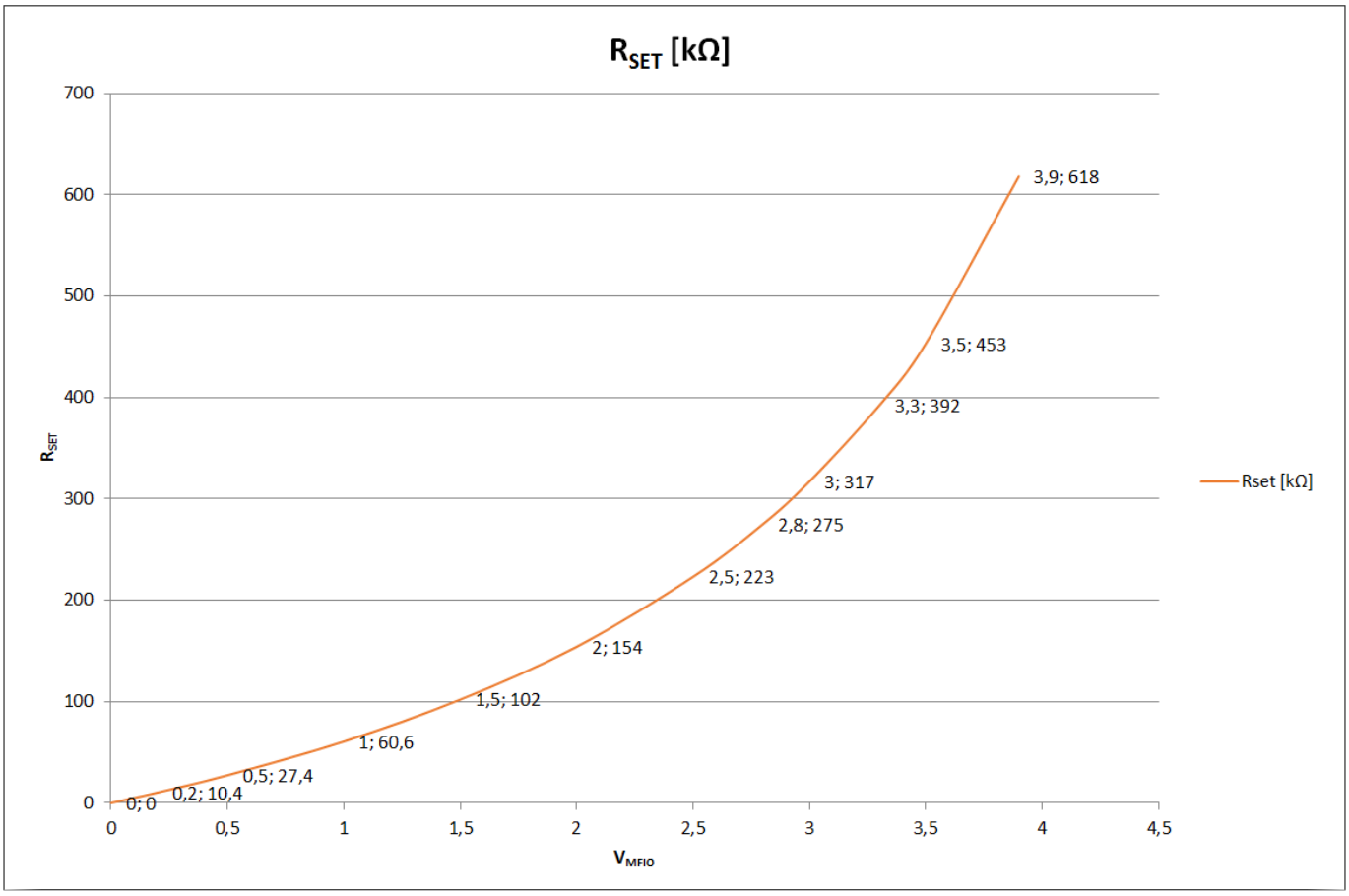


Figure 7 R_{set} versus V_{MFIO}

Note: Figure 7 shows the correlation between R_{set} value and the effective V_{MFIO}. The curve is determined according to the formula in Figure 5 . (R_{set}→ V_{MFIO}→ I_{LED})

2.3 BCR601 supply voltage requirements, LED array voltage limitations

The following section describes steps to determine the maximum LED array voltage of the system; all worst-case operating points of all parameters need to be considered.

BCR601 is designed for LED arrays up to 60 V.

Note: The LED array comprises the combined LED string voltage, the voltage drop over the power transistor and the 400 mV voltage drop via the VSENSE resistor.

The BCR601 IC can be operated between 8 V and 60 V. In the case of an LED array voltage less than 8 V a separate IC supply is required.

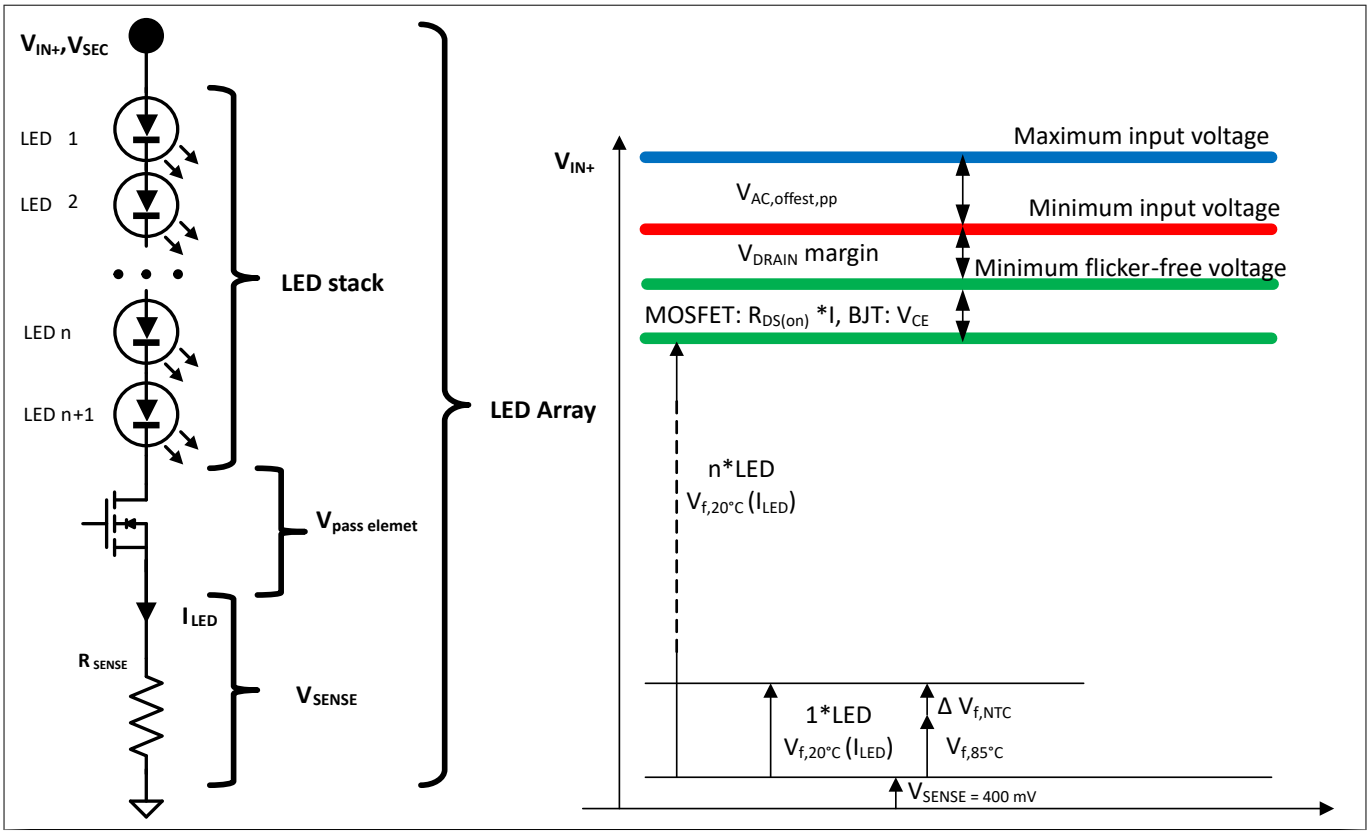


Figure 8 System input voltage components

Figure 8 shows the components contributing to the system input voltage.

LED array maximum voltage calculation

Determination of the maximum secondary-side voltage (V_{SEC}, V_{IN+}) is vital to properly chose and size all external components associated within the LED driver system. Maximum LED array voltage maybe seen under operating or fault conditions.

The Active Headroom Control (AHC) of the feedback loop adjusts the voltage across the LED array due to temperature effects and LED current reduced by dimming. All variables must be considered to determine the highest possible LED array voltage.

Largest voltage of the LED stack under all operating conditions

- Current through the LED string is at 100 percent ($_{ILED}$ = 100 percent)
- LED junction temperature is at its lowest

Pass element voltage requirements

- MOSFET V_{DS} voltage
- BJT V_{CE} voltage

V_{SENSE} resistor voltage drop

- The voltage drop over the V_{SENSE} resistor (100 percent load): $V_{SENSE} = R_{SENSE}*I_{LED}$ = 400 mV

Note: R_{SENSE} is exposed to the power dissipation of $P_{SENSE} = V_{SENSE}*I_{LED}$. The power class of the resistor(s) must be selected accordingly.

LED stack voltage is highest at lowest operating ambient temperature during initial turn-on.

The MOSFET voltage $V_{DS} = R_{DS(on)} * I_{LED}$, at its largest value during full load and maximum operating temperature (or BJT voltage $V_{CE, sat}$) induces an unavoidable power dissipation on the pass element of:

- In case of a MOSFET: $R_{DS(on)} * I_{LED}^2$,
- In case of a BJT: $V_{CE,\,sat} * I_{LED}$.

Maximum V_{SEC} (V_{IN+}) voltage required

- $V_{MAXLED-ARRAY}$ = (LED stack voltage) + (transistor voltage) + (V_{SENSE} voltage)

1. MOSFET

$$V_{\mathrm{IN+,\,LED}}\left(n, I_{\mathrm{LED}}, T, V_{\mathrm{ACoffset,\,pp}}, V_{\mathrm{sense}}\right)$$
$$= n * V_{\mathrm{LED}}\left(I_{\mathrm{LED}}, T\right) + \frac{V_{\mathrm{ACoffset,\,pp}}}{2} + V_{\mathrm{sense}} + R_{\mathrm{DS(on)}}\left(T\right) * I_{\mathrm{LED}}$$
$$= n * V_{\mathrm{LED}}\left(I_{\mathrm{LED}}, T\right) + \frac{V_{\mathrm{ACoffset,\,pp}}}{2} + 400\,\mathrm{mV} + R_{\mathrm{DS(on)}}\left(T\right) * I_{\mathrm{LED}}$$

2. BJT

$$V_{\mathrm{IN+,LED}}\left(n, I_{\mathrm{target}}, T, V_{\mathrm{ACoffset,\,pp}}, V_{\mathrm{sense}}\right)$$
$$= n * V_{\mathrm{LED}}\left(I_{\mathrm{LED}}, T\right) + \frac{V_{\mathrm{ACoffset,\,pp}}}{2} + V_{\mathrm{sense}} + V_{\mathrm{CE}}\left(T\right)$$
$$= n * V_{\mathrm{LED}}\left(I_{\mathrm{LED}}, T\right) + \frac{V_{\mathrm{ACoffset,\,pp}}}{2} + 400\,\mathrm{mV} + V_{\mathrm{CE}}\left(T\right)$$

Equation 2 System input voltage V_{IN+}

2.3.1 BCR601 thermal optimization

This section describes how to optimize power consumption of the BCR601.

The total current consumption consists of IC self-supply consumption plus current for the DRV supply .

The BCR601 has a self-supply current consumption of up to 2.2 mA.

To this current the maximum possible source current at the pin *DRV* of -10 mA must be added. High source currents at pin *DRV* usually occur in case of a BJT used as a pass element at low h_{FE} of the BJT.

In a static operating condition of constant dimming and usage of a MOSFET the *DRV* current component can be neglected.

Calculation of IC power consumption

BCR601 power consumption is: $P_{\mathrm{BCR}} = V_S * I_{\mathrm{BCR,\,total}}$

Power consumption of the BCR601 can be lowered by a reduction of the voltage applied to the *VS* pin. Lowering the voltage at *VS* is achieved by adding a series resistor between the input voltage V_{IN+} and *VS*.

VS series resistor power consumption: $P_{\mathrm{Rpred}} = R_{\mathrm{pred}} * I_{\mathrm{BCR,\,total}}^2$

BCR601 power consumption reduction by adding a resistor is recommended when secondary-side output voltage is large (high voltage LED array). To ensure proper start-up of the IC, the supply voltage of the IC at *VS* must not drop below the minimum operating voltage of 8 V.

To prevent a BCR601 system from failing start attempts, use a smaller or no power reduction resistor.

$$V_{VS} > 8\ V$$

Equation 3 IC supply voltage requirement

$$I_{BCR,\,VS,\,max} = 12.2\ mA$$

Equation 4 Maximum IC current consumption according the datasheet

Protected by the resistor the maximum power consumption of the IC can be reduced to:

$$P_{BCR,\,8\ V,\,wc} = 8\ V * 12.2mA = 97.6\ mW$$

Equation 5 Maximum IC power consumption at V_{VS} = 8 V

To avoid a drop below the minimum IC supply voltage Equation 6 must be fulfilled.

$$R_{pred} < \frac{V_{in+} - 8\ V}{I_{BCR,\,8V,\,wc}} \Leftrightarrow R_{pred} < \frac{V_{in+}}{12.2\ mA} - 656\ \Omega \Leftrightarrow R_{pred} < \frac{V_{in+}}{12.2\ mA} - 656\ \Omega$$

Equation 6 Maximum R_{pred}

2.3.2 BCR601 with opto-coupler feedback design

This section describes BCR601 system design with an opto-coupler for feedback to the primary side.

Opto-couplers are the common means of transferring signals between galvanic isolated areas of the system. Feedback to primary side is controlled via the curent flowing through the diode side of the opto-coupler. At BCR601 this current is controlled via pin *OPTO*. The *OPTO* pin represents the output of the feedback PI controller of the active headroom control. This enables a maximum flexibility for fine tuning covering all possible ranges of current transfer ratios (CTRs) of opto-couplers as well as changes caused by aging.

The power supply of the OPTO path depends on the nature of the power supply of the primary side:

- Opto-Coupler supply voltage ($V_{OPTO,path}$) must be well regulated and if possible $V_{OPTO,path}$ shall be lower than the LED supply voltage V_{SEC}, V_{IN+}. A simple Zener diode and series resistor from output to VOPTO is sufficient to achieve this requirement,
- In case of a primary side providing an auxiliary supply voltage, it is recommended to use a supply voltage in the range of 10 V to 15 V stabilized by a Zener diode.

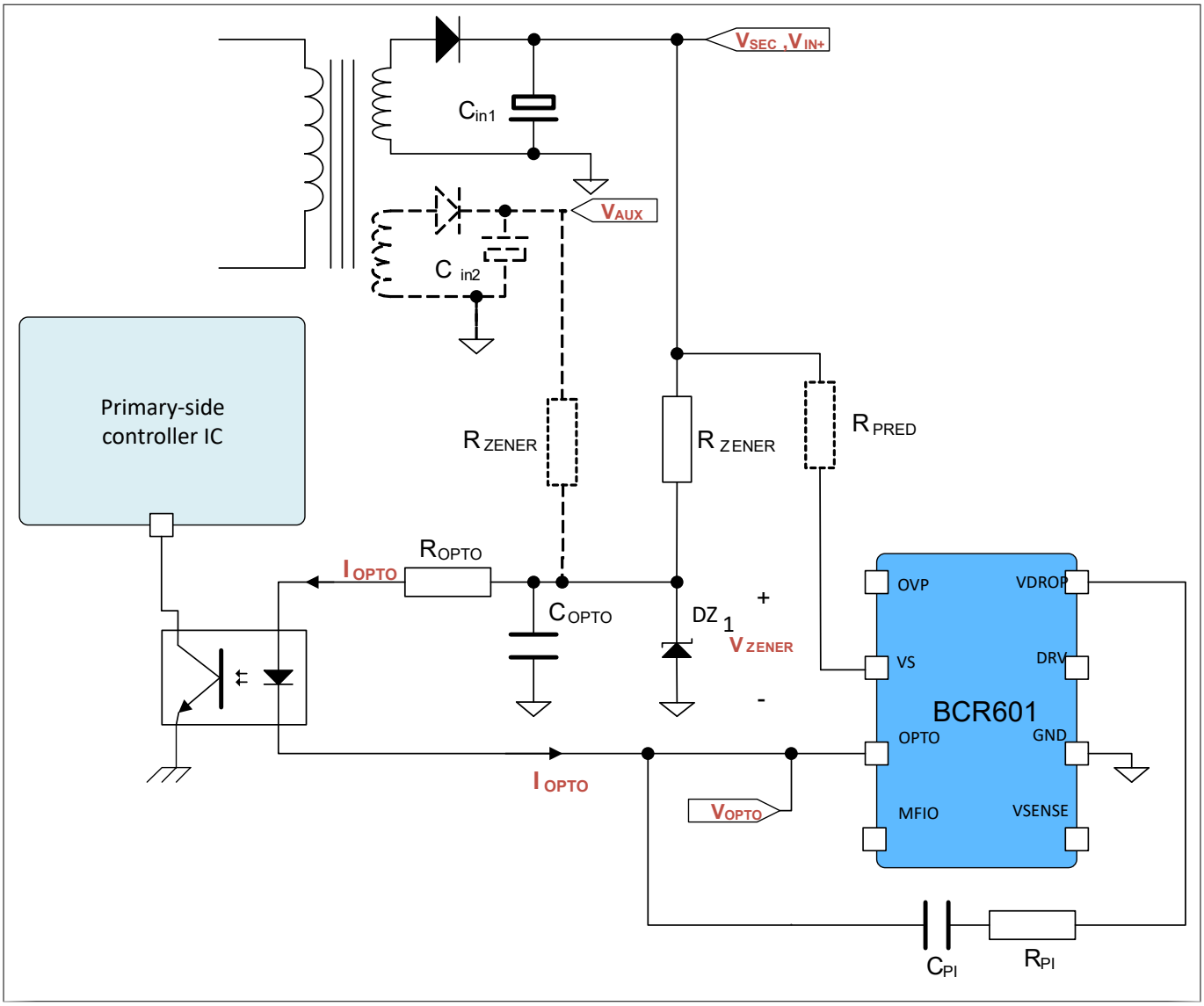


Figure 9 ***OPTO* supply voltage circuit in case of single supply**

2.3.2.1 Opto-coupler design with single voltage output rail on secondary side

This section describes the opto-coupler feedback design guidelines where a single secondary side voltage rail is present.

To achieve a well regulated voltage for the *OPTO* path, a Zener diode is used with a series current limiting resistor.

Zener breakdown voltage is dependent on supply voltage and opto-coupler choice. Zener diode breakdown voltages from 9V to 15V are well suited for typical applications. Ensure supply voltage to the zener diode is sufficiently larger than the breakdown voltage for proper regulation over all operating conditions

A prerequisite for the usage of a breakdown diode is a supply voltage of the LED path higher than the supply voltage of the *OPTO* path.

Requirements for the *OPTO* path are:

The protection resistor R_{Zener} placed between voltage V_{IN+} and the Zener diode must be selected in such a way that:

- A maximum drain current at pin *OPTO* current of 3.6 mA can be achieved,
- The minimum input voltage at the pin *OPTO* is at least 3 V. (The maximum voltage must be below 60 V.)

(For the values please refer to the datasheet.)

The breakdown diode itself must be protected against over current by the resistor R_{Zener}. This resistor must be configured in a way that

- The maximum *OPTO* current is guaranteed,
- Power losses via the breakdown diode are minimized,
- The overall current of the *OPTO* path and the current flowing via the Zener diode causes a power dissipation at this resistor within its power limits. This is especially of importance in case of LED drivers with a varying number of LEDs in the array. The power range of the resistor must take into account the highest input voltage at V_{IN+} caused by the highest supported number of LEDs in the array.

Please refer to Equation 8 for requirements for the breakdown protection resistor and the Zener diode.

$$V_{\text{Zener}} = V_{\text{IN}+} - R_{\text{Zener}} * I_{\text{OPTO}} = V_{\text{OPTO, pin}} + R_{\text{OPTO}} * I_{\text{OPTO}} + V_{F,\text{opto}-\text{coupler}} = R_{\text{OPTO}} * 3.6\ \text{mA} + V_{F,\text{opto}-\text{coupler}} + 3\ V$$

Equation 7 Supply voltage conditions

$$R_{\text{Zener}} < \frac{V_{\text{IN}+} - V_{\text{breakdown, Zener}}}{I_{\text{opto}}}$$

$$R_{\text{Zener}} < \frac{V_{\text{IN}+} - V_{\text{breakdown, Zener}}}{3.6\ \text{mA}}$$

$$P_{\text{Zener}} > I_{\text{opto, max}} * V_{\text{Zener}}$$

$$P_{\text{Zener}} > 3.6\ \text{mA} * V_{\text{Zener}}$$

Equation 8 Requirements for the protection resistor of the breakdown diode

2.3.2.2 Auxiliary supply voltage for the *OPTO* path

This section describes the voltage supply of the opto-coupler feedback where the primary side of the LED driver has an auxiliary output.

An auxiliary supply of the *OPTO* path is the option of choice. Requirements in this case are:

$V_{AUX} << V_{IN+}$

Where

- V_{AUX} is the supply voltage of the *OPTO* path,
- V_{IN+} is the supply voltage of the LED array.

In a PFC/Flyback primary side such as the XDPL8218 an auxiliary supply voltage usually is generated by a second winding on the transformer.

The auxiliary supply may have an AC phase ripple in phase, or with a phase shift compared to the AC input ripple of the primary supply.

Using this option a Zener diode at the entry of the *OPTO* path is not compulsory but may be used for stabilizing the input voltage.

2.3.3 BCR601 operation without opto-coupler

This section describes how the current loop can be configured without using the voltage-feedback loop.

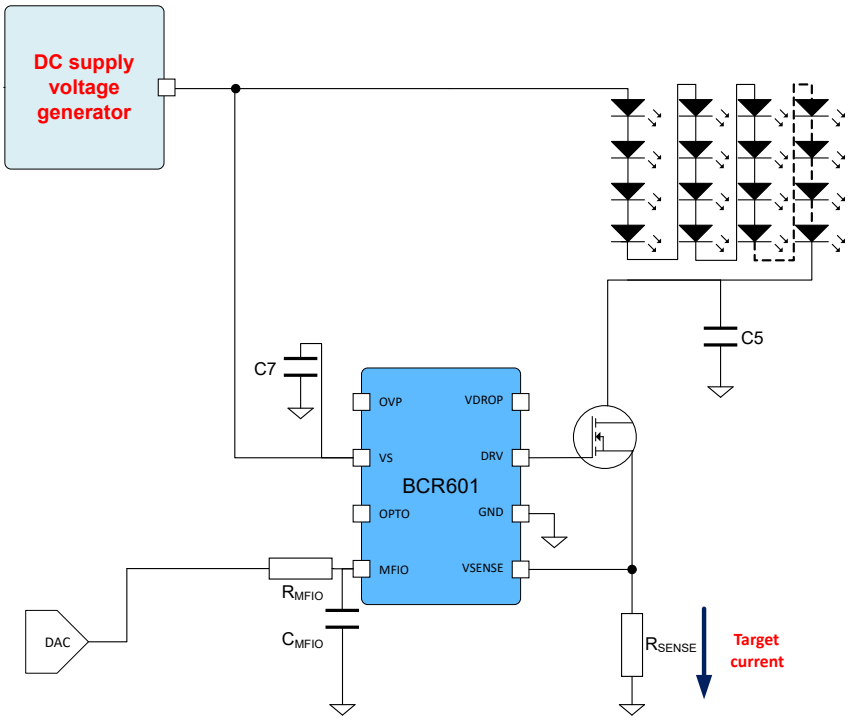
The BCR601 linear regulator can be implemented without the AHC activated. This would be realized if there were no feedback from the BCR601 to the voltage control loop. The LED driver system would be configured

to deliver a regulated voltage on the secondary side that would be set high enough to meet all operating conditions for the LED array.

Design steps for BCR601 operation without opto-coupler:

- Apply DC laboratory voltage to V_{SEC}, V_{IN+},
- Pin *OPTO* and the voltage feedback loop are left open,
- The voltage applied to pin V_{SEC}, V_{IN+} is steadily increased until the target voltage configured via the VSENSE serial resistor is reached,
- Additional voltage headroom is recommended to ensure any AC ripple superimposed on the final configuration does not affect current regulation,
- AC-DC secondary-side voltage set-point is now determined.

Figure 10 Setup for stand-alone configuration of the current loop



Note: Any voltage exceeding the system input voltage increases the power dissipation the pass element is exposed to. This power is transferred into heat in the power transistor. For further information please refer to Thermal limits*.*

Note: Stand-alone current configuration can also be used as acceptance test to check the correct behavior of the dimming mechanism. For further information about dimming please refer to BCR601 dimming

2.4 Control loop configurations

This section describes the configuration of the voltage and the current control loop.

BCR601 contains two control loops.

- The current control loop,
  - Regulates current through the LED array,
- The voltage control loop,
  - Adjusts V_{SEC} (V_{IN+}) voltage to the minimum headroom across the LED array to achieve highest efficiency.

Both control loops can be configured independently; however interactions between the two feedback loops occur, and need to be considered.

The type of power transistor used as the pass element influences the feedback loop in terms of transfer function, gain and frequency responses. This needs to be considered in the configuration values of the feedback loop parameters and causes differences from the theoretical to real values.

This gives a hierarchy of configurations.

1. Configuration of the current control loop,
2. Configuration of the voltage control with respect to stable operation over the whole *MFIO* dimming range,
3. Optimization of the opto-coupler feedback signal (path to pin *OPTO*),
4. Transistor input voltage optimization,
5. Power loss optimization with respect to the voltage drop over the pass element.

Secondary-side voltage optimization (AHC) has two effects on system performance:

- Power loss within the pass element (power transistor),
- System start-up time.

Table 2 lists the effects a change of key components of the control loop has.

Table 2 Change effect matrix

Component	Description	Effect	Notes
C_{PI}	Voltage feedback Capacitor	Increase value will increase loop response	As feedback loop response is increased or decreased, start-up time will be inversely affected
R_{PI}	Voltage feedback Resistor	Decrease value will increase loop response	As feedback loop response is increased or decreased, start-up time will be inversely affected
R_{DROP}	Voltage headroom adjustment resistor	Increase value will increase loop response	Increasing resistor RDROP will increase headroom voltage and add power loss to pass element
R_{OPTO}	Adjust current magnitude thru opto-coupler	Adjust opto-coupler CTR response	Adjust value to ensure proper regulation over operating conditions

2.4.1 Feedback voltage loop design considerations

This section describes how to achieve and stable low-loss configuration of the feedback voltage regulator and the BCR601 parts of the voltage control loop.

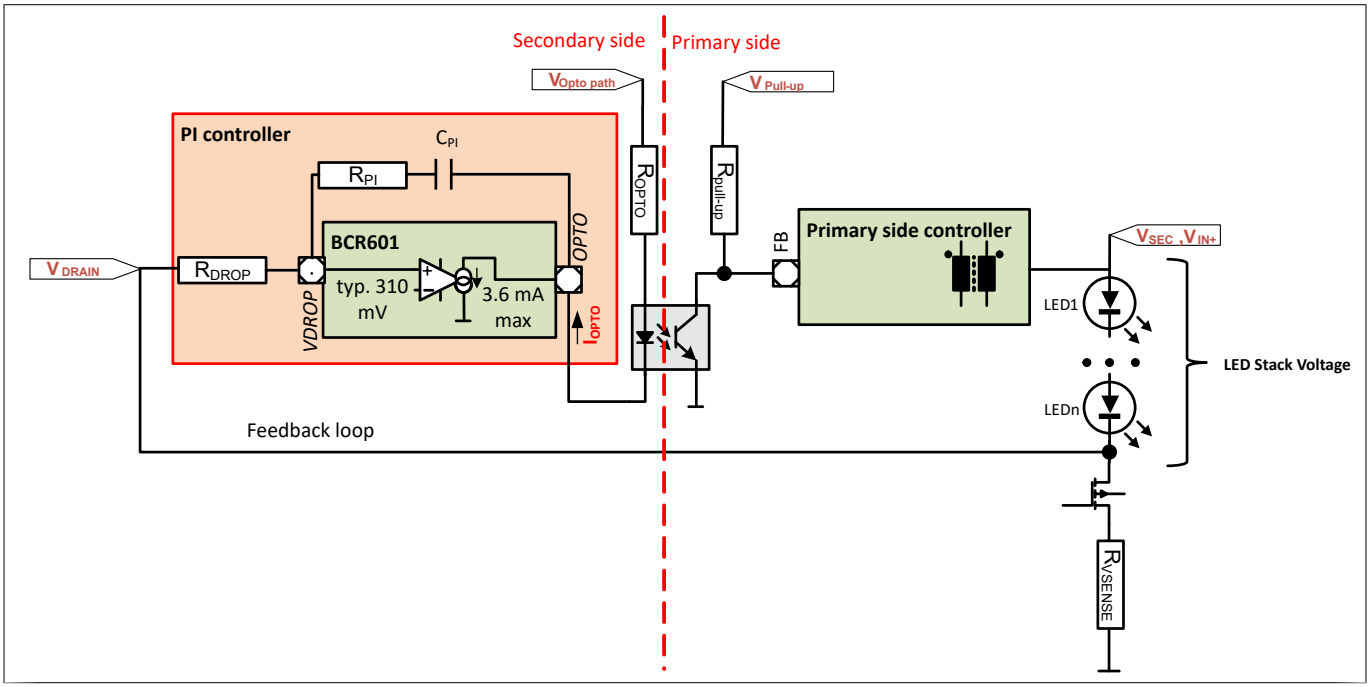


Figure 11 Plant of the feedback voltage loop

Configuration of the voltage control loop comprises setting of the parameter of the PI controller as well as optimizing the power loss over the transistor.

2.4.1.1 Transfer function and Bode

This section gives a comprehensive overview of the voltage feedback loop regulation plant.

The values of the following three external components are calculated to configure the IC's voltage and feedback loops for stable operation::

- C_{PI},
- R_{PI},
- R_{OPTO}.

Please refer to Figure 2.

(1)

$$\frac{I_{OPTO}}{V_{DRAIN}}(s) = \frac{sC_{PI}R_{PI} + 1}{sC_{PI}R_{DROP}R_{OPTO} + 1/g_m}$$

(2)

$$\frac{V_{FB}}{V_{DRAIN}}(s) = -\frac{R_{pull-up}R_{PI}}{R_{DROP}R_{OPTO}}\beta\frac{sC_{PI}R_{PI} + 1}{sC_{PI}R_{PI}}$$

1. Transfer function of BCR601,
2. Compensator transfer function, BCR601 plus a pull-up feedback on primary side.

Equation 9 Transfer functions of the voltage loop PI regulator

Where g_m is the gain of the voltage control path. Equation (2) assumes a system with a primary side with a feedback voltage as input of the control to the PWM signal. This feedback voltage is pulled up by the primary-side resistor R_{FB}. At no opto current the feedback voltage reaches its maximum voltage.

Regarding R_{DROP} this parameter is also the main parameter for the configuration of the voltage drop and hence the power loss over the transistor. (See Unstable current regulation due to insufficient voltage headroom).

Components of the reference design

For the components in Table 3 refer to References .

Table 3 Components for the voltage loop gain

Parameter in transfer function	Component in BCR601 demonstrator schematic	Purpose
I_{OPTO}	OPTO, PCI-1	Output of the BCR601 voltage feedback controller, steering control to be transferred to the primary side usually via an opto-coupler
V_{DRAIN}	LED-, X23	Drain voltage, also defines the power load on the transistor
R_{OPTO}	R15, R20	Resistor configuring BCR601 current loop gain and bandwidth
C_{PI}	C2	Capacitor configuring BCR601 current loop gain and bandwidth
R_{PI}	R8	Main element of configuration of the PI controller
g_m		Gain (transconductance) of BCR601 voltage control path
R_{DROP}	R6	Resistor for configuration of the voltage level of V_{DRAIN} (MOSFET), $V_{collector}$ (BJT) to ground

2.4.1.2 Compensator Bode plot dependency on components

This section describes the effect of parameter changes on gain and phase.

Configuration parameters of the feedback voltage loop in the BCR601 system are:

- C_{PI},
- R_{PI},
- R_{OPTO}

Note: R_{DROP} also influences gain and phase of the control loop. Because this parameter is used to minimize the power dissipation over transistor, it is not considered as a free parameter for the voltage loop.

Figure 12 shows the dependency of the phase on modifications of C_{PI} and R_{PI} based on equation (1) of Equation 9. Figure 13 shows the dependency of the gain on modifications of C_{PI} and R_{PI} based on equation (2) of Equation 9. In all cases the parameter of choice is increased by 67 percent.

The base parameters are:

- C_{PI} = 120 nF,
- R_{PI} = 8.2 kΩ,

- R_{OPTO} = 16 kΩ,
- R_{DROP} = 426 kΩ.

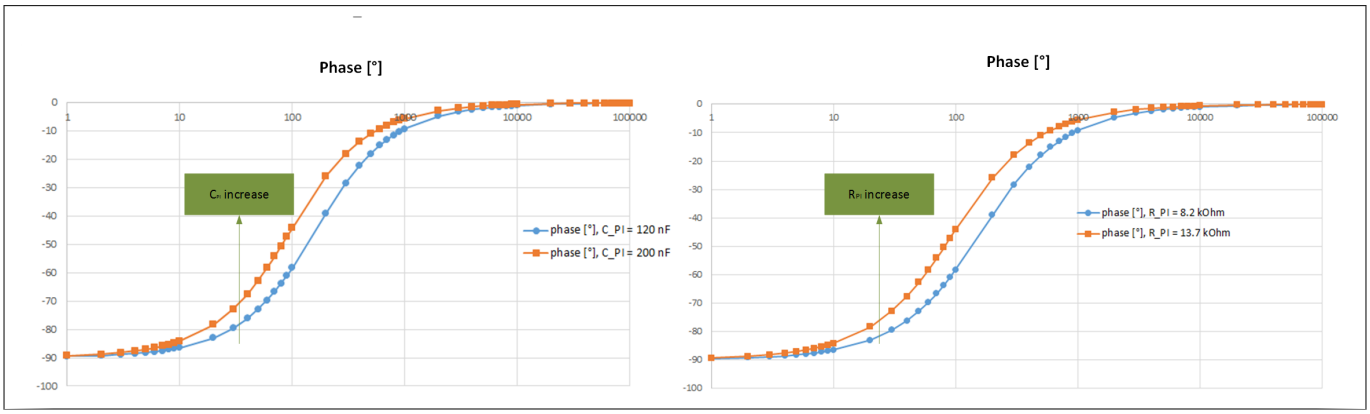


Figure 12 Dependency of phase on R_{PI}, C_{PI}

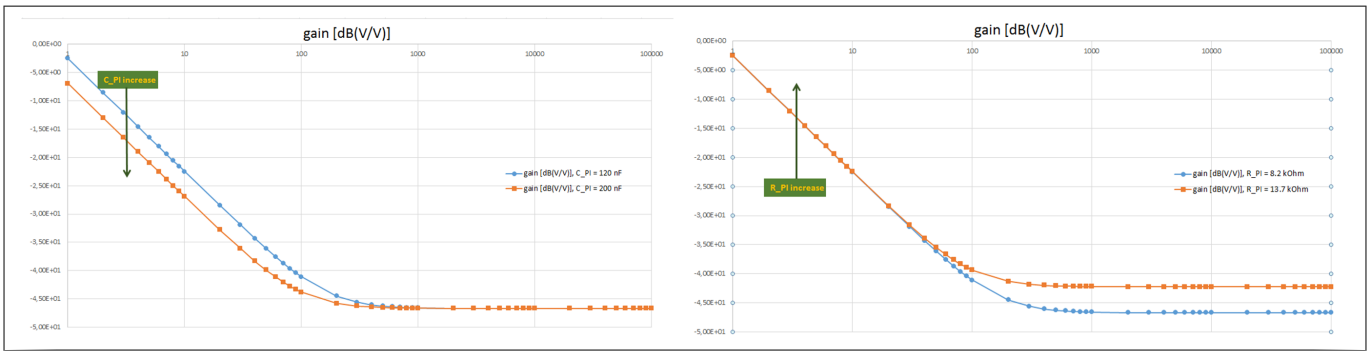


Figure 13 Dependency of gain on R_{PI}, C_{PI}

R_{OPTO}

Regarding R_{OPTO} of paramount importance is the fulfilling of the equations for the current transfer ratio, see Equation 10. When fulfilled stability can be increased by increasing the value of R_{OTPO}. This causes a decrease in gain and of the crossover frequency.

2.4.1.3 I_{OPTO} configuration

This section describes requirements and configurations for the OPTO current.

Output voltage (V_{SEC}, V_{IN+}) regulation is achieved with feedback from the secondary side to the primary PWM controller via the current flowing through the diode side of the opto-coupler.

The BCR601 internal feedback controller is designed to allow use of a wide range of opto-couplers covering all possible ranges of current transfer ratios (CTRs) as well as changes of the CTRs due to aging.

The opto current is generated by the pin *OPTO* as a current sink.

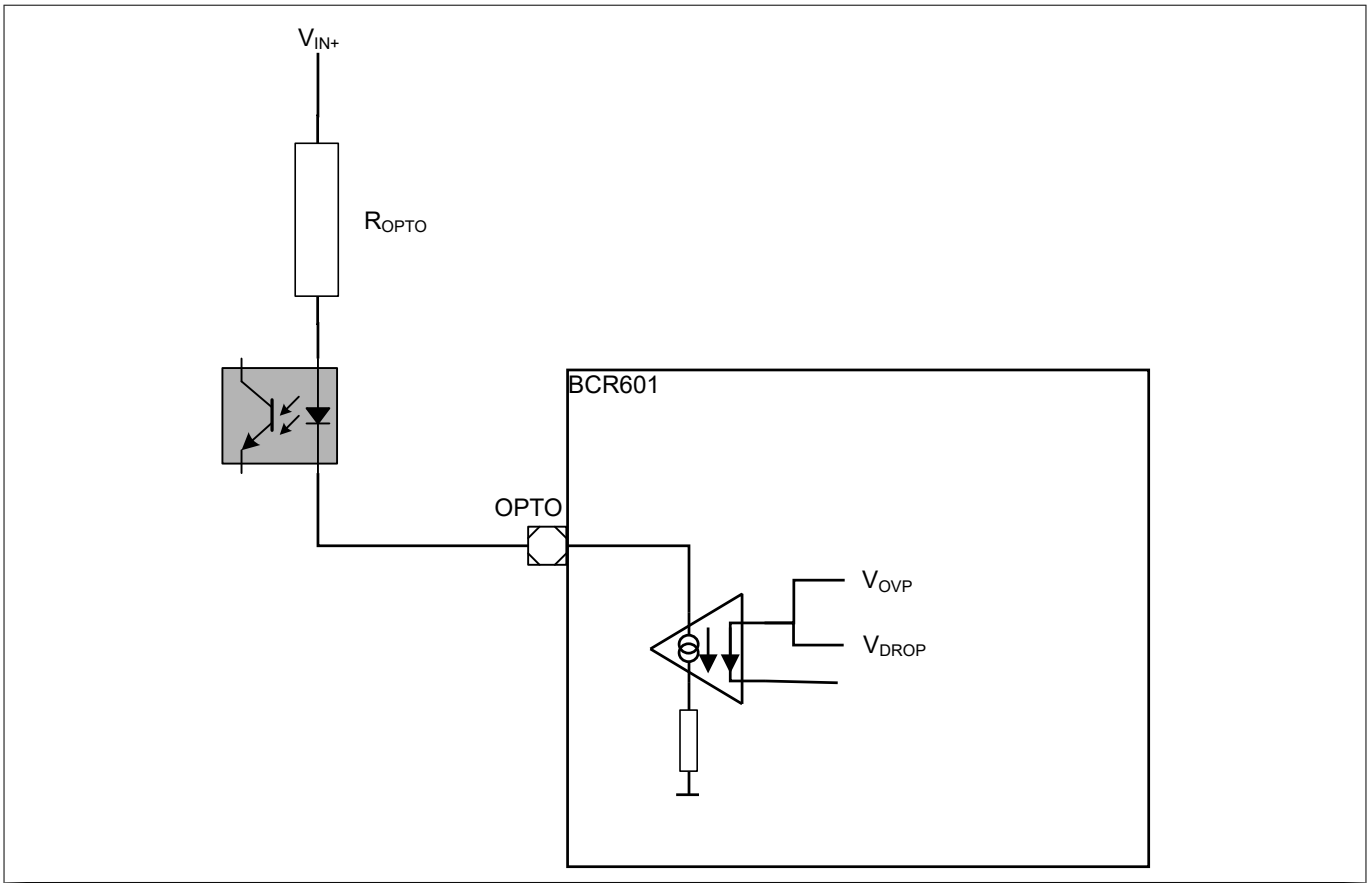


Figure 14 Circuit of the opto current

The current source inside the BCR601 attached to the OPTO pin has two components:

1. Current generated by the input signal at pin *VDROP*,
2. Current generated by the overvoltage protection (*OVP*).

It is a combination of the control output of the PI controller of the voltage feedback loop and the overvoltage protection.

For the PI controller, please refer to Transfer function and Bode.

For the overvoltage protection, please refer to Over-voltage protection (OVP).

Depending on V_{OVP} and V_{DROP} the range of I_{OPTO} is between 0 mA and 2 mA (typical). The voltage input at pin *VDROP* is compared to the internal reference voltage, with a typical value of 310 mV. The voltage of pin OVP is compared to another internal reference voltage of 1.2 V. (For maximum, minimum values and range please refer to the datasheet.) To achieve the full range the voltage offset at pin *OPTO* externally applied must be at least 3 V.

$$R_{OPTO} < \frac{V_{OPTO.supply} - V_{F,\,opto-coupler} - 3V}{I_{FB,\,max}} * CTR_{OPTO,\,min}\left(I_{CFB,\,sys,\,max}\right) \Leftrightarrow R_{OPTO} < \frac{V_{OPTO,\,supply} - V_{F,\,opto-coupler} - 3V}{2\,mA}$$

- $I_{CFB,sys,max}$: Maximum system-dependent control current required on primary side,
- $I_{FB,max}$: Maximum current through opto-coupler on primary side depending on the controller used.

Equation 10 Formula for R_{OPTO}

2.4.2 LED current regulation

This section describes the configuration and optimization of the current feedback loop.

Current regulation considerations:

- Removal of AC ripples in the V_{IN+} input signal; usual AC ripples are non-ideal DC signals with an AC offset at double line frequency,
- Protection of the LEDs from:
  - Thermal overstress, thus improving LED lifetime significantly
  - Over-voltage applied to the LED array
  - Short-cut protection of the LED array

2.4.2.1 BCR601 and Darlington BJTs

This section describes aspects to be considered when using a Darlington BJT.

Darlington transistors and BJTs with high current amplification (h_{FE}) can be used, but the current regulation feedback loop may need to be slowed down to compensate for their increased amplification.

Note: All contents of this section also applies to high h_{FE} standard BJTs.

Current feedback stability can be regained by reducing current feedback response, this is achieved by placing an additional capacitor into the loop that is connected between the base, the DRV pin of the BCR601 and the collector of the transistor.

Remedy

Table 4 lists some high current amplification BJTs and the minimum capacitor size to remove oscillations caused by the high gain.

Figure 15 shows how to place the Miller cap.

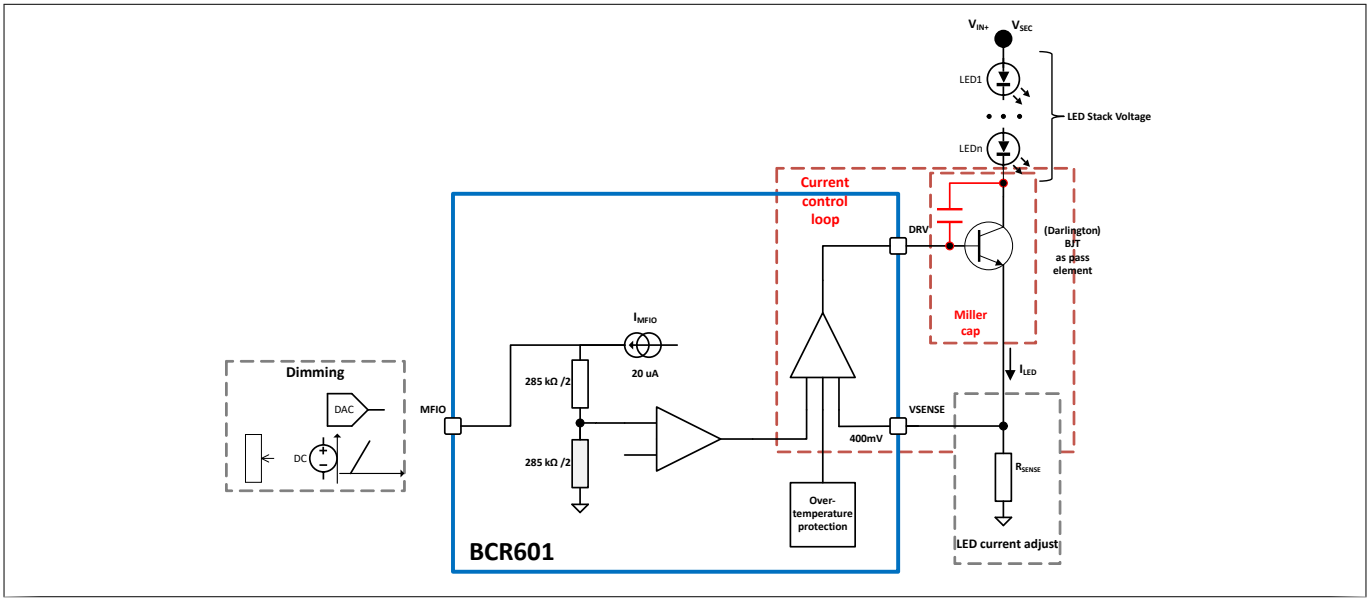


Figure 15 Miller cap to stabilize the current control loop

Table 4 Minimum Miller capacitors at different DC current gains in a 200 mA system

BJT	Type	h_{FE}	C [nF]
TIP-122	Darlington	1000	68
NZT7053	Darlington	1000	56

(table continues...)

Table 4 (continued) Minimum Miller capacitors at different DC current gains in a 200 mA system

BJT	Type	h_{FE}	C [nF]
MJF6039	Darlington	2500	100
NZT602	Standard	5000	100

Note: DC current gains h_{FE} according to the datasheets of the devices.

2.5 BCR601 pass element selection

This section describes requirements of Power MOSFETs and BJTs.

Note: This is a selection guide. It outlines necessary component parameters from the perspective of the BCR601.

Within a linear regulated system, transistor power loss (P_{loss}) is dominated by conduction losses:

- V_{DS}*I_{DS} in case of MOSFET
- V_{CE}*I_C in case of BJT

MOSFETs should be selected with this in mind, low $R_{DS(on)}$ being a critical specification.

BJTs are only recommended for use in low power, low LED current (< 200 mA) application where cost is critical.

2.5.1 MOSFET

This section describes the requirements in case of MOSFET usage.

Major MOSFET parameters to be considered for selection are (ordered according to degree of importance)

- Safe operating area (SOA)
- Threshold voltage ($V_{GS(th)}$)
- Maximum power dissipation (P_D)
- $R_{DS(on)}$,
- Continuous drain current (I_D)
- Operating junction temperature (T_J)
- Signal response characteristics
- Drain-to-source breakdown voltage ($V_{(BR)DSS}$)
- Total gate charge Q_g
- Logic level

Note: In Table 5 the typical values refer to the reference design. The reference design is equipped with an Infineon OptiMOS™ BSP716N.

Table 5 MOSFET selection parameters

Parameter	Selection criteria	Range	BCR601 demonstrator notes
SOA	The relation between V_{DS} and I_D must comply with the DC curve	See description below this table	2.8 V (at 500 mA), please refer to Figure 17
$V_{GS(th)}$	MOSFETs are usable with threshold voltages up to 4 V	See description below this table	2 V
P_D	The maximum value of this voltage together with the target current sets the required power dissipation of the MOSFET.	> V_{DRAIN}* I_{LED}	1.8 W

(table continues...)

Table 5 (continued) MOSFET selection parameters

Parameter	Selection criteria	Range	BCR601 demonstrator notes
$R_{DS(on)}$	A higher $R_{DS(on)}$ increases the MOSFET power dissipation. Usually the power dissipation caused by $R_{DS(on)}$ can be neglected compared to the power dissipation caused by the AC ripple on the input signal.	< 0.3 Ω	0.18 Ω
I_D	Set by the target current of the application plus margin	> I_{LED}+ 10 percent	2.3 A
T_J	Application system conditions plus margin. For optimal usage of the over-temperature protection (OTP) feature it shall be higher than $T_{OTP,on}$	> 140 °C	150 °C
Signal response characteristics, C_{iss}	Set by $\tau = R_{Gate} * C_{iss}$. The input capacitance acts as integration element in the current control loop	< 3000 pF	237 pF
$V_{(BR)DSS}$	The breakdown voltage is limited by the input voltage	> V_{IN+}+10 percent	75 V
Q_g	Gate charge is of importance in case of fast transitions of the current in the dimming case	< 60 nC	8.7 nC

$V_{GS(th)}$ selection

For safe selection of a MOSFET with an appropriate threshold value:

- $V_{GS(th),max}$ < 4.5 V,
- The margin between maximum and typical values of $V_{GS(th)}$ must be evaluted, e.g. with $V_{GS(th),max}$ = 1.8 V and a $V_{GS(th),typical}$ this yields a factor of $\gamma = \frac{V_{GS(th),\,max}}{V_{GS(th),\,typical}}$
- In the datasheet of the MOSFET check the typical transfer characteristics curve to evaluate the voltage V_{GS} for your target current $V_{GS,target,evaluated}$; see Figure 16, note that this diagram shows typical values,
- Multiply the determined voltage $V_{GS,I\text{-}target}$ with the factor y,
- The resulting voltage must fulfill the formula $V_{GS,\,target,\,max} = \gamma * V_{GS,\,target,\,evaluated} < 4.5\,V$.

Note: Generally the variance of $V_{GS(th)}$ between minimum and maximum value in the datasheets of used MOSFETs is very high. Also it is measured at very low drain current, at values of e.g. 100 µA or 250 µA.

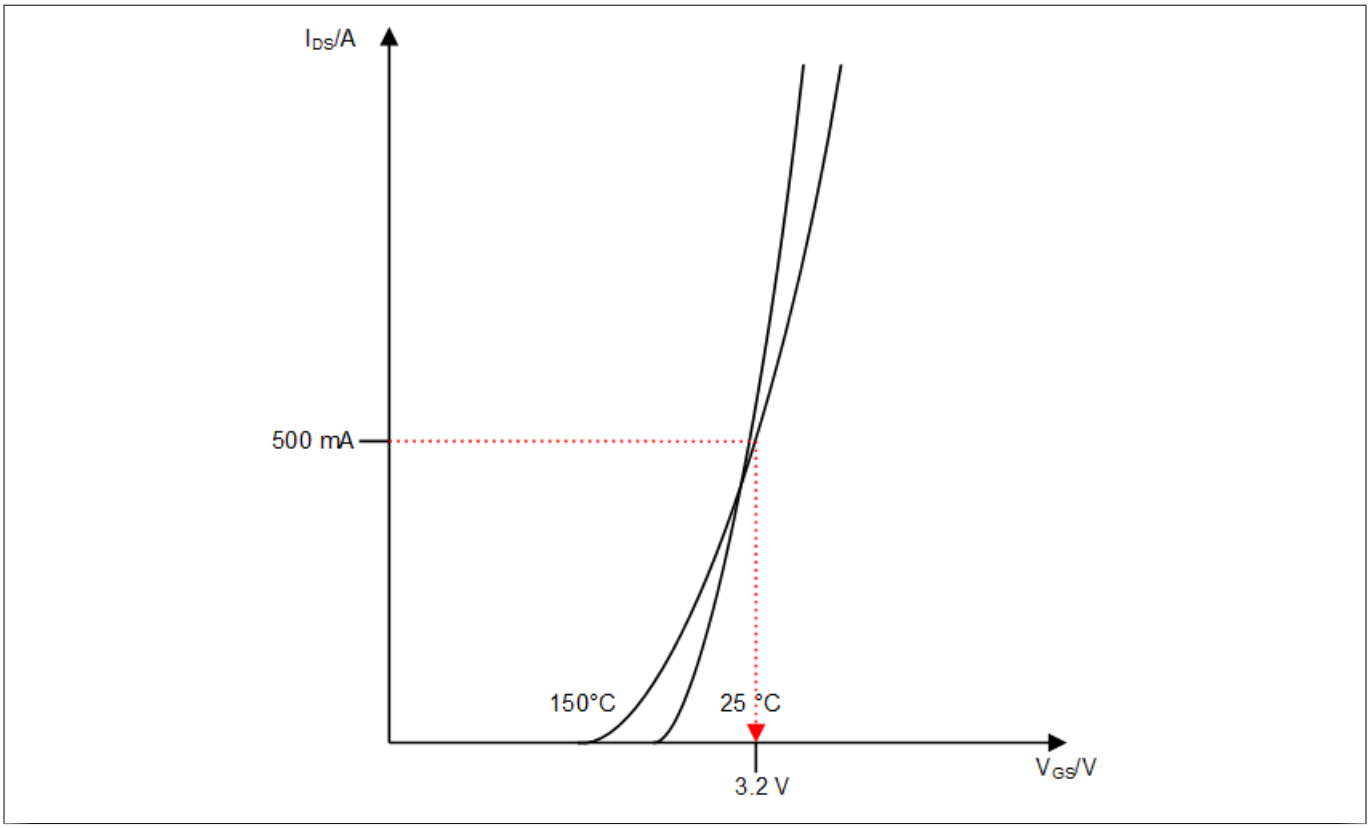


Figure 16 Example of a typical transfer characteristics curve

Safe operating area (SOA)

SOA curves for MOSFETs that are used in linear regulator systems are important diagrams to ensure the MOSFET meets system design requirements. When choosing operating conditions of the MOSFET in the system use worst case voltage (V_{DS}) and current (I_{LED}, I_{DS}) operating points. These are found on the DC graphs. For optimization please refer to LED current regulation and Power loss optimization.

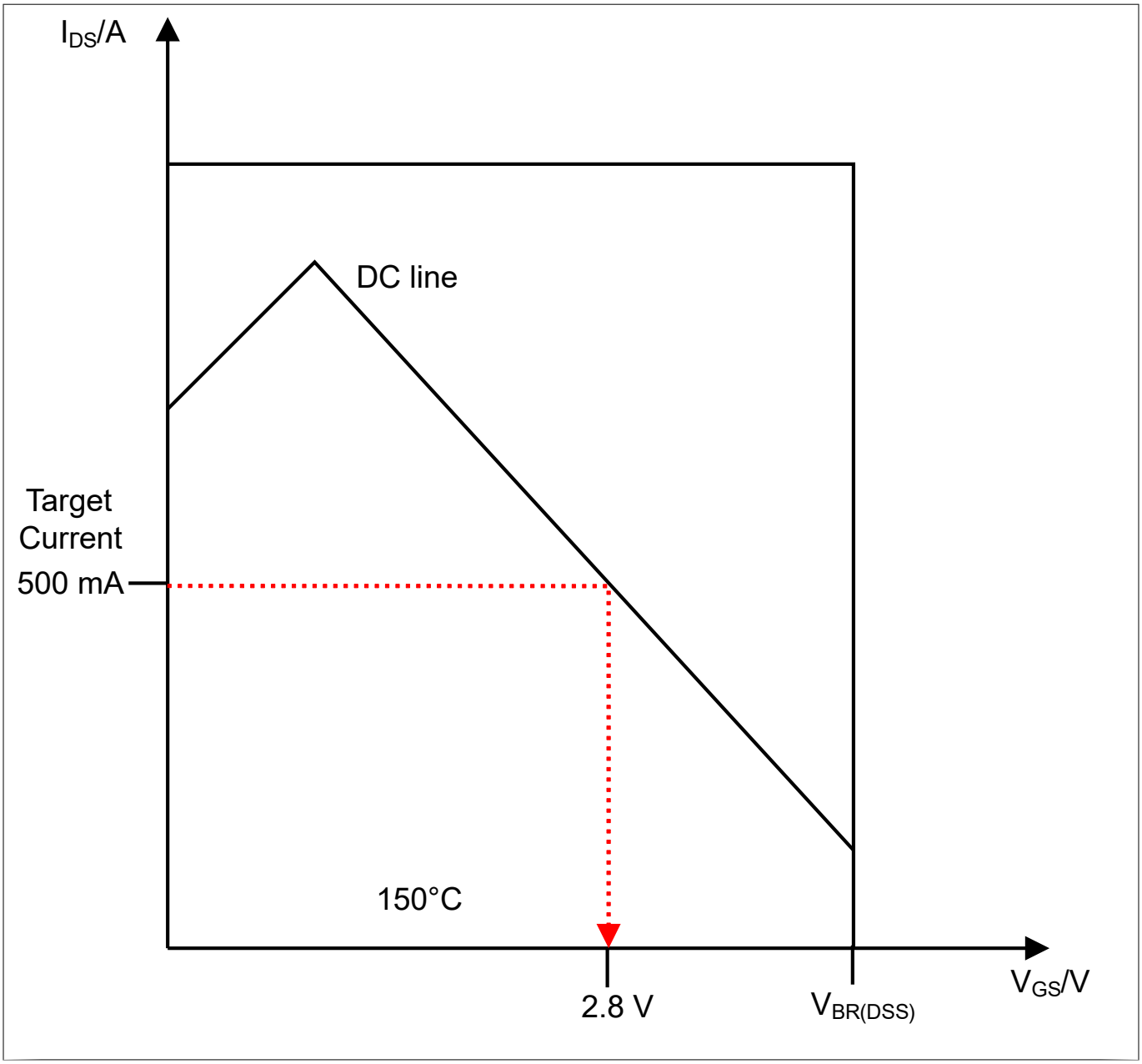


Figure 17 Example of a MOSFET SOA

Logic level

MOSFETs used shall be of type "logic level". Non-logic level MOSFETs require higher levels of V_{GS}. Using “logic level“ MOSFETs the current control is more robust because of a larger control range usable by the controller output.

Recommended MOSFETs

This list gives a selection of recommended MOSFETs.

Table 6 Recommended MOSFETs

Type	Package	$V_{gs,\ typ}$	$V_{gs,\ max}$	V_{gs} at specified $R_{DS(on),max}$	SOA maximum current at V_{DRAIN} = 2 V DC	SOA maximum current at V_{DRAIN}= 5 V DC
BSP761N	SOT-223	1.4 V	1.8 V	180mV at 4.5V	0.9 A	0.2 A
BSP372N	SOT-223	1.4 V	1.8 V	270 mV at 4.5V	0.9 A	0.1 A

2.5.2 BJT

This section describes requirements for the BJTs used.

The main BJT parameters to be considered for selection are (ordered according to degree of importance):

- DC current gain
- Collector-emitter breakdown voltage at $I_B = 0$ ($V_{(BR)CEO}$)
- Collector-base breakdown voltage ($V_{(BR)CBO}$)
- Continuous collector current (I_C)
- Total power dissipation (P_D)
- Operating junction temperature (T_J)

Table 7 BJT selection parameter

Parameter	Selection criteria	Range
DC current gain	Necessary to achieve target current of the system	$h_{FE} > \frac{I_{target}}{I_{DRV,\ source}}$
$V_{(BR)CEO}$	Set by the system configuration, more than the input voltage of the BCR601 system	> V_{IN+}+10 percent
$V_{(BR)CBO}$	Set by the system configuration, more than the input voltage of the BCR601 system	> V_{IN+}+10 percent
I_C	Set by the target current of the application plus margin	> I_{target}+ 10 percent
P_D	Proper current regulation requires a remaining $V_{Collector}$ offset voltage. The maximum value of this voltage together with the target current sets the required power dissipation of the BJT	> $V_{collector}$ * I_{LED}
T_J	Application system conditions plus margin. For optimal usage of the OVP protection feature it shall be higher than $T_{OTP,on}$	140°C

2.6 BCR601 protection overview and description

2.6.1 Over-voltage protection (OVP)

This section describes how to configure the over-voltage protection.

Over voltage protection secures the system, especially the BCR601 IC, the LEDs and the transistor, from damages caused by an overshooting input voltage.

Reaction time of the overvoltage protection depends on time constants existing in the voltage regulation plant.

Every overshoot of the input voltage leads to a temporary increase of the LED current. Due to the low time constants and fast reaction of the current control, usually voltage spikes are absorbed by the transistor. This protects the LEDs from an overshoot over the surge current. So for the system design safe operating areas (SOAs) of the system have to be considered, too.

Reaction time of the current control loop depends on the capacities of transistors used plus optionally used capacities in the loop.

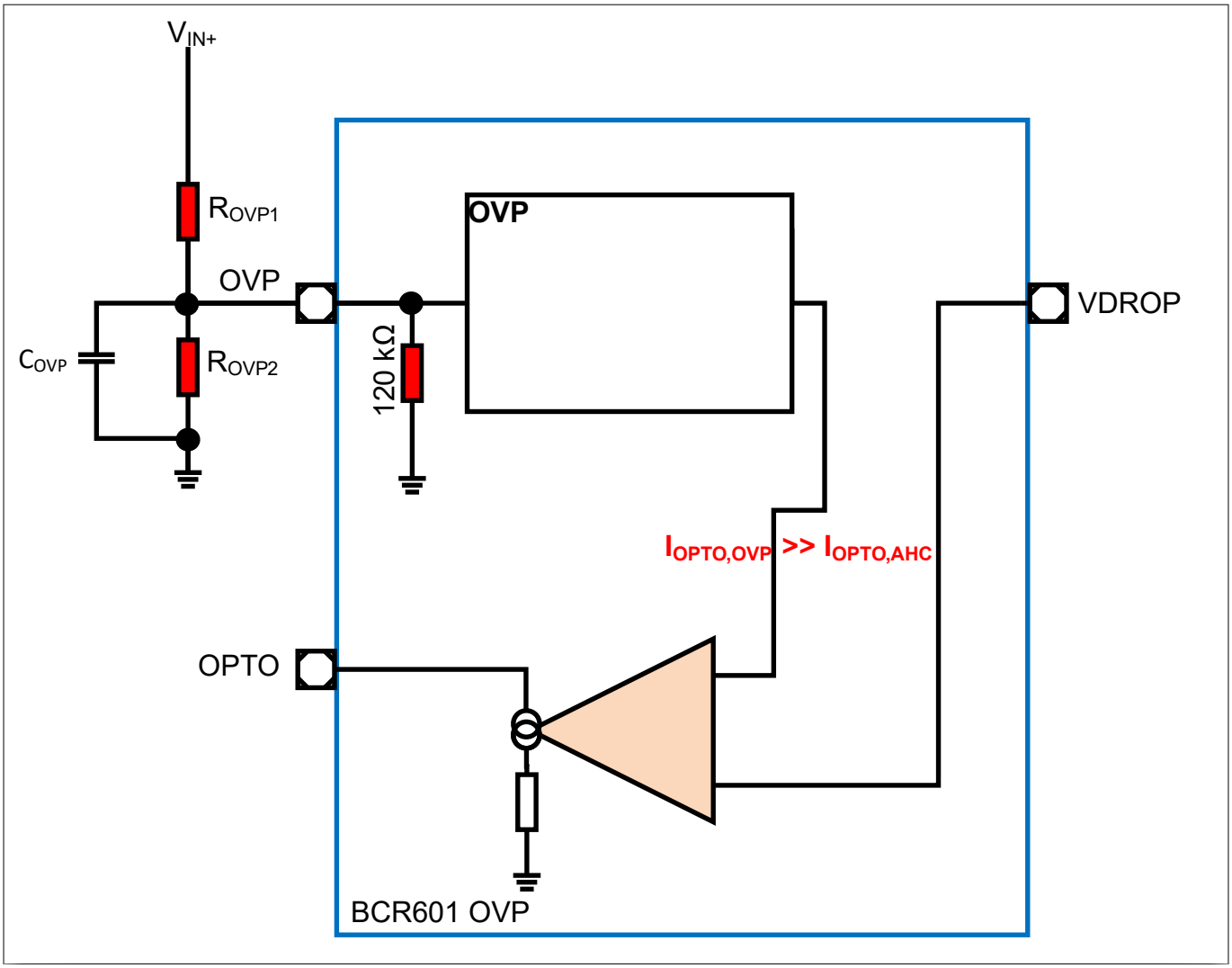


Figure 18 OVP effect on I_{OPTO} and configuration elements

2.6.1.1 OVP activation

This section describes the internal functionality of OVP.

In case of an overvoltage the standard regulation of the voltage feedback loop determined by the input at the pin *VDROP* is dramatically overruled by the over-voltage protection. The opto current sunk in the *OPTO* pin is sharply increased, leading to a fast slowdown of the primary side.

However over-voltage protection is not determined by a discrete threshold but an activation over a voltage range at the pin *OVP*.

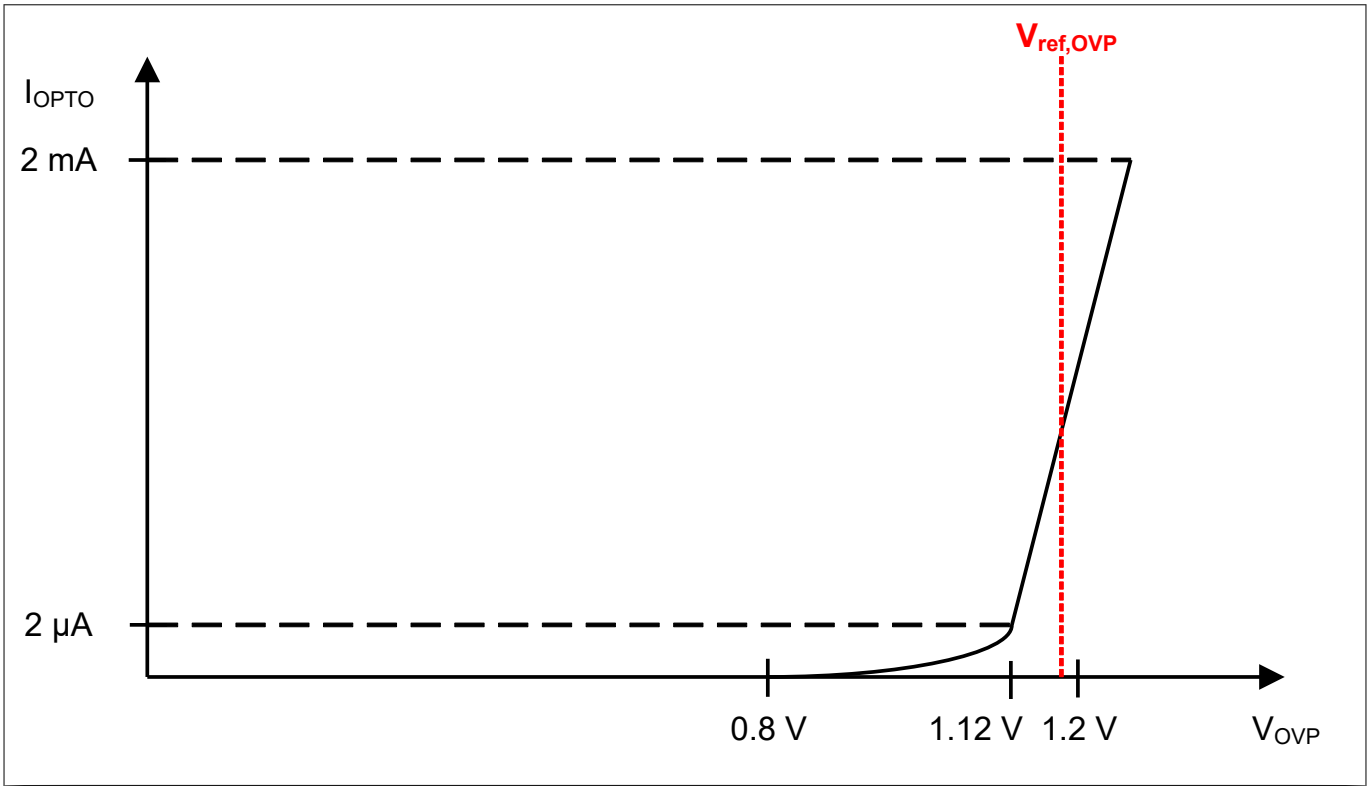


Figure 19 Activation range of the overvoltage protection

In case the voltage V_{OVP} of the pin *OVP* is

- Equal to $V_{ref,OVP}$: I_{OPTO} is 1 mA,
- Greater than $V_{ref,OVP}$: 2 mA > I_{OPTO} > 1 mA,
- Less than $V_{ref,OVP}$: 1 mA > I_{OPTO} > 0 mA.

Configuration is done with respect to the input voltage at the pin *OVP* by a voltage divider. The BCR601 has an internal resistor at pin *OVP*, hence the voltage divider can be setup by either one or two external resistors. In case of two external resistors the effective resistor consisting of the internal and the external resistor connected to ground has to be calculated.

Note: The typical value of the internal resistor connected to ground is determined to be 120 kΩ. For the exact value, please refer to the BCR601 datasheet.

2.6.1.2 OVP configuration

The BCR601 contains an internal base resistor of 120 kΩ. The voltage divider can be set up solely using this resistor. However for fine-tuning an external base resistor may be used additionally. In this case the effective base resistor has to be taken into account.

$$R_{\mathrm{OVP2,\,eff}} = \frac{120\,\mathrm{k\Omega} * R_{\mathrm{OVP2}}}{120\,\mathrm{k\Omega} + R_{\mathrm{OVP2}}}$$

Equation 11 Effective resistance OVP2

The voltage divider must be configured in a way that its threshold voltage is above the system input voltage. Usually a headroom between 5 percent and 10 percent above the maximum voltage is chosen. The maximum voltage is the maximum DC voltage plus the AC-line ripple peak-to-peak.

- $V_{IN,DC,max}$ is the maximum input voltage required to operate the system at the target current. The voltage is determined by the forward voltage of the LEDs which is usually highest at start-up. So the forward voltage at start-up ambient temperature has to be taken into account,
- $\Delta_{headroom}$ is the factor of overpower that is defined as acceptable before OVP triggers,
- $V_{IN,max}$ is the maximum DC voltage to operate the LEDs plus the maximum of the AC ripple in the system.

Note: AC ripple can be reduced by a larger input capacitor.

$$V_{\mathrm{IN,\,OVP}} = \left(V_{\mathrm{IN,\,DC,\,max}} + V_{\mathrm{AC,\,pp}}\right) * \Delta_{\mathrm{headroom}} = V_{\mathrm{IN,\,max}} * \Delta_{\mathrm{headroom}}$$
$$V_{\mathrm{IN,\,max}} = \left(\mathrm{max.nr.LEDs}\right) * V_{f,\,\mathrm{LED,\,max}} + V_{\mathrm{SENSE}} + V_{\mathrm{transistor,\ DS|\ collector\ emmitter}} + V_{\mathrm{AC,\,pp}}$$

Equation 12 Input voltage for over voltage trigger threshold

$$R_{\mathrm{OVP1}} = \frac{V_{\mathrm{IN,\,OVP}} - V_{\mathrm{OVP,\,IC}}}{V_{\mathrm{OVP,\,IC}}} R_{\mathrm{OVP2,\,eff}}$$
$$V_{\mathrm{IN,\,OVP}} = \left(V_{\mathrm{IN,\,DC,\,max}} + V_{\mathrm{AC,\,pp}}\right) * \Delta_{\mathrm{headroom}} = V_{\mathrm{IN,\,max}} * \Delta_{\mathrm{headroom}}$$
$$R_{\mathrm{OVP1}} = \frac{V_{\mathrm{IN,\,max}} * \Delta_{\mathrm{headroom}} - 1.12V}{1.12V} * V_{\mathrm{OVP2,\,eff}}$$
$$= \frac{\left(\left(\mathrm{max.nr.LEDs}\right) * V_{f,\,\mathrm{LED,\,max}} + V_{\mathrm{SENSE}} + V_{\mathrm{transistor,\ DS|\ collector\ emmitter}} + V_{\mathrm{AC,\,pp}}\right) * \Delta_{\mathrm{headroom}} - 1.12V}{1.12V}$$
$$* \frac{120\,\mathrm{k\Omega} * R_{\mathrm{OVP2}}}{120\,\mathrm{k\Omega} + R_{\mathrm{OVP2}}}$$

Equation 13 Requirement for OVP configuration resistors

To avoid unwanted triggering of OVP caused by voltage spikes, it is recommended to add a low-pass capacitance C_{OVP} to ground, and as physically close to the IC as possible.

2.6.2 Over-temperature, hot-plug and shortcut protection

Besides the OVP protection BCR601 provides over-temperature and hot-plug protection, plus the protection of a short of LEDs.

For the over-temperature protection an internal IC sensor is used. No further configuration steps are required for this protection. Over-temperature is activated at 140°C junction temperature. With activation I_{LED} is reduced to one third. Please refer to the datasheet.

Hot-plug protection protects the LED array from spikes and surges during the turn-on and connection phase. No further configuration steps are required for this protection. Hot-plug is activated whenever V_{SENSE} is below 8 mV. During this time $I_{LED}$is limited to 4 percent of $I_{LED,max}$ by reduction of the reference voltage for *VSENSE* from 400 mV to 16 mV. On reconnection this protects the LED string from surge current.

2 BCR601 detailed description

Note: A removed LED string reduces V_{DROP} to 0 V by discharging via the pass element. This caused the voltage loop to saturate V_{IN+}, V_{sec} at its device depending on the maximum voltage. Hot-plug disabling has a delay of 2 µs. The time constant of the active headroom control exceeds this time. So for 2 µs the pass element has an additional power exposition of $P_{hp} = (V_{sec,sat} - V_{sec,ahc}) * I_{LED} * 0.04$. After deactivation of the hot-plug, until the set-point of the active headroom control is reached again and additional power dissipation with $P_{hp,\,max} = (V_{sec,sat} - V_{sec,ahc}) * I_{LED}$ is exposed to the pass element. This has to be considered in the SOAs of the pass element.

In case of a short of one or more LEDs the given LED current does not deviate from its set-point. Headroom voltage is reduced to the remaining number of active LEDs within the time constant of the voltage feedback loop. Configuration is done by the configuration of the feedback voltage loop.

2.7 Power loss optimization

This section describes how to optimize light efficiency considering thermal effects.

Means of power loss optimizations:

- AC input ripple reduction

LED temperature compensation is done automatically by current regulation.

2.7.1 AC ripple reduction

The BCR601 has a unique feature that minimizes power loss within the pass element due to AC ripple on the secondary side.

The magnitude of the ripple at V_{sec}, V_{IN+} is sensed indirectly by the BCR601 , and the AHC continuously monitors and regulates an optimized secondary side voltage to properly regulate the LED array and reduce power loss across the pass element..

Parameters of influence for the output ripple are with respect to the capacitor C_{in}:

- Value,
- Tolerance.

Tolerance of electrolytic capacitors can be in the range of -20 percent to up to 50 percent.

Input ripples can also be reduced by bulk capacitors. Lower input ripples directly reduce the power dissipation at the transistor.

Electrolytic capacitors used on the secondary side of the LED driver determine the magnitude of AC voltage ripple of the LED driver. Lower ripple on the secondary side is recommended, which directly reduces the power dissipation at the transistor. Figure 20 shows the input ripple of V_{IN+} in case of the reference configuration of the BCR601 demonstrator design.

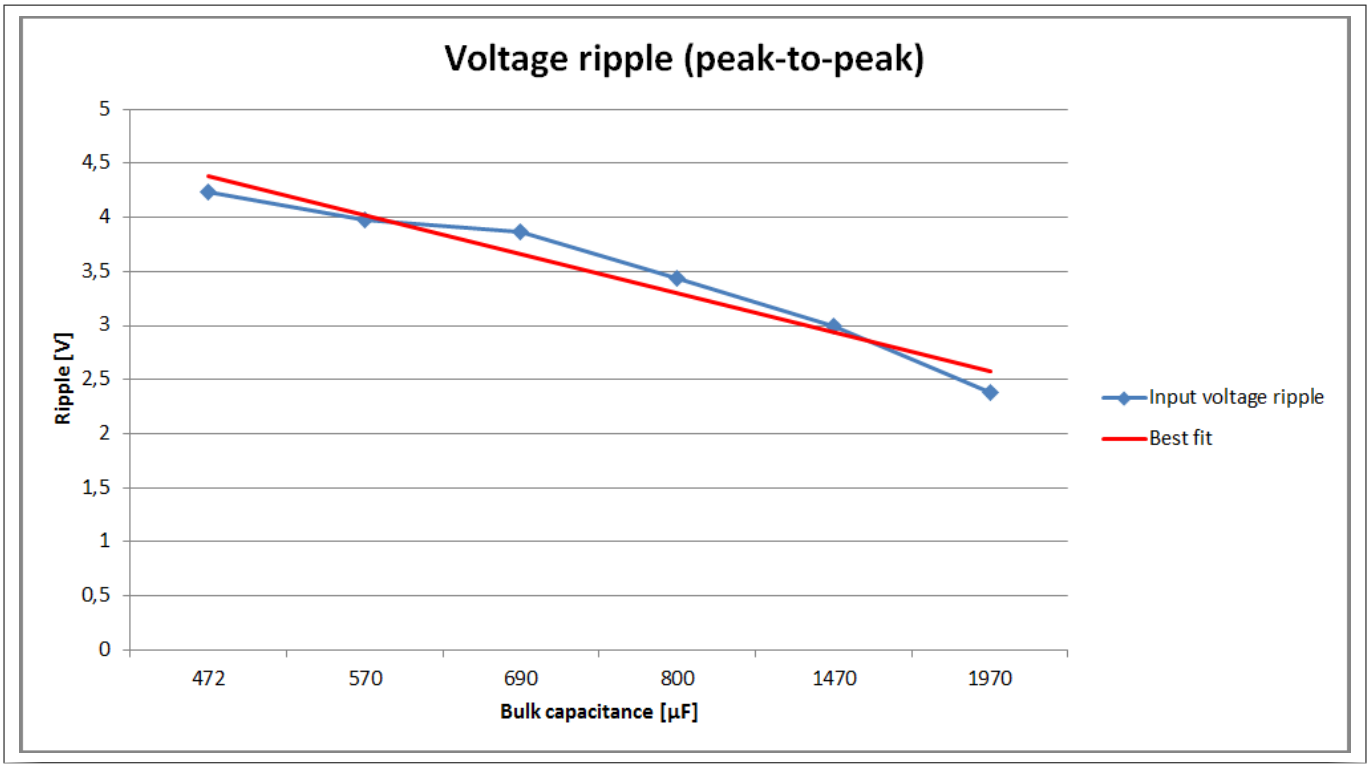


Figure 20 Input ripple versus input capacitor

2.8 Troubleshooting

2.8.1 Start-up time

This section describes how to optimize the start-up time.

Start-up time depends on these external components of the BCR601 system:

- C_{PI}
- R_{PI}
- R_{DROP}

A value increase of these components, increases the start-up time.

Regardless of whether the opto-coupler uses the V_{SEC}, V_{IN+} rail or V_{AUX} rails as its supply voltage, LED current starts to flow as soon as the input voltage gets above the minimum forward voltage of the LED chain. This may lead to some brief flicker at the doubled AC-line frequency, which usually disappears in a time frame of 250 ms depending on the response speed of the individual voltage loop.

2.8.2 Unstable current regulation due to insufficient voltage headroom

This section covers effects of an unstable current regulation loop caused by insufficient voltage headroom on the secondary-side output voltage (V_{SEC}, V_{IN+}).

The target is to keep the power loss over the transistor as low as possible, hence keeping V_{DRAIN} as low as possible.

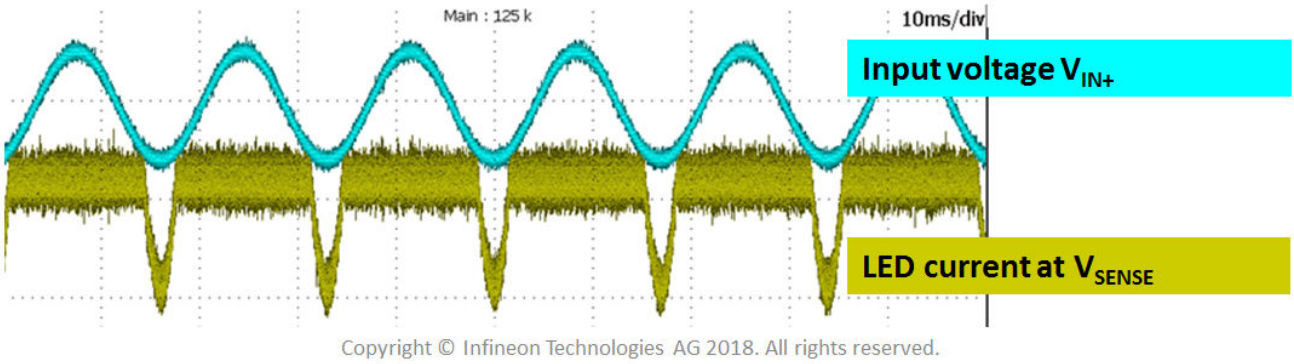
Note: Issues of current instabilities do not occur in the case of a properly configured feedback voltage loop! If this occurs it can be solved by an increase in the value of resistor R_{DROP}.

Note: R_{DROP} is configured at the sweet spot. It is kept as low as possible for minimization of the power dissipation over the pass element and high enough for a stable current control under all operating conditions.

A too low value of R_{DROP} in case of a mean input voltage plus an AC offset ripple causes an insufficient power supply at the low point of the AC phase. The LED signal starts to flicker.

Instability will first be observed during the valley of the AC ripple component seen on the secondary-side voltage, which is superposed to the DC voltage. If the minimum headroom is not available for proper LED current regulation, the LED current will reduce and be considered unstable. (See illustration below, Figure 21 .)

The range of the AC offset therefore also defines the minimum voltage drop over the transistor. The higher the peak-to-peak value of the AC offset, the higher the required average voltage drop over the transistor.



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Image legend

- Blue: V_{IN+} - Input voltage,
- Yellow: V_{SENSE} - LED current sensing.

Figure 21 Partial loss of current control caused by too low V_{IN+}

Depending on the behavior of the primary side, under voltage flickering might occur only in certain ranges of the *MFIO* dimming level. This is known as island of instability. The sizes of these islands of instability might differ depending on whether the dimming voltage is increasing or decreasing.

Acceptance test of the voltage loop is a double dimming sweep over the whole dimming range, one times in upwards, one times in downwards direction.

Note: Input signals delivered by the primary side might not always be sinusoidal. Also ramp like signals can be seen. It is paramount the minimum value of the input signal remains above the minimum forward voltage of the LED chain at the give LED current.

The optimum transistor input voltage V_{DRAIN} in case of a MOSFET, $V_{collector}$ in case of a BJT to achieve flicker-free LED current over ground is:

(1, MOSFET)

$$V_{\mathrm{DRAIN,\,min}} = V_{\mathrm{SENSE}} + R_{\mathrm{DS,\,on}} * I_{\mathrm{LED,\,target}}$$
$$V_{\mathrm{DRAIN,\,min}} = 400\,\mathrm{mV} + R_{\mathrm{DS,\,on}} * I_{\mathrm{LED,\,target}}$$

(2, BJT)

$$V_{\mathrm{collector,\,min}} = V_{\mathrm{SENSE}} + V_{\mathrm{CE}}$$
$$V_{\mathrm{collector,\,min}} = 400\,\mathrm{mV} + V_{\mathrm{CE}}$$

Equation 14 Minimum transistor input voltage

V_{DRAIN}, $V_{Collector}$ margin

The resistor R_{DROP} defines the voltage level of the drain in case of a MOSFET, the collector in case of a BJT above ground. This can be calculated according to Equation 15.

$$V_{\mathrm{DRAIN,\,collector}} = I_{\mathrm{VDROP,\ typical}} * R_{\mathrm{DROP}} = \ 5.5\,\mu\mathrm{A} * R_{\mathrm{DROP}} \ + 310\ \ \mathrm{mV}$$

$$V_{\mathrm{DRAIN,\,collector}} = I_{\mathrm{LED}} * R_{\mathrm{DROP}} + \frac{V_{\mathrm{AC,\,pp}}}{2} + 400\ \mathrm{mV}$$

$$R_{\mathrm{DROP}} = \frac{I_{\mathrm{LED}} * R_{\mathrm{DS(on)}} + \frac{V_{\mathrm{AC,\,pp}}}{2} + 90\ \mathrm{mV}}{5.5\,\mu\mathrm{A}}$$

Equation 15 **V_{DRAIN}, $V_{Collector}$ voltage level**

2.8.3 LED stack oscillations

This section describes how to stabilize in case of very long connecting lines between BCR601 and the LED stack.

In the application diagram in Figure 2 the pass element is connected to the capacitor C_{DRAIN}. The purpose of this capacitor is to remove high frequent oscillations caused by parasitic capacitors of long wire connections. 100 nF is sufficient even in case of very long cables to suppress the oscillations.

3 Implementation and design steps

This section describes the design steps and gives two application examples.

Design steps:

1. Selection of:
   - **a.** Type of LEDs and number of LEDs, in case of an LED driver, minimum and maximum numbers of LEDs
   - **b.** Target output current
   - **c.** Supply of input voltage and power
   - **d.** Power transistor for linear control
2. Selection of the *VSENSE* resistors for the current control loop. The resistors must fulfill the power class of the power drop required by the target current.
3. Check of IC supply level 8 V < V_S < 60 V
   - **a.** Calculate the highest DC input voltage. The highest input voltage assumes the elements, especially the LEDs at their highest achievable forward voltage per element during operation.
   - **b.** Calculate the maximum output power of the system consisting of the primary and the secondary side. The primary side must fulfill the power limits of the secondary side.
   - **c.** Check the thermal conditions of the power transistor; the heating of the power transistor must not violate peak thermal conditions of the system.
   - **d.** Define the input capacitor and check the resulting AC ripple at line frequency
4. Supply of the OPTO path:
   - Single supply voltage: Select the Zener diode so $V_{breakdown,Zener}$ << $V_{IN,CD}$, calculate protection resistor R_{ZENER}.
   - Second supply voltage, auxiliary supply voltage: V_{aux} << $V_{IN,DC}$; an additional stabilizing Zener diode is optional.
5. Definition of the OVP level
6. Configuration of the voltage feedback control loop
   - **a.** As starting for R_{DROP} use the value calculated by Equation 15 and select next higher standard value, a value for R_{OPTO} derived from the Equation 10 and select next smaller standard value and setting for C_{PI} and R_{PI} according to the transfer function as described in Compensator Bode plot dependency on components .
   - **b.** Selection of C_{PI} and R_{PI} with a closed-loop crossover frequency much less than 100 Hz and a closed-loop gain at 1 Hz of ~ 20 dB
   - **c.** Optimization of C_{PI} and R_{PI} until flicker free operation is achieved under all dimming conditions. Flicker free means gain of AHC is configured high enough, so V_{DS} in case of a MOSFET, V_{CE} in case of a BJT is always high enough to achieve the desired target.
   - **d.** If necessary reduce R_{DROP} so that V_{DRAIN}, $V_{collector}$ at no AC ripple fulfills this equation: $V_{\mathrm{DRAIN}|\ \mathrm{collector,\ DC}} = V_{\mathrm{SENSE}} + \left(\left(R_{\mathrm{DS(on)}} * I_{\mathrm{target}}\right) \vee V_{\mathrm{CE}}\right) + \Delta_{\mathrm{VDRAIN}|\ \mathrm{Vcollector,\ margin}}$. The V_{DRAIN}, $V_{Collector}$ margin is a safety margin taking into account sample variation for R_{DROP}. Usually the value is set to be less than 100 mV. The value can be calculated using Equation 15.

Due to the feedback control, in a BCR601 system there is no need to adapt V_{IN}.

Because of the need for thermal power optimization R_{OPTO} is not seen as free parameter of the transfer function of the AHC feedback voltage loop.

Opto-coupler usually have a wide range in the current transfer ratio (CTR). Because the CTR must be fulfilled under all conditions, R_{OPTP} is not seen as free parameter of the transfer function of the AHC feedback voltage loop.

For the power selection of the power transistor please refer to BCR601 pass element selection.

The input stage is usually an ACDC stage. The ACDC stage is very often realized by a PCF/Flyback like the Infineon XDPL8218. Usually the input voltage is offset by an AC ripple. This AC ripple can be reduced by an increased input capacitor and must be considered with regard to thermal aspects. Please refer to AC ripple reduction .

3.1 Application example using OptiMOS™ BSP716N MOSFET

This section gives the example of designing a light engine capable of driving 12 to 16 OSLON LEDs at 500 mA using a low-cost package MOSFET.

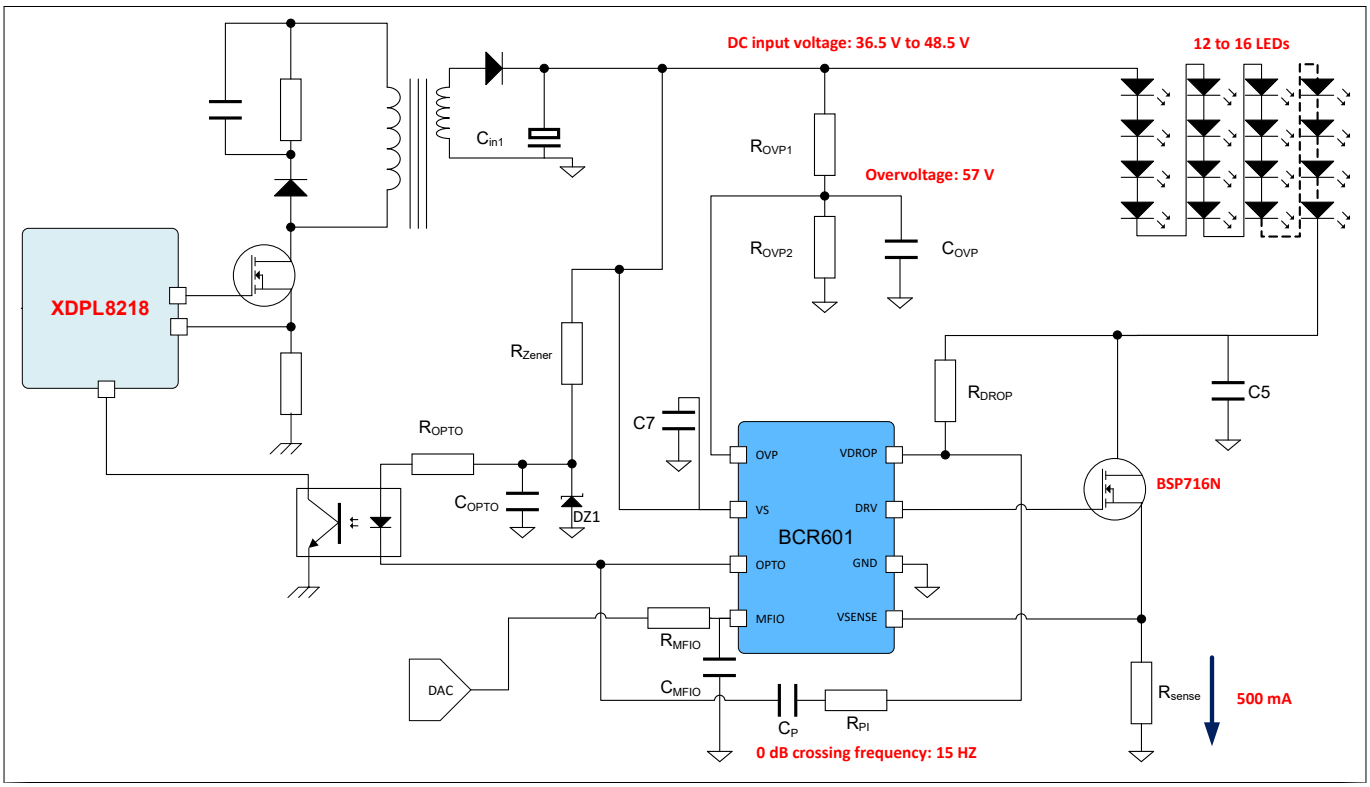


Figure 22 Light engine with 12 to 16 LEDs at 500 mA using MOSFET BSP716N

System parameters:

- Number of LEDs in the system: 12 to 16, OSLON Square™ capable of a target current of up to 1800 mA,
- Voltage supply: XDPL8218 Flyback/PFC 40 W as primary side,
- Power transistor: Infineon OptiMOS™ BSP716N,
  - $I_{D,max}$ = 2.3 A
  - V_{DS} = 75 V
  - $R_{DS(on)}$ = 0.16 Ω
  - R_{thJA} = 70 K/W
  - Logic level
- I_{target} = 500 mA,
  - R_{SENSE} = 400 mV/500 mA = 0.8 Ω
  - Power loss over *VSENSE* resistor: P = V_{SENSE}*I_{target} = 400 mV * 500 mA = 0.2 W
  - Split up in two resistors R_{11} = 1.3 Ω, R_{12} = 2.2 Ω, $R_{VSENSE,\,eff} = \frac{1}{\frac{1}{1.3\Omega} + \frac{1}{2.2\Omega}} = 0.82\ \Omega$

- Voltage sum:
  - Forward voltage at 85°C: $V_{f,LED}$ = 2.85 V
  - Relative forward voltage at 20°C (room temperature): $\Delta V_{f,LED}$ = 0.15 V
  - DC start-up voltage at 12 LEDs: $V_{LED,11,DC}$ = 12*(2.85 V + 0.15 V) + 400 mV + 80 mV ($R_{DS(on)}$) = 36.5 V
  - DC start-up voltage at 16 LEDs: $V_{LED,16,DC}$ = 16*(2.85 V + 0.15 V) + 400 mV + 80 mV ($R_{DS(on)}$) = 48.5 V
  - This fulfills the supply level range of the IC between 8 V and 60 V, no power reduction resistor is used
  - Maximum DC output power: $P_{max,DC,\ 16\ LEDs}$ = 48.5 V * 500 mA = 24.25 W
- Thermal limits:
  - Input capacitor C_{IN} = 470 µF
  - AC ripple: $V_{AC,pp}$ = 4 V
  - Average power dissipation of BSP71N: $P_{diss,BSP716N} = I_{LED}*(V_{AC,pp}/2 + \Delta_{V_{DROP}\ margin}) + R_{DS(on)}*I_{target}^2$ = 500 mA * (4 V/2 + 50 mV) + 0.16 Ω* 500 mA^2 = 1.065 W
  - Theoretical calculation of the headroom of V_{DRAIN}:

$$V_{\mathrm{DRAIN,\ BSP716}N\mathrm{,\ headroom}} = V_{\mathrm{DRAIN,\ BSP716}N} - \left(\frac{V_{\mathrm{AC,\ pp}}}{2} + V_{\mathrm{DS}} + V_{\mathrm{SENSE}}\right) = 5.5\ \mu\mathrm{A} * 430\ \mathrm{k\Omega}\ +\ 310\ mV$$

$$-\frac{V_{\mathrm{AC,\ pp}}}{2} - R_{\mathrm{DS(on)}} * I_{\mathrm{LED}} -\ 400\ \mathrm{mV} = 2.67\ V\ -2\ V\ -0.08\ V - 400\ \mathrm{mV} = 190\ \mathrm{mV}$$

  - Expected operating temperature BSP716N: $T_{BSP716N} = T_{room} + R_{thJA}*P_{diss,BSP716N}$ = 20°C + 70 K/W*1.065 W = 94°C
  - Power consumption including AC ripple: $P_{total,\ 16\ LEDs} = P_{max,DC,\ 16\ LEDs} + P_{diss,BSP716N} + P_{VSENSE}$ = 24.25 V + 1.04 W + 500 mA*400 mV = 25.5 W. XDPL8218 has a maximum output power of 40 W. So all applications from 12 to 16 OSLON LEDs are within this limit.
- Supply of OPTO path:
  - Because the minimum DC value of the light engine is 36.5 V, 15 V is chosen as supply voltage of the *OPTO* path.
  - Infineon XDPL8218 reference design supplies a 15 V secondary voltage; this voltage can be used without further measures, for auxiliary voltage supply solutions please refer to Auxiliary supply voltage for the *OPTO* path.
  - In case of just using a single winding on the secondary side a Zener diode at a breakdown voltage of 8 V is chosen, for single supply voltage please refer to Opto-coupler design with single voltage output rail on secondary side.
  - Protection resistor R_{ZENER}: To always enable an *OPTO* current of 3.6 mA maximum, the resistor is selected to generate a current of 4 mA at the worst case voltage drop. $R_{\mathrm{Zener}} = \frac{V_{\mathrm{in,\ min,\ 12LEDs}} - V_{\mathrm{Zener}}}{I_{\mathrm{OPTO}}} = \frac{36.5V - 15V}{4\ \mathrm{mA}} = 5.3\ \mathrm{k\Omega}$. For simplicity a 5.1 kΩ resistor is selected. The worst case power dissipation is .

$$P_{R_{\mathrm{Zener}}} = \frac{(V_{\mathrm{in,}} - V_{\mathrm{Zener}})^2}{R_{\mathrm{Zener}}} = \frac{(56.5\ V - 15\ V)^2}{5.1\ \mathrm{k\Omega}} = 337\ \mathrm{mW}$$

. An example for such kind of a resistor is KTR23 from ROHM semiconductor.
- Opto-coupler: Toshiba TLP383,
  - Collector-emitter voltage V_{CEO} = 80 V
  - Input forward voltage $V_{F,typical}$ = 1.25 V
  - Current transfer ratio $(I_C/I_F)_{max}$ = 600 percent
  - Maximum R_{OPTO} according to Equation 10:

$$R_{\mathrm{OPTO}} < \frac{V_{\mathrm{OPTO,\ supply}} - V_{F,\ \mathrm{typical}} - 3V}{2\ \mathrm{mA}} * 0.9 \Rightarrow R_{\mathrm{OPTO}} < 12.7\mathrm{k\Omega}$$

- OVP:
  - The maximum input voltage is: $V_{IN,max,\ 16\ LED} = V_{LED,16,DC} + V_{AC,pp}$= 48.5 V + 4 V = 52.5 V
  - With a headroom of 9 percent the over-voltage is configured to 57 V
  - OVP trigger level is defined by the IC to 1.12 V
  - R_{OVP2} = 3 kΩ
  - $R_{OVP2,eff}$ = 2.93 kΩ
  - R_{OVP1}= 146 kΩ
  - For better usability, these values are rounded to R_{OVP1} = 150 kΩ and R_{OVP2} = 3.6 kΩ
  - Please refer to OVP configuration,
- Configuration AHC, voltage feedback to primary side:
  - C_{PI} = 120 nF
  - R_{PI} = 8.2 kΩ
  - R_{OPTO} = 13 kΩ
  - R_{DROP} = 430 kΩ
  - Closed-loop crossing frequency $f_{0\ dB}$ = 15 Hz
  - Closed-loop phase margin greater than 95°
  - Please also refer to Compensator Bode plot dependency on components.

3.2 Application example using IRFR120N MOSFET

This section gives an example of a high-current design.

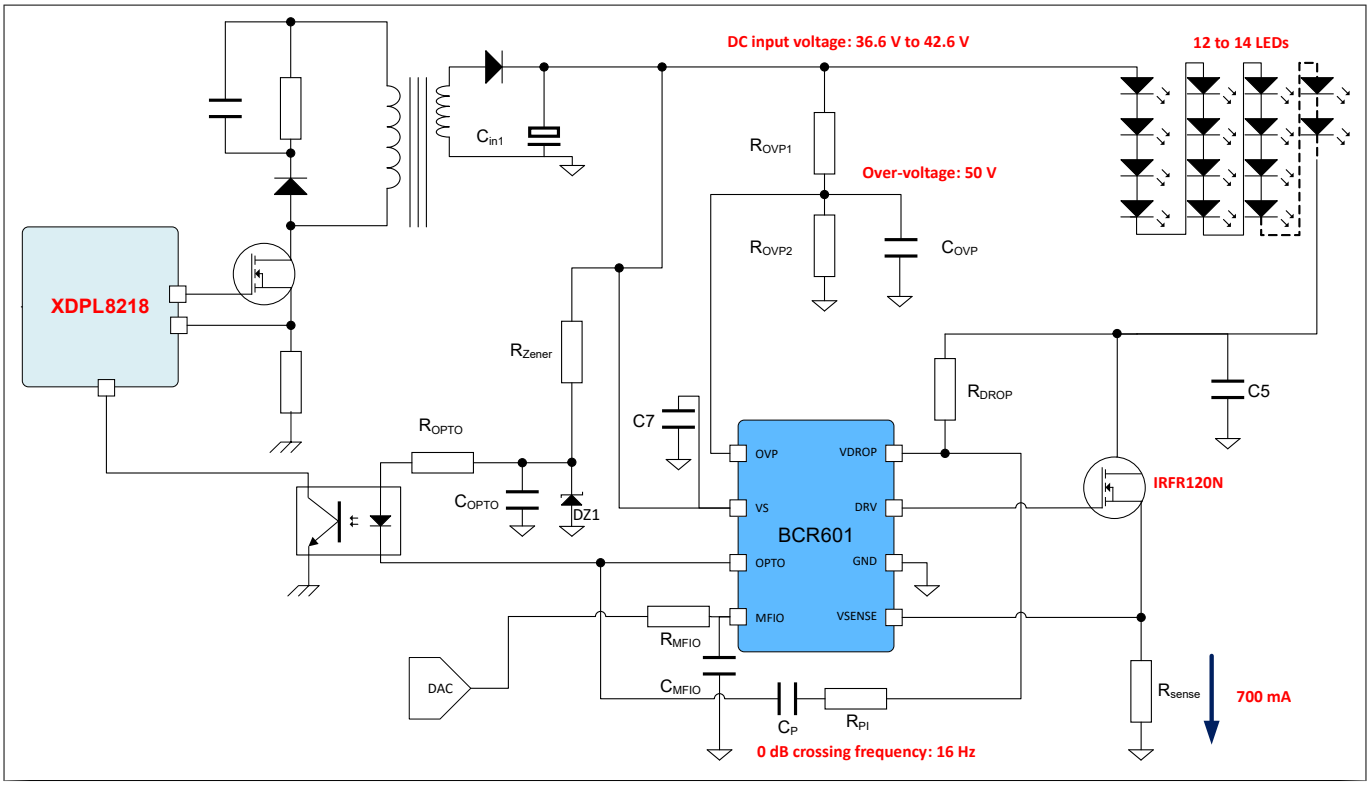


Figure 23 LED driver with 12 to 14 LEDs at 700 mA using MOSFET IRFR120N

IRFR120N due to its DPAK, TO-252 package, has a low thermal resistance R_{thJA}. This enables a high target current of 700 mA.

System parameters:

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- Number of LEDs in the system: 12 to 14, OSLON Square™ capable of a target current of up to 1800 mA,
- Voltage supply: XDPL8218 Flyback/PFC 40 W as primary side,
- Power transistor: Infineon IRFR120N,
  - $I_{D,max,\ T_C\ at\ 100°C}$ = 6.6 A
  - V_{DS} = 100 V
  - $R_{DS(on),max}$ = 0.21 Ω
  - $R_{\Theta JA}$ = 50 K/W
- I_{target} = 700 mA
  - R_{SENSE} = 400 mV/700 mA = 0.574 Ω
  - Power loss over *VSENSE* resistor: P = V_{SENSE}*I_{target} = 400 mV * 700 mA = 280 mW
  - Split into two resistors R_{11} = 1.1 Ω, R_{12} = 1.2 Ω, $R_{\mathrm{VSENSE,\ eff}} = \frac{1}{\frac{1}{1.3\Omega} + \frac{1}{2.2\Omega}} = 0.82\ \Omega$.
- Voltage sum:
  - Forward voltage at 85°C: $V_{f,LED}$ = 2.85 V
  - Relative forward voltage at 20°C (room temperature): $\Delta V_{f,LED}$ = 0.15 V
  - DC start-up voltage at 12 LEDs: $V_{LED,11,DC}$ = 12*(2.85 V + 0.15 V) + 400 mV + 0.15 V ($R_{DS(on)}$) = 36.6 V
  - DC start-up voltage at 14 LEDs: $V_{LED,16,DC}$ = 14*(2.85 V + 0.15 V) + 400 mV + 0.15 V ($R_{DS(on)}$) = 42.6 V
  - This fulfills the supply level range of the IC between 8 V and 60 V, no power reduction resistor is used
  - Maximum DC output power: $P_{max,DC,\ 16\ LEDs}$ = 42.6 V * 700 mA = 29.8 W
- Thermal limits:
  - Input capacitor C_{IN} = 800 µF
  - AC ripple: $V_{AC,pp}$ = 3.2 V
  - Average power dissipation of IRFR120N: $P_{diss,IRFR120N} = I_{LED}*(V_{AC,pp}/2 + \Delta_{V_{DROP}\ margin}) + R_{DS(on)}*I_{target}^{\ 2}$ = 700 mA * (3.2 V/2 + 50 mV) + 0.21 Ω* 700 mA^2 = 1.302 W
  - Theoretical calculation of the headroom of V_{DRAIN}:

$$V_{\mathrm{DRAIN,\ IRFR120}N\mathrm{,\ headroom}} = V_{\mathrm{DRAIN,\ IRFR120}N} - \left(\frac{V_{\mathrm{AC,\ pp}}}{2} + V_{\mathrm{DS}} + V_{\mathrm{SENSE}}\right) = 5.5\ \mu\mathrm{A} * 360\ \mathrm{k}\Omega\ +\ 310\ m$$

$$V\ - \frac{V_{\mathrm{AC,\ pp}}}{2} - R_{\mathrm{DS(on)}} * I_{\mathrm{LED}} -\ 400\ \mathrm{mV} = 1.98\ V\ - 1.6\ V\ - 0.15\ V - 90\ \mathrm{mV} = 140\ \mathrm{mV}$$

  - Expected operating temperature IRFR120N: $T_{IRFR120N}$ = T_{room} + RΘ_{JA}*$P_{diss,IRFR120N}$ = 20°C + 50 K/W*1.302 W = 85.1°C
  - Power consumption including AC ripple: $P_{total,\ 14\ LEDs}$ = $P_{max,DC,\ 16\ LEDs}$ + $P_{diss,IRFR120N}$ + P_{VSENSE} = 29.8 W + 1.29 W + 700 mA * 400 mW = 31.37 W. XDPL8218 has a maximum output power of 40 W. So all applications from 12 to 14 OSLON LEDs are within this limit
- Supply of OPTO path:
  - Because the minimum DC value of the LED driver is 36.6 V, 15 V is chosen as supply voltage of the *OPTO* path
  - Infineon XDPL8218 reference design supplies a 15 V secondary voltage; this voltage can be used without further measures; for auxiliary voltage supply solutions please refer to Auxiliary supply voltage for the *OPTO* path
  - In case of just using a single winding on the secondary side a Zener diode at a breakdown voltage of 15 V is chosen, for single supply voltage please refer to Opto-coupler design with single voltage output rail on secondary side
  - Protection resistor R_{ZENER}: To always enable an *OPTO* current of 3.6 mA maximum, the resistor is selected to generate a current of 4 mA at the

3 Implementation and design steps

worst case voltage drop. $R_{\text{Zener}} = \frac{V_{\text{in, min, 12LEDs}} - V_{\text{Zener}}}{I_{\text{OPTO}}} = \frac{36.6V - 15V}{2\,\text{mA}} = 10.8\,\text{k}\Omega$. For simplicity a 10 kΩ resistor is selected. The worst case power dissipation is .

$$P_{R_{\text{Zener}}} = \frac{(V_{\text{in, max, 16LED}} - V_{\text{Zener}})^2}{R_{\text{Zener}}} = \frac{(56.5\,V - 15\,V)^2}{10\,\text{k}\Omega} = 76\,\text{mW}$$

- Opto-coupler: Vishay CNY17,
  - Collector-emitter voltage V_{CEO} = 70 V
  - Input forward voltage $V_{F,typical}$ = 1.39 V
  - Current transfer ratio $(I_C/I_F)_{max}$ = 320 percent
  - Maximum R_{OPTO} according to Equation 10: $R_{\text{OPTO}} < \frac{V_{\text{OPTO, supply}} - V_{F,\text{ typical}} - 3V}{2\,\text{mA}} \Rightarrow R_{\text{OPTO}} < 19\,\text{k}\Omega$
- OVP:
  - The maximum input voltage is: $V_{IN,max,\ 16\ LED} = V_{LED,14,DC} + V_{AC,pp}$= 42.6 V + 3.2 V = 45.8 V
  - With a headroom of 9 percent the over voltage is configured to 50 V
  - OVP trigger level is defined by the IC to 1.12 V
  - R_{OVP2} = 3 kΩ
  - $R_{OVP2,eff}$ = 2.93 kΩ
  - R_{OVP1} = 131 kΩ
  - For better usability, these values are rounded to R_{OVP1} = 130 kΩ and R_{OVP2} = 3 kΩ
  - Please refer to OVP configuration
- Configuration active headroom control, voltage feedback to primary side:
  - C_{PI} = 100 nF
  - R_{PI} = 20 kΩ
  - R_{OPTO} = 16 kΩ
  - R_{DROP} = 360 kΩ
  - Closed-loop crossing frequency $f_{0\,dB}$ = 16 Hz
  - Closed-loop phase margin more than 100 degrees
  - Please also refer to Compensator Bode plot dependency on components

4 References

1. Engineering report for BCR601, Infineon Technologies AG, Munich 2018
2. BCR601 Datasheet, Infineon Technologies AG, Munich 2018
3. BCR601, Application Board Schematics and PCB, Infineon Technologies AG, Munich 2018

Revision history

Document version	Date of release	Description of changes
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1.0	2019-02-07	Initial release

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