ICE3ARxx80CJZ

CoolSET® F3R80CCM (DIP-7) brownout & CCM version Design Guide

Power Management & Supply



Never stop thinking.

Published by
Infineon Technologies AG
81726 Munich, Germany
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ICE3ARxx80CJZ

Revision History:	**2012-09**	V1.4
Previous Version:	1.3	
Page	Subjects (major changes since last revision)	
20	typo error	

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1 Introduction

The CoolSET®-F3R80CCM, **ICE3ARxx80CJZ** is the latest development of the CoolSET® in continuous conduction mode (CCM) operation. It is a PWM controller with power MOSFET and startup cell in a DIP-7 package. The switching frequency is running at 100 kHz and it targets for DVD player, set-top box, portable game console, white goods, auxiliary power supply for server/PC, etc.

The **ICE3ARxx80CJZ** adopts the BiCMOS technology and provides a wider Vcc operating range up to 24.7V. It inherits the proven good features of CoolSET® -F3R such as Active Burst Mode, propagation delay compensation, soft gate drive, auto restart protection for major faults (Vcc over voltage, over load, open loop Vcc under voltage, short optocoupler and over temperature), it also has the selectable entry and exit burst mode level, brownout feature, built-in soft start time, built-in blanking time for short duration peak power, frequency jitter feature, slope compensation for CCM operation, external latch enable and fast AC reset, etc. The particular features need to be stressed are 800V MOSFET, CCM/DCM operation, fixed voltage Brownout detect/reset, fast AC reset, the best-in-class low standby power and the good EMI performance.

2 List of Features

800V avalanche rugged CoolMOS® with Startup Cell
Active Burst Mode for lowest Standby Power
Slope compensation for CCM operation
Selectable entry and exit burst mode level
100kHz internally fixed switching frequency with jittering feature
Auto Restart Protection for Over load, Open Loop, VCC Under/Over voltage and Over temperature
External latch enable pin and fast AC reset
Over temperature protection with 50°C hysteresis
Built-in 10ms Soft Start
Built-in 40ms blanking time for short duration peak power
Propagation delay compensation for both maximum load and burst mode
Brownout feature
BiCMOS technology for low power consumption and wide VCC voltage range
Soft gate drive with 50Ω turn on resistor

3 Package

The package for F3R80CCM ICE3ARxx80CJZ brownout and frequency jitter mode product is DIP-7.

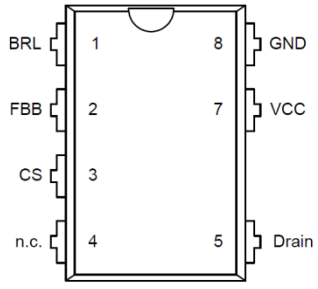


Figure 1 Pin configuration

Pin	Name	Description
1	BRL	Brownout, fast AC Reset & Latch enable
2	FBB	Feedback & Burst entry/exit control
3	CS	Current Sense/800V CoolMOS® Source
4	n.c	not connected
5	Drain	800V CoolMOS® Drain
6	-	(no pin)
7	VCC	Controller Supply Voltage
8	GND	Controller Ground

4 Block Diagram

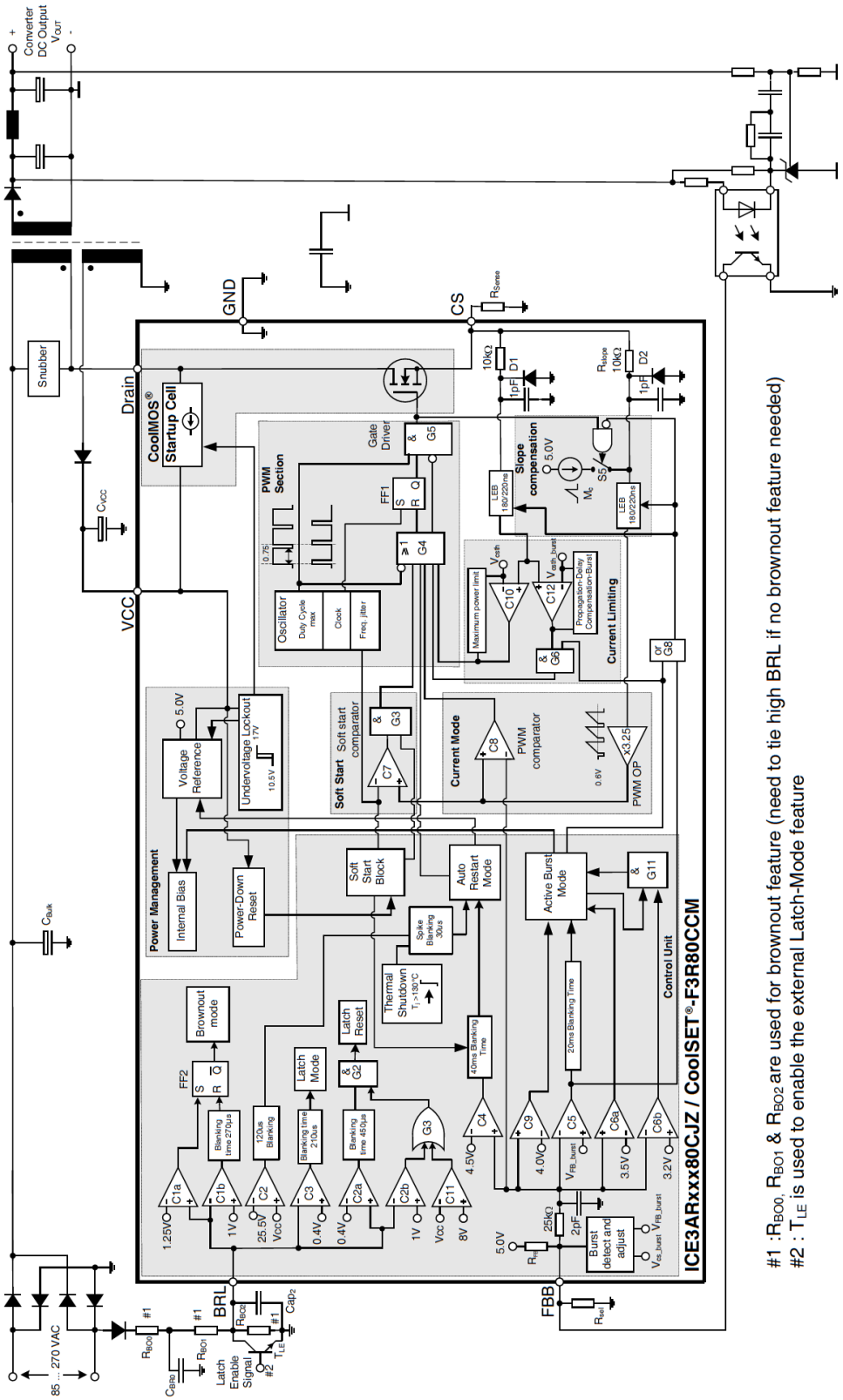


Figure 2 Block Diagram of ICE3ARxx80CJZ

5 Typical Application Circuit

(circuit with output OVP latch, brownout and fast AC reset features, etc.)

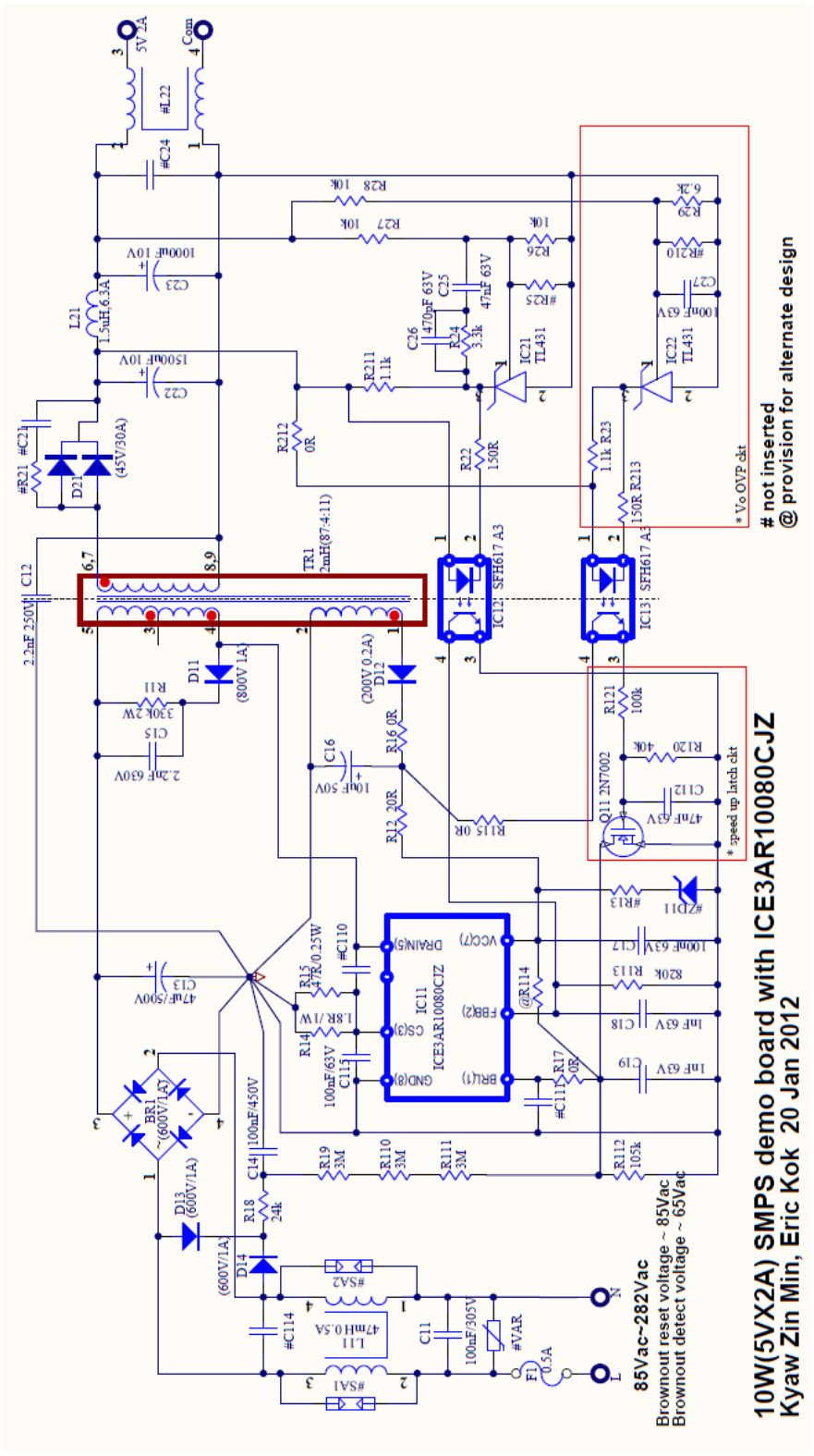


Figure 3 Typical application circuit with ICE3AR10080CJZ 10W 5V

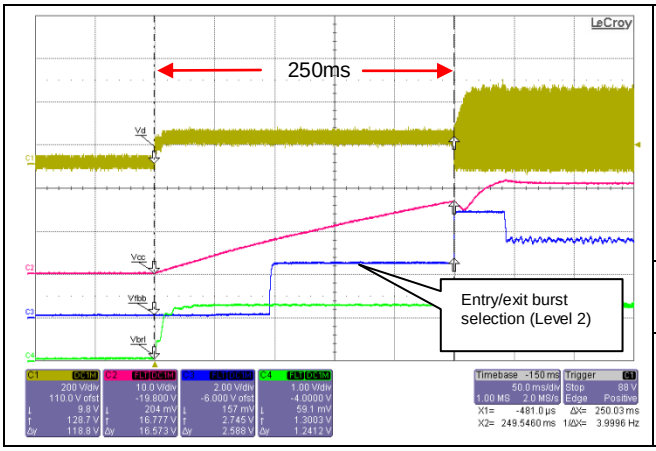
6 Functional description and component design

6.1 Startup time

Startup time is counted from applying input voltage to IC turn on. ICE3ARxx80CJZ has a startup cell which is connected to input bulk capacitor. When there is input voltage, the startup cell will act as a constant current source to charge up the Vcc capacitor and supply energy to the IC. When the Vcc capacitor reaches the Vcc_on threshold 17V, the IC turns on. Then the startup cell is turned off and the Vcc is supplied by the auxiliary winding. Start up time is independent from the AC line input voltage and it can be calculated by the equation (1). Figure 4 shows the start up time of 85Vac line input.

$$t_{StartUp} = \frac{V_{VCCon} \times C_{VCC}}{I_{VCCcharge}} \quad (1)$$

where, $I_{VCCcharge}$: average current of $I_{VCCcharge2}$ and $I_{VCCcharge3}$ (0.875mA),
V_{VCCon} : IC turns on threshold (17V),
C_{VCC} : Vcc capacitor
Please refer to the datasheet for the symbol used in the equation.



Channel 1; C1 : Drain voltage (V_D)
Channel 2; C2 : Supply voltage (V_{CC})
Channel 3; C3 : Feedback voltage (V_{FBB})
Channel 4; C4 : BRL voltage (V_{BRL})

Measured startup time = 0.25s

Startup @ 85Vac & max. load

Figure 4 The startup delay time at AC line input voltage of 85Vac

Pre-caution : For a typical application, start up should be VCC ramps up first, other pin (such as FBB pin) voltage will follow VCC voltage to ramp up. It is recommended not to have any voltage on other pins (such as FBB; BRL and CS) before VCC ramps up.
In addition, the dummy load in the Vcc pin should be larger than 150KΩ. Otherwise, it would have a risk of delay startup.

6.1.1 Vcc capacitor

The minimum value of the Vcc capacitor is determined by voltage drop during the soft start time. The formula is expressed in equation (2).

$$C_{VCC} = \frac{I_{VCCsup2_max} \times t_{SS}}{V_{VCChys}} \times \frac{2}{3} \quad (2)$$

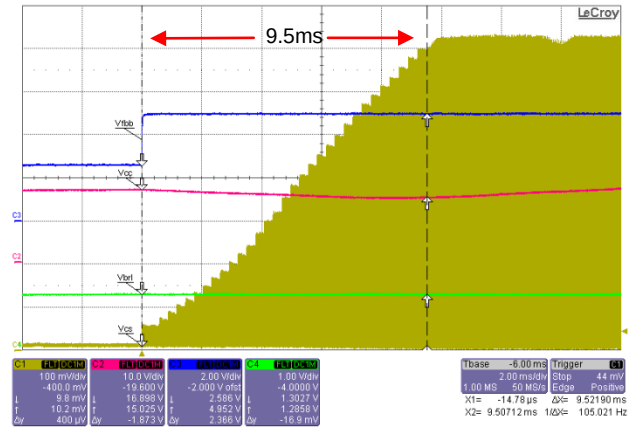
where, $I_{VCCsup2_max}$: supply current with active gate (4.8mA for ICE3AR10080CJZ)
t_{ss} : soft start time (10ms)
V_{CChys} : Vcc turn-on/off hysteresis voltage (6.5V)

Therefore, the minimum Vcc capacitance can be 4.9µF. In order to give more margins, 10uF is taken for the design. The startup time $t_{StartUp}$ is then 0.19s. The measured start up time is 0.25s (Figure 4). A 0.1uF filtering capacitor is always needed to add as near as possible to the Vcc pin to filter the high frequency noise.

6.2 Soft Start

When the IC is turned on after the startup time, a digital soft start circuit is activated. A gradually(32 steps) increased soft start voltage is emitted by the digital soft start circuit, which in turn releases the duty cycle gradually increase from zero. The duty cycle increases to maximum (which is limited by the transformer design) at the end of the soft start period. When the soft start time ends, IC goes into normal mode and the duty cycle is controlled by the FB signal. The soft start time is set at 10ms for maximum load. The soft start time is load dependent; shorter soft start time with lighter load.

Figure 5 shows the soft start behavior at 85Vac input and maximum load. The primary peak current increases slowly to the maximum in the soft start period.



Channel 1; C1 : Current sense voltage (V_{CS}) Channel 2; C2 : Supply voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FBB}) Channel 4; C4 : BRL voltage (V_{BRL})
Soft Start time = 9.5ms(32 steps)
Soft start @ Vin=85Vac & max. load

Figure 5 Soft start at AC line input voltage of 85 Vac & full load

6.3 Low standby power - Active Burst Mode

The IC will enter Active Burst Mode function at light load condition which enables the system to achieve the lowest standby power requirement of less than 100mW. Active Burst Mode means the IC is always in the active state and can therefore immediately response to any changes on the FB signal, V_{FB}.

6.3.1 Entering Active Burst Mode with selectable burst entry level

Because of the current mode control scheme, the feedback voltage V_{FB} actually controls the power delivery to output. An important relationship between the V_{CS} and the V_{FB} is expressed in equation (3).

$$V_{FB} = (V_{Mc} + V_{cs}) \cdot A_v + V_{Offset-Ramp} = (M_C \cdot t_{on} + R_{cs} \cdot I_p) \cdot A_v + V_{Offset-Ramp} \quad (3)$$

where, V_{CS} :current sense voltage
A_V :PWM OP gain (3.25)
$V_{Offset-Ramp}$:voltage ramp offset (0.6V)
M_C :slope compensation rate (50mV/µs)
t_{on} :switch on time
R_{cs} :current sense resistor
I_p :transformer primary current

When the output load reduces, the feedback voltage V_{FB} drops. If the V_{FB} stays below V_{FB_burst} for 20ms, the IC enters into the Active Burst Mode. The threshold power to enter burst mode is expressed in equation (4).

$$P_{burst_enter} = \frac{1}{2} \times L_P \times I_{P_burst}^{2} \times f_s \quad (4)$$

where, L_p : transformer primary inductance

I_{P_burst} : transformer primary current to enter burst mode

f_s : switching frequency

$$I_{P_burst} = \frac{V_{FB_burst} - V_{Offset-Ramp}}{\frac{A_V}{(\frac{M_C \times L_P}{V_{DC}}) + R_{CS}}} \quad (5)$$

where, V_{dc} :dc input voltage

V_{FB_burst} : feedback level to enter burst mode

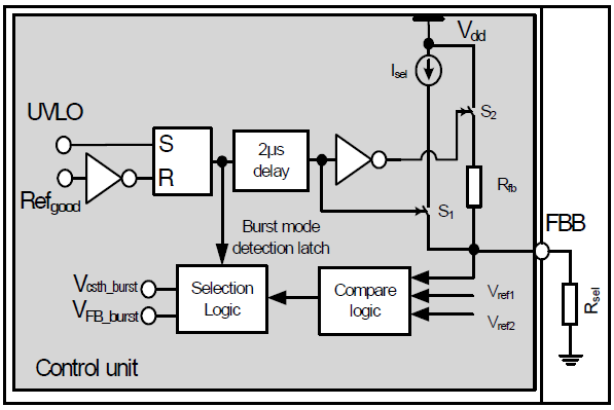
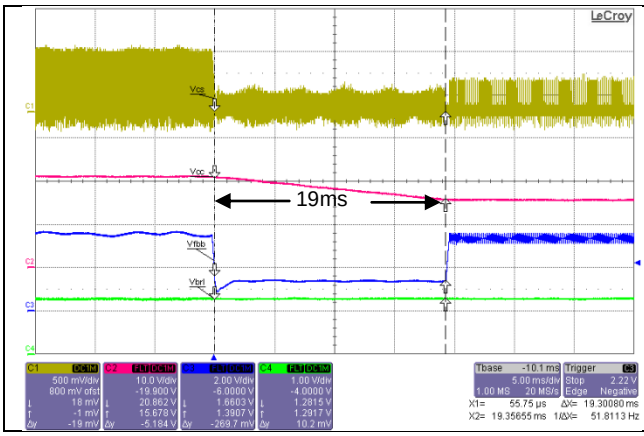


Figure 6 Burst mode detect and adjust

In enhancement to CoolSET® -F3R, user can select the burst mode entry and exit level in CoolSET® -F3R80CCM, according to the application by adding different values of R_{sel} (R113) resistor at FBB pin. The IC would detect the voltage level at the FBB pin within the V_{CC} charging time from 8V to 17V. During that detection time, the current source I_{sel} (3.5µA) current will charge the R_{sel} (R113) resistor. Based on the voltage level, the IC will select burst mode entry and exit level. There are 3 different levels of burst mode available and the following table is the recommended resistance range of the R_{sel} (R113) resistor for the entry and exit burst level.

Level	R_{sel}	V_{FBB}	Entry level		Exit level	
			% of P_{in_max}	V_{FB_burst}	% of P_{in_max}	V_{csth_burst}
1	<405kΩ	$V_{FBB} < V_{ref1}$ (1.8V)	5%	1.29V	11%	0.21V
2	685kΩ~900kΩ	V_{ref1} (1.8V) $< V_{FBB} < V_{ref2}$ (4V)	10%	1.61V	20%	0.29V
3	>1530kΩ	$V_{FBB} > V_{ref2}$ (4V)	15%	1.84V	27%	0.34V

Figure 7 shows the waveform with the load drops from nominal load to light load. After the 20ms blanking time IC goes into burst mode.



Channel 1; C1 : Current sense voltage (V_{CS}) Channel 2; C2 : Supply voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FBB}) Channel 4; C4 : BRL voltage (V_{BRL})	
Entering Active Burst mode with built-in blanking time 20ms when load changes from full to light @ Vin=85Vac	

Figure 7 Entering active burst mode

6.3.2 Working in Active Burst Mode

In the active burst mode, the IC is constantly monitoring the output voltage by feedback pin, V_{FBB}, which controls burst duty cycle and burst frequency. The burst "ON" starts when V_{FB} reaches 3.5V and it stops when V_{FB} is dropped to 3.2V. During burst "ON", the primary current limit is reduced to V_{csth_burst} (27% ~ 44% of maximum peak current) to reduce the conduction losses and to avoid audible noise. The FB voltage is swinging like a saw tooth between 3.2V and 3.5V. The corresponding secondary output ripple (peak to peak) is controlled to be small. It can be calculated by equation (6).

$$V_{out_ripple_pp} = \frac{R_{opto} \times \Delta V_{fb}}{R_{fb} \times G_{opto} \times G_{TL431}} \quad (6)$$

where, R_{opto} :series resistor with opto-coupler at secondary side (e.g. R22 in Figure 3)

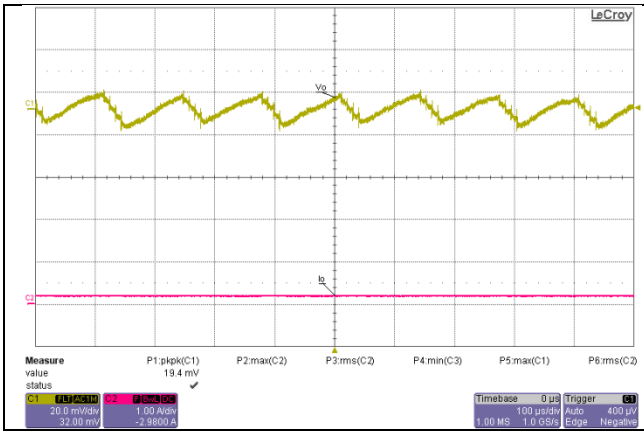
R_{fb} :IC internal pull up resistor connected to FB pin (R_{fb}=15.4KΩ)

G_{opto} :current transfer gain of opto-coupler

G_{TL431} :voltage transfer gain of the loop compensation network (e.g. R22, R211, R24, R25, R26, R27, C25, C26 in Figure 3)

ΔV_{fb} : feedback voltage change (0.3V)

Figure 8 is the output ripple waveform of the 10W 5V demo board. The burst ripple voltage is about 19mV.



Channel 1; C1 : Output ripple voltage (Vo) Channel 2; C2 : Output current (Io)	
$V_{ripple_pk_pk}$=19mV Probe terminal end with decoupling capacitor of 0.1uF(ceramic) & 1uF(electrolytic), 20MHz filter	
Output ripple voltage @ 85Vac and 1W load	

Figure 8 Output ripple during Active Burst Mode at light load

6.3.3 Leaving Active Burst Mode

When the output load increases to be higher than the maximum exit level of burst mode, V_{out} will drop a little and V_{FB} will rise up fast to exceed 4.0V. The system leaves burst mode immediately when V_{FB} reaches 4.0V. Once system leaves burst mode, the current sense voltage limit is set to V_{csth1} or V_{csth2} according the input AC line voltage, the feedback voltage V_{FBB} swings back to the normal control level.

The leaving burst power threshold (i.e. maximum power to be handled during burst operation) is expressed in equation (7). However, the actual power can be higher as it would include propagation delay time.

$$\begin{aligned} P_{burst_leave} &= 0.5 \times L_P \times \left(\frac{V_{csth_burst}}{R_{CS}}\right)^2 \times f_s \\ &= 0.5 \times L_P \times \left(\frac{V_{csth_burst}}{V_{csth}} \times \frac{V_{csth}}{R_{CS}}\right)^2 \times f_s \\ &= \left(\frac{V_{csth_burst}}{V_{csth}}\right)^2 \times P_{in_max} \end{aligned} \quad (7)$$

where, V_{csth_burst} : peak current in the burst mode

V_{csth} : maximum current limit threshold at CS pin

P_{in_max} : maximum input power

R_{CS} : current sense resistor

L_p : primary inductance of transformer

The leave burst mode timing diagram is shown in Figure 9.

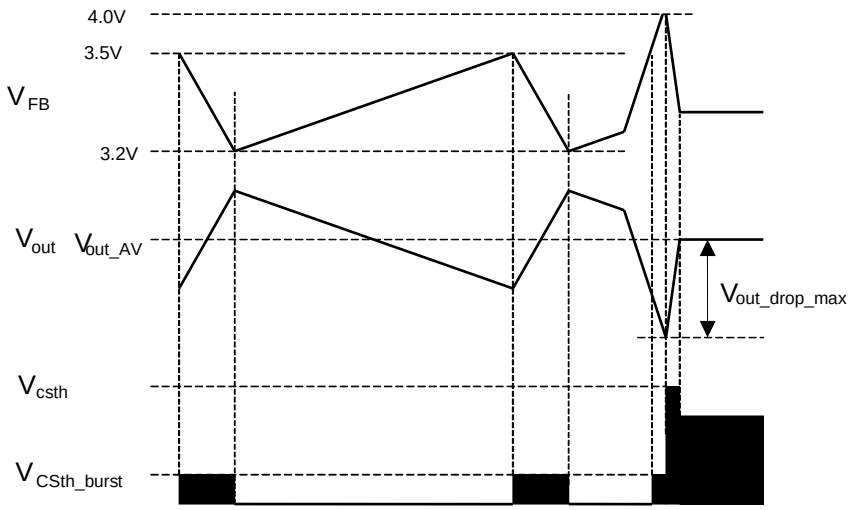


Figure 9 V_{out_drop} during leaving burst mode

The maximum output drop during the transition can be estimated in equation (8).

$$V_{out_drop_max} = \frac{R_{opto}}{R_{fb} \times G_{opto} \times G_{TL431}} \times \left(4 - \frac{3.2 + 3.5}{2}\right) = \frac{0.65 \times R_{opto}}{R_{fb} \times G_{opto} \times G_{TL431}} \quad (8)$$

Figure 10 is the captured waveform when there is a load jump from light load to full load. The output ripple drop during the transition is about 71mV.

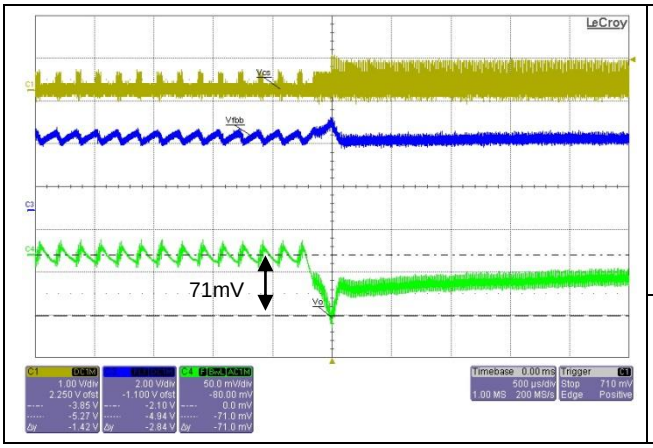
	Channel 1; C1 : Current sense voltage (V_{CS}) Channel 3; C3 : FB voltage (V_{FBB}) Channel 4; C4 : Output ripple voltage (Vo)
	Leaving Active Burst mode when load change from light to full @ Vin=85Vac

Figure 10 Leaving burst mode waveform

6.3.4 Minimum V_{CC} supply voltage during burst mode

It is particularly important that the Vcc voltage must stay above V_{VCCoff} (i.e. 10.5V). Otherwise, the expected low standby power cannot be achieved. The IC will go into auto-restart mode instead. A reference Vcc circuit is presented in Figure 3. This is for a low cost transformer design where the transformer coupling is not too good. Thus the circuit R13 and ZD11 is added to clamp the Vcc voltage exceeding 25.5V in extreme case such as high load and the Vcc OVP protection is triggered. If the transformer coupling is good, this circuit is not needed.

6.3.5 Remarks for the selection of entry/exit burst level

The selection of the entry/exit burst level will depend on the actual application. The below table is the remarks for the selection.

R_{sel}	Remarks
<405kΩ	Lowest entry/exit burst level: good for very small standby load. It needs to take care CS pin noise to be as small as possible as it would have a chance of unstable burst mode (rapid entry and exit burst mode). In case of unstable, it is better to add noise filtering capacitor (e.g., 100nF ceramic cap) in between CS (pin 3) and Gnd (pin 8). However, adding filtering cap would increase maximum overload power and widen the burst mode entry and exit power. Besides, it can also be improved by reducing the loop gain by increasing the opto-coupler biasing resistor, R22. However, if the gain is too low, it would result in higher output ripple.
685kΩ<900kΩ	2nd highest entry/exit burst level: good for general application. It needs to take care CS pin noise to be as small as possible as it would have a chance of unstable burst mode (rapid entry and exit burst mode). In case of unstable, it is better to add noise filtering capacitor (e.g., 100nF ceramic cap) in between CS (pin 3) and Gnd (pin 8). However, adding filtering cap would increase maximum overload power and widen the burst mode entry and exit power. Besides, it can also be improved by reducing the loop gain by increasing the opto-coupler biasing resistor, R22. However, if the gain is too low, it would result in higher output ripple.
>1530kΩ	Highest entry/exit burst level: highest burst power, good for larger standby load. It needs to take care of not having too high loop gain as it would have a chance of unstable burst mode (rapid entry and exit burst mode). In case of unstable, the easiest way is to reduce the loop gain by increasing the opto-coupler biasing resistor, R22. However, too low loop gain would result to higher output ripple.

6.4 Low EMI noise

6.4.1 Frequency jittering

The IC is running at a fixed frequency of 100kHz with jittering frequency at +/-4% in a switching modulation period of 4ms. This kind of frequency modulation can effectively help to obtain a low EMI noise level particularly for conducted EMI. The jittering frequency measured for ICE3AR10080CJZ is 96 KHz ~ 104 KHz (refer to Figure 11).

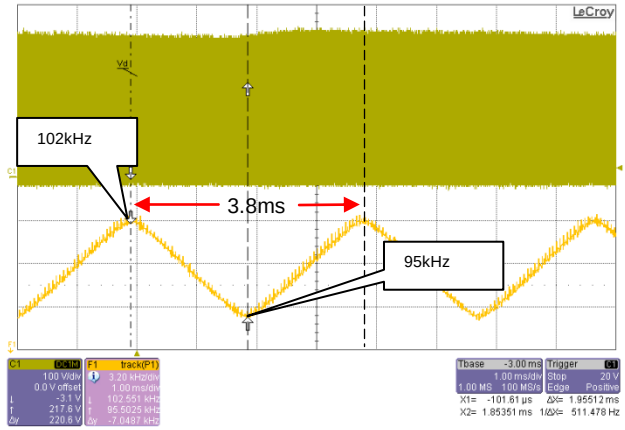
	Channel 1; C1 : Drain voltage (V_D)
	Frequency jittering from 95 kHz ~ 102 kHz,
	Frequency jittering @ 85Vac and max. load

Figure 11 Switching frequency jittering

6.4.2 Soft gate drive and gate turn on resistor

The gate soft driving is to split the gate driving slope into two, so that the CoolMOS® turns on speed is relatively slower comparing to a single slope drive (see Figure 12). Besides soft gate drive, it is also implemented with 50Ω gate turn on resistor. In this way, the high ΔI/Δt noise is greatly reduced and the noise signal reflected in the EMI spectrum is also reduced.

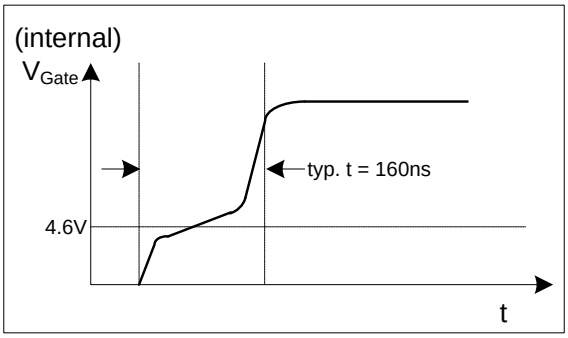


Figure 12 Soft gate drive waveform

6.4.3 Other suggestions to solve EMI issue

Some more suggestions to improve the EMI performance are listed below.

1. Add RCD clamper circuit to the primary winding of the transformer: RCD clamper circuit (D11, R11 & C15) can absorb the current due to leakage inductance of transformer during switch off time of the MOSFET, so voltage spike of the drain can clamp to desired voltage level and suppress the EMI noise (refer to Figure 3).
2. Add capacitor (C_{DS}) at the drain source pin: C_{DS} (C110) can slow down the turn off speed of the MOSFET and the high ΔV/Δt noise will be reduced and so is the EMI noise. The drawback is more energy will be dissipated due to slower turn off speed of MOSFET (refer to Figure 3).
3. Add snubber circuit to the output rectifier: Most of the radiated EMI noise comes out from the output of the system especially for a system with output cable. Adding snubber circuit (R21 and C21) to the output rectifier is a more direct way to suppress those EMI noise (refer to Figure 3).

4. Reduce the reflection voltage: if the secondary to primary reflection voltage is reduced, the switching voltage at drain can also be reduced. Hence the voltage switching noise is reduced and so is the EMI noise. The drawback is the reverse voltage of the secondary rectifier will increase.

6.5 Tight control in maximum power – (Combined OPP curve considering propagation delay & slope compensation)

The maximum power of the system is changed with the different AC line input voltage, the higher the input AC line voltage, the higher the maximum power and vice versa. This is due to the propagation delay of the IC for DCM converters and the propagation delay plus CCM characteristic for CCM converters. In this ICE3ARxx80CJZ, two different types of compensation have implemented to reduce maximum power difference between low and high line. One is for switch on time lower than 4µs (DCM) and the other one is for switch on time higher than 4µs (CCM). The propagation delay compensation is realized by means of a dynamic threshold voltage. In case of a steeper slope, the switch off time of the driver is earlier to compensate the delay.

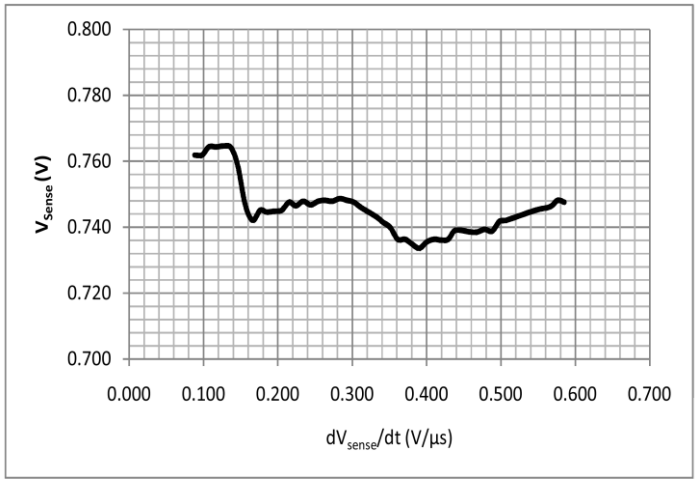


Figure 13 Propagation delay compensation curve

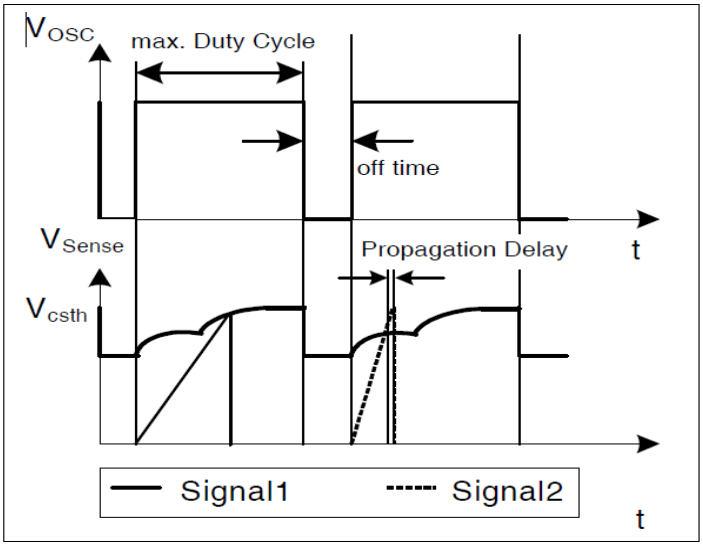


Figure 14 Dynamic voltage threshold

6.6 Protection Features

Protection is one of the major factors to determine whether the system is safe and robust. Therefore sufficient protection is necessary. ICE3ARxx80CJZ provides two kinds of protection mode; odd skip auto restart mode and non switch auto restart mode. A list of protections and the failure conditions are shown in the following table.

Protection function	Failure condition	Protection Mode
V_{CC} over voltage	V_{CC} > 25.5V & last for 120µs	Odd skip auto restart
Over load	V_{FBB} > 4.5V & 40ms blanking time	Odd skip auto restart
Open loop	Same as over load	Odd skip auto restart
V_{CC} under voltage	V_{CC} < 10.5V	Normal auto restart
Short opto-coupler	-> V_{CC} under voltage	Normal auto restart
Over temperature (controller junction)	T_J > 130°C (recovered with 50°C hysteresis)	Non switch Auto restart
External protection enable	V_{BRL} < 0.4V & last for 210 µs	Latch

6.6.1 Odd skip auto restart protection mode

When the failure condition meets the odd skip auto restart protection mode, the IC will enter into odd skip auto restart. The switching pulse will stop. Then the Vcc voltage will drop. When the Vcc voltage drops to 10.5V, the startup cell will turn on again. The Vcc voltage is then charged up until 17V. Unlike auto restart mode, there is no detect of fault and no switching pulse for the first (odd number) restart cycle. At the second (even number) of restart cycle, the fault detects and soft start switching pulses maintained. If the fault persists, it would continue the auto-restart mode. However, if the fault is removed, it can release to normal operation only at the even number auto restart cycle.

The main purpose of the odd skip auto restart is to extend the restart time such that the power loss during auto restart protection can be reduced. This feature can allow adopting smaller V_{CC} capacitor where the restart time is shorter.

Figure 15 shows the odd skip auto restart switching waveform of the V_{CC} and V_{CS}. No detect of fault and no switching pulse for the first and odd restart cycle and there are fault detect and soft start switching pulses at the second and even restart cycle.

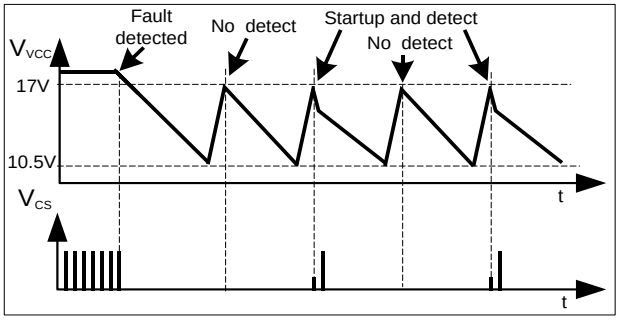


Figure 15 Odd skip auto restart mode

6.6.2 Non switch auto restart mode

Non switch auto restart mode is similar to odd skip auto restart mode except the start up switching pulses are also suppressed at the even number of the restart cycle. The detection of fault still remains at the even number of the restart cycle. When the fault is removed, the IC will resume to normal operation at the even number of the restart cycle (Figure 16).

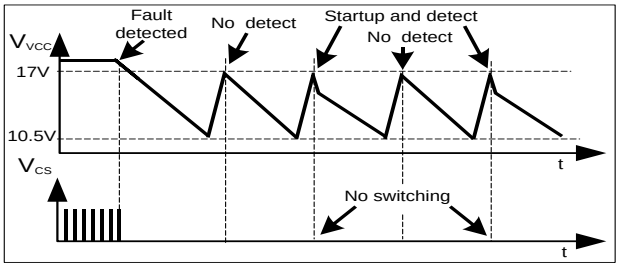
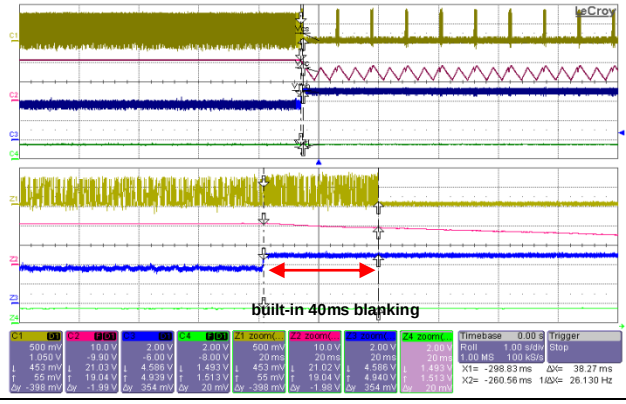


Figure 16 Non switch auto restart mode

6.6.3 Blanking Time for over load protection

The IC controller provides a blanking window before entering into the odd skip auto restart mode due to output overload/short circuit. The purpose is to ensure that the system will not enter protection mode unintentionally. The built-in blanking time is set at 40ms.



Channel 1; C1 : Current sense voltage (V_{CS})
Channel 2; C2 : Supply voltage (V_{CC})
Channel 3; C3 : Feedback voltage (V_{FBB})
Channel 4; C4 : BRL voltage (V_{BRL})

Blanking time =38.27ms

Over load protection with built-in blanking time @ 85Vac

Figure 17 blanking window for over load protection

6.6.4 Brownout Mode

When the AC line input voltage is lower than the designed voltage range, brownout mode is detected by sensing the voltage level at BRL pin through the voltage divider resistors from the separate AC hold up circuit (to get the stabilize voltage at BRL pin, brownout sense voltage should not take from bulk capacitor directly as the ripple voltage of bulk capacitor is big and varied with load). Once the voltage level at BRL pin falls below 1V for 270µs, the controller stops switching and enters into brownout mode. It is until the input AC level goes up to the designed voltage range, BRL voltage is higher than 1.25V and the Vcc hits 17V, the brownout mode is released. Unlike DCM CoolSET® ICE3xRXX80JZ, which sense the voltage and charging current for hysteresis, this CCM CoolSET® ICE3ARXX80CJZ only sense the voltage level. As a result, the brownout resistors can be in bigger resistance and hence lower the standby power especially in high line. Note that there is no MOSFET switching but it always detect brownout level in every restart cycle during brownout mode (Figure 18).

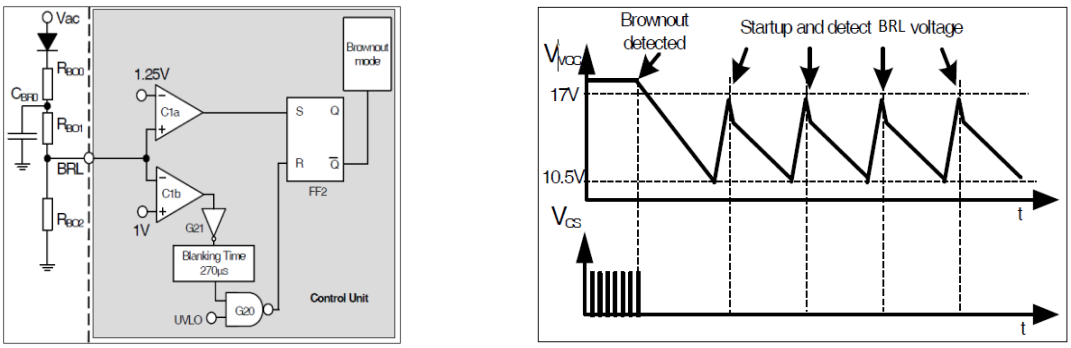


Figure 18 Brownout detection circuit and the waveform

Brownout sensing resistor R_{BO1} can be fixed to 9MΩ and R_{BO2} can be calculated as below.

$$R_{BO2} \geq \frac{\frac{V_{BO_L_max}}{V_{BO_L_DC}} \times R_{BO1}}{1 - \frac{V_{BO_L_max}}{V_{BO_L_DC}}} \quad (9)$$

where $V_{BO_L_max}$ = 1.36V (leave/reset brownout): brownout reference voltage for comparator C1a
$V_{BO_E_max}$ = 1.09V (enter/detect brownout): brownout reference voltage for comparator C1b
$V_{BO_L_DC}$: input DC voltage to leave/reset brownout (high point)
$V_{BO_E_DC}$: input DC voltage to enter/detect brownout (low point)
R_{BO1} and R_{BO2} : Brownout resistors divider from input voltage to BRL pin

For example, if brownout leave/reset voltage is 85Vac and assuming there is no ripple voltage at hold up capacitor, C14 (refer to Figure.3).

$$V_{BO_L_DC} = 85 \times \sqrt{2} = 120Vdc$$

$$R_{BO2} \geq \frac{\frac{1.36}{120} \times 9 \times 10^6}{1 - \frac{1.36}{120}} = 103k\Omega \qquad (\text{choose } R_{BO2} = 105k\Omega)$$

By using the above brownout resistors R_{BO1}=9MΩ & R_{BO2}=105kΩ, brownout enter/detect voltage can be calculated as below.

$$V_{BO_E_DC} = \frac{V_{BO_E_max}}{\frac{R_{BO2}}{R_{BO2} + R_{BO1}}} = \frac{1.09}{\frac{105 \times 10^3}{105 \times 10^3 + 9 \times 10^6}} = 94.51V \quad (10)$$

So, enter/detect brownout AC voltage is $\frac{94.51}{\sqrt{2}} = 66.83\,Vac$

Note: minimum current at R_{BO1} should be higher than 10 times of BRL pin leakage current (0.5μA) to avoid malfunction. For example, R_{BO1} =9MΩ, R_{BO2} =105kΩ, minimum current through R_{BO1}

$$I_{RBO1} = \frac{V_{BO_E_DC}}{R_{BO1} + R_{BO2}} = \frac{94.51}{105 \times 10^3 + 9 \times 10^6} = 10.38\mu A,$$

which is 20 times higher than leakage current at BRL pin.

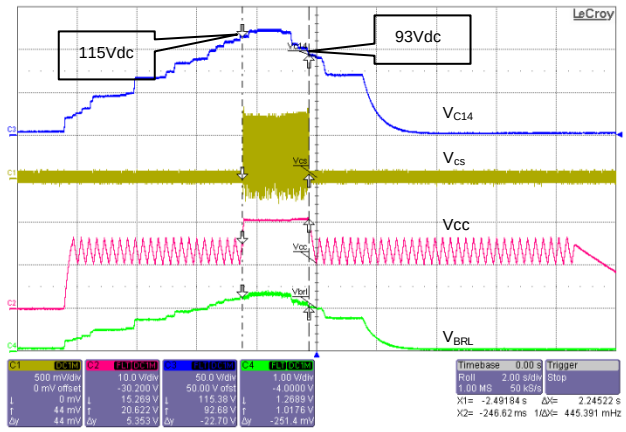
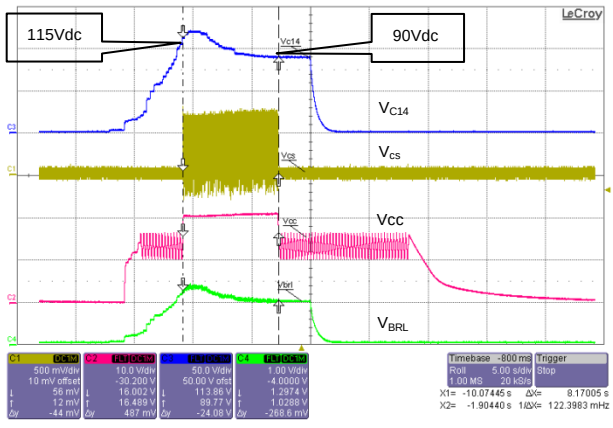
<table>
<tr>
<td>
</td>
<td>
</td>
</tr>
<tr>
<td>Brownout reset: V_{C14}= 115Vdc (82Vac), V_{BRL}=1.26V
Brownout detect: V_{C14}= 93Vdc (66Vac), V_{BRL}=1V</td>
<td>Brownout reset: V_{bulk}= 115Vdc (82Vac),V_{BRL}=1.26V
Brownout detect: V_{bulk}= 90Vdc (65Vac), V_{BRL}=1V</td>
</tr>
<tr>
<td>Brownout mode with max. load</td>
<td>Brownout mode with no load</td>
</tr>
</table>

Figure 19 Brownout mode waveform

If the brownout feature is not needed, it needs to tie the BRL pin to the Vcc pin through a current limiting resistor (R114), 5MΩ~10MΩ. The BRL pin cannot be in floating condition.

Alternatively a lower cost brownout circuit connection can be achieved as shown in Figure 20. The C1 and C2 capacitors can be a low voltage capacitor as the resistor divider R1, R2 and R3 are in high impedance. However, since the IC brownout window is narrow, it needs to have another RC filter R4, R5 and C2 to reduce the ripple voltage. A design example for this design is as below.

Leave brownout voltage = 70Vac, Enter brownout voltage = 55~60Vac
R1=3.9MΩ, R2=1.5MΩ, R3=3MΩ, R4=215kΩ, R5=140kΩ, C1=47nF, C2=1nF

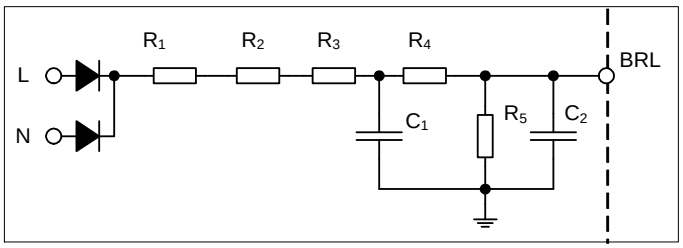


Figure 20 Alternative brownout circuit connection

6.6.5 User defined protection by latch enable (BRL) pin

Although there are lots of pre-defined Auto Restart Protection is implemented in the IC, customer still can have some tailor-made protection for the application needs by pulling down the BRL pin to lower 0.4V for 210µs. When BRL pin is lower than 0.4V, the gate drive switching will be stopped and IC will enter to latch mode.

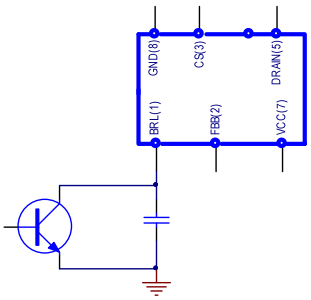


Figure 21 User defined external latch enable circuit

A simply output OVP circuit is shown in Figure 22. The output voltage is sensed by the auxiliary winding. When the pre-set OVP voltage is reached, the zener diode Z1 is triggered and the transistor T1 is on. The BRL pin is pulled down and latched off.

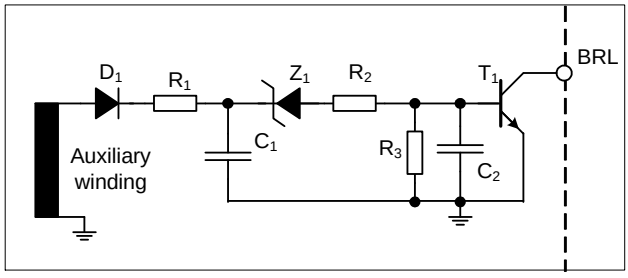


Figure 22 Output OVP circuit by sensing the auxiliary winding

6.6.6 Fast AC reset

During the normal operation, the ICE3ARxx80CJZ can be latched by pulling down the BRL voltage as explained in section 6.6.5 and latch mode can be reset by the AC recycle. For the ordinary AC recycle, switch of the main AC power until the Vcc voltage below 8V and it will take quite a long time depending on the size of Vcc capacitor. To avoid this longer time to reset latch, “Fast AC reset” feature is implemented in the ICE3ARxx80CJZ, by sensing the BRL voltage rise time from 0.4V to 1V for at least 450µs after IC enter latch mode.

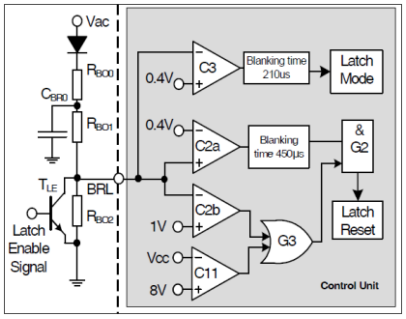


Figure 23 Latch and fast AC reset

Case a : not latched (solid line); the timing below 0.4V is 150µs and is less than 210µs.

Case b : latched (dashed line); the timing below 0.4V is 450µs which is larger than 210µs. No latch reset as the rise time from 0.4V to 1V is 300µs which is less than the 450µs.
Case c : latched and reset (dotted line); the timing below 0.4V is 710µs which is larger than 210µs. But the rise time from 0.4V to 1V is 560µs which is larger than the latch reset blanking time of 450µs.

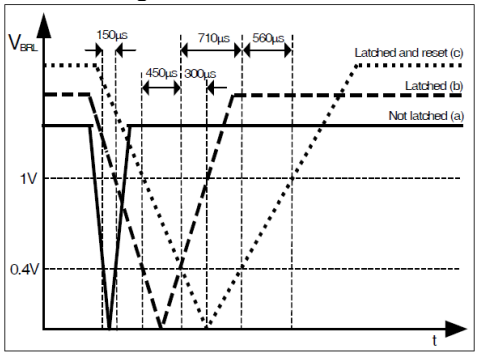


Figure 24 Latch and fast AC reset example

Pre-caution: During the lightning surge test if the lightning surge noise is too much and strong, the latch protection voltage at BRL pin may mis-triggered and the system may enter into protection mode. To avoid this risk, R17 and C19 (refer to figure 3) can be selected to reduce the risk. In general, the design can be as below.

The bigger the C19 capacitance, the longer the V_{BRL} dip and it may enter to protection mode (recommended value for C19=100pF~1nF).

The smaller the R17 resistance, the bigger the negative spike and it may malfunction the controller. On the other hand, the R17 resistance cannot be too large as it may couple the noise easily and the brownout/latch function may not work properly in normal operation (recommended value for R17=0Ω~2kΩ).

7 Input power curve

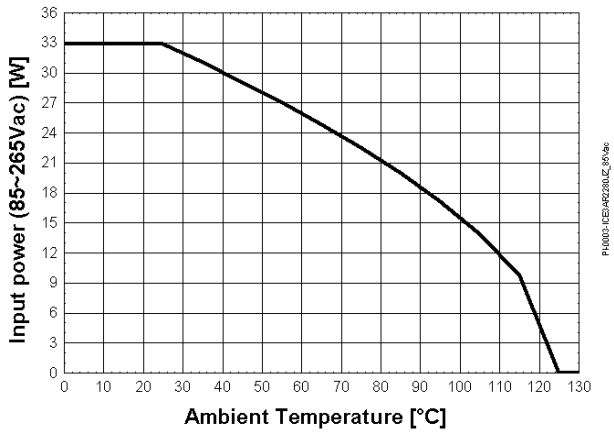
The purpose of the input power curve is to simplify the selection of the CoolSET® device. The curve is a function of ambient temperature to the input power of the system in which the input filter loss, bridge rectifier loss and the MOSFET power loss are considered. The only information needed is the required output power, the input voltage range, the operating ambient temperature and the efficiency of the system. The required input power can then be calculated as equation (11).

$$P_{in} = \frac{P_o}{\eta} \quad \textbf{(11)}$$

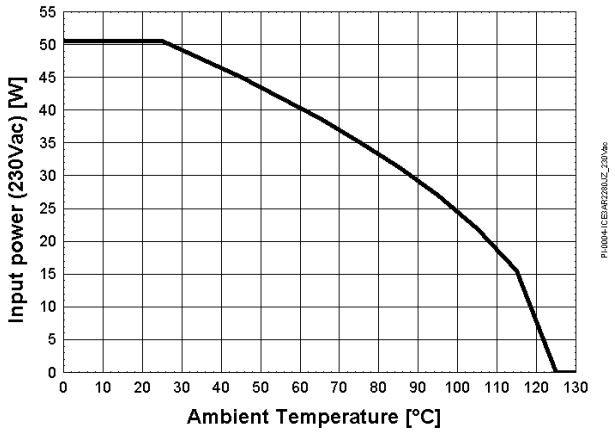
where P_{in} : input power, P_o : output power, η : efficiency

It then simply looks up the closed input power at the required ambient temperature from the input power curve.

The input power curves for the CoolSET-F3R80CCM (DIP-7) family are listed below.

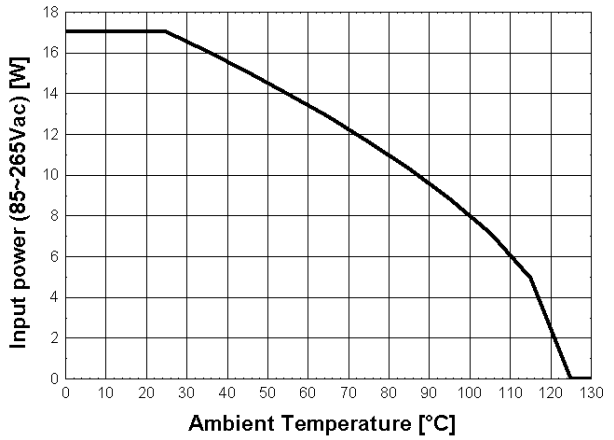


ICE3AR2280CJZ : Vin=85Vac~265Vac

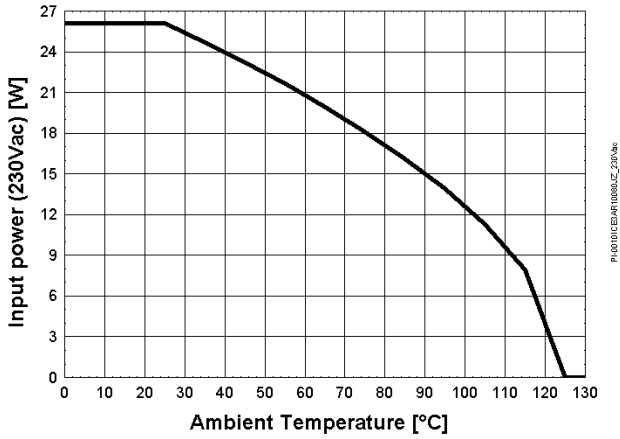


ICE3AR2280CJZ : Vin=230Vac±15%

Figure 25 Input power curve for ICE3AR2280CJZ



ICE3AR10080CJZ : Vin=85Vac~265Vac



ICE3AR10080CJZ : Vin=230Vac±15%

Figure 26 Input power curve for ICE3AR10080CJZ

The major assumption for the calculation is listed below.

1. Reflection voltage from secondary side to primary side is 150V.
2. The assumed maximum power for the device is when the junction temperature of the integrated CoolMOS® reaches 125°C. (With some margins to reach the over temperature protection of the device : 130°C). The maximum R_{dson} of the device at 125°C is taken for calculation.
3. There is no copper area as heat sink and the R_{thja}=96K/W (DIP-7)
4. Saturation current (I_{d_max} @ 125°C) of the MOSFET is considered which is showed in below table.
5. The typical resistance of the EMI filter is listed in the below table.
6. The voltage drop for the bridge rectifier is assumed to be 1V.

	Rdson_125°C (Ω)	I_{d_max} @125°C (A)	R_{EMI_filter} (Ω)	V_{F_bridge} (V)
ICE3AR2280CJZ	5.80	2.87	2 * 2	2 * 1
ICE3AR10080CJZ	24.6	0.675	2 * 3	2 * 1

8 Layout Recommendation

In order to get the optimized ruggedness of the IC to the transient surge events like ESD and lightning Surge test, the grounding of the PCB layout must be connected carefully. From the circuit diagram in Figure 3, it indicates that the grounding for the controller can be split into several groups; signal ground, Vcc ground, Current sense resistor ground and EMI return ground. All the split grounds should be “star” connected to the bulk capacitor ground directly. The split grounds are described as below.

- Signal ground includes all small signal grounds connecting to the controller GND pin such as filter capacitor ground, C17, C18, C19, C111, C115 and opto-coupler ground..
- Vcc ground includes the Vcc capacitor ground, C16 and the auxiliary winding ground, pin 2 of the power transformer.
- Current Sense resistor ground includes current sense resistor R14 and R15.
- EMI return ground includes Y capacitor, C12.

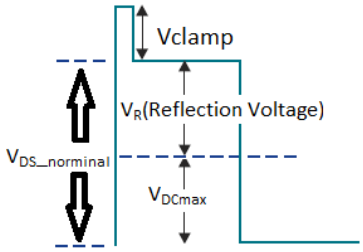
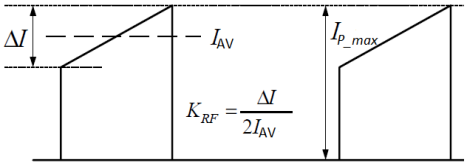
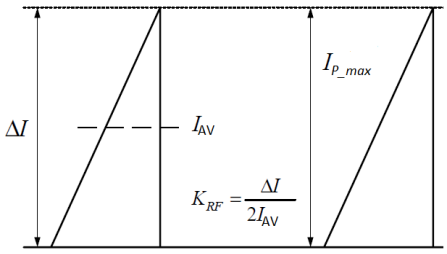
9 Product portfolio of CoolSET® F3R80CCM (DIP-7) brownout & CCM version

Device	Package	V_{DS}	Frequency / kHz	R_{dson} /Ω[1]	230Vac±15%[2]	85-265Vax±15% [2]
ICE3AR10080CJZ	PG-DIP-7	800V	100	10.0	22W	15W
ICE3AR2280CJZ	PG-DIP-7	800V	100	2.26	43W	28W

[1] Typ @ 25°C

[2] Calculated maximum input power rating at T_a=50°C, T_j=125°C and without copper area as heat sink. Refer to the data sheet for input power curve of other T_a

10 Useful formula for the SMPS design

Transformer (CCM flyback)	
Input data	$V_{DC_min} = 92V$, $V_{DC_max} = 400V$, $V_{DS_norminal} = 520V$ for 800V Mosfet (Reflection voltage, $V_R = V_{DS_norminal} - V_{DC_{max}}$) $D_{max} < 0.65$(65%) 
Turn ratio	$N_{ratio} = \frac{V_{DS_norminal} - V_{DC_max}}{V_{out} + V_{FDiode}} = \frac{V_R}{V_{out} + V_{FDiode}}$
Duty maximum	$D_{max} = \frac{V_R}{V_R + V_{DC_min}}$
Primary Inductance	$L_P = \frac{(V_{DC_min} \times D_{max})^2}{2 \times P_{in} \times f_s \times K_{RF}}$ (where, K_{RF} = 0.25~0.5 for universal input range, K_{RF} = 0.4~0.8 for European input range)
Primary peak current	$I_{P_max} = I_{AV} + \frac{\Delta I}{2}$ ($where, I_{AV} = \frac{P_{in}}{V_{DC_min} \times D_{max}}$, $\Delta I = \frac{V_{DC_min} \times D_{max}}{L_P \times f_s}$) $K_{RF} < 1\ for\ CCM$  K_{RF} = 1 for DCM 
Maximum DC voltage for CCM full load	$V_{DC_max_CCM} = (\frac{1}{\sqrt{2 \times P_{in} \times L_P \times f_s}} - \frac{1}{V_R})^{-1}$
Primary rms current	$I_{P_rms} = \sqrt{\left[3(I_{AV})^2 + (\frac{\Delta I}{2})^2\right] \times \frac{D_{max}}{3}}$
Primary turns	$N_P \geq \frac{I_{P_max} \times L_P}{B_{max} \times A_e}$
Secondary turns	$N_S = \frac{N_P}{N_{ratio}}$
Auxiliary turns	$N_{aux} = \frac{V_{cc} + V_{FDiode}}{V_{out} + V_{FDiode}} \times N_S$

ICE3ARxx80CJZ other components	
Current sense resistor	$R_{CS} \leq \frac{V_{csth2_min}}{I_{P_max}}$
Soft start time	$t_{SS} = 10ms$
Vcc capacitor	$C_{VCC} = \frac{I_{VCCsup2_max} \times t_{SS}}{V_{VCChys}} \times \frac{2}{3}$
Startup time	$t_{StartUp} = \frac{V_{VCCon} \times C_{VCC}}{I_{VCCcharge}}$ (where $I_{VCCcharge}$ is the average current of $I_{VCCcharge2}$ and $I_{VCCcharge3}$)
Enter burst mode power	$P_{burst_enter} = \frac{1}{2} \times L_P \times (I_{P_{burst}})^2 \times f_s$ where , $I_{P_burst} = \frac{\frac{V_{FB_burst} - V_{Offset-Ramp}}{A_V}}{(\frac{M_C \times L_P}{V_{DC}}) + R_{CS}}$
Output ripple during burst mode	$V_{out_ripple_pp} = \frac{R_{opto} \times \Delta V_{fb}}{R_{fb} \times G_{opto} \times G_{TL431}}$
Leave burst mode power	$P_{burst_leave} = 0.5 \times L_P \times \left(\frac{V_{csth_burst}}{R_{CS}}\right)^2 \times f_s$
Built-in blanking time for over load protection	$t_{BK} = 40ms$
Brownout resistor , R_{BO1} & R_{BO2}	Choose $R_{BO1} = 9M\Omega$, $R_{BO2} \geq \frac{\frac{V_{BO_L_max}}{V_{BO_L_DC}} \times R_{BO1}}{1 - \frac{V_{BO_L_max}}{V_{BO_L_DC}}}$ Note: minimum current at R_{BO1} should be higher than 10 times of BRL pin leakage current (0.5µA) to avoid malfunction
Input DC voltage to enter brownout mode	$V_{BO_E_DC} = \frac{V_{BO_E_max}}{\frac{R_{BO2}}{R_{BO2} + R_{BO1}}}$

11 Design calculation example

Design calculation for CCM Transformer(5VX2A=10W)

$V_DC_min := 104V$

$V_DC_max := 399V$

$Vout := 5V$

$Iout := 2A$

$Vcc := 15V$

$Bmax := 0.3T$

$Ae := 32.1mm^2$ (From Epcos datasheet, E20/10/6 (N87))

$Pout := Vout \cdot Iout$

$\eta := 0.8$

$Pin := \frac{Pout}{\eta}$ $Pin = 12.5W$

$fs := 100kHz$

$K_RF := 0.5$

$V_DS_norminal := 480V$

$V_F_Diode := 0.6V$

$V_F_Diode_aux := 1V$

$V_R := V_DS_norminal - V_DC_max$ $V_R = 81V$

1.1 Turn ratio(N_{ratio})

$N_ratio := \frac{V_R}{Vout + V_F_Diode}$ $N_ratio = 14.464$

1.2 Maximum duty cycle(D_{max})

$Dmax := \frac{V_R}{V_R + V_DC_min}$ $Dmax = 0.438$ Choose $Dmax := 0.438$

1.3 Primary inductance(L_P)

$Lp := \frac{(V_DC_min \cdot Dmax)^2}{2 \cdot Pin \cdot fs \cdot K_RF}$ $Lp = 1.66 \times 10^{-3} H$ Choose $Lp := 1.6mH$

1.4 Primary current(I_{P_max} ,I_{P_rms})

$$\Delta I := \frac{V_DC_min \cdot Dmax}{Lp \cdot fs} \qquad \Delta I = 0.285\,A$$

$$Iav := \frac{Pin}{V_DC_min \cdot Dmax} \qquad Iav = 0.274\,A$$

$$I_P_max := Iav + \frac{\Delta I}{2} \qquad I_P_max = 0.417\,A$$

$$I_P_rms := \sqrt{\left[3 \cdot Iav^2 + \left(\frac{\Delta I}{2}\right)^2\right] \cdot \frac{Dmax}{3}} \qquad I_P_rms = 0.19\,A$$

1.5 Primary,secondary and auxiliary turns (N_P, N_S and N_{aux})

$$Np := \frac{I_P_max \cdot Lp}{Bmax \cdot Ae} \qquad Np = 69.244$$

$$Ns := \frac{Np}{N_ratio} \qquad Ns = 4.787 \qquad \text{Choose} \quad Ns := 5$$

$$Np := N_ratio \cdot Ns \qquad Np = 72.321 \qquad \text{Choose} \quad Np := 72$$

$$Naux := Ns \cdot \frac{Vcc + V_F_Diode_aux}{Vout + V_F_Diode} \qquad Naux = 14.286 \qquad \text{Choose} \quad Naux := 14$$

1.6 Maximum DC voltage for CCM full load ($V_{DC_max_CCM}$)

$$Vdc_max_CCM := \left(\frac{1}{\sqrt{2Pin \cdot Lp \cdot fs}} - \frac{1}{V_R}\right)^{-1} \qquad Vdc_max_CCM = 288.541\,V$$

Design calculation for other components

2.1 Curent sense resistor (R_{CS})

$$Vcsth2_min := 0.72V$$

$$Rcs := \frac{Vcsth2_min}{I_P_max} \qquad Rcs = 1.728\,\Omega \qquad \text{Choose lower value} \quad Rcs := 1.7\Omega$$

2.2 Vcc capacitor (C_{Vcc})

$Ivccsup2_max := 4.8mA$

$tss := 10ms$

$Vvcchys := 6.5V$

$Cvcc := \frac{Ivccsup2_max \cdot tss \cdot 2}{Vvcchys \cdot 3}$ $Cvcc = 4.923 \times 10^{-6} F$ (Choose higher value, Cvcc=10µF)

2.3 Startup time ($t_{StartUp}$)

$Vvccon := 17V$

$Cvcc := 10\mu F$

$Ivcccharge2 := 1mA$

$Ivcccharge3 := 0.75mA$

$Ivcccharge := \frac{(Ivcccharge2 + Ivcccharge3)}{2}$ $Ivcccharge = 8.75 \times 10^{-4} A$

$t_startup := \frac{Cvcc \cdot Vvccon}{Ivcccharge}$ $t_startup = 0.194 s$

2.4 Enter burst mode power (P_{burst_enter})

$Vfb_burst := 1.61V$ (choose according the the user design, V_{FB_burst1} / V_{FB_burst2} / V_{FB_burst3})

$Voffset_ramp := 0.6V$

$Av := 3.25$

$Mc := 50\frac{mV}{\mu s}$

$Lp = 1.6 \times 10^{-3} H$

$Vdc := 120V$

$$Ip_burst := \frac{\frac{Vfb_burst - Voffset_ramp}{Av}}{\left(\frac{Mc \cdot Lp}{Vdc}\right) + Rcs}$$

$Pburst_enter := \frac{1}{2} \cdot Lp \cdot Ip_burst^2 \cdot fs$ $Pburst_enter = 1.379 W$

2.5 Leave burst mode power (P_{burst_leave})

Vcsth_burst := 0.2 (choose according the the user design, V_{CSth_burst1} / V_{CSth_burst2} / V_{CSth_burst3})

$$\mathbf{Pburst_leave} := \frac{1}{2}\cdot\mathbf{Lp}\cdot\left(\frac{\mathbf{Vcsth_burst}}{\mathbf{Rcs}}\right)^2\cdot\mathbf{fs} \qquad \mathbf{Pburst_leave} = 2.328\,\mathbf{W}$$

2.6 Brownout resistor (R_{BO1} & R_{BO2})

Choose **Rbo1** := 9MΩ

Vbo_L_max := 1.36 <(leave/reset brownout):brownout reference voltage for comparator C1a>

Vbo_L_DC := 120V <input DC voltage to leave/reset brownout(high point)>

$$\mathbf{Rbo2} := \frac{\frac{\mathbf{Vbo_L_max}}{\mathbf{Vbo_L_DC}}\cdot\mathbf{Rbo1}}{1-\frac{\mathbf{Vbo_L_max}}{\mathbf{Vbo_L_DC}}} \qquad \mathbf{Rbo2} = 1.032\times10^{5}\,\Omega \quad \text{(choose higher vlaue)} \qquad \mathbf{Rbo2} := 105\text{k}\Omega$$

Input DC voltage to enter/detect brownout mode(low point) ($V_{BO_E_DC}$)

Vbo_E_max := 1.09V <(enter/detect brownout):brownout reference voltage for comparator C1b>

$$\mathbf{Vbo_E_DC} := \frac{\mathbf{Vbo_E_max}}{\frac{\mathbf{Rbo2}}{\mathbf{Rbo2}+\mathbf{Rbo1}}} \qquad \mathbf{Vbo_E_DC} = 94.519\,\mathbf{V}$$

12 References

[1] Infineon Technologies, Datasheet “CoolSET®-F3R80 ICE3AR2280CJZ Off-Line SMPS Current Mode Controller with Integrated 800V CoolMOS® and Startup Cell (Brownout & CCM) in DIP-7”

[2] Infineon Technologies, Datasheet “CoolSET®-F3R80 ICE3AR10080CJZ Off-Line SMPS Current Mode Controller with Integrated 800V CoolMOS® and Startup Cell (Brownout & CCM) in DIP-7”

[3] Kyaw Zin Min, Kok Siu Kam Eric, Infineon Technologies, Application Note “AN-EVAL3AR2280CJZ, 20W 5V SMPS Evaluation Board with CoolSET®-F3R80CCM ICE3AR2280CJZ”

[4] Kyaw Zin Min, Kok Siu Kam Eric, Infineon Technologies, Application Note “AN-EVALICE3AR10080CJZ, 10W 5V SMPS Evaluation Board with CoolSET®-F3R80CCM ICE3AR10080CJZ”

13 Appendix 1 – reference circuit to solve output OVP by external voltage short

If there is a high external output voltage shorted to the 5V output, the circuit in Figure 3 cannot react for the OVP protection. Additional circuit is needed to achieve the protection.

1. D22 and C28 : additional power to sustain the Vo OVP ckt as the switching will stop.
2. Q12, Q13, R117, R118, R119 and C113 : additional circuit to open the control loop and leave the active burst mode to normal load if the OVP happened at light load (burst mode).

