CoolSET™ F3R80 Family
ICE3xRxx80JZ/VJZ

ICE3xRxx80JZ/VJZ Design Guide
AN-PS0044

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Major changes since previous revision			
Date	**Version**	**Changed By**	**Change Description**
9 Sep 2013	1.5	Kyaw Zin Min	Add input OVP version CoolSET F3R80 ICE3xRxx80VJZ

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1 Introduction

The CoolSET™-F3R80, **ICE3xRxx80JZ/VJZ** is the latest development of the CoolSET™. It is a PWM controller with power MOSFET and startup cell in a DIP-7 package. The switching frequency is running at 65/100 kHz and it targets for DVD player, set-top box, portable game console, white goods, auxiliary power supply for server/PC, etc.

The **ICE3xRxx80JZ/VJZ** adopts the 800V avalanche rugged CoolMOS™ power switch and the BiCMOS technology to provide a wider Vcc operating range up to 25V. It inherits the proven good features of CoolSET™ F3R such as Active Burst Mode, propagation delay compensation, soft gate drive, auto restart protection for major faults (Vcc over voltage, Vcc under voltage, over temperature, over-load, open loop and short opto-coupler), it also has selectable entry and exit burst mode level, brownout feature/input OVP, built-in soft start time, built-in and extendable blanking time, frequency jitter feature and external auto-restart enable, etc. The particular features are the best-in-class low standby power with selectable burst mode power level and the good EMI performance.

2 List of Features

800V avalanche rugged CoolMOS™ with Startup Cell
Active Burst Mode for lowest Standby Power
Selectable entry and exit burst mode level
65/100kHz internally fixed switching frequency with jittering feature
Auto Restart Protection for Over load, Open Loop, VCC Under voltage & Over voltage and Over temperature
External auto-restart enable pin (only for ICE3xRxx80JZ)
Over temperature protection with 50°C hysteresis
Built-in 10ms Soft Start
Built-in 20ms and extendable blanking time for short duration peak power
Propagation delay compensation for both maximum load and burst mode
Adjustable brownout (only for ICE3xRxx80JZ)
Input OVP (only for ICE3xRxx80VJZ)
Overall tolerance of Current Limiting < ±5%
BiCMOS technology for low power consumption and wide VCC voltage range
Soft gate drive with 50Ω turn on resistor

3 Package

The package for F3R80 ICE3xRxx80JZ brownout and frequency jitter mode product is DIP-7.

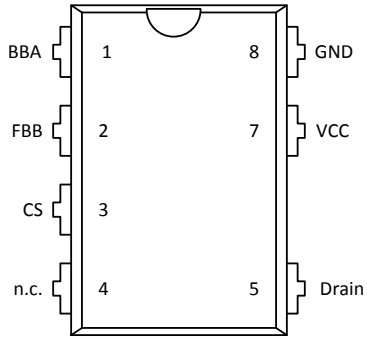


Figure 1 ICE3xRxx80JZ Pin configuration

Pin	Name	Description
1	**BBA**	Brownout, extended Blanking time & Auto-restart enable
2	**FBB**	Feedback & Burst entry/exit control
3	**CS**	Current Sense/800V CoolMOS™ Source
4	n.c	not connected
5	**Drain**	800V CoolMOS™ Drain
6	-	(no pin)
7	**VCC**	Controller Supply Voltage
8	**GND**	Controller Ground

The package for F3R80 ICE3xRxx80VJZ input OVP and frequency jitter mode product is DIP-7.

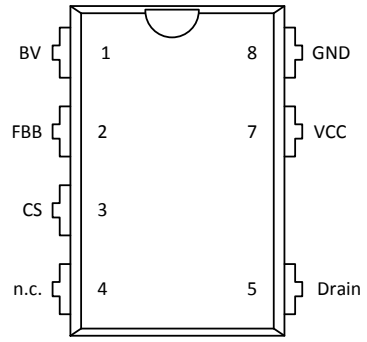


Figure 2 ICE3xRxx80VJZ Pin configuration

Pin	Name	Description
1	**BV**	extended Blanking time & input OVP
2	**FBB**	Feedback & Burst entry/exit control
3	**CS**	Current Sense/800V CoolMOS™ Source
4	n.c	not connected
5	**Drain**	800V CoolMOS™ Drain
6	-	(no pin)
7	**VCC**	Controller Supply Voltage
8	**GND**	Controller Ground

4 Block Diagram

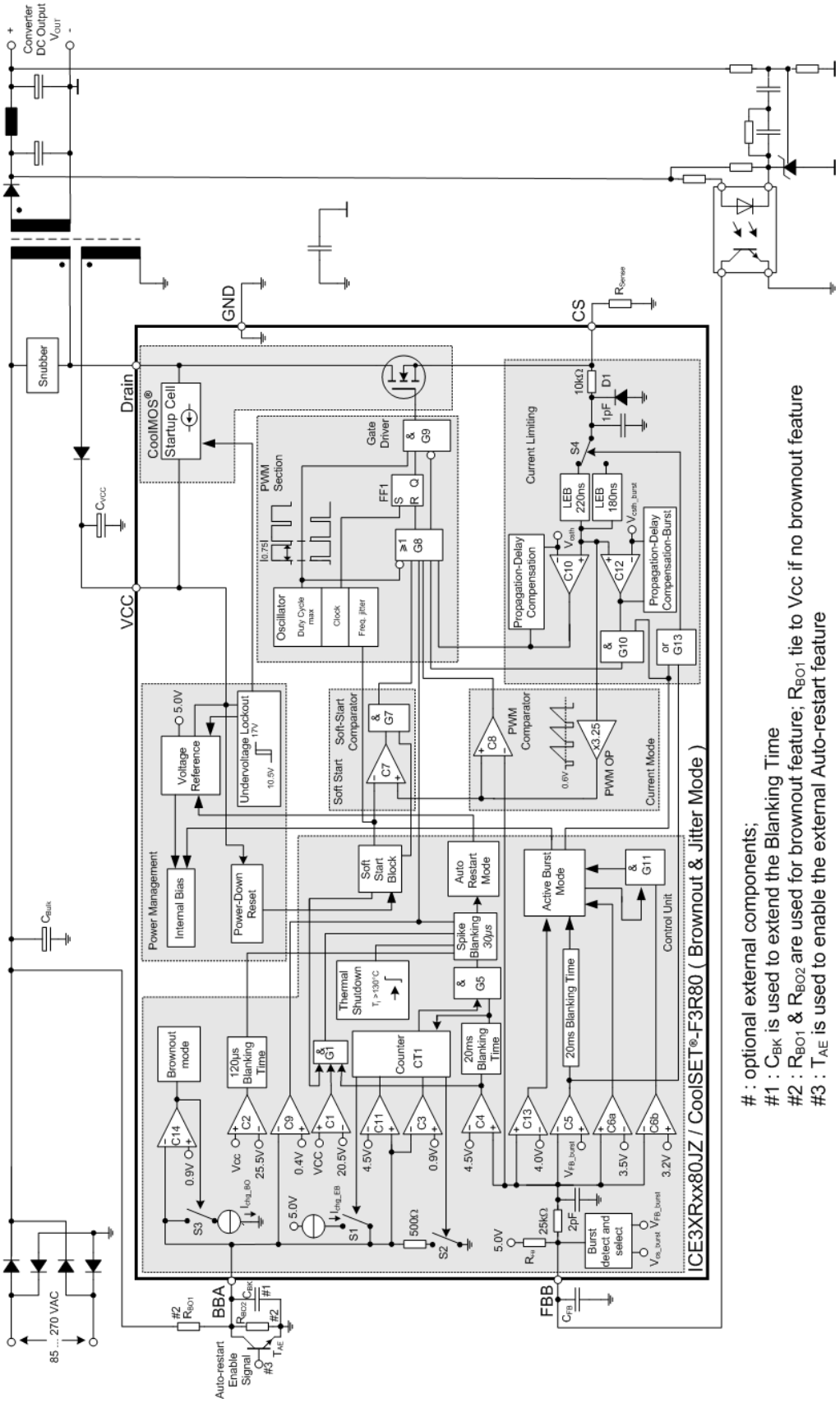


Figure 3 Block diagram of ICE3xRxx80JZ

Block Diagram

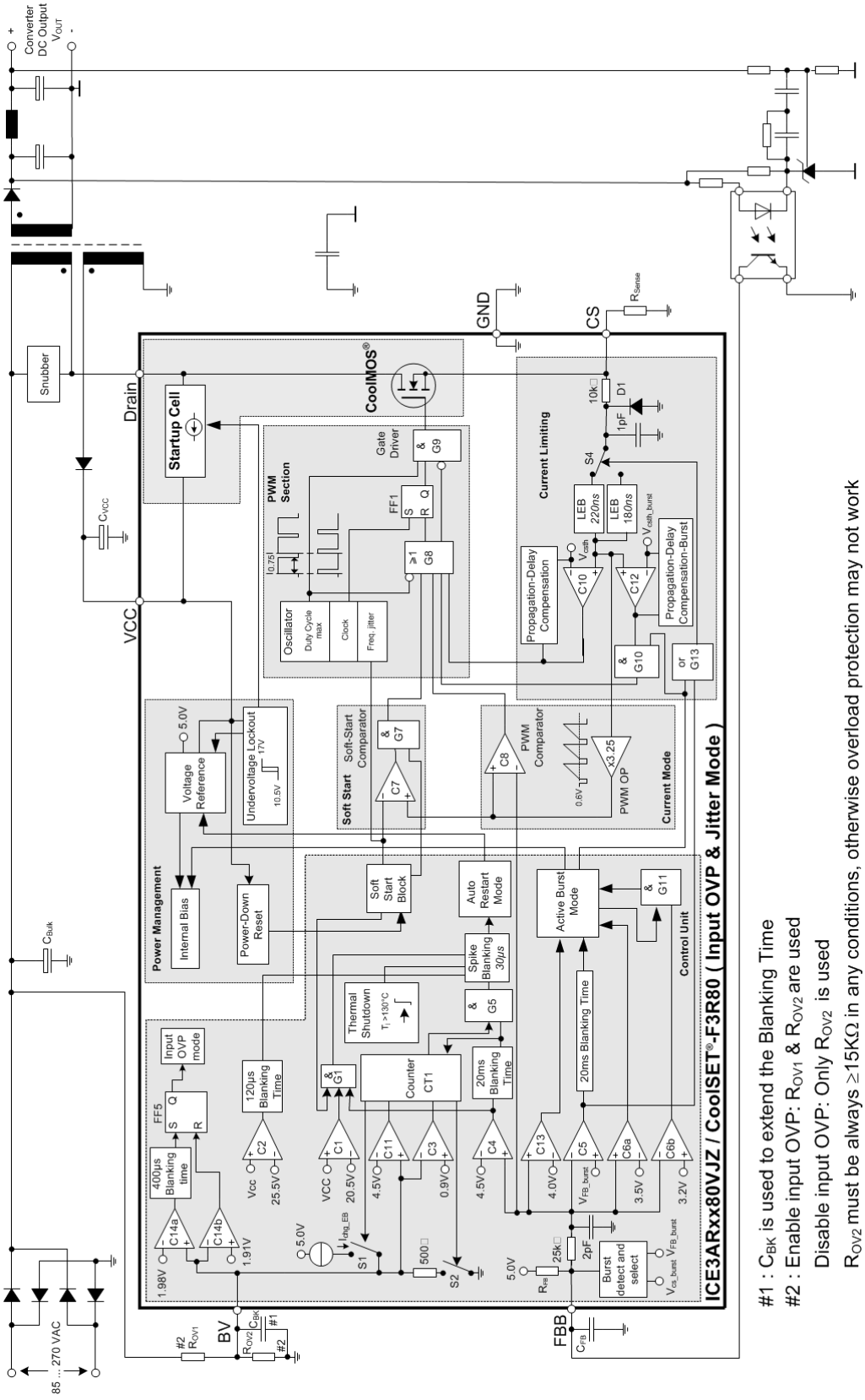


Figure 4 Block diagram of ICE3xRxx80VJZ

5 Typical Application Circuit

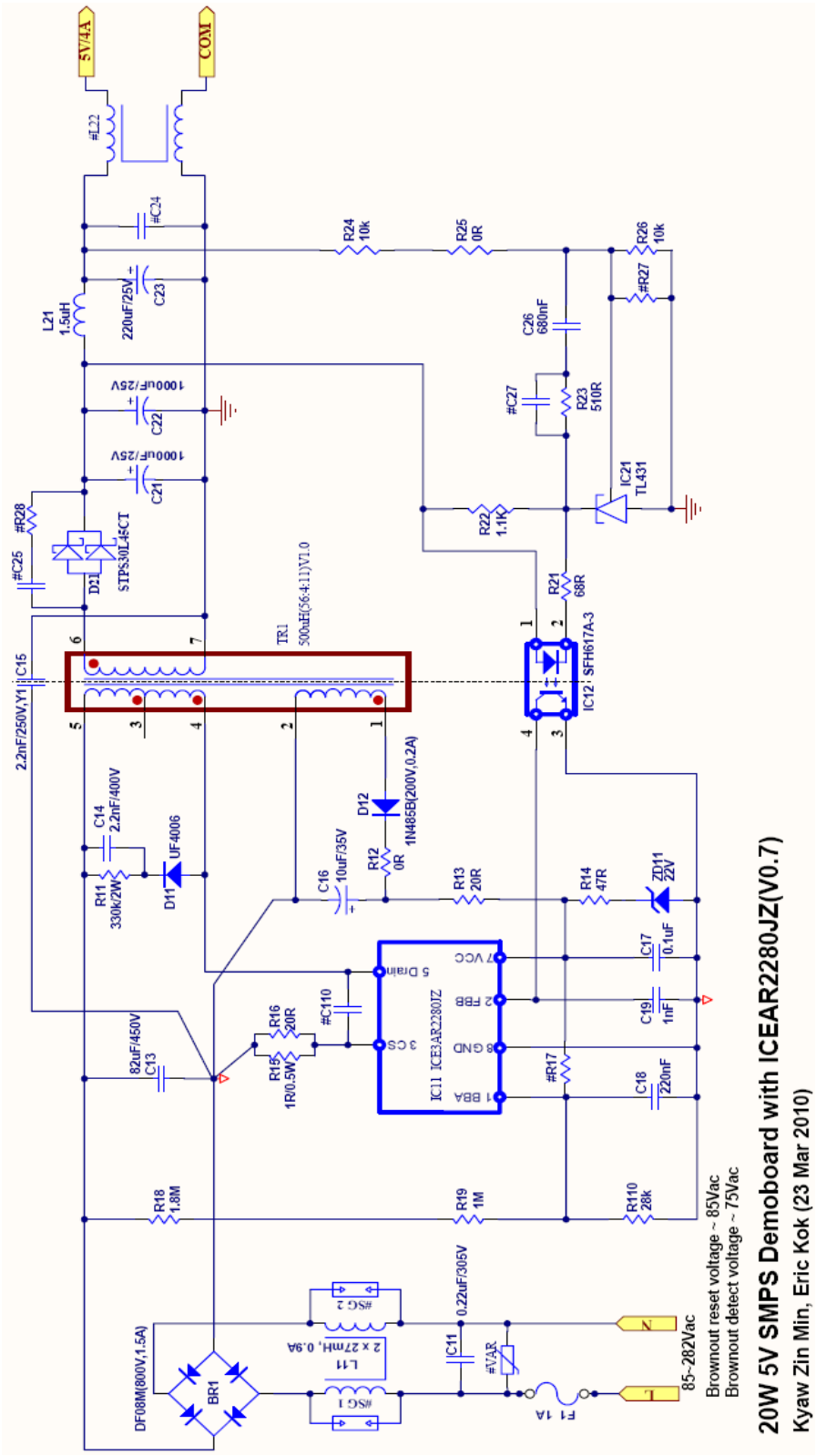


Figure 5 Typical application circuit with ICE3AR2280JZ 20W 5V

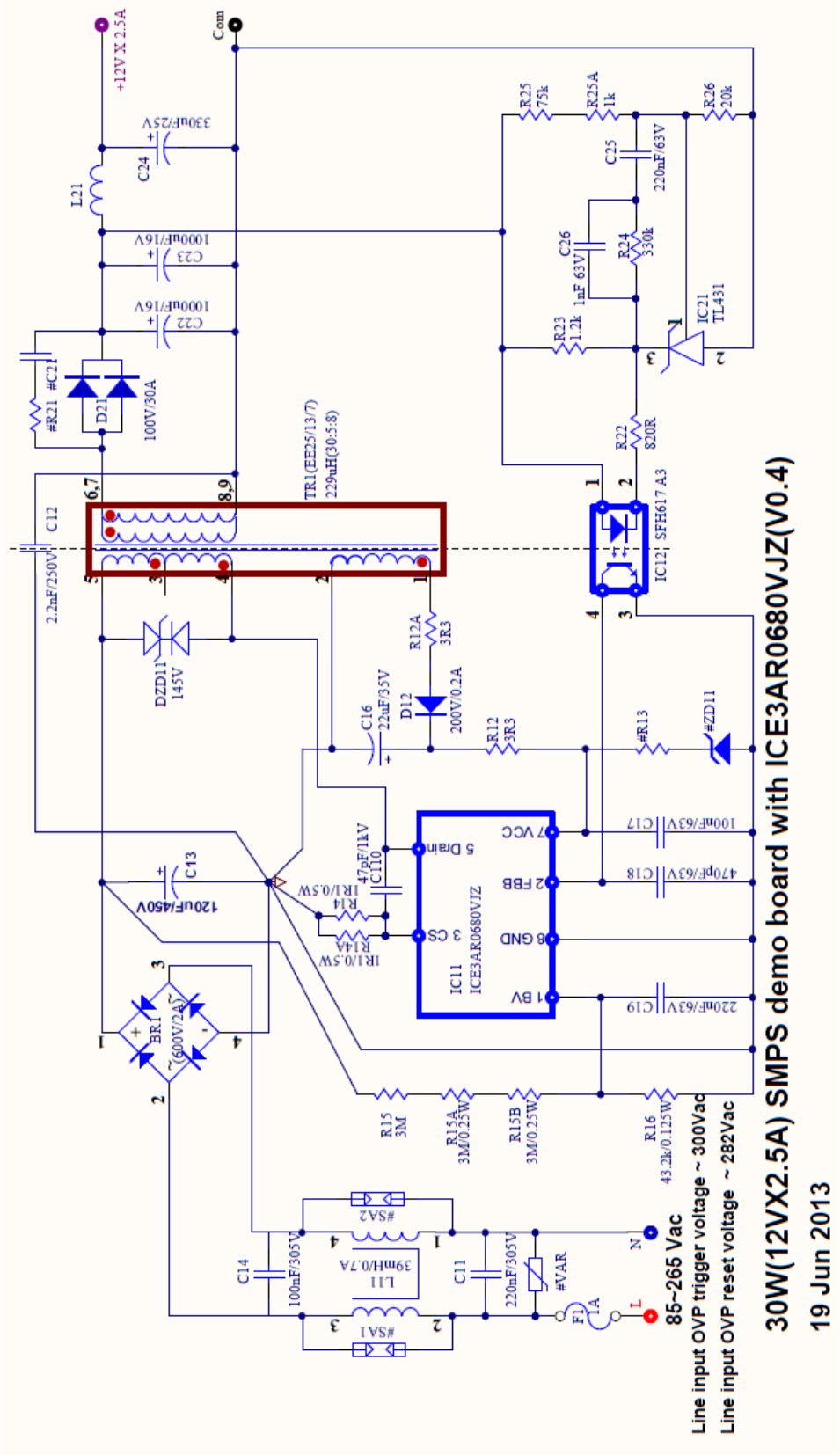


Figure 6 Typical application circuit with ICE3AR0680VJZ 30W 12V

6 Functional description and component design

6.1 Startup time

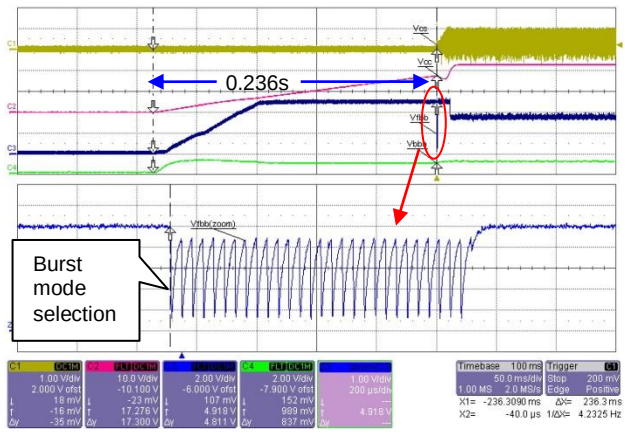
Startup time is counted from applying input voltage to IC turn on. ICE3xRxx80JZ/VJZ has a startup cell which is connected to input bulk capacitor. When there is input voltage, the startup cell will act as a constant current source to charge up the Vcc capacitor and supply energy to the IC. When the Vcc capacitor reaches the Vcc_on threshold 17V, the IC turns on. Then the startup cell is turned off and the Vcc is supplied by the auxiliary winding. Start up time is independent from the AC line input voltage and it can be calculated by the equation (1). Figure 7 shows the start up time of 85Vac line input.

$$t_{STARTUP} = \frac{V_{VCCon} \cdot C_{VCC}}{I_{VCCCharge}} \quad (1)$$

where, $I_{VCCCharge}$: average of Vcc charge current of $I_{VCCCharge2}$ and $I_{VCCCharge3}$ (0.8mA),

V_{VCCon} : IC turns on threshold (17V), C_{VCC} : Vcc capacitor

Please refer to the datasheet for the symbol used in the equation.



Channel 1; C1 : Current sense voltage (V_{CS})
Channel 2; C2 : Supply voltage (VCC)
Channel 3; C3 : Feedback voltage (V_{FBB})
Channel 4; C4 : BBA voltage (V_{BBA})

Measured startup time = 0.23s

Startup @ 85Vac & max. load

Figure 7 The startup delay time at AC line input voltage of 85Vac

Precaution : For a typical application, start up should be Vcc ramps up first, other pin (such as FB pin) voltage will follow Vcc voltage to ramp up. It is recommended not to have any voltage on other pins (such as FBB; BBA and CS) before Vcc ramps up.
In addition, the dummy load in the Vcc pin should be larger than 150kΩ. Otherwise, it would has a risk of delay startup.

6.1.1 Vcc capacitor

The minimum value of the Vcc capacitor is determined by voltage drop during the soft start time. The formula is expressed in equation (2).

$$C_{VCC} = \frac{I_{VCCsup2} \cdot t_{ss}}{V_{CCHY}} \cdot \frac{2}{3} \quad (2)$$

where, $I_{VCCsup2}$: IC consumption current (4.8mA for ICE3AR2280JZ), t_{ss} : soft start time (10ms),

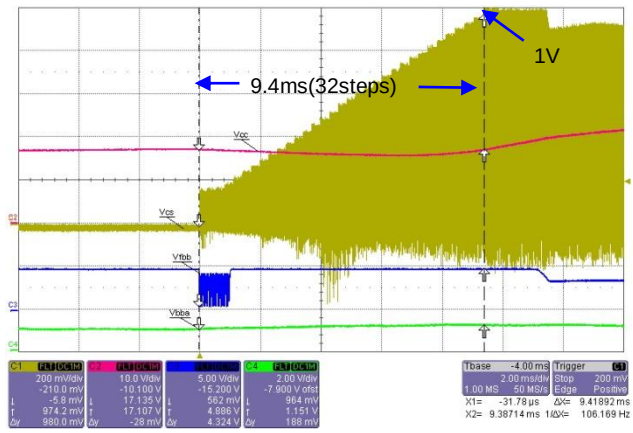
VCC_{HY} : Vcc turn-on/off hysteresis voltage (6.5V)

Therefore, the minimum Vcc capacitance can be 4.9µF. In order to give more margins, 10uF is taken for the design. The startup time $t_{STARTUP}$ is then 0.21s. The measured start up time is 0.23s (Figure 6). A 0.1uF filtering capacitor is always needed to add as near as possible to the Vcc pin to filter the high frequency noise.

6.2 Soft Start

When the IC is turned on after the startup time, a digital soft start circuit is activated. A gradually(32 steps) increased soft start voltage is emitted by the digital soft start circuit, which in turn releases the duty cycle gradually increase from zero. The duty cycle increases to maximum (which is limited by the transformer design) at the end of the soft start period. When the soft start time ends, IC goes into normal mode and the duty cycle is controlled by the FB signal. The soft start time is set at 10ms for maximum load. The soft start time is load dependent; shorter soft start time with lighter load.

Figure 8 shows the soft start behavior at 85Vac input and maximum load. The primary peak current increases slowly to the maximum in the soft start period.



Channel 1; C1 : Current sense voltage (V_{CS}) Channel 2; C2 : Supply voltage (VCC) Channel 3; C3 : Feedback voltage (V_{FBB}) Channel 4; C4 : BBA voltage (V_{BBA})
Soft Start time = 9.4ms(32 steps)
Soft start @ Vin=85Vac & max. load

Figure 8 Soft start at AC line input voltage of 85 Vac

6.3 Low standby power - Active Burst Mode

The IC will enter Active Burst Mode function at light load condition which enables the system to achieve the lowest standby power requirement of less than 100mW. Active Burst Mode means the IC is always in the active state and can therefore immediately response to any changes on the FB signal, V_{FB}.

6.3.1 Entering Active Burst Mode with selectable burst entry level

Because of the current mode control scheme, the feedback voltage V_{FB} actually controls the power delivery to output. An important relationship between the V_{CS} and the V_{FB} is expressed in equation (3).

$$V_{FB} = V_{CS} \cdot A_V + V_{Offset-Ramp} \quad (3)$$

where, V_{FB}:feedback voltage, V_{CS}:current sense voltage, A_V:PWM OP gain (3.25), $V_{Offset-Ramp}$:voltage ramp offset (0.6V)

When the output load reduces, the feedback voltage V_{FB} drops. If the V_{FB} stays below V_{FB_burst} for 20ms, the IC enters into the Active Burst Mode. The threshold power to enter burst mode is expressed in equation (4).

$$P_{BURST_enter} = \frac{1}{2} \cdot L_P \cdot I_p^2 \cdot f_{SW} = \frac{1}{2} \cdot L_P \cdot \left(\frac{V_{CS}}{R_{sense}}\right)^2 \cdot f_{SW} = \frac{1}{2} \cdot L_P \cdot \left(\frac{V_{FB_burst} - V_{Offset-Ramp}}{R_{sense} \cdot A_V}\right)^2 \cdot f_{SW} \quad (4)$$

where, L_p : transformer primary inductance

R_{sense}: current sense resistance, f_{sw}: switching frequency, V_{FB_burst}: Feedback level to enter burst mode

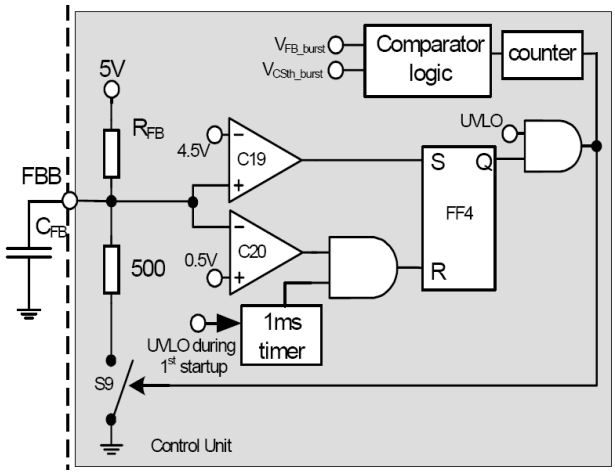
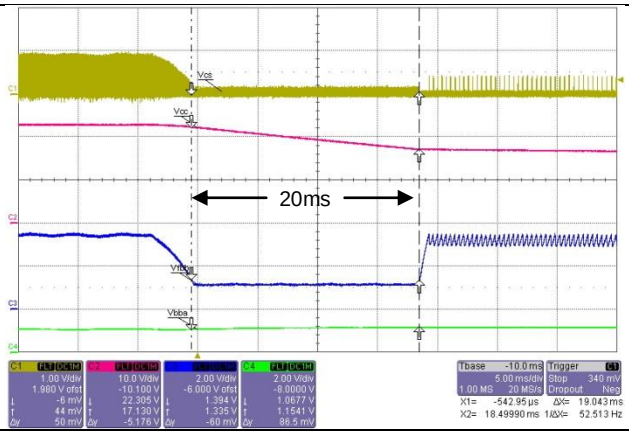


Figure 9 Entry burst mode detection

In enhancement to CoolSET™ F3R, user can select the burst mode entry and exit level in CoolSET™ -F3R80 according to the application by adding different values of C_{FB} (C19) capacitor at FBB pin. The IC would detect the number of count at the FBB pin within the 1st 1ms after VCC reaches the V_{Vcc_on} (17V). During that detection time, the V_{FBB} voltage swings between 0.5 V to 4.5V like a sawtooth waveform by charging and discharging the FBB capacitor, C_{FB} as shown in Figure 4. Based on the number of count, the IC will select burst mode entry and exit level. There are 4 different levels are available and the following table is the recommended capacitance range of the C_{FB} (C19) capacitor for the entry and exit burst level.

C_{FB}	Corresponding no. of counts	Entry level		Exit level	
		% of P_{in_max}	V_{FB_burst}	% of P_{in_max}	V_{csth_burst}
≥ 6.8nF	≤ 7	10%	1.6V	20%	0.45V
1nF~2.2nF	8 ~ 39	6.67%	1.42V	13.30%	0.37V
220pF~470pF	40 ~ 91	4.38%	1.27V	9.60%	0.31V
≤100pF	≥ 92	0	never	0	always

Figure 10 shows the waveform with the load drops from nominal load to light load. After the 20ms blanking time IC goes into burst mode.



Channel 1; C1 : Current sense voltage (V_{CS})
Channel 2; C2 : Supply voltage (VCC)
Channel 3; C3 : Feedback voltage (V_{FBB})
Channel 4; C4 : BBA voltage (V_{BBA})

Entering Active Burst mode with built-in blanking time 20ms when load changes from full to light @ Vin=85Vac

Figure 10 Entering active burst mode

6.3.2 Working in Active Burst Mode

In the active burst mode, the IC is constantly monitoring the output voltage by feedback pin, V_{FBB}, which controls burst duty cycle and burst frequency. The burst "ON" starts when V_{FB} reaches 3.5V and it stops when V_{FB} is dropped to 3.2V. During burst "ON", the primary current limit is reduced to V_{csth_burst} (31% ~ 45% of maximum peak current) to reduce the conduction losses and to avoid audible noise. The FB voltage is swinging like a saw tooth between 3.2V and 3.5V. The corresponding secondary output ripple (peak to peak) is controlled to be small. It can be calculated by equation (5).

$$V_{out_ripple_pp} = \frac{R_{opto}}{R_{FB} \cdot G_{opto} \cdot G_{TL431}} \cdot \Delta V_{FB} \quad (5)$$

where, R_{opto} : series resistor with opto-coupler at secondary side (e.g. R21 in Figure 3)

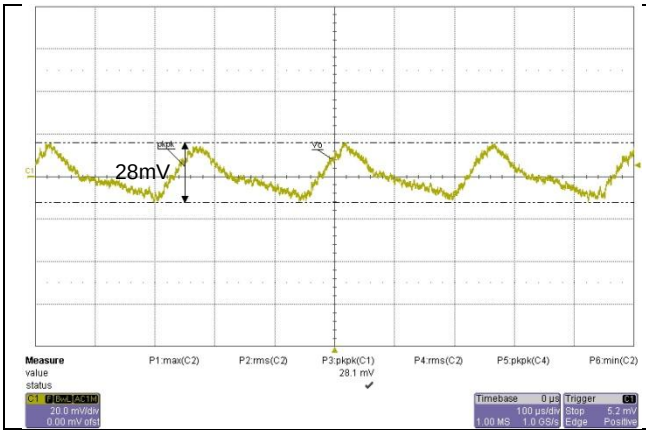
R_{FB} : IC internal pull up resistor connected to FB pin (R_{FB}=15.4KΩ)

G_{opto} : current transfer gain of opto-coupler

G_{TL431} : voltage transfer gain of the loop compensation network (e.g. R23, R24, R25, R26, C26, C27 in Figure 5)

ΔV_{FB} : feedback voltage change (0.3V)

Figure 11 is the output ripple waveform of the 20W 5V demo board. The burst ripple voltage is about 30mV.



Channel 1; C1 : Output ripple voltage (Vo)
$V_{ripple_pk_pk}$=28mV Probe terminal end with decoupling capacitor of 0.1uF(ceramic) & 1uF(electrolytic), 20MHz filter
Output ripple voltage @ 85Vac and 1W load

Figure 11 Output ripple during Active Burst Mode at light load

6.3.3 Leaving Active Burst Mode

When the output load increases to be higher than the maximum exit level of burst mode, V_{out} will drop a little and V_{FB} will rise up fast to exceed 4.0V. The system leaves burst mode immediately when V_{FB} reaches 4.0V. Once system leaves burst mode, the current sense voltage limit, V_{csth}, is released to 1.06V, the feedback voltage V_{FBB} swings back to the normal control level.

The leaving burst power threshold is (i.e. maximum power to be handled during burst operation) is expressed in equation (6). However, the actual power can be higher as it would include propagation delay time.

$$P_{burst_max} = 0.5 \cdot L_P \cdot \left(\frac{V_{csth_burst}}{R_{sense}}\right)^2 \cdot f_{SW} = 0.5 \cdot L_P \cdot \left(\frac{V_{csth_burst}}{V_{csth}} \cdot \frac{V_{csth}}{R_{sense}}\right)^2 \cdot f_{SW} = \left(\frac{V_{csth_burst}}{V_{csth}}\right)^2 \cdot P_{in_max} \quad (6)$$

where, V_{csth_burst}: peak current in the burst mode, V_{csth}: maximum current limit threshold at CS pin,

P_{in_max}: maximum input power, R_{sense}: current sense resistor, L_p : primary inductance of trf

The leave burst mode timing diagram is shown in Figure 12.

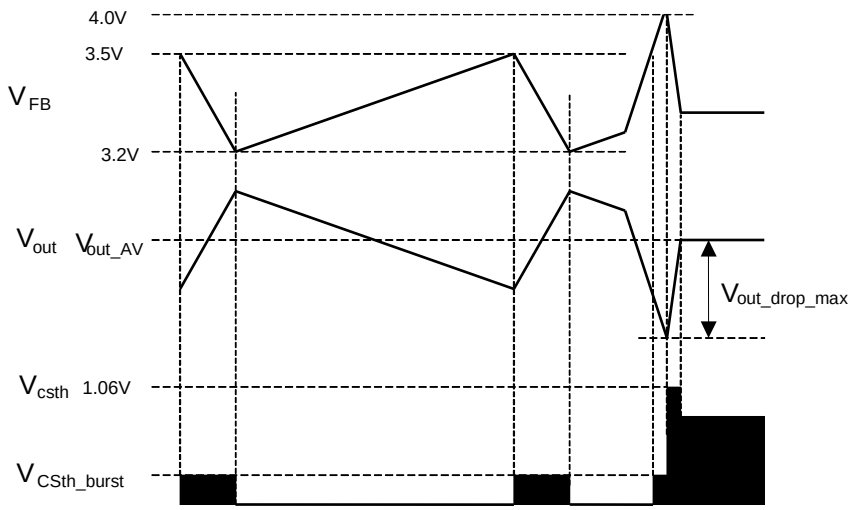
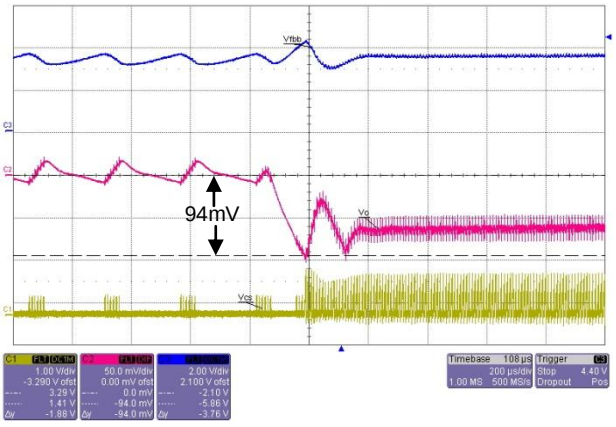


Figure 12 V_{out_drop} during leaving burst mode

The maximum output drop during the transition can be estimated in equation (7).

$$V_{out_drop_max} = \frac{R_{opto}}{R_{FB} \cdot G_{opto} \cdot G_{TL431}} \cdot (4 - \frac{3.2 + 3.5}{2}) = \frac{0.65 \cdot R_{opto}}{R_{FB} \cdot G_{opto} \cdot G_{TL431}} \quad (7)$$

Figure 13 is the captured waveform when there is a load jump from light load to full load. The output ripple drop during the transition is about 94mV.



Channel 1; C1 : Current sense voltage (V_{CS})
Channel 2; C2 : Output ripple voltage (Vo)
Channel 3; C3 : FB voltage (V_{FBB})

Leaving Active Burst mode when load change from light to full @ Vin=85Vac

Figure 13 Leaving burst mode waveform

6.3.4 Minimum Vcc supply voltage during burst mode

It is particularly important that the Vcc voltage must stay above V_{VCCoff} (i.e. 10.5V). Otherwise, the expected low standby power cannot be achieved. The IC will go into auto-restart mode instead. A reference Vcc circuit is presented in Figure 3. This is for a low cost transformer design where the transformer coupling is not too good. Thus the circuit R14 and ZD11 is added to clamp the Vcc voltage exceeding 25.5V in extreme case such as high load and the Vcc OVP protection is triggered. If the transformer coupling is good, this circuit is not needed.

6.3.5 Remarks for the selection of entry/exit burst level

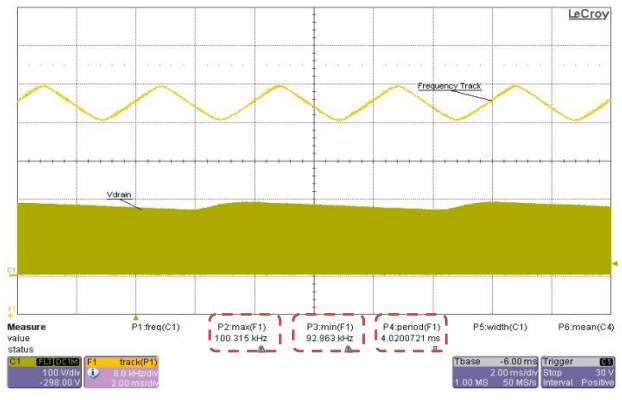
The selection of the entry/exit burst level will depend on the actual application. The below table is the remarks for the selection.

C_{FB}	Remarks
≥ 6.8nF	Highest entry/exit burst level: highest burst power, good for larger standby load. It needs to take care of not having too high loop gain as it would have a chance of unstable burst mode (rapid entry and exit burst mode). In case of unstable, the easiest way is to reduce the loop gain by increasing the opto-coupler biasing resistor, R21. However, too low loop gain would result to higher output ripple.
1nF~2.2nF	2nd highest entry/exit burst level: good for general application. It needs to take care CS pin noise to be as small as possible as it would have a chance of unstable burst mode (rapid entry and exit burst mode). In case of unstable, it is better to add noise filtering capacitor (eg., 100nF ceramic cap) in between CS(Pin 3) and Gnd (Pin 8). However, adding filtering cap would increase maximum overload power and widen the burst mode entry and exit power. Besides, it can also be improved by reducing the loop gain by increasing the opto-coupler biasing resistor, R21. However, if the gain is too low, it would result in higher output ripple.
220pF~470pF	Lowest entry/exit burst level: good for very small standby load. It needs to take care CS pin noise to be as small as possible as it would have a chance of unstable burst mode (rapid entry and exit burst mode). In case of unstable, it is better to add noise filtering capacitor (eg., 100nF ceramic cap) in between CS(Pin 3) and Gnd (Pin 8). However, adding filtering cap would increase maximum overload power and widen the burst mode entry and exit power. Besides, it can also be improved by reducing the loop gain by increasing the opto-coupler biasing resistor, R21. However, if the gain is too low, it would result in higher output ripple.
≤100pF	Do not enter burst mode: good for application that can accept higher standby power but with lowest output ripple voltage.

6.4 Low EMI noise

6.4.1 Frequency jittering

The IC is running at a fixed frequency of 65kHz or 100kHz with jittering frequency at +/-4% in a switching modulation period of 4ms. This kind of frequency modulation can effectively help to obtain a low EMI noise level particularly for conducted EMI. The jittering frequency measured for ICE3AR2280JZ is 92 KHz ~ 100 KHz (refer to Figure 14).



	Channel 1; C1 : Drain voltage (V_{Drain}) Channel F1 : Frequency track of C1
	Frequency jittering from 93 kHz ~ 100 kHz, Jitter period=4ms
	Frequency jittering @ 85Vac and max. load

Figure 14 Frequency jittering (V_{drain})

6.4.2 Soft gate drive and gate turn on resistor

The gate soft driving is to split the gate driving slope into 2 so that the CoolMOS™ turns on speed is relatively slower comparing to a single slope drive (see Figure 15). Besides soft gate drive, it is also implemented with 50Ω gate turn on resistor. In this way, the high ΔI/Δt noise is greatly reduced and the noise signal reflected in the EMI spectrum is also reduced.

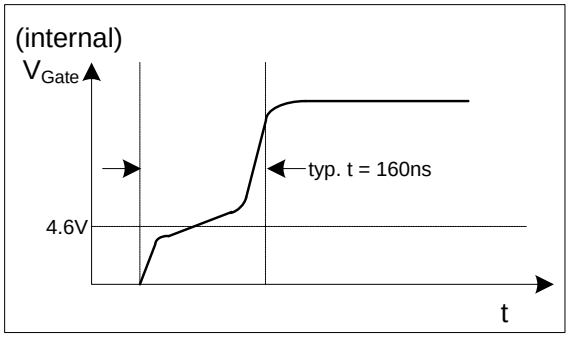


Figure 15 Soft gate drive waveform

6.4.3 Other suggestions to solve EMI issue

Some more suggestions to improve the EMI performance are listed below.

Add capacitor (Cds) at the drain source pin: it can slow down the turn off speed of the MOSFET and the high ΔV/Δt noise will be reduced and so is the EMI noise. The drawback is more energy will be dissipated due to slower turn off speed of MOSFET.

Add snubber circuit to the output rectifier: Most of the radiated EMI noise comes out from the output of the system esp. for a system with output cable. Adding snubber circuit (R28 and C25) to the output rectifier is a more direct way to suppress those EMI noise (refer to Figure 5).

6.5 Tight control in maximum power - Propagation delay compensation

The maximum power of the system is changed with the input voltage; higher voltage got higher maximum power. This is due to the propagation delay of the IC and the different rise time of the primary current under different input voltage. The propagation delay time is around 200ns. But if the primary current rise time is faster, the maximum power will increase. The power difference can be as high as >14% between high line and low line. In order to make the maximum power control become tight, a propagation delay compensation network is implemented so that the power difference is greatly reduced to best around 2%. Figure 13 shows the compensation scheme of the IC. The equation (8) explains the rate of change of the current sense voltage is directly proportional to the input voltage and current sense resistor. For a DCM operation, the operating range for the dV_{sense}/dt is from 0.1 to 0.7. It can show in Figure 13 that higher dV_{sense}/dt will give more compensation; i.e. lower value of V_{sense}.

$$\frac{dI_p}{dt} = \frac{V_{in}}{L_p} \Rightarrow R_{sense} \cdot \frac{dI_p}{dt} = R_{sense} \cdot \frac{V_{in}}{L_p} \Rightarrow \frac{dV_{sense}}{dt} = R_{sense} \cdot \frac{V_{in}}{L_p} \quad (8)$$

where, I_p : primary peak current, V_{in} : input voltage, L_p : primary inductance of the transformer,

V_{sense} : current sense voltage, R_{sense} : current sense resistor

The measured maximum input power for the 20W 5V demo board at 85Vac and 282Vac shows ±3.86% of maximum input power. This function is limited to discontinuous conduction mode flyback converter only.

Note that similar compensation also is applied to burst mode but since the switching pulse duty cycle is relatively small and the effect is not very obvious.

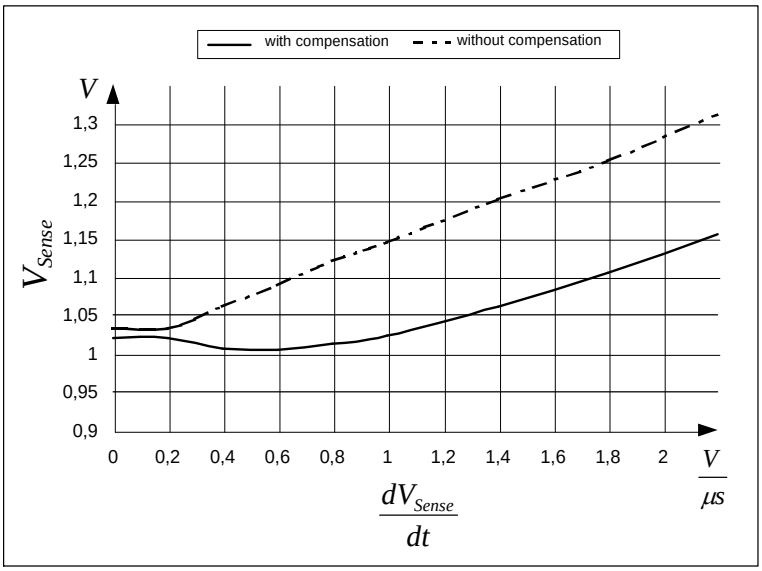


Figure 16 Propagation delay compensation curve

6.6 Protection Features

Protection is one of the major factors to determine whether the system is safe and robust. Therefore sufficient protection is necessary. ICE3xRxx80JZ/VJZ provides three kinds of protection mode; odd skip auto restart, non switch auto restart and normal auto restart. A list of protections and the failure conditions are shown in the following table.

Protection function	Failure condition	Protection Mode	ICE3xRxx80JZ	ICE3xRxx80VJZ
VCC overvoltage(1)	VCC > 20.5V & V_{FBB} > 4.5V & during soft start period	Odd skip auto restart	√	√
VCC overvoltage(2)	VCC > 25.5V	Odd skip auto restart	√	√
Over load/ Open loop	V_{FBB} > 4.5V, after blanking time	Odd skip auto restart	√	√
VCC under voltage/ Short optocoupler	VCC < 10.5V	Normal auto restart	√	√
Over temperature	T_J > 130°C (recovered with 50°C hysteresis)	Non switch auto restart	√	√
External protection enable	V_{BBA} < 0.4V	Non switch auto restart	√	-

6.6.1 Odd skip auto restart protection mode

When the failure condition meets the odd skip auto restart protection mode, the IC will enter into odd skip auto restart. The switching pulse will stop. Then the Vcc voltage will drop. When the Vcc voltage drops to 10.5V, the startup cell will turn on again. The Vcc voltage is then charged up until 17V. Unlike auto restart mode, there is no detect of fault and no switching pulse for the first (odd number) restart cycle. At the second (even number) of restart cycle, the fault detects and soft start switching pulses maintained. If the fault persists, it would continue the auto-restart mode. However, if the fault is removed, it can release to normal operation only at the even number auto restart cycle.

The main purpose of the odd skip auto restart is to extend the restart time such that the power loss during auto restart protection can be reduced. This feature can allow adopting smaller Vcc capacitor where the restart time is shorter.

Figure 16 shows the odd skip auto restart switching waveform of the Vcc and V_{CS}. No detect of fault and no switching pulse for the first and odd restart cycle and there are fault detect and soft start switching pulses at the second and even restart cycle.

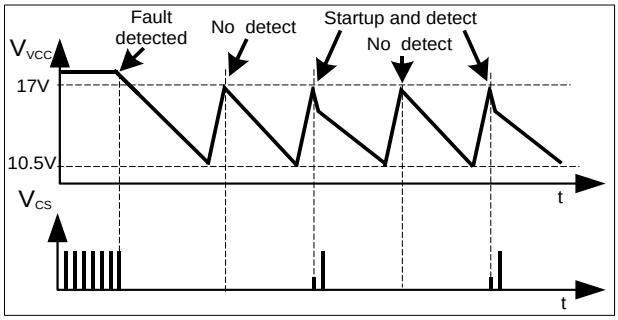


Figure 17 Odd skip auto restart mode

6.6.2 Non switch auto restart mode

Non switch auto restart mode is similar to odd skip auto restart mode except the start up switching pulses are also suppressed at the even number of the restart cycle. The detection of fault still remains at the even number of the restart cycle. When the fault is removed, the IC will resume to normal operation at the even number of the restart cycle (Figure 17).

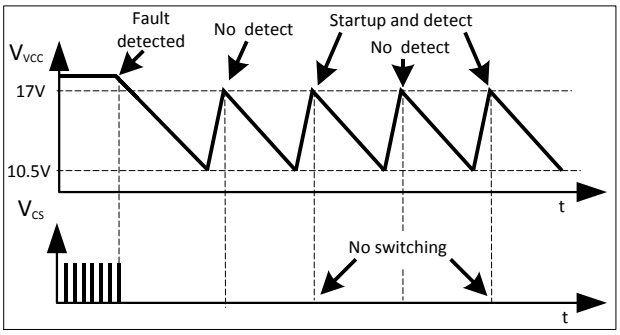


Figure 18 Non switch auto restart mode

6.6.3 Blanking time for over load protection

The IC controller provides a blanking window before entering into the odd skip auto restart mode due to output overload/short circuit. The purpose is to ensure that the system will not enter protection mode unintentionally. There are 2 kinds of the blanking time; basic and the extendable. The basic one is a built-in feature which is set at 20ms.

The extendable one is to extend the basic one with a user defined additional blanking time. The extendable blanking time can be attained by adding a capacitor, C_{BK} (0.22µF) to the BBA/BV pin. When there is over load occurred (V_{FBB} > 4.5V), the built-in blanking time counter starts to count for 20ms, then extended blanking time timer (CT1) starts to activate and monitor the counting at C_{BK} capacitor. During extended blanking time, C_{BK} capacitor is charged by an internal constant current (I_{chg_EB} =720uA) through S1 until C_{BK} voltage reaches 4.5V and CT1 timer count will increase by 1, then discharged by switch S2 via 500Ω resistor until C_{BK} voltage reaches 0.9V. The CT1 timer will count up to 256 times, and then the odd skip auto restart protection will be activated. The total blanking time is the addition of the basic and the extended blanking time and it can be calculated by equation (9) and (10).

$$t_{blanking} = 20ms + \left\{256 \times \left(\left(\frac{(4.5-0.9) \times C_{BK}}{I_{chg_EB}'} \right) + \left(C_{BK} \times 500 \times \ln\left(\frac{4.5}{0.9}\right) \right) \right) \right\} \quad (9)$$

$$I_{chg_EB}' = 720\mu A - \frac{(4.5+0.9)}{2 * R_2} \quad (10)$$

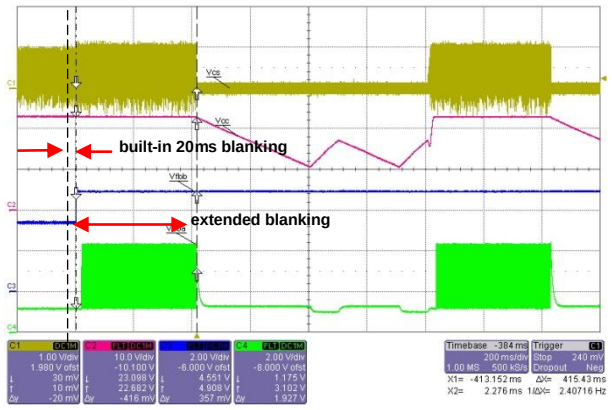
where, R_2 : R_{BO2} for ICE3xRxx80JZ
R_2 : R_{OV2} for ICE3xRxx80VJZ

Blanking time calculation for Figure 5 is as follows,

$$I_{chg_EB}' = 720\mu A - \frac{(4.5+0.9)}{2*R_{BO2}} = 623.6\mu A$$

where R_{BO2}=28kΩ

$$t_{blanking_R_{BO2}} = 20ms + \left\{256 \times \left(\left(\frac{(4.5-0.9)\times C_{BK}}{I_{chg_EB}'}\right) + \left(C_{BK} \times 500 \times \ln(\frac{4.5}{0.9})\right)\right)\right\} = 390.4ms$$



Channel 1; C1 : Current sense voltage (V_{CS})
Channel 2; C2 : Supply voltage (VCC)
Channel 3; C3 : Feedback voltage (V_{FBB})
Channel 4; C4 : BBA voltage (V_{BBA})

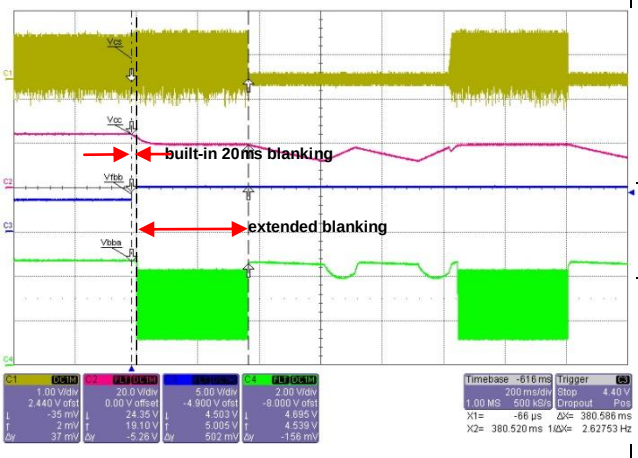
Total blanking time =415ms (Enable brownout, R_{BO2}=28kΩ & C_{BK} =0.22µF)

Over load protection with extended blanking time @ 85Vac

Figure 19 Blanking window for overload protection (Enable brownout & C_{BK}=0.22uF)

If brownout mode is disable, then no R_{BO2} and $I_{chg_EB}' = I_{chg_EB} = 720\mu A$

$$t_{blanking} = 20\text{ms} + \left\{256 \times \left(\left(\frac{(4.5-0.9)\times C_{BK}}{I_{chg_EB}}\right) + \left(C_{BK} \times 500 \times \ln(\frac{4.5}{0.9})\right)\right)\right\} = 346.9\text{ms}$$



Channel 1; C1 : Current sense voltage (V_{CS})
Channel 2; C2 : Supply voltage (VCC)
Channel 3; C3 : Feedback voltage (V_{FBB})
Channel 4; C4 : BBA voltage (V_{BBA})

Total blanking time =380ms (Disable brownout & C_{BK} =0.22µF)

Over load protection with extended blanking time @ 85Vac

Figure 20 Blanking window for overload protection (Disable brownout & C_{BK}=0.22uF)

Blanking time calculation for Figure 6 is as follows,

$$I_{chg_EB}' = 720\mu A - \frac{(4.5+0.9)}{2*R_{OV2}} = 657.5\mu A$$

where R_{OV2}=43.2kΩ

$$t_{blanking_R_{OV2}} = 20ms + \left\{256 \times \left(\left(\frac{(4.5-0.9)\times C_{BK}}{I_{chg_EB}'}\right) + \left(C_{BK} \times 500 \times \ln(\frac{4.5}{0.9})\right)\right)\right\} = 373.7ms$$

Note: The above calculation does not include the effect of the brownout/input OVP circuit where there is extra biasing current flowing from the input (bulk capacitor). That means the extended blanking time will be shortened with the line voltage change if brownout/input OVP circuit is implemented.

In case of output overload or short circuit, the transferred power during the blanking period is limited to the maximum power defined by the value of the sense resistor R_{sense}.

The noise level in BBA/BV pin can be quite high particularly in some high power application. In order to avoid mis-triggering of other protection features, it is recommended to add a minimum 100pF filter capacitor at BBA/BV pin.

6.6.4 Brownout Mode (ICE3xRxx80JZ only)

When the AC line input voltage is lower than the input voltage range, brownout mode is detected by sensing the voltage level at BBA pin through the resistors divider from the bulk capacitor. Once the voltage level at BBA pin falls below 0.9V, the controller stops switching and enters into brownout mode. It is until the input level goes back to input voltage range and the Vcc hits 17V, the brownout mode is released. Note that there is no switching waveform but always brownout detect in every restart cycle during brownout mode (Figure 21).

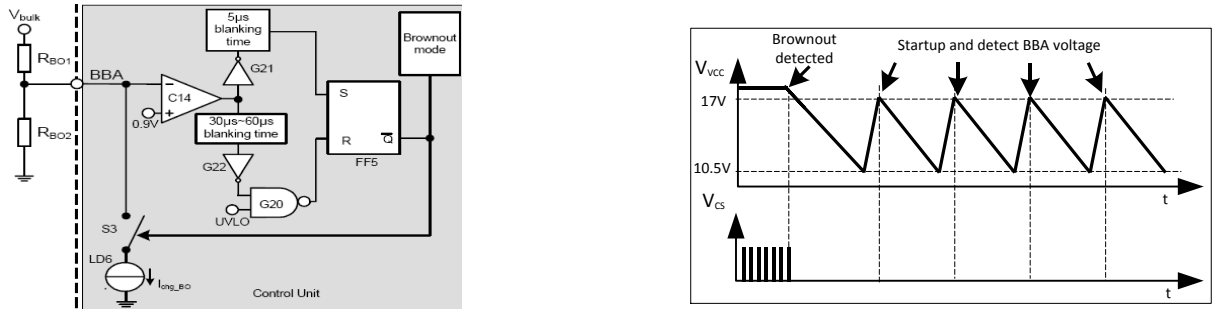


Figure 21 Brownout detection circuit and the waveform

Brownout sensing resistor R_{BO1} and R_{BO2} can be calculated as below.

$$R_{BO1} = \frac{V_{BO_hys}}{I_{chg_BO}} \quad (11)$$

$$R_{BO2} = \frac{V_{BO_ref} \times R_{BO1}}{V_{BO_L} - V_{BO_ref}} \quad (12)$$

where,
- V_{BO_hys} : input brownout hysteresis voltage
- I_{chg_BO} = 10µA : charging current for brownout
- V_{BO_ref} = 0.9V : brownout reference voltage for IC
- V_{BO_L} : input brownout voltage (low point)
- R_{BO1} and R_{BO2} : resistors divider from input voltage to BBA pin

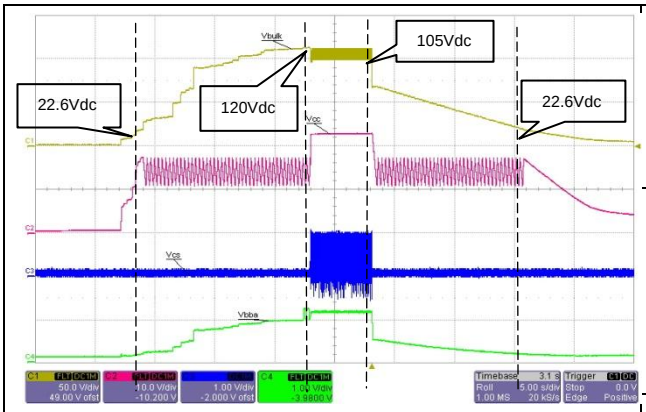
For example, if brownout release voltage is 85Vac and entry voltage is 75Vac and assuming there is a ripple voltage of 14Vdc at the bulk capacitor before entering brownout at full load.

$$V_{BO_H} = 85 \times \sqrt{2} = 120Vdc \qquad V_{BO_L} = 75 \times \sqrt{2} - 14 = 92Vdc$$

$$V_{BO_hys} = V_{BO_H} - V_{BO_L} = 28Vdc$$

$$R_{BO1} = \frac{V_{BO_hys}}{I_{chg_BO}} = 2.8M\Omega \quad , \quad R_{BO2} = \frac{V_{BO_ref} \times R_{BO1}}{V_{BO_L} - V_{BO_ref}} = 28k\Omega$$

(Note: R_{BO2} must be always ≥15kΩ in enable brownout mode, otherwise overload protection may not work)



Channel 1; C1 : Bulk voltage(V_{bulk})
Channel 2; C2 : Supply voltage (VCC)
Channel 3; C3 : Current sense voltage (V_{CS})
Channel 4; C4 : BBA voltage (V_{BBA})

IC on & 1st detect brownout: V_{bulk}= 22.6Vdc (16Vac)
Brownout reset: V_{bulk}= 120Vdc (85Vac)
Brownout triggered: V_{bulk}= 105Vdc (74Vac)
IC off: V_{bulk}= 22.6Vdc (16Vac)

Brownout mode with max. load

Figure 22 Brownout mode waveform

The above calculation assumes the tapping point (bulk capacitor) has a 14Vdc ripple voltage at full load when entering brownout mode. If there is no ripple voltage at light load, the enter brownout point will be lower, 65Vac. Besides that the low side brownout voltage V_{BO_L} added with the ripple voltage at the tapping point should always be lower than the high side brownout voltage (V_{BO_H}); V_{BO_H} > V_{BO_L} + ripple voltage. Otherwise, the brownout feature cannot work properly. In short, when there is a high load running in system before entering brownout, the input ripple voltage will increase and the brownout voltage will increase (V_{BO_L} = V_{BO_L}+ ripple voltage) at the same time. If the V_{BO_hys} is set too small and is close to the ripple voltage, then the brownout feature cannot work properly (V_{BO_L} = V_{BO_H}).
If the brownout feature is not needed, it needs to tie the BBA pin to the Vcc pin through a current limiting resistor (R17), 500kΩ~1MΩ. The BBA pin cannot be in floating condition. If the brownout feature is disabled with a tie up resistor, there is a limitation of the capacitor C_{BK} (C18) at the BBA pin. It is as below.

	Vcc tie up resistor	C_{BK_max}
1	500kΩ	0.47µF
2	1MΩ	0.22µF

6.6.5 Line input over voltage protection (ICE3xRxx80VJZ only)

The input OVP mode is detected by sensing the voltage level at BV pin through the resistors divider from the bulk capacitor. Once the voltage level at BV pin hits above 1.98V, the controller stops switching and enters into input OVP mode. When the BV voltage drop to 1.91V and the Vcc hits 17V, the input OVP mode is released. Input OVP sensing resistors R_{OV1} and R_{OV2} can be calculated as below.

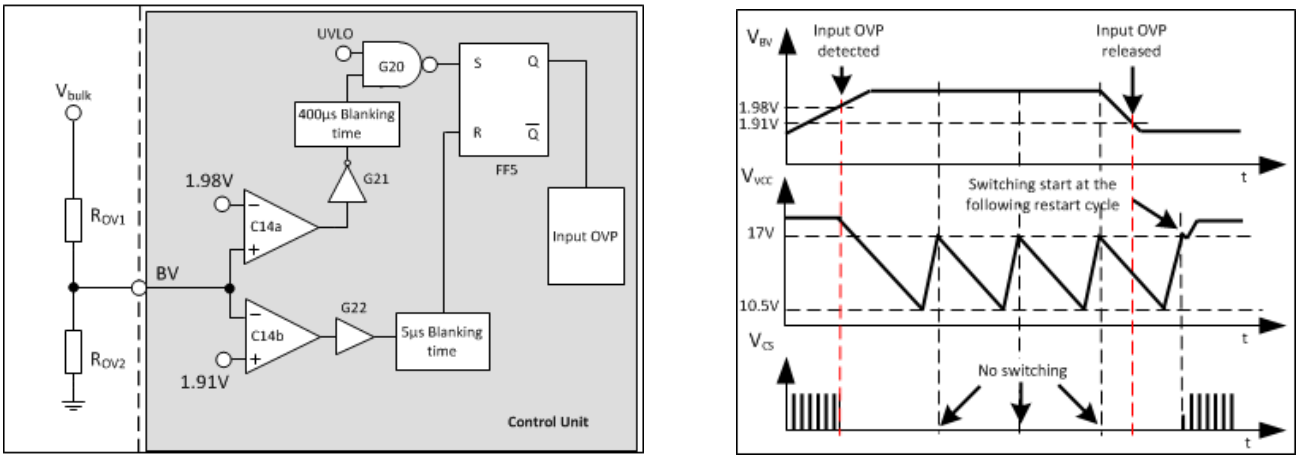


Figure 2 – Input OVP circuit and the waveform

$$R_{OV2} = \frac{R_{OV1} \times V_{OVP_ref}}{V_{OVP} - V_{OVP_ref}} \tag{13}$$

where V_{OVP} : input over voltage
V_{OVP_ref} : IC reference voltage for OVP (1.98V)
V_{OVP_hys} : IC hysteresis voltage for OVP (0.07V)
R_{OV1} & R_{OV2} : resistors divider from input voltage to BV pin

The formula to calculate the input OVP reset voltage is as below.

$$V_{OVP_reset} = \frac{(V_{OVP_ref} - V_{OVP_hys}) \times (R_{OV1} + R_{OV2})}{R_{OV2}} \tag{14}$$

where V_{OVP_reset} : input OVP reset voltage

For example, if input OVP detect level is 300Vac (424.26Vdc) and R_{OV1}=9MΩ

$$R_{OV2} = \frac{9M \times 1.98}{424.26 - 1.91} = 42.2k\Omega$$

$$V_{OVP_reset} = \frac{(1.98 - 0.07) \times (9M + 42.2k)}{42.2k} = 409.2Vdc(289Vac)$$

To disable the input OVP mode, the BV pin must connect with a resistor R_{OV2}≥15kΩ to the IC ground and remove R_{OV1}.

(Note: R_{OV2} must be always ≥15kΩ in all conditions, otherwise overload protection may not work)

6.6.6 External protection enable (ICE3xRxx80JZ only)

Although there are lots of pre-defined Auto Restart Protection is implemented in the IC, customer still can have some tailor-made protection for the application needs by pulling down the BBA pin to lower 0.4V. When BBA pin is lower than 0.4V, the gate drive switching will be stopped and IC will enter to non switch auto restart mode until the external protection enable signal released.

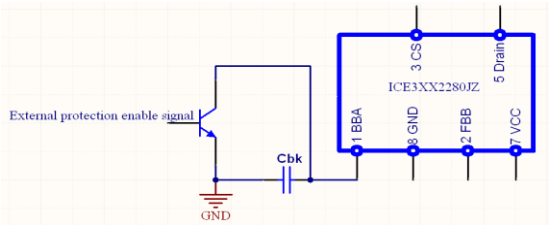


Figure 23 User defined external protection enable circuit

7 Input power curve

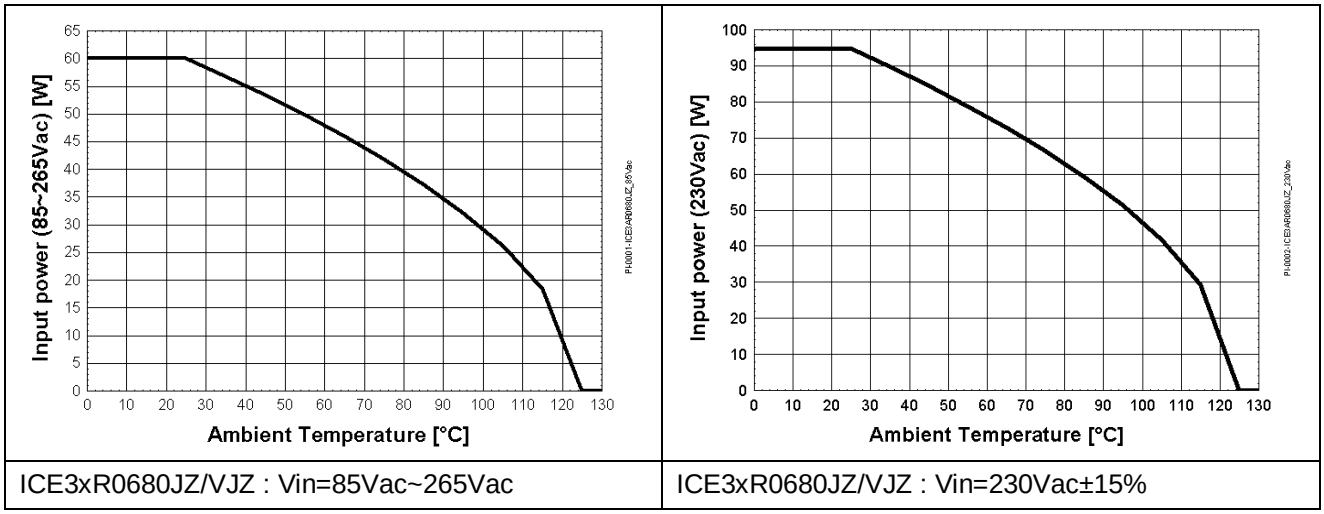
The purpose of the input power curve is to simplify the selection of the CoolSET™ device. The curve is a function of ambient temperature to the input power of the system in which the input filter loss, bridge rectifier loss and the MOSFET power loss are considered. The only information needed is the required output power, the input voltage range, the operating ambient temperature and the efficiency of the system. The required input power can then be calculated as equation (14).

$$P_{in} = \frac{P_o}{\eta} \tag{15}$$

where P_{in} : input power, P_o : output power, η : efficiency

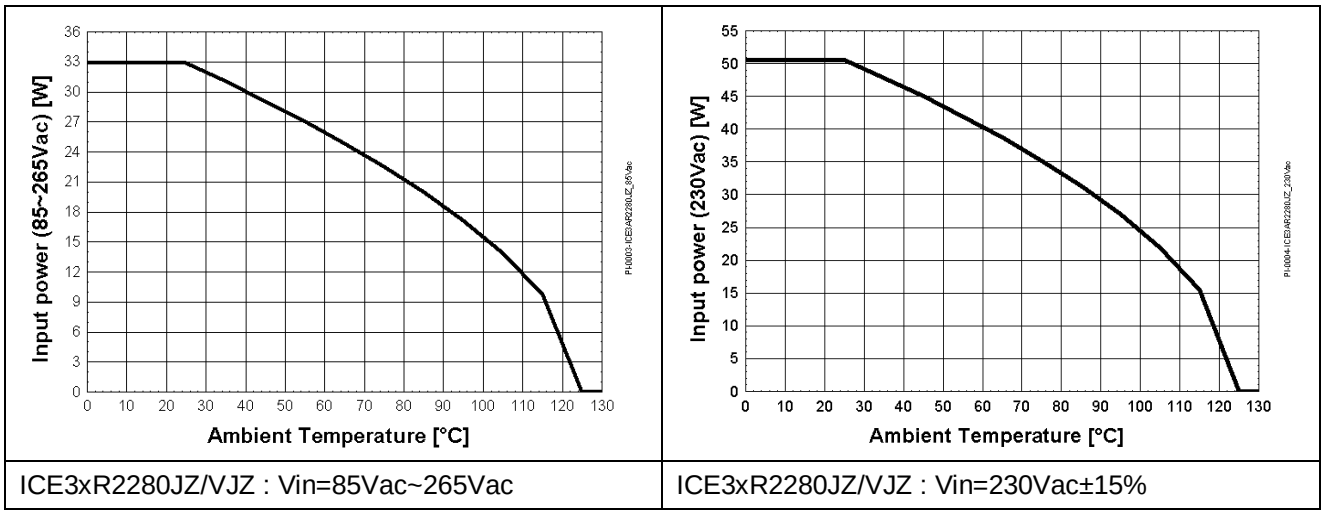
It then simply looks up the closed input power at the required ambient temperature from the input power curve.

The input power curves for the CoolSET-F3R80 (DIP-7) family are listed below.



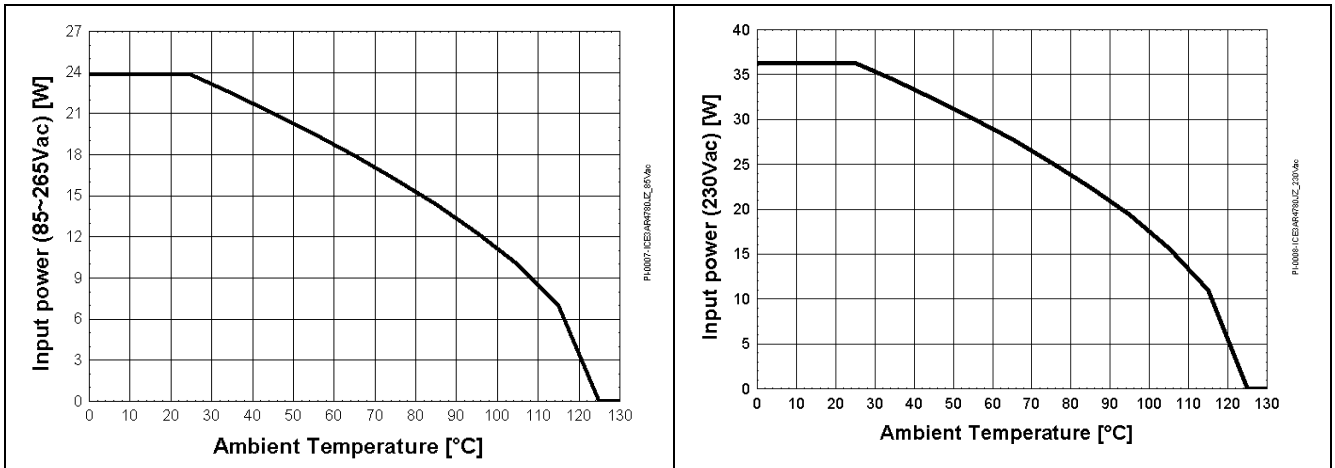
ICE3xR0680JZ/VJZ : Vin=85Vac~265Vac	ICE3xR0680JZ/VJZ : Vin=230Vac±15%

Figure 24 Input power curve for ICE3xR0680JZ/VJZ



ICE3xR2280JZ/VJZ : Vin=85Vac~265Vac	ICE3xR2280JZ/VJZ : Vin=230Vac±15%

Figure 25 Input power curve for ICE3xR2280JZ/VJZ



ICE3AR4780JZ/VJZ : Vin=85Vac~265Vac	ICE3AR4780JZ/VJZ : Vin=230Vac±15%

Figure 26 Input power curve for ICE3AR4780JZ/VJZ

The major assumption for the calculation is listed below.

Reflection voltage from secondary side to primary side is 150V.

The assumed maximum power for the device is when the junction temperature of the integrated CoolMOS™ reaches 125°C. (With some margins to reach the over temperature protection of the device : 130°C). The maximum R_{dson} of the device at 125°C is taken for calculation.

There is no copper area as heatsink and the R_{thja}=96K/W (DIP-7)

Saturation current (I_{d_max} @ 125°C) of the MOSFET is considered which is showed in below table.

The typical resistance of the EMI filter is listed in the below table.

The voltage drop for the bridge rectifier is assumed to be 1V.

	Rdson_125°C (Ω)	I_{d_max} @125°C (A)	R_{EMI_filter} (Ω)	V_{F_bridge} (V)
ICE3xR0680JZ/VJZ	1.58	12.60	2 * 0.56	2 * 1
ICE3xR2280JZ/VJZ	5.80	2.87	2 * 2	2 * 1
ICE3AR4780JZ/VJZ	11.50	1.45	2 * 3	2 * 1

8 Layout Recommendation

In order to get the optimized ruggedness of the IC to the transient surge events like ESD and lightning Surge test, the grounding of the PCB layout must be connected carefully. From the circuit diagram in Figure 5, it indicates that the grounding for the controller can be split into several groups; signal ground, Vcc ground, Current sense resistor ground and EMI return ground. All the split grounds should be "star" connected to the bulk capacitor ground directly. The split grounds are described as below.

Signal ground includes all small signal grounds connecting to the controller GND pin such as filter capacitor ground, C17, C18, C19 and opto-coupler ground.

Vcc ground includes the Vcc capacitor ground, C16 and the auxiliary winding ground, pin 2 of the power transformer.

Current Sense resistor ground includes current sense resistor R15 and R16.

EMI return ground includes Y capacitor, C15.

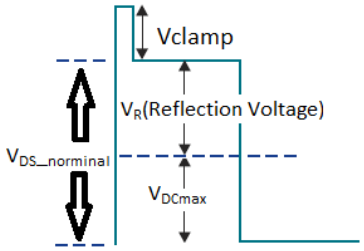
9 Product portfolio of CoolSET™ F3R80 (DIP-7) brownout/input OVP & frequency jitter version

Device	Package	V_{DS}	Frequency / kHz	R_{dson} /Ω[1]	230Vac±15%[2]	85-265Vax±15% [2]
ICE3AR4780JZ/VJZ	PG-DIP-7	800V	100	4.70	31W	20W
ICE3AR2280JZ/VJZ	PG-DIP-7	800V	100	2.26	43W	28W
ICE3AR0680JZ/VJZ	PG-DIP-7	800V	100	0.62	82W	52W
ICE3BR2280JZ	PG-DIP-7	800V	65	2.26	43W	28W
ICE3BR0680JZ	PG-DIP-7	800V	65	0.62	82W	52W

[1] Typ @ 25°C

[2] Calculated maximum input power rating at T_a=50°C, T_j=125°C and without copper area as heat sink. Refer to the data sheet for input power curve of other T_a

10 Useful formula for the SMPS design

Transformer calculation (DCM flyback)	
Input data	$V_{DC_min} = 90V$, $V_{DC_max} = 400V$, (Reflection voltage, $V_R = V_{DS_norminal} - V_{DC_{max}}$) $D_{max} < 0.55(55\%)$ 
Turn ratio	$N_{ratio} = \frac{V_{DS_norminal} - V_{DC_max}}{V_{out} + V_{FDiode}} = \frac{V_R}{V_{out} + V_{FDiode}}$
Maximum Duty ratio	$D_{max} = \frac{V_R}{V_R + V_{DC_min}}$
Primary Inductance	$L_P = \frac{(V_{DC_min} \times D_{max})^2}{2 \times P_{in} \times f_s}$
Primary peak current	$I_{p_max} = \frac{V_{DC_min} \cdot D_{max}}{L_p \cdot f_s}$
Primary turns	$N_p \geq \frac{I_{p_max} \cdot L_p}{B_{max} \cdot A_e}$
Secondary turns	$N_s = \frac{N_p}{N_{ratio}}$
Auxiliary turns	$N_{aux} = \frac{V_{cc} + V_{FDiode}}{V_{out} + V_{FDiode}} \cdot N_s$
ICE3xRxx80JZ/VJZ external component Design	
Current sense resistor	$R_{sense} \leq \frac{V_{csth}}{I_{p_max}}$
Soft start time	$t_{ss} = 10ms$
Vcc capacitor	$C_{VCC} = \frac{I_{VCCsup2} \times t_{ss}}{V_{VCChys}} \times \frac{2}{3}$
Startup time	$t_{STARTUP} = \frac{V_{VCCon} \times C_{Vcc}}{I_{VCCcharge}}$ (where $I_{VCCcharge}$ is the average current of $I_{VCCcharge2}$ and $I_{VCCcharge3}$)

Enter burst mode power	$P_{BURST_enter} = 0.5 \times L_P \times (\frac{V_{FB_burst} - V_{Offset-Ramp}}{R_{sense} \times A_V})^2 \times f_{SW}$
Leave burst mode power	$P_{burst_max} = 0.5 \times L_P \times (\frac{V_{csth_burst}}{R_{sense}})^2 \times f_{SW}$
Output ripple during burst mode	$V_{out_ripple_pp} = \frac{R_{opto}}{R_{FB} \times G_{opto} \times G_{TL431}} \times \Delta V_{FB}$
Voltage drop when leave burst mode	$V_{out_drop_max} = \frac{0.65 \times R_{opto}}{R_{FB} \times G_{opto} \times G_{TL431}}$
ICE3xRxx80JZ external component Design	
Total blanking time for over load protection (Disable brownout)	$t_{blanking} = 20ms + \left\{256 \times \left(\left(\frac{(4.5-0.9) \times C_{BK}}{I_{chg_EB}} \right) + \left(C_{BK} \times 500 \times ln(\frac{4.5}{0.9}) \right) \right) \right\}$
New charging current for extended blanking time with R_{BO2}	$I_{chg_EB}' = 720\mu A - \frac{(4.5+0.9)}{2 * R_{BO2}}$
Total blanking time for over load protection with R_{B02} (Enable brownout)	$t_{blanking_R_{BO2}} = 20ms + \left\{256 \times \left(\left(\frac{(4.5-0.9) \times C_{BK}}{I_{chg_EB}'} \right) + \left(C_{BK} \times 500 \times \ln(\frac{4.5}{0.9}) \right) \right) \right\}$
Brownout resistor 1, R_{BO1}	$R_{BO1} = \frac{V_{BO_hys}}{I_{chg_BO}}$ where $V_{BO_hys} = V_{BO_H} - V_{BO_L}$
Brownout resistor 2, R_{BO2}	$R_{BO2} = \frac{V_{BO_ref} \times R_{BO1}}{V_{BO_L} - V_{BO_ref}}$ **(Note: R_{BO2} must be always ≥15kΩ in enable brownout mode, otherwise overload protection may not work)**
ICE3xRxx80VJZ external component Design	
Charging current for extended blanking time with R_{OV2}	$I_{chg_EB}' = 720\mu A - \frac{(4.5+0.9)}{2 * R_{OV2}}$
Total blanking time for over load protection with R_{0V2}	$t_{blanking_R_{OV2}} = 20ms + \left\{256 \times \left(\left(\frac{(4.5-0.9) \times C_{BK}}{I_{chg_EB}'} \right) + \left(C_{BK} \times 500 \times \ln(\frac{4.5}{0.9}) \right) \right) \right\}$
Input OVP resistors, R_{OV1} & R_{OV1}	$R_{OV2} = \frac{R_{OV1} \times V_{OVP_ref}}{V_{OVP} - V_{OVP_ref}}$ **Note: R_{OV2} must be always ≥15kΩ in all conditions, otherwise overload protection may not work** **Minimum current at R_{ov1} should be higher than 5µA to avoid malfunction**
OVP reset voltage	$V_{OVP_reset} = \frac{(V_{OVP_ref} - V_{OVP_hys}) \times (R_{OV1} + R_{OV2})}{R_{OV2}}$

11 References

[1] Infineon Technologies, Datasheet “CoolSET™-F3R80 ICE3AR0680JZ Off-Line SMPS Current Mode Controller with Integrated 800V CoolMOS™ and Startup Cell (Brownout & frequency Jitter) in DIP-7”

[2] Infineon Technologies, Datasheet “CoolSET™-F3R80 ICE3AR2280JZ Off-Line SMPS Current Mode Controller with Integrated 800V CoolMOS™ and Startup Cell (Brownout & frequency Jitter) in DIP-7”

[3] Infineon Technologies, Datasheet “CoolSET™-F3R80 ICE3AR4780JZ Off-Line SMPS Current Mode Controller with Integrated 800V CoolMOS™ and Startup Cell (Brownout & frequency Jitter) in DIP-7”

[4] Infineon Technologies, Datasheet “CoolSET™-F3R80 ICE3BR0680JZ Off-Line SMPS Current Mode Controller with Integrated 800V CoolMOS™ and Startup Cell (Brownout & frequency Jitter) in DIP-7”

[5] Infineon Technologies, Datasheet “CoolSET™-F3R80 ICE3BR2280JZ Off-Line SMPS Current Mode Controller with Integrated 800V CoolMOS™ and Startup Cell (Brownout & frequency Jitter) in DIP-7”

[6] Infineon Technologies, Datasheet “CoolSET™-F3R80 ICE3AR0680VJZ Off-Line SMPS Current Mode Controller with Integrated 800V CoolMOS™ and Startup Cell (Input OVP & frequency Jitter) in DIP-7”

[7] Kyaw Zin Min, Kok Siu Kam Eric, Infineon Technologies, Application Note “AN-EVALSF3R80-ICE3AR0680JZ, 30W 12V SMPS Evaluation Board with CoolSET™-F3R80 ICE3AR0680JZ”

[8] Kyaw Zin Min, Kok Siu Kam Eric, Infineon Technologies, Application Note “AN-EVALSF3R80-ICE3AR2280JZ, 20W 5V SMPS Evaluation Board with CoolSET™-F3R80 ICE3AR2280JZ”

[9] Kyaw Zin Min, Kok Siu Kam Eric, Infineon Technologies, Application Note “AN-EVALSF3R80-ICE3AR4780JZ, 12W 5V SMPS Evaluation Board with CoolSET™-F3R80 ICE3AR4780JZ”

[10] Infineon Technologies, Application Note ANPS0079 “AN-EVAL-3AR0680VJZ, 30W 12V SMPS Evaluation Board with ICE3AR0680VJZ”

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