ICE3BRxx65JF

CoolSET®-F3R (FullPak) new Jitter version Design Guide

Power Management & Supply



Never stop thinking.

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ICE3BRxx65JF

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1 Introduction

The **ICE3BRxx65JF** is the latest development of the CoolSET®-F3. It is a PWM controller with power MOSFET and startup cell in FullPak package. The switching frequency is running at 67 kHz and it is especially suitable for medium AC/DC power supply such as battery charger, LCD monitors, adapters for printers and notebook computers, DVD players and recorder, Blue-Ray DVD player and recorder, set-top boxes and industrial auxiliary power supplies.

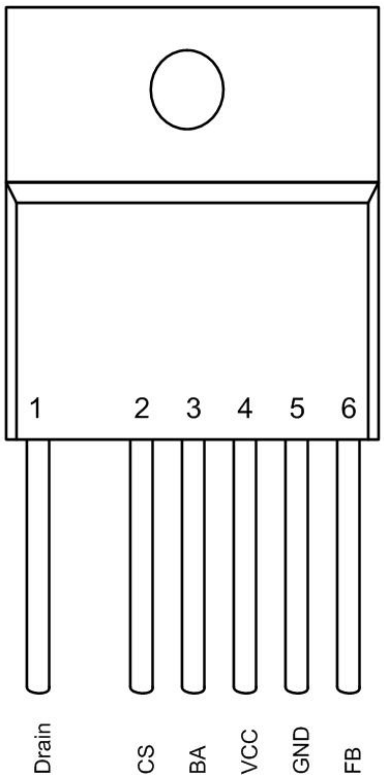
The **ICE3BRxx65JF** adopts the BiCMOS technology and provides a wider Vcc operating range up to 25V. It inherits the proven good features of CoolSET®-F3 such as the active burst mode achieving the lowest standby power, the propagation delay compensation making the most precise current limit control in wide input voltage range, etc. In addition, it also adds on some useful features such as built-in soft start time, built-in basic with extendable blanking time for over load protection and built-in switching frequency modulation (frequency jittering), external auto-restart enable, etc.

2 List of Features

650V avalanche rugged CoolSET® with built-in Startup Cell
Active Burst Mode for lowest Standby Power
Fast load jump response in Active Burst Mode
67 kHz internally fixed switching frequency
Auto Restart Protection Mode for Over-load, Open Loop, Vcc Undervoltage, Over temperature & Vcc Over-voltage
Built-in Soft Start
Built-in blanking window with extendable blanking time for short duration high current
External auto-restart enable pin
Max Duty Cycle 75%
Overall tolerance of Current Limiting < ±5%
Internal PWM Leading Edge Blanking
BiCMOS technology provides wide VCC range
Built-in Frequency jitter feature and soft driving for low EMI

3 Package

The package for F3R ICE3BRxx65JF Jitter mode product is TO220 FullPak.



Pin	Symbol	Function
1	Drain	650V[1)] CoolMOS® Drain
2	CS	Current Sense/650V[1)] CoolMOS® Source
3	BA	extended Blanking & Auto Restart enable
4	VCC	Controller Supply Voltage
5	GND	Controller Ground
6	FB	Feedback

Figure 1 Pin configuration

[1] at T_j=110°C

4 Block Diagram

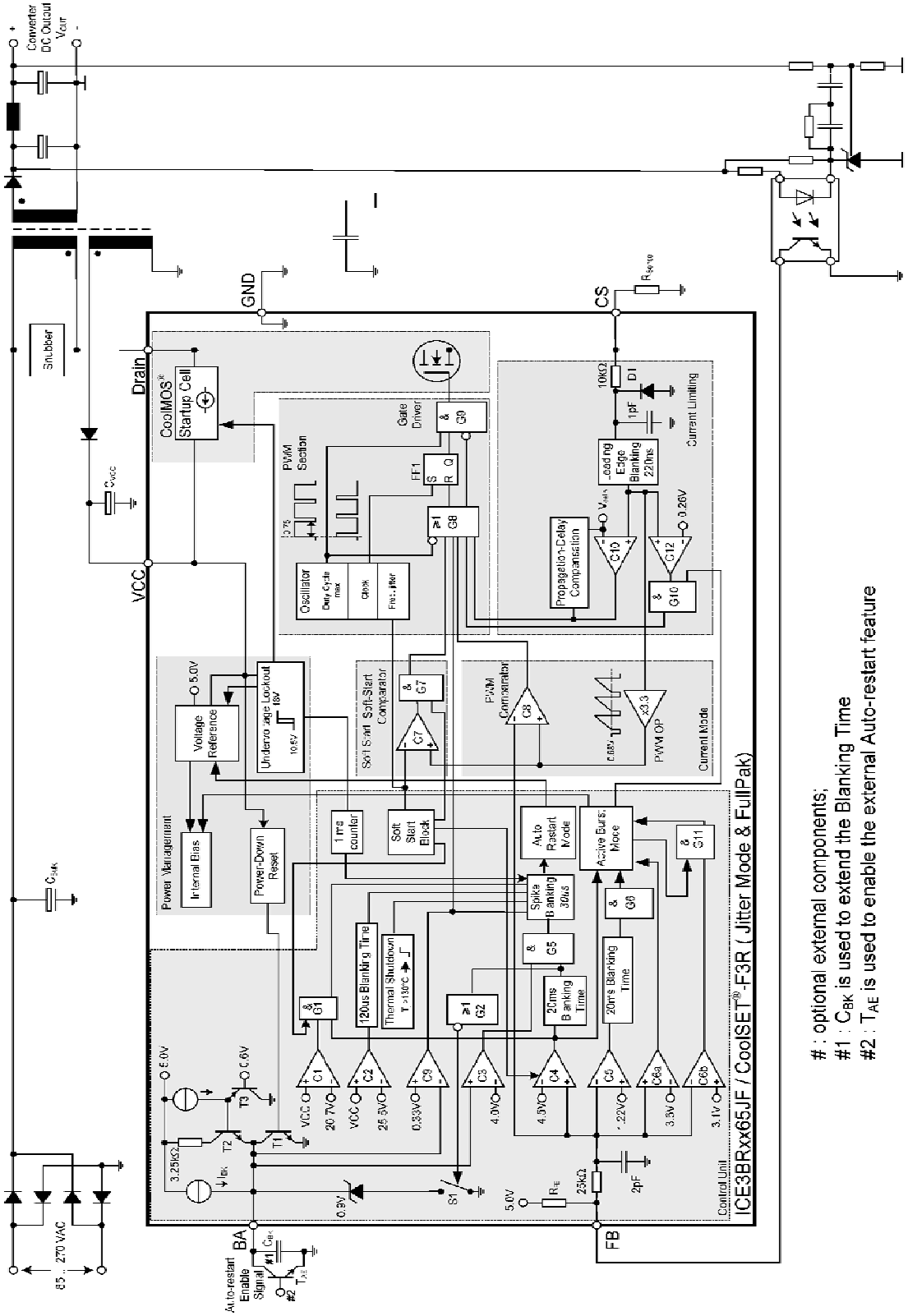


Figure 2 Block Diagram of ICE3BRxx65JF

5 Typical Application Circuit

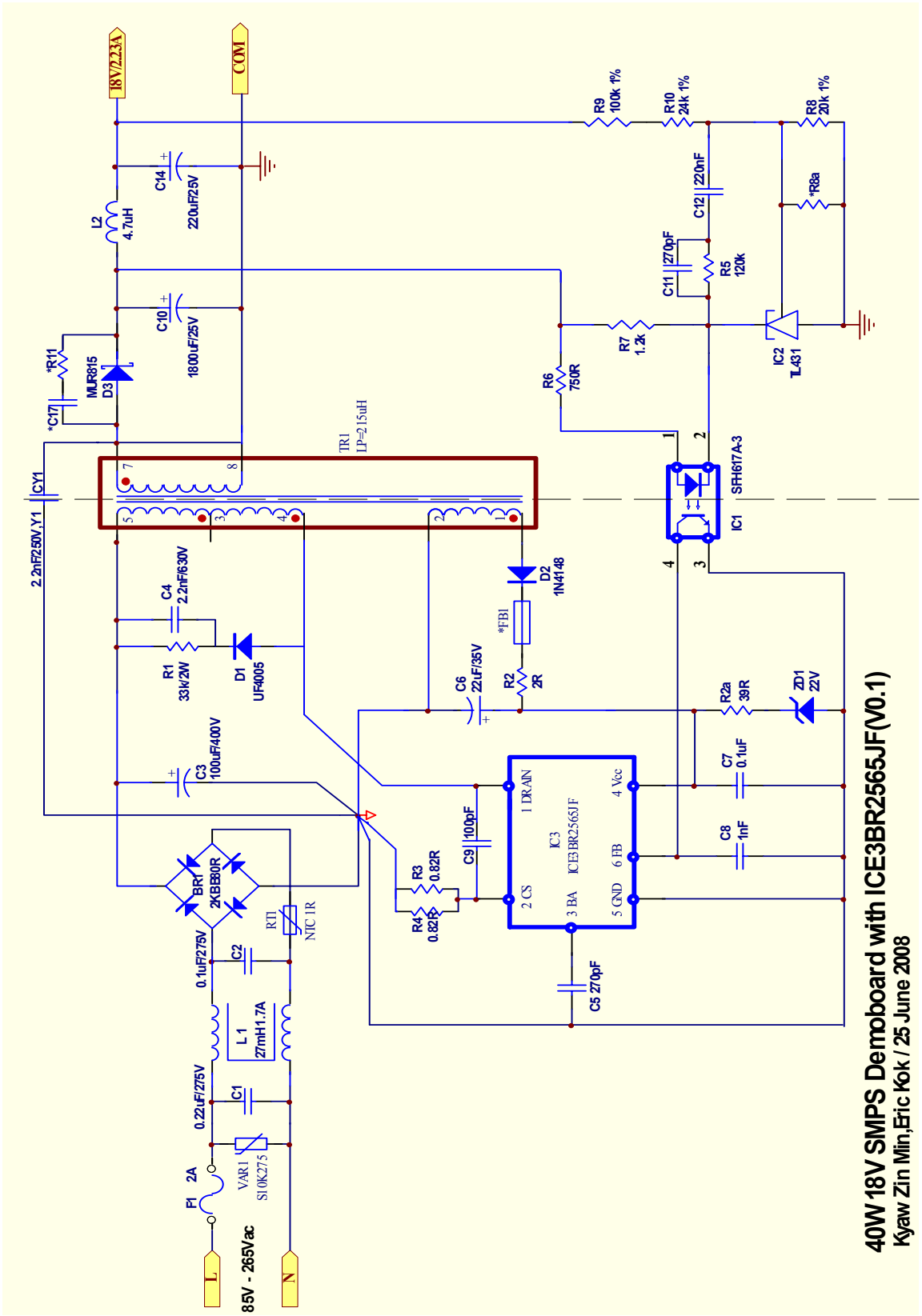


Figure 3 Typical application circuit with ICE3BR2565JF 40W 18V

6 Functional description and component design

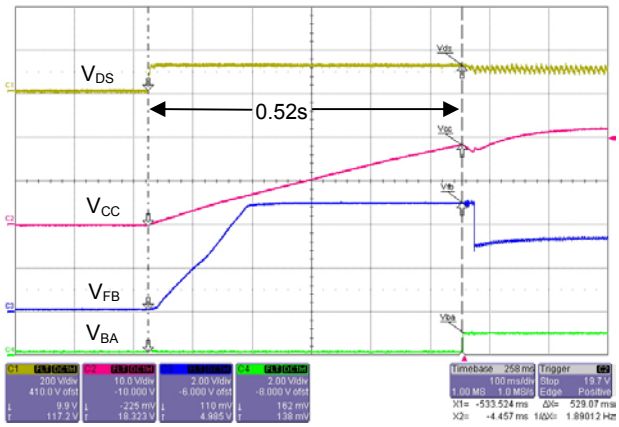
6.1 Startup time

Startup time is counted from applying input voltage to IC turn on. ICE3BRxx65JF has a startup cell which is connected to input bulk capacitor. When there is input voltage, the startup cell will act as a constant current source to charge up the Vcc capacitor and supply energy to the IC. When the Vcc capacitor reaches the Vcc_on threshold 18V, the IC turns on. Then the startup cell is turned off and the Vcc is supplied by the auxiliary winding. Start up time is independent from the AC line input voltage and it can be calculated by the equation (1). Figure 4 shows the start up time of 85Vac line input.

$$t_{STARTUP} = \frac{V_{VCCon} \cdot C_{Vcc}}{I_{VCCch\,arg\,e3}} \quad (1)$$

where, $I_{VCCcharge3}$: constant current from startup cell (0.7mA), V_{VCCon} : IC turns on threshold (18V), C_{VCC} : Vcc capacitor

Refer to the datasheet for the symbol used in the equation.



Channel 1; C1 : Drain to Source Voltage (V_{DS})
Channel 2; C2 : Supply Voltage (V_{CC})
Channel 3; C3 : FB voltage (V_{FB})
Channel 4; C4 : BA Voltage (V_{BA})

Startup time = 0.52s

Startup delay time @ Vin=85Vac & 40W load

Figure 4 The startup delay time at AC line input voltage of 85Vac

Precaution : For a typical application, start up should be VCC ramps up first, other pin (such as FB pin) voltage will follow VCC voltage to ramp up. It is recommended not to have any voltage on other pins (such as FB; BA and CS) before VCC ramps up.

6.1.1 Vcc capacitor

The minimum value of the Vcc capacitor is determined by voltage drop during the soft start time. The formula is expressed in equation (2).

$$C_{VCC} = \frac{I_{VCC\,sup\,2} \cdot t_{ss}}{V_{CChys}} \cdot \frac{2}{3} \quad (2)$$

where, $I_{VCCsup2}$: IC consumption current (4.2mA), t_{ss} : soft start time (20ms),

V_{CChys} : Vcc turn-on/off hysteresis voltage (7.5V)

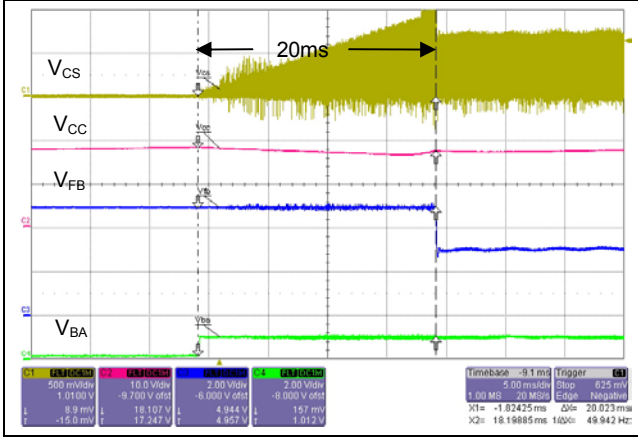
Therefore, the minimum Vcc capacitance can be 7.47µF. In order to give more margins, 22µF is taken for the design. The startup time $t_{STARTUP}$ is then 0.528s. The measured start up time is 0.52s (Figure 4). A 0.1uF filtering capacitor is always needed to add as near as possible to the Vcc pin to filter the high frequency noise. The filter capacitor C7 and the auxiliary series resistor R2 form a R-C filter which can effectively filter

the transformer switching noise from auxiliary winding going into the IC. Besides, the ferrite bead FB1 can also help to reduce the high frequency noise from going into the IC.

6.2 Soft Start

When the IC is turned on after the Startup time, a digital soft start circuit is activated. A gradually increased soft start voltage is generated by the digital soft start circuit, which in turn releases the duty cycle gradually increase. The duty cycle increases to maximum (which is limited by the transformer design) at the end of the soft start period. When the soft start time ends, IC goes into normal mode and the duty cycle is controlled by the FB signal. The soft start time is set at 20ms for maximum load. The soft start time is load dependent; shorter soft start time with lighter load.

Figure 5 shows the soft start behavior at 85Vac input. The primary peak current increases slowly to the maximum in the soft start period.



Channel 1; C1 : CS Voltage (V_{CS})
Channel 2; C2 : Supply Voltage (V_{CC})
Channel 3; C3 : FB voltage (V_{FB})
Channel 4; C4 : BA Voltage (V_{BA})

Soft start time = 20ms

20ms built in SoftStart time @ Vin=85Vac & 40W load

Figure 5 Soft start at AC line input voltage of 85Vac

6.3 Low standby power - Active Burst Mode

The IC will enter Active Burst Mode function at light load condition which enables the system to achieve the lowest standby power requirement of less than 100mW. Active Burst Mode means the IC is always in the active state and can therefore immediately response to any changes on the FB signal, V_{FB}.

6.3.1 Entering Active Burst Mode

Because of the current mode control scheme, the feedback voltage V_{FB} actually controls the power delivery to output. An important relationship between the V_{CS} and the V_{FB} is expressed in equation (3).

$$V_{FB} = V_{CS} \cdot A_V + V_{Offset-Ramp} \quad (3)$$

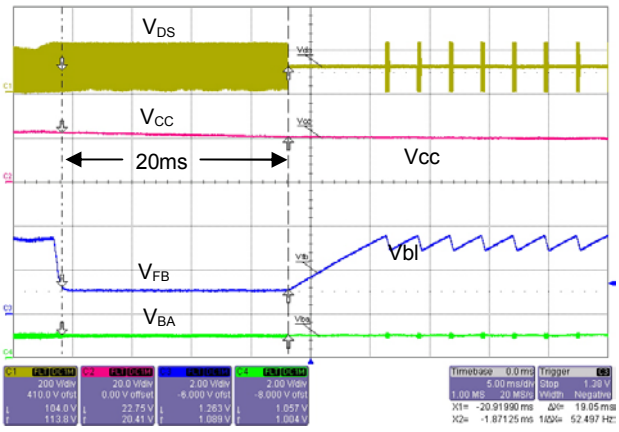
where, V_{FB}:feedback voltage, V_{CS}:current sense voltage, A_V:PWM OP gain, $V_{Offset-Ramp}$:voltage ramp offset

When the output load reduces, the feedback voltage V_{FB} drops. If the V_{FB} stays below 1.22V for 20ms, the IC enters into the Active Burst Mode. The threshold power to enter burst mode is expressed in equation (4).

$$P_{BURST_enter} = \frac{1}{2} \cdot L_P \cdot I_p^2 \cdot f_{SW} = \frac{1}{2} \cdot L_P \cdot \left(\frac{V_{CS}}{R_{sense}}\right)^2 \cdot f_{SW} = \frac{1}{2} \cdot L_P \cdot \left(\frac{V_{FBC5} - V_{Offset-Ramp}}{R_{sense} \cdot A_V}\right)^2 \cdot f_{SW} \quad (4)$$

where, L_p : transformer primary inductance, R_{sense}: current sense resistance, f_{sw}: switching frequency, V_{FBC5}: Feedback level to enter burst mode

Figure 6 shows the waveform with the load drops from nominal load to light load. After the 20ms blanking time IC goes into burst mode.



Channel 1; C1 : Drain-Source Voltage (V_{DS})
Channel 2; C2 : Supply Voltage (V_{CC})
Channel 3; C3 : FB voltage (V_{FB})
Channel 4; C4 : BA Voltage (V_{BA})

Entering Active Burst mode with preset time 20ms when load changes from full to light @ Vin=85Vac

Figure 6 Entering Burst Mode

6.3.2 Working in Active Burst Mode

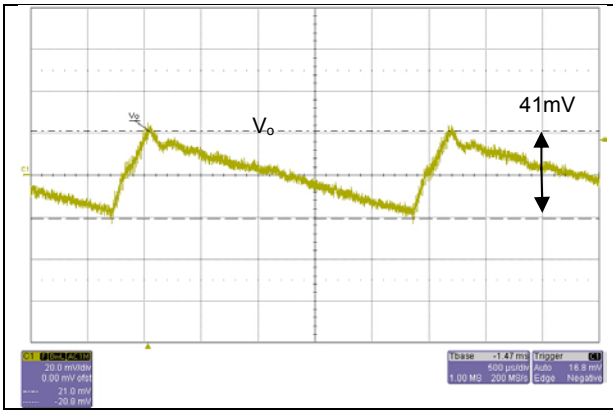
In the active burst mode, the IC is constantly monitoring the output voltage by feedback pin, V_{FB}, which controls burst duty cycle and burst frequency. The burst "ON" starts when V_{FB} reaches 3.6V and it stops when V_{FB} is dropped to 3.1V. During burst "ON", the primary current limit is set to 26% of maximum peak current (V_{CS}=0.26V) to reduce the conduction losses and to avoid audible noise. The FB voltage is changing like a saw-tooth between 3.1V and 3.6V. The corresponding secondary output ripple (peak to peak) is controlled to be small. It can be calculated by equation (5).

$$V_{out_ripple_pp} = \frac{R_{opto}}{R_{FB} \cdot G_{opto} \cdot G_{TL431}} \cdot \Delta V_{FB} \qquad (5)$$

where, R_{opto} : series resistor with opto-coupler at secondary side (e.g. R6 in Figure 3), R_{FB} : IC internal pull up resistor connected to FB pin (R_{FB}=15.4KΩ), G_{opto} : current transfer gain of opto-coupler, G_{TL431} : voltage transfer gain of the loop compensation network (e.g. R5, R8, R9, R10, C11, C12 in figure 3), ΔV_{FB} : feedback voltage change (0.5V)

Usually there is a noise coupling capacitor at the FB pin to filter the switching noise and spike (e.g. C8 in Figure 3). However, if this capacitor is too large (>10nF), it would affect the normal operation of the controller. This capacitor should be as small as possible (without the capacitor is the best). In the mean time, it is found that this filter capacitor will also affect the output ripple voltage during burst mode; larger capacitance will get larger ripple voltage and smaller capacitance get lower ripple voltage.

Figure 7 is the output ripple waveform of the 40W demo board. The burst ripple voltage is about 41mV.



Channel 1; C1 : Output ripple Voltage (V_o)

Output ripple voltage at light load @ Vin=85Vac

Figure 7 Output ripple during Active Burst Mode at light load

6.3.3 Leaving Active Burst Mode

When the output load increases to be higher than the maximum burst power, P_{burst_max}, V_{out} will drop a little bit and V_{FB} will rise up fast to exceed 4.5V. The system leaves burst mode immediately when V_{FB} reaches 4.5V. Once system leaves burst mode, the current sense voltage limit, V_{CS_MAX}, is released to 1V, the feedback voltage V_{FB} swings back to the normal control level.

The leaving burst power threshold is (i.e. maximum power to be handled during burst operation) is expressed in equation (6).

$$P_{burst_\max} = 0.5 \cdot L_P \cdot (0.26 \cdot I_{p_\max})^2 \cdot f_{SW} = 0.5 \cdot L_P \cdot (0.26 \cdot \frac{V_{CS_\max}}{R_{sense}})^2 \cdot f_{SW} = 0.0676 \cdot P_{in_\max} \quad (6)$$

where, $I_{p_\max}$: maximum primary peak current, V_{CS_max} : current limit threshold at CS pin, P_{in_max} : maximum input power

The calculated maximum power in burst mode is around 6.76% of P_{in_max}. However, the actual power can be higher as it would include propagation delay time.

The leave burst mode timing diagram is shown in Figure 8.

The maximum output drop during the transition can be estimated in equation (7).

$$V_{out_drop_\max} = \frac{R_{opto}}{R_{FB} \cdot G_{opto} \cdot G_{TL431}} \cdot (4.5 - \frac{3.1 + 3.6}{2}) = \frac{1.15 \cdot R_{opto}}{R_{FB} \cdot G_{opto} \cdot G_{TL431}} \quad (7)$$

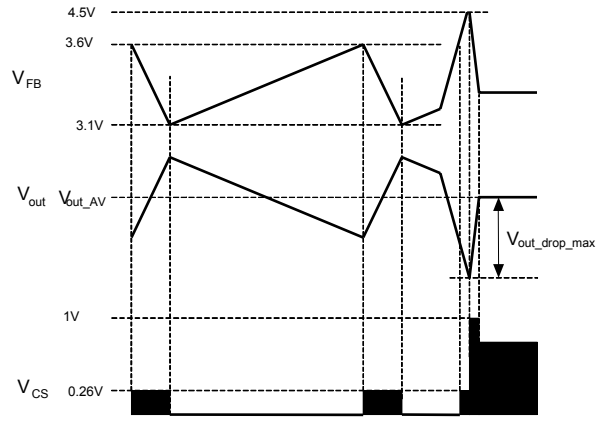
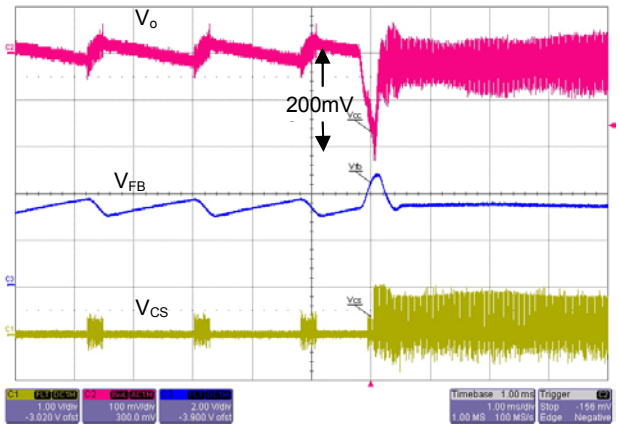


Figure 8 Timing diagram of leaving burst mode

Figure 9 is the captured waveform when there is a load jump from light load to full load. The output ripple drop during the transition is about 200mV.



Channel 1; C1 : CS Voltage (V_{CS})
Channel 2; C2 : Output Voltage (V_o)
Channel 3; C3 : FB voltage (V_{FB})

Leaving Active Burst mode when load change from light to full @ Vin=85Vac

Figure 9 Leaving burst mode waveform

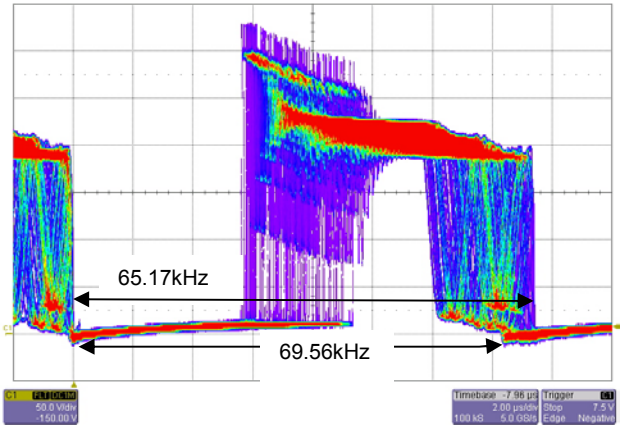
6.3.4 Minimum V_{CC} supply voltage during burst mode

It is particularly important that the Vcc voltage must stay above V_{VCCoff} (i.e. 10.5V). Otherwise, the expected low standby power cannot be achieved. The IC will go into auto-restart mode instead of Active Burst Mode. A reference Vcc circuit is presented in Figure 3. This is for a low cost transformer design where the transformer coupling is not too good. Thus the circuit R2a and Z1 is added to clamp the Vcc voltage exceeding 25V in extreme case such as high load and the Vcc OVP protection is triggered. If the transformer coupling is good, this circuit is not needed.

6.4 Low EMI noise

6.4.1 Frequency jittering

The IC is running at a fixed frequency of 67 KHz with jittering frequency at +/-2.7 KHz in a switching modulation period of 4ms. This kind of frequency modulation can effectively help to obtain a low EMI noise level particularly for conducted EMI. The jittering frequency measured is 65.1 KHz ~ 69.5 KHz (refer to Figure 10).



Channel 1; C1 : Drain to Source Voltage (V_{DS})
Frequency changing from 65.17kHz ~ 69.56kHz, Jitter period is set at 4ms internally
Frequency jittering at 40W load @ Vin=85Vac

Figure 10 Switching frequency jittering (Vds)

6.4.2 Soft gate drive

The gate soft driving is to split the gate driving slope into 2 so that the MOSFET turns on speed is relatively slower comparing to a single slope drive (see Figure 11). In this way, the high ΔI/Δt noise is greatly reduced and the noise signal reflected in the EMI spectrum is also reduced.

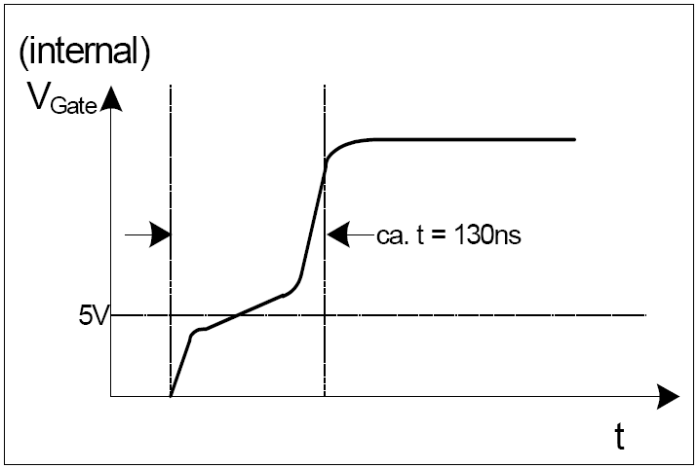


Figure 11 Soft gate drive waveform

6.4.3 Other suggestions to solve EMI issue

Some more suggestions to improve the EMI performance and is listed below.

1. Add capacitor (C_{ds}) at the drain source pin: it can slow down the turn off speed of the MOSFET and the high ΔV/Δt noise will be reduced and so is the EMI noise. The drawback is more energy will be dissipated due to slower turn off speed of MOSFET.
2. Add snubber circuit to the output rectifier: Most of the radiated EMI noise comes out from the output of the system esp. for a system with output cable. Adding snubber circuit (R11 and C17) to the output rectifier is a more direct way to suppress those EMI noise (refer to Figure 3).

6.5 Tight control in maximum power - Propagation delay compensation

The maximum power of the system is changed with the input voltage; higher voltage got higher maximum power. This is due to the propagation delay of the IC and the different rise time of the primary current under different input voltage. The propagation delay time is around 200ns. But if the primary current rise time is faster, the maximum power will increase. The power difference can be as high as >14% between high line and low line. In order to make the maximum power control become tight, a propagation delay compensation network is implemented so that the power difference is greatly reduced to best around 2%. Figure 12 shows the compensation scheme of the IC. The equation (8) explains the rate of change of the current sense voltage is directly proportional to the input voltage and current sense resistor. For a DCM operation, the operating range for the dV_{sense}/dt is from 0.1 to 0.7. It can show in Figure 12 that higher dV_{sense}/dt will give more compensation; i.e. lower value of V_{sense}.

$$\frac{dI_p}{dt} = \frac{V_{in}}{L_p} \Rightarrow R_{sense} \cdot \frac{dI_p}{dt} = R_{sense} \cdot \frac{V_{in}}{L_p} \Rightarrow \frac{dV_{sense}}{dt} = R_{sense} \cdot \frac{V_{in}}{L_p} \quad (8)$$

where, I_p : primary peak current, V_{in} : input voltage, L_p : primary inductance of the transformer, V_{sense} : current sense voltage, R_{sense} : current sense resistor

The measured maximum input power for the 40W demo boards at 85Vac and 265Vac shows ±0.99% of maximum input power. This function is limited to discontinuous conduction mode flyback converter only.

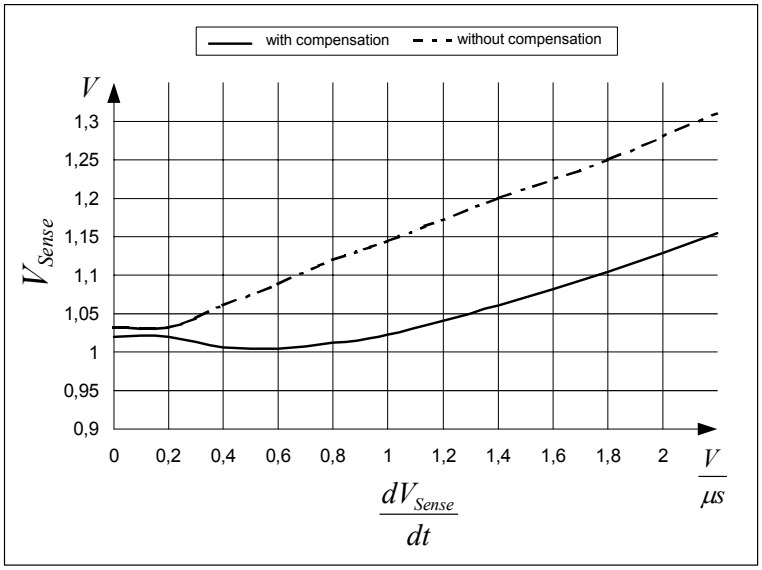


Figure 12 Propagation delay compensation curve

6.6 Protection Features

The IC provides several protection features which lead to the Auto Restart Protection Mode. The following table shows the conditions of the system failure and the associate protection mode.

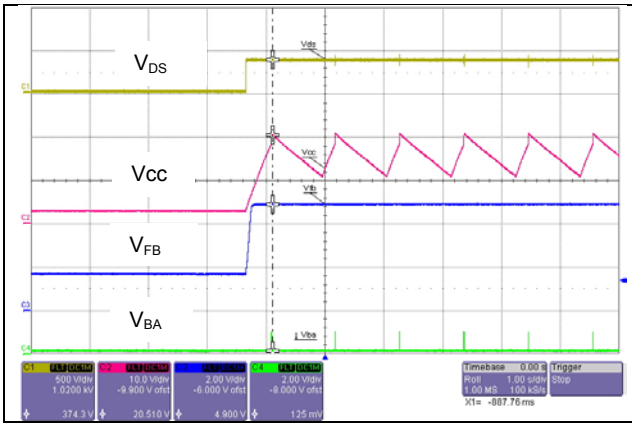
Protection function	Failure condition	Protection Mode
Vcc Over-voltage	1. Vcc > 25.5V or 2. Vcc > 20.7V & FB > 4.5V & during soft start period	Auto Restart
Over-temperature (controller junction)	T_J > 130°C	Auto Restart
Over-load / Open loop	V_{FB} > 4.5V and V_{BA} > 4.0V (Blanking time counted from charging V_{BA} from 0.9V to 4.0V)	Auto Restart
Vcc Under-voltage / short Opto-coupler	Vcc < 10.5V	Auto Restart
Auto-restart enable	V_{BA} < 0.33V	Auto Restart

Table 1 Protection functions and failure conditions

6.6.1 Auto Restart Protection Mode

When the failure condition meets the auto restart protection mode, the IC will go into auto-restart. The switching pulse will stop. Then the Vcc voltage will drop. When the Vcc voltage drops to 10.5V, the startup cell will turn on again. The Vcc voltage is then charged up. When it hits 18V, the IC will turn on and the startup cell will turn off. It would then start the startup phase with soft start. After the startup phase the failure condition is checked to determine whether the fault persists. If the fault is removed, it will go to normal operation. Otherwise, the IC will repeat the auto restart protection and the switching pulse stop again.

Figure 13 shows the switching waveform of the V_{CC} and the feedback voltage V_{FB} when the output is overloaded by shorting the outputs. The IC is turned on at V_{CC} = 18V. After going through the startup phase, IC is off again due to the presence of the fault. V_{CC} is discharged until 10.5V. Then, the Startup Cell is activated again to charge up capacitor at V_{CC} that initiates another restart cycle.



Channel 1; C1 : Drain-Source Voltage (V_{DS})
Channel 2; C2 : Supply Voltage (V_{CC})
Channel 3; C3 : Feedback Voltage (V_{FB})
Channel 4; C4 : BA voltage (V_{BA})

System enters auto restart mode when output voltage short circuit @ Vin=85Vac

Figure 13 Auto Restart Mode

6.6.2 Blanking Time for over load protection

The IC controller provides a blanking window before entering into the auto restart mode due to output overload/short circuit. The purpose is to ensure that the system will not enter protection mode unintentionally. There are 2 kinds of the blanking time; basic and the extendable. The basic one is a built-in feature which is set at 20ms. The extendable one is to extend the basic one with a user defined additional blanking time. The extendable blanking time can be achieved by adding a capacitor, C_{BK} to the BA pin. When there is over load occurred (V_{FB} > 4.5V), the C_{BK} capacitor will be charged up by a constant current source, I_{BK} (13uA) from

0.9V to 4.0V. Then the auto restart protection will be activated. The charging time from 0.9V to 4.0V to the C_{BK} capacitor is the extended blanking time. The total blanking time is the addition of the basic and the extended blanking time.

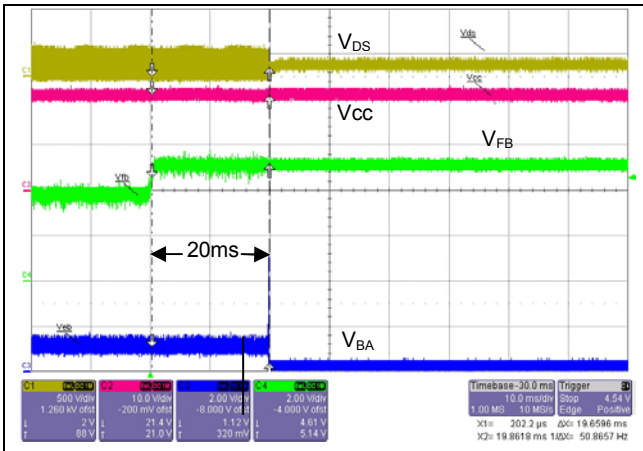
$$t_{blanking} = Basic + Extended = 20ms + \frac{(4.0-0.9)*C_{BK}}{I_{BK}} = 20ms + 238461.5*C_{BK} \quad (9)$$

The measured total blanking time showing in Figure 15 is 45ms using C_{BK}=0.1µF.

In case of output overload or short circuit, the transferred power during the blanking period is limited to the maximum power defined by the value of the sense resistor R_{sense}.

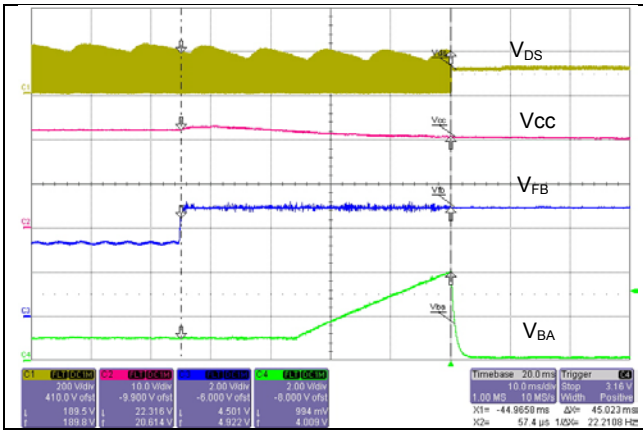
The noise level in BA pin can be quite high particularly in some high power application. In order to avoid mis-triggering of other protection features, it is recommended to add a minimum 270pF filter capacitor at BA pin to filter the noise for 40W design.

The maximum capacitor added at BA is restricted to be less than 0.65uF. Otherwise, the IC cannot be startup properly.



Channel 1; C1 : Drain to Source Voltage (V_{DS}) Channel 2; C2 : Supply Current (V_{CC}) Channel 3; C3 : Feedback Voltage (V_{FB}) Channel 4; C4 : BA voltage (V_{BA})
System enters auto-restart when V_{FB}>4.5V, V_{BA} >4V with built-in blanking time ≈ 20ms
Over load protection without extended blanking time; Cba=270pF @ Vin=85Vac and output power step from 2.23A to 4A load

Figure 14 blanking window for output over load protection (basic blanking time)



Channel 1; C1 : Drain to Source Voltage (V_{DS}) Channel 2; C2 : Supply Current (V_{CC}) Channel 3; C3 : Feedback Voltage (V_{FB}) Channel 4; C4 : BA voltage (V_{BA})
System enters auto-restart when V_{FB}>4.5V, V_{BA} >4V with (built-in+extendable) blanking time ≈45ms
Over load protection with extended blanking time; Cba=0.1µF @ Vin=85Vac; output power step from 2.23A to 4A load.

Figure 15 blanking window for output overload protection (extended blanking time=24ms with C_{BK}=0.1uF)

6.6.3 User defined protection by external protection enable pin

Although there are lots of pre-defined Auto Restart Protection is implemented in the IC, customer still can have some tailor-made protection for the application needs by pulling down the BA pin to lower 0.33V. When

BA pin lower than 0.33V, the gate drive switching will be stopped and IC will enter to auto restart mode until the external auto restart enable signal released.

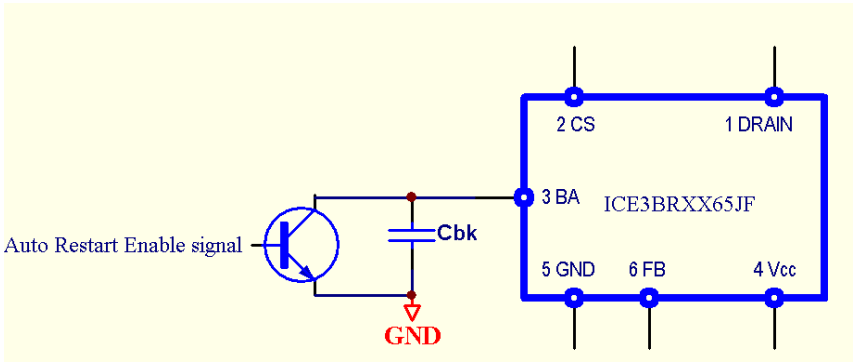


Figure 16 User defined Auto Restart Protection circuit

7 Input power curve

The purpose of the input power curve is to simplify the selection of the CoolSET® device. The curve is a function of ambient temperature to the input power of the system in which the input filter loss, bridge rectifier loss and the MOSFET power loss are considered. The only information needed is the required output power, the input voltage range, the operating ambient temperature and the efficiency of the system. The required input power can then be calculated as equation (10).

$$P_{in} = \frac{P_o}{\eta} \tag{10}$$

where P_{in} : input power, P_o : output power, η : efficiency

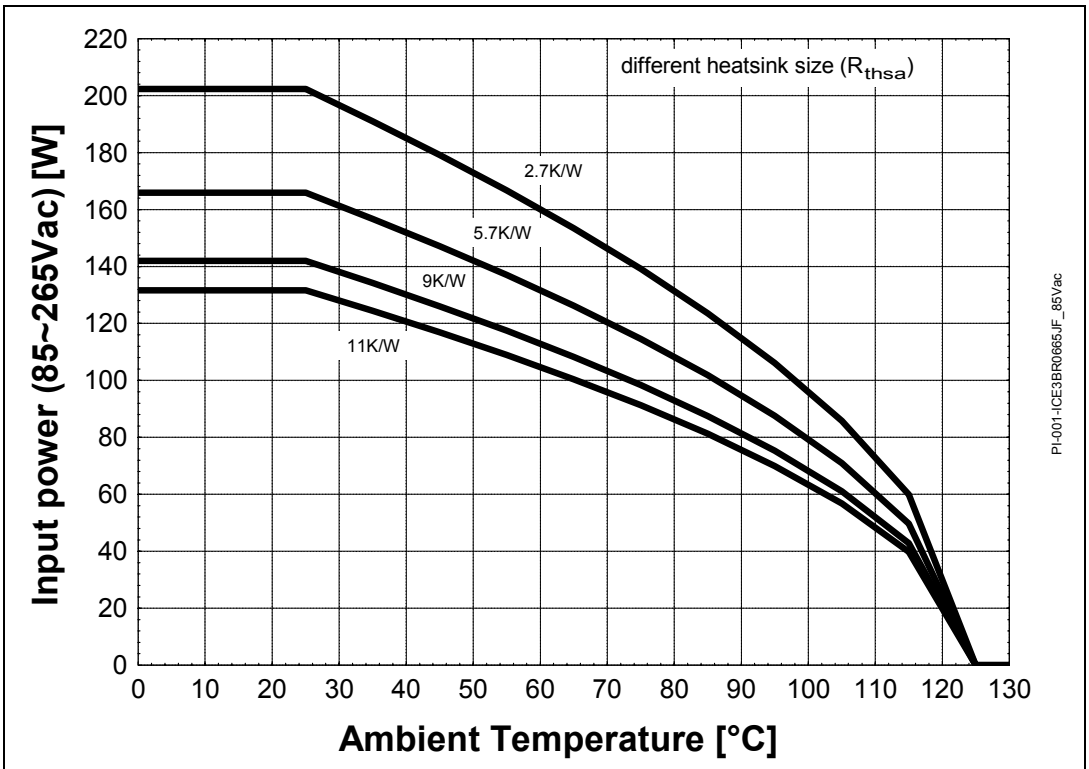
It then simply looks up the closed input power of the CoolSET at the required ambient temperature and expected heatsink size from the input power curve.

The input power curves for the CoolSET-F3R (FullPak) family with different heatsink size (R_{thsa}=2.7K/W, 5.7K/W, 9K/W and 11K/W） are listed in Figure 17, 18, 19 and 20.

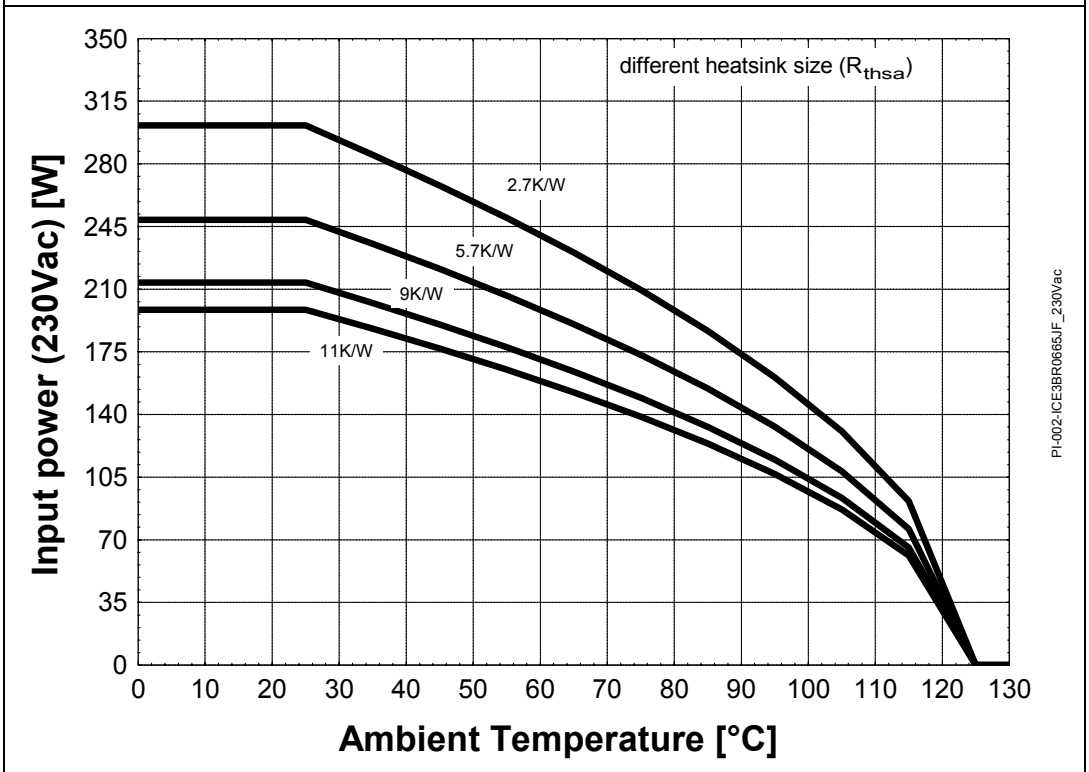
The major assumption for the calculation is listed below.

1. Reflection voltage from secondary side to primary side is 100V.
2. The assumed maximum power for the device is when the junction temperature of the integrated CoolMOS® reaches 125°C. (With some margins to reach the over temperature protection of the device : 130°C). The maximum R_{dson} of the device at 125°C is taken for calculation.
3. The heatsink R_{thsa}=2.7K/W , 5.7K/W, 9K/W and 11K/W and the thermal grease R_{thcs}=1.1K/W
4. Saturation current (I_{d_max} @ 125°C) of the MOSFET is considered which is showed in below table.
5. The typical resistance of the EMI filter is listed in the below table.
6. The voltage drop for the bridge rectifier is assumed to be 1V.

	Rdson_125°C (Ω)	I_{d_max} @125°C (A)	R_{thjc} (K/W)	R_{EMI_filter} (Ω)	V_{F_bridge} (V)
ICE3BR0665JF	1.79	11.64	3	2 * 0.085	2 * 1
ICE3BR1065JF	3.21	6.59	4.4	2 * 0.185	2 * 1
ICE3BR1465JF	4.53	4.51	4.8	2 * 0.56	2 * 1
ICE3BR2565JF	6.26	2.68	5.2	2 * 0.56	2 * 1

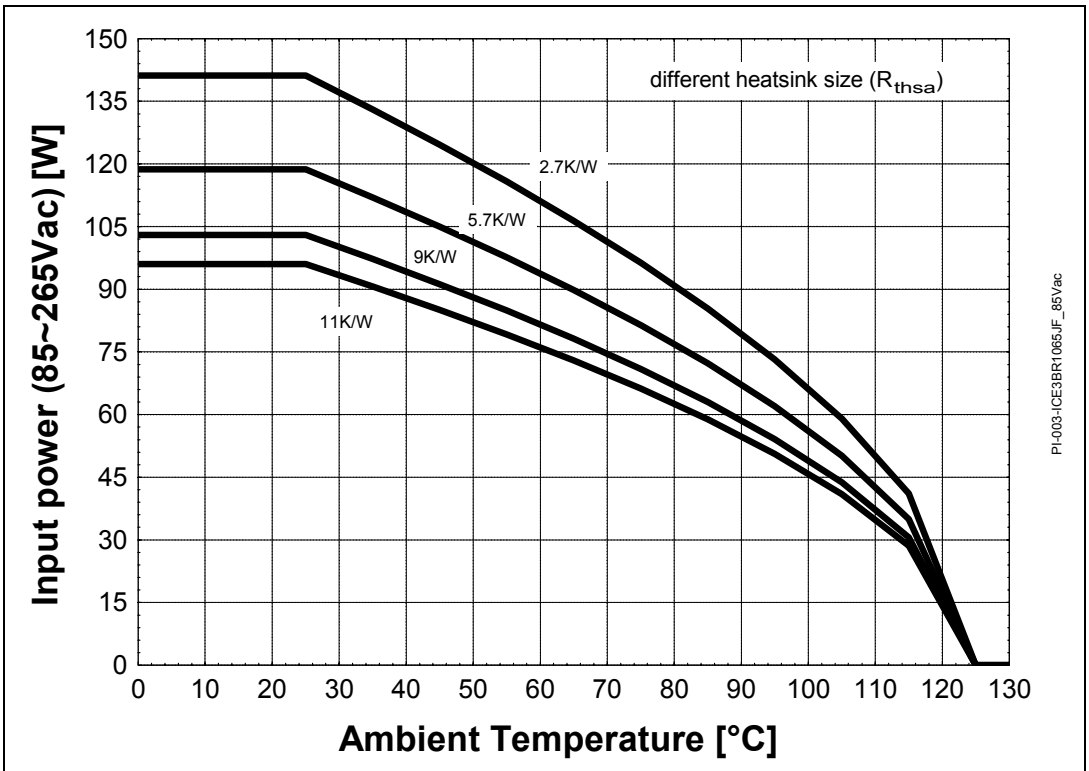


ICE3BR0665JF : Vin=85Vac~265Vac

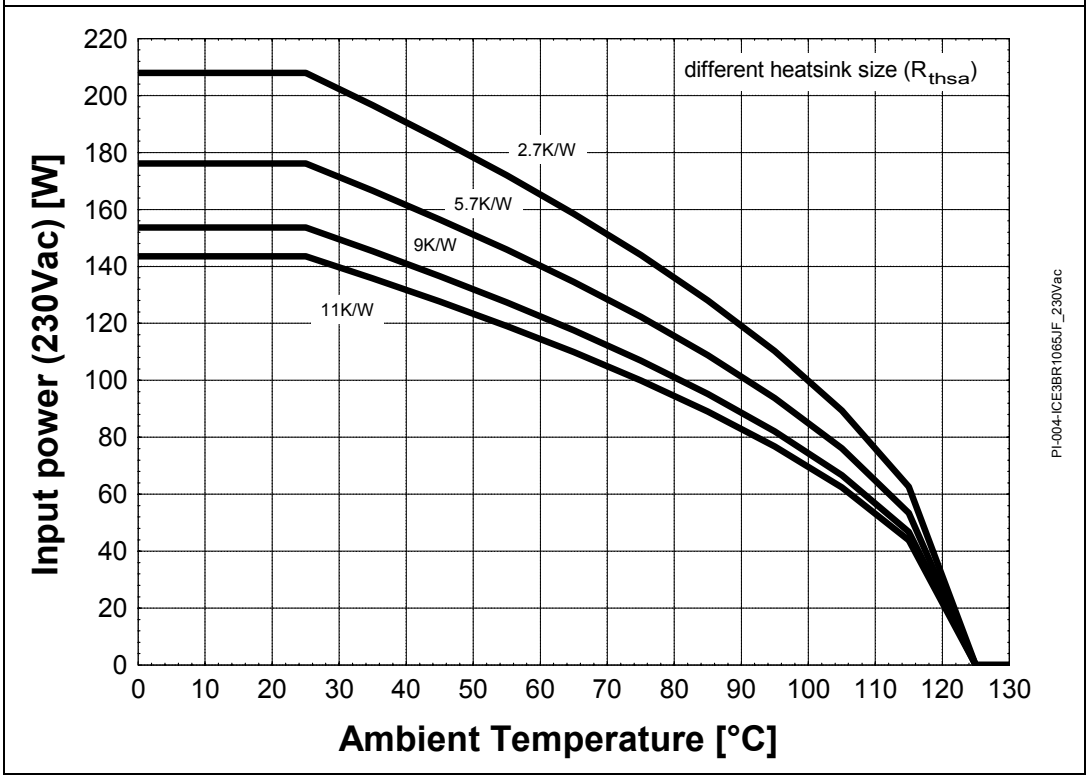


ICE3BR0665JF : Vin=230Vac±15%

Figure 17 Input power curve for ICE3BR0665JF

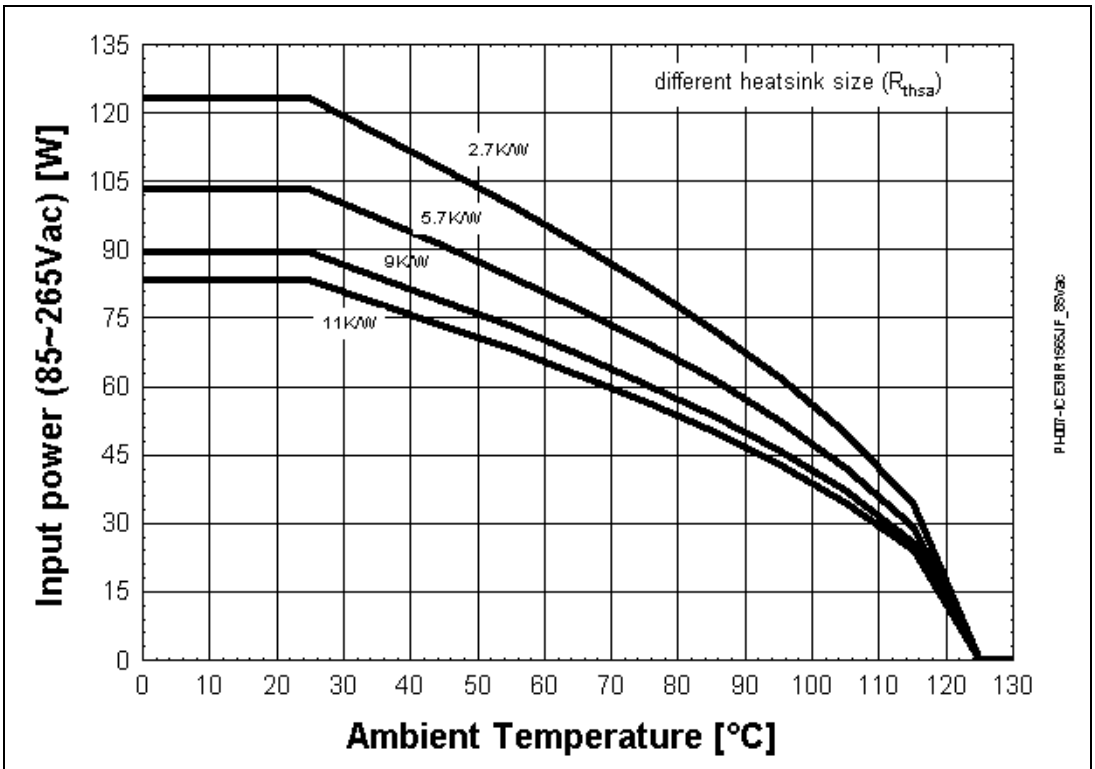


ICE3BR1065JF : Vin=85Vac~265Vac

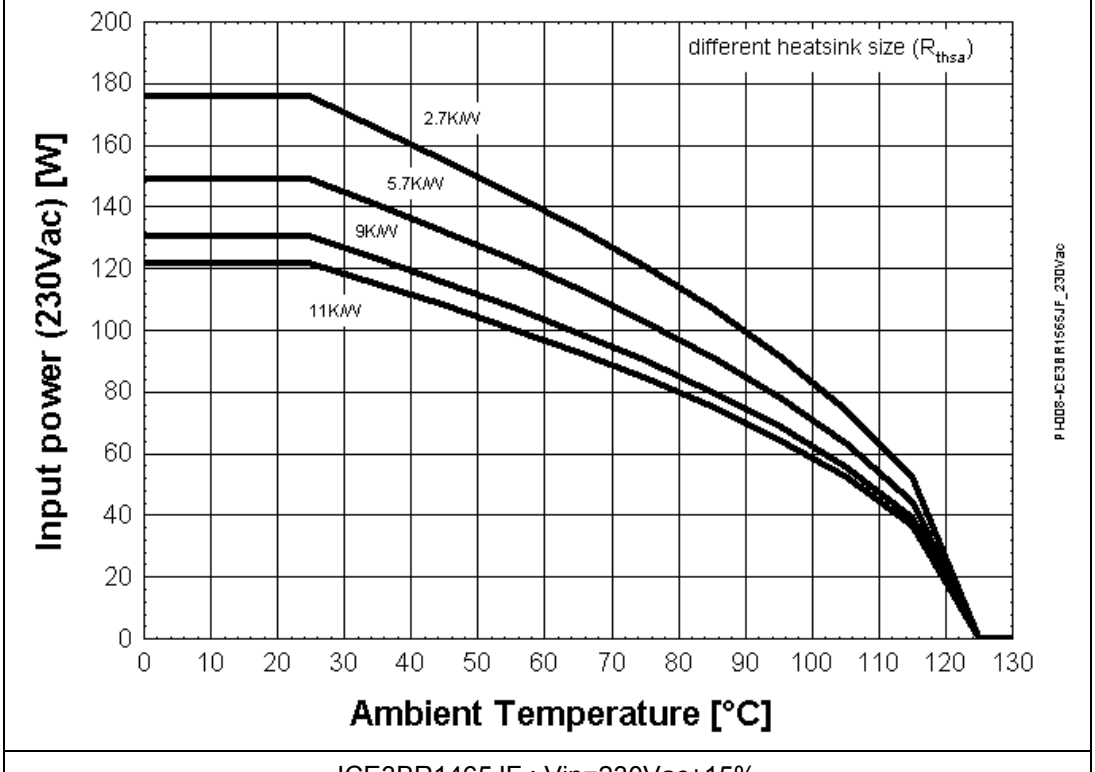


ICE3BR1065JF : Vin=230Vac±15%

Figure 18 Input power curve for ICE3BR1065JF



ICE3BR1465JF : Vin=85Vac~265Vac



ICE3BR1465JF : Vin=230Vac±15%

Figure 19 Input power curve for ICE3BR1465JF

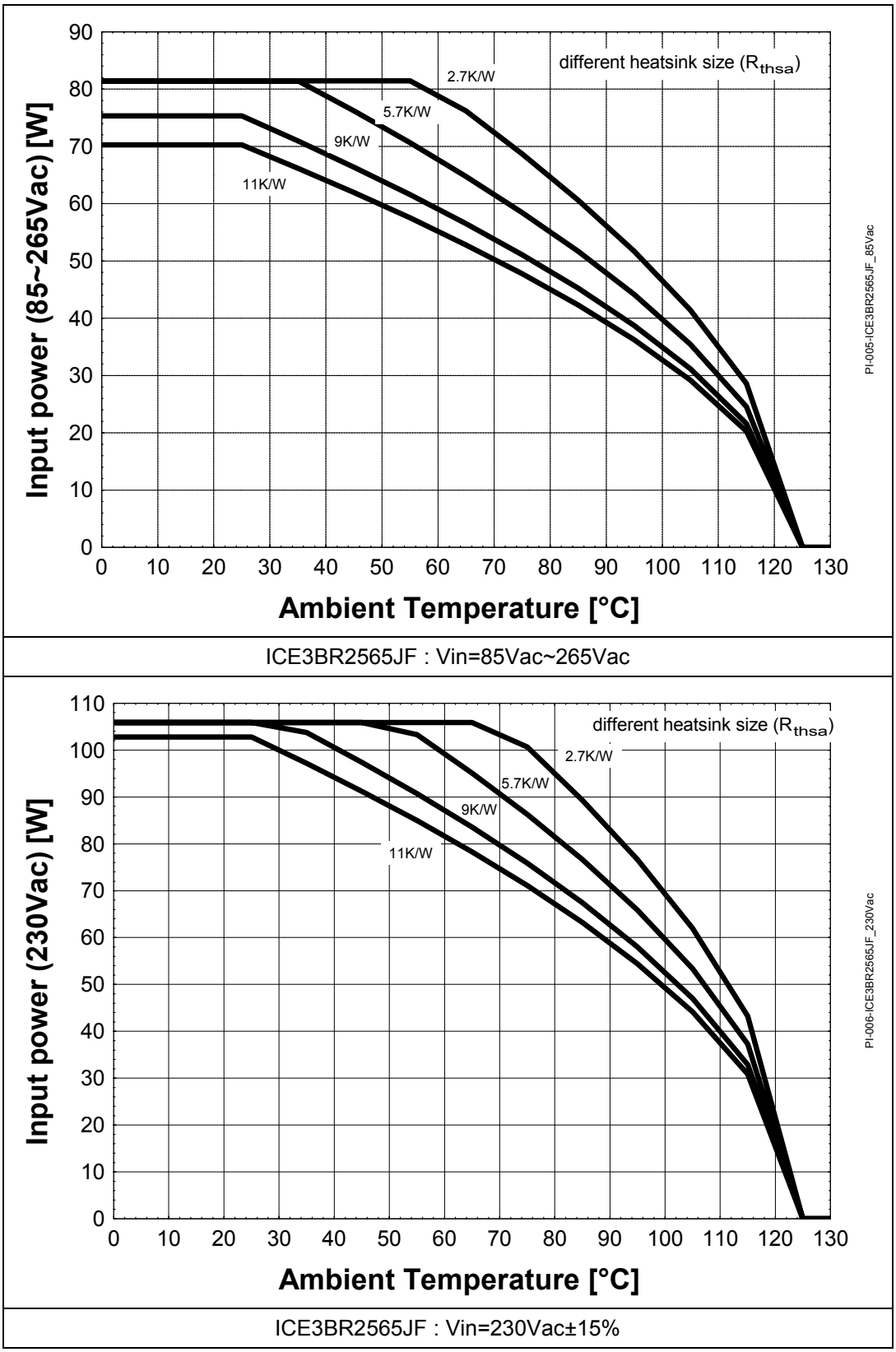


Figure 20 Input power curve for ICE3BR2565JF

8 Layout Recommendation

In order to get the optimized ruggedness of the IC to the transient surge events like ESD and lightning Surge test, the grounding of the PCB layout must be connected carefully. From the circuit diagram in Figure 3, it indicates that the grounding for the controller can be split into several groups; signal ground, Vcc ground, Current sense resistor ground and EMI return ground. All the split grounds should be "star" connected to the bulk capacitor ground directly. The split grounds are described as below.

- Signal ground includes all small signal grounds connecting to the controller GND pin such as filter capacitor ground, C5, C7, C8 and opto-coupler ground.
- Vcc ground includes the Vcc capacitor ground, C6 and the auxiliary winding ground, pin 2 of the power transformer.
- Current Sense resistor ground includes current sense resistor R3 and R4.
- EMI return ground includes Y capacitor, CY1.

9 Product Portfolio of CoolSET®-F3R(FullPak) new Jitter version

Device	Package	V_{DS}	Frequency / kHz	R_{dson} /Ω[1]	P_{in} max. @ 85-265Vac [2]	P_{in} max. @ 230Vac±15% [2]
ICE3BR0665JF	PG-TO220-6-347	650V	67	0.59	173W	259W
ICE3BR1065JF	PG-TO220-6-247	650V	67	1.00	120W	178W
ICE3BR1465JF	PG-TO220-6-247	650V	67	1.44	104W	150W
ICE3BR2565JF	PG-TO220-6-247	650V	67	2.56	81W	106W

10 Useful formula for the SMPS design

Transformer calculation (DCM flyback)	
Input data	V_{in_min} = 90Vdc, V_{in_max} = 380Vdc, V_{ds_max} = 470V for 600V MOSFET, $D_{max} \leq 50\%$
Turn ratio	$N_{ratio} = \frac{V_{ds_max} - V_{in_max}}{V_{out} + V_{diode}}$
Maximum Duty ratio	$D_{max} = \frac{(V_{out} + V_{diode}) \cdot N_{ratio}}{V_{in_min} + (V_{out} + V_{diode}) \cdot N_{ratio}}$
Primary Inductance	$L_p \leq \frac{(V_{in_min} \cdot D_{max})^2}{2 \cdot P_{in} \cdot f_{sw}}$
Primary peak current	$I_{p_max} = \frac{V_{in_min} \cdot D_{max}}{L_p \cdot f_{sw}}$

[1] Typ @ 25°C

[2] Calculated maximum input power rating at T_a=50°C, T_j=125°C and R_{thSA} (external heatsink)=2.7K/W. Refer to the data sheet for input power curve of other T_a

Primary turns	$N_p \geq \frac{I_{p_\max} \cdot L_p}{B_{\max} \cdot A_{\min}}$
Secondary turns	$N_s = \frac{N_p}{N_{ratio}}$
Auxiliary turns	$N_{aux} = \frac{V_{cc} + V_{diode}}{V_{out} + V_{diode}} \cdot N_s$

ICE3BRxx65JF external component Design	
Current sense resistor	$R_{sense} \leq \frac{V_{csth}}{I_{p_\max}}$
Soft start time	$t_{ss} = 20ms$
Vcc capacitor	$C_{VCC} = \frac{I_{VCC\sup 2} \times t_{ss}}{V_{VCChys}} \times \frac{2}{3}$
Startup delay time	$t_{DELAY} = \frac{V_{VCCon} \times C_{Vcc}}{I_{VCCcharge2} - I_{VCCstart}}$
Enter burst mode power	$P_{BURST_enter} = 0.5 \times L_P \times (\frac{V_{FBC5} - V_{Offset-Ramp}}{R_{sense} \times A_V})^2 \times f_{SW}$
Leave burst mode power	$P_{burst_\max} = 0.5 \times L_P \times (0.26 \times I_{p_\max})^2 \times f_{SW}$
Output ripple during burst mode	$V_{out_ripple_pp} = \frac{R_{opto}}{R_{FB} \times G_{opto} \times G_{TL431}} \times \Delta V_{FB}$
Voltage drop when leave burst mode	$V_{out_drop_\max} = \frac{1.15 \times R_{opto}}{R_{FB} \times G_{opto} \times G_{TL431}}$
Total blanking time for over load protection	$t_{blanking} = 20ms + \frac{(4.0 - 0.9) \times C_{BK}}{I_{BK}}$

11 References

[1] Infineon Technologies, Datasheet “CoolSET®-F3R ICE3BR2565JF Off-Line SMPS Current Mode Controller with Integrated 650V CoolMOS® and Startup Cell (Frequency Jitter Mode) in FullPak”

[2] Infineon Technologies, Datasheet “CoolSET®-F3R ICE3BR1465JF Off-Line SMPS Current Mode Controller with Integrated 650V CoolMOS® and Startup Cell (Frequency Jitter Mode) in FullPak”

[3] Infineon Technologies, Datasheet “CoolSET®-F3R ICE3BR1065JF Off-Line SMPS Current Mode Controller with Integrated 650V CoolMOS® and Startup Cell (Frequency Jitter Mode) in FullPak”

[4] Infineon Technologies, Datasheet “CoolSET®-F3R ICE3BR0665JF Off-Line SMPS Current Mode Controller with Integrated 650V CoolMOS® and Startup Cell (Frequency Jitter Mode) in FullPak”

[5] Eric Kok Siu Kam, Kyaw Zin Min, Infineon Technologies, Application Note “AN-EVALSF3R-ICE3BR0665JF, 100W 18.0V SMPS Evaluation Board with CoolSET®-F3R ICE3BR0665JF”

[6] Eric Kok Siu Kam, Kyaw Zin Min, Infineon Technologies, Application Note “AN-EVALSF3R-ICE3BR2565JF, 40W 18.0V SMPS Evaluation Board with CoolSET®-F3R ICE3BR2565JF”

[7] Harald Zoellinger, Rainer Kling, Infineon Technologies, Application Note “AN-SMPS-ICE2xXXX-1, CoolSET® ICE2xXXXX for Off-Line Switching Mode Power supply (SMPS)”