ICE3Bxx65J(G)

CoolSET® F3 Jitter Version Design Guide (DIP-8 & DSO - 16/12)

About this document

The CoolSET® - F3 (jitter version), ICE3Bxx65J(G) is the further development of the third generation CoolSET® - F3 with a frequency jitter feature for better EMI and BiCMOS technology to provide a wider Vcc operating range and a lower controller power consumption. The switching frequency is running at 67 kHz and it targets for DVD player, set-top box, portable game console, white goods, smart meter, auxiliary power supply for server/PC, etc.

This application note provides detail functional description of the new features. The description of all other functions, and calculations are shown in the datasheet as well as in the application note “AN-PS0076”.

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1 Features

650 V Avalanche rugged CoolMOS® with built in startup cell
Active burst mode for lowest standby power at light load controlled by feedback signal
Fast load jump response in active burst mode
67 kHz fixed switching frequency
Auto restart mode for overtemperature detection
Auto restart mode for overvoltage detection
Auto restart mode for overload and open loop
Auto restart mode for VCC undervoltage
User defined soft start
Minimum of external components required
Max. duty dycle 75%
Overall tolerance of current limiting < ±5%
Internal leading edge blanking
BiCMOS technology provides wide VCC range
Frequency jittering for low EMI

2 Package

The package for F3 (jitter version) ICE3Bxx65J product is DIP-8.

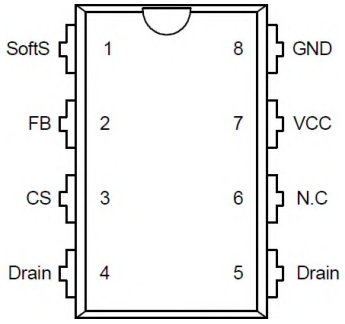


Figure 1 Pin configuration - ICE3Bxx65J

Pin	Name	Description
1	SoftS	Soft start
2	FB	Feedback
3	CS	Current sense/650 V CoolMOS® source
4	Drain	650 V[1] CoolMOS® Drain
5	Drain	650 V[1] CoolMOS® Drain
6	N.C.	Not connected
8	GND	Controller ground

The package for F3 (jitter version) ICE3Bxx65JG product is DSO-16/12.

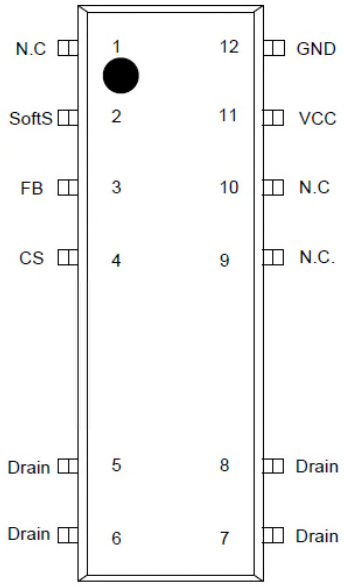


Figure 2 Pin configuration - ICE3Bxx65J

Pin	Name	Description
1	N.C.	Not connected
2	SoftS	Soft start
3	FB	Feedback
4	CS	Current sense/650 V CoolMOS® source
5	Drain	650 V[1] CoolMOS® Drain
6	Drain	650 V[1] CoolMOS® Drain
7	Drain	650 V[1] CoolMOS® Drain
8	Drain	650 V[1] CoolMOS® Drain
9	N.C.	Not connected
10	N.C.	Not connected
11	VCC	Controller supply voltage
12	GND	Controller ground

3 Block diagram

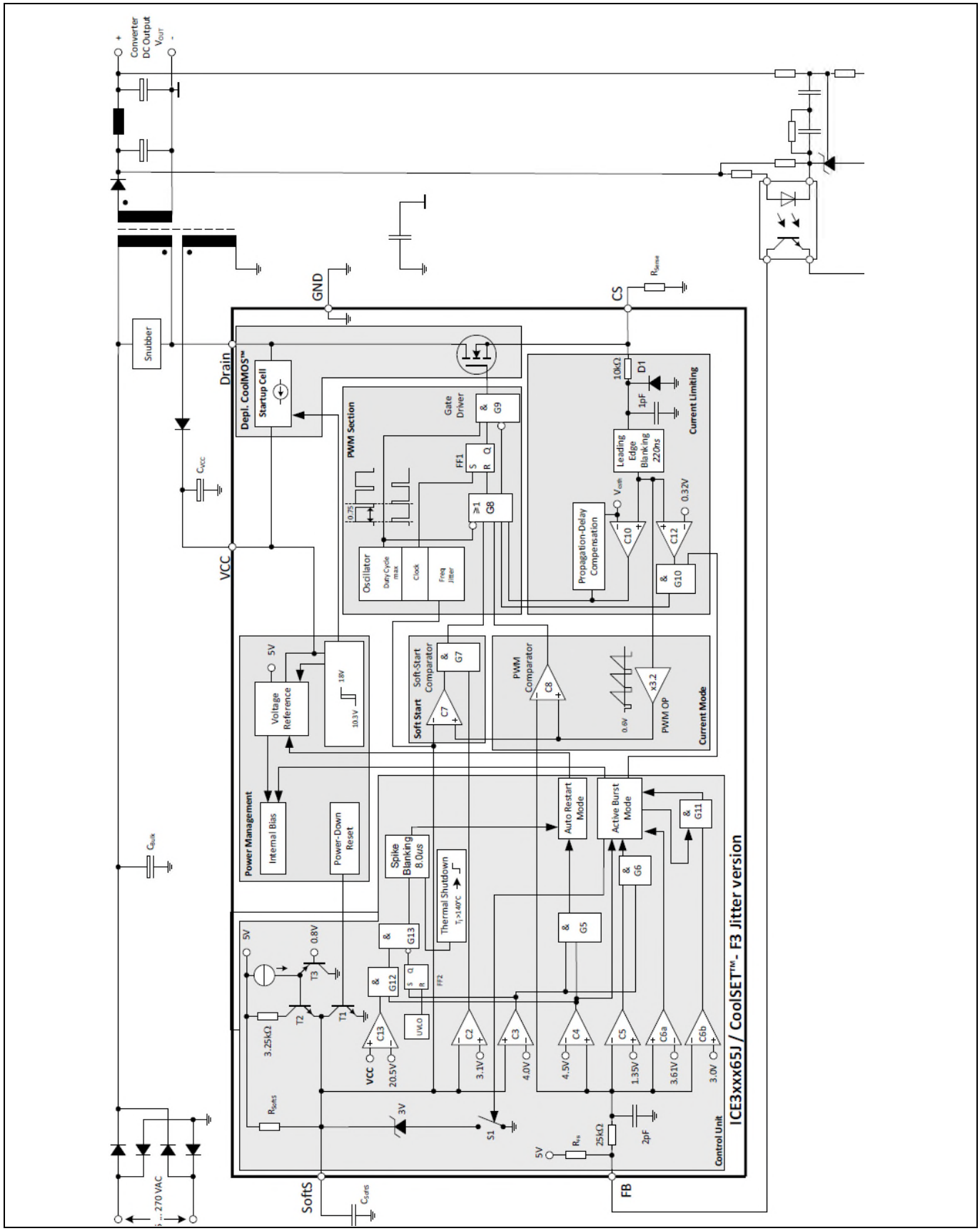


Figure 3 Block diagram of ICE3Bxx65J(G)

4 Typical application circuit

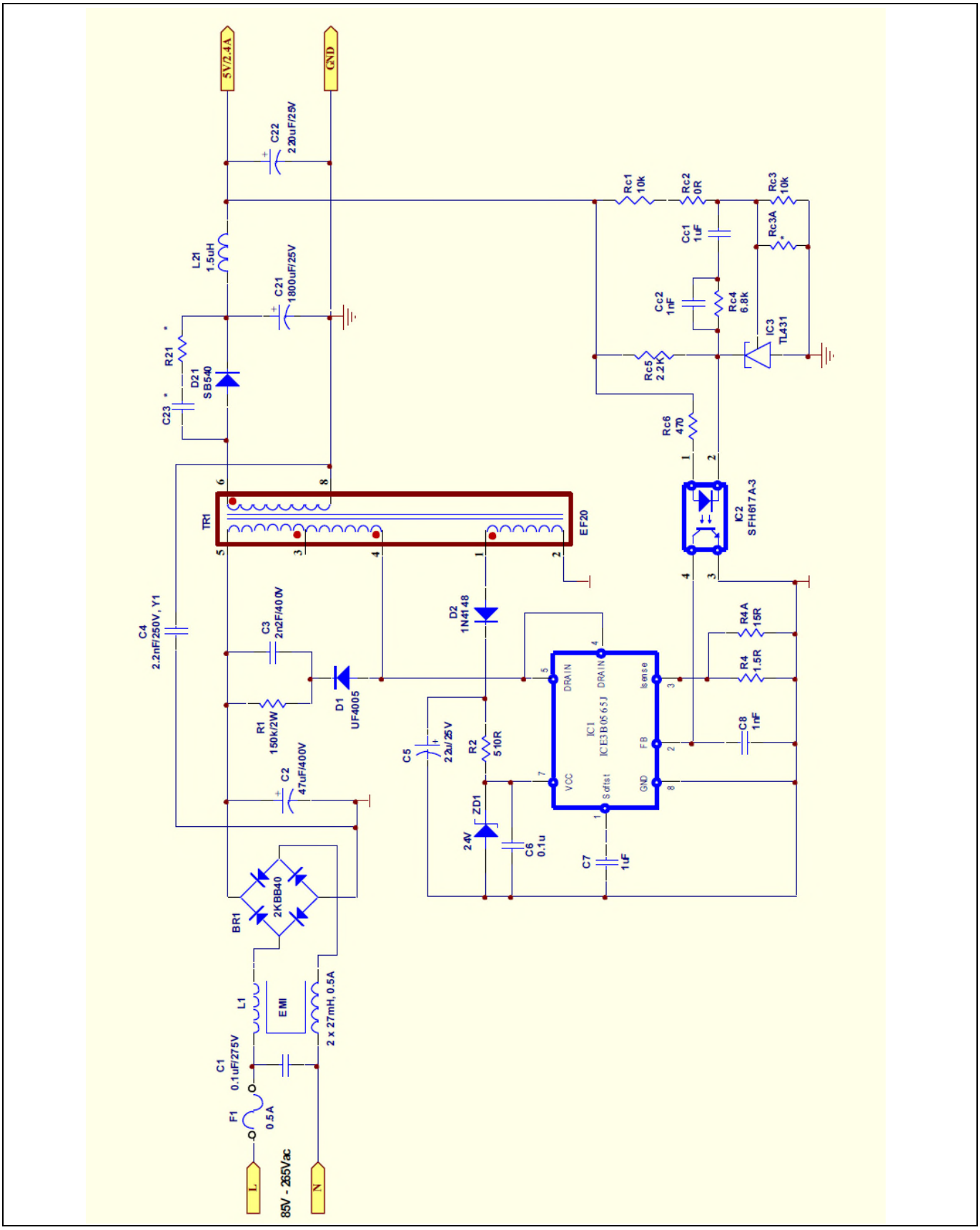


Figure 4 Typical application circuit with ICE3B0565J 12 W 5 V

5 Functional description and component design

5.1 Startup time

Startup time is counted from applying input voltage to IC turn on. ICE3Bxx65J(G) has a startup cell, which is connected to input bulk capacitor. When there is input voltage, the startup cell will act as a constant current source to charge up the Vcc capacitor and supply energy to the IC. When the Vcc capacitor reaches the Vcc_on threshold 18 V, the IC turns on. Then the startup cell is turned off and the Vcc is supplied by the auxiliary winding. Start up time is independent from the AC line input voltage and it can be calculated by the equation (1). Figure 5 shows the start up time of 85 Vac line input.

$$t_{StartUp} = \frac{V_{VCCon} \times C_{VCC}}{I_{VCCcharge}} \quad (1)$$

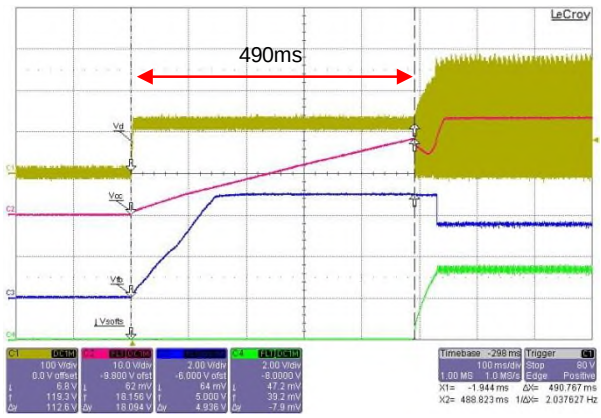
Where:

$I_{VCCcharge}$: 0.965 mA (average current of $I_{VCCcharge2}$ and $I_{VCCcharge3}$)

V_{VCCon} : IC turns on threshold (18 V)

C_{VCC} : Vcc capacitor

Please refer to the datasheet for the symbol used in the equation.



Channel 1; C1 : Drain voltage (V_D)
Channel 2; C2 : Supply voltage (V_{CC})
Channel 3; C3 : Feedback voltage (V_{FB})
Channel 4; C4 : Soft start voltage (V_{SoftS})

Measured startup time = 490 ms

Start-up at 85 Vac and max. load

Figure 5 The start-up time at AC line input voltage of 85 Vac

Note: For a typical application, start up should be VCC ramps up first, other pin (such as FB pin) voltage will follow VCC voltage to ramp up. It is recommended not to have any voltage on other pins (such as FB; SoftS and CS) before VCC ramps up.

5.2 Soft start

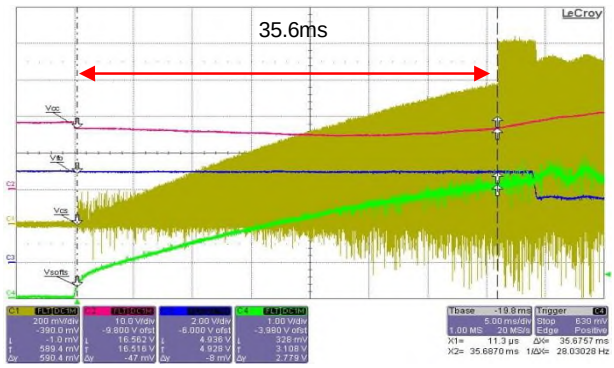
When the IC is turned on after the start-up time, the soft start capacitor at pin1, C_{SoftS} is immediately charged up to approximately 0.8 V and from this point IC starts switching. The soft start voltage V_{SoftS} is generated by C_{SoftS} and the internal pull up resistor R_{SoftS}. The duty cycle of the gate drive is determined by the V_{SoftS} during the soft start phase, which is terminated when V_{Softs} reaches 3.1 V. Afterward, IC goes into normal mode and the duty cycle is dependent on the FB signal. The duration of the soft start can be estimated by the equation (2). Figure 6 shows the soft start behaviour at 85 VAC input and full load. It can be seen that the primary peak current follows V_{SST} voltage and slowly increase to the maximum. The soft start time is approximately 35.6 ms.

$$t_{SS} = C_{Softs} \times R_{Softs} \times \ln\frac{5-0.8}{5-3.1} = 0.793 \times C_{Softs} \times R_{Softs} \quad (2)$$

Where:

R_{softs} : Internal soft start resistor (45 kΩ)

C_{softs} : Soft start capacitor



Channel 1; C1 : Current sense voltage (VCS)
Channel 2; C2 : Supply voltage (VCC)
Channel 3; C3 : Feedback voltage (VFB)
Channel 4; C4 : Soft start voltage (VSoftS)

Soft start time = 35.6 ms

Soft start at Vin = 85 Vac and max. load

Figure 6 FSoft start at AC line input voltage of 85 Vac and full load

5.2.1 Vcc capacitor

The minimum value of the Vcc capacitor is determined by voltage drop during the soft start time. The formula is expressed in equation (3).

$$C_{VCC} = \frac{I_{VCCsup_g_max} \times t_{SS}}{V_{VCChys}} \times \frac{2}{3} \quad (3)$$

Where:

$I_{VCCsup_g_max}$: Supply current with active gate (3.6 mA)

t_{ss} : Soft start time (35.6 ms)

V_{CChys} : Vcc turn-on/off hysteresis voltage (7.7 V)

Therefore, the minimum Vcc capacitance can be 11.09 µF. In order to give more margins, 2 2uF is taken for the design. The startup time $t_{StartUp}$ is then 0.41 s. The measured start up time is 0.49 s (Figure 5). A 0.1 uF filtering capacitor is always needed to add as near as possible to the Vcc pin to filter the high frequency noise.

5.3 Low standby power - Active burst mode

The IC enters active burst mode function at light load condition which enables the system to achieve the lowest standby power requirement of less than 100 mW. Active Burst Mode means the IC is always in the active state and can therefore immediately response to any changes on the FB signal, V_{FB}.

5.3.1 Entering active burst mode

Because of the current mode control scheme, the feedback voltage V_{FB} actually controls the power delivery to output. When the output load is getting lower, the feedback voltage V_{FB} drops. If it stays below 1.35 V for a timeframe set by the blanking time, the IC enters into the burst mode operation. The threshold power to enter burst mode is:

$$P_{burst_enter} = \frac{1}{2} \times L_P \times \left(\frac{V_{FBC5} - V_{Max-Ramp}}{A_V \times R_{CS}}\right)^2 \times f_s \quad (4)$$

Where:

L_p : Transformer primary inductance

V_{FBC5} : Feedback level to enter burst mode (1.35 V)

$V_{Max-Ramp}$: Voltage ramp offset (0.6 V)

f_s : Switching frequency

A_V : PWM OP gain (3.2)

R_{CS} : Current sense resistor

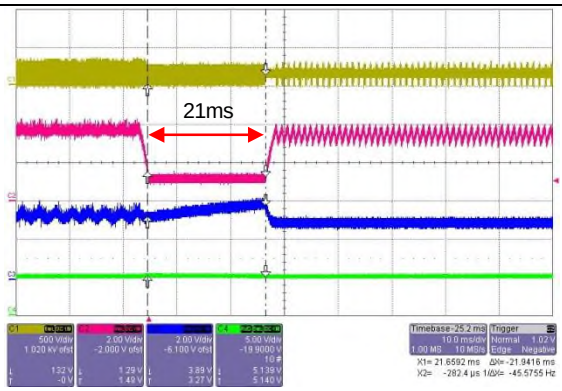
Figure 7 shows the waveform with the load drops from nominal load to light load. After the 21 ms blanking time IC goes into burst mode. The blanking time to enter burst mode is:

$$t_{blanking} = C_{SoftS} \times R_{SoftS} \times \ln\frac{5-3.4}{5-4} = 0.47 \times C_{SoftS} \times R_{SoftS} \quad (5)$$

Where:

R_{softs} : Internal soft start resistor (45 kΩ)

C_{softs} : Soft start capacitor



Channel 1; C1 : Drain voltage (V_D)
Channel 2; C2 : Feedback voltage (V_{FB})
Channel 3; C3 : Soft start voltage (V_{SoftS})
Channel 4; C4 : Output voltage (Vo)

Entering active burst mode with blanking time when load changes from full to light at Vin = 85 Vac

Figure 7 Enterning active burst mode

5.3.2 Working in active burst mode

In the active burst mode, the IC is constantly monitoring the output voltage by feedback pin, V_{FB}, which controls burst duty cycle and burst frequency. The burst "ON" starts when V_{FB} reaches 3.61 V and it stops when V_{FB} is dropped to 3 V. During burst "ON", the primary current limit is reduced to V_{cs2} (32% of maximum peak current) to reduce the conduction losses and to avoid audible noise. The FB voltage is swinging like a saw tooth between 3 V and 3.61 V. The corresponding secondary output ripple (peak to peak) is controlled to be small. It can be calculated by equation (6).

$$V_{out_ripple_pp} = \frac{R_{opto} \times \Delta V_{fb}}{R_{fb} \times G_{opto} \times G_{TL431}} \quad (6)$$

Where:

R_{opto} : Series resistor with opto-coupler at secondary side (for example, Rc6 in Figure 4)

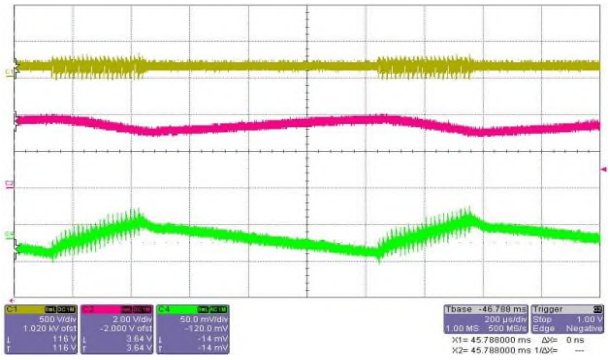
R_{fb} : IC internal pull up resistor connected to FB pin (R_{fb} = 14 kΩ)

G_{opto} : Current transfer gain of opto-coupler

G_{TL431} : Coltage transfer gain of the loop compensation network (for example, Rc1, Rc2, Rc3, Rc4, Rc5, Rc6, Cc1, Cc2 in Figure 4)

ΔV_{fb} : Feedback voltage change (0.61 V)

Figure 8 is the output ripple waveform of the 12 W 5 V demo board. The burst ripple voltage is about 19 mV.



Channel 1; C1 : Drain voltage (V_D)
Channel 2; C2 : Feedback voltage (V_{FB})
Channel 4; C4 : Output ripple voltage ($V_{ripple_pk_pk}$)

$V_{ripple_pk_pk}$ = 60 mV
Probe terminal end with decoupling capacitor of 0.1 uF (ceramic) and 1 uF (electrolytic), 20 MHz filter

Output ripple voltage at 85 Vac and 0.5 W load

Figure 8 Output ripple during active burst mode at light load

5.3.3 Leaving active burst mode

When the output load increases to be higher than the maximum exit level of burst mode, Vout will drop a little and VFB will rise up fast to exceed 4.5 V. The system leaves burst mode immediately when V_{FB} reaches 4.5 V. Once system leaves burst mode, the current sense voltage limit is set to V_{csth} = 1.06 V and the feedback voltage V_{FB} swings back to the normal control level.

The leaving burst power threshold (that is, maximum power to be handled during burst operation) is expressed in equation (7). However, the actual power can be higher as it would include propagation delay time.

$$P_{burst_leave} = 0.5 \times L_P \times \left(\frac{V_{cs2}}{R_{CS}}\right)^2 \times f_s = 0.5 \times L_P \times \left(\frac{V_{cs2}}{V_{csth}} \times \frac{V_{csth}}{R_{CS}}\right)^2 \times f_s = \left(\frac{V_{cs2}}{V_{csth}}\right)^2 \times P_{in_max} \quad (7)$$

Where:

V_{cs2} : Peak current in the burst mode (0.32 V)

V_{csth} : Maximum current limit threshold at CS pin

P_{in_max} : Maximum input power

R_{CS} : Current sense resistor

L_p : Primary inductance of transformer

The leave burst mode timing diagram is shown in Figure 9.

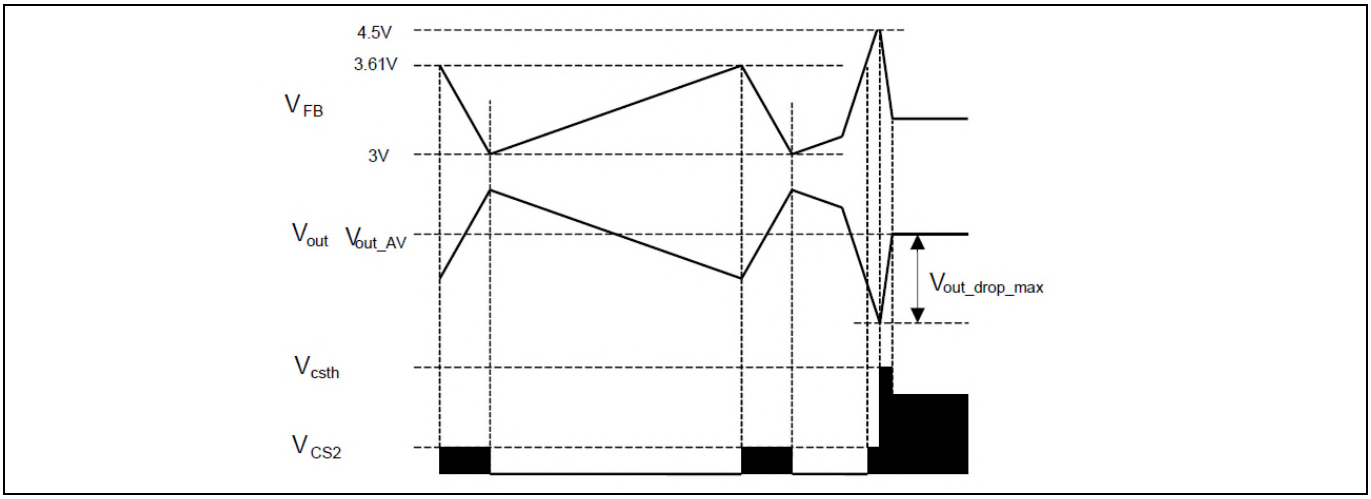


Figure 9 **V_{out_drop} during leaving burst mode**

$$V_{out_drop_max} = \frac{R_{opto}}{R_{fb} \times G_{opto} \times G_{TL431}} \times \left(4.5 - \frac{3.6+3}{2}\right) = \frac{1.2 \times R_{opto}}{R_{fb} \times G_{opto} \times G_{TL431}} \quad (8)$$

Where:

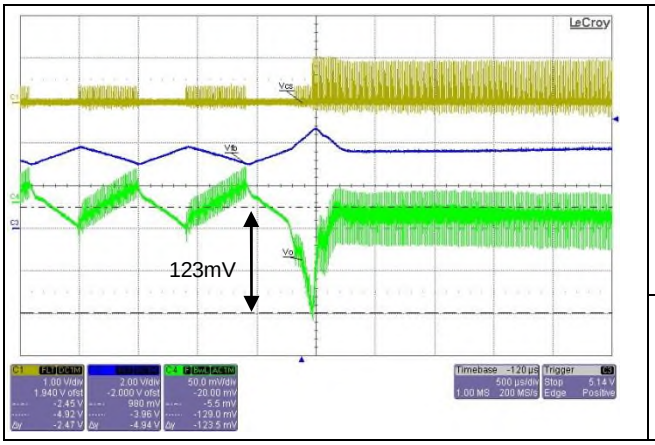
R_{opto} : Series resistor with opto-coupler at secondary side (for example, Rc6 in Figure 4)

R_{fb} : IC internal pull up resistor connected to FB pin (R_{fb} = 14 kΩ)

G_{opto} : Current transfer gain of opto-coupler

G_{TL431} : Voltage transfer gain of the loop compensation network (for example Rc1, Rc2, Rc3, Rc4, Rc5, Rc6, Cc1, Cc2 in Figure 4)

Figure 10 is the captured waveform when there is a load jump from light load to full load. The output ripple drop during the transition is about 123 mV.



Channel 1; C1 : Current sense voltage (V_{CS})
Channel 3; C3 : FB voltage (V_{FBB})
Channel 4; C4 : Output ripple voltage (Vo)

Leaving active burst mode when load change from light to full at Vin = 85 Vac

Figure 10 **Leaving burst mode waveform**

5.3.4 Minimum V_{CC} supply voltage during burst mode

It is particularly important that the Vcc voltage must stay above V_{VCCoff} (that is, 10.3 V). Otherwise, the expected low standby power cannot be achieved. The IC goes into auto-restart mode instead. A reference Vcc circuit is presented in Figure 4. This is for a low cost transformer design where the transformer coupling is not too good. Thus the circuit ZD1 is added to clamp the Vcc voltage exceeding 25.5 V in extreme case such as high load and the Vcc OVP protection is triggered. If the transformer coupling is good, this circuit is not needed.

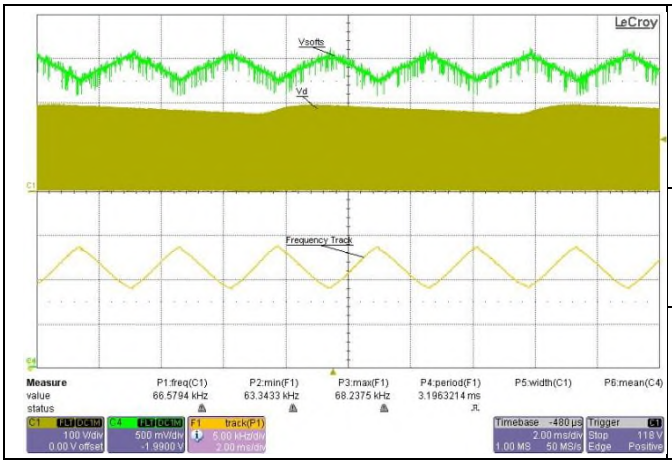
5.4 Low EMI noise

5.4.1 Frequency jittering

The IC is running at a fixed frequency of 67 kHz with jittering frequency of ± 4% (± 2.7 kHz) and adjustable jittering period in a switching modulation period by changing the value of the capacitor, C_{SoftS}. This kind of frequency modulation can effectively help to obtain a low EMI noise level particularly for conducted EMI. The jittering frequency measured for ICE3B0565J is 63 kHz ~ 68 kHz with a jittering period of 3.2 ms which is controlled by C_{SoftS} (refer to Figure 11).

$$T_{FJ} = K_{FJ} \times C_{SoftS} \tag{11}$$

Where: $K_{FJ} = \frac{4ms}{\mu F}$



Channel 1; C1 : Drain voltage (V_D) Channel 4; C4 : Soft start voltage (V_{SoftS}) Channel F1; F1 : Frequency track of drain
Frequency jittering from 63 kHz ~ 68 kHz with a jittering period of 3.2 ms
Frequency jittering at 85 Vac and max. load

Figure 11 Switching frequency jittering

5.4.2 Other suggestions to solve EMI issue

Some more suggestions to improve the EMI performance are listed below.

1. Add RCD clamper circuit to the primary winding of the transformer: RCD clamper circuit (D1, R1, and C3) can absorb the current due to leakage inductance of transformer during switch off time of the MOSFET, so voltage spike of the drain can clamp to desired voltage level and suppress the EMI noise (refer to Figure 4).
2. Add capacitor (C_{DS}) at the drain source pin: C_{DS} can slow down the turn off speed of the MOSFET and the high ΔV/Δt noise will be reduced and so is the EMI noise. The drawback is more energy will be dissipated due to slower turn off speed of MOSFET.
3. Add snubber circuit to the output rectifier: Most of the radiated EMI noise comes out from the output of the system especially for a system with output cable. Adding snubber circuit (R21 and C23) to the output rectifier is a more direct way to suppress those EMI noise (refer to Figure 4).

4. Reduce the reflection voltage: if the secondary to primary reflection voltage is reduced, the switching voltage at drain can also be reduced. Hence the voltage switching noise is reduced and so is the EMI noise. The drawback is the reverse voltage of the secondary rectifier will increase.

5.5 Tight control in maximum power (propagation delay compensation)

The maximum power of the system is changed with the input voltage; higher voltage got higher maximum power. This is due to the propagation delay of the IC and the different rise time of the primary current under different input voltage. The propagation delay time is around 200 ns. But if the primary current rise time is faster, the maximum power increases. The power difference can be as high as > 14% between high line and low line. To make the maximum power control become tight, a propagation delay compensation network is implemented so that the power difference is greatly reduced to best around 2%. Figure 14 shows the compensation scheme of the IC. The equation (10) explains the rate of change of the current sense voltage is directly proportional to the input voltage and current sense resistor. For a DCM operation, the operating range for the dV_{sense}/dt is from 0.1 to 0.7. It can be seen in Figure 12 that higher dV_{sense}/dt gives more compensation; that ism lower value of V_{sense}.

$$\frac{dI_p}{dt} = \frac{V_{in}}{L_p} \Rightarrow R_{sense} \cdot \frac{dI_p}{dt} = R_{sense} \cdot \frac{V_{in}}{L_p} \Rightarrow \frac{dV_{sense}}{dt} = R_{sense} \cdot \frac{V_{in}}{L_p} \quad (10)$$

Where:

I_p : Primary peak current

V_{in} : Input voltage

L_p : Primary inductance of the transformer

V_{sense} : Current sense voltage

R_{sense} : Current sense resistor

This function is limited to discontinuous conduction mode flyback converter only.

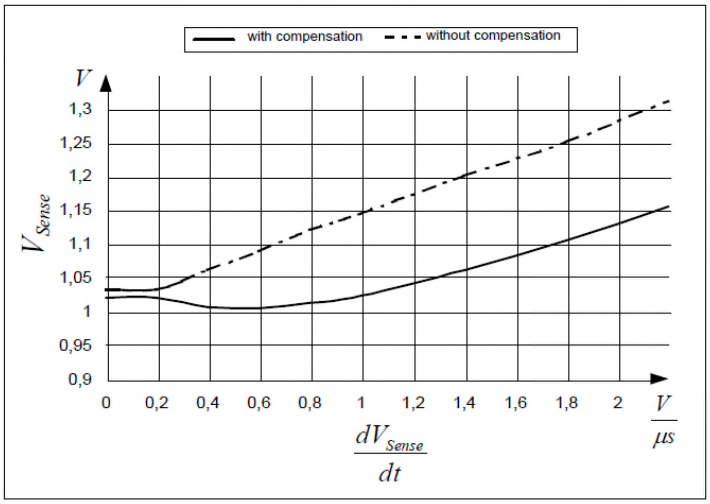


Figure 12 Propagation delay compensation curve

5.6 Protection features

Protection is one of the major factors to determine whether the system is safe and robust. Therefore, sufficient protection is necessary. A list of protections and the failure conditions are shown in the following table.

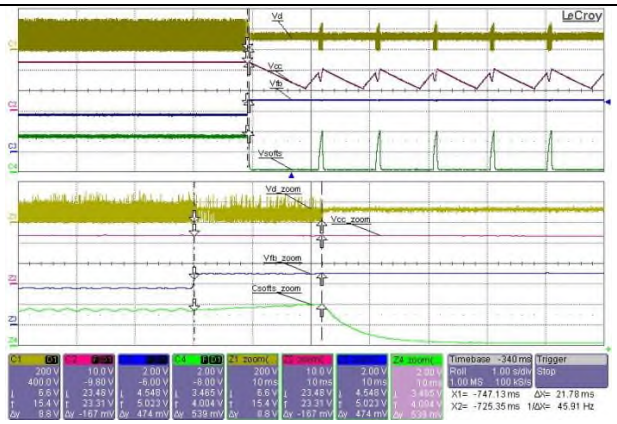
Protection function	Failure condition	Protection mode
Vcc overvoltage	Vcc > 20.5 V and V_{SoftS} < 4 V and V_{FB} > 4.5 V and last for 8 µs	Auto restart mode
Overtemperature (controller junction)	T_J > 140°C and last for 8 µs	Auto restart mode
Overload / Open loop	V_{FB} > 4.5 V and V_{SOFTS} > 4 V (blanking time counted from charging C_{SST} from (3.2 V ~ 3.6 V to 4 V)	Auto restart mode
Vcc undervoltage / short opto-coupler	Vcc < 10.3 V	Auto restart mode

5.6.1 Auto restart protection mode

When the failure condition meets the auto restart protection mode, the IC switches into auto restart. The switching pulse will stop. Then the Vcc voltage will drop. When the Vcc voltage drops to 10.3 V, the startup cell will turn on again. The Vcc voltage is then charged up. When it hits 18 V, the IC turns on and the startup cell turns off. It would then start the startup phase with soft start. After the startup phase the failure condition is checked to determine whether the fault persists. If the fault is removed, it will go to normal operation. Otherwise, the IC repeats the auto restart protection and the switching pulse stop again.

5.6.2 Blanking time for over load protection

The IC controller provides a blanking window before entering into the auto restart mode due to output overload/short circuit. The purpose is to ensure that the system will not enter protection mode unintentionally. The blanking time calculation for overload protection is same as active burst mode blanking window (equation 5).



Channel 1; C1 : Drain voltage (V_D) Channel 2; C2 : Supply voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FB}) Channel 4; C4 : Soft start voltage (V_{SoftS})	
Blanking time = 21 ms	
Over load protection with blanking time a 85 Vac	

Figure 13 Blanking window for over load protection

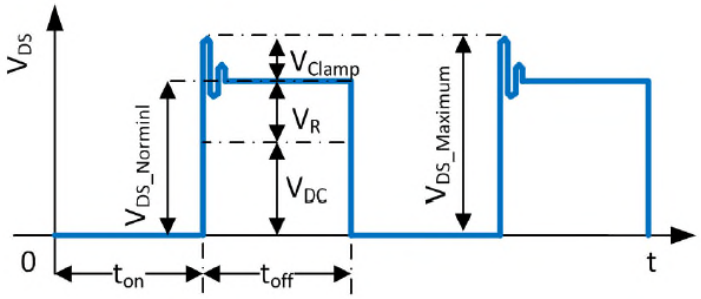
6 Product portfolio of CoolSET®-F3 jitter version (DIP-8 & DSO-16/12)

Device	Package	V_{DS}	Frequency / kHz	R_{dson} /Ω[1]	230Vac±15%[2]	85-265Vac
ICE3B0365J	PG-DIP-8	650 V	67	6.45	22 W	10 W
ICE3B0565J	PG-DIP-8	650 V	67	4.70	25 W	12 W
ICE3B1565J	PG-DIP-8	650 V	67	1.70	42 W	20 W
ICE3B2065J	PG-DIP-8	650 V	67	0.92	57 W	28 W
ICE3B0365JG	PG-DSO-16/12	650 V	67	6.45	22 W	10 W
ICE3B0565JG	PG-DSO-16/12	650 V	67	4.70	25 W	12 W

[1] Typ. at 25°C

[2] Calculated maximum input power rating at T_a = 75°C, T_j = 125°C and without copper area as heat sink.

7 Useful formula for the SMPS design

Transformer (DCM flyback)	
Input data	$V_{DC_min} = 90V$, $V_{DC_max} = 374V$, $V_{DS_norminal} = 450V$ for 600V Mosfet (Reflection voltage, $V_R = V_{DS_norminal} - V_{DC_{max}}$) $D_{max} < 0.50(50\%)$  **Drain to source voltage composition**
Turn ratio	$N_{ratio} = \frac{V_{DS_norminal} - V_{DC_max}}{V_{out} + V_{FDiode}} = \frac{V_R}{V_{out} + V_{FDiode}}$
Duty maximum	$D_{max} = \frac{V_R}{V_R + V_{DC_min}}$
Primary Inductance	$L_P = \frac{(V_{DC_min} \times D_{max})^2}{2 \times P_{in} \times f_s}$
Primary peak current	$I_{P_max} = \frac{V_{DC_min} \times D_{max}}{L_P \times f_s})$
Primary rms current	$I_{P_rms} = I_{P_max} \times \sqrt{\frac{D_{max}}{3}}$
Primary turns	$N_P \geq \frac{I_{P_max} \times L_P}{B_{max} \times A_e}$
Secondary turns	$N_S = \frac{N_P}{N_{ratio}}$
Auxiliary turns	$N_{aux} = \frac{V_{cc} + V_{FDiode}}{V_{out} + V_{FDiode}} \times N_S$
ICE3Bxx65J(G) other components	
Current sense resistor	$R_{CS} \leq \frac{V_{csth}}{I_{P_max}}$
Soft start time	$t_{SS} = C_{SoftS} \times R_{SoftS} \times \ln\frac{5 - 0.8}{5 - 3.1} = 0.793 \times C_{SoftS} \times R_{SoftS}$ $where, R_{SoftS} = 45k\Omega$
Vcc capacitor	$C_{VCC} = \frac{I_{VCCsup_g_max} \times t_{SS}}{V_{VCChys}} \times \frac{2}{3}$

Useful formula for the SMPS design

Startup time	$t_{StartUp} = \frac{V_{VCCon} \times C_{VCC}}{I_{VCCcharge}}$ where, $I_{VCCcharge}$ is the average current of $I_{VCCcharge2}$ and $I_{VCCcharge3}$
Enter burst mode power	$P_{burst_enter} = \frac{1}{2} \times L_P \times \left(\frac{V_{FBC5} - V_{Max-Ramp}}{A_V \times R_{CS}}\right)^2 \times f_s$ where, $V_{FBC5} = 1.35V, A_V = 3.2, f_s = 67kHz, V_{Max-Ramp} = 0.6V$
Output ripple during burst mode	$V_{out_ripple_pp} = \frac{R_{opto} \times \Delta V_{fb}}{R_{fb} \times G_{opto} \times G_{TL431}}$
Leave burst mode power	$P_{burst_leave} = 0.5 \times L_P \times \left(\frac{V_{cs2}}{R_{CS}}\right)^2 \times f_s$ *where,* $V_{cs2} = 0.32V$
Blanking time for over load protection/ active burst mode	$t_{blanking} = C_{SoftS} \times R_{SoftS} \times \ln\frac{5-3.4}{5-4} = 0.47 \times C_{SoftS} \times R_{SoftS}$ *where,* $R_{SoftS} = 45k\Omega$

8 References

[1] Infineon Technologies, Datasheet “CoolSET®-F3(Jitter Version) ICE3Bxx65J Off-Line SMPS Current Mode Controller with Integrated 650V CoolMOS® and Startup Cell in DIP-8”

[2] Infineon Technologies, Datasheet “CoolSET®-F3(Jitter Version) ICE3Bxx65JG Off-Line SMPS Current Mode Controller with Integrated 650V CoolMOS® and Startup Cell in DSO-16/12”

[3] Kok Siu Kam Eric, Jeoh Meng Kiat, Infineon Technologies, Application Note “AN-EVALSF3-ICE3B0565J, 12W 5V SMPS Evaluation Board with CoolSET®-F3 ICE3B0565J”

[4] Kyaw Zin Min, Kok Siu Kam Eric, He Yi, Jeoh Meng Kiat, Infineon Technologies, Application Note “AN-EVALSF3-ICE3B0365J, 5W 2 outputs (5V & 18V) DC/DC SMPS Demo Board with CoolSET®-F3 ICE3B0365J”

Revision history

Document version	Date of release	Description of changes
1.1	2023-03-27	Editorial changes
1.0	2013-03-19	Initial release

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