ICE3Axxx/ICE3Bxxx

CoolSET F3 Design Guide

Power Management & Supply

Never stop thinking.

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Table of Contents Page

1 Introduction 5

2 Block Diagram 6

3 Package 8

4 Typical Application Circuit 9

5 Function Description 10
5.1 Startup Cell 10
5.2 Soft Start and Normal Operation 10
5.3 Active Burst Mode 11
5.3.1 Entering Active Burst Mode 11
5.3.2 Working in Active Burst Mode 12
5.3.3 Leaving Active Burst Mode 13
5.3.4 V_{CC} supply during burst mode 14

6 Protection Features 15
6.1 Auto Restart Mode 15
6.2 Latched Off Mode 15

7 Blanking Window 16

References 17

1 Introduction

The CoolSET™-F3, **ICE3AXXX/ICE3BXXX**, is the further development of the second generation CoolSET™-F2 with some new features. This application note provides detail functional description of these new features. The description of all other functions and calculations are shown in the datasheet as well as in the application note “AN-SMPS-ICE2Axxx”.

A new standby power concept is implemented into the controller to meet the requirements for the lowest Standby Power at minimum load and no load condition. An intelligent Active Burst Mode is used for the Standby Mode. The controller constantly monitors the feedback voltage during Burst Mode which leads to immediate response in case of load jump at the output. Entering and leaving Burst Mode depends on the level of the feedback voltage.

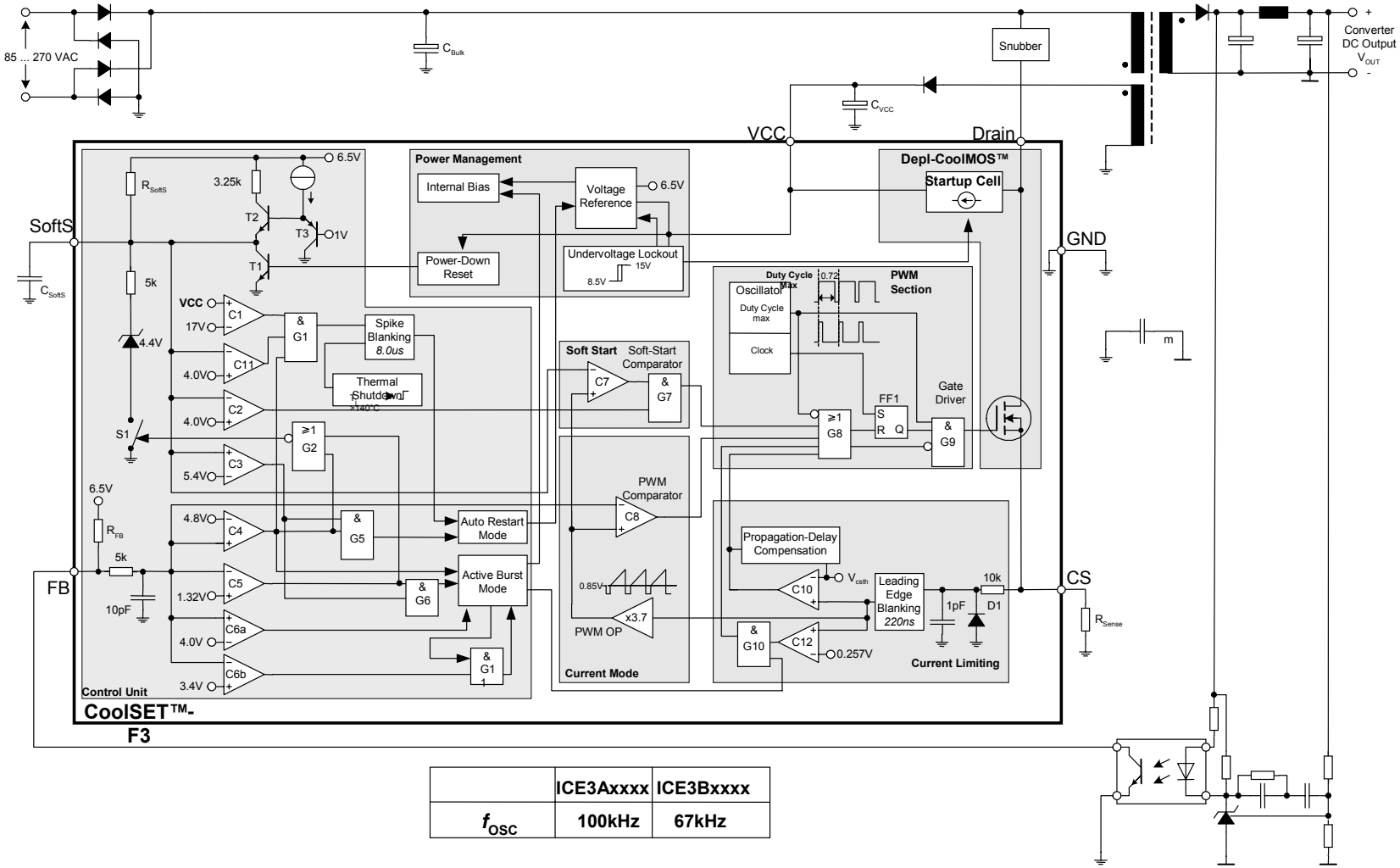
Unlike the CooSET™-F2 which uses an external resistor for startup, the CooSET™-F3 has an integrated startup cell which is connected to high voltage MOSFET Drain. It charges the VCC capacitor when AC is pluged in. the startup cell is switched off once Undervoltage Lockout on-threshold 15V is exceeded. Power losses are therefore reduced. The efficiency under light load condition is increased dramatically.

Auto Restart Mode and Latched Off Mode are implemented in the IC during protection. This feature increase the system’s robustness and safety.

The ICE3AXXX/ICE3BXXX provides a Blanking Window, which delays the activation of the overload protection for a limited time. This allows the IC to support applications which need surge power for a short while (e.g. switching on capacitive load). The Blanking Window is also used to avoid accidentally entering of the Active Burst Mode, which assures the stability of the system in all operating conditions.

In this application note, the IC functions are described in detail and its performance is shown by the results.

2 Block Diagram



	ICE3Axxxx	ICE3Bxxxx
f_{osc}	100kHz	67kHz

Figure 1 Block Diagram of CoolSET™-F3 ICE3XXXX65 (non latached mode)

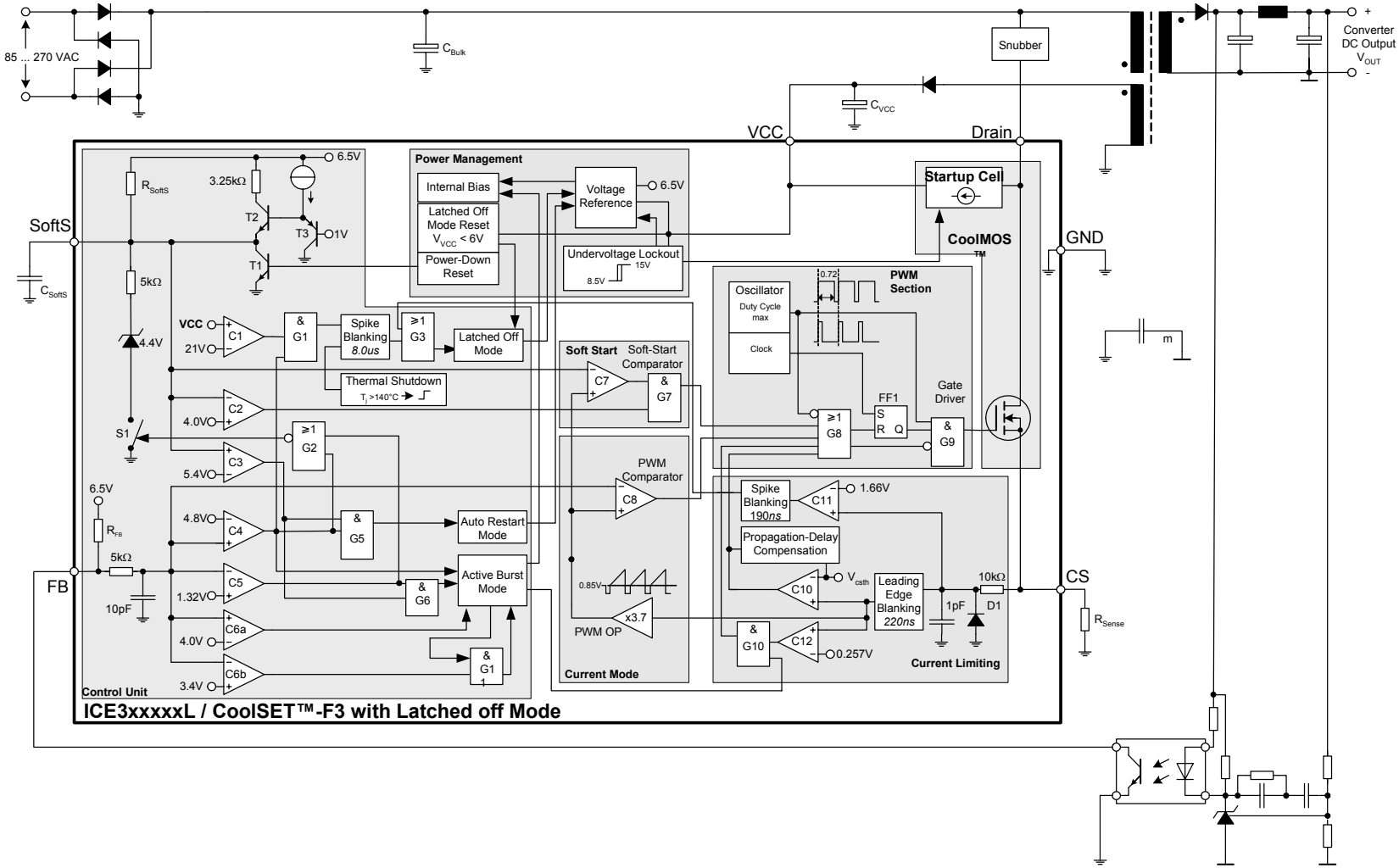
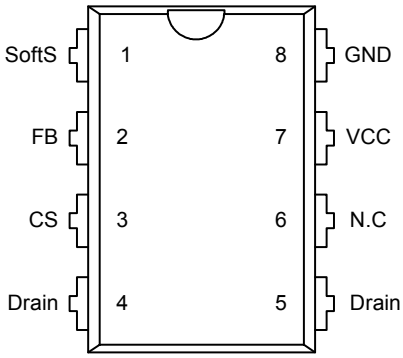


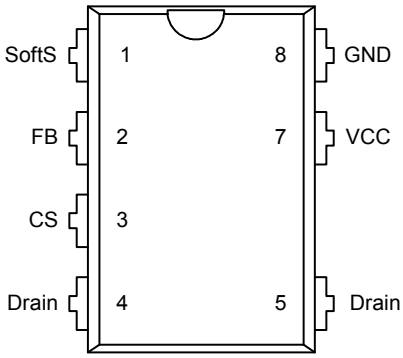
Figure 2 Block Diagram of CoolSET™-F3 ICE3XXXX65L (Latached mode)

3 Package

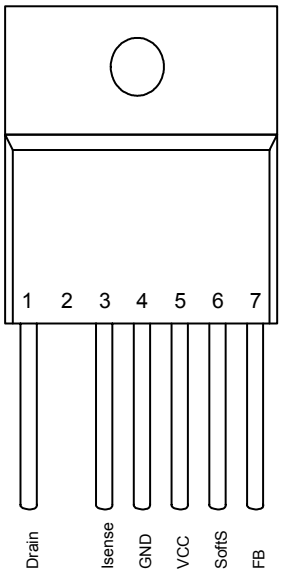
There are four different package for CoolSET™-F3 product, DIP-8, DIP-7, TO-220 and I²-Pak.



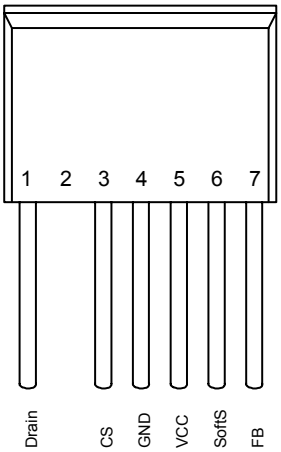
DIP-8



DIP-7



TO-220



I²-Pak

4 Typical Application Circuit

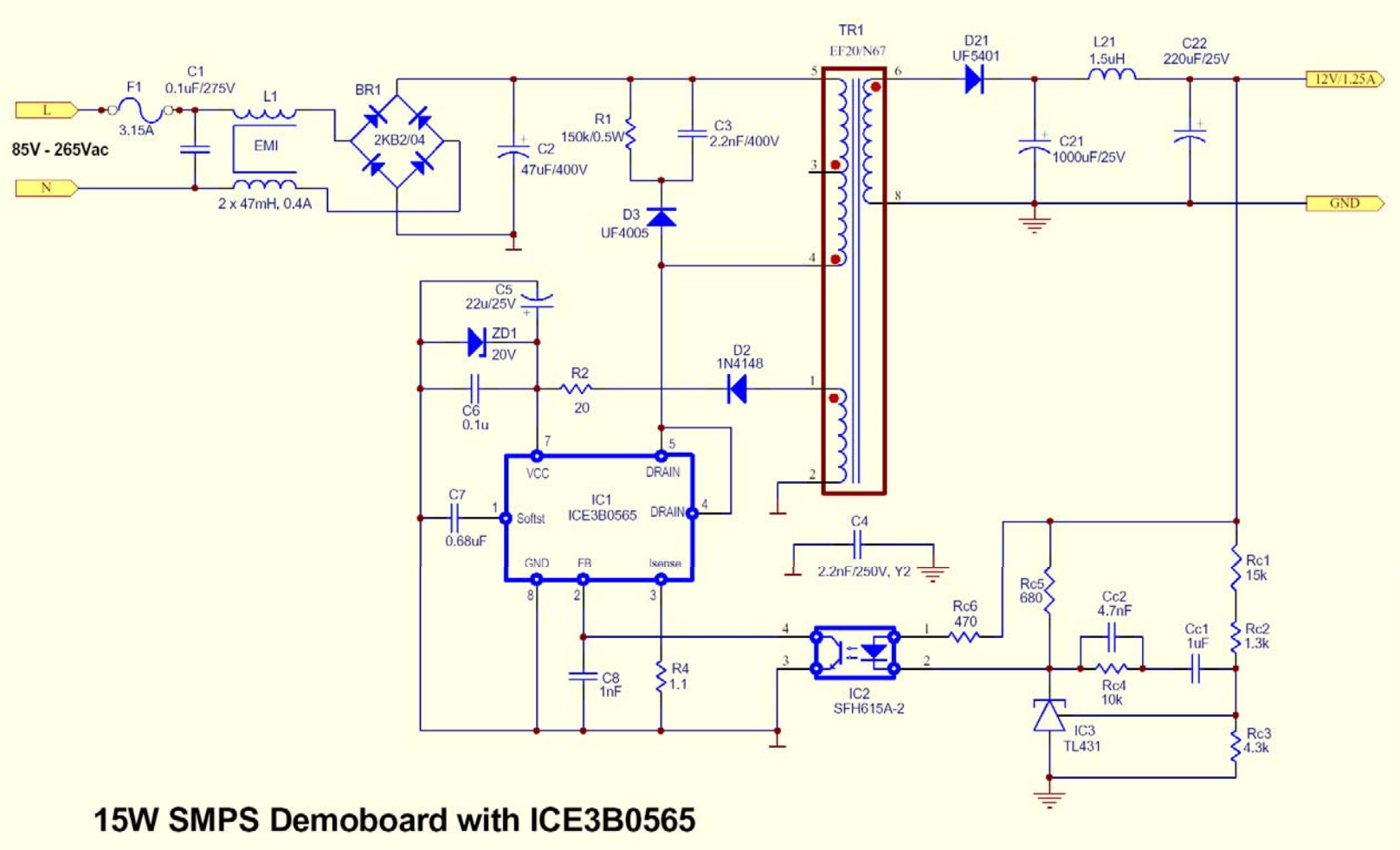


Figure 3 Typical application circuit with CoolSET™-F3, ICE3B0565 15W

5 Function Description

5.1 Startup Cell

The Startup Cell delivers a constant charge current of $I_{VCCCharge}$=1.05mA to charge up the V_{CC} capacitor C_{Vcc} at V_{CC} pin. When V_{CC} exceeds the on-threshold V_{CCon}=15V, the internal reference voltages and bias circuit are switched on and IC blocks start to be operates. The Startup Cell is switched off by UVLO for energy saving. The startup delay time, t_{DELAY}, is independent from the AC line input voltage. It can be estimated by the equation (1):

$$t_{DELAY} = \frac{V_{CCon} \cdot C_{Vcc}}{I_{Vcc_Charge} - I_{Vcc_Start}} \quad (1)$$

where, I_{Vcc_Start} is the supply current when IC is in off state. Figure 4 shows the startup time delay at 85VAC input.

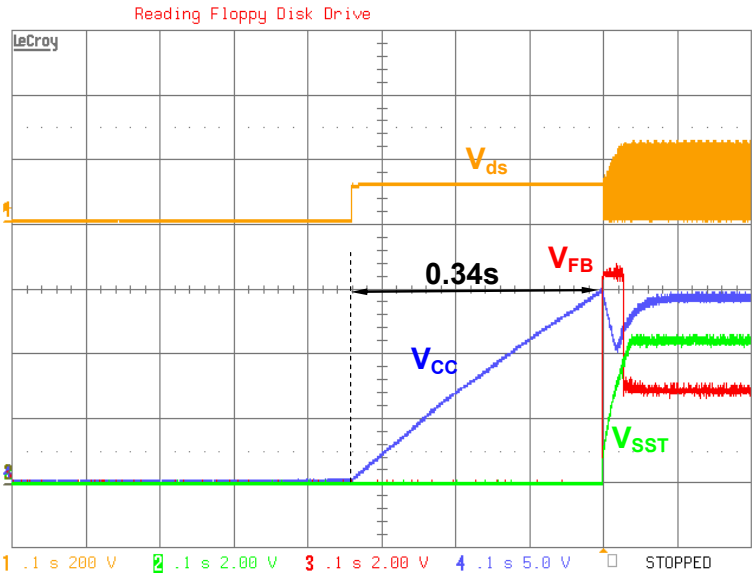


Figure 4 The startup delay time at AC line input voltage of 85V.

Precaution : For a typical application, start up should be VCC ramps up first, other pin (such as FB pin) voltage will follow VCC voltage to ramp up. It is recommended not to have any voltage on other pins (such as FB; BA and CS) before VCC ramps up.

5.2 Soft Start and Normal Operation

When the IC is turned on after the Startup Delay time, the Soft Start capacitor at pin1, C_{SST}, is charged from the initial level of 1V. The Soft Start voltage V_{SOFTS} is generated by C_{SST} and the internal pull up resistor R_{SOFTS}. The duty cycle of the gate drive is determined by the V_{SOFTS} during the Soft Start phase, which is terminated when V_{SOFTS} reaches 4V. Afterward, IC goes into normal mode and the duty cycle is dependent on the FB signal. V_{SOFTS} is internally clamped to 4.4V during normal operation mode. The duration of the Soft Start can be estimated by the equation (2). Figure 5 shows the soft start behaviour at 85VAC input. It can be seen that the primary peak current follows V_{SST} voltage and slowly increase to the maximum. The soft start time is about 32ms.

$$t_{SOFTS} = C_{SST} \times R_{SOFTS} \times \ln\frac{5.5V}{6.5V - 4V} = 0.79 \cdot C_{SST} \cdot R_{SOFTS} \quad (2)$$

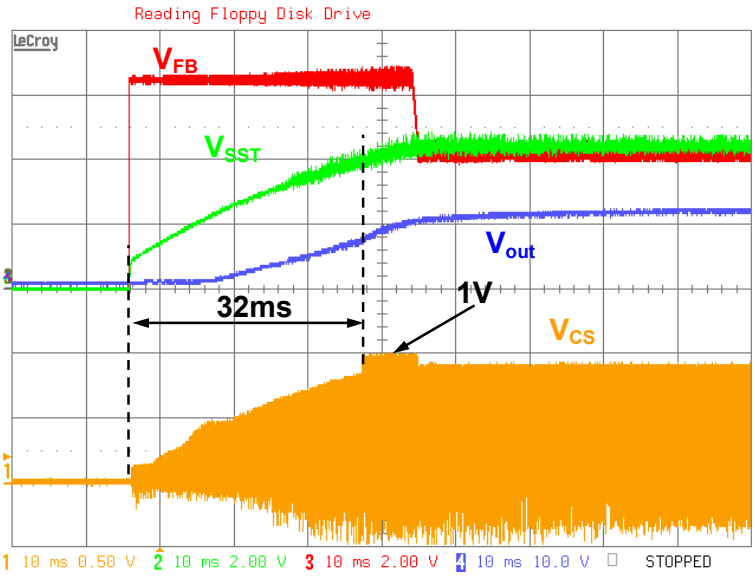


Figure 5 Soft start at AC line input voltage of 85V

After soft start stage, IC goes into normal operation with the conventional primary peak current control scheme. Please refer to “AN-SMPS-ICE2Axxx”.for the details of normal operation.

5.3 Active Burst Mode

The IC provides an Active Burst Mode function at no load or low load conditions to enable the system to achieve the lowest standby power requirement of less than 100mW. Active Burst Mode means the IC is always in the active state and can therefore immediately response to any changes on the FB signal, V_{FB}.

5.3.1 Entering Active Burst Mode

Because of the current mode control scheme, the feedback voltage V_{FB} actually controls the power delivery to output. When the output load is getting lower, the feedback voltage V_{FB} drops. If it stays below 1.32V for a timeframe set by the blanking time, the IC enters into the burst mode operation. The threshold power to enter burst mode is:

$$P_{BURST_enter} = 0.5 \cdot L_P \cdot \left(\frac{V_{FB_burst} - V_{RAMP}}{R_{sense} \cdot A_V}\right)^2 \cdot f_{SW} \quad (3)$$

where, L_P is the transformer primary inductance, V_{FB_burst}=1.32V is the feedback voltage at which the system starts to burst, V_{RAMP}=0.85V is the maximum level of the internal Voltage Ramp on which the amplified current ramp signal of the PWM-OP is superimposed, A_V =3.7 is the internal PWM-OP gain, R_{sense} is the current sense resistor, f_{SW} is the switching frequency. Figure 6 shows the test waveform with the load drop from full load to light load. After blanking time IC goes into burst mode.

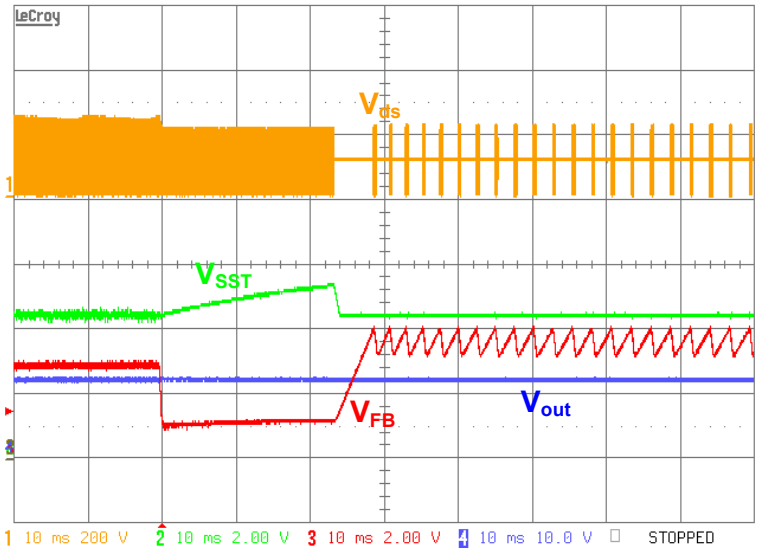


Figure 6 Entering Burst Mode

5.3.2 Working in Active Burst Mode

During active burst mode, the IC is constantly monitoring the output voltage by feedback pin, V_{FB}, which controls burst duty cycle and burst frequency. The burst "on" starts at V_{FB} reaches 4V and stop at V_{FB} is down to 3.4V. During burst "on", the primary current limit is set to only 25% of maximum peak current (V_{CS}=0.25V) to reduce the conduction losses and to avoid audible noise. The FB voltage is changing like a saw tooth between 3.4V and 4V.The corresponding secondary output ripple (peak to peak) is regulated as below:

$$V_{out_ripple_pp} = \frac{R_{opto}}{R_{FB} \cdot G_{opto} \cdot G_{TL431}} \cdot \Delta V_{FB} \quad (4)$$

where, R_{opto} is the resistor series with optocoupler at the secondary to limit the ooptocoupler current, R_{FB} is the IC internal pull up resistor connected to FB Pin, G_{opto} is the current transfer gain of optocoupler, G_{TL431} is the voltage transfer gain between the comparator TL431 output and V_{out}, ΔV_{FB}=4-3.4=0.6V is the ripple on the V_{FB} during burst operation.

The leaving burst power threshold, ie. maximum power to be handled during burst operation is:

$$P_{burst_\max} = 0.5 \cdot L_P \cdot (0.25 \cdot i_{peak_\max})^2 \cdot f_{SW} = 0.5 \cdot L_P \cdot (0.25 \cdot \frac{V_{CS_\max}}{R_{sense}})^2 \cdot f_{SW} = 0.0625 \cdot P_{\max} \quad (5)$$

Where, ipeak_max is the maximum primary peak current, V_{CS_max} is the cycle by cycle current limit threshold at CS Pin, P_{max} is the maximum output power of the power supply. It can be seen that the maximum power in burst mode is around 6.25% of P_{max}. Figure 7 and Figure 8 show the test waveforms of burst mode at no load and light load respectively. It can be seen that the burst ripple is well regulated to be 32mV and it is independent on the output power.

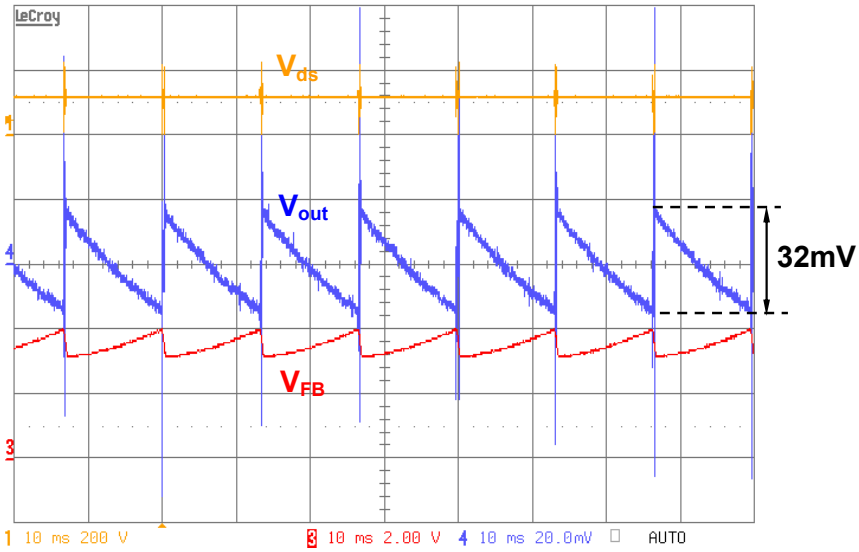


Figure 7 working in Burst Mode at no load

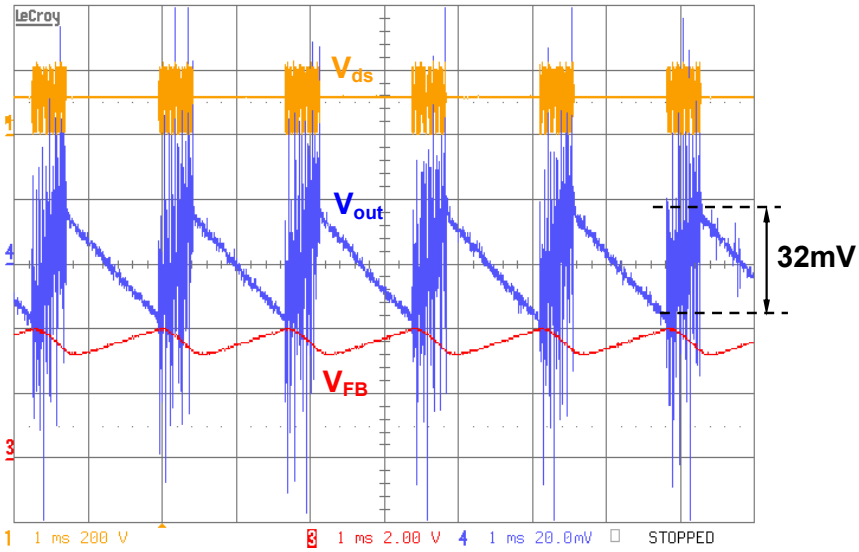


Figure 8 working in Burst Mode at light load

5.3.3 Leaving Active Burst Mode

When the output load is increasing to be higher than P_{burst_max}, Vout will drop a little bit and V_{FB} will rise up fast to 4.8V. The system leaves burst mode immediately when V_{FB} reaches 4.8V. Once system leaves burst mode, the current sense voltage limit, V_{CS_MAX}, is released to 1V, the feedback voltage V_{FB} swings back to the required level. The timing diagram of leaving burst mode is shown in Figure 9.

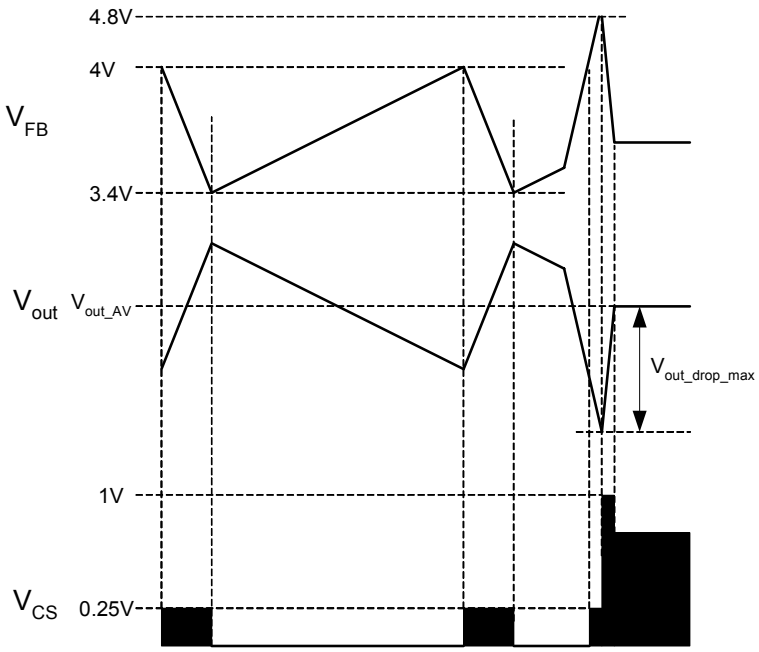


Figure 9 the timing diagram of leaving burst mode

The maximum V_{out} drop during the mode transition is

$$V_{out_drop_max} = \frac{R_{opto}}{R_{FB} \cdot G_{opto} \cdot G_{TL431}} \cdot (4.8 - \frac{3.4+4}{2}) = \frac{1.1 \cdot R_{opto}}{R_{FB} \cdot G_{opto} \cdot G_{TL431}} \quad (6)$$

Figure 10 shows the waveform to leave burst mode with load jump from light load to full load. The output voltage drop during the transition is about 130mV.

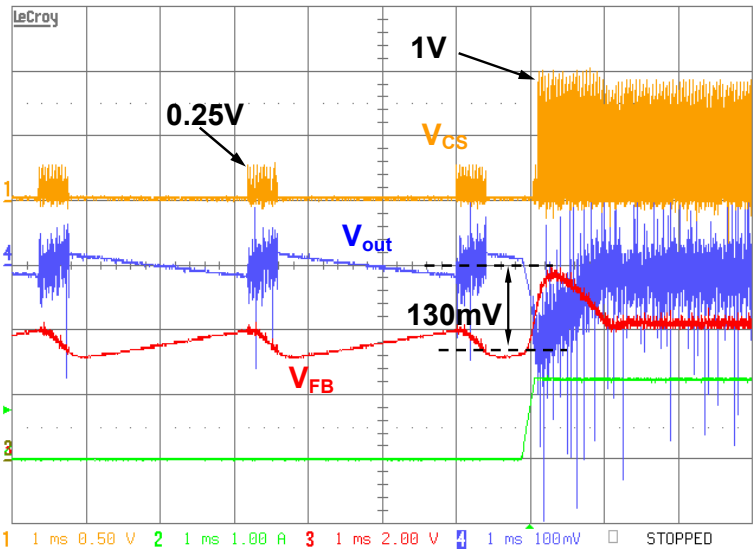


Figure 10 test waveform of leaving burst mode

5.3.4 V_{CC} supply during burst mode

The supply voltage for V_{CC} has to be designed so that it always stays above V_{CC_OFF} limit during burst mode, even at no load. This can lead to a substantial high voltage at V_{CC} pin during maximum load operation. The

circuit configuration for V_{CC} in Figure 3, which consists of C5, R2, ZD1 and C6, is to ensure that the V_{CC} will never exceed 22V under any operation conditions.

6 Protection Features

The IC provides several protection features which lead to the Auto Restart Mode or Latched off mode. The following table shows the conditions of the system failure and the associate protection mode.

Protection functions	Failure condition	"Non-Latch" ICE3xxx65	"Latched" ICE3xxx65L
V_{CC} Overvoltage	V_{CC} > 17V, V_{SOFTS} < 4V V_{FB} > 4.8V	Auto Restart	NA
	V_{CC} > 21V, V_{FB} > 4.8V	NA	Latched off
Overtemperature	T_J > 140°C	Auto Restart	Latched off
Short Winding/ Short Diode	V_{CS}>1.67V	NA	Latched off
Output Overload / Output Short Circuit	V_{FB} > 4.8V and after the blanking window at V_{SOFTS} > 5.4V	Auto Restart	Auto Restart
Open Loop	During power up at light load condition –> **V_{CC} Overvoltage**	Auto Restart	Latched off
	During normal operation –> **Output Over Load**	Auto Restart	Auto Restart
V_{CC} Undervoltage	V_{CC} < 8.5V	Auto Restart	Auto Restart

6.1 Auto Restart Mode

There is always a startup phase with switching cycles in the Auto Restart Mode. After this startup phase the conditions are checked whether the failure is still present. Normal operation proceeds once the failure mode is removed. Otherwise, new startup phase will be initiated again.

Figure 11 shows the switching waveform of the V_{CC} and the feedback voltage V_{FB} when the output is shorted to ground. The IC is turned on at V_{CC} = 15V. After going through the startup phase, IC is off again due to the fault still exists. V_{CC} is discharged until 8.5V. Then, the Startup Cell is activated again to charge up capacitor at V_{CC} that initiates another restart cycle.

6.2 Latched Off Mode

In case of Latched Off Mode (only available for ICE3XXX65L), there is no new startup phase any more. Once Latched Off Mode is entered, the internal Voltage Reference is switched off in order to reduce the current consumption of the IC. In this stage only the UVLO is working which switches on/off the startup cell at V_{CCoff}/V_{CCon}. Latched Off Mode can only be reset when AC line input is plugged out and V_{CC} is discharged to be lower than 6V.

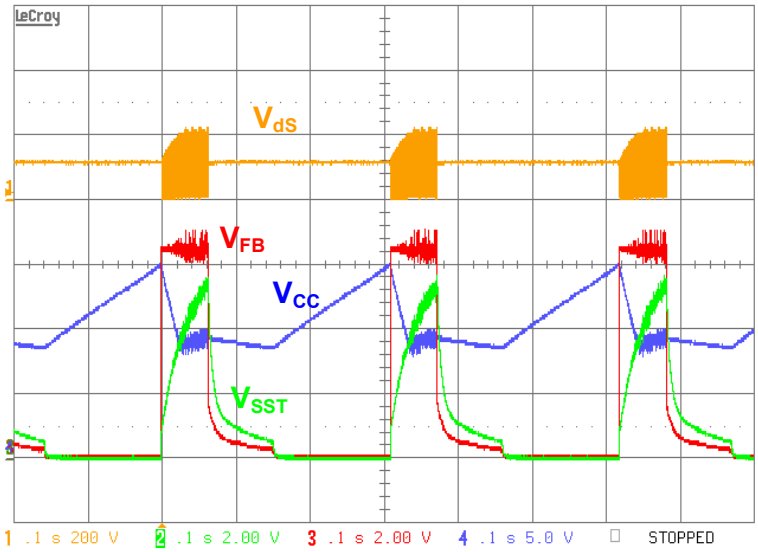


Figure 11 Auto Restart Mode

7 Blanking Window

The IC controller provides an adjustable blanking window before entering into Burst Mode or entering the Auto Restart Mode due to output overload/short circuit. The purpose is to ensure that the system will not enter Active Burst Mode or Protection Mode unintentionally. The blanking time is generated by charging the soft start capacitor C_{SST} from 4.4V to maximum 5.4V. The gate drive is still activated during this time period until the feedback voltage V_{FB} rises up above 4.8V. In case of output overload or short circuit, the transferred power during the blanking period is limited to the maximum power defined by the value of the sense resistor R_{sense}. The blanking time can be calculated by

$$t_{blanking} = C_{SST} \cdot R_{SOFTS} \cdot \ln \frac{2.1V}{6.5V - 5.4V} = 0.65 \cdot C_{SST} \cdot R_{SOFTS} \quad (7)$$

Figure 12 shows the test waveform when secondary output is shorted. The blanking time to enter the protection mode is about 23ms.

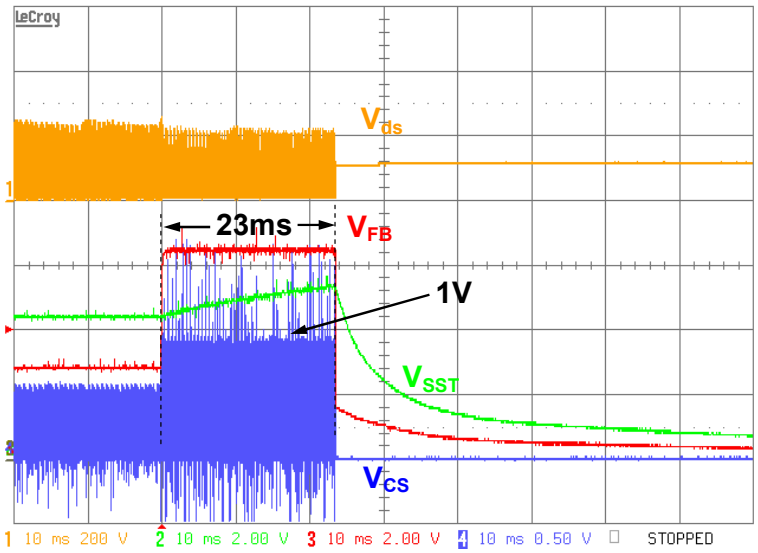


Figure 12 blanking window for output overload protection

References

[1] Infineon Technologies, Datasheet, CoolSET™-F3 Off-Line SMPS Current Mode Controller with Integrated 650V Startup Cell / CoolMOS™

[2] Harald Zoellinger, Rainer Kling, ICE2AXXX for Off-Line Switching Power supply.

[3] Lim Chee Siong, Luo Junyang, Jeoh Meng Kiat, SMPS Evaluation Board with CoolSET™ F3 ICE3B0565.