ICE3Axx65ELJ

CoolSET®-F3 Latch & Jitter version

Design Guide

Power Management & Supply



Never stop thinking.

Edition 2009-11-01

Published by Infineon Technologies Asia Pacific,
8 Kallang Sector,
349282 Singapore, Singapore

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ICE3Axx65ELJ

Revision History:	**2009-11**	V1.1
Previous Version:	V1.0	
Page	Subjects (major changes since last revision)	
9	Add precaution for the start up sequence.	

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1 Introduction

The **ICE3Axx65ELJ** is the further development of the 3rd generation CoolSET®. It is a PWM controller with power MOSFET together in a DIP-8 package. The switching frequency is running at 100 KHz and it targets for DVD player, set-top box, portable game console, auxiliary power supply, etc.

The **ICE3Axx65ELJ** adopts the BiCMOS technology and provides a wider Vcc operating range up to 26V. It inherits the proven good features of CoolSET®-F3 such as the active burst mode achieving the lowest standby power, the propagation delay compensation making the most precise current limit control in wide input voltage range, etc. In addition, it also adds on some useful features such as built-in soft start time, built-in basic with extendable blanking time for over load protection and built-in switching frequency modulation (frequency jittering), external latch enable, etc. Furthermore, it has implemented with enhanced noise immunity feature such that it can pass 20KV ESD test (contact discharge) and 8KV lightning surge test.

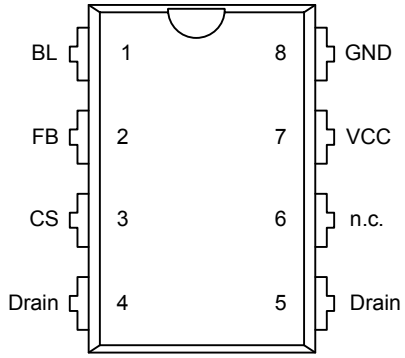
In this application note, functions of the device are described in detail with formula and its performance is shown with test waveforms. The description of other related information such as DCM/CCM mode operating principles and slope compensation and the detailed design procedure are shown in the application note “AN-SMPS-ICE2xXXX-1”.

2 List of Features

650V avalanche rugged CoolMOS® with built in switchable Startup Cell
Active Burst Mode for lowest Standby Power
BiCMOS technology provide wide Vcc voltage range
Fast load jump response in Active Burst Mode
100kHz fixed switching frequency with frequency modulation
Latched Off mode for over temperature, Vcc over voltage and short winding protection
Auto Restart Mode for over load protection, Open Loop protection and Vcc under voltage protection
Built-in soft start time
Built-in and extendable blanking window for short duration peak power
External latch enable feature
Propagation delay compensation tighten the maximum power control between high line and low line
Switching frequency modulation and soft gate driving for low EMI
Robustness to system noise such as ESD, lightning surge, etc.

3 Package & pin assignment

The package for CoolSET®-F3 Latch and Jitter mode product is DIP-8.



Pin	Symbol	Function
1	BL	extended Blanking & Latch enable
2	FB	FeedBack
3	CS	Current Sense / 650V[1] CoolMOS® Source
4	Drain	650V[1] CoolMOS® Drain
5	Drain	650V[1] CoolMOS® Drain
6	n.c.	not connected
7	VCC	controller supply Voltage
8	GND	controller GrouND

Figure 1 DIP-8 package

[1] T_j=110°C

4 Block Diagram

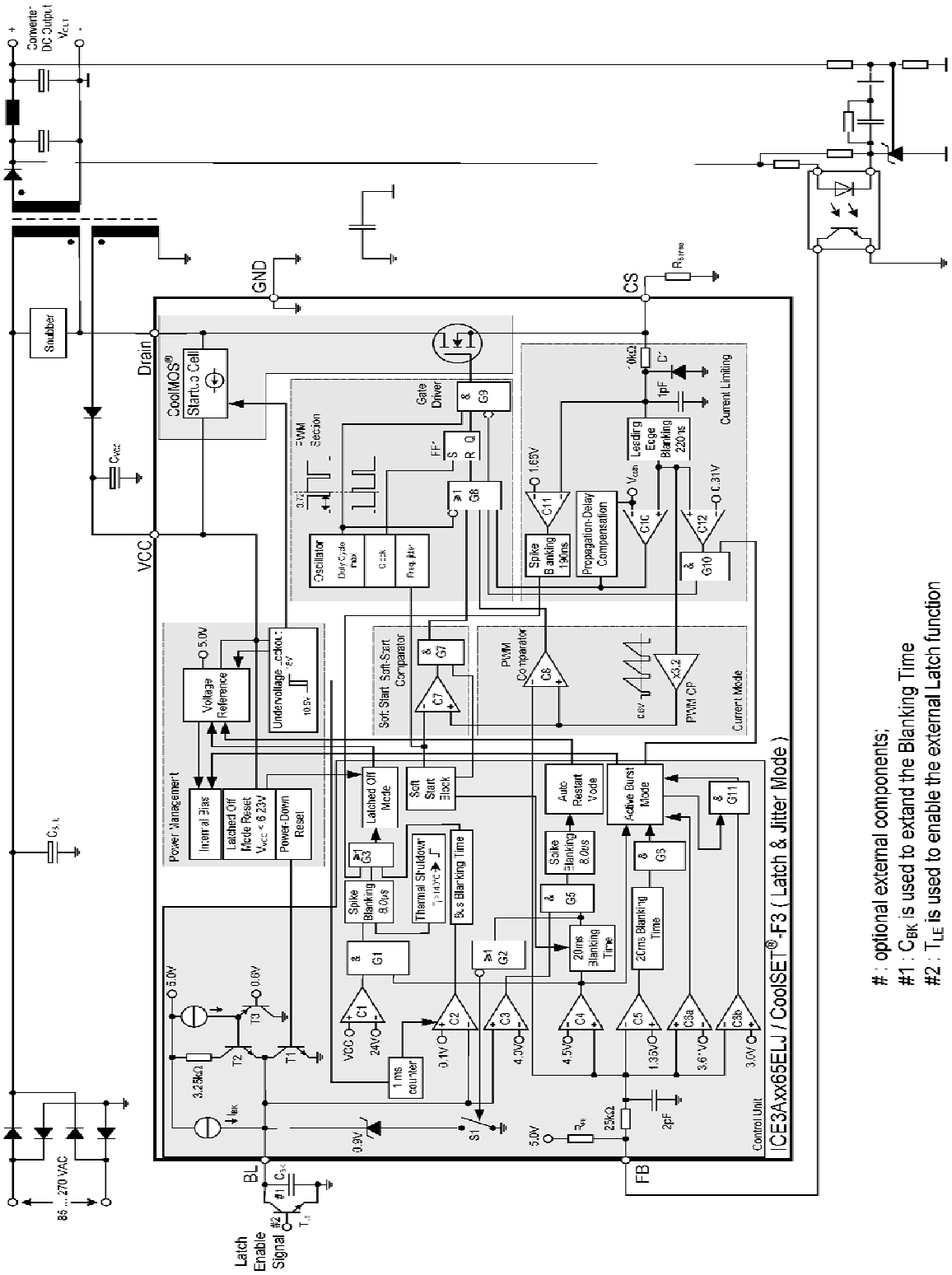


Figure 2 Block Diagram of CoolSET®-F3 ICE3Axx65ELJ

5 Typical Application Circuit

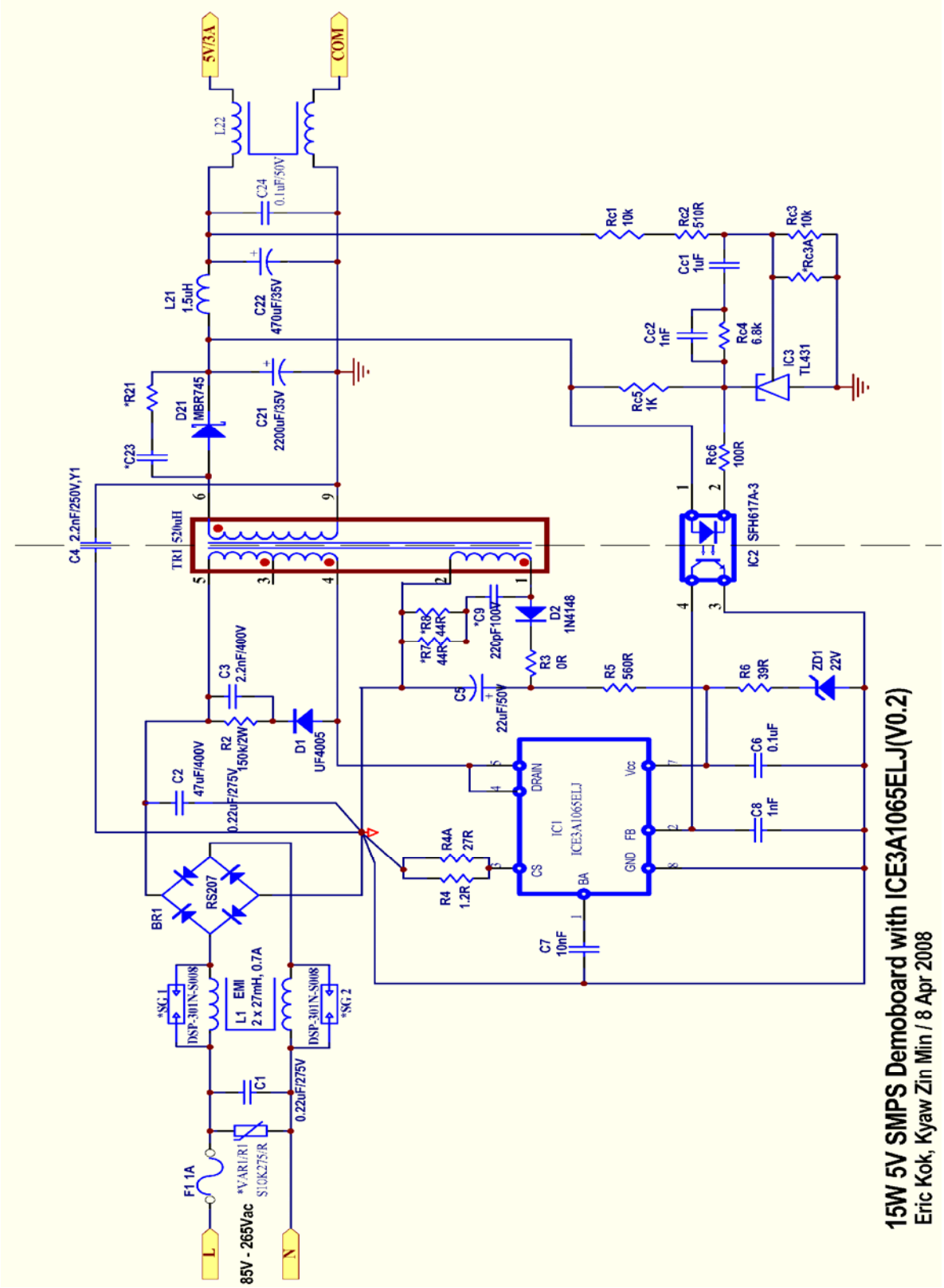


Figure 3 Typical application circuit with CoolSET®-F3, ICE3A1065ELJ 15W 5V

6 Function Description

6.1 Startup Cell

The Startup Cell delivers a constant charge current of $I_{VCCcharge3}$=0.7mA to charge up the V_{CC} capacitor C_{Vcc} at V_{CC} pin. When V_{CC} exceeds the on-threshold V_{CCon}=18V, the bias circuit is switched on. The Startup Cell is switched off to reduce the power loss. The startup delay time, t_{DELAY}, is independent from the AC line input voltage. It can be estimated by the Equation(1).

$$t_{DELAY} = \frac{V_{VCCon} \cdot C_{Vcc}}{I_{VCCcharge3}} \quad (1)$$

Figure 4 shows the startup time delay at 85V_{AC} input. (Pls refer to the datasheet for the symbol used in the equation)

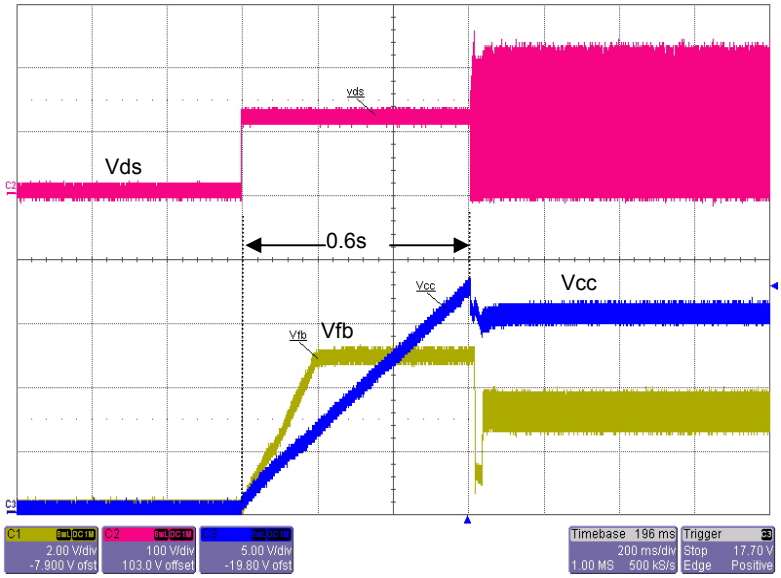


Figure 4 **The startup delay time at AC line input voltage of 85V_{AC}**

Precaution : For a typical application, start up should be VCC ramps up first, other pin (such as FB pin) voltage will follow VCC voltage to ramp up. It is recommended not to have any voltage on other pins (such as FB; BA and CS) before VCC ramps up.

6.2 Soft Start and Normal Operation

When the IC is turned on after the Startup Delay time, a digital soft start circuit is activated. A gradually increased soft start voltage is released by the digital soft start circuit, which in turn increases the duty cycle accordingly. The soft start control voltage is increased with the increasing of count number in the digital counter of the soft start circuit. The soft start time is set at 20ms. When the soft start time ends, IC goes into normal mode and the duty cycle is dependent on the FB signal. Figure 5 shows the soft start behaviour at 85V_{AC} input. It can be seen that the primary peak current slowly increase to the maximum in the soft start period. After soft start stage, IC goes into normal operation with the conventional primary peak current control scheme. Please refer to “AN-SMPS-ICE2xXXXX-1” for the details of normal operation.

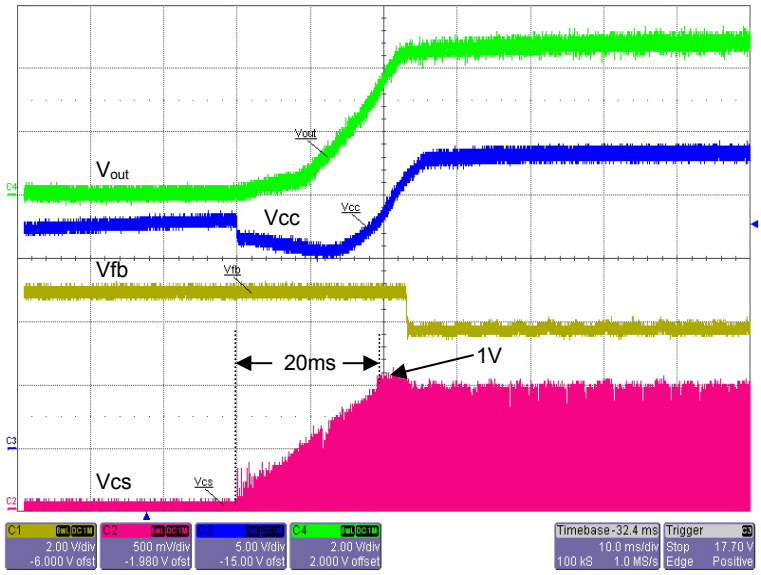


Figure 5 Soft start at AC line input voltage of 85V_{AC}

6.3 Active Burst Mode

The IC provides an Active Burst Mode function at no load or low load conditions to enable the system to achieve the lowest standby power requirement of less than 100mW. Active Burst Mode means the IC is always in the active state and can therefore immediately response to any changes on the FB signal, V_{FB}.

6.3.1 Entering Active Burst Mode

Because of the current mode control scheme, the feedback voltage V_{FB} actually controls the power delivery to output. When the output load is getting lower, the feedback voltage V_{FB} drops. If it stays below 1.35V for a period of 20ms, the IC enters the burst mode operation. The threshold power to enter burst mode can be estimated in Equation(2).

$$P_{BURST_enter} = 0.5 \cdot L_P \cdot \left(\frac{V_{FBC5} - V_{Offset-Ramp}}{R_{sense} \cdot A_V}\right)^2 \cdot f_{SW} \quad (2)$$

where, L_P is the transformer primary inductance, V_{FBC5}=1.35V is the feedback voltage at which the system starts to burst, $V_{Offset-Ramp}$=0.6V is the maximum level of the internal Voltage Ramp on which the amplified current ramp signal of the PWM-OP is superimposed, A_V=3.2 is the internal PWM-OP gain, R_{sense} is the current sense resistor, f_{SW} is the switching frequency. Figure 6 shows the test waveform with the load drop from full load to light load. After blanking time IC goes into burst mode.

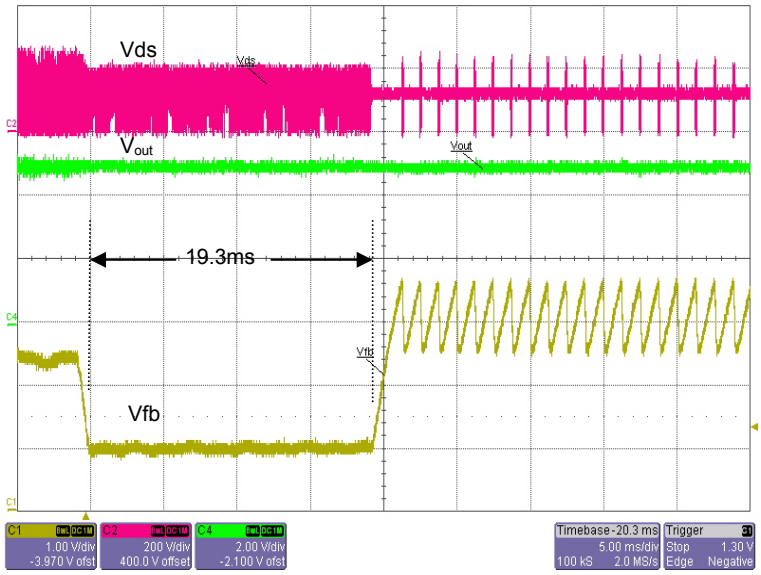


Figure 6 Entering Burst Mode

6.3.2 Working in Active Burst Mode

During active burst mode, the IC is constantly monitoring the output voltage by feedback pin, V_{FB}, which controls burst duty cycle and burst frequency. The burst "on" starts when V_{FB} reaches 3.61V and stops when V_{FB} is down to 3.0V. During burst "on", the primary current limit is set to only 31% of maximum peak current (V_{CS}=0.31V) to reduce the conduction losses and to avoid audible noise. The FB voltage is changing like a saw-tooth between 3.0V and 3.61V.The corresponding secondary output ripple (peak to peak) is regulated in Equation(3).

$$V_{out_ripple_pp} = \frac{R_{opto}}{R_{FB} \cdot G_{opto} \cdot G_{TL431}} \cdot \Delta V_{FB} \quad (3)$$

where, R_{opto} is the resistor in series with opto-coupler at the secondary side to limit the opto-coupler current, R_{FB} is the IC internal pull up resistor connected to FB Pin (refer to Figure 2), G_{opto} is the current transfer gain of opto-coupler, G_{TL431} is the voltage transfer gain between the comparator TL431 output and V_{out}, ΔV_{FB}=3.61-3.0=0.61V is the saw-tooth voltage on the V_{FB} during burst operation.

The leaving burst power threshold, i.e. maximum power to be handled during burst operation is showed in Equation(4).

$$P_{burst_max} = 0.5 \cdot L_P \cdot (0.31 \cdot i_{peak_max})^2 \cdot f_{SW} = 0.5 \cdot L_P \cdot (0.31 \cdot \frac{V_{CS_max}}{R_{sense}})^2 \cdot f_{SW} = 0.0961 \cdot P_{max} \quad (4)$$

Where, i_{peak_max} is the maximum primary peak current, V_{CS_max} is the cycle by cycle current limit threshold at CS pin, P_{max} is the maximum output power of the power supply. It can be seen that the maximum power in burst mode is around 9.61% of P_{max}. Figure 7 shows the waveform of burst mode at light load. It can be seen that the burst ripple is well regulated to be 40mV and it is independent on the output power.

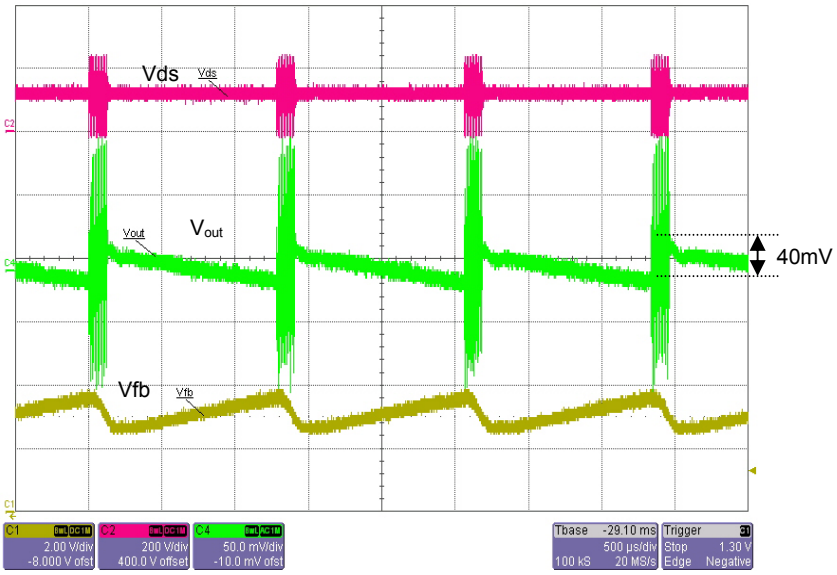


Figure 7 In Burst Mode at light load

6.3.3 Leaving Active Burst Mode

When the output load is increasing to be higher than P_{burst_max}, V_{out} will drop a little bit and V_{FB} will rise up fast to 4.5V. The system leaves burst mode immediately when V_{FB} reaches 4.5V. Once system leaves burst mode, the current sense voltage limit, V_{CS_MAX}, is released to 1V, the feedback voltage V_{FB} swings back to the required level. The timing diagram of leaving burst mode is shown in Figure 8.

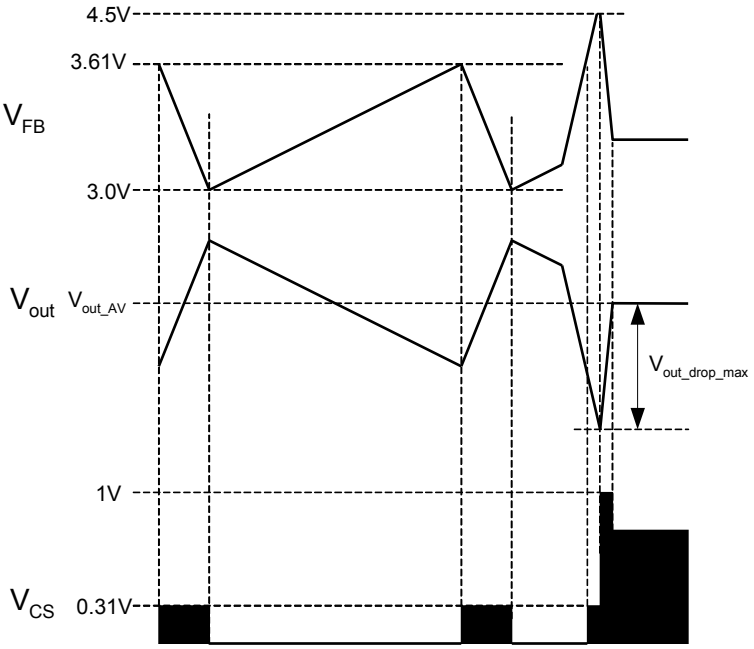


Figure 8 the timing diagram of leaving burst mode

The maximum V_{out} drop during the mode transition is estimated in Equation(5).

$$V_{out_drop_max} = \frac{R_{opto}}{R_{FB} \cdot G_{opto} \cdot G_{TL431}} \cdot (4.5 - \frac{3.0 + 3.61}{2}) = \frac{1.195 \cdot R_{opto}}{R_{FB} \cdot G_{opto} \cdot G_{TL431}} \quad (5)$$

Figure 9 shows the waveform to leave burst mode with load jump from light load to full load. The output voltage drop during the transition is about 140mV.

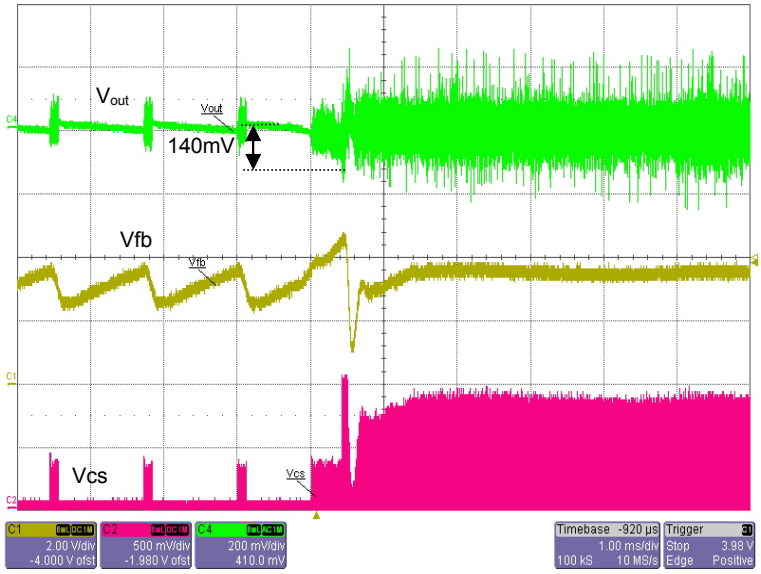


Figure 9 Scope waveform of leaving burst mode

6.3.4 V_{CC} supply during burst mode

The supply voltage for V_{CC} has to be designed so that it always stays above V_{VCCoff} limit during burst mode, especially at no load. If there is a substantial high voltage at V_{CC} pin during maximum load operation, it should add a voltage clamp circuit to absorb the high surge voltage. The circuit configuration for V_{CC} in Figure 3, which consists of C5, R3, R5, R6, ZD1 and C6, is to ensure the V_{CC} will not exceed 26V under any operation conditions.

6.4 Switching frequency modulation

The IC is running at fixed frequency of 100KHz with jittering frequency at +/-4KHz in a switching modulation period of 4ms. This kind of frequency modulation can effectively help to obtain a low EMI level. The measured jittering frequency is 94.5KHz ~ 102.06KHz (Figure 10).

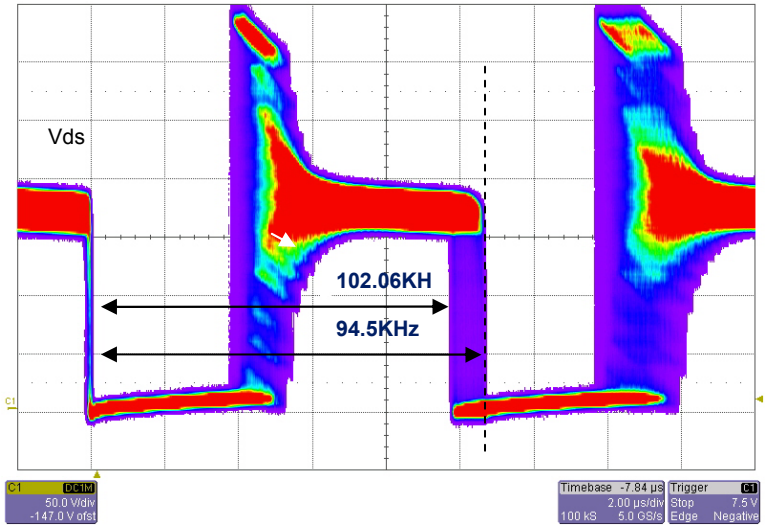


Figure 10 Switching frequency jittering

6.5 Propagation delay compensation

It is observed that the maximum input power will change with input voltage. This is due to the propagation delay of the controller in different dI/dt of the input voltage. The power difference can be as high as >14% between high line and low line. Starting from our 2nd generation, a propagation delay compensation network is implemented so that the power difference is greatly reduced to best around 2%. A measured result for this 15W demo boards shows an output power difference of around +/-3.25% between 85Vac and 269 Vac input. Figure 11 shows the propagation delay compensation curve implemented to the IC. This function applies to discontinuous conduction mode flyback converter only.

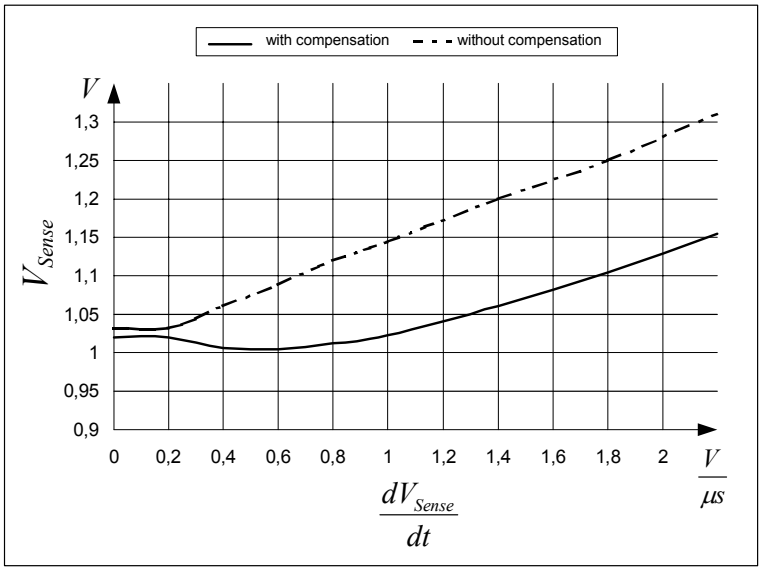


Figure 11 Propagation delay compensation curve

6.6 Protection Features

The IC provides several protection features which lead to the Auto Restart Mode or Latched off mode. The following table lists the conditions of the system faults and the associate protection mode.

Protection functions	Failure condition	Protection Mode
V_{CC} Over voltage	V_{CC} > 24V and V_{FB} > 4.5V	Latched off
Over temperature (controller)	T_J > 130^{O}C	Latched off
Short Winding/ Short Diode	V_{CS} > 1.66V	Latched off
External latch enable	V_{BL} < 0.1V	Latched off
Output Overload / Output Short Circuit	V_{FB} > 4.5V and V_{BL} > 4.0V (after built-in / extended blanking time)	Auto Restart
Open Loop	–> Output Over Load	Auto Restart
V_{CC} Undervoltage / short Opto-coupler	V_{CC} < 10.5V	Auto Restart

6.6.1 Auto Restart Mode

There is always a startup phase with switching pulses in the Auto Restart Mode. After this startup phase the fault conditions are checked. If the fault persists, it would continue the auto-restart mode. Otherwise, it would resume to normal mode.

Figure 12 shows the switching waveform of the V_{CC} and the feedback voltage V_{FB} when the output is shorted to ground. The IC turns on when the V_{CC} reaches 18V. It then start the startup phase. However, the IC is off again due to the fault still persists. The V_{CC} is discharged until 10.5V. Then, the Startup Cell is activated again to charge up capacitor at V_{CC} to 18V. Then it initiates another restart cycle.

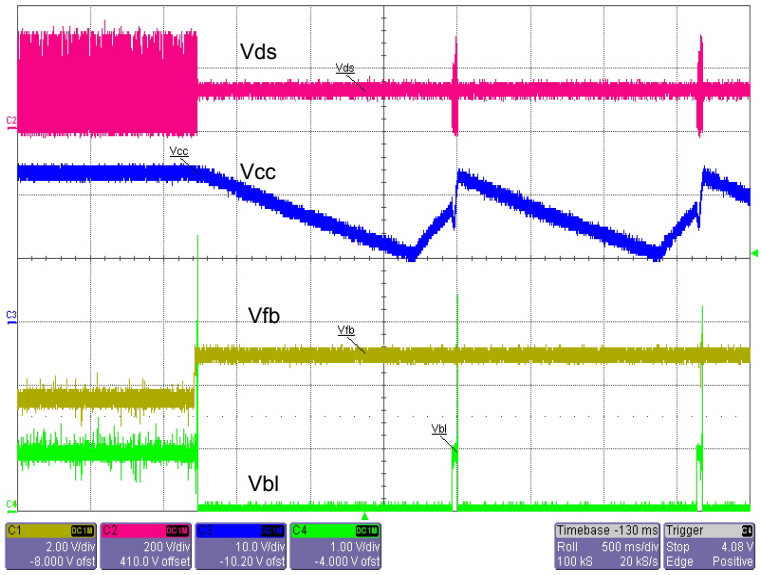


Figure 12 Auto Restart Mode (without extended blanking time)

6.6.2 Latched Off Mode

In case of Latched Off Mode, there is no new startup phase any more. Once Latched Off Mode is entered, the internal Voltage Reference is switched off in order to reduce the current consumption of the IC. In this stage only the UVLO circuit is working which switches on/off the startup cell at V_{CCon}/V_{CCoff}. Latched Off Mode can only be reset when AC line input is removed and the V_{CC} is discharged to lower than 6.23V.

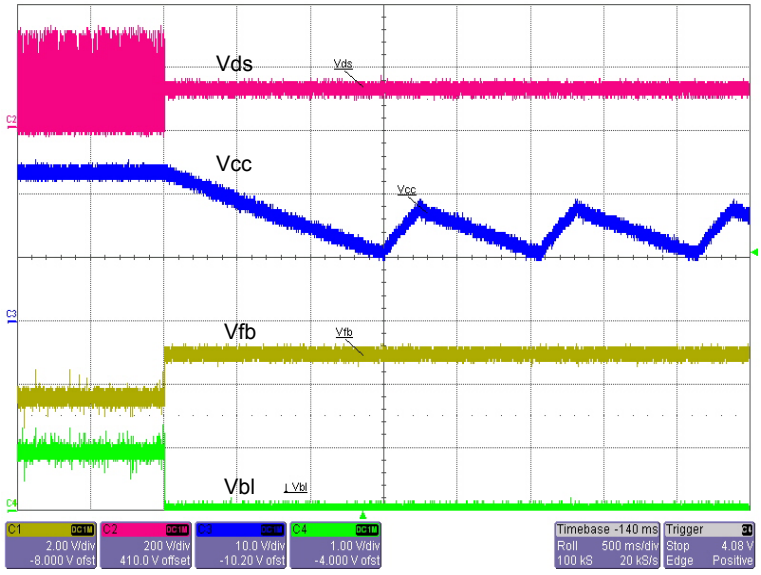


Figure 13 Latch off Mode (V_{BL} < 0.1V)

6.6.3 Blanking Time for over load protection

The IC controller provides a blanking window before entering into the auto restart mode due to output overload/short circuit. The purpose is to ensure that the system will not enter protection mode unintentionally. There are 2 kinds of the blanking time; basic and the extendable. The basic one is a built-in feature which is set at 20ms. The extendable one is to extend the basic one with a user defined additional blanking time. The extendable blanking time can be achieved by adding a capacitor, C_{BK} to the BL pin. When there is over load occurred (V_{FB} > 4.5V), the C_{BK} capacitor will be charged up by an constant current source, I_{BK} (8.4uA) from 0.9V to 4.0V. Then the auto restart protection will be activated. The charging time from 0.9V to 4.0V to the C_{BK} capacitor is the extended blanking time. The total blanking time can be calculated by the Equation(6).

$$T_{blanking} = Basic + Extended = 20ms + \frac{(4.0-0.9)*C_{BK}}{I_{BK}} = 20ms + 369047.6*C_{BK} \quad (6)$$

The measured total blanking time showing in figure 14 is 125ms using C_{BK}=0.22uF.

In case of output overload or short circuit, the transferred power during the blanking period is limited to the maximum power defined by the value of the current sense resistor R_{sense}.

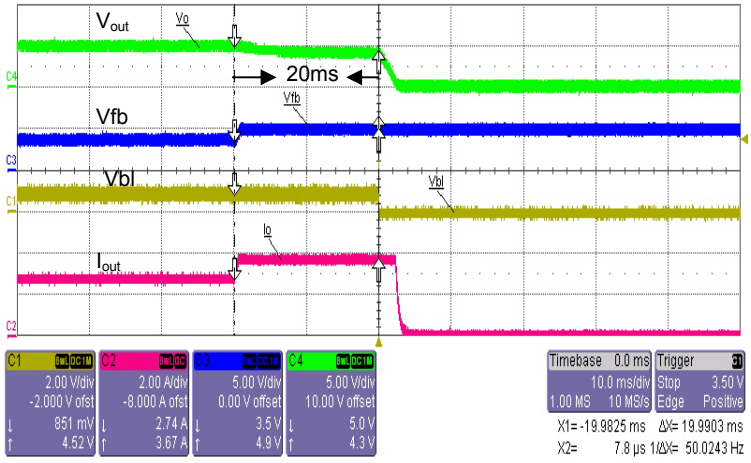


Figure 14 Blanking window for over load protection (basic blanking time)

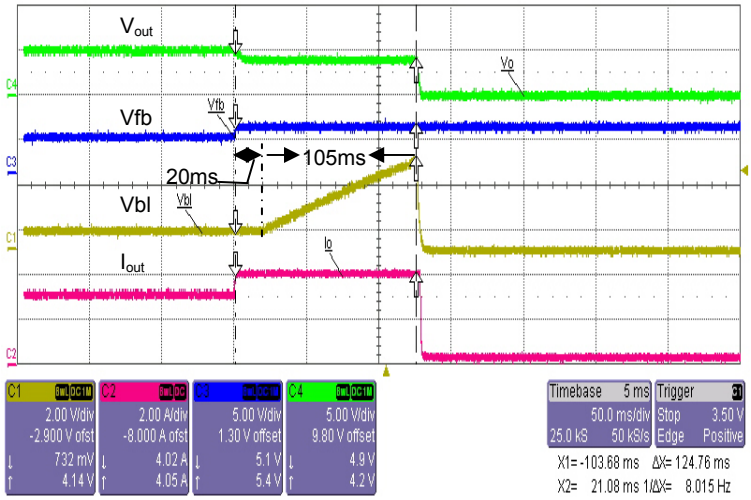


Figure 15 Blanking window for overload protection (with extended blanking time, C_{BK}=0.22uF)

7 Layout Consideration

In order to get the optimized performance of the CoolSET®-F3, the grounding of the PCB layout must be connected carefully. From the circuit diagram in Figure 3, it indicates that the grounding for the CoolSET®-F3 can be split into several groups; signal ground, Vcc ground, Current sense resistor ground and EMI return ground. All the split grounds should be "star" connected to the bulk capacitor ground directly. The split grounds are described as below.

- Signal ground includes all small signal grounds connecting to the CoolSET® GND pin such as filter capacitor ground, C6, C7, C8 and opto-coupler ground.
- Vcc ground includes the Vcc capacitor ground, C5 and the auxiliary winding ground, pin 2 of the power transformer.
- Current Sense resistor ground includes current sense resistor R4 and R4A.
- EMI return ground includes Y capacitor, C4.

8 CoolSET®-F3 ICE3Axx65ELJ product list

Device	Package	V_{DS}	Current /A	R_{dson} /Ω[1]	Frequency / KHz	Pout Vin=230Vac±15%[2]	Pout Vin=85-265Vac [2]
ICE3A1065ELJ	PG-DIP-8	650V	1.0	2.95	100	32W	16W
ICE3A2065ELJ	PG-DIP-8	650V	2.0	0.92	100	57W	28W

9 Useful formula & external component design

Transformer calculation (DCM flyback)	
Input data	V_{in_min} = 90Vdc, V_{in_max} = 380Vdc, V_{ds_max} = 470V for 600V MOSFET, $D_{max} \le 50\%$
Turn ratio	$N_{ratio} = \frac{V_{ds_max} - V_{in_max}}{V_{out} + V_{diode}}$
Maximum Duty ratio	$D_{max} = \frac{(V_{out} + V_{diode}) \cdot N_{ratio}}{V_{in_min} + (V_{out} + V_{diode}) \cdot N_{ratio}}$
Primary Inductance	$L_p \le \frac{(V_{in_min} \cdot D_{max})^2}{2 \cdot P_{in} \cdot f_{sw}}$
Primary peak current	$I_{p_max} = \frac{V_{in_min} \cdot D_{max}}{L_p \cdot f_{sw}}$
Primary turns	$N_p \ge \frac{I_{p_max} \cdot L_p}{B_{max} \cdot A_{min}}$

[1] Typ @ 25°C

[2] Calculated maximum input power rating at T_a=75°C, T_j=125°C and without copper area as heat sink.

Secondary turns	$N_s = \frac{N_p}{N_{ratio}}$
Auxiliary turns	$N_{aux} = \frac{V_{cc} + V_{diode}}{V_{out} + V_{diode}} \cdot N_s$

ICE3AXX65ELJ external component design	
Current sense resistor	$R_{sense} \le \frac{V_{csth_max}}{I_{p_max}}$
Soft start time	$t_{soft} = 20ms$
Vcc capacitor	$C_{VCC} = \frac{I_{VCCsup2} \cdot t_{soft}}{V_{CCHY}} \cdot \frac{2}{3}$
Startup time	$t_{STARTUP} = \frac{V_{VCCon} \cdot C_{Vcc}}{I_{CCcharge3}}$
Enter burst mode power	$P_{burst_enter} = \frac{1}{2} \cdot L_P \cdot (\frac{V_{FB_enter} - V_{Offset-Ramp}}{R_{sense} \cdot A_V})^2 \cdot f_{SW}$
Leave burst mode power	$P_{burst_max} = 0.0961 \cdot P_{in_max}$
Output ripple during burst mode	$V_{out_ripple_pp} = \frac{R_{opto}}{R_{FB} \cdot G_{opto} \cdot G_{TL431}} \cdot \Delta V_{FB}$
Voltage drop when leave burst mode	$V_{out_drop_max} = \frac{1.195 \cdot R_{opto}}{R_{FB} \cdot G_{opto} \cdot G_{TL431}}$
Total blanking time for over load protection	$t_{blanking} = 20ms + 369047.6 \cdot C_{BK}$

10 References

[1] Infineon Technologies, Datasheet “CoolSET®-F3 ICE3A1065ELJ Off-Line SMPS Current Mode Controller with Integrated 650V CoolMOS® and Startup Cell (Latched and Frequency Jitter Mode)”

[2] Kyaw Zin Min, Eric Kok Siu Kam, Infineon Technologies, Application Note “AN-EVALSF3-ICE3A1065ELJ, 15W 5.0V SMPS Evaluation Board with CoolSET®-F3 ICE3A1065ELJ “

[3] Harald Zoellinger, Rainer Kling, Infineon Technologies, Application Note “AN-SMPS-ICE2xXXX-1, CoolSET™ ICE2xXXXX for Off-Line Switching Mode Power Supply (SMPS)”