CoolGaN™ totem-pole PFC design guide and power loss modeling

About this document

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Scope and purpose

This document is a design guide for a gallium nitride (GaN) Power Factor Correction (PFC) totem-pole converter, including:

- Equations for design and power losses
- Selection guide for semiconductor devices and passive components
- Totem-pole PFC controller using ICE3PCS01G
- 2500 W design example with calculated and experimental results

Intended audience

This document is intended for design engineers who want to design a CoolGaN™ Continuous Conduction Mode (CCM) PFC totem-pole converter.

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1 Introduction

Many applications require a front-end AC-DC rectifier (Figure 1), which contains a PFC front-end stage that regulates the bus voltage to a DC value (~390 V), followed by a DC-DC stage that steps down the bus voltage and provides a galvanically isolated and regulated DC output (e.g. 12 V or 48 V). This document discusses the PFC stage in high-power applications such as telecom and data center server power supplies.

PFC shapes the input current of the power supply to be in synchronization with the mains voltage, in order to maximize the real power drawn from the mains. In a perfect PFC circuit, the input current follows the input voltage as a pure resistor, without any input current harmonics.

Boost-derived topologies are the most common for PFC. GaN-based totem-pole PFC proves to be a winning topology in terms of efficiency and power density. This document shows the benefits of GaN-based totem-pole PFC and introduces its analysis and design methodology, including equations for power loss estimation, a selection guide for semiconductor devices and passive components, and a design example with experimental results.

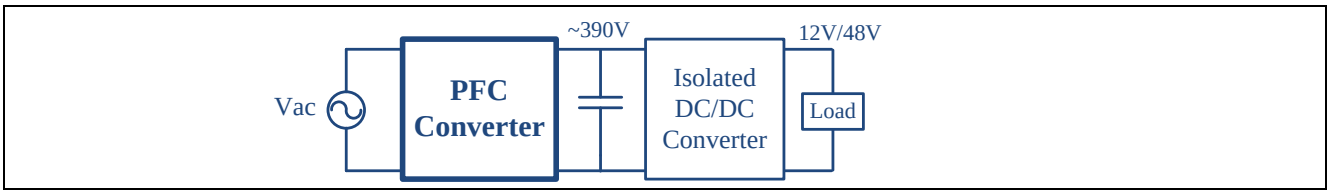


Figure 1 AC-DC rectifier

The following is a quick overview of the classic boost PFC vs. GaN totem pole.

1.1 Classic boost PFC

Although active PFC can be achieved by several topologies, the classic boost converter (Figure 2) is the most popular topology used in PFC applications. The boost converter key waveforms are shown on the right of Figure 2. Since the input voltage to the boost is a rectified sinusoidal voltage, varying from zero to the sinusoidal peak voltage, the duty cycle also varies with the input voltage variation across the line cycle. The average inductor current shown in Figure 2 is conducted through two diodes of the rectifier bridge at all times, and this causes significant conduction loss, especially at higher power and low-line conditions.

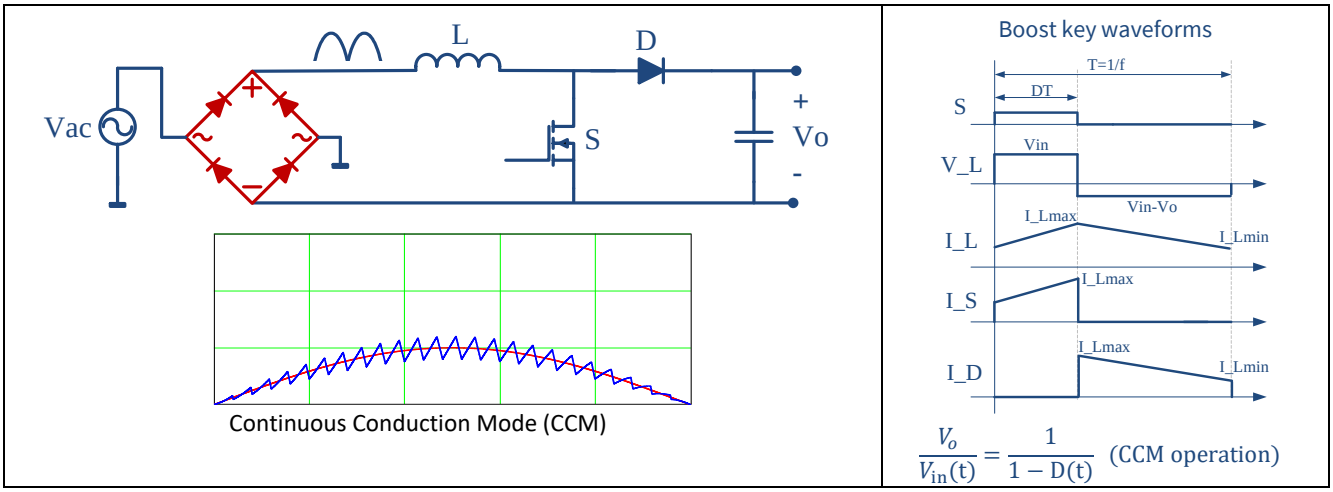


Figure 2 Structure and key waveforms of a boost converter

1.2 Bridgeless totem-pole PFC

Figure 3 shows the totem-pole PFC topology. Its main benefit compared to the classic boost PFC is that it is a bridgeless circuit, meaning that it does not include a rectifier diode bridge at its input. Therefore the associated rectifier bridge losses are eliminated, leading to higher efficiency and power density.

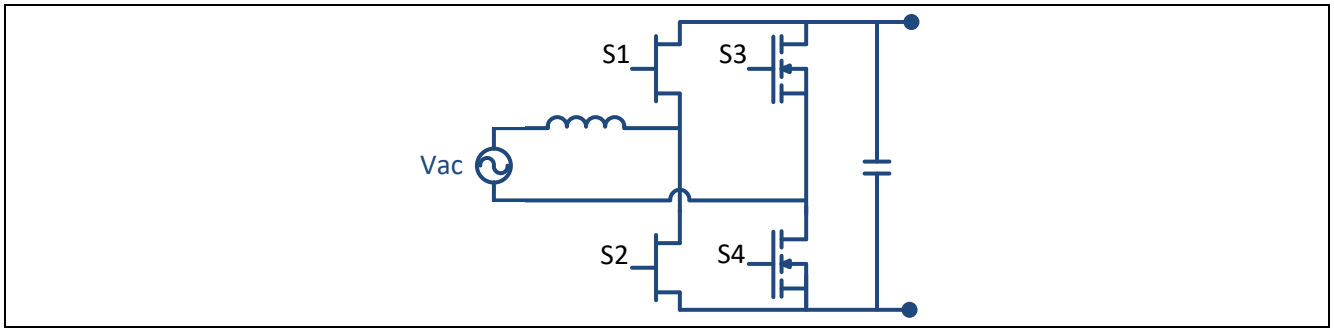
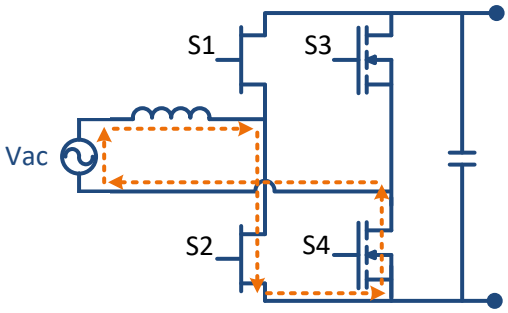
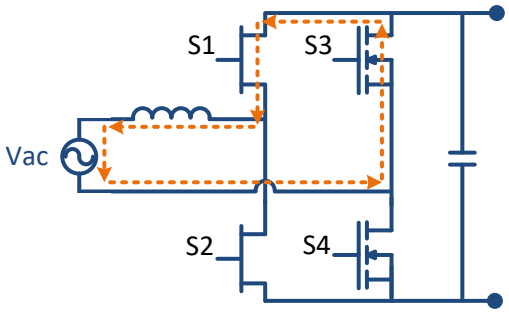
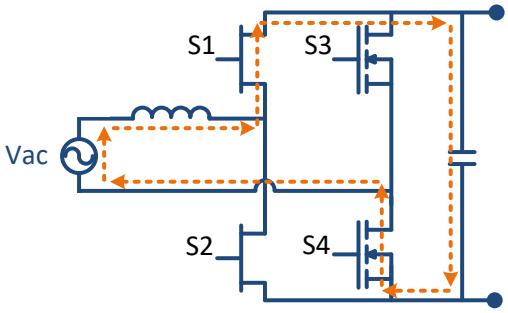
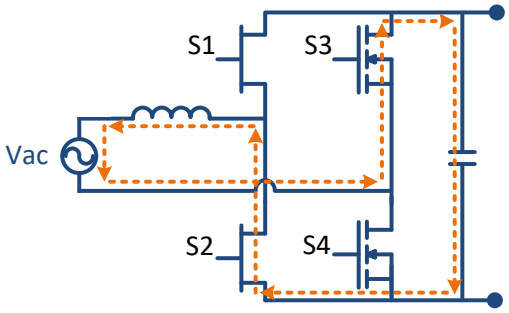


Figure 3 Block schematic for totem-pole PFC power stage

Table 1 shows the operational modes of the totem pole during the positive and negative halves of the AC-line cycle. Two switches run at high switching frequency with the function of the boost switch and rectifier switch, while the other two switches run at line frequency with the function of line rectifier.

Table 1

Positive AC voltage half-line	Negative AC voltage half-line
S1: Switching as synchronous switch S2: Switching as control switch S3: Off S4: On	S1: Switching as control switch S2: Switching as synchronous switch S3: On S4: Off
	
	

2 Totem pole PFC benefits

2.1 Efficiency

CoolGaN™ has the unique benefit of zero reverse recovery, which makes GaN an enabling device for totem-pole PFC topology, because the switch is working as a main PFC switch in one half of the line cycle and then as a synchronous switch in the following half-line cycle, as shown in Table 1. A CoolMOS™ body diode is not suitable for such an operation because it has large reverse recovery charge.

To illustrate the CoolGaN™ efficiency benefit, Figure 4 shows a breakdown of main power losses at 50 percent load and high-line condition. This example breakdown belongs to a 3000 W PFC design using classic PFC boost with CoolMOS™ vs. totem-pole PFC with CoolGaN™.

Although the two GaN switches have lower loss compared to the combined boost CoolMOS™ and diodes, the more pronounced benefits of totem-pole PFC include the saved diode bridge loss, which has a significant share of total losses as seen in the classic boost PFC case.

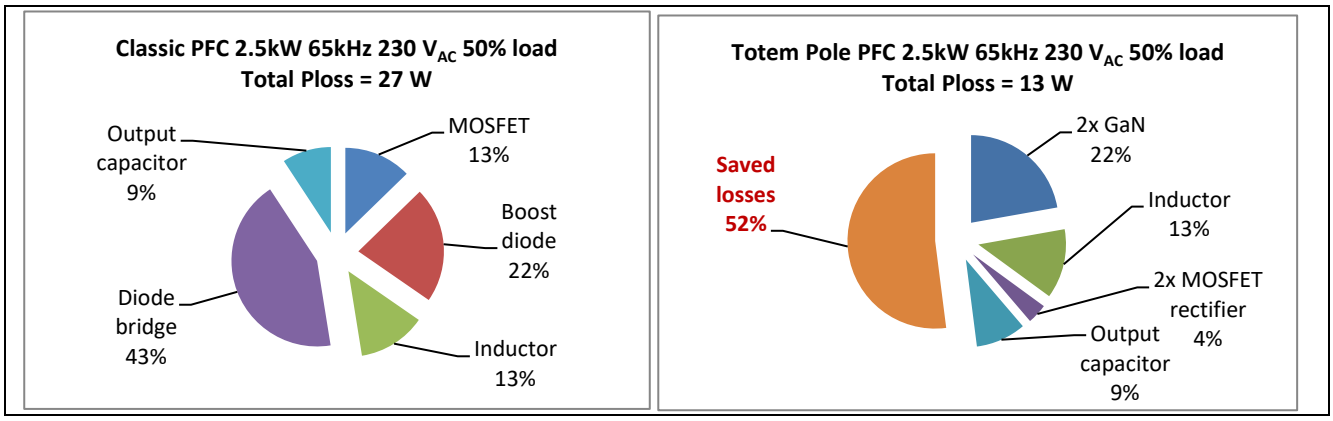


Figure 4 Breakdown of power losses: classic boost PFC vs. totem pole PFC

2.2 Power density

A multi-domain/objective optimization simulation calculates the maximum attainable efficiency vs. power density based on the limits of technological parameters. Figure 5 shows the trade-off limit curve (Pareto front) of a multi-objective, i.e. efficiency and power density design optimizations for classic boost PFC and totem-pole PFC. It clearly shows the maximum possible efficiency benefit of the totem pole compared to classic boost PFC for the same power density; furthermore, totem pole can reach higher density limits at higher efficiency compared to classic boost PFC.

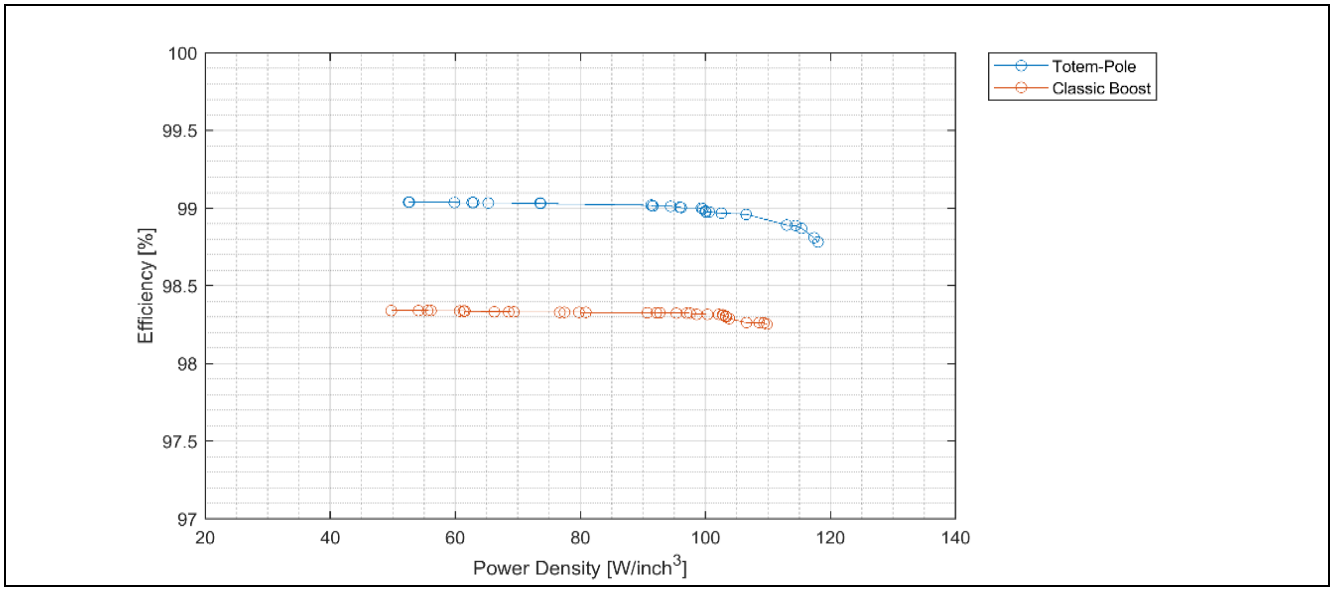


Figure 5 **Pareto chart showing efficiency and power density, for classic boost PFC vs. totem-pole PFC**

3 Totem-pole PFC power stage design

This section details the converter design and power loss equations for the CCM totem-pole PFC. The design example specifications listed in Table 2 will be used for all of the equation calculations. Since the converter is designed to deliver full power at high-line 230 V AC, and power is derated at low-line voltage, all design equations and power losses will be calculated using the high-line voltage condition, unless it is necessary to also consider the low-line condition.

Table 2 Specifications of the power stage

Input voltage	85 to 265 V AC 60 Hz
Output voltage	390 V
Maximum power steady-state	2500 W at $V_{ac.HL} = 230\,V$ AC, 1250 W at $V_{ac.LL} = 115\,V\,AC$
Switching frequency	65 kHz
Inductor current ripple	25 percent at low-line/full load
Output voltage 120 Hz ripple	20 V_{p-p}
Hold-up time	8.33 ms at $V_{o,min}$ = 340 V

3.1 PFC inductor

The PFC inductor value and its maximum current are determined based on the specified maximum inductor current ripple as shown below:

$$L = \frac{1}{\%Ripple} \cdot \frac{{V_{ac.HL}}^2}{P_o}\left(1 - \frac{\sqrt{2} \cdot V_{ac.HL}}{V_o}\right) \cdot T = \frac{1}{25\%} \cdot \frac{(230V)^2}{2500W}\left(1 - \frac{\sqrt{2} \cdot 230V}{390V}\right) \cdot \frac{1}{65 \cdot 10^3 Hz} = 216\,\mu H \quad \text{Eq. 1}$$

$$I_{L.max} = \frac{\sqrt{2} \cdot P_o}{V_{ac.HL}} \cdot \left(1 + \frac{\%Ripple}{2}\right) = \frac{\sqrt{2} \cdot 2500W}{230V} \cdot \left(1 + \frac{0.25}{2}\right) = 17.2\,A \quad \text{Eq. 2}$$

A swinging choke has an inductance value that is inversely proportional to its operating current. AmoFlux or Kool Mu material from Magnetics Inc., for example, can deliver good power factor, THDi and EMI performance, due to the high inductance at lower current (or DC bias).

In this design, a 60 µ permeability AmoFlux core from Magnetics Inc. is used. It consists of three stacked 0088071A7 toroid cores, with 60 turns of AWG#15 copper wire. The DC resistance is about 52 mΩ, and the inductance ranges from 651 µH at no-load dropping to about 231 µH at 230 V AC and full load, which is very close to the desired value calculated above in Eq. 1.

Inductor saturation current must be rated at more than $I_{L.max}$, in order to survive line and load transients.

Since the inductance value varies across the line and load range, and also across the line cycle, it would be more accurate to model the inductance value as a function of V_{in}, P_o and t in order to obtain better estimation of the switching currents and losses. This specific inductor design was modeled as shown in Figure 6 as a function of power (P_o) and time (t) across the line cycle, using the equations Eq. 3 to Eq. 6 below:

$$I(t, Po) = \frac{P_o \cdot \sqrt{2}}{V_{ac}} \cdot sin(2\pi \cdot f_{line} \cdot \mathrm{t}) \quad \text{Eq. 3}$$

$$H(t, Po) = \left|\frac{0.4 \cdot \pi \cdot N \cdot I_L(t, Po)}{l_e\,(cm)}\right| \quad \text{Eq. 4}$$

$$\mu_{eff}(t,Po) = \mu_i \cdot (0.9931 + 2.295 \cdot 10^{-3} \cdot H(t,Po) - 1.291 \cdot 10^{-4} \cdot H(t,Po)^2 + 7.653 \cdot 10^{-7} \cdot H(t,Po)^3 - 1.361 \cdot 10^{-9} \cdot H(t,Po)^4$$ Eq. 5

$$L(t,Po) = \frac{0.4 \cdot \pi \cdot N^2 \cdot \mu_{eff}(t,Po) \cdot A_e(in\ cm^2)}{l_e\ (cm)}$$ Eq. 6

$Inductor\ cross\ section\ area\ A_e = 3 \cdot 65.6\ mm^2$

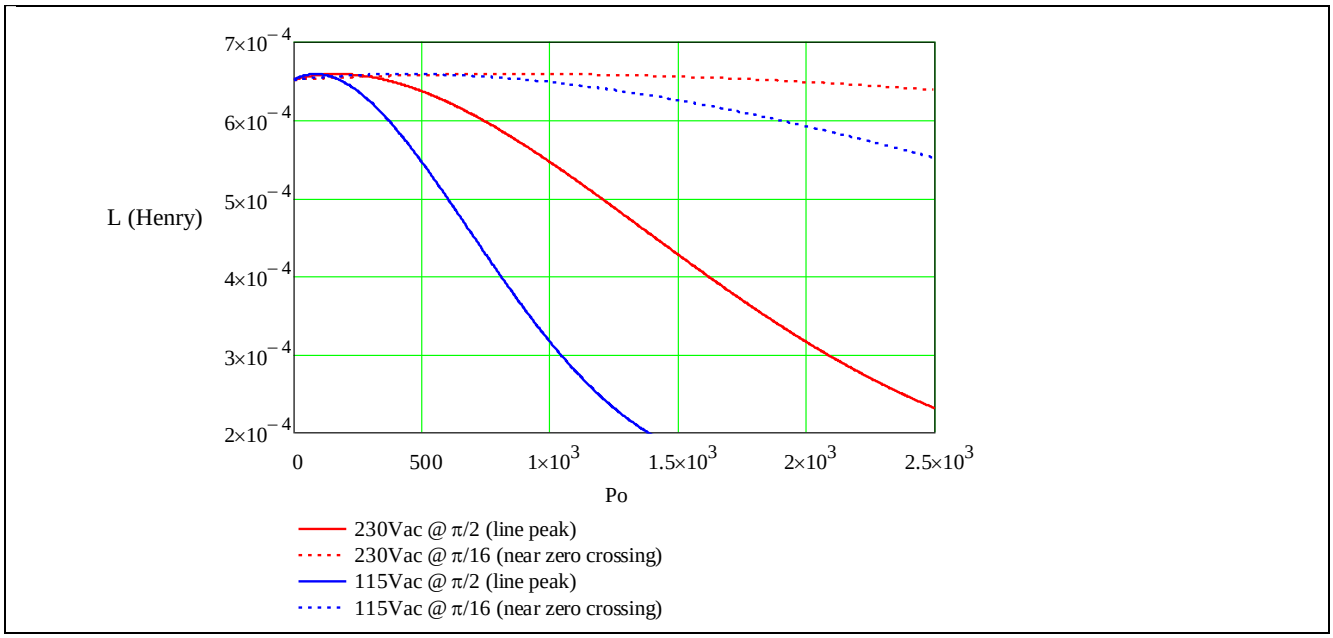


Figure 6 Swinging inductance accros load/line range

3.1.1 Inductor copper loss

The inductor RMS current and the corresponding copper loss are:

$$I_{L.rms} \cong I_{in.rms} = \frac{P_o}{V_{ac.HL}} = \frac{2500\ W}{230\ V} = 10.87\ A$$ Eq. 7

$$P_{L.cond} = {I_{L.rms}}^2 \cdot DCR = (10.87\ A)^2 \cdot 0.052\ \Omega = 6.15\ W$$ Eq. 8

3.1.2 Inductor core losses

At low-line, core loss across the line cycle is found to be close to a sinusoidal shape (Figure 7, left). Therefore a simple and accurate enough method to estimate the average core loss is to calculate the peak core loss at the peak of the line-cycle point, then multiply by 2/π. However, at high-line, core losses are far from the sinusoidal shape (Figure 7, right), so the aforementioned method is not valid any more, and it is necessary to model the core loss across the line cycle as a function of time, and then integrate it to obtain the average loss. This integration method can also be used for the low-line core loss calculation for more accurate results. Both methods are demonstrated below.

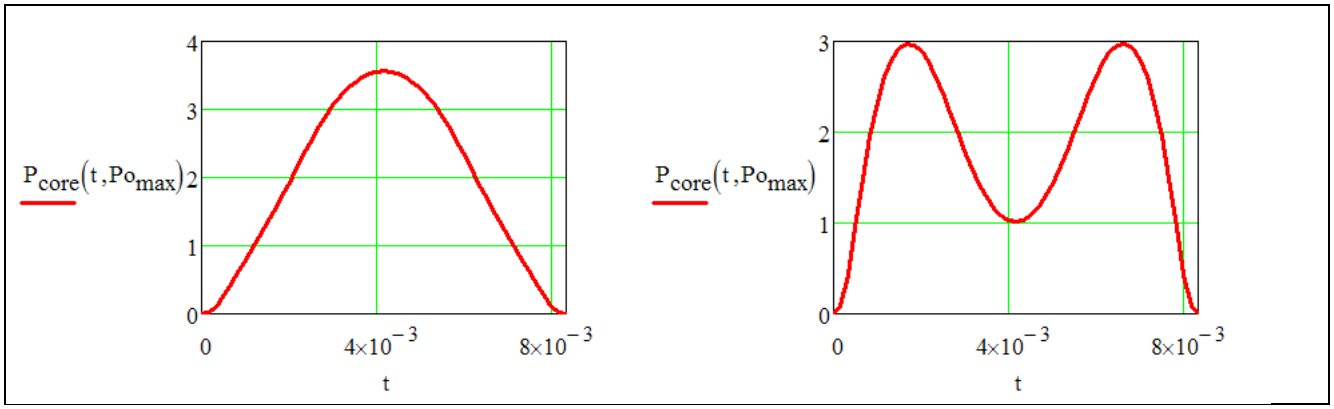


Figure 7 **Inductor core loss across the line cycle, 115 V AC/1250 W (left) and 230 V AC/2500 W (right)**

3.2 Low-line core loss

In order to calculate the average core loss, we need to calculate the peak core loss at the peak of the line-cycle point, then multiply by 2/π.

To calculate the peak core loss we calculate the minimum and maximum inductor current and the associated minimum and maximum magnetic force (H) at the peak of the line-cycle point. Then we can use the fitted equation of that magnetic material to calculate the minimum and maximum magnetic flux (B). Then the peak AC flux swing can be used to calculate the peak core loss by using another fitted equation.

For three stacked AmoFlux 0088071A7 toroids, we get:

$Path\ length\ \ l_e = 81.4\ mm \qquad Cross\ section\ area\ \ A_e = 3 \cdot 65.6\ mm^2 \qquad Volume\ \ V_e = 3 \cdot 5340\ mm^3$

Using the maximum inductor current calculated in Eq. 2, the magnetic force at the peak of the line cycle can be found as:

$$I_{L.max.LL} = \frac{P_{o.LL} \cdot \sqrt{2}}{V_{ac.LL}}\left(1 - \frac{\%Ripple}{2}\right) = \frac{1250W \cdot \sqrt{2}}{115V}\left(1 - \frac{25\%}{2}\right) = 18.5\ A \qquad \text{Eq. 9}$$

$$H_{max} = \frac{0.4 \cdot \pi \cdot N \cdot I_{L.max.LL}}{l_e\ (cm)} = \frac{0.4 \cdot \pi \cdot 60\ turns \cdot 18.5A}{98.4mm/10} = 171\ Oersteds \qquad \text{Eq. 10}$$

The minimum inductor current and magnetic force at the peak of the line cycle are:

$$I_{L.min.LL} = \frac{P_o \cdot \sqrt{2}}{V_{ac.HL}}\left(1 - \frac{\%Ripple}{2}\right) = \frac{2500W \cdot \sqrt{2}}{230V}\left(1 - \frac{25\%}{2}\right) = 12.2\ A \qquad \text{Eq. 11}$$

$$H_{min} = \frac{0.4 \cdot \pi \cdot N \cdot I_{L.min}}{l_e\ (cm)} = \frac{0.4 \cdot \pi \cdot 64turns \cdot 17.42A}{98.4mm/10} = 113.2\ Oersteds \qquad \text{Eq. 12}$$

Flux density for 60 µ AmoFlux material is:

$$B = \left(\frac{a + b \cdot H + c \cdot H^2}{1 + H + d \cdot H^2}\right)^x \qquad \text{Eq. 13}$$

where a = $8.252*10^2$ b = $1.236*10^{-1}$ c = $2.017*10^{-2}$ d = $1.689*10^{-2}$ x = 2

The minimum and maximum flux densities at the peak of the line cycle are:

$$B_{max} = \left(\frac{a + b \cdot H + c \cdot H^2}{1 + H + d \cdot H^2}\right)^x = 0.843\ Tesla \qquad \text{Eq. 14}$$

$$B_{min} = \left(\frac{a + b \cdot H + c \cdot H^2}{1 + H + d \cdot H^2}\right)^x = 0.679\ Tesla$$ Eq. 15

The AC flux swing at the peak of the line cycle is:

$$\Delta B = \frac{B_{max} - B_{min}}{2} = 0.082\ Tesla$$ Eq. 16

Peak core loss at the peak of the line cycle is:

$$P_{core.pk} = 55.6 \cdot \Delta B^{2.2} \cdot \left(\frac{f}{10^3}\right)^{1.65} \cdot V_e \cdot 10^{-6} = 0.236^2 \cdot \left(\frac{65 \cdot 10^3}{10^3}\right)^{1.46} \cdot 3 \cdot 5340 \cdot 10^{-6} = 3.56\ W$$ Eq. 17

Average core loss across the line cycle is:

$$P_{core.av} = P_{core.pk} \cdot \frac{2}{\pi} = 3.25\ W \cdot \frac{2}{\pi} = 2.27\ W$$ Eq. 18

3.3 High-line core loss

At high-line, core losses are far from the sinusoidal shape (Figure 7, right), so it is necessary to model the core loss across the line cycle as a function of time, and then integrate it to obtain the average loss. The following set of equations can be used in Mathcad® or other tools:

$$I_{L.max}(t) = \frac{P_o \cdot \sqrt{2}}{V_{ac.HL}} \cdot sin(2\pi \cdot f_{line} \cdot t)\left(1 + \frac{\%Ripple}{2}\right), \quad H_{max}(t) = \frac{0.4 \cdot \pi \cdot N \cdot I_{L.max}(t)}{l_e\ (cm)}$$ Eq. 19

$$I_{L.min}(t) = \frac{P_o \cdot \sqrt{2}}{V_{ac.HL}} \cdot sin(2\pi \cdot f_{line} \cdot t)\left(1 - \frac{\%Ripple}{2}\right), \quad H_{min}(t) = \frac{0.4 \cdot \pi \cdot N \cdot I_{L.min}(t)}{l_e\ (cm)}$$ Eq. 20

$$B = \left(\frac{a + b \cdot H + c \cdot H^2}{1 + H + d \cdot H^2}\right)^x$$ Eq. 21

$a = 8.252*10^{2}$ $b = 1.236*10^{-1}$ $c = 2.017*10^{-2}$ $d = 1.689*10^{-2}$ $x = 2$

$$B_{max}(t) = \left(\frac{a + b \cdot H_{max}(t) + c \cdot H_{max}(t)^2}{1 + H_{max}(t) + d \cdot H_{max}(t)^2}\right)^x, \quad B_{min}(t) = \left(\frac{a + b \cdot H_{min}(t) + c \cdot H_{min}(t)^2}{1 + H_{min}(t) + d \cdot H_{min}(t)^2}\right)^x$$ Eq. 22

$$\Delta B(t) = \frac{B_{max}(t) - B_{min}(t)}{2}$$ Eq. 23

$$P_{core}(t) = \Delta B(t)^2 \cdot \left(\frac{f}{10^3}\right)^{1.46} \cdot V_e \cdot 10^{-6}$$ Eq. 24

Average core loss across the line cycle is:

$$P_{core.av} = f_{line} \cdot \int_0^{1/f_{line}} P_{core}(t)\, dt \quad = 1.9W$$ Eq. 25

3.4 CoolGaN™ features

CoolGaN™ transistors offer improved performance over silicon transistors (like SJ MOSFETs) due to several key characteristics:

- **Output charge Q_{OSS}:** Traditional silicon (Si) SJ 600 V power transistors have a very non-linear output charge characteristic. As V_{DS} is increased from 0 to about 25 V, the charge increases rapidly at a steep slope. Then suddenly the slope flattens out, and the charge only increases a small additional amount as V_{DS} is further increased all the way to 400 V or more. CoolGaN™ has a mostly linear characteristic, and the overall charge is much lower. Comparing the same $R_{DS(on)}$ CoolGaN™ with SJ, the CoolGaN™ Q_{OSS} is about 10 times lower. This is a significant benefit in soft-switching circuits, shortening the required dead-time and enabling higher-frequency operation without additional loss.

- **E_{OSS} – the energy stored in Q_{OSS}:** While the Q_{OSS} mentioned above is an order of magnitude improved in GaN compared to SJ, the difference in the energy stored in C_{OSS} is much smaller. This paradox is due to the non-linear nature of the output capacitance of SJ, where most of the charge is accumulated at low V_{DS} and therefore lower energy compared to the more linear capacitance of the GaN HEMT. The result is that E_{OSS} is a relatively modest 25 percent improvement compared to SJ. So the big advantage of GaN in hard-switching applications is not primarily that E_{OSS} is lower; the key benefit is that the GaN HEMT has no body diode recovery issues, so it can be applied effectively in hard-switching half-bridge applications like totem-pole PFC circuits operating in CCM and achieve extremely high efficiencies. This is covered in the next section.

- **Reverse-recovery charge Q_{rr}:** The reverse recovery performance of CoolGaN™ is perhaps the biggest single benefit of GaN compared to Si transistors. 600 V Si power transistors have intrinsic body diode structures with a large reverse recovery charge and associated peak current. It is so large that SJ is generally not applied to topologies or control strategies that include repetitive reverse recovery requirements, for example hard-switching half-bridge. CoolGaN™ transistors have no Qrr because there are no minority carriers in the channel to recover. Because of this, GaN enables a whole new class of topologies that, for the first time, can be effectively and efficiently deployed for improved performance.

- **Gate charge Q_g:** Gate charge affects how quickly the transistor can be switched on and off, and how frequently – as in the power required to operate the gate-drive circuit at high frequencies. Low gate charge is a desired characteristic in power transistors. Again, comparing CoolGaN™ to SJ with the same $R_{DS(on)}$, GaN has about seven times lower Q_g than SJ.

- **$R_{DS(on)}$ temperature coefficient:** The temperature coefficient of $R_{DS(on)}$ for CoolGaN™ is lower than for Si SJ. Over the range from 25°C to 150°C, the typical temperature coefficient of $R_{DS(on)}$ for GaN is 2.0, compared to 2.4 for SJ. The 20 percent difference in temperature coefficient means that for the same $R_{DS(on)}$ rating, the CoolGaN™ conduction losses will be lower at operating temperature. As a result of these key transistor characteristics, switched-mode power circuits using CoolGaN™ can benefit from improved energy efficiency and/or improved power density that is not possible with state-of-the-art Si devices.

3.5 CoolGaN™ power losses

Across the 60 Hz line cycle, each CoolGaN™ works as a boost switch for half-line cycle, then as a boost rectifier for the following half-line cycle, so we need to calculate the loss in both operational modes then average them to find the total loss per device across the full 60 Hz line cycle, as follows:

3.5.1 CoolGaN™ losses during operation as a boost switch

RMS current of a boost switch can be calculated by the following equation, and consequently the conduction loss can be obtained as:

$$I_{S.rms} = \frac{P_o}{V_{ac.HL}} \cdot \sqrt{1 - \frac{8 \cdot \sqrt{2} \cdot V_{ac.HL}}{3 \cdot \pi \cdot V_o}} = \frac{2500\ W}{230\ V} \cdot \sqrt{1 - \frac{8 \cdot \sqrt{2} \cdot 230V}{3 \cdot \pi \cdot 390V}} = 5.9\ A$$ Eq. 26

$$P_{S.cond} = {I_{S.rms}}^2 \cdot R_{on(80℃)} = 5.9^{\,2} \cdot (0.055 \cdot 1.4) = 2.7\ W$$ Eq. 27

$(Assuming\ R_{on(80℃)} = 1.4 \cdot R_{on(25℃)})$

For switching turn-on and turn-off losses, the typical equations used for calculating switching times and losses become inaccurate in fast-switching CoolGaN™, due to the high di/dt effects associated with package and PCB parasitics. Therefore, characterization of turn-on and turn-off losses in an experimental set-up would be more realistic, as shown in Figure 8 (left). The total turn-on and turn-off equation as a function of switching current is as shown in Figure 8 (right).

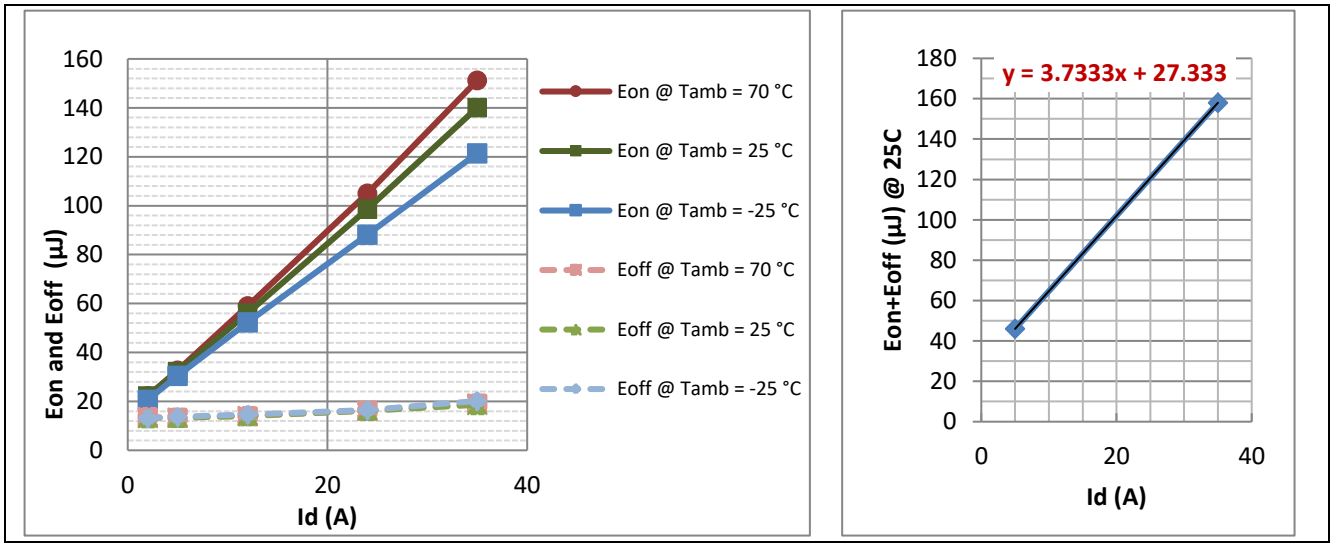


Figure 8 IGO60R070D1 switching losses at different temperatures, V_{DS} = 400 V, R_g = 10.5 Ω

Since the switching current in a PFC application varies across the AC-line cycle, the average inductor current can be used to calculate the average switching losses across the AC-line cycle.

The average input current is given as:

$$I_{L.avg} = \frac{P_o}{V_{ac.HL}} \cdot \frac{2 \cdot \sqrt{2}}{\pi} = \frac{2500\ W}{230\ V} \cdot \frac{2 \cdot \sqrt{2}}{\pi} = 9.8\ A$$ Eq. 28

From Figure 8 (right), E_{on} + E_{off} is:

$$E_{on,off} = 3.7333 \cdot I_{L.avg} + 27.333 = 63.9\ \mu J$$ Eq. 29

Note: Because $E_{on,off}$ was extracted experimentally, it includes the output capacitace switching loss (E_{oss}).

Turn-on and turn-off switching loss:

$$P_{S.sw} = E_{on,off} \cdot f = 63.9\mu J \cdot 65 \cdot 10^3 Hz = 4.15\ W$$ Eq. 30

Gate drive loss:

In addition to the charge required to drive the gate from 0 V to 3 V (gate diode forward voltage, $V_{f,gs}$) to turn on the CoolGaN™, a steady-state gate current of several mA is also needed to keep the gate diode fully

biased in the forward direction, so the transistor has sufficient saturation drain current. Assuming a steady-state gate current (I_{ss}) of 10 mA and a gate diode forward voltage ($V_{f,gs}$) of 3V, then gate drive loss is:

$$P_{S.g} = V_{f,gs} \cdot Q_g \cdot f + I_{ss} \cdot V_{f,gs} \cdot Average\ duty\ cycle \qquad \text{Eq. 31}$$
$$= 3\,V \cdot 5.8nC \cdot 65 \cdot 10^3 Hz + 10mA \cdot 3V \cdot 0.469 = 0.015\,W$$

$$Average\ duty\ cycle = 1 - \frac{2 \cdot \sqrt{2} \cdot V_{ac.HL}}{\pi \cdot V_o} = 1 - \frac{2 \cdot \sqrt{2} \cdot 230V}{\pi \cdot 390V} = 47\%$$

Total loss during the boost switch mode (half-line cycle):

$$P_{S.total} = P_{S.cond} + P_{S.sw} + P_{S.oss} + P_{S.g} = 6.8\,W \qquad \text{Eq. 32}$$

3.5.2 CoolGaN™ losses during operation as a boost rectifier

The switch operation as a rectifier will have conduction loss, reverse conduction loss and gate drive loss. Other switching losses do not apply in this mode because the channel turns on and off at ZVS condition and the reverse conduction has no reverse recovery charge.

Conduction loss when the channel is turned on can be calculated by the following equations:

$$I_{R.rms} = \frac{P_o}{V_{ac.HL}} \cdot \sqrt{\frac{8 \cdot \sqrt{2} \cdot V_{ac.HL}}{3 \cdot \pi \cdot V_o}} = \frac{2500\,W}{230\,V} \cdot \sqrt{\frac{8 \cdot \sqrt{2} \cdot 230V}{3 \cdot \pi \cdot 390V}} = 9.15\,A \qquad \text{Eq. 33}$$

$$P_{R.cond} = I_{S.rms}^2 \cdot R_{on,80°C} = (9.15\text{A})^2 \cdot 0.055\,\Omega \cdot 1.4 = 6.4\,W \qquad \text{Eq. 34}$$

$$Assuming\ R_{on,80°C} = 1.4 \cdot R_{on,25°C}$$

When the channel is turned off, the CoolGaN™ switch operates in reverse conduction mode (third quadrant) during the dead-times. Typically the associated conduction loss is small; however, in higher switching frequency applications, the dead-time percentage of the switching period becomes higher, and its associated power loss becomes noticeable.

The average inductor current $I_{L.avg}$ = 9.8A (Eq. 28) passes through the reverse conduction voltage drop (V_{SD}) during the dead-times before turn-on and after turn-off. V_{SD} is dependent on the negative gate voltage during off-time, as shown in Figure 9. From the figure, we can see V_{SD} is equal to ~8.4 V at I_{SD} = 9.8 A, V_{GS} = -6 V, therefore the reverse conduction loss can be calculated as:

$$P_{R.reverse.cond} = 2 \cdot I_{L.avg} \cdot V_{SD} \cdot DeadTime \cdot f = 2 \cdot 9.8A \cdot 8.4V \cdot 100ns \cdot 65kHz = 1.1\text{W} \qquad \text{Eq. 35}$$

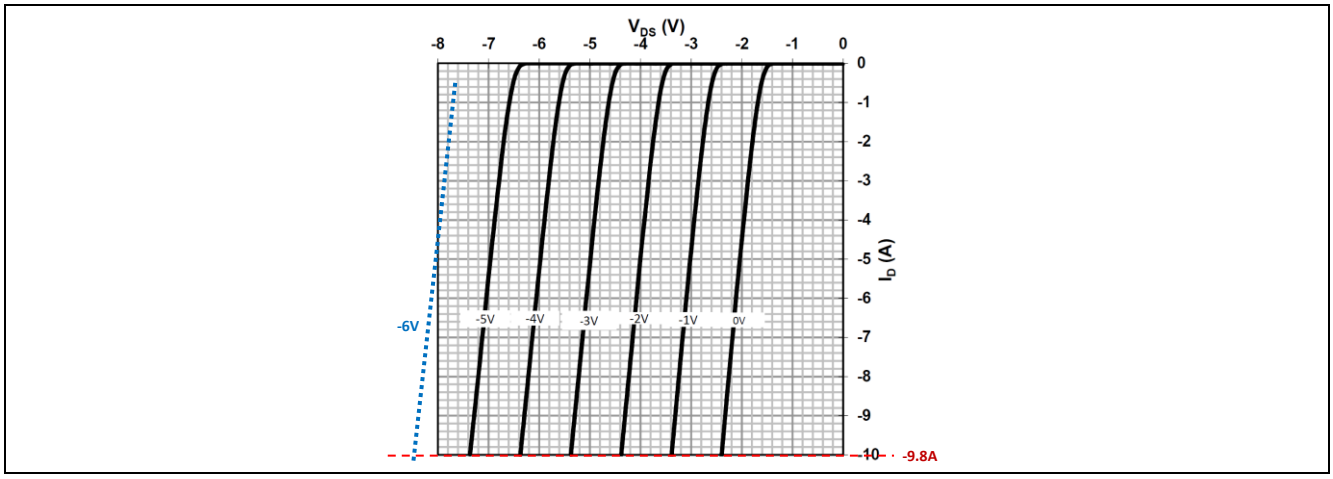


Figure 9 CoolGaN™ reverse characteristics, $V_{DS} = f(I_D, V_{GS})$, $T_j = 25°C$

Gate drive loss is defined as:

$$P_{S.g} = V_{f,gs} \cdot Q_g \cdot f + I_{ss} \cdot V_{f,gs} \cdot (1 - Average\ duty\ cycle) \quad \text{Eq. 36}$$
$$= 3\,V \cdot 5.8nC \cdot 65 \cdot 10^3 Hz + 10mA \cdot 3V \cdot (1 - 0.469) = 0.017\,W$$

$$Average\ duty\ cycle = 1 - \frac{2 \cdot \sqrt{2} \cdot V_{ac.HL}}{\pi \cdot V_o} = 1 - \frac{2 \cdot \sqrt{2} \cdot 230V}{\pi \cdot 390V} = 47\%$$

Total loss during the rectifier switch mode (half-line cycle):

$$P_{R.total} = P_{R.cond} + P_{R.g} + PR.reverse.cond = 7.5\,W \quad \text{Eq. 37}$$

Total CoolGaNTM loss across a full line cycle:

$$P_{CoolGaN.total} = \frac{P_{S.total} + P_{R.total}}{2} = 7.2W \quad \text{Eq. 38}$$

3.6 Line rectifier MOSFET

The line rectifier chosen is CoolMOS™ IPT65R033G7. Each rectifier MOSFET conducts for half the line cycle to carry the line current, and only conduction loss is considered since it operates at line frequency.

RMS current and conduction loss are:

$$I_{CoolMOS.rms} = \frac{P_o}{V_{ac.HL}} \cdot \sqrt{0.5} = \frac{2500\,W}{390\,V} \cdot \sqrt{0.5} = 7.7A \quad \text{Eq. 39}$$

$$P_{CoolMOS.cond} = {I_{CoolMOS.rms}}^2 \cdot R_{on(80°C)} = (7.7\,A)^2 \cdot 0.029\,\Omega \cdot 1.6 = 2.4\,W \quad \text{Eq. 40}$$

$Assuming\ R_{on,40°C} = 1.4 \cdot R_{on,25°C}$

3.7 Output capacitor

The output capacitor is sized to meet both the hold-up time and the low-frequency voltage ripple requirements. The capacitor value is selected to have the larger value among the two equations, below:

$$C_o \geq \frac{2 \cdot P_o \cdot t_{hold}}{{V_o}^2 - {V_{o.min}}^2} = \frac{2 \cdot 2500W \cdot 8.33 \cdot 10^{-3} sec}{(390V)^2 - (340V)^2} = 1141\,\mu F \quad \text{Eq. 41}$$

$$C_o \geq \frac{P_o}{2 \cdot \pi \cdot f_{line} \cdot \Delta V_o \cdot V_o} = \frac{2500W}{2 \cdot \pi \cdot 60Hz \cdot 10V \cdot 390V} = 850\,\mu F \quad \text{Eq. 42}$$

$$\rightarrow C_o = max\ (2283\,\mu F, 1700\,\mu F) = 1141\ \mu F$$

In this design we used two parallel 560 µF, 450 V, with dissipation factor ($\tan\delta$) of 0.2; consequently the capacitor ESR loss is obtained as:

$$ESR = \frac{DF}{2 \cdot \pi \cdot f \cdot C_o} = \frac{0.2}{2 \cdot \pi \cdot 120Hz \cdot (2 \cdot 560\,\mu F)} = 0.237\,\Omega \quad \text{Eq. 43}$$

The capacitor RMS current and power loss across the line cycle can be calculated by the following equations:

$$I_{Co.rms} = \sqrt{\frac{8 \cdot \sqrt{2} \cdot {P_o}^2}{3 \cdot \pi \cdot V_{ac.HL} \cdot V_o} - \frac{{P_o}^2}{{V_o}^2}} = \sqrt{\frac{8 \cdot \sqrt{2} \cdot (2500\,W)^2}{3 \cdot \pi \cdot 230V \cdot 390\,V} - \frac{(2500\,W)^2}{(390\,V)^2}} = 6.5\,A \quad \text{Eq. 44}$$

$$P_{Co} = {I_{Co.rms}}^2 \cdot ESR = (6.5A)^2 \cdot 0.237\ \Omega = 10.1\ W$$ Eq. 45

4 Totem-pole controller using ICE3PCS01G

The totem-pole control is realized using ICE3PCS01G analog CCM PFC boost controller, which achieves a stable operation across the complete load range and reasonable PFC, as well as handling of fault events.

To satisfy the special requirements of the totem-pole PFC circuit, the behavior of the classic boost PFC controller has been extended with additional logic gates. Thus, additional features such as the phase rectification of the low-frequency half-bridge (switching with 50 Hz or 60 Hz respectively) can be supported. The phase recification and the blanking of the PWM operation for the GaN half-bridge were realized with digital gates on the “gate” output of the ICE3 control IC. The dead-time settings are controlled with RC time constants and a comparator.

4.1 Zero crossing detection

A simple V AC zero crossing circuit is used to provide the required signal to exchange the PWM signal between the high-side and low-side switch over the sinusoidal grid input voltage.

4.2 Signal generation for CoolGaN™ boost switch, CoolGaN™ boost rectifier and CoolMOS™ line rectifier

A logic circuitry add-on to the analog controller circuit is used to accurately and correspondingly generate all CoolGaN™ and CoolMOS™ PWM signals from a single PFC gate signal depending on the line voltage polarity.

4.3 Zero current turn-off and zero window comparator

This circuit prevents the PWM signal from being applied to the power switches for approximately 100 µs during a zero crossing of the grid voltage to maintain exchange of the high-side and low-side PWM signals. This leads to elimination of possible cross-conduction in the half-bridge configuration.

4.4 True DCM monitor/enabler

As the ICE3PCS01G controller is originally designed for a classic or traditional PFC topology where a MOSFET is switching against a SiC Schottky diode, in order to fit this controller to the CCM totem-pole topology, a fast comparator is needed to prevent a negative current flow in the PFC choke during DCM operation.

4.5 Current sensing approach

A cost-effective and simple approach to the current sensing for the controller is depicted in Figure 14.

As GND_iso is referenced to HB2 and not to V_{BULK}; a differential rectification sensing circuit must be used to provide the V AC voltage to the PFC controller.

More details on the controller implementation are available in the “2500 W full-bridge totem-pole power factor correction using CoolGaN™” application note.
https://www.infineon.com/dgdl/InfineonApplicationNote_EvaluationBoard_CoolGaN_2500W_CCM_Totem-Pole_PFC-AN-v03_00-EN.pdf?fileId=5546d46262b31d2e016368e4dd3b070b

5 Experimental and modeling results

The design example discussed in this document was modeled in Mathcad®. All of the power loss equations were written as a function of the output power in order to be able to plot an estimated efficiency curve across the output power range, as shown in Figure 10 (left). The experimental efficiency curve of this design example (evaluation board) was tested as shown in Figure 10 (right). It is clear that the theoretical curve is close enough to the experimental curve, therefore verifying the modeling equations used.

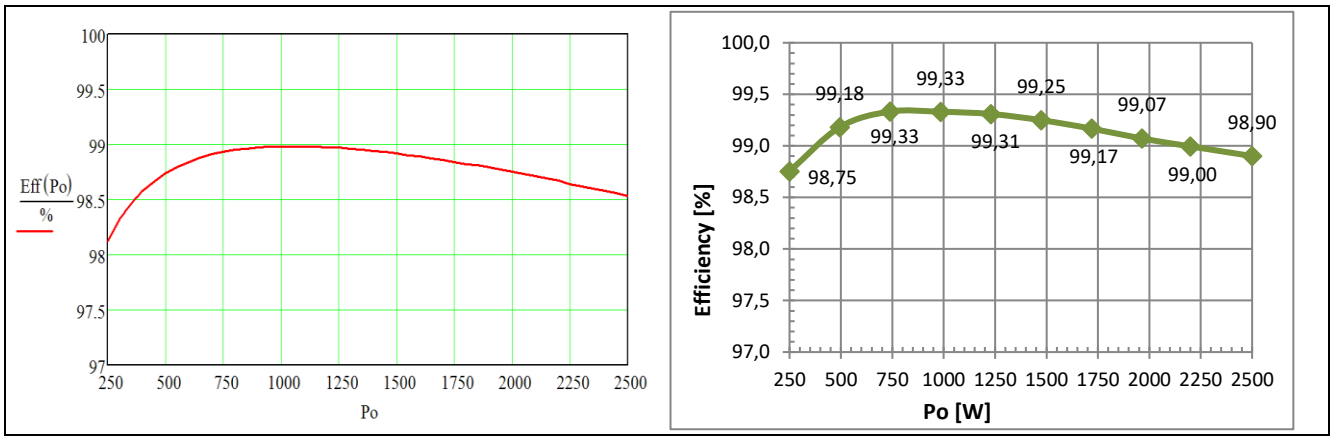


Figure 10 Calculated efficiency (left) vs. experimental efficiency (right) at 230 V AC

Figure 11 shows a breakdown of main power losses at the 230 V, 50 percent and 100 percent load conditions.

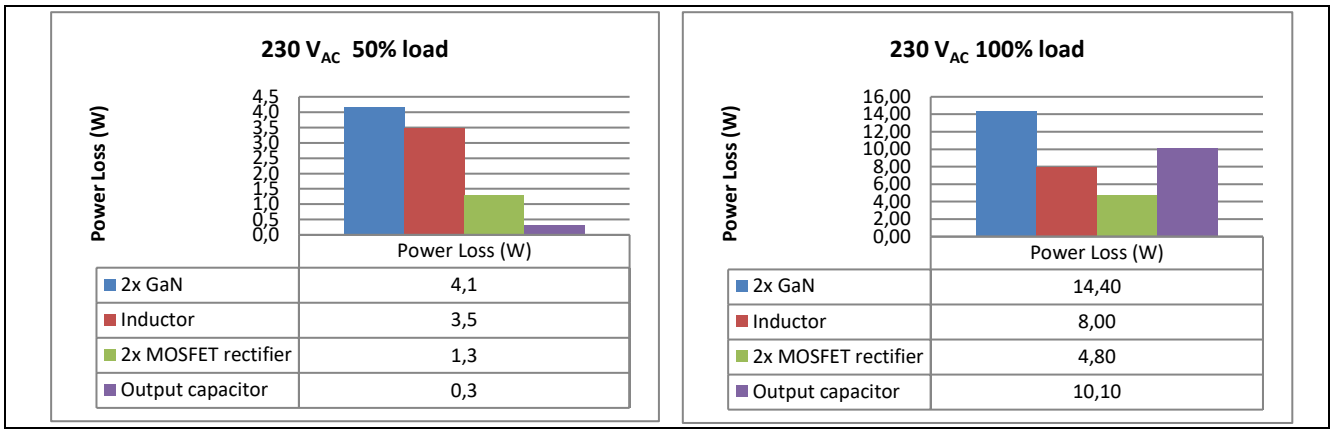


Figure 11 Breakdown of main power losses at 50 percent and 100 percent load conditions

Figure 12 shows a breakdown of the GaN power losses at the 230 V, 50 percent and 100 percent load conditions.

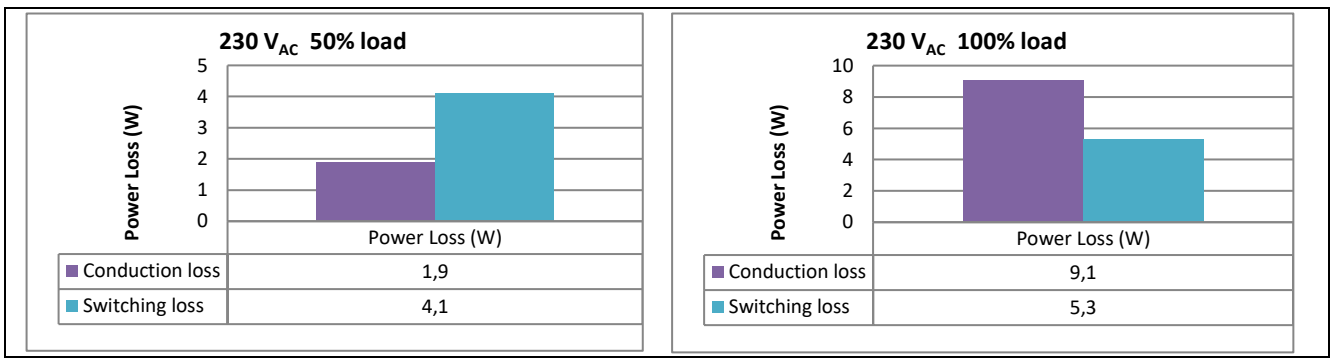


Figure 12 GaN power losses breakdown at 230 V, 50 percent and 100 percent load conditions

6 Board design

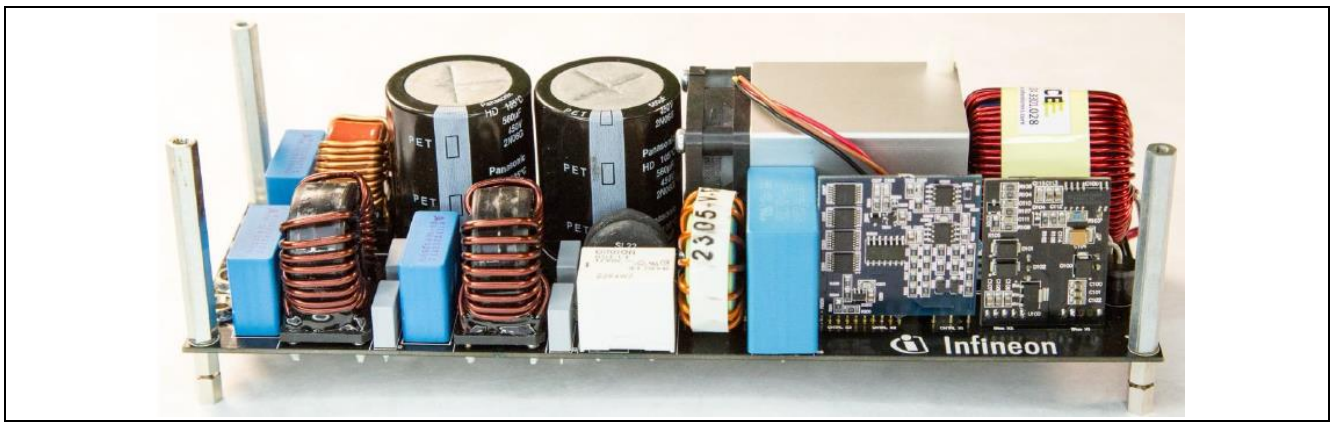


Figure 13 Evaluation board

6.1 Schematics

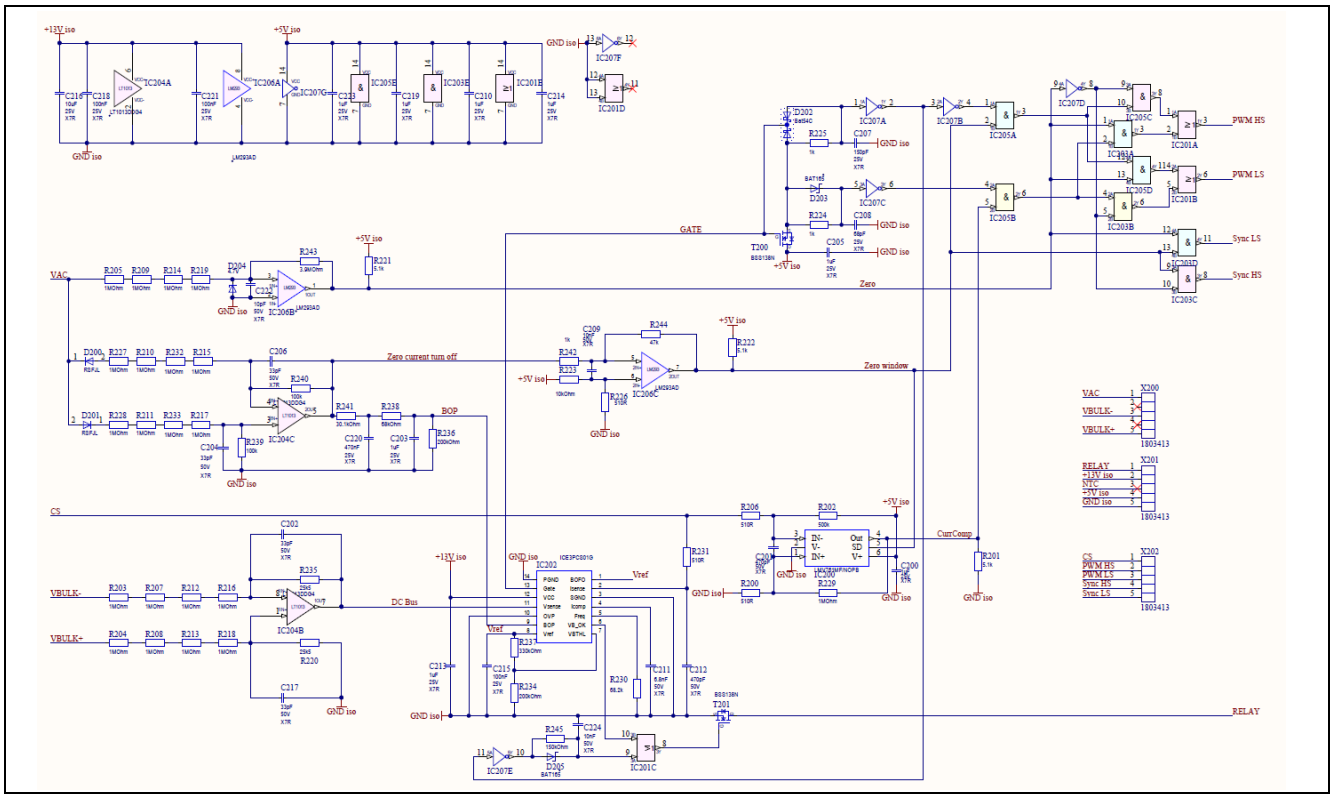


Figure 14 Control board schematic

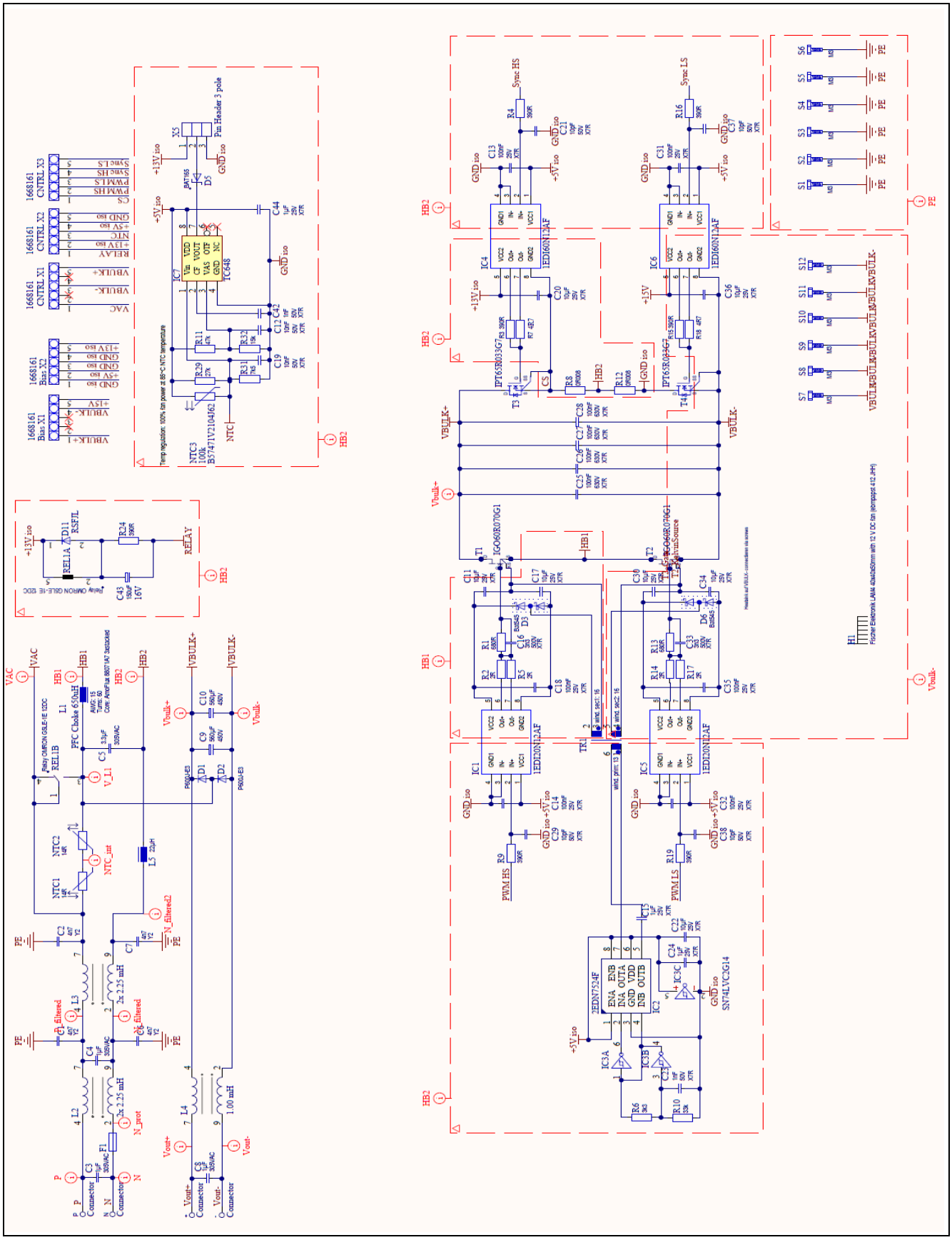


Figure 15 Main board schematic

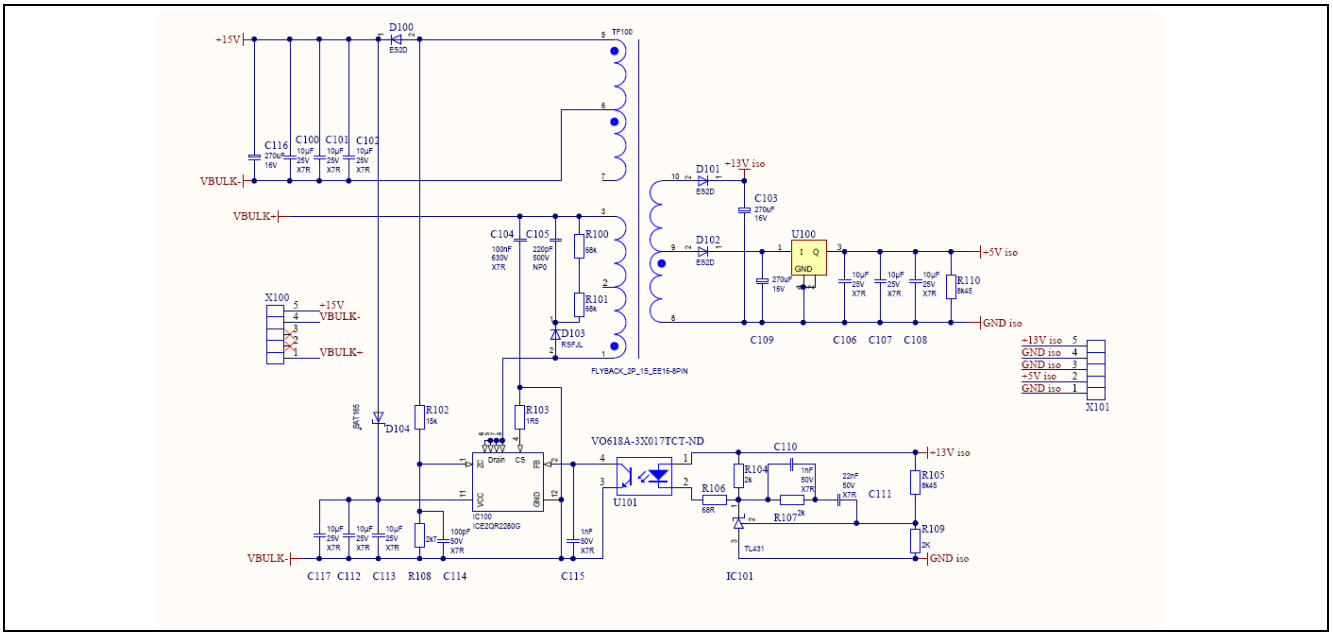


Figure 16 Bias board schematic

More details on the board design and Bill of Materials (BOM) are available in the “2500 W full-bridge totem-pole power factor correction using CoolGaN™” application note.
https://www.infineon.com/dgdl/InfineonApplicationNote_EvaluationBoard_CoolGaN_2500W_CCM_Totem-Pole_PFC-AN-v03_00-EN.pdf?fileId=5546d46262b31d2e016368e4dd3b070b

7 References

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[2] Gallium nitride – CoolGaN™ 600 V e-mode HEMTs – Infineon Technologies Application Note.

https://www.infineon.com/dgdl/Infineon-ApplicationNote_CoolGaN_600V_emode_HEMTs-AN-v01_00-EN.pdf?fileId=5546d46262b31d2e016368e4cab10701

[3] PFC boost converter design guide – Infineon Technologies Application Note.

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[4] ICE3PCS01G controller datasheet.

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8 Symbols used in formulas

Table 3 Symbols used in formulas

V_{AC}	Input voltage
V_{OUT}	Output voltage
P_{OUT}	Output power
f	Switching frequency
T	Switching time period
f_{line}	Line frequency
L	Filter inductor
%Ripple	Inductor current ripple percentage of input current
DCR	Inductor DC resistance
$R_{on(100C)}$	MOSFET on-resistance at 100°C
Q_g	MOSFET total gate charge
R_g	MOSFET gate resistance
E_{OSS}	MOSFET output capacitance switching energy
ESR	Output capacitor resistance
t_{hold}	Hold-up time
$V_{o.min}$	Hold-up minimum output voltage
ΔV_{OUT}	Output voltage ripple

Revision history

Major changes since the last revision

Page or reference	Description of change
–	First release

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