Application note

ANPS0045 - ICE2QS03G

Converter Design Using Quasi-resonant PWM Controller ICE2QS03G

Power Management & Supply



Never stop thinking.

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Infineon Technologies AG
81726 Munich, Germany
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Title: ICE2QS03G Design Guide

Revision History:	**7 April 2010**	**V1.0**
Previous Version:	none	
Page	Subjects (major changes since last revision)	

Converter design using the quasi-resonant PWM controller ICE2QS03G
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Table of Contents

1 Introduction 5
2 IC description 5
2.1 Main features 5
2.2 Pin layout 5
2.3 Pin functions 5
2.3.1 ZC (Zero Crossing) 6
2.3.2 FB (Feedback) 6
2.3.3 CS (Current Sensing) 6
2.3.4 Gate (Gate drive output) 6
2.3.5 HV (High voltage) 6
2.3.6 VCC (Power supply) 6
2.3.7 GND (Ground) 6
3 Overview of quasi-resonant flyback converter 6
4 Functions and Application Overview 8
4.1 VCC Pre-Charging and Typical VCC Voltage During Start-up 8
4.2 Soft-Start 9
4.3 Normal Operation 9
4.3.1 Switch-on Determination 9
4.3.2 Switch-off Determination 10
4.4 Active Burst Mode Operation 11
4.4.1 Entering Active Burst Mode Operation 11
4.4.2 During Burst Mode Operation 11
4.4.3 Leaving Active Burst Mode 12
4.5 Current sense 12
4.6 Feedback 12
4.7 Zero crossing 12
4.8 Gate drive 13
4.9 Others 13
5 Typical application circuit 14
6 References 14

1 Introduction

This application notes describes how to design quasi-resonant flyback converters using ICE2QS03G, which is a new Quasi-resonant PWM controller developed by Infineon Technologies
In this application note, The basic description of IC will be given first including the main features and Pin's layout. Then an overview of quasi-resonant flyback converter will be given, followed by the introduction of ICE2QS03G's functions and operations. Some application examples and hints will be given in the last part of this document.

2 IC description

ICE2QS03G is a second generation quasi-resonant PWM controller optimized for off-line power supply applications such as LCD TV, and notebook adapter. The digital frequency reduction with decreasing load enables a quasi-resonant operation till very low load. As a result, the system average efficiency is significantly improved compared to conventional solutions. The active burst mode operation enables ultra-low power consumption at standby mode operation and low output voltage ripple. The numerous protection functions give a full protection of the power supply system in failure situation. All of these make the ICE2QS03G an outstanding controller for quasi-resonant flyback converter in the market.
In addition, numerous protection functions have been implemented in the IC to protect the system and customize the IC for the chosen applications. All of these make the ICE2QS03G an outstanding product for real quasi-resonant flyback converter in the market.

2.1 Main features

- Quasi-resonant operation
- Load dependent digital frequency reduction
- Active burst mode for light load operation
- Built-in high voltage startup cell
- Built-in digital soft-start
- Cycle-by-cycle peak current limitation with built-in leading edge blanking time
- Foldback Point Correction with digitalized sensing and control circuits
- VCC undervoltage and overvoltage protection with Autorestart mode
- Over Load /open loop Protection with Autorestart mode
- Built-in Over temperature protection with Autorestart mode
- Adjustable output overvoltage protection with Latch mode
- Short-winding protection with Latch mode
- Maximum on time limitation
- Maximum switching period limitation

2.2 Pin layout

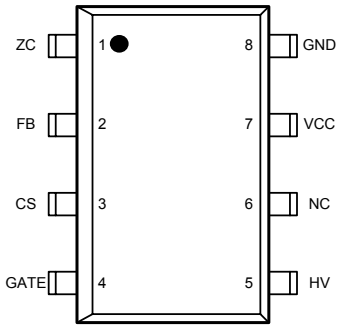


Figure 1 Pin configurations (top view)

2.3 Pin functions

2.3.1 ZC (Zero Crossing)

Three functions are incorporated at the ZC pin. First, during MOSFET off time, the de-magnetization of the transformer is detected when the ZC voltage falls below V_{ZCCT} (100mv). Second, after the MOSFET is turned off, an output overvoltage fault will be assumed if V_{ZC} is higher than V_{ZCOVP} (3.7V). Finally, during the MOSFET on time, a current depending on the bus voltage flows out of this pin. Information on this current is then used to adjust the maximum current limit. More details on this function are provided in Section 4.

2.3.2 FB (Feedback)

Usually, an external capacitor is connected to this pin to smooth the feedback voltage. Internally, this pin is connected to the PWM signal generator for switch-off determination (together with the current sensing signal), and to the digital signal processing for the frequency reduction with decreasing load during normal operation. Additionally, the openloop/overload protection is implemented by monitoring the voltage at this pin.

2.3.3 CS (Current Sensing)

This pin is connected to the shunt resistor for the primary current sensing, externally, and the PWM signal generator for switch-off determination (together with the feedback voltage), internally. Moreover, short-winding protection is realised by monitoring the V_{cs} voltage during on-time of the main power switch.

2.3.4 Gate (Gate drive output)

The GATE pin is the output of the internal driver stage, which has a rise time of 117ns and a fall time of 27ns when driving a 1nF capacitive load.

2.3.5 HV (High voltage)

The HV pin provides startup current to the IC by connecting this pin to the high voltage bus directly. Internally, a 500V depletion startup cell is integerated which omits the external startup resistor to achieve low standby power loss.

2.3.6 VCC (Power supply)

The VCC pin is the positive supply of the IC and should be connected to auxiliary winding of the main transformer.

2.3.7 GND (Ground)

This is the common ground of the controller

3 Overview of quasi-resonant flyback converter

Figure shows a typical application of ICE2QS03G in quasi-resonant flyback converter. In this converter, the mains input voltage is rectified by the diode bridge and then smoothed by the capacitor C_{bus} where the bus voltage V_{bus} is available. The transformer has one primary winding W_p, one or more secondary windings (here one secondary winding W_s), and one auxiliary winding W_a. When quasi-resonant control is used for the flyback converter, the typical waveforms are shown in Figure 3. The voltage from the auxiliary winding provides information about demagnetization of the power transformer, the information of input voltage and output voltage.

As shown in Figure 3, after switch-on of the power switch the voltage across the shunt resistor V_{CS} shows a spike caused by the discharging of the drain-source capacitor. After the spike, the voltage V_{CS} shows information about the real current through the main inductance of the transformer L_p. Once the measured current signal V_{CS} exceeds the maximum value determined by the feedback voltage V_{FB}, the power switch is turned off. During this on-time, a negative voltage proportional to the input bus voltage is generated across the auxiliary winding.

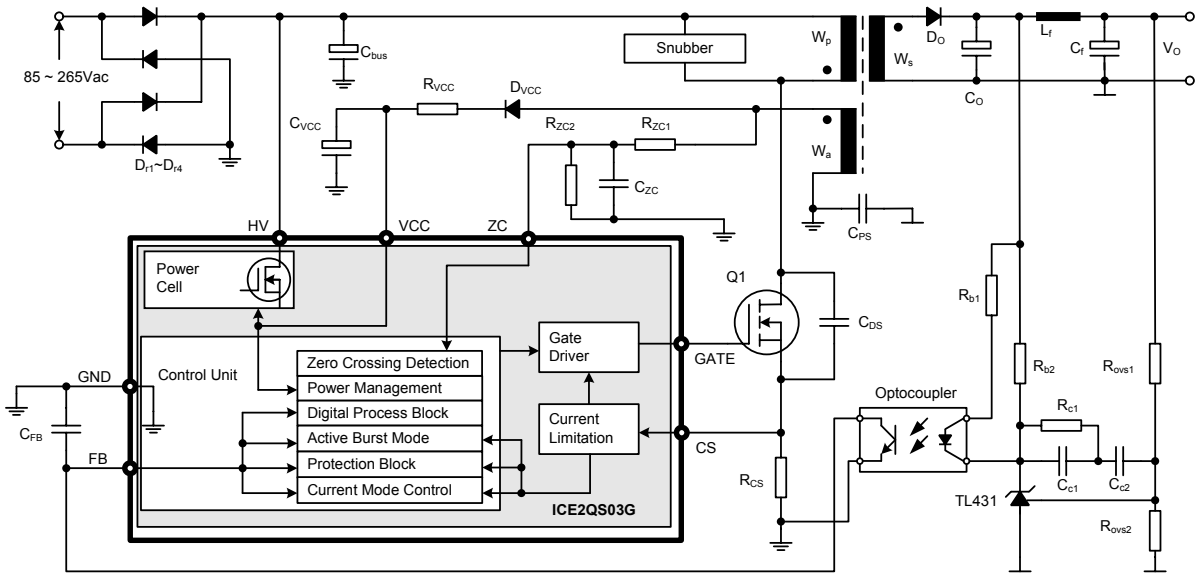


Figure 2 Typical Application of ICE2QS03G

The drain-source voltage of the power switch v_{ds} will rise very fast after MOSFET is turned off. This is caused by the energy stored in the leakage inductance of the transformer. A snubber circuit, RCD in most cases, can be used to limit the maximum drain source voltage caused. After the oscillation 1, the drain-source voltage goes to its steady value. Here, the voltage v_{Refl} is the reflected value of the secondary voltage at the primary side of the transformer and is calculated as:

$$V_{Refl} = \frac{V_{out} + V_{do}}{n} \quad (1)$$

where n the turns ratio of the transformer, which is defined in this document as:

$$n = N_S/N_P \quad (2)$$

with N_p and N_s are the turns count of the primary and secondary winding, respectively.

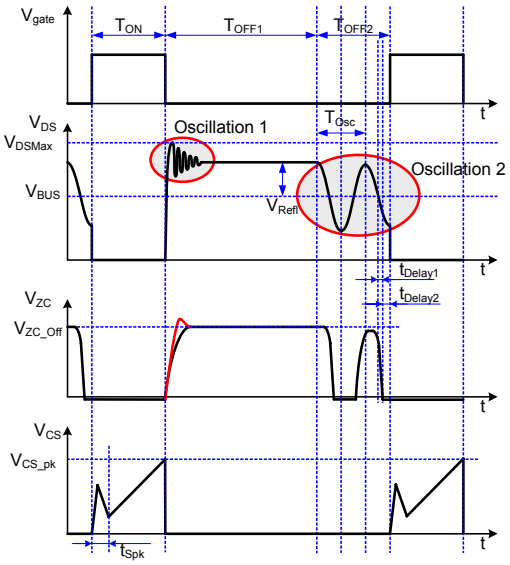


Figure 3 Key waveforms of a quasi-resonant flyback converter

After the oscillation 1 is damped, the drain-source voltage of the power switch shows a constant value of v_{bus}+v_{Refl} until the transformer is fully demagnetized. This duration builds up the first portion of the off-time T_{OFF1}.

After the secondary side current falls to zero, the drains-source voltage of the power switch shows another oscillation (oscillation 2 in Figure 3, this is also mentioned as the main oscillation in this document). This oscillation happens in the circuit consisting of the equivalent main inductance of the transformer L_p and the capacitor across the drain-source (or drain-ground) terminal C_{DS}. The frequency of this oscillation is calculated as:

$$f_{OSC} = \frac{1}{2\pi\sqrt{L_P \cdot C_{DS}}} \quad (3)$$

The amplitude of this oscillation begins with a value of v_{Refl} and decreases exponentially with the elapsing time, which is determined by the losses factor of the resonant circuit. The first minimum of the drain voltage appears at the half of the oscillation period after the time t_4 and can be apporximated as:

$$V_{dsMin} = V_{bus} - V_{Refl} \quad (4)$$

In the quasi-resonant control, the power switch is switched on at the minimum of the drain-source voltage. From this kind of operation, the switching-on losses are minimized, and switching noise due to dv_{ds}/dt is reduced compared to a normal hard-switching flyback converter.

4 Functions and Application Overview

4.1 VCC Pre-Charging and Typical VCC Voltage During Start-up

In the controller ICE2QS03G, a power cell is integrated and it consists of a 500V high voltage device and a controller, whereby the high voltage device is controlled by the controller. The power cell provides a pre-charging of the VCC capacitor till VCC voltage reaches the VCC turned-on threshold V_{VCCon} and the IC begins to operate, while it may keep the VCC voltage at a constant value during burst mode operation when the output voltage is pulled down or the power from the auxiliary winding is not enough, or when the IC is latched off in certain protection mode.

Once the mains input voltage is applied, a rectified voltage shows across the capacitor C_{bus}. The high voltage device provides a current to charge the VCC capacitor C_{vcc}. Before the VCC voltage reaches a certain value, the amplitude of the current through the high voltage device is only determined by its channel resistance and can be as high as several mA. After the VCC voltage is high enough, the controller controls the high voltage device so that a constant current around 1mA is provided to charge the VCC capacitor further, until the VCC voltage exceeds the turned-on threshold V_{VCCon}. As shown as the time phase I in Figure 4, the VCC voltage increase nearly linearly.

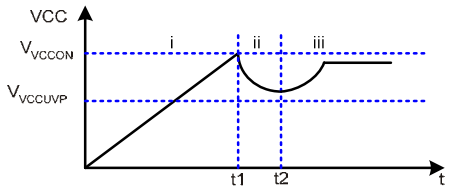


Figure 4 VCC voltage at start up

The time taken for the charging VCC to turn-on threshold can then be approximately calculated as:

$$t_1 = \frac{V_{VCCon} \cdot C_{VCC}}{I_{VCCcharge2}} \quad [5]$$

where $I_{VCCcharge2}$ is the charging current from the power cell which is 1.05mA, typically.
When the VCC voltage exceeds the turned-on threshold V_{VCCon} of at time t_1, the power cell is switched off, and the IC begins to operate with a soft-start. Because the energy from the auxiliary winding is not enough to supply the IC operation when output voltage is low, the VCC voltage drops (Phase II). Once the output voltage is high enough, the VCC capacitor receives energy from the auxiliary winding from the time point t_2 on. The VCC voltage will then reach a constant value depending on output load.
Since there is a VCC undervoltage protection, the capacitance of the VCC capacitor should be selected to be high enough to ensure that enough energy is stored in the VCC capacitor so that the VCC voltage will never touch the VCC under voltage protection threshold V_{VCCUVP} before the output voltage is built up. Therefore, the capacitance should fulfill the following requirement:

$$C_{VCC} \geq \frac{I_{VCCop} \cdot (t_2 - t_1)}{V_{VCCon} - V_{VCCUVP}} \quad [6]$$

with I_{VCCop} the operating current of the controller.

4.2 Soft-Start

After IC supply voltage is higher than 18V, which corresponding to t1 of Fig.3, IC will start switch with a soft start. The soft start function is built inside the IC in a digital manner. During softstart, the peak current of the MOSFET is controlled by an internal voltage reference instead of the voltage on FB pin. The maximum voltage on CS pin for peak current control is increased step by step as shown in Figure 5. The maximum duration of softstart is 12ms with 4ms for each step.
During softstart, the over load protection function is disabled.

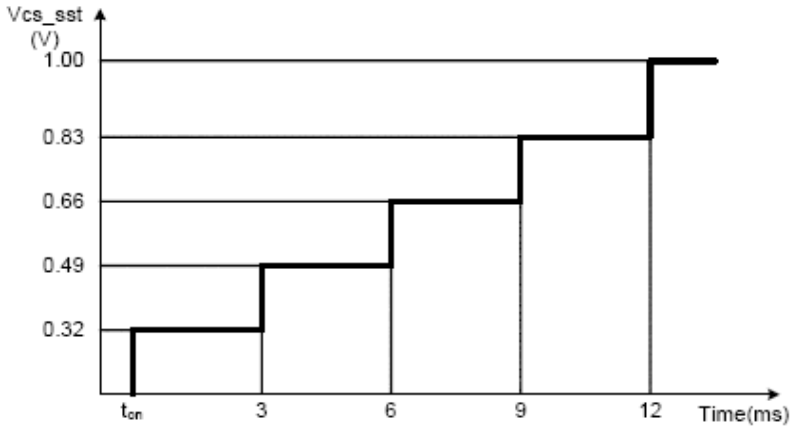


Figure 5 Maximum current sense voltage during softstart

4.3 Normal Operation

The PWM section of the IC can be divided into two main portions: PWM controller for normal operation and PWM controller for burst mode operation. The PWM controller for normal operation will be described in the following paragraphs, while the PWM controller for burst mode operation will be discussed in the next section. The PWM controller for normal operation consists of digital signal processing circuit including an up/down counter, a zero-crossing counter (ZC-counter) and a comparator, and analog circuit including a current measurement unit and a comparator. The switch-on and -off time point is determined by the digital circuit and the analog circuit, respectively. As input information for the switch-on determination, the zero-crossing input signal and the value of the up/down counter are needed, while the feedback signal v_{REG} and the current sensing signal v_{CS} are necessary for the switch-off determination. Details about the operation of the PWM controller in normal operation are illustrated in the following paragraphs.

4.3.1 Switch-on Determination

As mentioned above, the digital signal processing circuit consists of an up/down counter, a zero-crossing counter and a comparator. A ringing suppression time controller is implemented to avoid mistriggering by the ring after MOSFET is turned off. Functionality of these parts is described as in the following.

4.3.1.1 Up/down Counter

The up/down counter stores the number of zero crossing to be ignored before the main power switch is switched on after demagnetisation of the transformer. This value is a function of the regulation voltage, which contains information about the output power. Generally, a high output power results in a high regulation voltage. According to this information, the value in the up/down counter is changed to a low value in case of high regulation voltage, and to a high value in case of low regulation voltage. In ICE2QS03G, the lowest value of the counter is 1 and the highest 7. Following text explains how the up/down counter value changes in response to the regulation voltage v_{REG}. The regulation voltage v_{REG} is internally compared with three

thresholds V_{RL}, V_{RH} and V_{RM}. According to the results, the value in the up/down counter is changed, which is summarised in Table 1 and Figure 6 respectively.
According to the comparison results the up/down counter counts upwards, keeps unchanged or counts downwards. However, the value in up/down counter is limited between 1 and 7. If the counter tends to count beyond this range, the attempt is ignored.
In normal case, the up/down counter can only be changed by one each time at the clock period of 48ms. However, to ensure a fast response to load increase, the counter is set to 1 in the following switching period after the regulation voltage v_{REG} exceeds the threshold V_{RM}.

Table 1 Operation of the up/down counter

V_{REG}	Up/down counter action
Always lower than V_{RL}	Count upwards until 7
Once higher than V_{RL}, but always lower than V_{RH}	No changes
Once higher than V_{RH}, but always lower than V_{RM}	Count downwards until 1
Once higher than V_{RM}	Counter set to 1

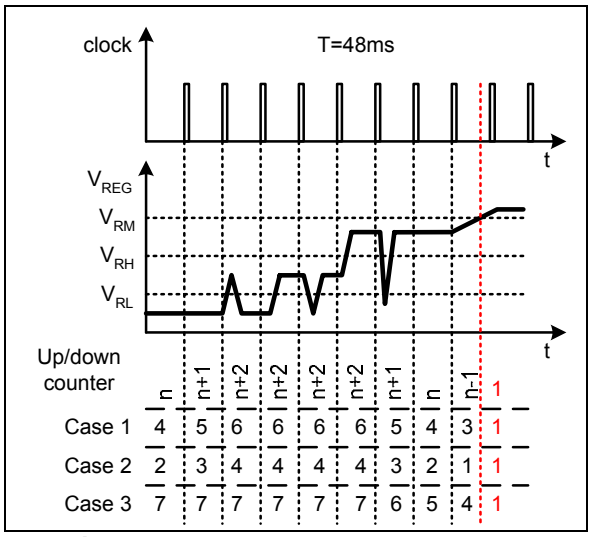


Figure 6 Up/down counter operation

4.3.1.2 Switch-on Determination

In the system, turn-on of the power switch depends on the value of the up/down counter, the value of the zero-crossing counter and the voltage at the ZC pin v_{ZC}. Turn-on happens only when the value in the both counters are the same and the voltage at the ZC is lower than the threshold V_{ZCCT}. For comparison of the values from both counters, a digital comparator is used. Once these counters have the same value, the comparator generates a signal which sets the on/off flip-flop, only when the voltage v_{ZC} is lower than the threshold V_{ZCCT}.
Another signal which may trigger the digital comparator is the output of a T_{sMax} clock signal, which limits the maximum off time to avoid the low-frequency operation.
During active burst mode operation, the digital comparator is disabled and no pulse will be generated.

4.3.2 Switch-off Determination

In the converter system, the primary current is sensed by an external shunt resistor, which is connected between low-side terminal of the main power switch and the common ground. The sensed voltage across the shunt resistor v_{CS} is applied to an internal current measurement unit, and its output voltage v_1 is compared with the regulation voltage v_{reg}. Once the voltage v_1 exceeds the voltage v_{REG}, the output flip-flop is reset. As a result, the main power switch is switched off. The relationship between the v_1 and the v_{cs} is described by:

$$V_1 = 3.3 \cdot V_{CS} + 0.7 \quad [7]$$

To avoid mistriggering caused by the voltage spike across the shunt resistor after switch-on of the main power switch, a 330ns leading edge blanking time (t_{LEB}) is applied to the output of the comparator.

4.4 Active Burst Mode Operation

At very low load condition, the IC enters active burst mode operation to minimize the input power. Details about active burst mode operation are explained in the following paragraphs.

4.4.1 Entering Active Burst Mode Operation

For determination of entering active burst mode operation, three conditions apply:

- The regulation voltage is lower than the threshold of V_{EB}(1.25V). Accordingly, the peak voltage across the shunt resistor is 0.17V;
- The up/down counter has its maximal value of 7;
- The two above conditions have to been fulfilled for a certain duration (24ms)

Once all of these conditions are fulfilled, the active burst mode flip-flop is set and the controller enters burst mode operation and the gate will be turned off until V_{REG} increase to on threshold V_{BH}. This multi-conditional determination for entering active burst mode operation prevents mistriggering of entering active burst mode operation, so that the controller enters active burst mode operation only when the output power is really low during the preset blanking time.

4.4.2 During Burst Mode Operation

After entering the Active Burst Mode the regulation voltage rises as V_{OUT} starts to decrease due to the inactive PWM section. One comparator observes the regulation signal if the voltage level V_{BH} (3.6V) is exceeded. In that case the internal circuit is again activated by the internal bias to start with swtiching.
Turn-on of the power MOSFET is triggered by the timer. The PWM generator for burst mode operation composes of a timer with a fixed frequency of 52 kHz, typically, and an analog comparator. Turn-off is resulted by comparison of the voltage signal v_1 with an internal threshold, by which the voltage across the shunt resistor V_{csB} is 0.34V, accordingly. A turn-off can also be triggered by the maximal duty ratio controller which sets the maximal duty ratio to 50%. In operation, the output flip-flop will be reset by one of these signals which come first.
If the output load is still low, the regulation signal decreases as the PWM section is operating. When regulation signal reaches the low threshold V_{BL}(3.0V), the internal bias is reset again and the PWM section is disabled until next time regultaion signal increases beyond the V_{BH} threshold. If working in active burst mode the regulation signal is changing like a saw tooth between 3.0V and 3.6V shown in Figure 7.

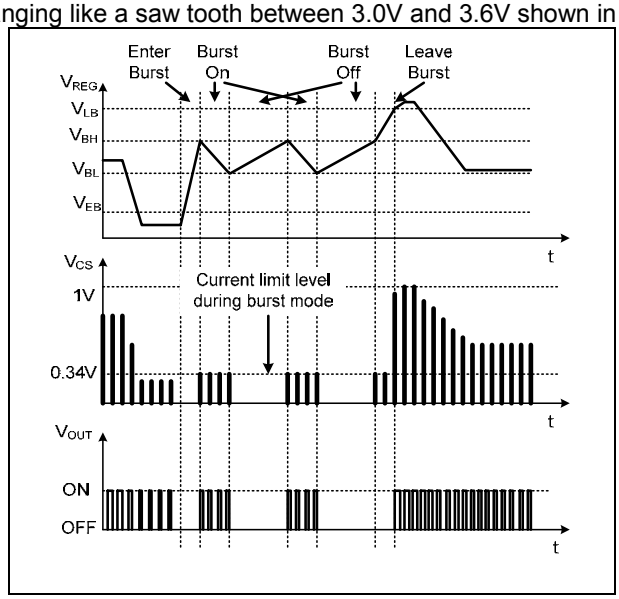


Figure 7 Signals in active burst mode

4.4.3 Leaving Active Burst Mode

The regulation voltage immediately increases if there is a high load jump. This is observed by one comparator. As the current limit is 25% during active burst mode a certain load is needed so that regulation voltage can exceed VLB (4.5V). After leaving active burst mode, maximum current can now be provided to stabilize VO. In addition, the up/down counter will be set to 1 immediately after leaving active burst mode. This is helpful to decrease the output voltage undershoot.

4.5 Current sense

The PWM comparator inside the IC has two inputs: one from current sense pin and the other from feedback voltage. Before being sent to the PWM comparator, there is an offset and operational gain on current sense voltage. In normal operation, the relationship between feedback voltage and maximum current sense votlage is determined by equation (8).

$$v_{FB} = G_{PWM} v_{CS_pk} + V_{PWM} \quad (8)$$

The absolute maximum current sense voltage is 1V. Therefore, the current sense resistor can be chosen according to the maximum required peak current in the transformer as shown in (9).

$$R_{CS} = 1 / I_{pk_p} \quad (9)$$

The design procedure of quasi-resonant flyback transformer is shown in [2]. In addition, a leading edge blanking (LEB) is already built inside the current sense pin. The typical value of leading edge blanking time is 330ns, which can be thought as a minimum on time. In most cases, the normal RC filter to blocking the spike because of MOSFET turn-on is not needed. However, in some applications, adding this RC filter is helpful to improve the converter performance.

4.6 Feedback

Inside the IC, the feedback (FB) pin is connected to the 5V voltage source through a pull-up resistor R_{FB}. Outside the IC, this pin is connected to the collector of opto-coupler. Normally, a ceramic capacitor C_{FB}, 1nF for example, can be put between this pin and ground for smooting the signal.

Feedback voltage will be used for a few functions as following:

- It determines the maximum current voltage, equivalent to the transformer peak current.
- It determines the ZC counter value according to load condition

4.7 Zero crossing

The circuit components connected to zero crossing (ZC) pin include resistors R_{ZC1} and R_{ZC2} and capacitor C_{ZC}. The values of three components shall be chosen so that the three functions combined to this pin will perform as designed.

At first, the ratio between R_{ZC1} and R_{ZC2} is chosen first to set the trigger level of output overvoltage protection. Assuming the protection level of output voltage is V_{O_OVP}, the turns of auxiliary winding is Na and the turns of secondary output winding is Ns, the ratio is calculated as

$$\frac{R_{ZC2}}{R_{ZC1} + R_{ZC2}} < V_{ZCOVP} \frac{N_S}{V_O N_a} \quad (10)$$

In (5), V_{ZCOVP} is the trigger level of output overvoltage protection which can be found in product datasheet.

Secondly, as shown in Figure 3, there are two delay times for detection of the zero crossing and turn on of the MOSFET. The delay time t_{Delay1} is the delay from the drain-source voltage cross the bus voltage to the ZC voltage follows below 100mV. This delay time can be adjusted through changing C_{ZC}. The second one, t_{Delay2}, is the delay time from ZC voltage follows below 100mV to the MOSFET is turned on. This second delay time is determined by IC internal circuit and cannot be changed. Therefore, the capacitance C_{ZC} is chosen to adjust the delay time t_{Delay1} MOSFET is justed turned on at the valley point of drain-source voltage. This is normally done through experiment.

Next, there is a foldback point correction integrated in this pin. This function is to decrease the peak current limit on current sense pin so that the maximum output power of the converter will not increase when the input

voltage increases. This is done through sensing the current flowing out from ZC pin when MOSFET is turned on.

When the main power switch is turned on, the negative voltage on auxiliary winding can be calculated as

$$V_{aux} = -V_{BUS}\frac{N_a}{N_P} \quad (11)$$

Inside ZC pin, there is a clamping circuit so that the ZC pin voltage is kept at nearly zero. Therefore, the current flowing out from ZC pin at this moment is

$$I_{ZC_ON} = \frac{V_{BUS}N_a}{R_{ZC1}N_P} \quad (12)$$

The threshold in ZC pin to start the foldback point correction is I_{ZC} = 0.5 mA. Therefore, R_{ZC1} can be chosen so that

$$R_{ZC1} = \frac{V_{BUS_S}N_a}{0.5mA * N_P} \quad (13)$$

In (13), V_{BUS_S} is the voltage from which the maximum output power is desired to be maintained at constant level. The corresponding maximum current sense voltage in relation to the ZC current is shown in Figure 8.

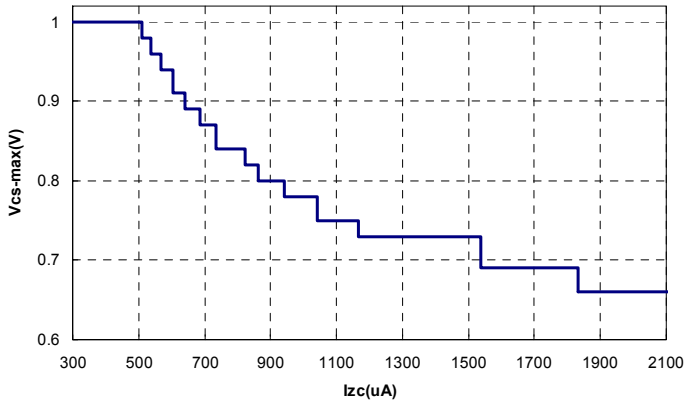


Figure 8 Maximum current sense limit versus ZC current during MOSFET on-state

In addition, as shown in Figure 3, an overshoot is possible on ZC voltages when MOSFET is turned off. This is because of the oscillation 1 on drain voltage, shown in Figure 3 may be coupled to the auxiliary winding. Therefore, the capacitance C_{ZC} and ratio can be adjusted to obtain the trade off between the output overvoltage protection accuracy and the valley switching performace.
Furthermore, to avoid mis-triggerring of ZC detection just after MOSFET is turned off, a ring suppression time is provided. The ring suppression time is 2.5 µs typically if V_{ZC} is higher than 0.7V and it is 25 µs typically if V_{ZC} is lower than 0.7V. During the ring suppression time, IC can not be turned on again. Therefore, the ring suppression time can also be thought as a minimum off time.

4.8 Gate drive

Inside Gate pin, a totem-drive circuit is integrated. The gate drive voltage is 10V, which is enough for most of the available MOSFET. In case of a 1nF load capacitance, the typically values of rise time and fall time are 117ns and 27ns, respectively. In practice, a gate resistor can be used to adjust the turn-on speed of the MOSFET. In addition, to accelerate the turn off speed, the gate resistor can be anti-paralleled with an ultra-fast diode like 1N4148. To avoid the oscillation during turn-off of the MOSFET, it is suggested that the loop area of the driver, through gate resistor and MOSFET gate, source and back to IC ground should be as small as possible.

4.9 Others

For quasi-resonant flyback converters, it is possible that the operation frequency goes too low, which normally resulted in audible noise. To prevent it, in ICE2QS03G, a maximum on time and maximum switching period is provided.

The maximum on time in ICE2QS03G is 30 µs typically. If the gate is maintained on for 30 µs, IC will turn off the gate regardless of the current sense voltage.
When the MOSFET is off and IC can not detect enough number of ZC to turn on the MOSFET, IC will turn on the MOSFET when the maximum switching period, 50 µs typically, is reached. Please note that even a non-zero ZC pin voltage can not prevent IC from turning on the MOSFET. Therefore, during soft start, a CCM operation of the converter can be expected.

5 Typical application circuit

An 36W evaluation board with ICE2QS03G is also available. The detailed information can be found in [3]. The application circuit is shown in Figure 9.

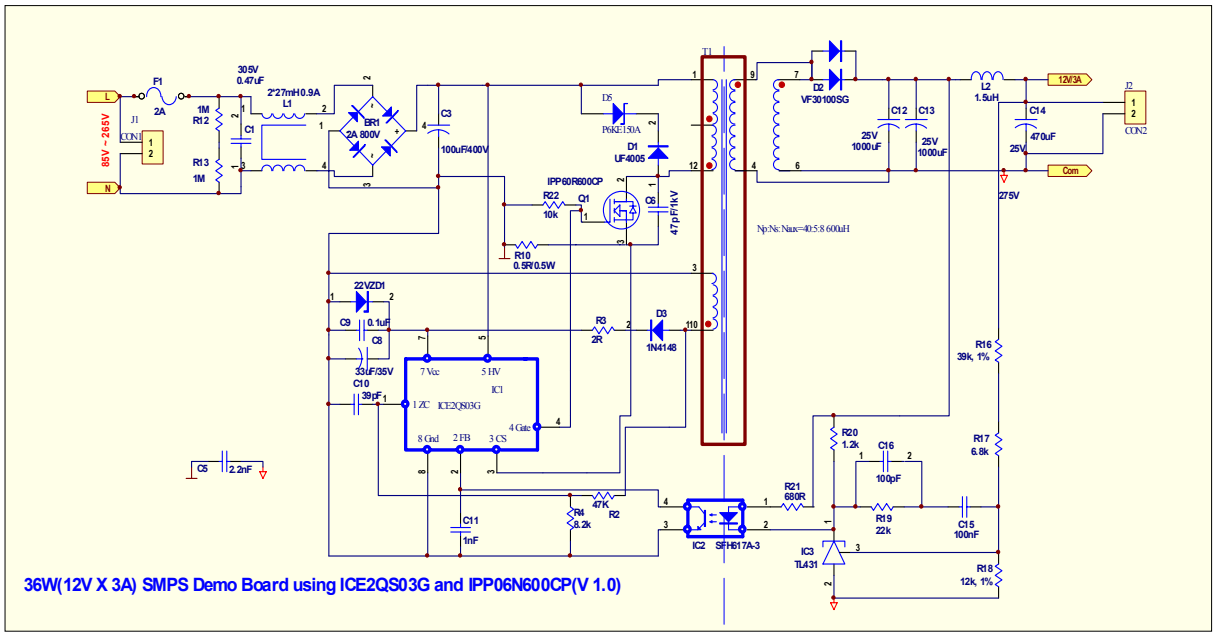


Figure 9 Schematic of the 36W evalulation board with ICE2QS03G

6 References

[1] ICE2QS03G, product datasheet, Infineon Technologies, 2009

[2] Converter design using the quasi-resonant PWM controller ICE2QS01, application notes, Infineon Technologies, 2006

[3] 36W Evaluation Board with Quasi-Resonant PWM Controller ICE2QS03G, AN-EVALQRS-ICE2QS03G, Infineon Technologies, 2009