Infineon power for FPGA of Xilinx/Zynq® Ultrascale+™ MPSoC for Embedded Vision applications

Zu07, Zu05 and Zu04 EV series and others

About this document

Scope and purpose

Infineon has several power solutions for the Zynq® UltraScale+ MPSoC family for Embedded Vision applications. This application note shows brief highlights and high level examples of actual reference designs with both Xilinx direct on the ZCU104 evaluation platform and also on Avnet's UltraZED-EV evaluation platform both featuring the Zu07EV. This application note will also show available Infineon power macros developed with Xilinx featuring scalable power designs for the Zu04EV, Zu05EV and Zu07EV targeting space constrained applications. Three distinct design examples from Infineon will be presented.

Intended audience

Designers interested in high level Infineon power maps for Zu04EV, Zu05EV to Zu07EV Zynq UltraScale MPSoC requiring separate voltages for the VCCINT (Vcore block) and the VCCINT_VCU (Video codec block), EV series family from Xilinx. Designers challenged with tight board space designs for small form factor applications.

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1 Avnet's - Zynq UltraScale+ MPSoC, UltraZED-EV Embedded Vision Platform

Figure 1 depicts the Infineon power solution for the Avnet UltraZED-EV platform consisting of Xilinx Zynq US+ MPSoC, Zu07EV, with integrated video codec. This kit is orderable from Avnet and features a modular MPSoC/FPGA SOM card and carrier board format with various I/O to develop a wide variety of Embedded Vision applications with sensor fusion capability. Infineon's power solutions focus on space constrained applications on both the SOM card and the carrier board.

Avnet offers the UltraZED-EV kit with complete designs using Infineon's power solutions:

- Schematics, BOM, layout and performance data is available from both Avnet and Infineon
  - www.infineon.com/xilinx
- Infineon's PowIRCenter GUI software for power design and evaluation
- Avnet's UltraZED-EV, Zynq UltraScale+ Zu07EV
  - Evaluation kit overview (Avnet)
  - www.zedboard.org/product/ultrazed-eg-starter-kit

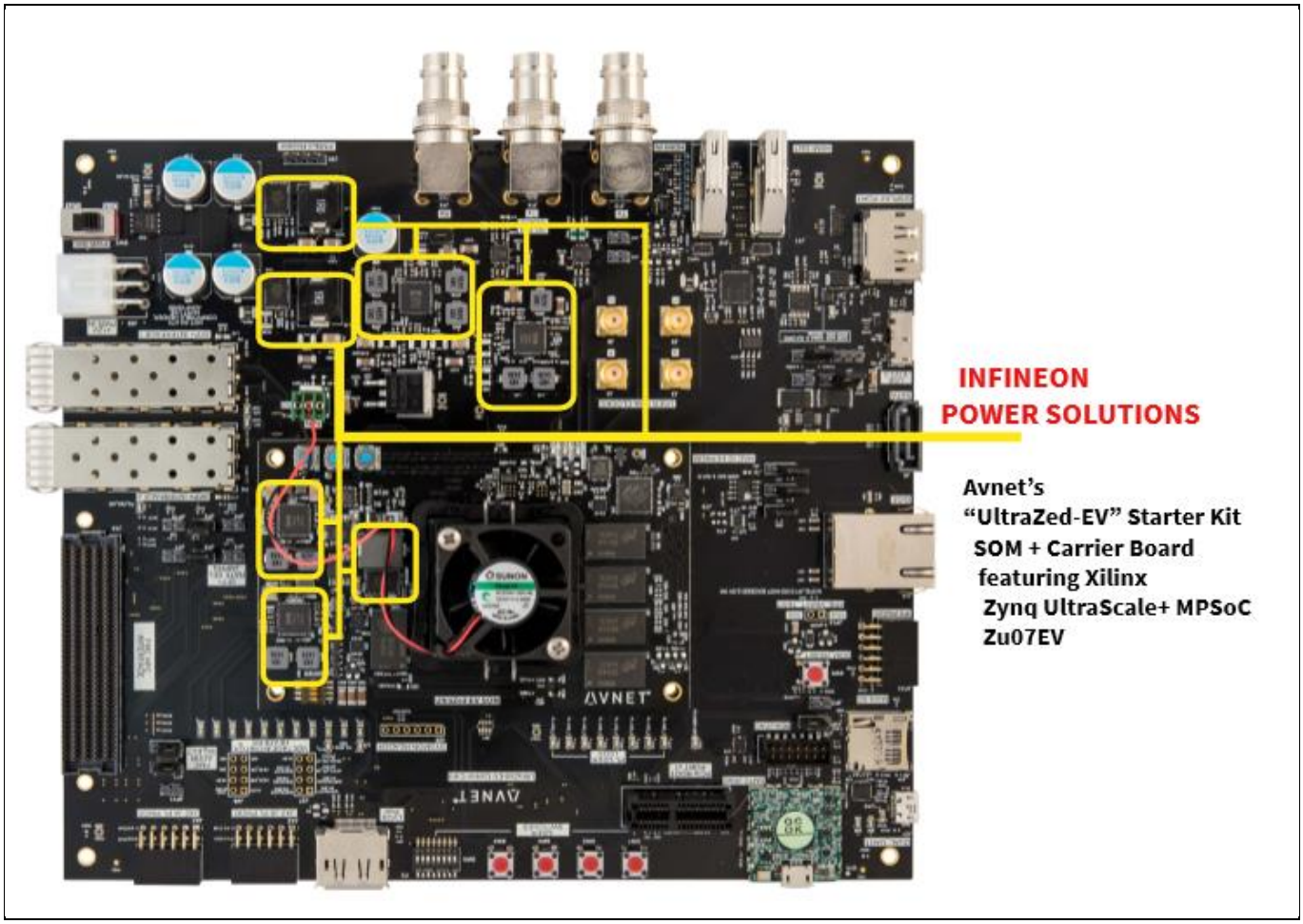


Figure 1 Infineon power solution for Avnet's UltraZED-EV, Zu07EV

Infineon's power solution for Zynq UltraScale+ MPSoC and Avnet's UltraZED-EV is shown in Figure 2 below. Seen in Figure 2 is the recommend consolidation of the power rails for the MPSoC from Xilinx on the left; while on the right is the actual implementation from Infineon. The power implementation focuses on tight board space design.

Highlights of Infineon's space optimized solution (Figure 2):

- Power solution optimized with minimum number of voltage rails to Xilinx power optimization recommendations
    - See also Section 3 for more Infineon compact power solutions for the EV-series.
- Power solution offers scalable power for Zu07EV, Zu05EV and Zu04EV using an IR38064 and IRPS5401 PMIC by spreading the Vcore rails of the PS and PL blocks of the MPSoC and Video codec VCCINT_VCU from -40°C to +125°C for best thermal operation
- Power solution offers low noise voltage rails for SERDES for compact space implementation using the PMIC(s)
- Power solution offers integrated sequencing between the IR38063 and IRPS5401 PMICs using internal timing delays adjustable via I2C/PMBus for setting from 0 ms to 127 ms
- Power solution was crafted using Infineon's PowIRCenter GUI tool for design and for monitoring purposes

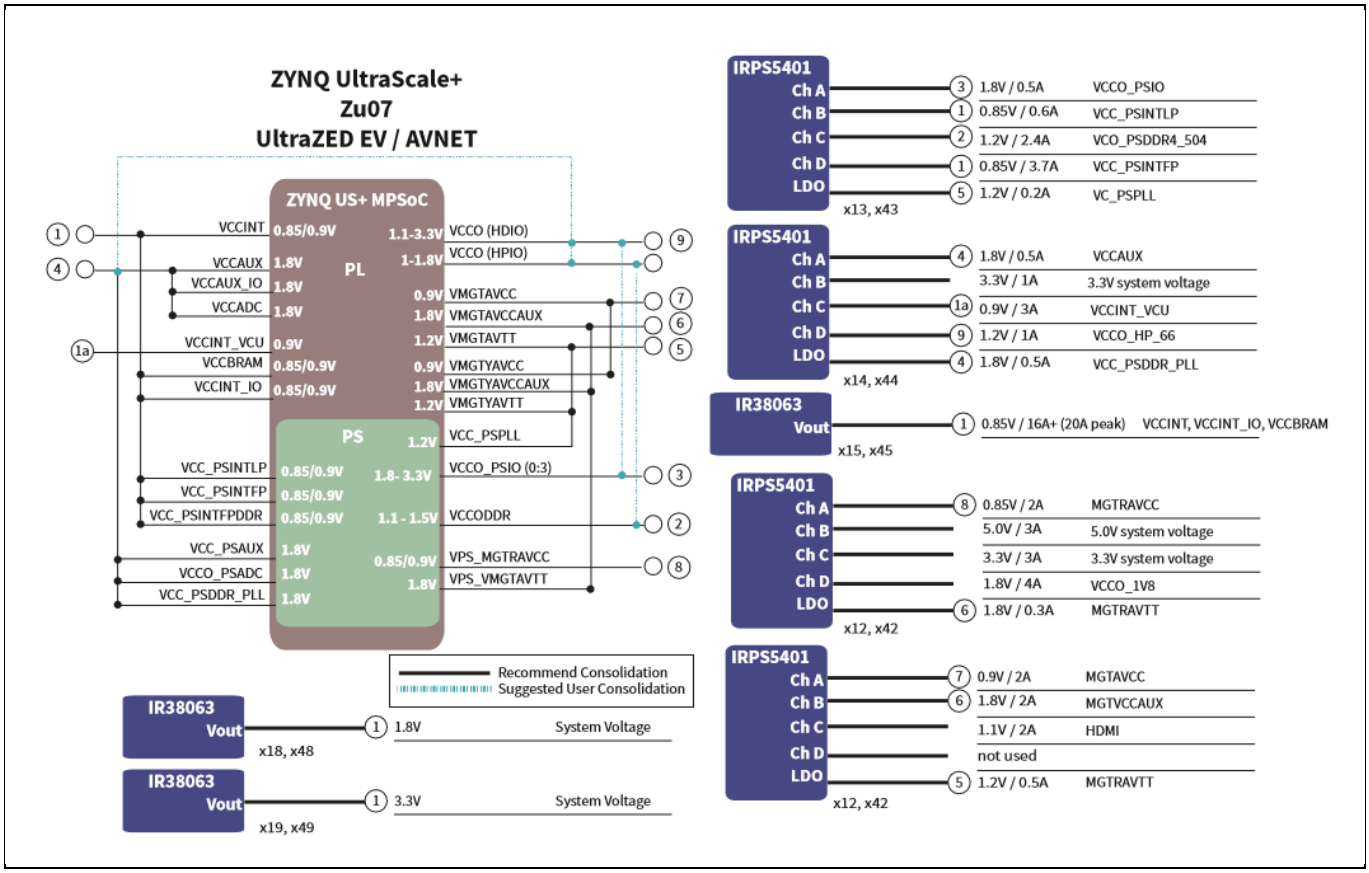


Figure 2 Infineon power map solution for UltraZED-EV, Zu07EV

2 Xilinx' - Zynq UltraScale+ MPSoC, ZCU104 Embedded Vision Platform

Figure 3 depicts the Infineon power solution for the Xilinx ZCU104 platform consisting of Xilinx Zynq US+ MPSoC, Zu07EV with integrated video codec. This kit is orderable from Xilinx and/or Avnet. This kit features a Zynq UltraScale+ MPSoC EV device with video codec and supports many common peripherals and interfaces for embedded vision use cases including in the development of a wide variety of Embedded Vision applications with sensor fusion capability. Infineon power focuses on space constrained solution using the IRPS5401 PMIC and several other Infineon devices.

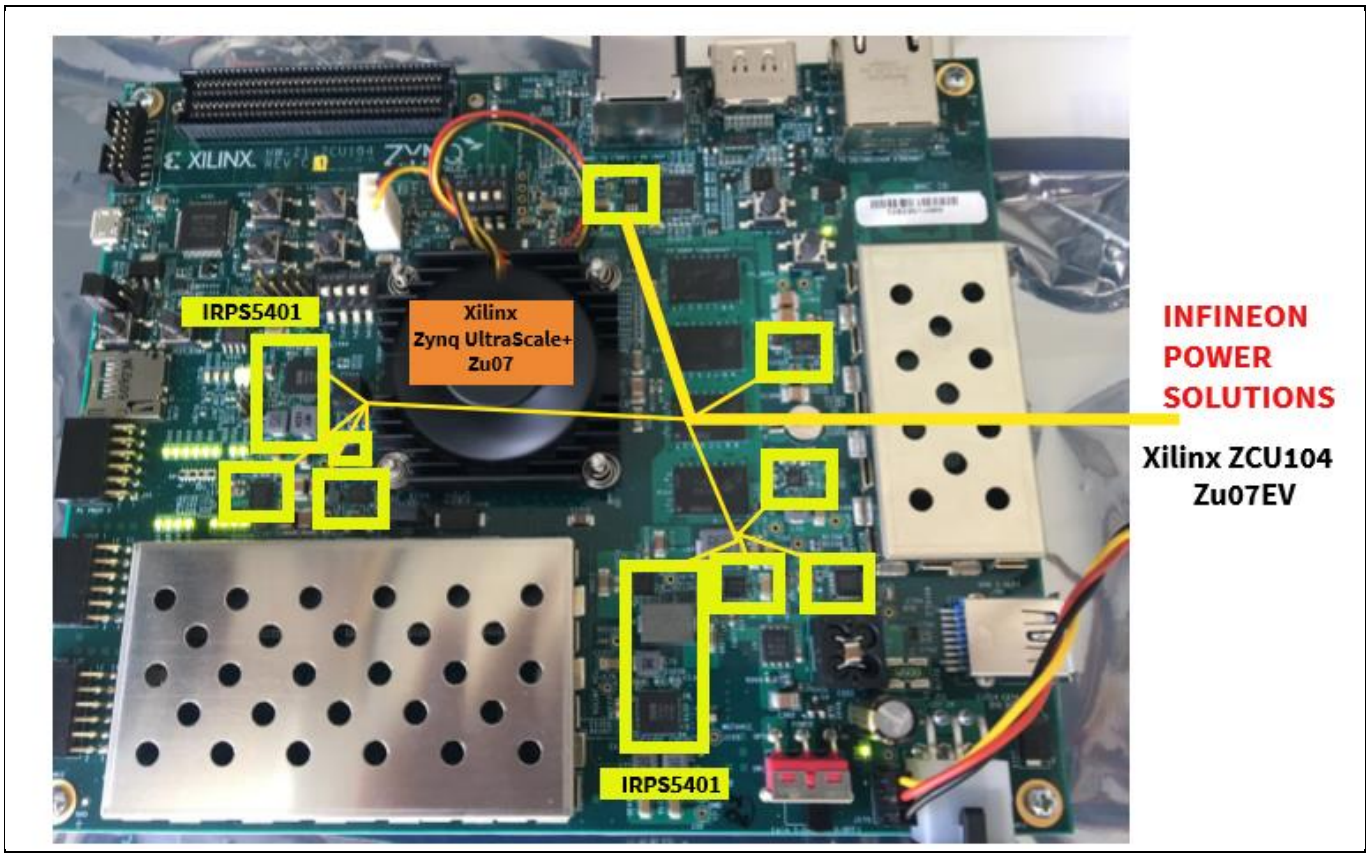


Figure 3 Infineon power solution for Xilinx ZCU104, Zu07EV

Xilinx offers the ZCU104 kit with complete designs using Infineon's power solutions:

- Schematics, BOM, layout and performance data available from both Xilinx and Infineon
  - www.infineon.com/xilinx
- Infineon PowIRCenter GUI Software for power design and evaluation
- ZCU104 Zynq UltraScale+ MPSOC Zu07EV evaluation kit overview (Xilinx)
  - www.xilinx.com/products/boards-and-kits/zcu104.html
- ZCU104 hardware schematics and boards files (Xilinx)
  - www.xilinx.com/products/boards-and-kits/zcu104html#documentation

Infineon's power solutions for Zynq UltraScale+ MPSoC in Xilinx ZCU104 is shown in Figure 4 below. Seen in Figure 4 is the recommend consolidation of the power rails for the MPSoC from Xilinx on the left; while on the right is the actual implementation from Infineon. The power implementation focuses on tight board space design.

Highlights of Infineon's space optimized solution (Figure 4):

- Power solution optimized with minimum number of voltage rails to Xilinx power optimization recommendations
    - See also Section 3 for more Infineon compact power solutions for the EV-series
- Power solution offers scalable power for Zu07EV, Zu05EV and Zu04EV using a combination of two IRPS5401 PMIC + TDA21240 Power stage devices consolidating the Vcore rails from the PL and PS block of the MPSoC. This approach allows for power scalability of the Zu07, Zu05 and/or Zu04. The Video codec VCCINT_VCU is powered independently using a IR3897. These solutions operate in applications from -40°C to +125°C for best thermal operation.
- Power solution offers low noise voltage rails for SERDES for compact space implementation using the PMIC, analog regulators and LDO.
- Power solution offers integrated sequencing between the IRPS5401 PMICs by using internal timing delays adjustable via I2C/PMBus for setting from 0 ms to 127 ms
- Power solution was crafted using Infineon's PowIRCenter GUI tool for design and for monitoring purposes

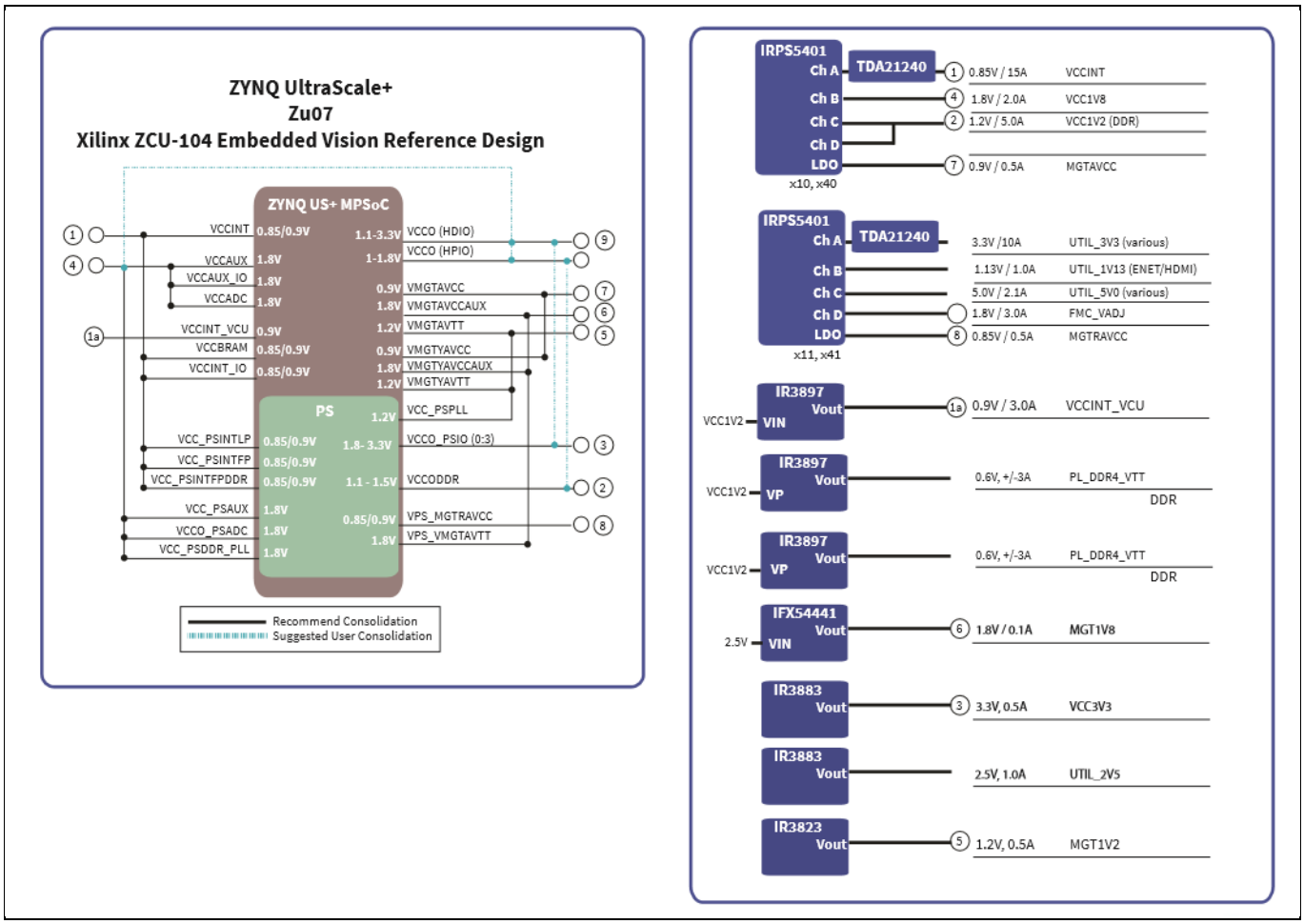
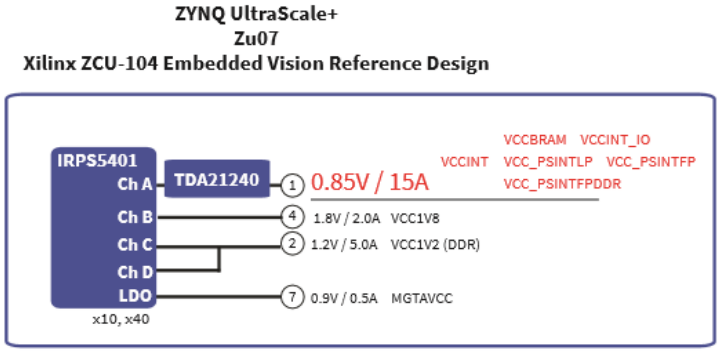


Figure 4 Infineon power map solution for Xilinx ZCU104, Zu07EV

2.1 Performance data - example

Infineon's is a PROVEN power solution provider for the Zynq UltraScale+ MPSoC for Xilinx ZCU104, Zu07EV.

Below is an excerpt from Xilinx' and Infineon's comprehensive PERFORMANCE VALIDATION REPORT for the power rails of the ZCU104 reference design. Note that all the rails were validated on this design; including the integrated power sequencing scheme.



Measurement	Result	Pass/Fail	Test Condition
Vout	0.849V (0.852V) 0.840V (0.848V)	Pass	0A 15A
DC Ripple	11.2mV 10.8mV	Pass	0A 15A
Isense	0.25A 5.13A 10A 14.25A	Pass	0A 5A 10A 14.5A
Vac(droop)	4.4mV	Pass	10.75A to 14.5A
Vac(overshoot)	5.0mV	Pass	14.55A to 10.75A

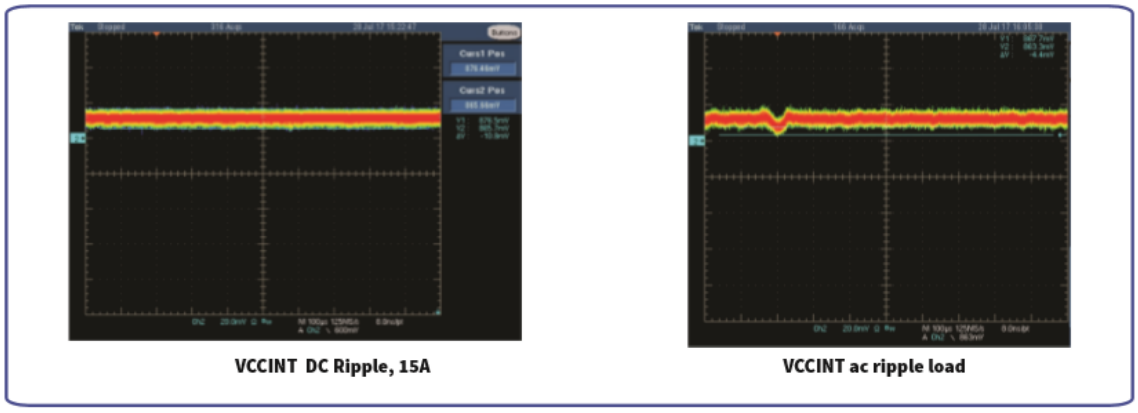


Figure 5 Infineon power map solution for Xilinx ZCU104, Zu07EV

Example Vcore rails of the Zu07EV

- Device: IRPS5401 + TDA21240
- V_{out} measurement location, C1216
- Load test location, J25/C696/C697
- SW node measurement location, L82

Conditions:

- VCCINT group rails: IRPS5401 channel A
- V_{in}, 12 V
- V_{out}, 0.85 V
- $I_{out(pk)}$, 15 A
- I_{step}, 3.75 A
- I_{ramp}, 1 A/µs

3 Infineon's Power Macros for EV series of the Zynq UltraScale+ MPSoC

Figure 6 depicts the space optimized Infineon power macros solutions for the Xilinx Zynq US+ MPSoC, EV series with integrated video codec. These designs were designed in collaboration with Xilinx and are available from Infineon. The combination of these 4 power macros allows for scalable power design on the Vcore voltages from 5 A to 40 A using the combination of the PMIC (IRPS5401) and external power stages (TDA21242 [25 A] and TDA21240 [40 A]). Options for SERDES and non-SERDES are available. All of the solutions below include integrated sequencing.

- Power solution for Zu07EV without SERDES: Use configurations 8 and 9
- Power solution for Zu07EV with SERDES: Use configurations 8 and 10
- Power solution for Zu05EV and/or Zu04EV without SERDES: Use configurations 7 and 9
- Power solution for Zu05EV and/or Zu04EV with SERDES: Use configurations 7 and 10



Figure 6 Infineon power macros for Xilinx EV series, Zu07EV, Zu05EV, Zu04EV

Figure 7 depicts the Infineon power maps of the space optimized power macros for the Xilinx Zynq US+ MPSoC, EV series with integrated video codec. These were designs in collaboration with Xilinx and are available from Infineon. The combination of these 4 power macros allows for scalable power design on the Vcore voltages from 5 A to 40 A using the combination of the IRPS5401 PMIC and external power stages, TDA21242 (25 A) and TDA21240 (40 A). Options for SERDES and non-SERDES is available. All of the solutions below include integrated sequencing.

- Power solution for Zu07EV without SERDES: Use configurations 8 and 9
- Power solution for Zu07EV with SERDES: Use configurations 8 and 10
- Power solution for Zu05EV and/or Zu04EV without SERDES: Use configurations 7 and 9
- Power solution for Zu05EV and/or Zu04EV with SERDES: Use configurations 7 and 10

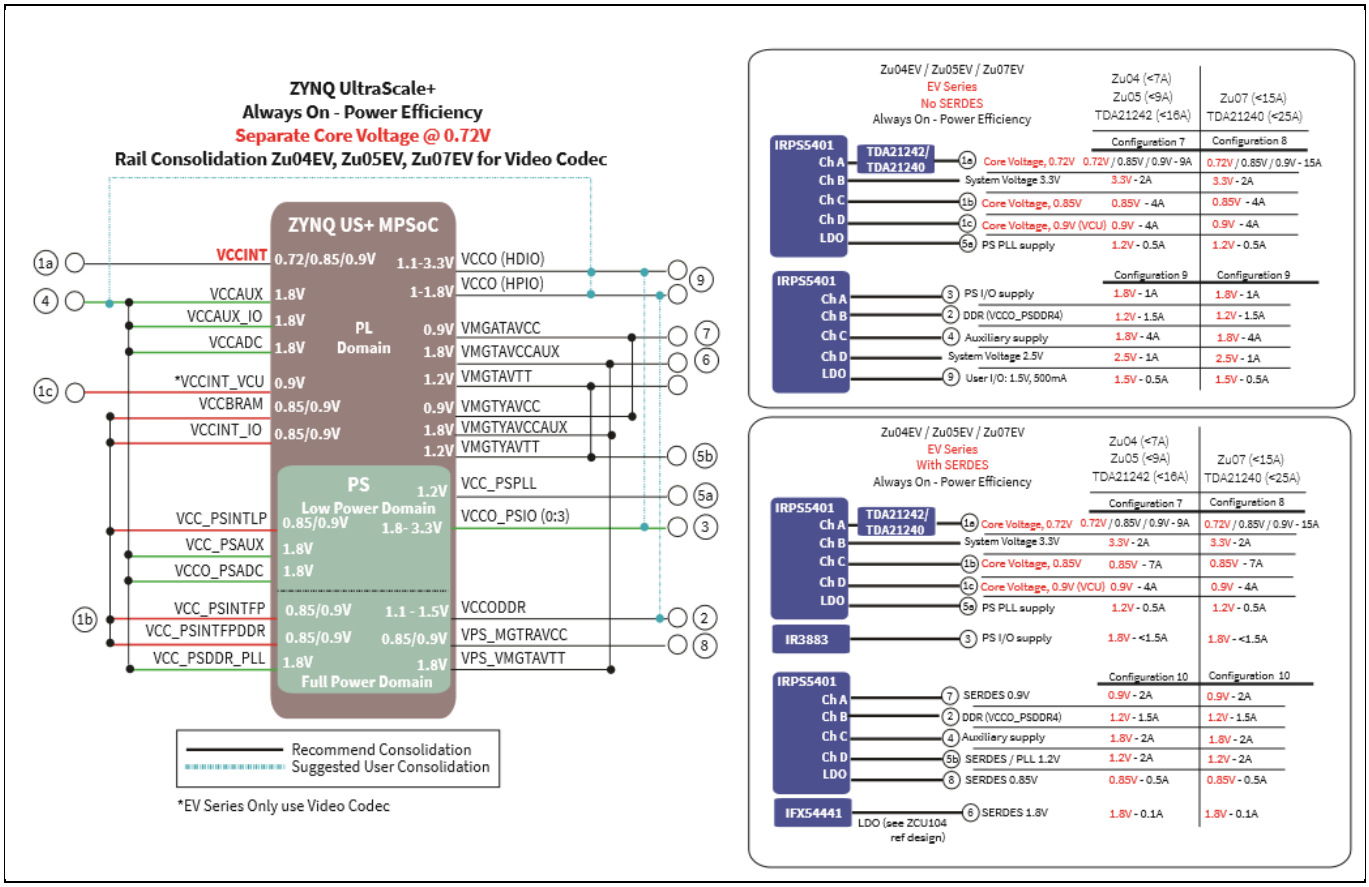


Figure 7 Infineon power map solution for EV series of the Zynq UltraScale+ MPSoC

Infineon offers the Zynq UltraScale+ MPSoC power macros with complete designs solutions. These are optimized designs specifically for the MPSoC:

- Schematics, BOM, layout and performance data is available from Infineon. Currently available in ORCAD/Cadence and Altium. Mentor pending.
    - www.infineon.com/xilinx
- Infineon PowIRCenter GUI software for power design and evaluation

Figure 8 provides an example power schematic for the main rail for the Zu07EV MPSoC with emphasis on the power scalability of the Vcore for the Zu04EV, Zu05EV and Zu07EV; integrated voltage sequencing; minimum BOM count and high integration for tight board space applications. This design features the IRPS5401 5-output

PMIC and the TDA21240 40 A power stage. Note: IRPS5401 with 3 V power stages will require a clamp circuit for operation.

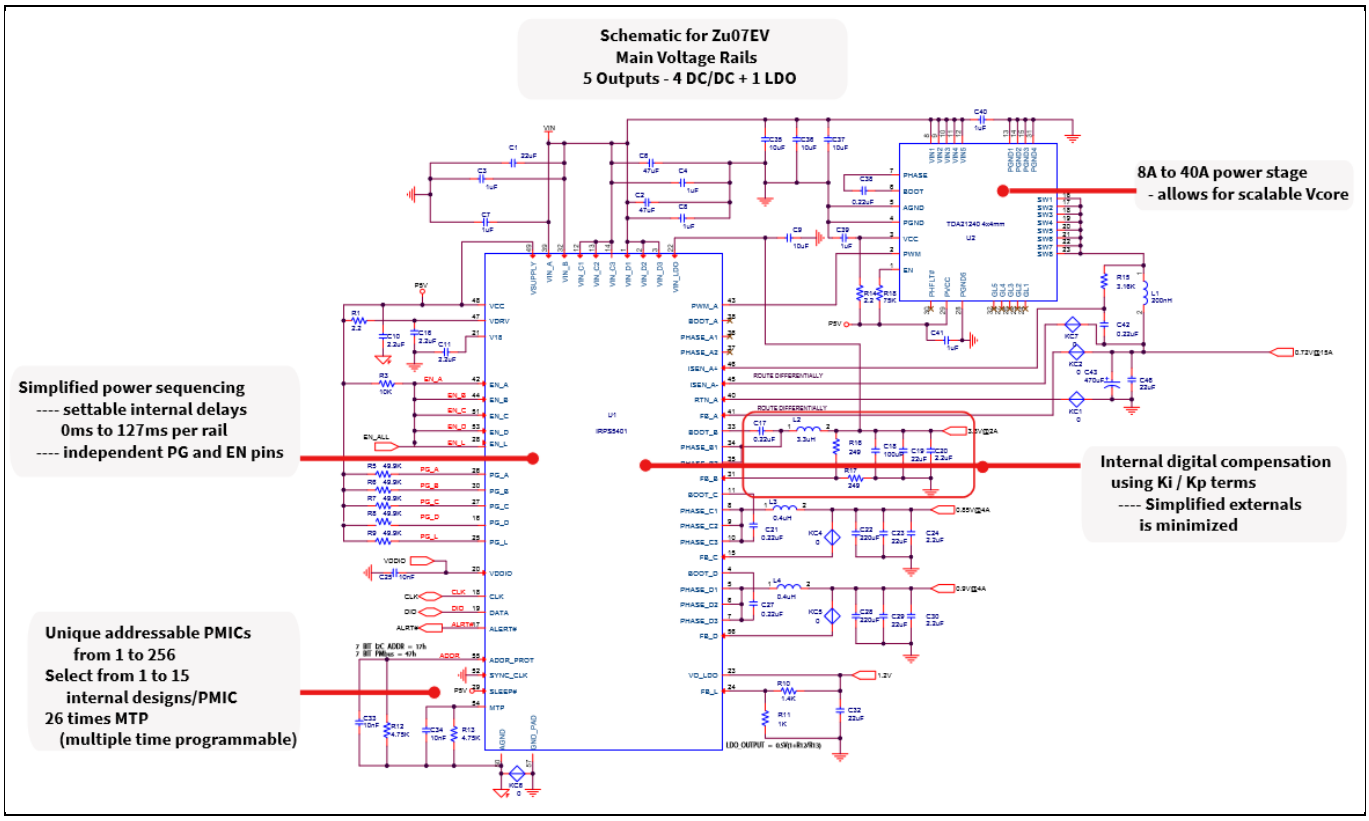


Figure 8 Infineon power schematic example for Zu07EV's main rails – Zynq US+ power macro EV113-008 (configuration 8)

Figure 9 provides a power layout example for the main rail of the Zu07EV MPSoC with emphasis on the scalable power for the Vcore of the Zu04EV, Zu05EV and Zu07EV; integrated voltage sequencing; minimum BOM count and high integration for tight board space applications. Infineon offers various layout configurations that are fitting for practical embedded vision applications for common form-factors such as:

1) PCI-express for narrow rectangle PCB footprint (see figure 9a); or for
2) SOM (System on Module) or CCD/Camera Modules for thinner "L-shaped" PCB footprints (see figure 9b), where the voltage rails "wrap around" the MPSoC.

Each of these designs feature the IRPS5401 5-output PMIC and the TDA21240 40 A power stage offering scalable Vcore voltages for any of the EV series: Zu04EV, Zu05EV and Zu07EV with the same layout design. Additionally, a separate output is also provided for the VCCINT_VCU rail at 0.9 V for the video codec. This compact design contains an internal voltage sequencer as well as options for I2C/PMBus fault and telemetry management and reporting functions.

The layout "snippets" are available today in ORCAD/Cadence and Altium for "drop and place" design; and soon Infineon will offer Mentor tool set layout formats. Note that these are turnkey practical designs. Additional layout flexibility is also possible to displace the Vcore (channel A) inductor and power stage (TDA21240) closely

to the POL (point of load) since the IRPS5401 has a differential amplifier feedback loop. Hence allowing for more creative PCB placement for odd shaped layout techniques in space constraint designs.

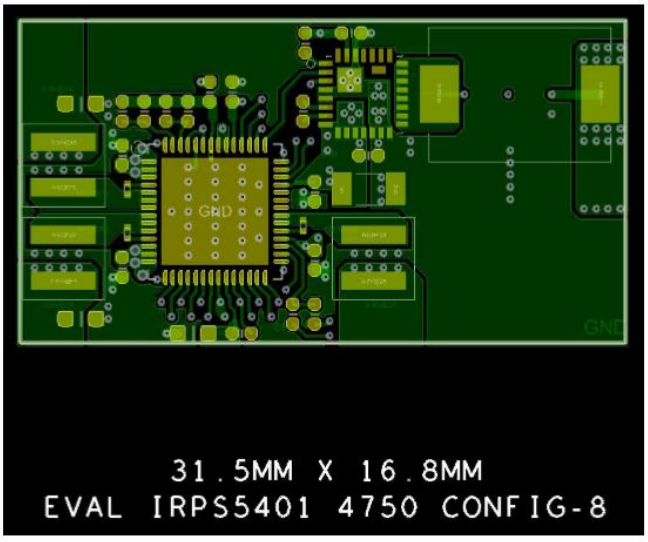


Figure 9(a): Rectangular Layout Example for PCI-express form-factor

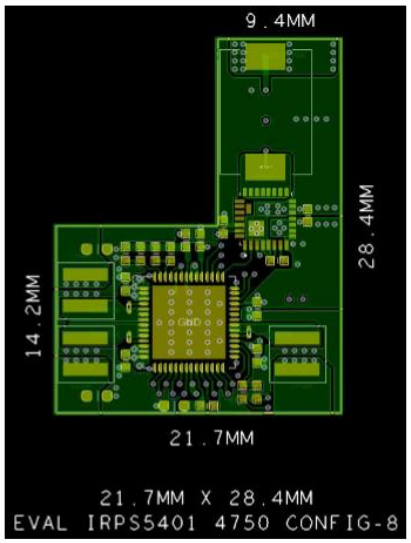


Figure 9(b): "L-shaped" Layout Example for System on Module (SOM) or Camera/CCD modules so the power can "wrap" around the MPSoC

Figure 9 Infineon power layout for Zu07EV's main rail – Zynq US+ power macro EV113-008 (configuration 8)

3.1 Performance data example

Infineon is a PROVEN power solution provider for the Zynq UltraScale+ MPSoC for Xilinx, EV series. Below is data for the power solution of the Zu07EV.

Below is an excerpt from Infineon's comprehensive PERFORMANCE VALIDATION for the Xilinx Zynq Power Macros. Figure 10(a) shows the DC accuracy for the VCCINT voltage rail at 0.72 V and ~12 A active load to be less than 1% DC accuracy; while Figure 10(b) shows the VCCINT rail at setup load response from 11 A to 15 A to be well below 3% AC accuracy specifications.

Again, this design is scalable for VCCINT core voltage design from 10 A to 40 A; hence covering the range of performance for the EV series.

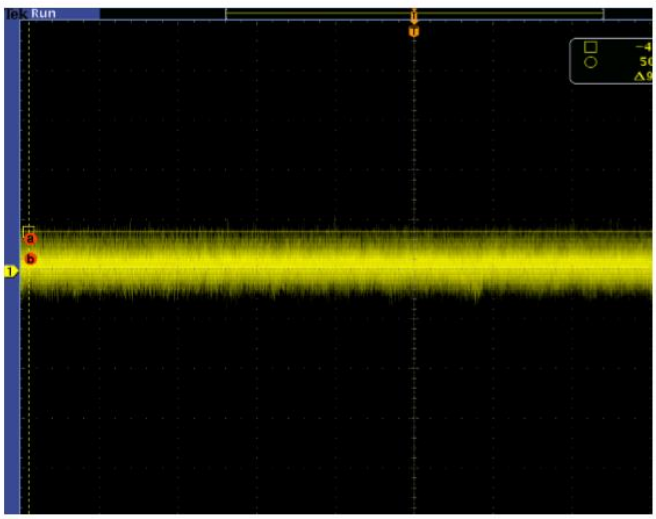


Figure 10(a): IRPS5401 + TDA21240 VCCINT < 1% DC at load

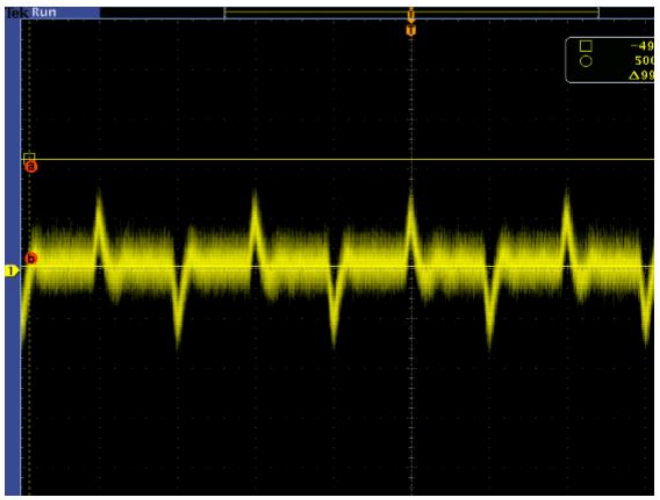


Figure 10(b): IRPS5401 + TDA21240 VCCINT <3% AC accuracy at load

Figure 10 Infineon power performance data example for the VCCINT rail of the Zu07EV EV113-008 (configuration 8)

Revision history

Document version	Date of release	Description of changes

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