# How load-line will help the application

## Advantages of implementing Load-Line in a multi-phase buck converter design for applications requiring currents of 200 A to 1000 A with high dynamic content

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## About this document

### Scope and purpose

With the increasing need for more processing capabilities, FPGAs and ASICs are observing more complex power delivery requirements. The general trend is toward increasing load current with lower core voltages. Advanced power Load-Line (LL) design techniques can be very helpful for 200 A to 1000 A CPUs, GPUs, FPGAs and ASICs in Artificial Intelligence (AI) servers and 5G datacom applications. Such applications require multi-phase buck converters, as high load currents that dynamically change in high di/dt load steps have a very stringent output voltage deviation spec. In this paper we examine the implementation of LL in such applications. We review the advantages that LL provides over a conventional voltage-mode buck converter without LL enabled.

### Intended audience

FPGA and ASIC system design engineers

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# 1 Introduction

The implementation of LL had its genesis in the Intel VRM applications. As processors change power states and vary clock speeds, implementing LL has numerous advantages. FPGAs and other ASICs are seeing such a need in the marketplace today. FPGA processing capabilities are used in various applications including Machine Learning, AI inference engines, video processing and Radar applications. In this paper, the term LL will be used interchangeably with Adaptive Voltage Positioning (AVP). AVP was the term coined by Intel, and is commonly used in the industry to refer to LL. In this paper, we will use a generic FPGA core power requirement to evaluate the implementation of LL:

- $V_{IN}$ = 12 V
- $V_{OUT}$ = 0.78 V
- Thermal Design Current (TDC) and $I_{out\,max}$ = 240 A
- Transient load step: $\Delta I_{out}$ = 10 A to 130 A with a rise time of 200 ns → di/dt = 600 A/µs
- $V_{OUT}$ DC ripple: $dV_{OUTripple} = \pm 0.5\% \cdot V_{OUT}$
- $V_{OUT}$ AC deviation: $dV_{OUT} = \pm 3\% \cdot V_{OUT} = \pm 23.4$ mV

  That requires $V_{OUT}$ to be between 756.6 mV and 803.4 mV at all times.

We selected a six-phase buck converter to maintain a good balance between phase current, power loss and transient support.

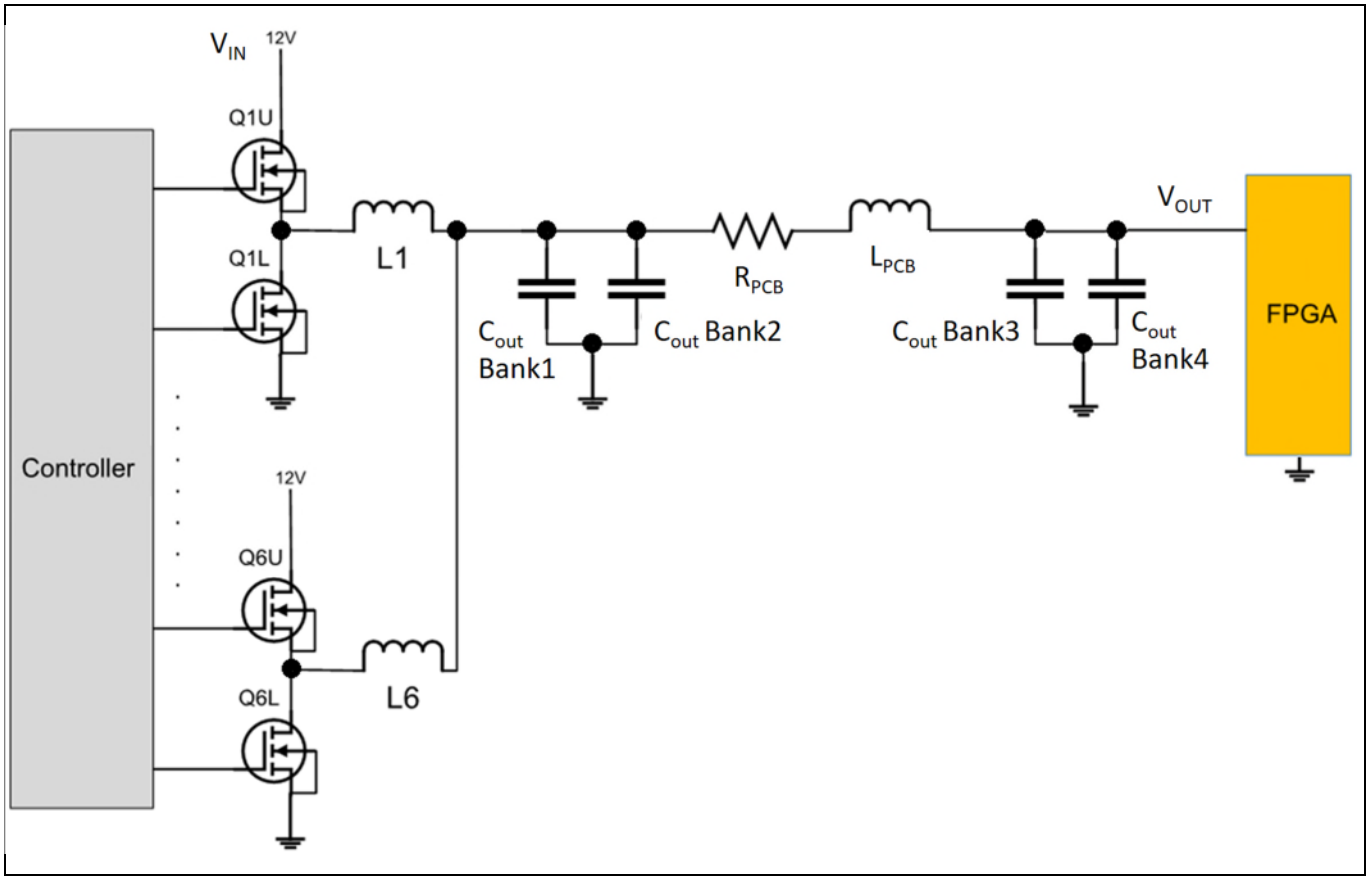



**Figure 1 Overview of the Power Delivery Network (PDN) of a six-phase buck converter**

Shown above is a PDN associated with a six-phase buck converter

. Q1U and Q1L represent the upper and lower MOSFETs of Phase 1; similarly, Q6U and Q6L represent Phase 6. L1 and L6 represent the output inductors of Phases 1 and 6. $C_{OUT}$ Banks 1 and 2 represent the output capacitors at the output of the Voltage Regulator (VR). $R_{pcb}$ and $L_{pcb}$ represent the parasitic resistance and inductance between the output of the VR and the FPGA load. In theory this value should be very small and indicative of a tight and well-planned PCB layout. $C_{OUT}$ Banks 3 and 4 represent the capacitors at the FPGA load. Between $R_{pcb}$, $L_{pcb}$, and $C_{OUT}$ Banks 3 and 4 a secondary low-pass filter is formed and needs to be considered in the PDN modeling.

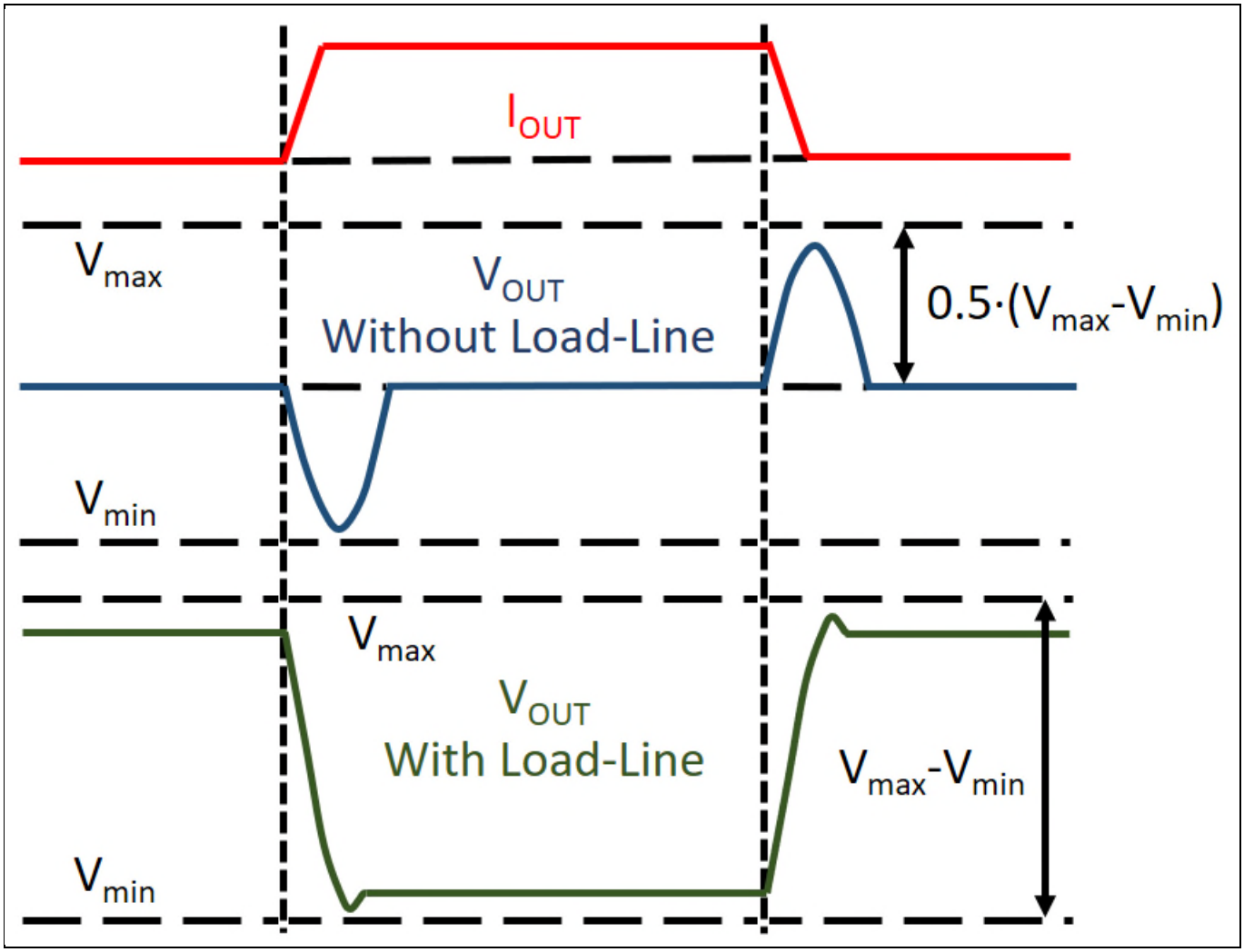



**Figure 2 $V_{OUT}$ behavior during a transient event with and without LL**

Figure 2 demonstrates the output voltage behavior during a transient load condition. A load step (top waveform) causes a disturbance of $V_{OUT}$. Without LL (middle waveform), $V_{OUT}$ has to return to the initial $V_{OUT}$ value (steady-state value) after the load step. This applies to both directions of current change. During a load increase the output voltage dips as charge is taken from the output capacitors. At load release the voltage overshoots because the stored energy in the inductors is being absorbed by the output capacitors.

A defined LL permits the output voltage to shift between its minimum and maximum (or a fraction thereof) based on the output current. This behavior is depicted in the lower waveform of Figure 2.

## Introduction

The advantages of using LL are manifold:

- Lower power dissipation at heavy load because of lower driving voltage
- Better transient response with fewer output capacitors because the voltage window for the excursion is bigger
- Simpler compensation as the prominent LC filter double pole disappears from the transfer function by adding a zero in the outer loop
- Promotes natural current sharing in a multi-phase design

# 2 Set-up

The goal of this investigation is to show that with LL enabled, the output capacitor banks can be significantly smaller in value compared to the case without LL in order to meet the $V_{OUT}$ deviation specification. This will be verified with SIMPLIS models and hardware demo board testing.

The hardware measurements will be done on the PXE1610C demo board.

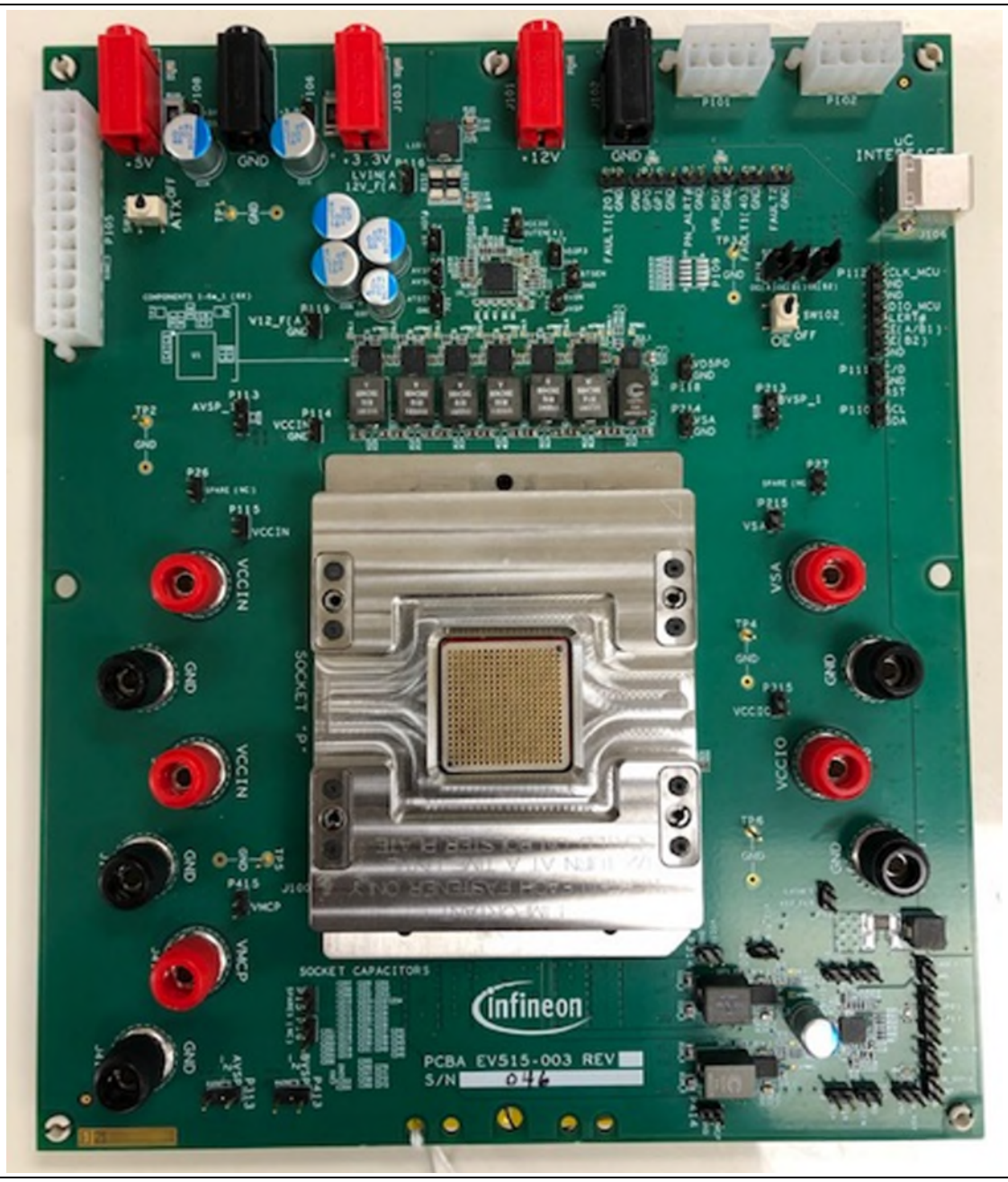



**Figure 3 Picture of the PXE1610C demo board used for hardware testing and verification**

On this demo board, connectors P105 and P101 are the ATX power supply connectors use to power the board with 12 V, 5 V and 3.3 V. An Intel socket P0 was used with the Intel VRTT tool to conduct the high di/dt transient load testing, shown below. The board has various test points for the differential voltage sense lines. The measured transient-load waveforms are taken directly from the outputs of the Intel VRTT Gen 4 test tool.

# 3 Investigation without LL

The test parameters and circuit values used are as follows:

- LL = 0
- $L_{OUT}$ = 100 nH inductor, DCR = 1 mΩ
- $C_{OUT}$ Bank 1 = 12 x 470 µF POSCAP
- $C_{OUT}$ Bank 2 = 12 x 47 µF ceramic caps
- $C_{OUT}$ Bank 3 = 60 x 22 µF ceramic caps (at FPGA load)
- $C_{OUT}$ Bank 4 = 70 x 47 µF ceramic caps (at FPGA load)
- $L_{pcb} \approx 50$ pH
  This represents the parasitic inductance between the output of the VR and the FPGA load. In this case, we are expecting a design with very good parasitic values.
- $R_{pcb} \approx 0.2$ mΩ
  This represents the parasitic copper resistance from the output of the VR to the FPGA load.
- $f_{sw}$ = 800 kHz
- $N_{phase}$ = 6 (phase count of the multi-phase controller set-up)

## 3.1 Simulation

To test the hypothesis outlined above, extensive modeling is conducted on the PDN and the multi-phase model in SIMPLIS/Simetrix.

### 3.1.1 Transient simulation

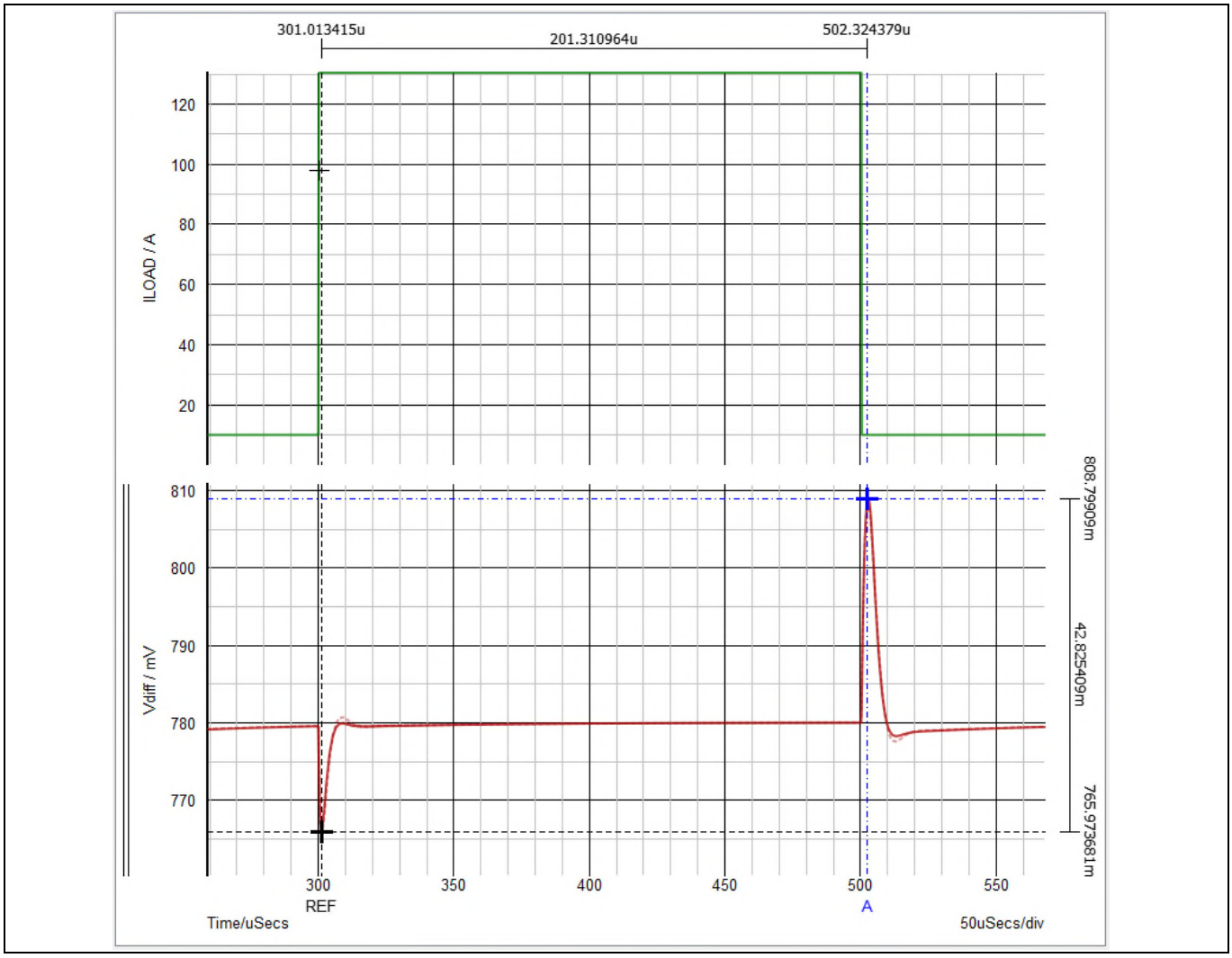



**Figure 4 Transient response of a six-phase buck converter without LL enabled**

In the above waveform, we are using a SIMPLIS model to examine the transient response of the control loop without LL enabled. At 300 µs, from 10 A there is a transient load step up to 130 A in 200 ns. During this time, $V_{OUT}$ dips to 0.765 V before the controller responds to the transient event. There is a slight overshoot as the $V_{OUT}$ swings back into regulation. During a load release of 130 A to 10 A, the output voltage has 28 mV overshoot before it reaches the 0.78 V steady-state value. A voltage-mode PID-based multi-phase controller is simulated here. On such a controller, the only way to minimize this overshoot is to either use a smaller output inductor value or more electrolytic capacitors on the output to sink the current. At the moment, the 28 mV overshoot is in violation of the original ±3 percent spec.

It is also worth noting the small overshoot during a load step and a slight undershoot during a load release on the $V_{OUT}$ waveform. This response indicates that the phase margin for the controller is around 50 degrees. The AC simulation shows this behavior.

### 3.1.2 AC simulation

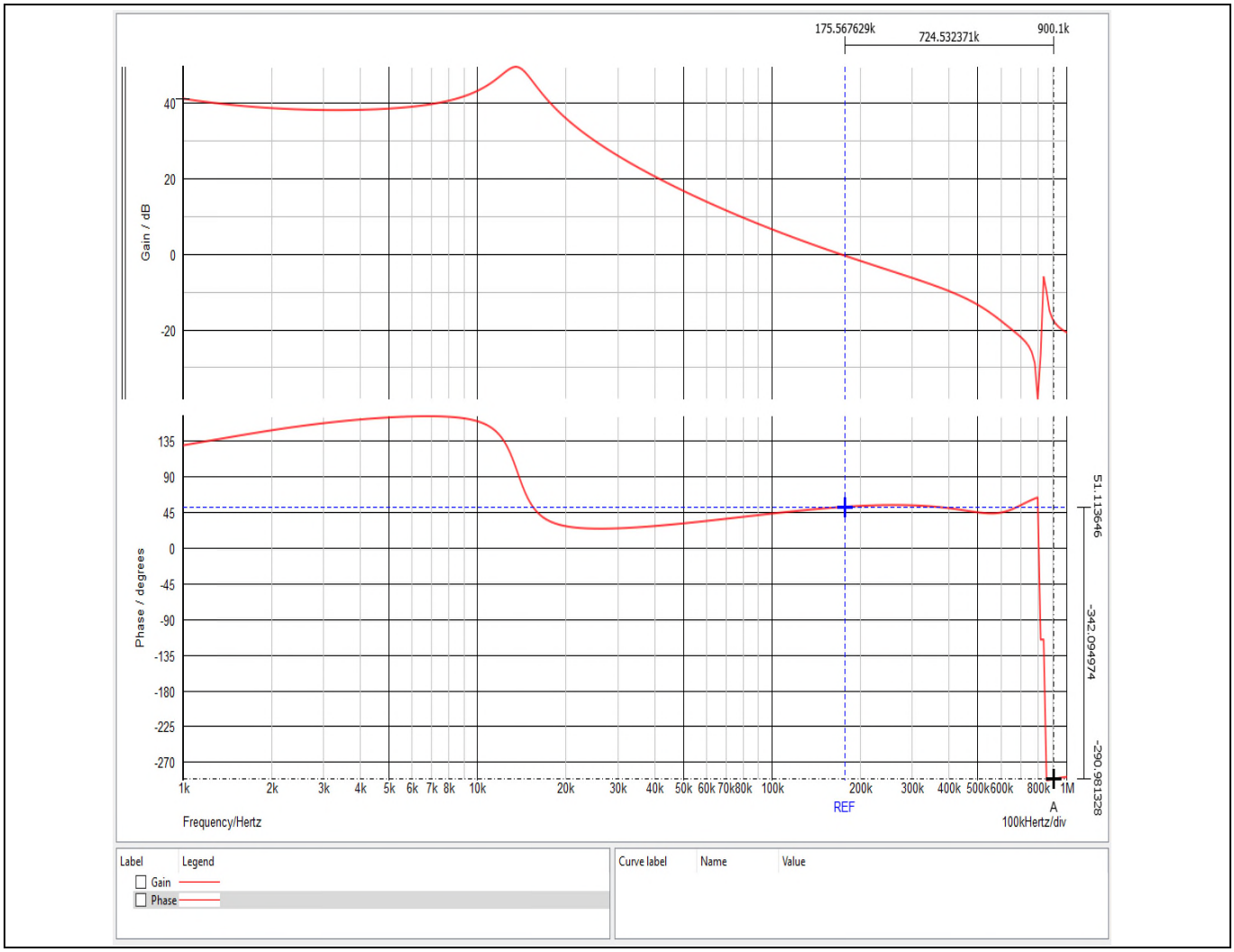



**Figure 5 Simulated Bode plot of the six-phase controller without LL enabled**

In Figure 5 the simulated Bode plot of the six-phase controller is plotted. The crossover frequency is expected to be around 175 kHz with a phase margin of 51 degrees. In voltage-mode-controlled systems the current in the output filter is not a controlled parameter. Therefore, the LC resonance is observable in the transfer function as a spike, accompanied by a 180-degree phase drop beyond the resonance frequency. This is a problem for stability, as the target for the crossover frequency is normally far beyond the LC filter pole frequency. Therefore, the Type III error amplifier is used to boost the phase by 180 degrees in the area where the LC double-pole phase drop occurs (red area in Figure 6).

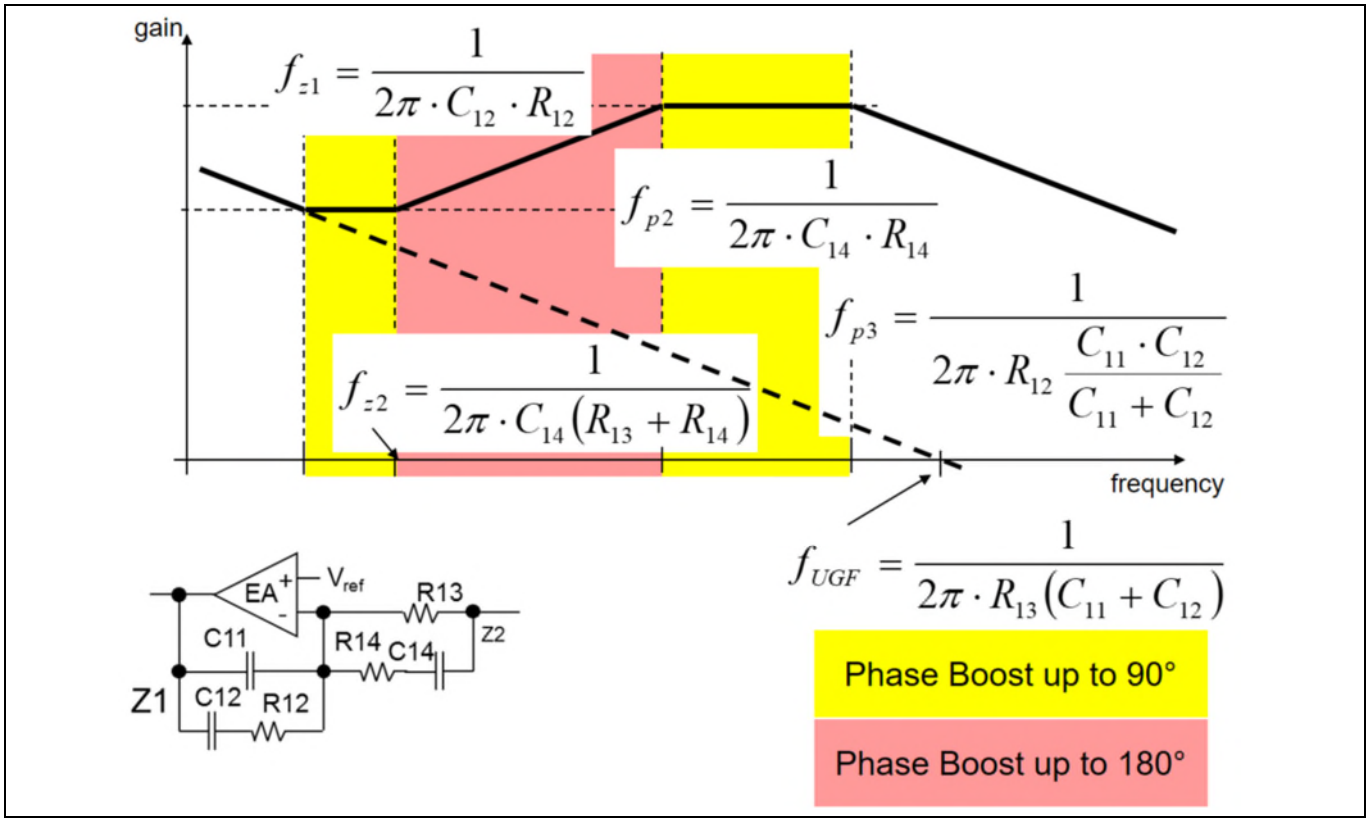



**Figure 6 PID compensation network with Type III analog error amplifier**

Figure 6 shows the traditional analog approach to a compensation network. Each R and C define one pole and one zero.

In our digital controller implementation the kp, ki and kd terms correspond to the gain of the first three line segments. The segments starting at fp2 and fp3 are set by additional HF pole values kfp_a and kfp_b. These correspond to similar terms in each controller GUI.

From a compensator standpoint, the ki integral value gain defines the crossover frequency at zero dB gain ($f_{UGF}$). The kp and kd terms set the mid-frequency gains for achieving the proper placement of the zeroes. The HF gain terms kfp_a and kfp_b affect the HF poles to provide attenuation for reaching the desired crossover frequency and gain margin.

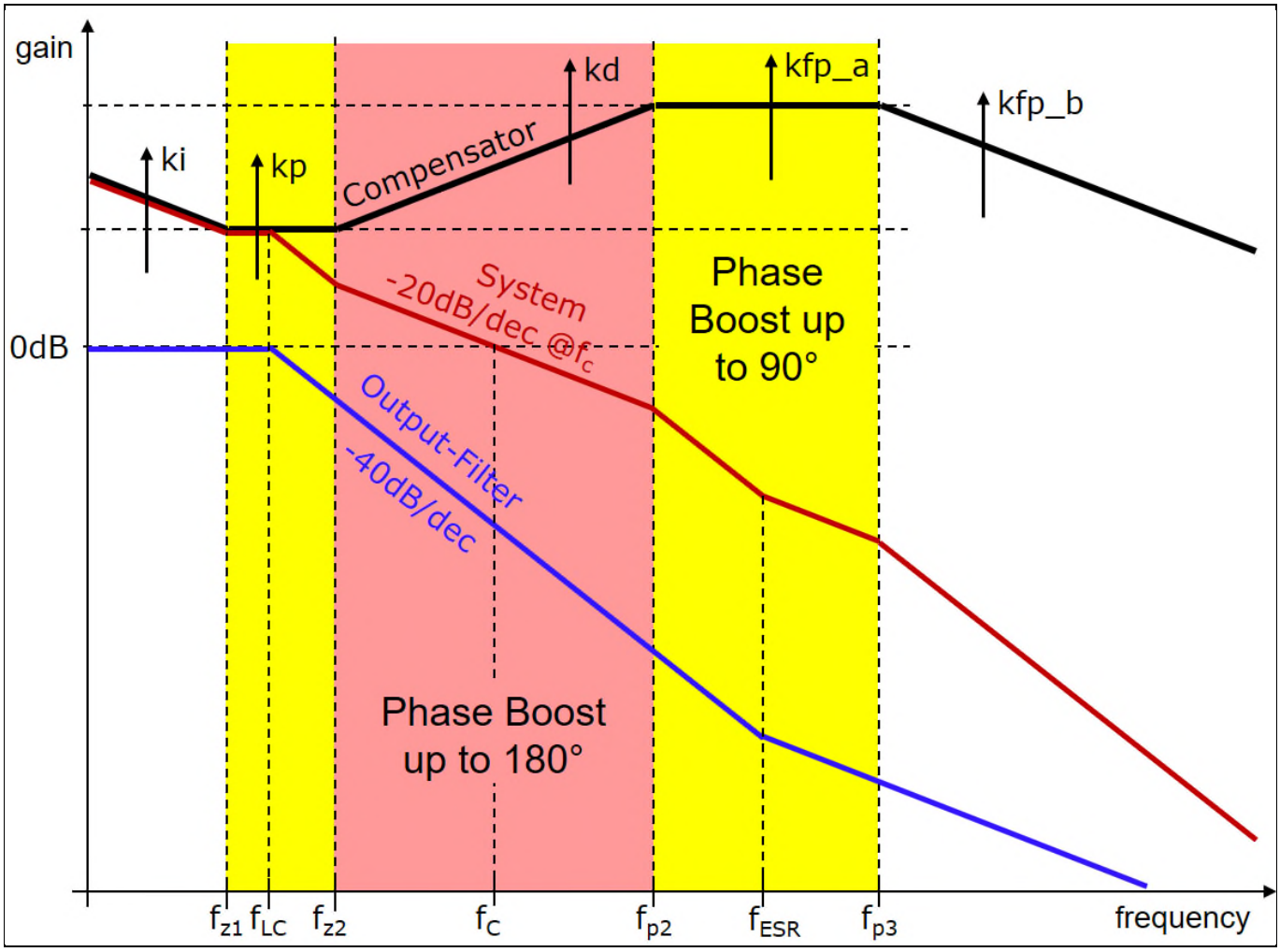



**Figure 7 Linearized frequency response of a voltage-mode-controlled buck converter at no LL**

The black waveform represents the frequency response of the PID compensation network. The blue waveform represents the frequency response of the output filter. The red waveform represents the output response of the overall system.

At the LC filter response shown in blue above, $f_{LC}$ represents the double-pole frequency of the output filter. In reality, all transitions between the linear segments are smooth.

The target is to achieve maximum phase gain at the crossover frequency by properly placing $f_{z2}$ and $f_{p2}$ with respect to $f_C$.

# 4 Analysis with LL

The test parameters and circuit values used are as follows:

- LL = 97.5 µΩ
- $L_{OUT}$ = 100nH inductor, DCR = 1 mΩ
- $C_{OUT}$ Bank 1 = 6 x 470 µF POSCAP
- $C_{OUT}$ Bank 2 = 12 x 47 µF ceramic caps
- $C_{OUT}$ Bank 3 = 60 x 22 µF ceramic caps (at FPGA load)
- $C_{OUT}$ Bank 4 = 70 x 47 µF ceramic caps (at FPGA load)
- $L_{pcb} \approx 50$ pH
  This represents the parasitic inductance between the output of the VR and the FPGA load. In this case, we are expecting a design with very good parasitic values.
- $R_{pcb} \approx 0.2$ mΩ
  This represents the parasitic copper resistance from the output of the VR to the FPGA load.
- $f_{sw}$ = 800 kHz
- $N_{phase}$ = 6 (phase count of the multi-phase controller set-up)

The difference to the case without LL is that there are six fewer 470 µF output bulk capacitors.

The value for the LL is based conservatively on a 240 A maximum current delivered while staying within one half of the voltage specification band:

$$Load_Line = \frac{23.4mV}{240A} = 97.5\mu\Omega \quad (1)$$

## 4.1 Theoretical expectations

The output voltage regulation loop for a voltage-mode buck converter is shown below:

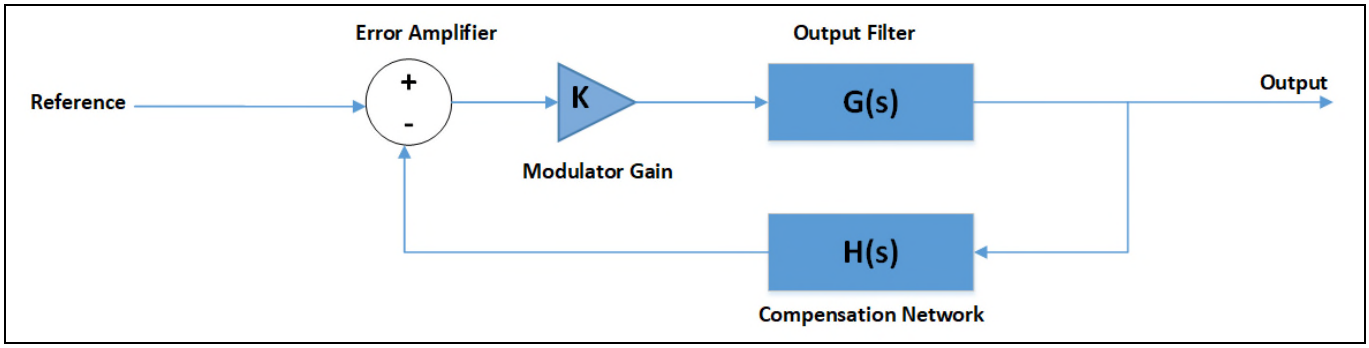



**Figure 8 Control loop of a voltage-mode buck converter**

In Figure 8 the control loop of a voltage-mode buck converter is shown, with K representing the modulation gain block. The transfer function of the output filter G(s) and the transfer function of the compensation network H(s) will close the control loop.

$$K = \frac{V_{IN}}{\Delta V_{OSC}} \quad (2)$$

$$G(s) = \frac{1+s*ESR*C_{OUT}}{1+s(ESR+DCR)*C_{OUT}+s^2*L_{OUT}*C_{OUT}} \quad (3)$$

G(s) represents the transfer function of a second-order LC output filter network with ESR being the effective Equivalent Series Resistance of the output capacitor bank. $C_{OUT}$ is the total output capacitance at the output of the voltage regulator.

The transfer function of the output filter plotted below uses the following values:

$C_{OUT}$ = 470 µF x 12 + 47 µF x 12 = 6204 µF
L = 100 nH
DCR = 1 mΩ

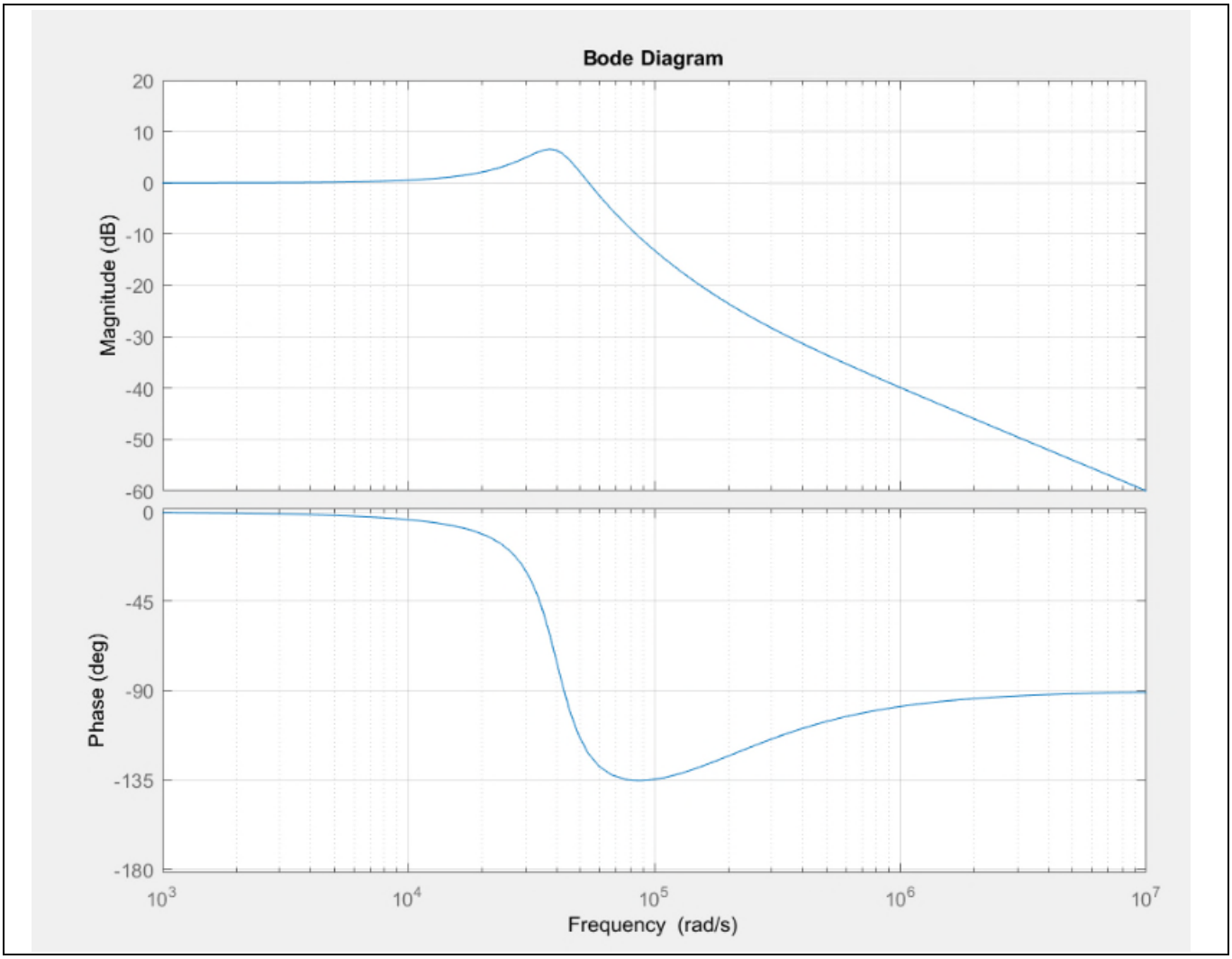



**Figure 9 Bode plot of the output filter of the voltage regulator**

The inherent damping of the filter is too small to prevent a substantial phase decay by -135 degrees and the characteristic gain peak at the LC resonant frequency.

By introducing a LL the reference voltage is affected by the output current. The figure below shows the control loop with LL implementation.

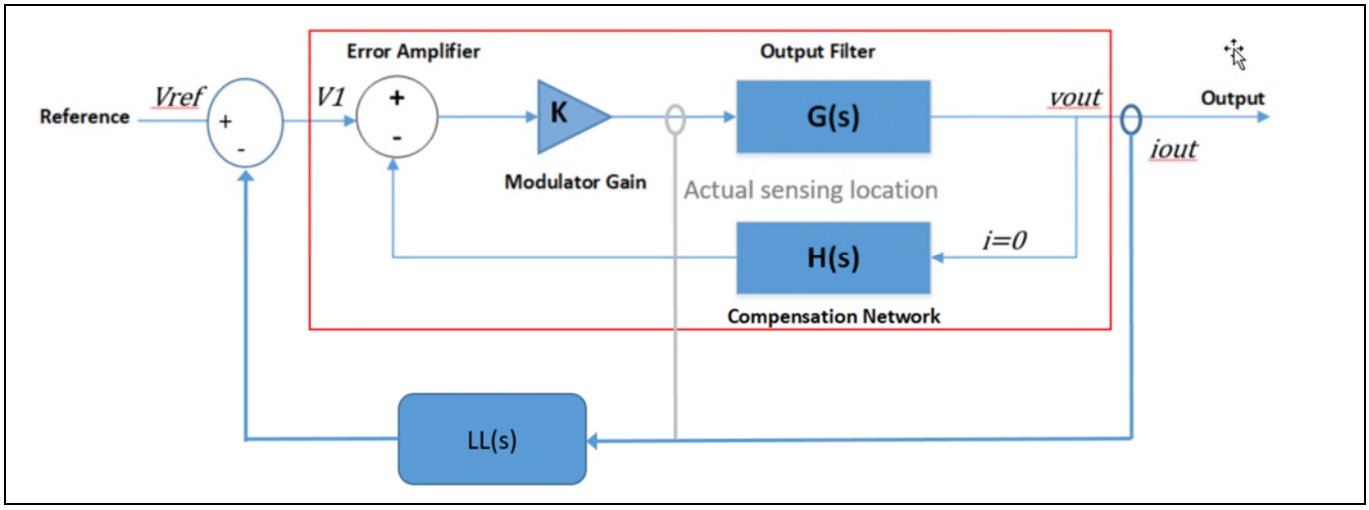



**Figure 10 High-level-control-block diagram of a voltage-mode buck converter with LL**

The sensing location of the current can be inside the power train of the power stage. Because the signal measured is the output current, it is practically identical (for our considerations within the frequency range considered) to the output current, so the LL block can be wrapped around the converter in Figure 8.

This leads to an inner loop consisting of the case without LL (eq. 5) and an outer loop in which the reference control is wrapped around the inner block (eq. 6).

$$vout = G(s) \cdot \mathrm{K} \cdot (V1 - H(s) \cdot vout) \tag{4}$$

$$vout/V1 = G(s) \cdot \mathrm{K}/(1 + G(s) \cdot H(s) \cdot K) \tag{5}$$

$$V1 = Vref\text{-}LL \cdot Iout \cdot \frac{1}{1+s/\omega_{AVP}} \tag{6}$$

$$\frac{vout}{Vref\text{-}\mathrm{LL}\cdot\mathrm{iout}\cdot\frac{1}{1+s/\omega_{AVP}}} = \frac{G(s)\cdot\mathrm{K}}{1+G(s)\cdot H(s)\cdot K} \tag{7}$$

$$vout = \frac{G(s)\cdot K}{1+G(s)\cdot H(s)\cdot K} \cdot \left(Vref\text{-}LL \cdot iout \cdot \frac{1}{1+s/\omega_{AVP}}\right) \tag{8}$$

The differential output impedance is given by:

$$\frac{d(vout)}{d(iout)} = \frac{G(s)\cdot\mathrm{K}}{1+G(s)\cdot H(s)\cdot K} \cdot \frac{-LL}{1+s/\omega_{AVP}} \tag{9}$$

The AVP filter frequency must be greater than the LC pole frequency to obtain good attenuation of the LC resonance.

The reason for suppression of the LC resonant spike can be understood as follows:

The current through the output filter is in series with the load. At high current at the LC resonance frequency the current increase in the filter leads to an output voltage drop. The regulator compensates for it by driving harder (longer duty cycle delivering more energy). Much of it feeds the resonant tank, leading to the observable spike and rapid phase decay.

### Analysis with LL

Having a LL that is rolled off beyond the LC double-pole frequency means that a voltage decay by current does not require full compensation since the voltage is meant to decrease. Therefore, less or no additional energy will be fed into the resonant circuit, resulting in less or no excitement of the LC resonance.

This can be verified by simulation. Figure 11 shows a circuit AC simulation with a 1 mΩ LL. The dotted plot has an AVP roll-off at 10 kHz while the solid line has it at 100 kHz.

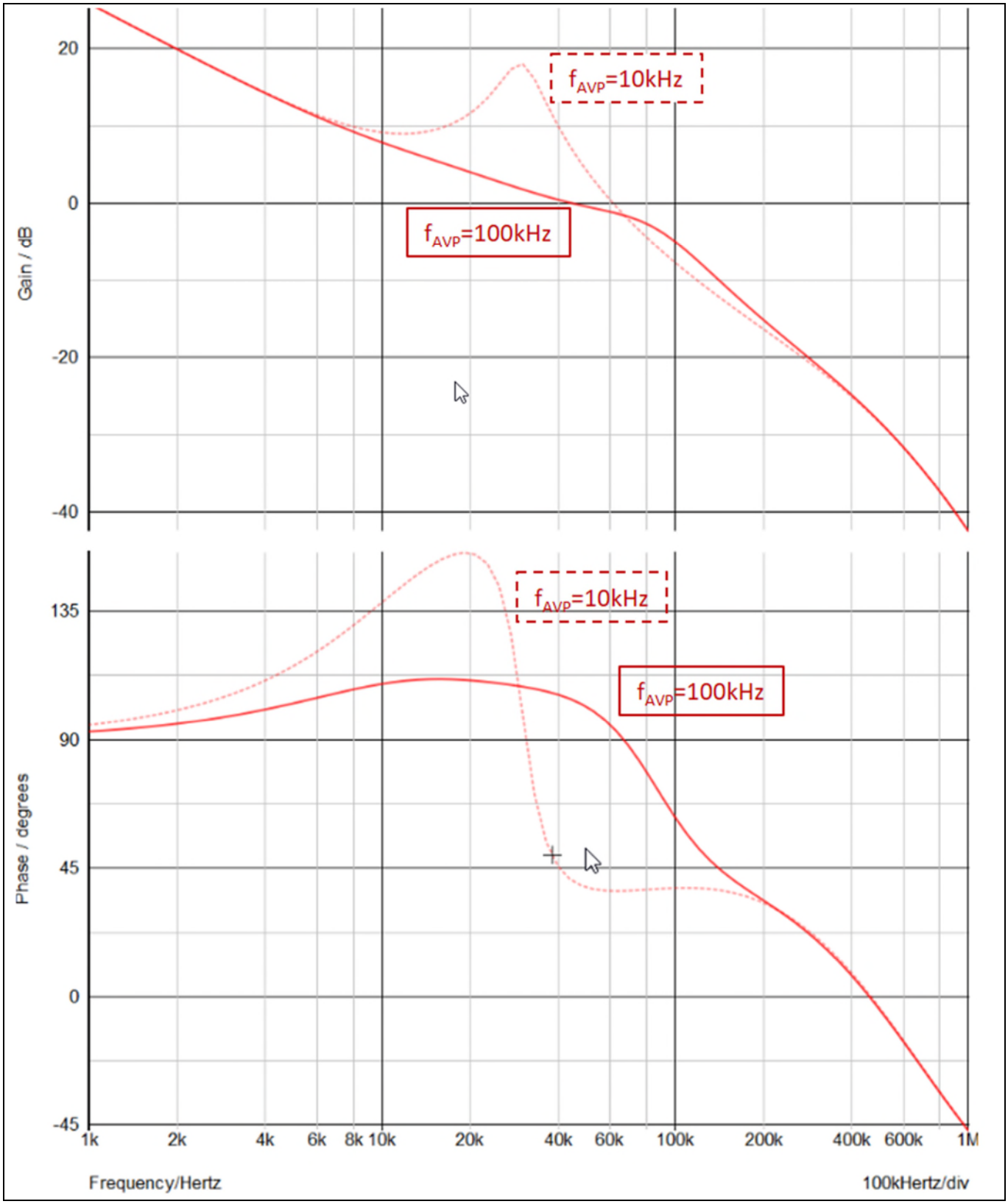



**Figure 11 AVP roll-off frequency impact on resonant spike**

With AVP roll-off at 100 kHz, the crossover frequency is around 50 kHz with about 112 degrees of phase margin and almost no resonant peak, while the AVP roll-off at 10 kHz has virtually no effect on the resonant double pole at 30 kHz.

That shows that the zero introduced by the LL contributes to the phase boost and successfully attenuates the LC resonant spike in the voltage transfer function.

## 4.2 Transient simulation with LL

To recap, the target range for the output voltage to be in 0.78 V ±23.4 mV. Since we set our zero-load voltage to the nominal value, the LL cannot be greater than 0.0975 mΩ to meet the goal at 240 A load current. The bulk capacitor count of the 470 µF capacitors was reduced from 12 to 6.

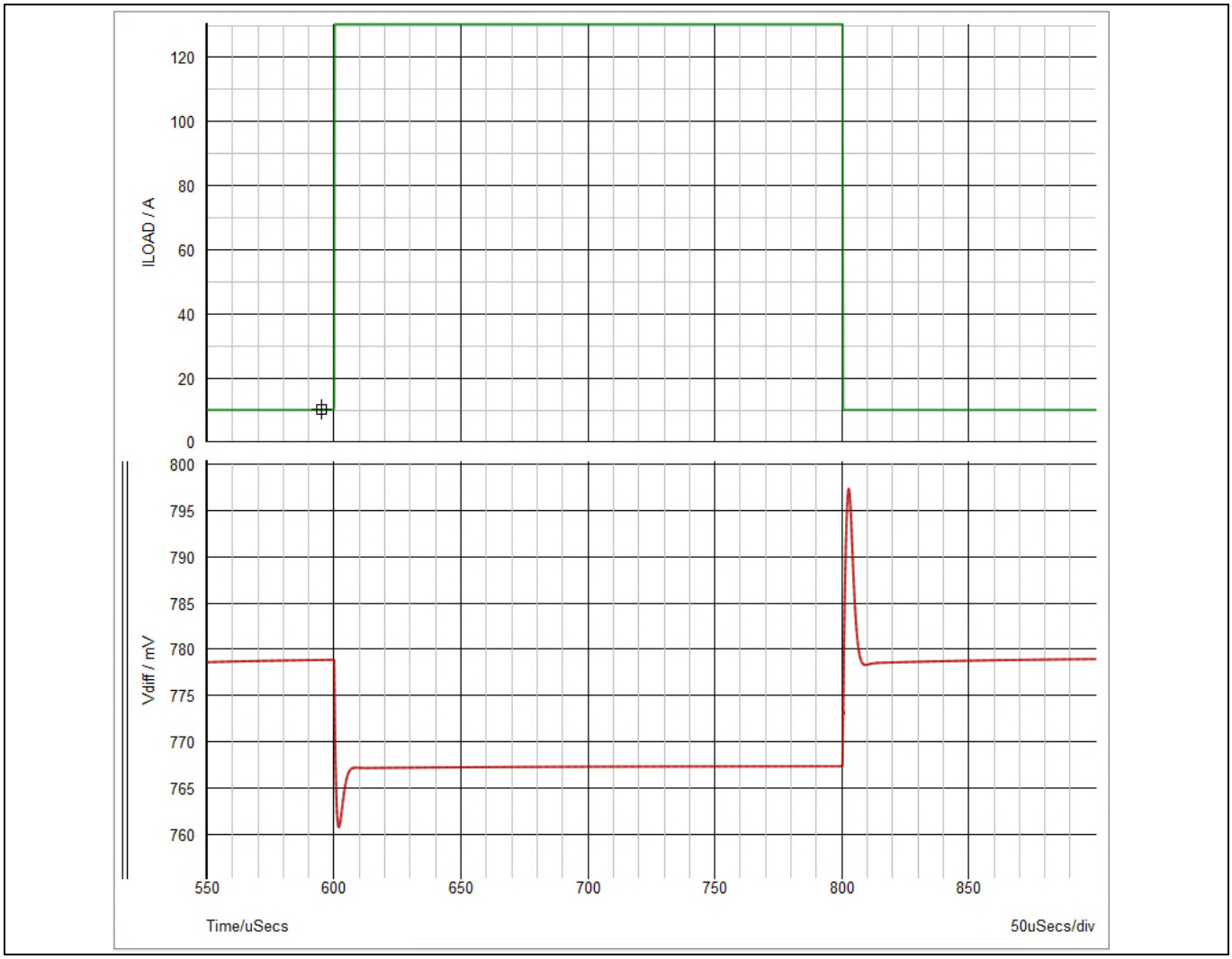



**Figure 12 Transient response with 97.5 µΩ of LL**

Observations:

The output voltage droops to 779 mV at 10A, and to 767.3 mV at 130 A. The lowest value simulated is at about 761 mV. During the load release there is a voltage overshoot to 797.5 mV. The voltage undershoot can be minimized by using a more aggressive PID compensation. However, the response as it settles at 767 mV is that of a critically damped system. This indicates a phase margin of around 75 degrees. Also, with this undershoot, the output voltage is well within the ±3 percent deviation spec.

During the 130 A to 10 A load release, the output voltage should settle at 779 mV. There is overshoot to 797 mV before settling. The 797 mV is also below the targeted maximum of 803.4 mV per deviation spec.

## 4.3 AC simulation with LL

The Bode plot of the six-phase buck converter in voltage-mode control with LL is shown below:

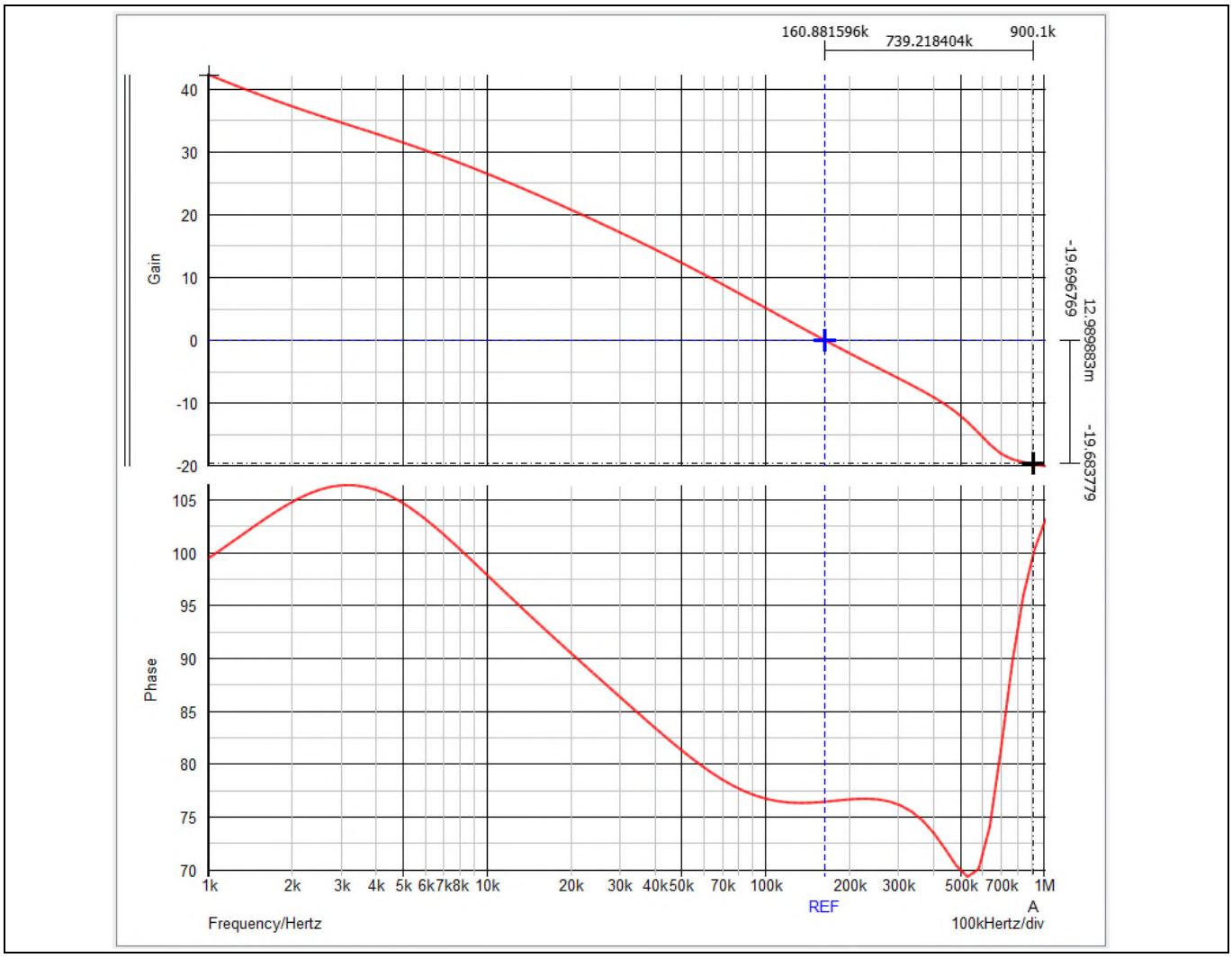



**Figure 13 Bode plot of the control loop with 97.5µΩ of LL**

The gain plot has no observable peak and the phase stays well above76 degrees far beyond the crossover frequency of 161 kHz, with about 76 degrees of phase margin.

## 4.4 Measurements

All measurements are taken with the setting of infinite persistence over multiple load cycles.

### 4.4.1 Transient measurements with LL

The repetitive load-transient test was set up at the GUI of the Intel VRTT tool to toggle between 10 A and 130 A at 1 kHz with a duty cycle of 0.5. The load current transient steps up and down are 200 ns each.




**Figure 14 Transient load steps and releases over multiple load cycles at a duty cycle of 0.5 and 1 kHz repetition rate**

At any given time $V_{OUT}$ must be between 756.6 mV and 803.4 mV.

### Analysis with LL

A closer look during the load step and load release conditions provides insight:

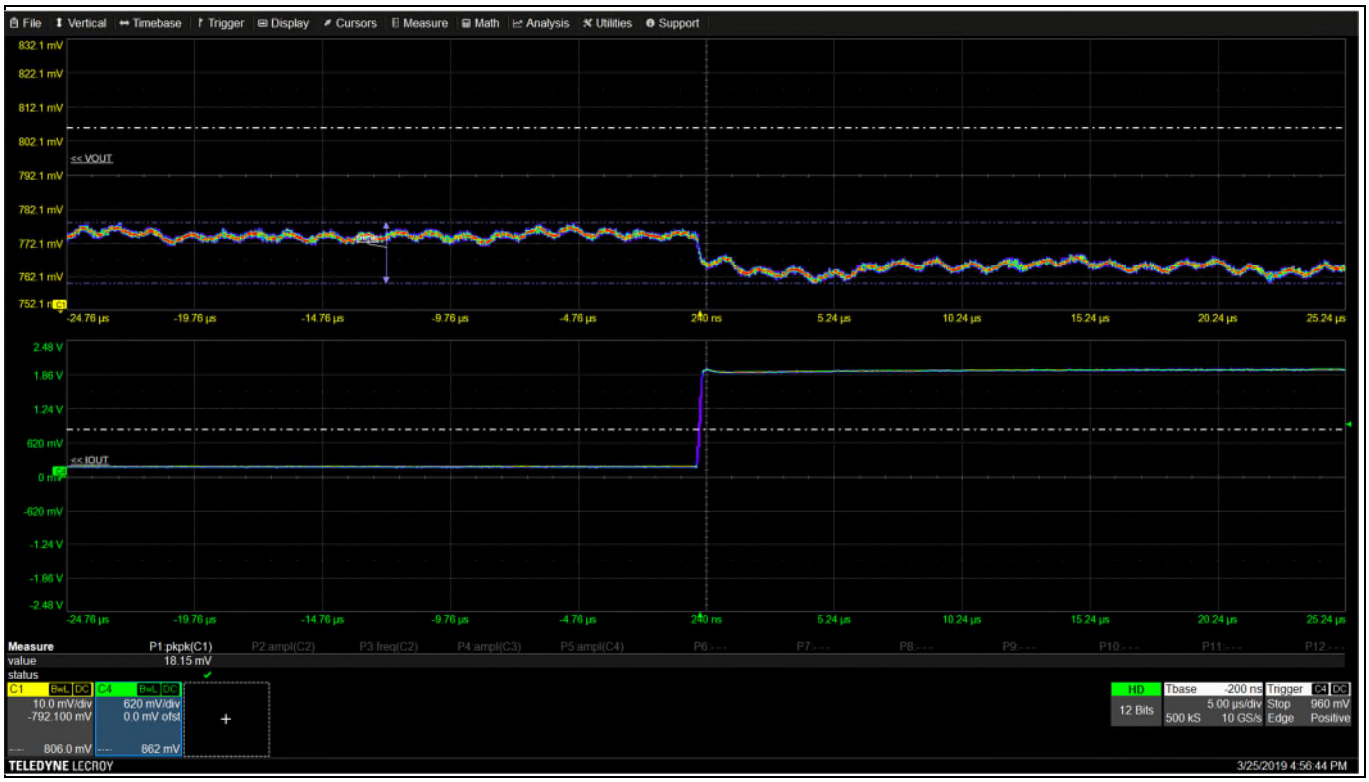



**Figure 15 Transient load step from 10 A to 130 A in 200 ns**

The output voltage droops to about 760 mV during the load step.

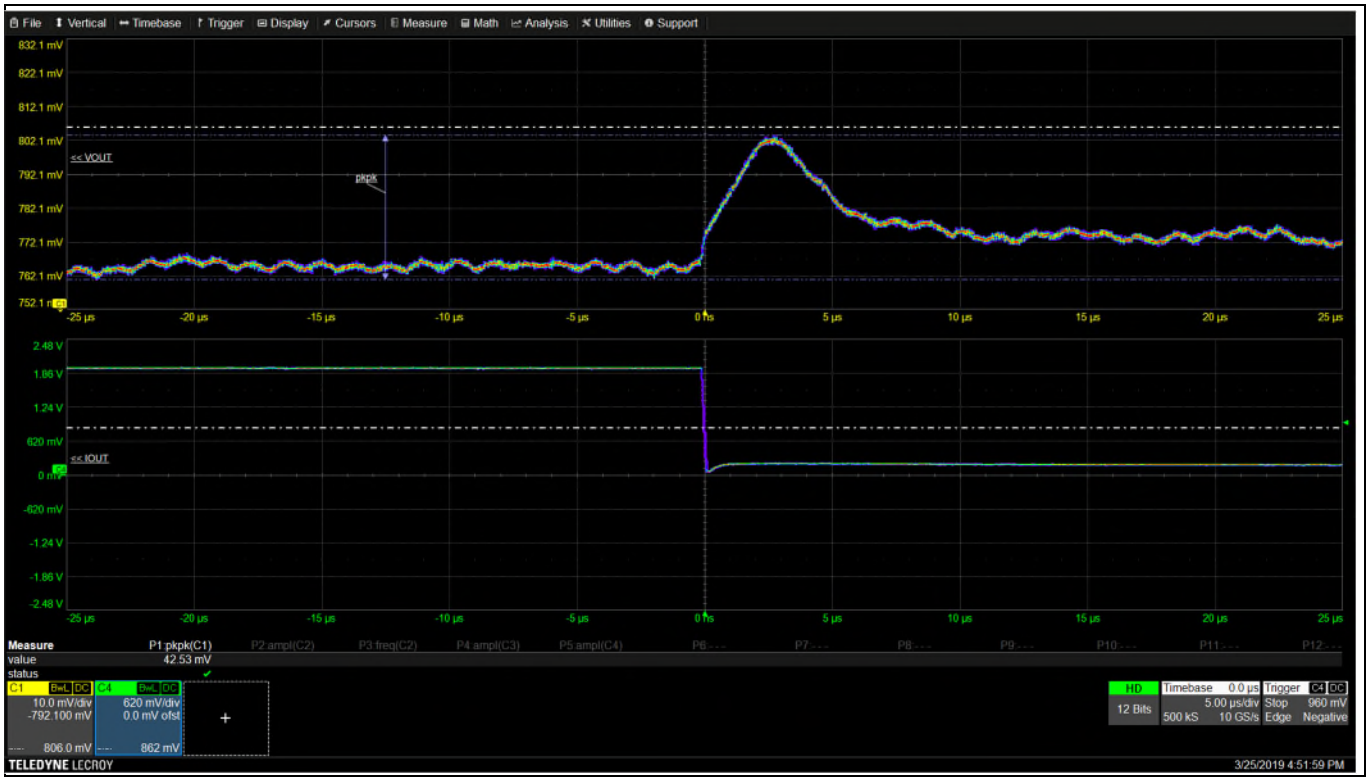



**Figure 16 Transient load release from 130 A to 10 A in 200 ns**

During the 130 A to 10 A load release a big overshoot of the output voltage is observed as result of the phase inductors' stored energy. The output voltage peaks at 802.1 mV.

The overshoot can be minimized by design using smaller phase inductors and/or by applying non-linear control techniques such a diode braking, for example.

Without LL and with only 6 x 470 µF POSCAPs the $V_{OUT}$ overshoot would have been significantly higher, as the steady-state value of $V_{OUT}$ before the load release was at already 780 mV.

### 4.4.2 AC measurement with LL

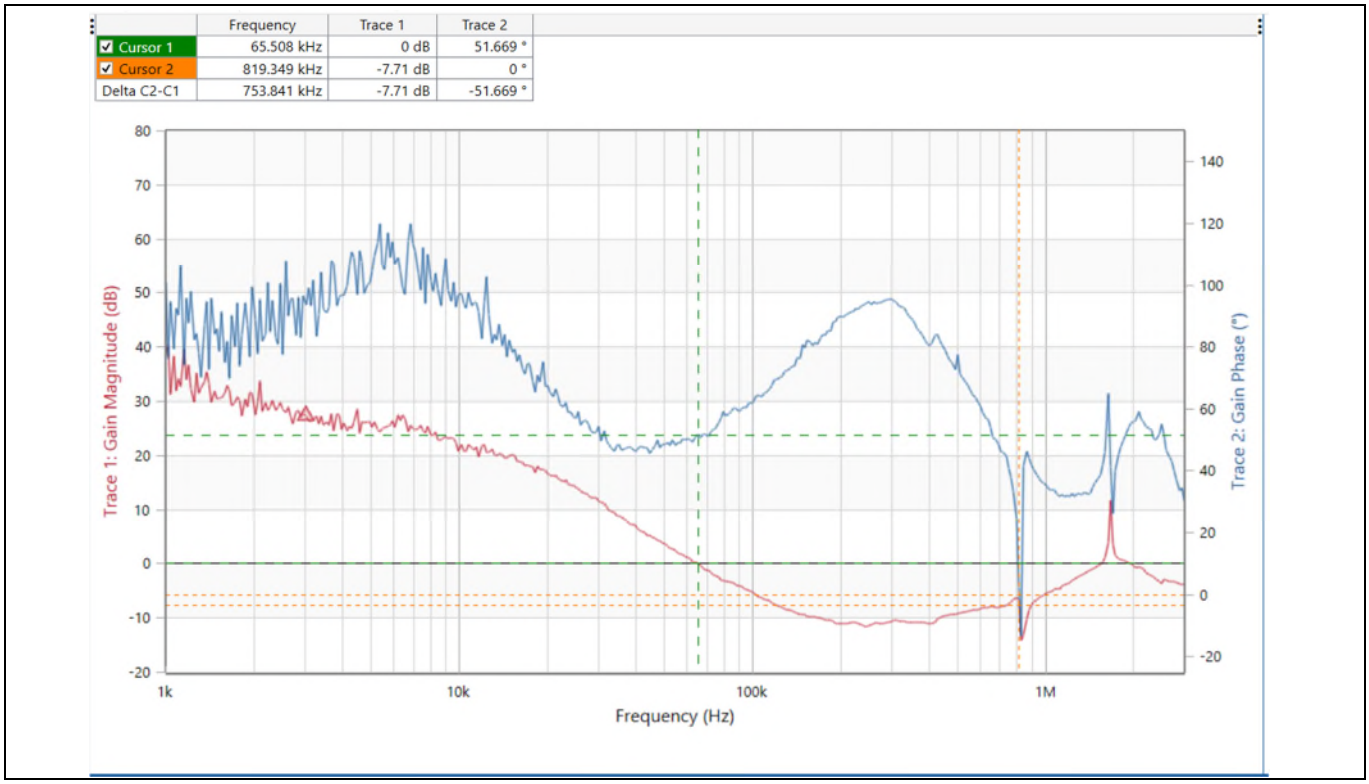



**Figure 17 Bode plot of the PXE1610C control loop with 130 A of constant load current**

The Bode plot analysis of the test board confirms the effect of the applied LL. There is no gain peak, and high phase margin far beyond the crossover frequency.

# 5 Conclusion

The implementation of a LL into the design has brought tangible improvements:

- Six fewer 470 µF output bulk capacitors, saving cost and board space
- Less compensation effort on fine-tuning the control loop

The low-pass filter in the LL feedback loop provides gain and phase boost in the transfer function and removes the voltage gain caused by the output filter resonance. That simplifies the compensation effort.

A small LL such as that shown here is almost always an option, as the specification for power delivery needs to have a band in which the regulation of transients can occur. A LL exploits this band to the extend, that it will be maximized for load steps by moving the steady-state voltage within that band to allow for a bigger available permissible excursion range before reaching the specification limits.

The voltage ripple has not been considered in this discussion, as its impact is very small compared to any transient excursion. However, any design needs to have enough room to absorb half of the output voltage ripple for any transient step in addition to the voltage change caused by the transient.

## Revision history

| Document version | Date of release | Description of changes |
|---|---|---|
| 1.0 | 03/29/2019 | Initial release |
| | | |
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