Configuration of inverting buck-boost using IR3889 buck regulator

About this document

Scope and purpose

This application note summarizes the application approaches of deriving an inverting buck-boost using DC-DC buck regulator which uses Fast COT (constant on-time) architecture.

Intended audience

Customers, field application engineers and application engineers who design power conversion circuits with Fast COT point-of-load (POL) products

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1 Introduction

Among Infineon's POL product families, the proprietary Fast COT is the most popular loop control. It achieves fast load transient as conventional COT control does, but at the same time, it maintains high DC accuracy in V_{out} as voltage mode and current mode control do. A quick introduction to Fast COT control is available on Infineon's website [1].

This application note demonstrates a unique way of generating a negative output voltage rail from a positive input voltage of the standard buck regulator. This topology is called "inverting buck-boost".

Many systems require a negative power supply rail; in general, a positive supply with respect to ground is always available. Examples of such systems include both medical ultrasound scanners and test and measurement equipment. Other uses have been observed in LCD displays and embedded applications, where some application-specific ICs require a negative supply. A unique DC-DC regulator called an inverting buck-boost can be used to provide this negative output voltage from a positive supply, with a common ground connection. Almost any ordinary buck regulator can be converted into an inverting buck-boost with a few simple changes in line and load connections.

The design example uses the IR3889 regulator [2] to demonstrate the design procedure. The IR3889 is an easy-to-use, fully integrated –DC-DC buck regulator. The onboard PWM controller and OptiMOS™ FETs with integrated bootstrap diode make IR3889 a small-footprint solution, providing highly efficient power delivery. Furthermore, it uses a Fast COT control scheme, which simplifies the design efforts and achieves fast control response. The IR3889 is a versatile regulator, offering programmable switching frequency from 600 kHz to 2 MHz, four selectable current limits, four selectable soft-start times, forced continuous conduction mode (FCCM) and diode emulation mode (DEM) operation.

This document details the procedure for designing the circuit, capturing the test results of the designed circuit. The procedure can be applied to the family of POLs.

2 Design requirements

The designed circuit has to meet the following requirements:

Table 1 Design parameters of the converter

Input voltage, V_{IN}	+5 V
Output voltage, V_{OUT}	-5 V
Output current	5 A
Switching frequency	600 kHz
Mode	FCCM

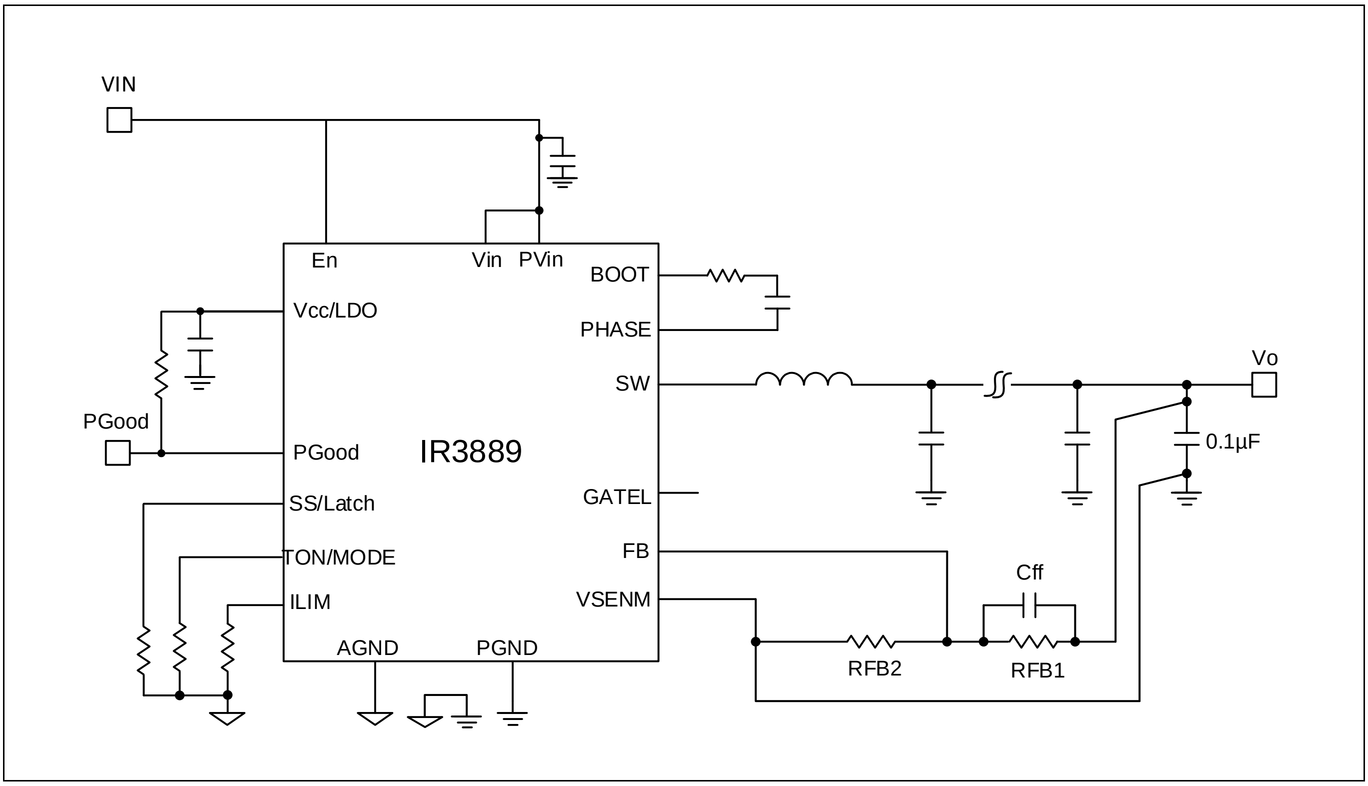

Figure 1 Typical application of IR3889

2.1 Inverting buck-boost topology

The simplified inverting buck-boost topology is shown in Figure 2. The topology consists of an inductor, two hpower switches operating out of phase from one another, and input and output capacitors. During the on-time, the primary switch (Q1) is conducting and current is flowing from the input and charging the inductor (L1) while the output capacitor (C_{OUT}) provides energy to the load (R_{LOAD}). During the off-time, the secondary switch (Q2) is conducting and current is flowing through the inductor to the load and the output capacitor. Because this is an inverting topology, the current flows from ground to -V_{OUT}, which is negative, through the load.

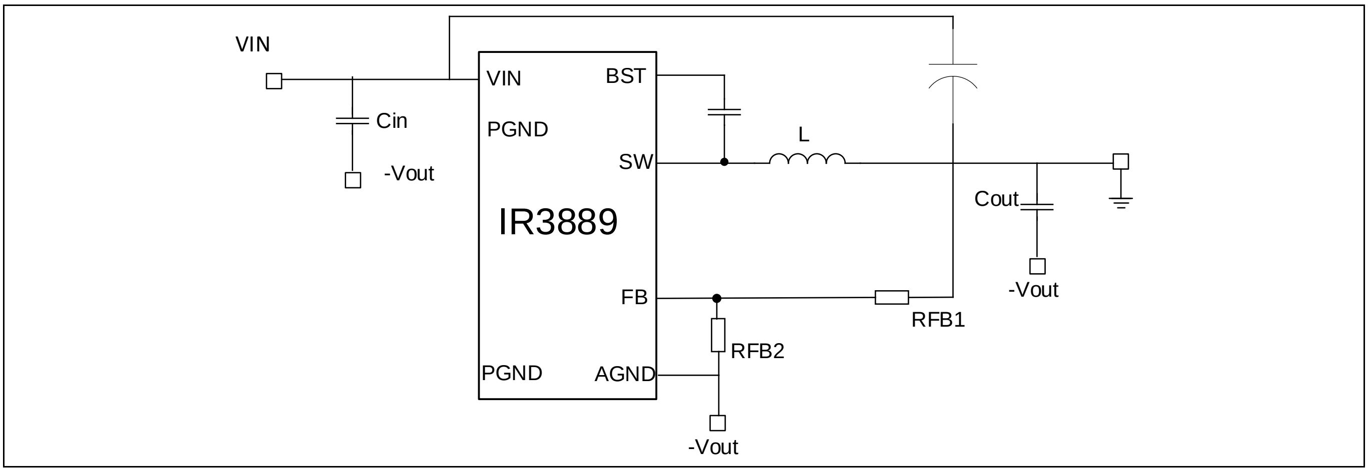

Figure 2 **Inverting buck-boost topology**

2.2 Converting buck into inverting buck-boost

The buck regulator takes a positive input voltage and converts it to a positive output voltage of smaller magnitude. The inverting buck-boost takes a positive input voltage and converts it to a negative output voltage, with a common ground connection between input and output. We can observe the similarity between the two regulators. The regulator in Figure 3 shows the connections for taking the buck regulator and converting it into an inverting buck-boost. Looking at the connections highlighted, we see that the buck output is now the system ground and the buck "ground" becomes the negative output. An additional input capacitor is added between the input supply and system ground. Notice that the "ground" reference for the IC is now the negative output voltage. This has consequences for the maximum input voltage and the control inputs when using this configuration. Therefore, no extra level shift or inversion of the feedback signal is needed to properly regulate the negative output. Also, note that the feedback connection to the regulator is not changed from that of an ordinary buck.

The connection changes are detailed in the following list:

1. Assign the buck regulator positive output as system ground.

2. Assign the buck regulator ground connection as the negative output voltage.

3. The positive input stays the same.

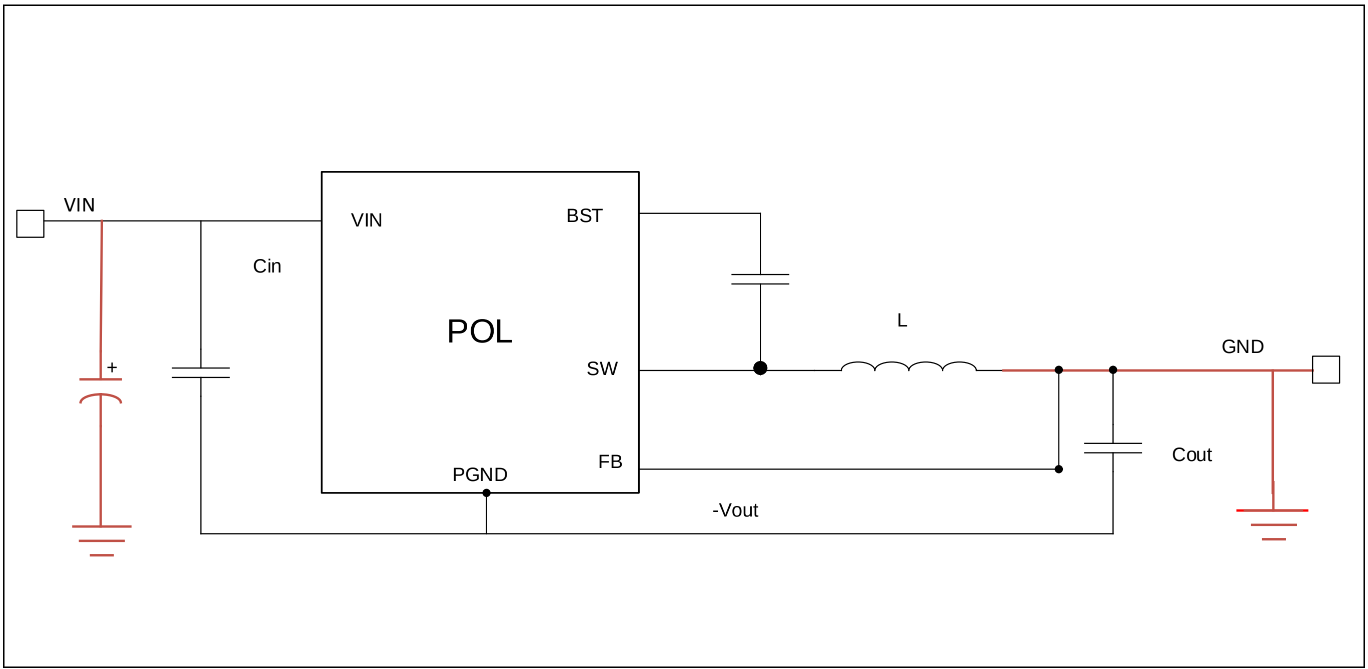

Figure 3 **Configuring inverting buck-boost using buck regulator**

2.3 Operation

The basic operation of the regulator is as follows. During the portion of the switching cycle in which the HS FET is on, the inductor voltage is equal to V_{IN}. For the remainder of the switching cycle, the LS FET turns on and the inductor voltage is $-V_{OUT}$. At this point the inductor energy is supplied to the load and the output capacitor. The regulator regulates the output voltage by adjusting the duty cycle of the HS and LS FET switches.

When the voltage is first applied to the circuit the initial capacitor charge current will cause a positive voltage spike at the output when the capacitor CC is used. However, this positive voltage spike is typically small enough to not cause any problems. The initial capacitor charge current will cause a voltage drop across the capacitor equivalent series resistance (ESR). Since the capacitor CC and output capacitor form a voltage divider, the magnitude of the initial voltage spike depends on the ESR values of CC and the output capacitor. Since the overall output capacitor ESR value is usually much smaller than the compensation capacitor ESR, the initial voltage spike is very small.

3 Selection of external components

3.1 Selection of inductor

The average inductor current is affected in this topology. In the buck configuration, the average inductor current equals the average output current because the inductor always supplies current to the load during both the on- and off-times of the control MOSFET. However, in the inverting buck-boost configuration, the load is supplied with current only from the output capacitor and is completely disconnected from the inductor during the on-time of the control MOSFET. During the off-time, the inductor connects to both the output capacitor and the load. Knowing that the off-time is 1 – D of the switching period, then the average inductor current is:

$$IL(avg) = Iout/(1-D)$$

The duty cycle for the typical buck regulator is simply V_{OUT}/V_{IN} but the duty cycle for an inverting buck-boost regulator becomes:

$$D = Vout/(Vout + Vin)$$

The peak inductor current will be:

$$IL(peak) = Iout + \Delta Il/2$$

The inductance value will be:

$$L = \frac{Vin * D}{Fsw * \Delta Il}$$

Where Fsw is switching frequency.

Where $\Delta Il = 0.2\ to\ 0.3\ times\ of\ IL(avg)$

3.2 Selection of output capacitor

Ordinarily, the output capacitor energy store of the regulator combined with the control loop response are prescribed to maintain the integrity of the output voltage within the dynamic (transient) tolerance specifications. The usual boundaries restricting the output capacitor in power management applications are driven by finite available PCB area, component footprint and profile, and cost. The capacitor parasitics - ESR and equivalent series inductance (ESL) -take greater precedence in shaping the load transient response of the regulator as the load step amplitude and slew rate increase. The output capacitor, COUT, filters the inductor ripple current and provides a reservoir of charge for step-load transient events.

Typically, ceramic capacitors provide extremely low ESR to reduce the output voltage ripple and noise spikes, while tantalum and electrolytic capacitors provide a large bulk capacitance in a relatively compact footprint for transient loading events.

$$Cout \geq \frac{ILoad * D}{Fsw * \Delta Vout}$$

Where $\Delta Vout$ is desired output ripple voltage

To meet the dynamic specification of output voltage overshoot during such a load-off transient additional capacitance can be added based on the transient specification.

3.3 Selection of input capacitors

As we see from Figure 3 the input capacitor(s) of the buck become the capacitance between input and output of the inverting buck-boost. Typically, this will be one or two ceramic capacitors in parallel with a small case-size high-frequency bypass capacitor. To size these capacitors, use the recommendations in the buck data sheet; they can also be increased if desired. The new capacitors can help with load transients by providing a path from input to output for the load current transient. Remember that the capacitor bank will see a voltage of V_{IN} + $|V_{OUT}|$, and must have a voltage rating in excess of this voltage to help mitigate the voltage derating effect of the ceramic capacitors. As a first pass, the output capacitor can be sized based on the buck data sheet recommendations. Although the first pass should be stable, the output capacitors will probably need to be increased to get the best performance.

New input capacitor for inverting buck-boost: Input capacitor from V_{IN} to system ground helps to provide a low impedance path at the input for the inverting buck-boost. This can be a ceramic or a large-value aluminum electrolytic capacitor.

$$Cin \geq \frac{Irms * D}{Fsw * \Delta Vout}$$

Where

$$Irms = Iload * \sqrt{D * (1 - D)}$$

3.4 Selection of feedforward capacitor

A small MLCC capacitor, Cff, is preferred in parallel with the top feedback resistor, RFB1, to provide extra phase boost and to improve the transient load response. The following formula can be used to help select Cff and RFB1. The value of Cff is recommended to be 100 pF or higher to minimize the impact of circuit parasitic capacitance, where L_{OUT} and C_{OUT} are the output LC filter of the buck regulator. The table lists the suggested k for some common outputs. Cff and RFB1 may be further optimized based on the transient load tests.

$$R_{FB1}C_{ff} = \frac{\sqrt{L_0 C_0}}{k \times 5.6}$$

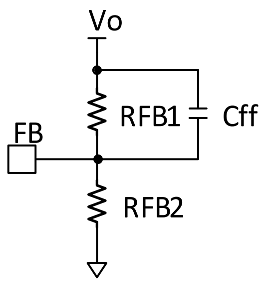

Figure 4 Selection of Cff capacitor

Table 2 Selection of k

Vo	k
-3 V ≤ V_{OUT} ≤ -5 V	0.4
-3V < V_{OUT} < -1.2 V	0.6
V_{OUT} ≤ -1.2 V	0.8

4 Operating conditions of inverting buck-boost based on buck

4.1 Voltage stress

Voltage stress selecting a buck regulator to convert to an inverting buck-boost requires special attention to the voltage and current requirements of the application. A quick glance at Figure 5 shows that the voltage across the V_{IN} and GND pins of the regulator IC is equal to the input voltage plus the negative output voltage. This voltage is greater than for a buck regulator, which only sees the input voltage across the V_{IN} and GND terminals. As an example, if you needed to convert from an input of +12 V to an output of –12 V, you would need a regulator with a voltage rating of at least 24 V. This would exclude many of the available "16-V" devices, requiring the use of a device rated at 36V or more. The datasheet specification that applies here is the "Input Voltage Absolute Maximum" ratings.

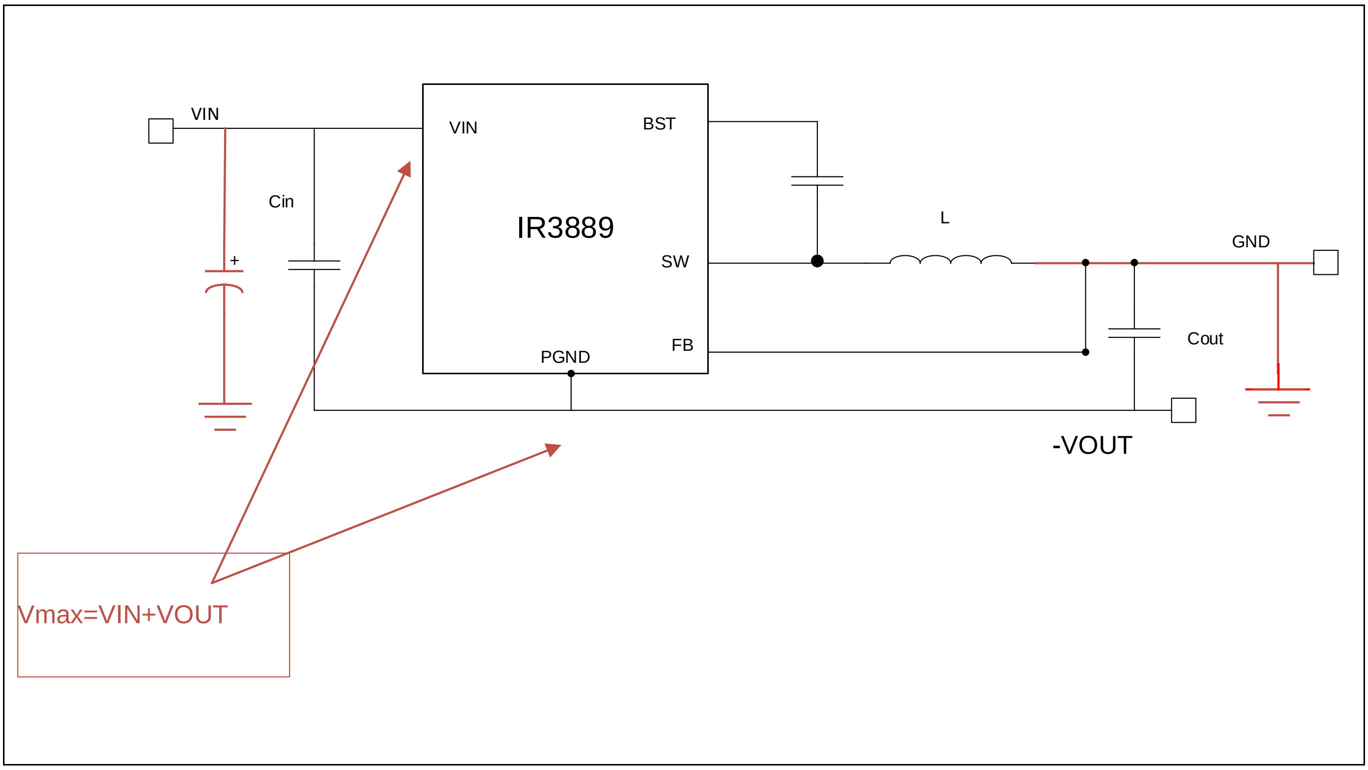

Figure 5 Maximum voltage rating of the converter

4.2 Current stress

The inductor currents and peak switch currents in the inverting buck-boost are larger than in the equivalent buck regulator from which it is made. First, the average input supply current can be calculated as for any regulator:

$$Iin = Iout * \frac{Vout}{Vin * \eta}$$

When the magnitude of the output voltage is less than the input voltage (buck mode), the input current is less than the output current. This is the same as for an ordinary buck. However, when the output voltage is greater than the input voltage (boost mode), the input current is greater than the output current. This is the same as for an ordinary boost regulator. Another thing to note is that the efficiency of the inverting buck-boost is somewhat less than an equivalent buck or boost, which is discussed below. The average inductor current is the sum of the input and output currents, and is given by the equation below; the peak and valley of the inductor current are also mentioned below. The first term in the equation is the average inductor current, while the second and third terms represent the inductor ripple current. Since the peak and valley of the inductor current pass through the MOSFET power switches, they determine how much output current a given inverting buck-boost can supply, when built from a buck. Most buck regulators are rated for a certain maximum load current. This is convenient since the load current and average inductor current are the same for a buck. However, one can understand from the equations that the average inductor current for an inverting buck-boost is always greater than the load current. Therefore, choose a buck regulator with a greater maximum load current when using it as an inverting buck-boost.

$$IL(avg) = Iout * [1 + \frac{Vout}{Vin * \eta}]$$

$$IPeak = Iout * \left[1 + \frac{Vout}{Vin * \eta}\right] + \frac{Vin * D}{2 * Fs * L}$$

$$IValley = Iout * \left[1 + \frac{Vout}{Vin * \eta}\right] - \frac{Vin * D}{2 * Fs * L}$$

4.3 Output clamp

Many times, the negative supply is used in conjunction with a positive rail to supply a common load such as a driver for MOSFET, op-amp etc., to avoid the malfunction and to ensure proper start-up of the slower regulator. Also, with the presence of an input capacitor between the positive and negative rail, it is needed prevent the charging of the capacitor in the negative direction. Both of these issues can be solved by placing a diode clamp across the negative output, as shown in Figure 6:

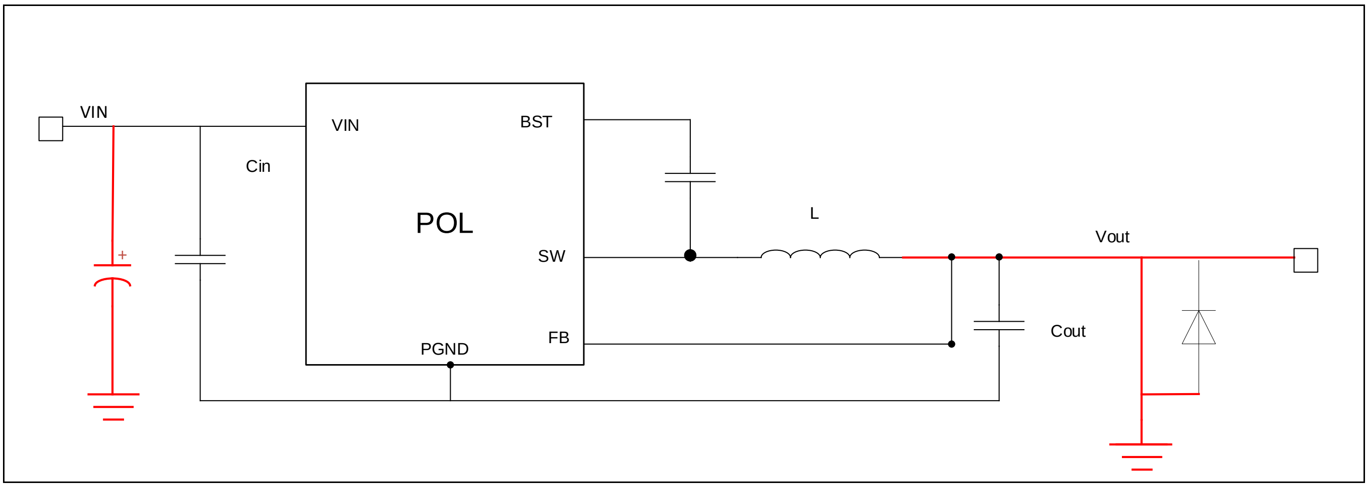

Figure 6 Output clamp requirement of the converter

4.4 Enable level input shift

If the system is required to control the enable function of the inverting buck-boost, a simple level shifter is required. Two possible circuits are shown in Figure 7.

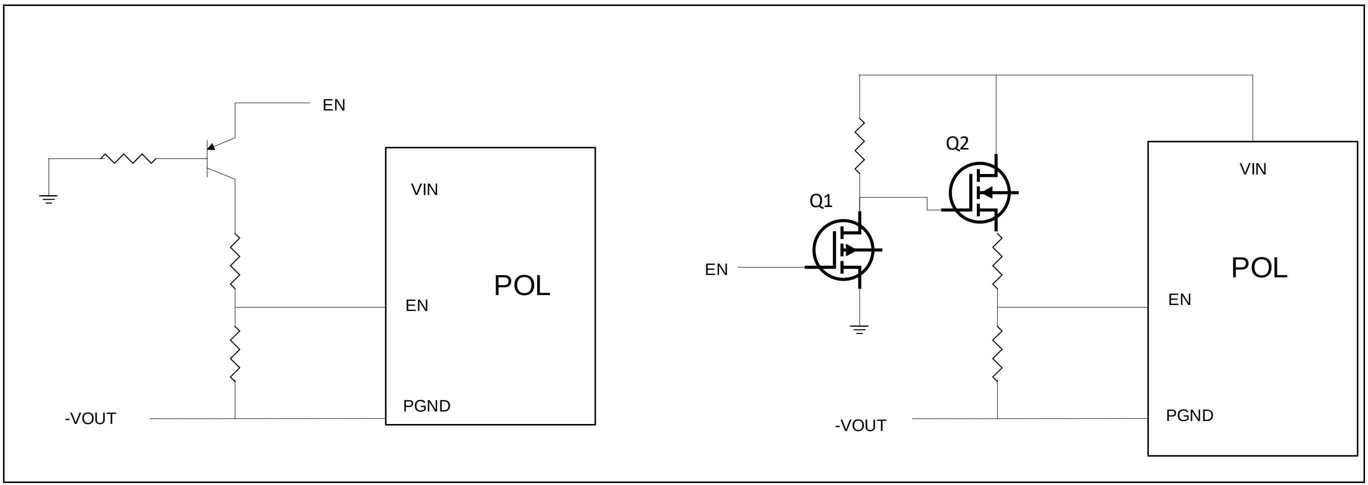

Figure 7 Level shifter circuit for enable signal

The circuit on the left has a large hysteresis in the threshold and does not consume any amount of current from the control logic. However, it requires only one transistor. The circuit on the right has no hysteresis and requires no current from the logic, but requires two transistors. In any case, the enable input of the buck can withstand the full input voltage rating of the regulator (from the datasheet “Absolute Maximum Ratings” section). If not, then a Zener diode, rated below the maximum enable voltage limit, must be used as shown. Even if the system is not required to control the enable of the regulator, this input must still be terminated correctly to keep the regulator turned on. In some systems the user may wish to use the enable control as an input undervoltage lockout (UVLO) feature. The best way to do this would be to use one of the enable level shifters shown, with an external op-amp/ reference to provide the UVLO function.

4.5 P_{GOOD} level input shift

Many applications require a “power good” or “reset” flag from the buck regulator to alert the µC that the output voltage is within specification. The circuits shown below can be used to level shift the status flag to the system ground.

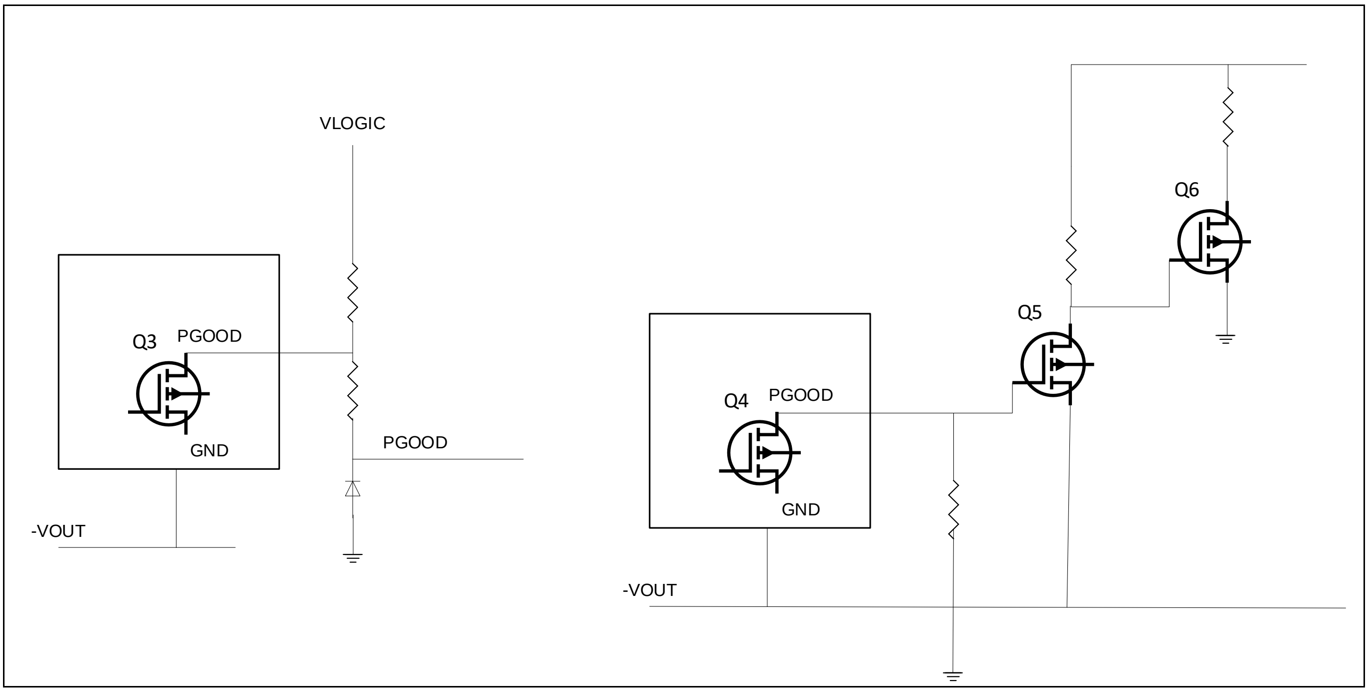

Figure 8 Level shifter circuit for P_{GOOD} signal

The circuit on the left is simple, but the P_{GOOD} signal swings below ground by a diode drop. The circuit on the right is slightly more complicated, giving a P_{GOOD} signal that swings to zero volts. In either case the PGOOD signal swings high to the user defined V_{LOGIC} level. Be sure to check the absolute maximum rating on the power good pin from the buck datasheet. For the circuit on the left, the power good pin must withstand $V_{LOGIC} + |V_{OUT}|$. For the other design the power good must withstand $|V_{OUT}|$.

5 Test results

5.1 Board features

V_{IN} = 5 V, V_{OUT} = -5 V, Fsw = 600 kHz, FCCM Mode, 0 to 5 A

L = 150 nH (12.4 mm x 8.3 mm x 8 mm, DCR = 0.15 mΩ)

C_{IN} = 10 x 22 µF (25 V, ceramic 0805)

New C_{IN}=2 x 22 µF (25 V, ceramic 0805)

C_{OUT} = 10 x 22 µF (6.3 V, ceramic 0805) + 4 x 47 µF (6.3 V, ceramic 0805) + 1 x 470 µF (2 V, 6 mΩ, SP-cap)

5.2 Schematic

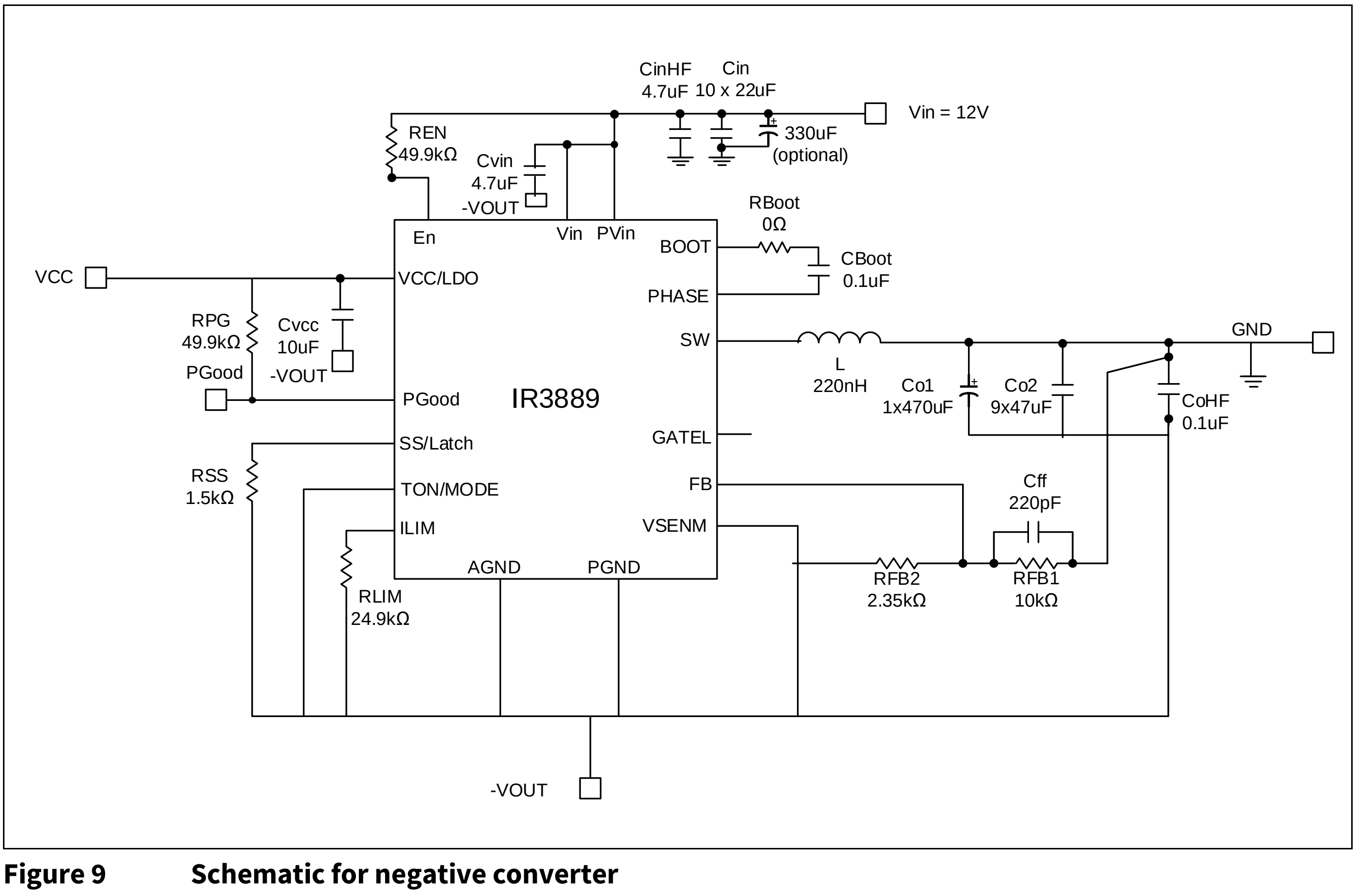

Figure 9 Schematic for negative converter

5.3 Efficiency

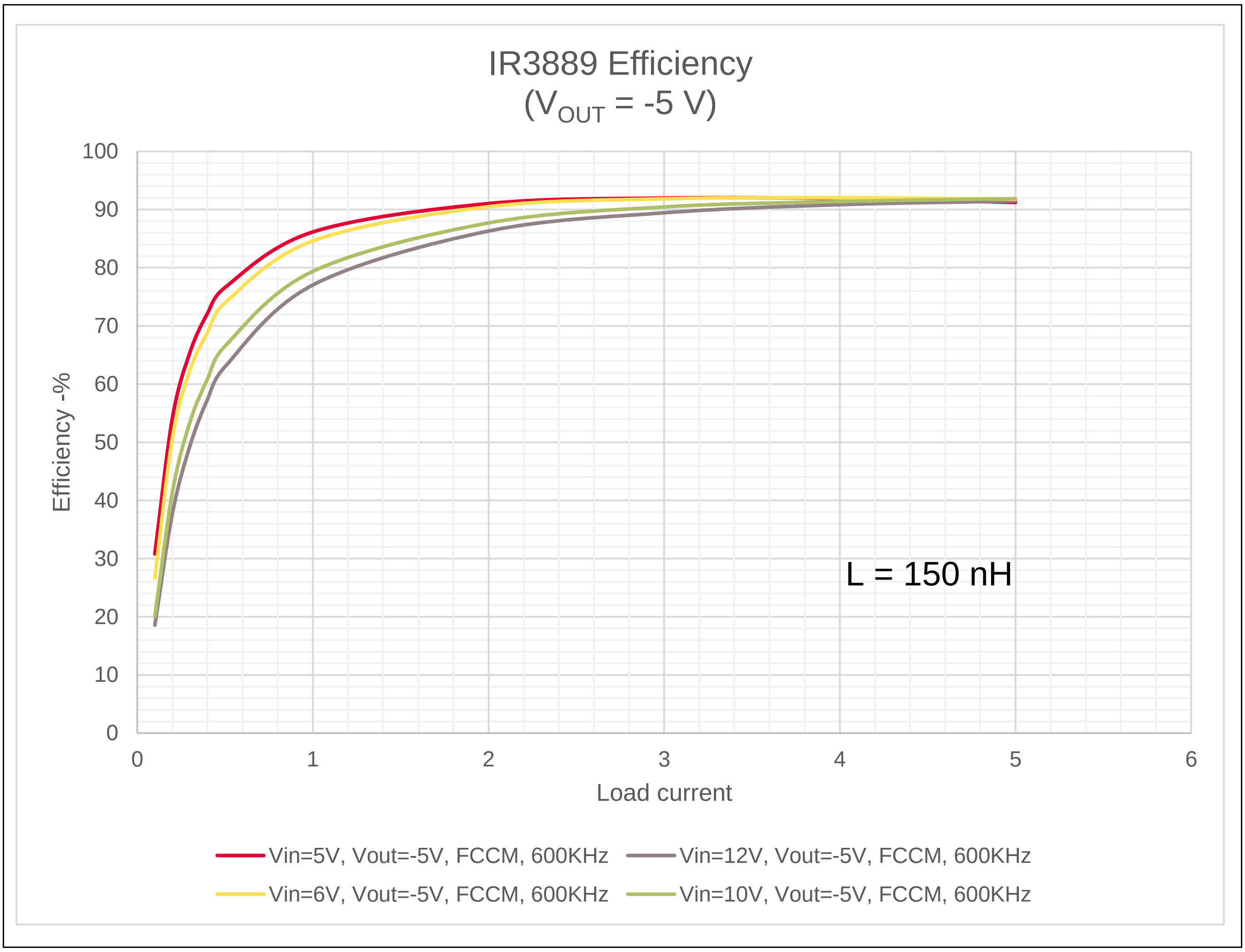

Figure 10 Efficiency for -5 V output for different conditions

5.4 Load regulation

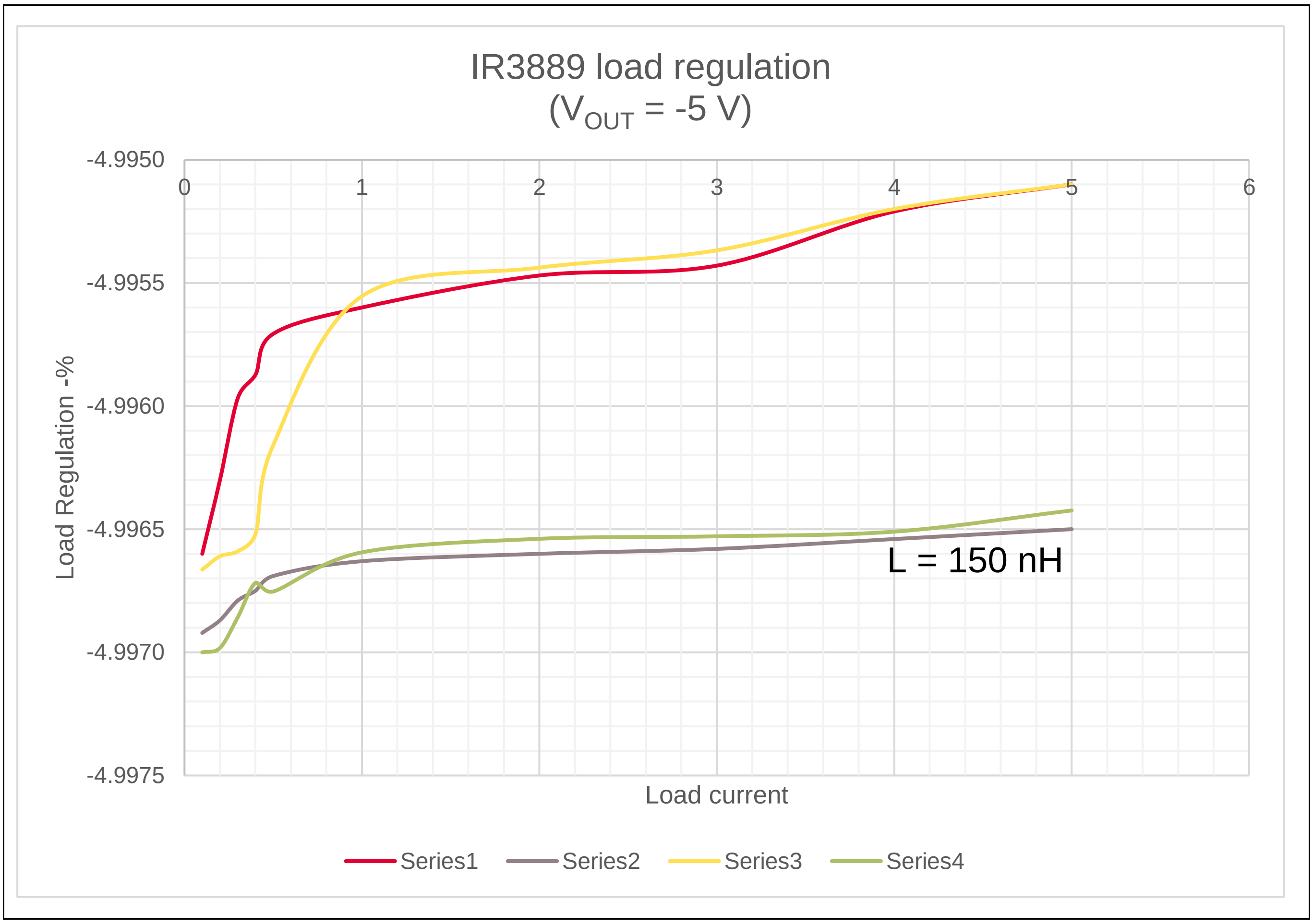

Figure 11 Load regulation for -5 V output

Series 1: Vin=5V, Vout=-5V, FCCM, 600KHz

Series 2: Vin=6V, Vout=-5V, FCCM, 600KHz

Series 3: Vin=10V, Vout=-5V, FCCM, 600KHz

Series 4: Vin=12V, Vout=-5V, FCCM, 600KHz

5.5 Start-up

V_{IN} = 10 V, V_{OUT} = -5 V, Fsw = 600 kHz, FCCM, 0 to 5 A

Oscilloscope:

Channel 1: output voltage

Channel 2: input voltage

Channel 3: load current of IR3889

From the **Figure 12** we can see the output voltage rising as the input rises to its set value.

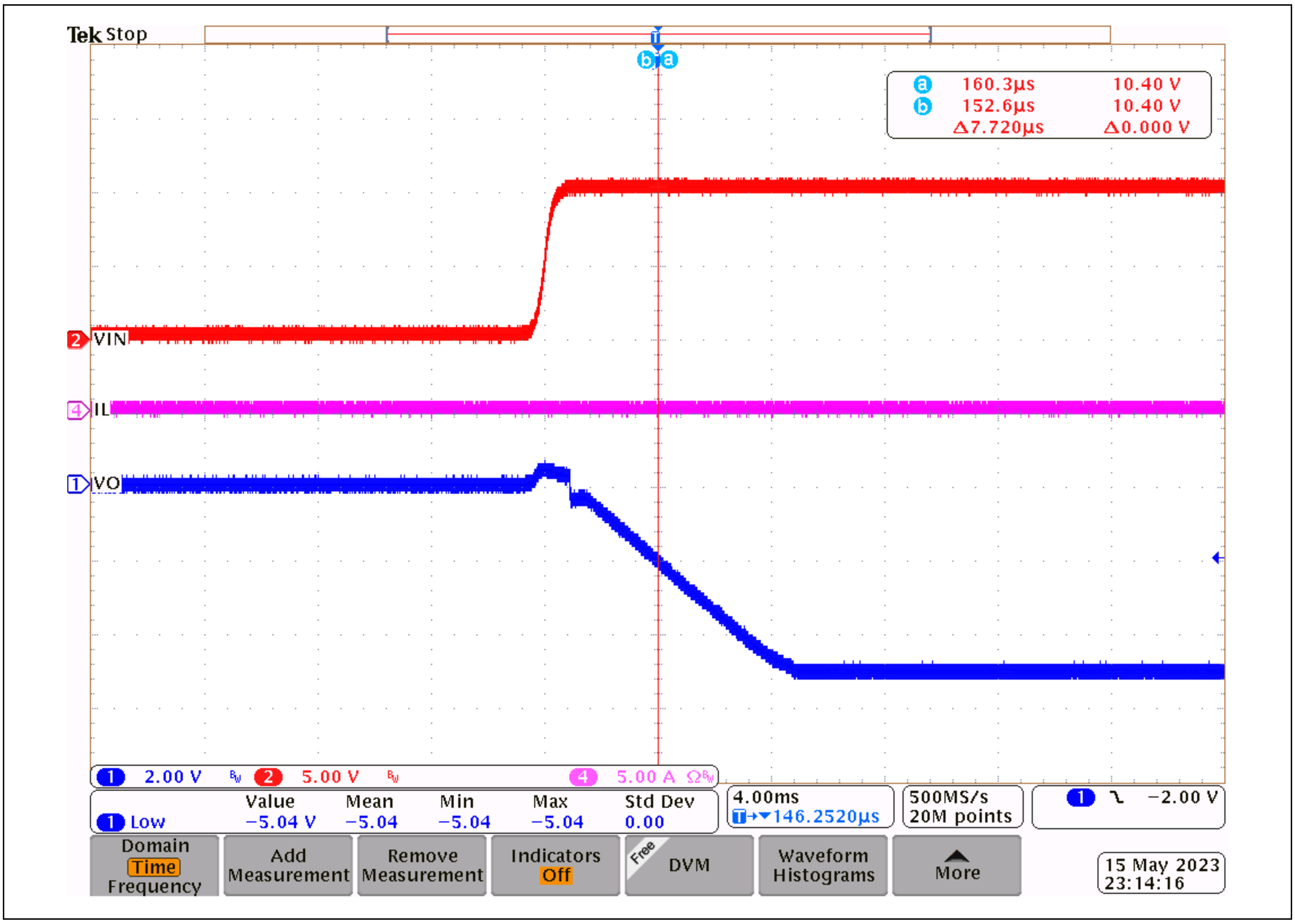

Figure 12 Start-up of IR3889 with proposed solution

5.6 Shutdown

Oscilloscope:

Channel 1: output voltage

Channel 2: input voltage

Channel 3: load current of IR3889

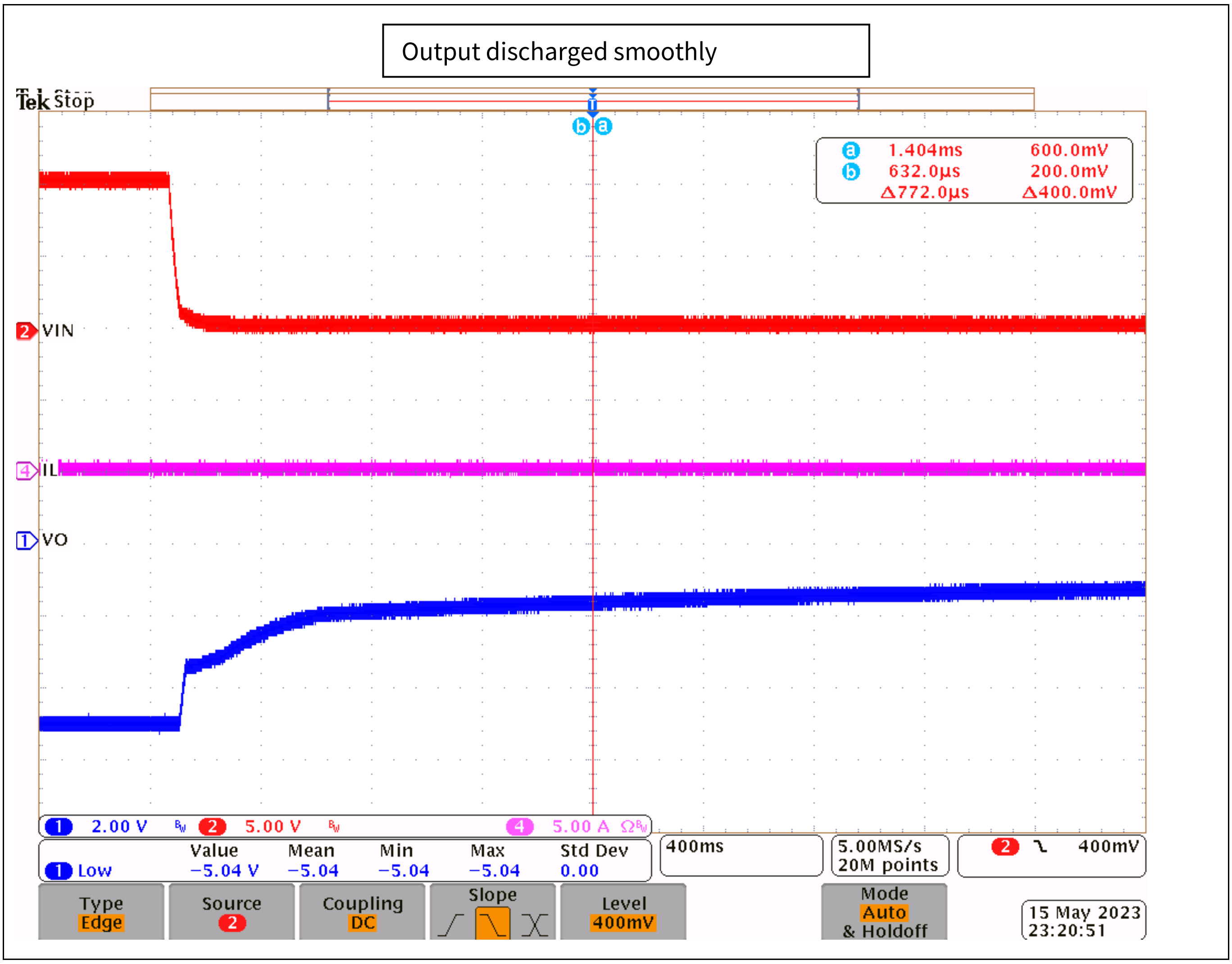

Figure 13 **Shutdown of IR3889**

The output discharge smoothly when the V_{IN} goes to 0 V when it is turned off.

5.7 Start-up with load

Oscilloscope:

Channel 1: output voltage

Channel 2: input voltage

Channel 3: load current of IR3889

An ERL of 5 A is connected across the V_{OUT} terminals, and we can see that the current also increases linearly (pink color) with an increase in the output voltage as expected.

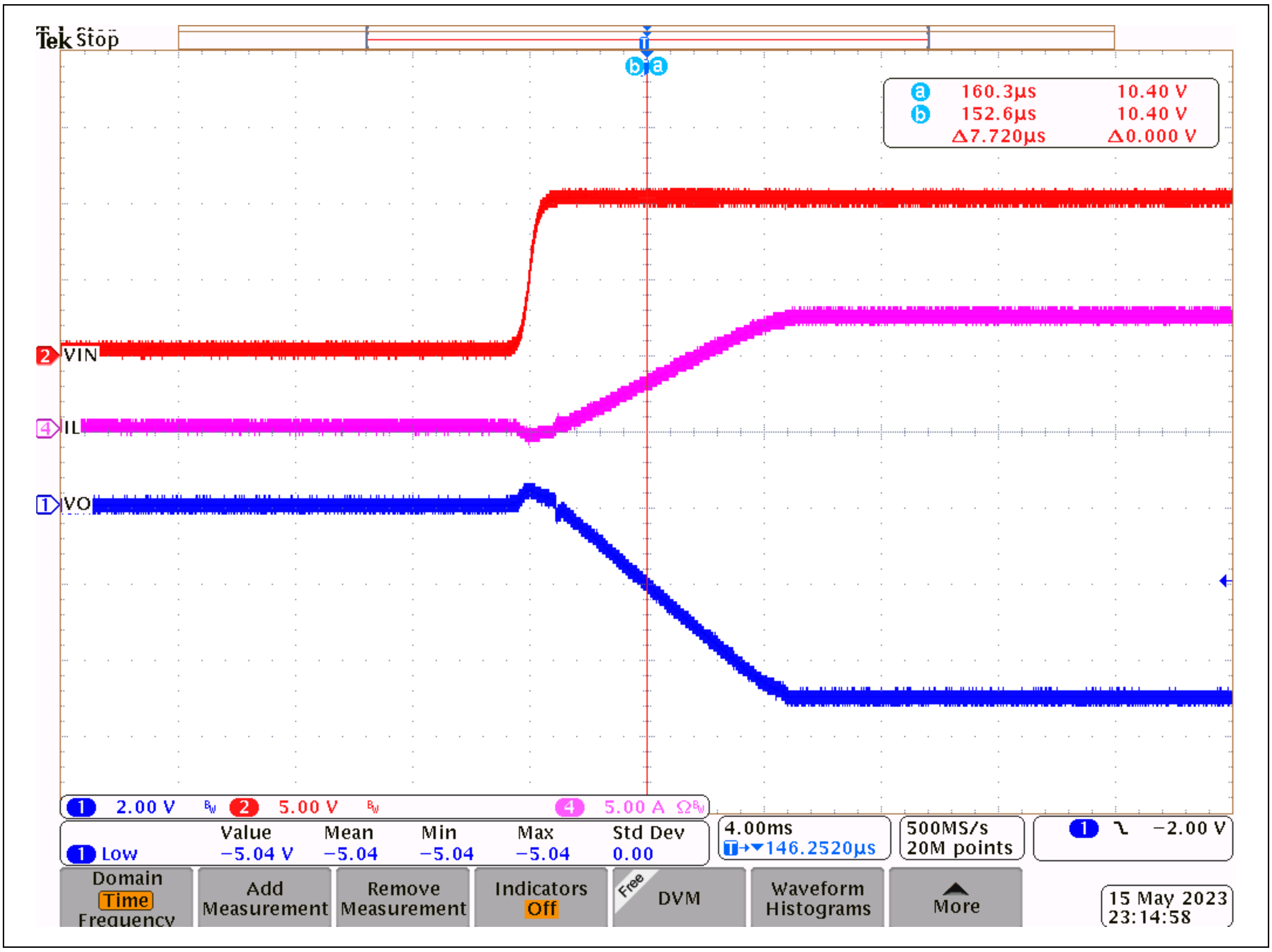

Figure 14 **Start-up with load**

5.8 Shutdown with load

Oscilloscope:

Channel 1: output voltage

Channel 2: input voltage

Channel 3: load current of IR3889

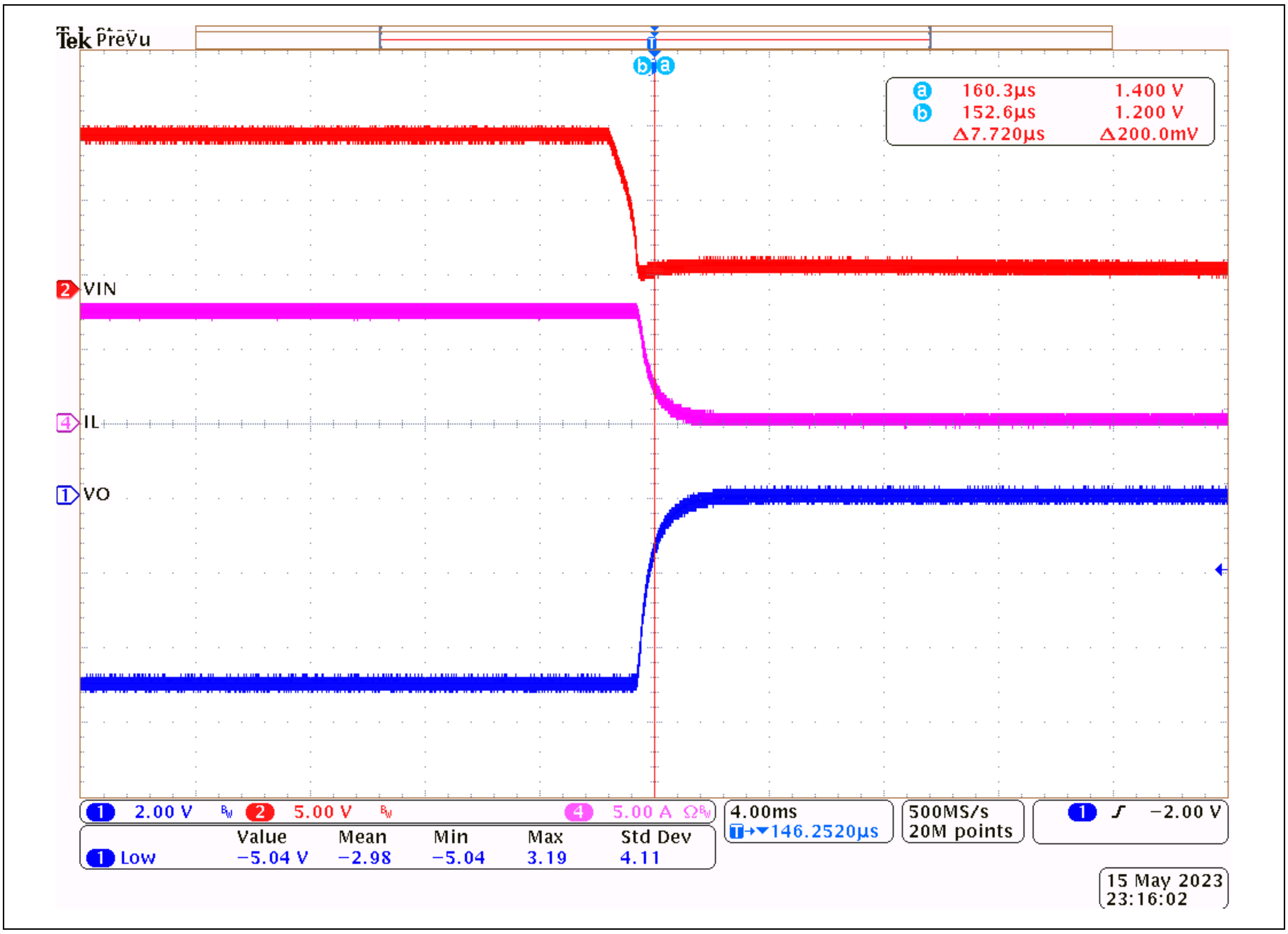

Figure 15 **Shutdown with load**

5.9 Transient test

Transient setup:

V_{IN} = 5 V, V_{OUT} = -5 V, Fsw = 600 kHz, 5A, FCCM, 0 to 0.5 A load, 2.5 A/µs

Oscilloscope:

Channel 1: control voltage of transient circuit

Channel 2: output voltage (AC mode)

Channel 4: load current

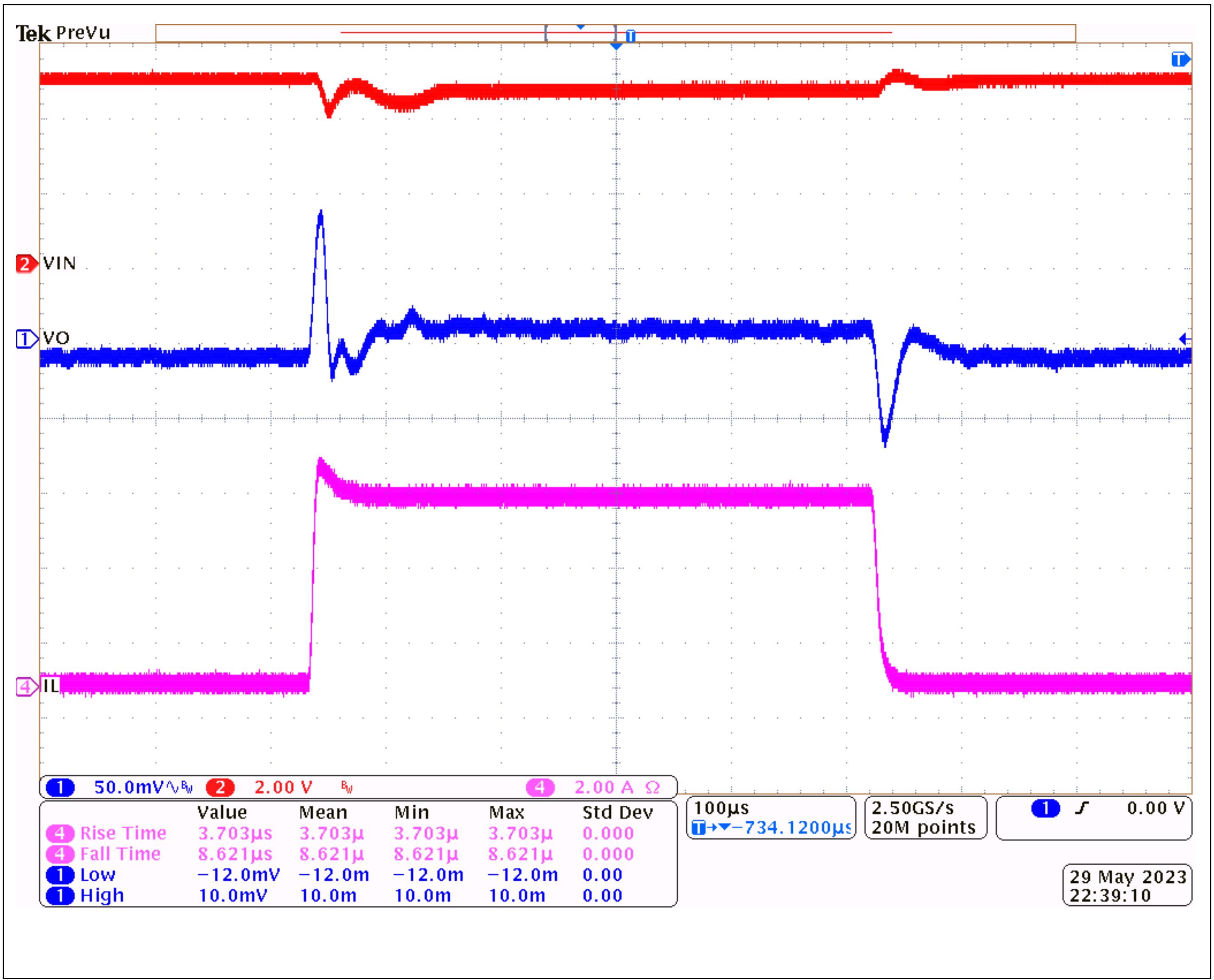

Figure 16 Transient behavior

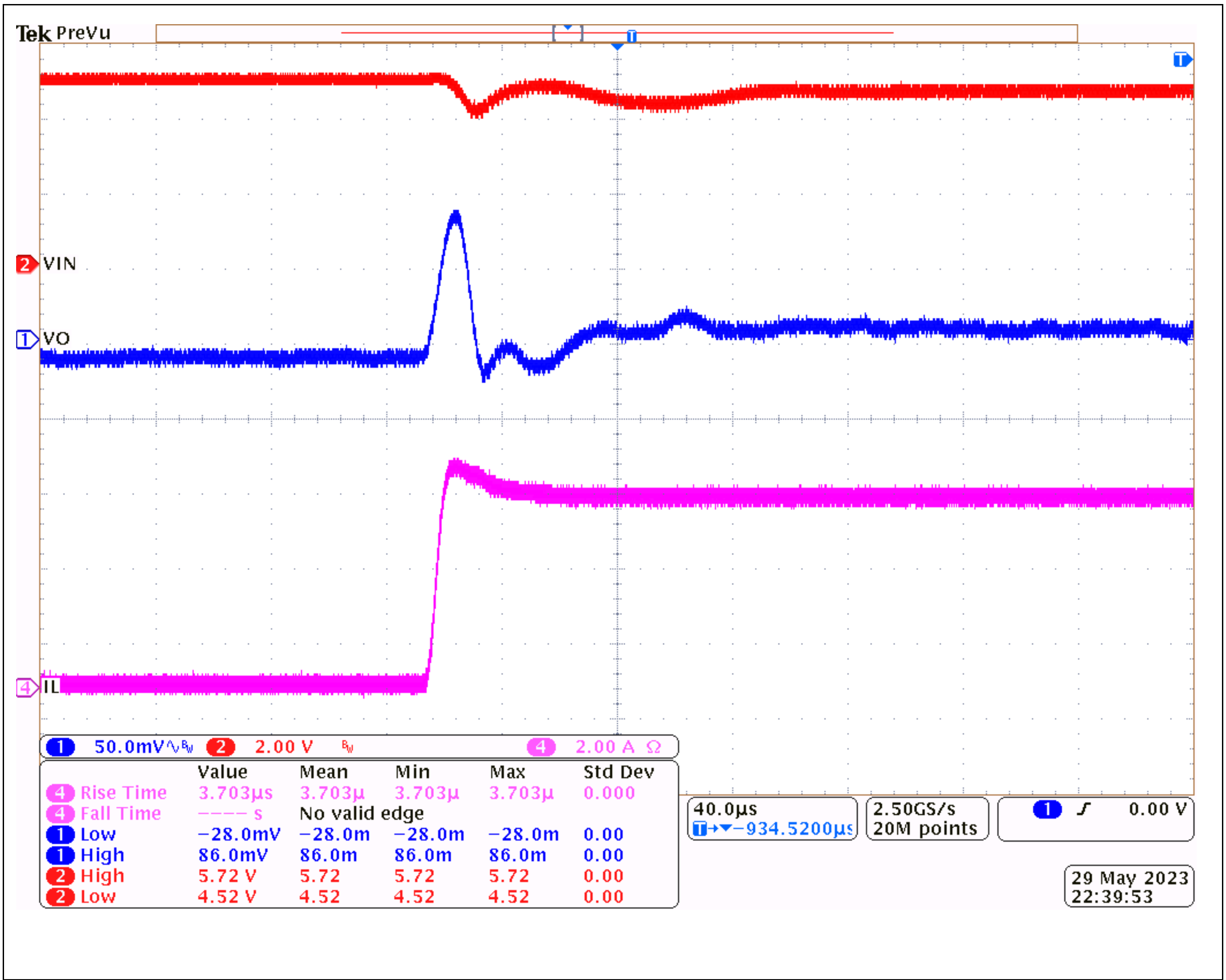

Figure 17 Transient start-up behavior

5.10 Transient shutdown

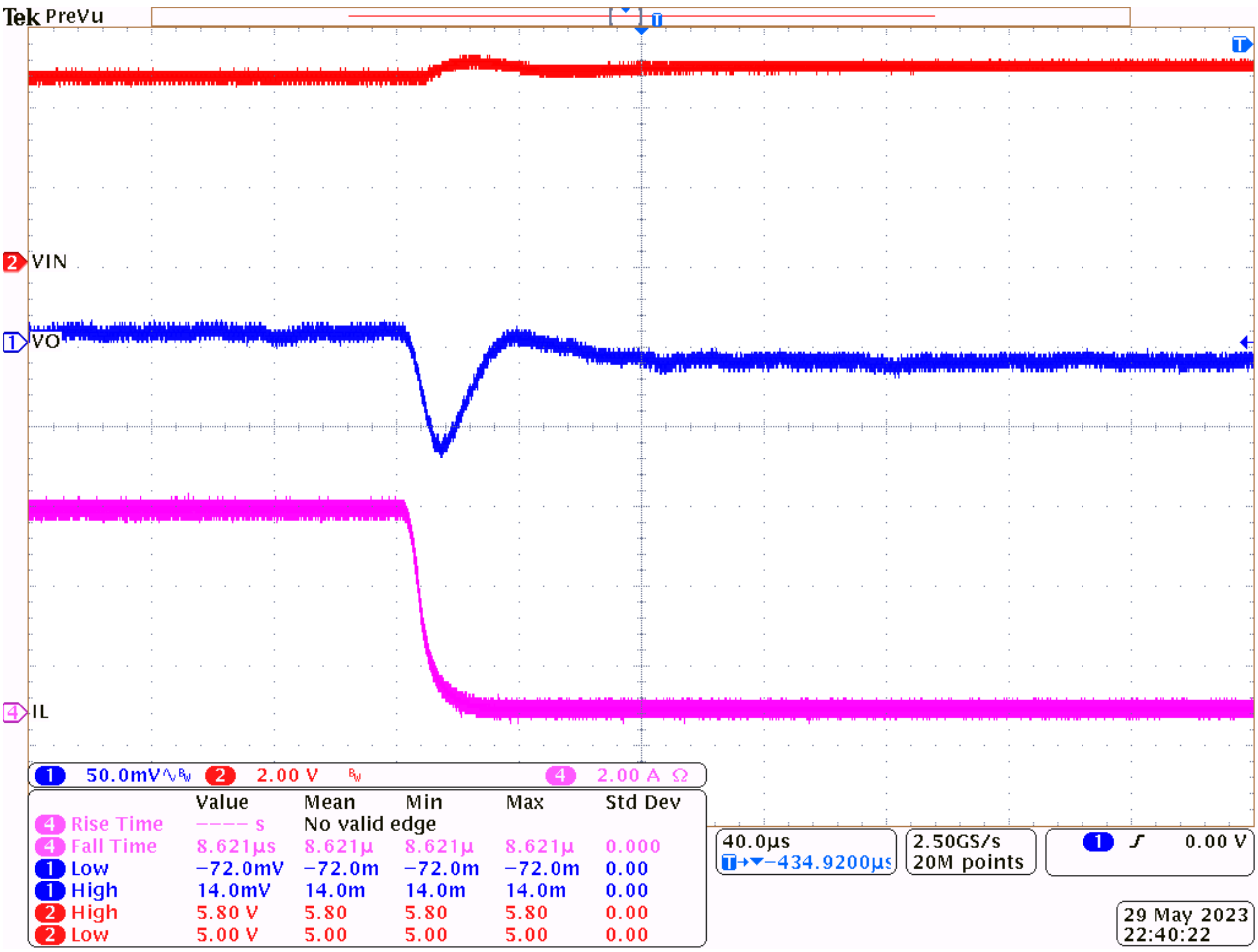

Figure 18 Transient shutdown behavior

5.11 Thermal behavior

V_{IN} = 10 V, V_{OUT} = -5 V, Fsw = 600 kHz, FCCM, 5 A load

The part is running continuously for the above conditions.
The ambient temperature is 23.8° C.
We can see SP1 marking which is the IC temperature 41.9° C.
SP2 is Inductor temperature at 81.2° C after achieving the steady state.

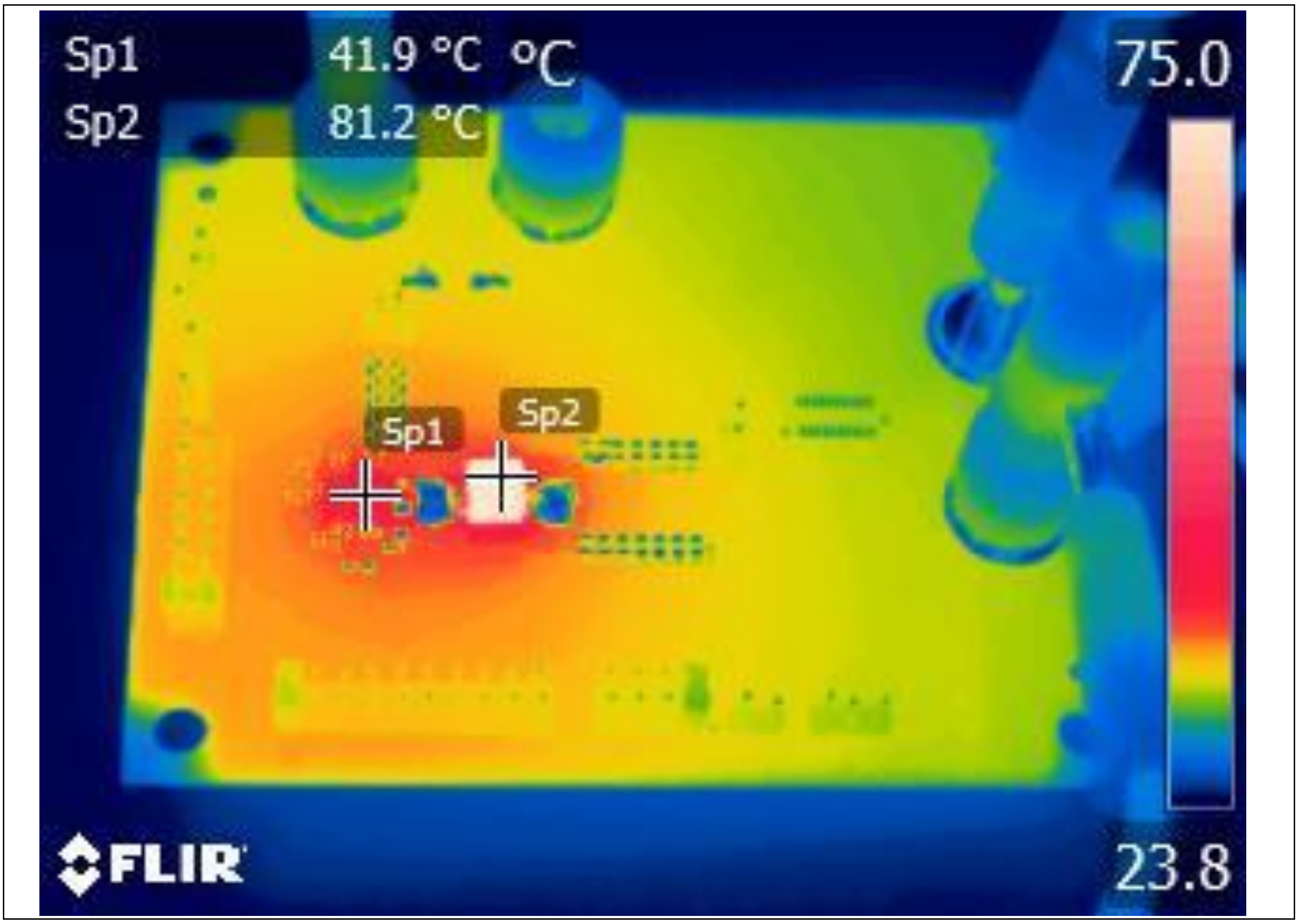

Figure 19 Thermal performance evaluation

Summary

The IR3889 offers an ideal way of creating a high-performance negative voltage output from a positive supply. If the designer follows the rules, a maximum input voltage of 12 V can supply a 5 V output, or a typical application with a 3.3 V output.

References

[1] Infineon Technologies AG: *Designing with the new fast COT for POL applications*; eLearning; **Available online**

[2] Infineon Technologies AG: *IR3889 OptiMOS™ IPOL*; Datasheet; **Available online**

Revision history

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