CoolSiC™ 1400 V Gen2 MOSFET in TO247-HC & Reflow package

About this document

Scope and purpose

SiC MOSFETs are becoming an attractive transistor for high-power applications. This application note introduces the Generation 2 CoolSiC™ 1400 V trench MOSFET in the TO247 packages in standard and reflow versions for industrial power applications. The purpose of this application note is to introduce and explain the features of the new family products. Important application topics are covered to help design the system for maximum performance and reliability.

Intended audience

The intended audience for this document are design engineers, power system developers, technicians or power electronics aficionados who would like to get more information about Infineon´s CoolSiC™ products.

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1 Introduction

The new generation of CoolSiC™ 1400 V Gen2 MOSFETs in the TO247 standard and reflow packages is a significant addition to the Infineon Industrial SiC MOSFET portfolio, offering the best-in-class switching performance, optimized for both liquid and air-cooling systems, robustness against parasitic turn-ons, as well as improved $R_{DS(on)}$ and $R_{th(j-c)}$. The features of these new devices address the requests and challenges of the Industrial application for which this product family was initially optimized. The following details are explained in the subsequent chapters:

- Specific requirements of the target application and how this new family addresses them
- Features of the higher blocking voltage device, including the device trade-off and parasitic turn-on robustness
- Advantages and special features of the packages
- Topics of device usage, such as gate driving or thermal management

1.1 Target applications

In any industrial-grade application, the efficiency and performance of SiC MOSFETs help in meeting high-power demand and ensuring reliability. Today's market trends indicate a growing demand for increased system-level power density and efficiency. However, these demands also bring new design challenges, such as managing thermal stress, ensuring robustness against transient overload, and optimizing system performance. With the fast evolution and growing penetration of multiple industrial applications, the parameters vary based on the application, and different topologies are used. Some of the following

General trends can be identified:

- Increasing power output
- Increasing power density
- DC bus voltage increases to 1250 V and higher
- Increasing robustness – PTO, cosmic radiation
- Lower thermal resistance

Following these trends and requirements, the package advancement is also needed to meet the application trends of drives, Solar, ESS, etc. This will enable flexible topologies like 2-level B6, 2-level Buck/ Boost, and 3-level ANPC/NPC1 using 1400 V SiC MOSFETs (Figure 1). On the other hand, the loop inductance (Lσ) in a system is ~50 nH and above in a fast switching condition (40 V/ns), 1200 V SiC discrete devices reach their limit, considering a 100 V buffer in the application. A higher breakdown voltage device, like 1400 V CoolSiC™, allows the customer to move to faster switching without violating design rules due to an 18 % buffer in voltage.

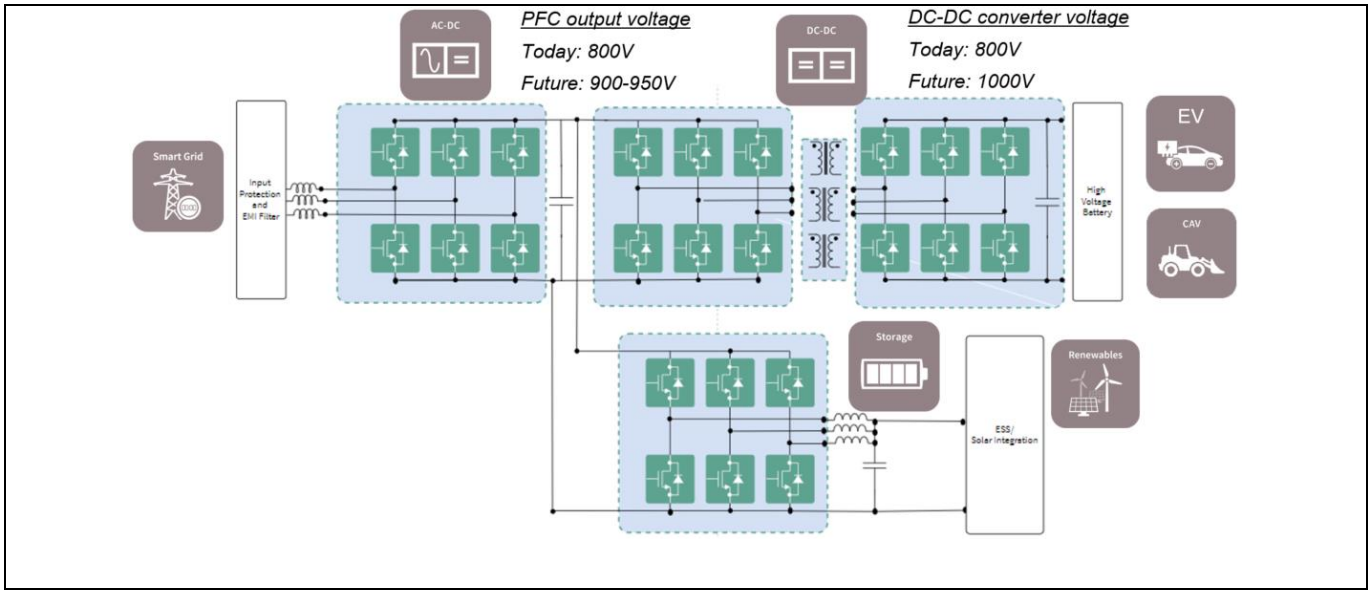


Figure 1 Illustration of various topologies that need a 1400 V device due to a higher DC bus

1.2 Technology features and benefits

The new higher blocking voltage discrete CoolSiC™ MOSFETs in the TO-247-4 pin package are based on the second generation (Gen2) of SiC MOSFET chip technology [1]. The new Gen2 SiC MOSFET family in the TO247-4 pin packages brings the following enhancements compared to the Gen1 family in the TO247-4 pin package:

- Compact optimized chip design with improved RDSon* area FOM
- Clear dv/dt and di/dt controllability
- Faster switching performance vs. CoolSiC™ G1, thus lower total switching losses E_{tot}
- Better reverse recovery performance than CoolSiC™ G1
- Best-in-class device capacitances and switching energy
- A combination of low C_{rss}/C_{iss} ratio and high $V_{GS(th)}$ helps avoid parasitic turn-ons
- Increased turn-on voltage (V_{GS} = 20 V) for lower $R_{DS(on)}$
- Advanced diffusion soldering (.XT technology) chip-mount technology for improved $R_{th(j-c)}$
- Lower package stray inductance for faster and cleaner switching
- Source sense (Kelvin) pin for better gate control and reduced switching losses
- Increased creepage distance to fit 1250 V DC applications without the need for coating
- Choice of $R_{DS(on)}$ options for an optimal fit for application requirements, including the only 6 mΩ device in the TO247-4 pin reflow package currently available on the market

These features provide the following benefits in the application:

- Smaller inductors and capacitors due to higher switching frequency
- Lower cooling effort and smaller heat sinks due to lower switching losses

Introduction

- Higher power density and lower system/assembly costs because of the reflow package
- Simplified unipolar gate driver enabled by 0 V turn-off with reduced driving power due to low QG

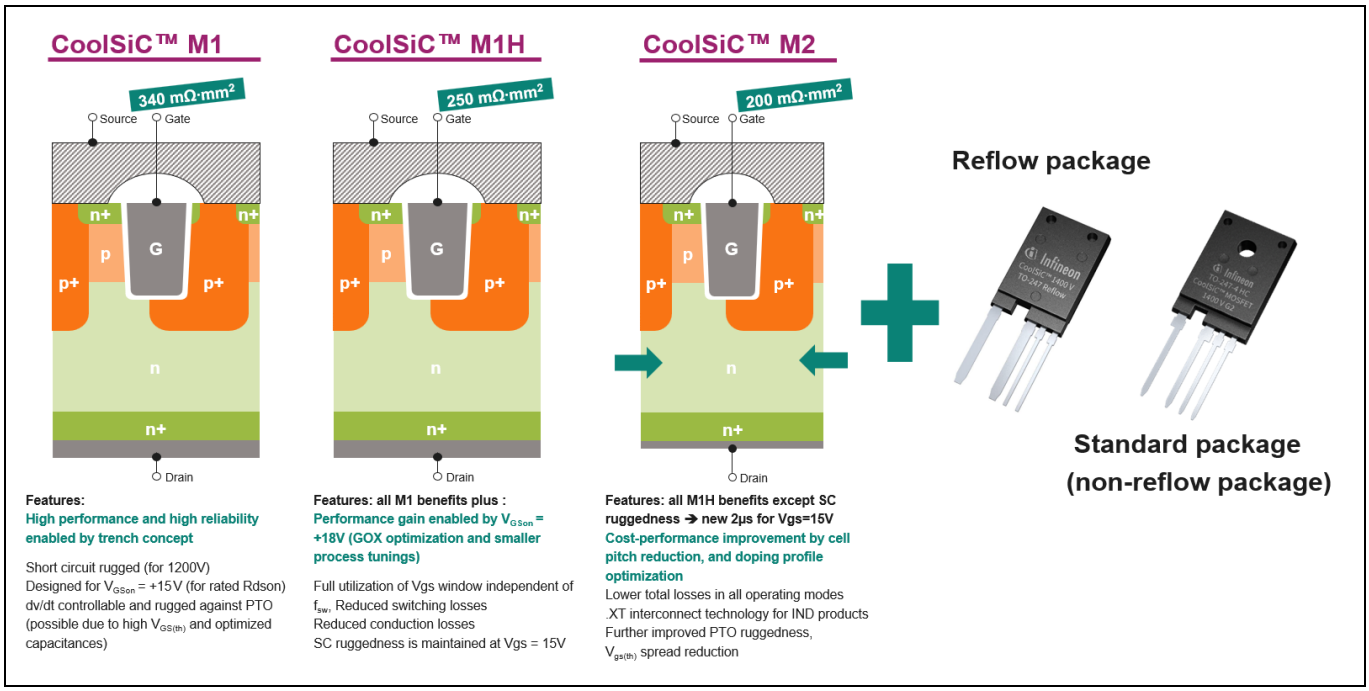


Figure 2 The technology evolution of CoolSiC™ from G1 to G2, in addition to the package advancement for high-power applications

High temperature operation, superior voltage handling, fast switching speeds, low on-state resistance, high thermal conductivity, avalanche, and short circuit capabilities enhance power conversion and make 1400 V Gen2 CoolSiC™ MOSFET a preferred choice for efficient and improved power conversion across diverse applications. **Error! Reference source not found.** shows the advancement in the technology between the two Infineon's CoolSiC™ generations and packages improvements for higher blocking voltage.

1.3 Portfolio

From the implemented technology improvements, the Gen2 family portfolio is expanded even further for the 1400 V-rated device family. The Gen2 1400 V Industrial qualified CoolSiC™ Mosfet consists of 11 devices with different Rdson ratings in two different TO-247 packages, including the only 6mΩ 1400 V device in a TO-247 package, as shown in Table 1. This choice ensures the optimal fit for any combination of conduction/switching losses in hard-switching and soft-switching applications. The key advantages of the higher blocking voltage are explained in Chapters 2, 3, and 4, followed by the package benefits discussed in Chapter 5.

Larger SiC MOSFET offers increased power handling, enabling higher power density in electronic systems. The ability to handle elevated power levels leads to reduced component count and compact system design as well as better thermal management. With potential for higher integration levels and support for high-voltage applications, these devices are crucial for applications prioritizing power density, efficiency, and space constraints.

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Table 1 CoolSiC™ 1400 V G2 MOSFET portfolio

$R_{DS(on)}$, typ 25°C [mΩ]	TO-247-4 Reflow (TO247-4-18)	TO-247-4 HC (TO247-4-17)
		
6	IMYR140R006M2H	
8	IMYR140R008M2H	
11	IMYR140R011M2H	IMZC140R011M2H
19	IMYR140R019M2H	IMZC140R019M2H
24	IMYR140R024M2H	IMZC140R024M2H
29	IMYR140R029M2H	IMZC140R029M2H
38		IMZC140R038M2H

In addition, Infineon's .XT technology addresses design challenges and enables smaller form factors with maintained thermal performance. The new Gen2 CoolSiC™ MOSFET with .XT, feature 10% better junction-to-case thermal resistance value due to improved die attachment process. As a result higher output currents and prolonged device lifespan can be facilitated. .XT technology employs minimizing solder voids, diffusion soldering, and reduced solder layer thickness [2].

2 Higher blocking voltage device

Economies of scale and advancements in system technology are contributing to a decrease in the levelized cost of energy (LCOE), which is leading to more stringent requirements within the industry. Furthermore, there is a significant transition in direct current (DC) system voltage from 1000 V to 1500 V across various applications, including photovoltaic systems (PV), energy storage systems (ESS), and electric vehicles (EV). This shift toward higher operational voltages has progressed from low-power classes to high-power converter systems. As a result, voltages ranging from 800 V to 1000 V, even for some applications to 1250 V, have now become the standard across different power classes for discrete devices.

The higher operational voltage of 1250 V necessitates a low failure rate due to cosmic radiation, while also demanding high system efficiency in power devices. Existing solutions for 1100 V systems utilizing single or parallel 1200 V discrete devices encounter several challenges. For instance, loop inductance (Lσ) is often quite high, typically greater than 50 nH. This high loop inductance can lead to significant voltage overshoots during switching, necessitating safety features such as overvoltage clamping or the need to reduce switching speed by employing a higher gate resistance (Rg), which can negatively impact system efficiency.

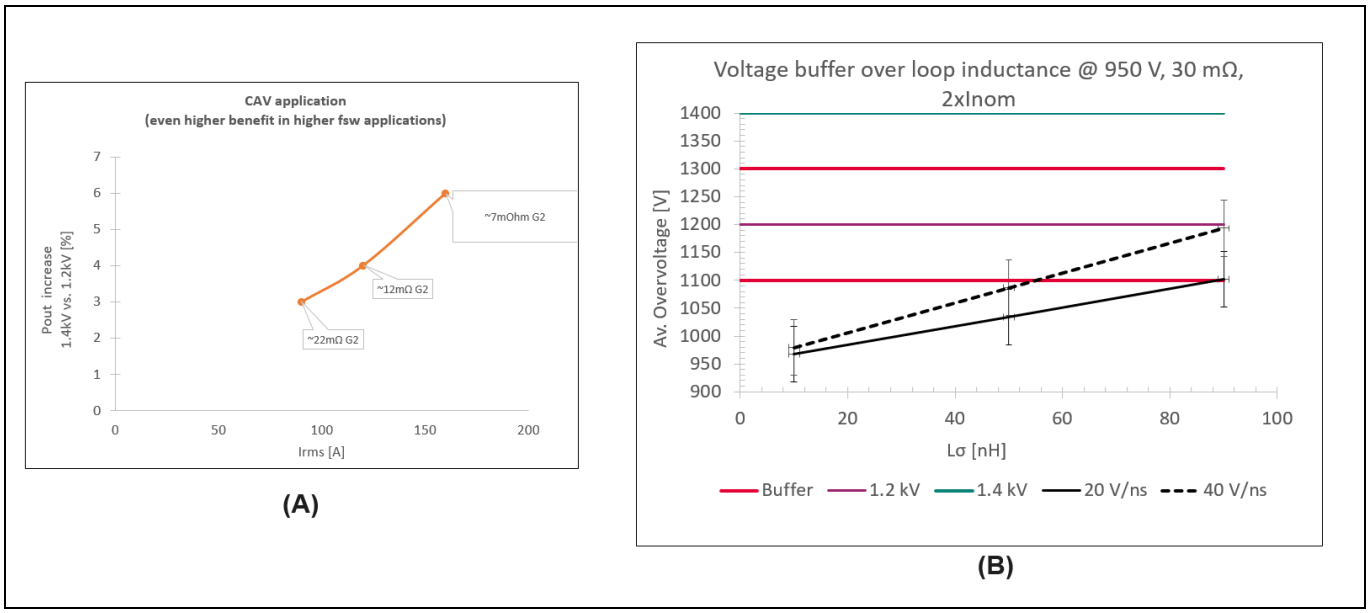


Figure 3 Value proposition of higher blocking voltage devices (A) Higher output power with lower Rg (B) Higher voltage buffer for faster switching

An example of high blocking voltage devices that offer design flexibility and faster switching is illustrated in Figure 3. The new 1400 V CoolSiCTM from Infineon allows customers to adopt faster switching without breaching design guidelines, providing an 18% voltage buffer. Additionally, advancements in packaging help achieve higher power ratings while simultaneously increasing the power density of the system.

In addition, 1400 V CoolSiC™ shows higher losses at 20 V/ns turn off, but slightly better / similar losses as 1200 V when increasing switching speed to ~ 40 V/ns turn off. 1200 V cannot be used at a higher switching speed, as the voltage limit is reached at 20 V/ns already, as shown in Figure 4. Higher blocking voltage device also enables customers to move to a faster switching set up, reaching similar efficiency levels as 1200 V with 25 % higher $R_{DS(on)}$

Higher blocking voltage device

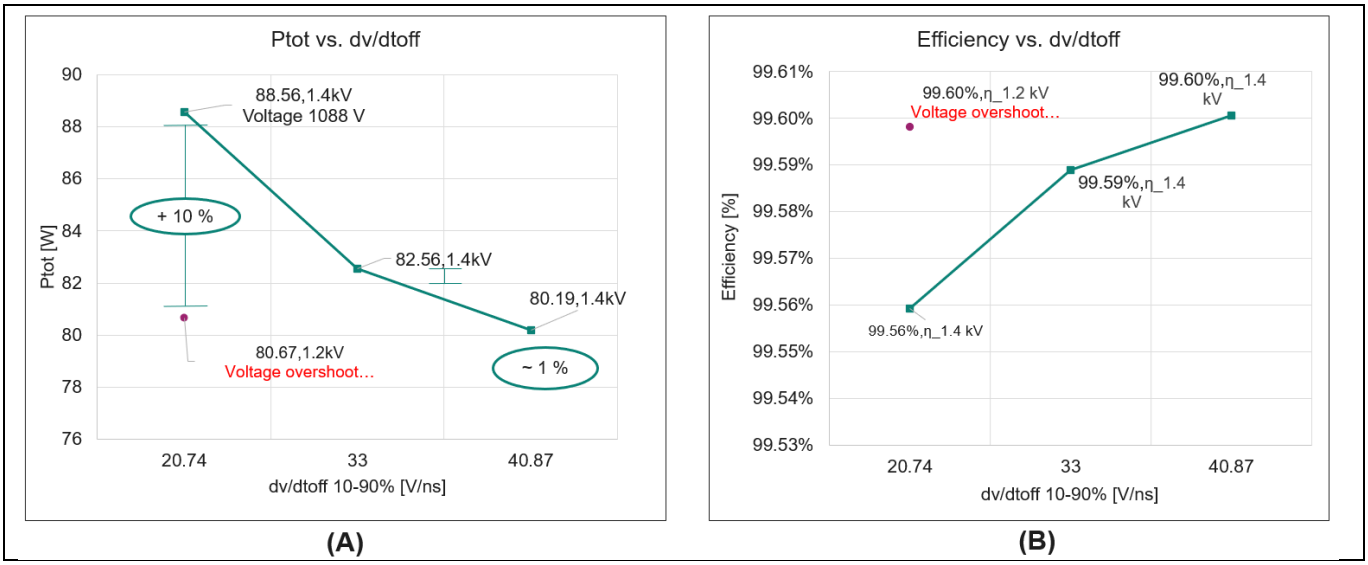


Figure 4 Value proposition of higher blocking voltage device (A) Higher switching speed vs low losses (B) Higher switching speed vs efficiency

The industrial sector is increasingly driven by demand for improved performance, including higher reliability and a preference for smaller packages featuring discrete components with higher current and voltage ratings, while maintaining best-in-class robustness. Silicon carbide (SiC) MOSFETs stand out for their ability to operate at much higher temperatures than traditional silicon-based MOSFETs. While specific temperature ratings may vary among different SiC MOSFET models and manufacturers, many are designed for reliable operation up to junction temperatures of 175 °C. Infineon's second-generation Gen2 CoolSiC™ MOSFET is even qualified for operation at 200 °C for a cumulative duration of up to 100 hours. This specification enhances reliability during overload conditions and provides engineers with greater flexibility in their system designs.

3 Technology parameters

This section describes the most important technology parameters and provides general guidance on the changes of FOM due to the higher blocking voltage implementations for the usage of CoolSiC™ 1400 V G2 MOSFETs. The comparison is represented for CoolSiC™ 1400 V G2 IMZC140R029M2H against CoolSiC™ 1200 V G2 IMZC120R026M2H, as both products represent a similar area. In addition, CoolSiC™ 1200 V G1 IMZA120R030M1H is also compared against G2 devices. For more details on the device nomenclature, see Infineon Power MOSFET product webpage.

As the blocking voltage capability of a silicon carbide (SiC) MOSFET increases, its internal structure and corresponding technology parameters must be significantly modified to sustain higher electric fields. These changes stem primarily from the scaling requirements of the drift region, which dominates the MOSFET's ability to withstand high voltages. Because SiC devices rely on their superior critical electric field strength, designers adjust multiple physical and electrical parameters to strike a balance between breakdown reliability, conduction loss, and switching performance.

One of the most important modifications is the increase in drift layer thickness. Higher-voltage devices require a thicker epitaxial layer so that the material can support larger electric fields without breaking down. However, to maintain safe field distribution, the doping concentration of this drift region must be reduced. Lower doping decreases the peak electric field but increases the resistivity, directly contributing to higher on-state resistance. These two adjustments—greater thickness and lower doping—form the fundamental trade-off in high-voltage SiC MOSFET design.

In addition to drift-layer scaling, the MOSFET's cell structure must also adapt. Higher blocking voltages demand wider cell pitches to ensure uniform electric field distribution around trench gates. This reduces the number of cells per unit area, increasing channel resistance and limiting current density. The gate oxide thickness typically increases slightly as well, helping to improve long-term reliability under high fields. More sophisticated field-management structures, such as field plates, guard rings, and advanced junction termination extensions, become necessary to shape the electric field at the chip periphery. As voltage ratings rise, these termination structures occupy a larger portion of the die area, especially for 1200 V and 1700 V devices.

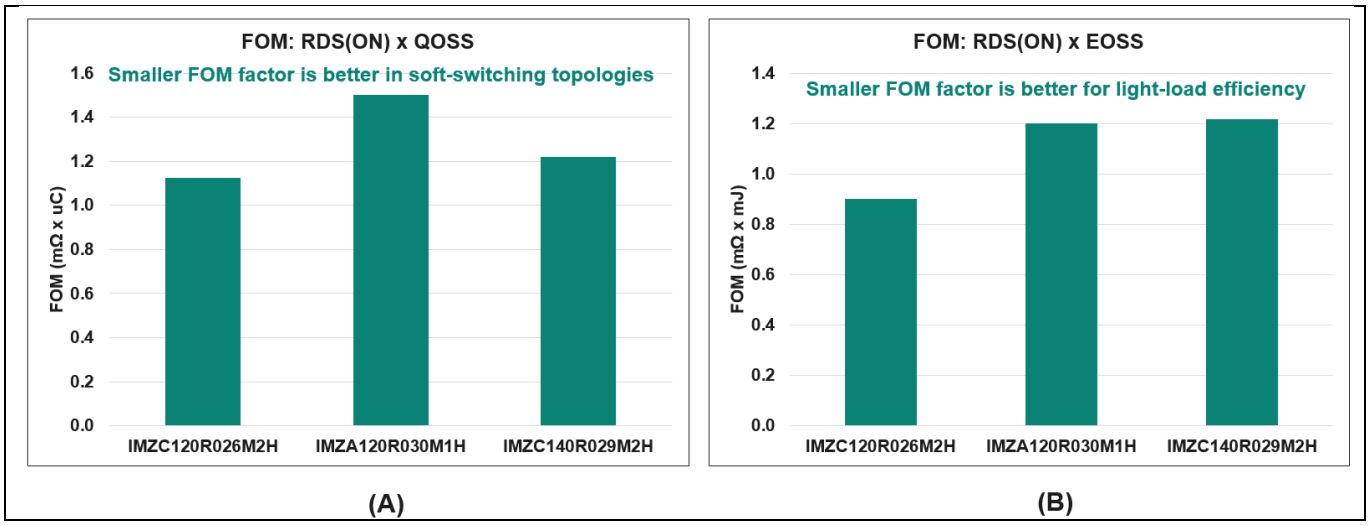


Figure 5 Figure of Merits (A)on-resistance*output charge (B) on-resistance*output capacitance

These structural changes have direct consequences for the electrical parameters of the device. The most noticeable impact is an increase in on-state resistance, which rises because both the drift and channel resistances grow with voltage. Conversely, important parasitic capacitances—particularly output capacitance

(C_{oss}) and reverse transfer capacitance (C_{rss})—tend to decrease due to the thicker and more lightly doped drift region [3]. Gate charge may increase slightly, however, due to the larger device area and wider cell structures as shown in Figure 6.

Another parameter influenced by voltage scaling is avalanche capability. Higher-voltage devices often show improved avalanche ruggedness because of their stronger termination structures and more controlled field profiles. Yet, the thicker epitaxial region and larger chip area can also result in a slight increase in thermal resistance, influencing heat dissipation during high-power operation.

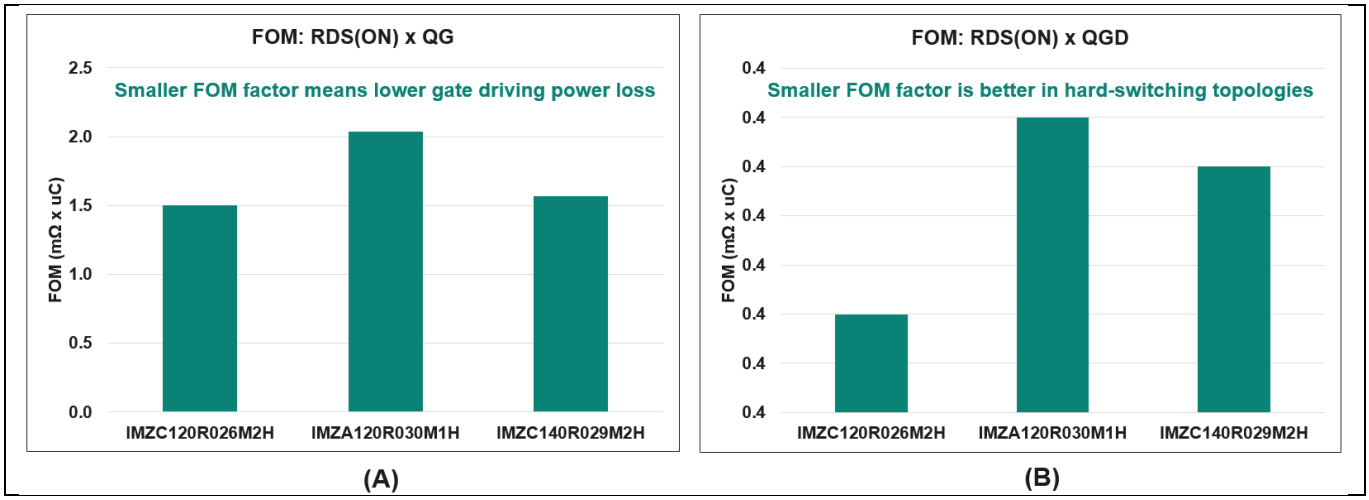


Figure 6 Figure of Merits (A)on-resistance*gate charge (B) on-resistance*gate-drain charge

Higher blocking-voltage SiC MOSFETs offer clear advantages in terms of voltage robustness, making them better suited for applications requiring higher DC bus voltages, greater surge tolerance, and improved avalanche capability. Their thicker and more lightly doped drift region enhances reliability under high-stress operating conditions and allows designers to reduce the number of series-connected switches, thereby simplifying system architecture. However, this same structural modification leads to performance penalties, as reflected in the Figure 5 & Figure 6 FOM plots: higher blocking devices exhibit increased $R_{Ds(on)}$, larger Q_{OSS} and Q_{GD}, and higher E_{OSS}, all of which contribute to elevated conduction and switching losses. These increases result in reduced efficiency, slower switching behavior, and greater gate-drive power demand, especially in high-frequency applications. Consequently, while higher blocking SiC devices deliver superior voltage handling and robustness, they do so at the cost of greater dynamic and conduction losses.

3.1 On-state resistance for higher blocking voltage device

CoolSiC™ Gen2 MOSFETs have a slightly worse behavior than CoolSiC™ Gen1 MOSFETs; however, this little drawback can be completely ignored due to the reduced switching losses from CoolSiC™ Gen2 MOSFETs, allowing CoolSiC™ Gen2 MOSFETs to be still better in efficiency than CoolSiC™ Gen1 MOSFETs in the target applications (described in a later section of this document). Furthermore, this behavior is the result of a channel improvement. Therefore, the $R_{DS(on)}$ distribution is shifted to the drift region of the device, resulting in an increased process stability leading to a reduction of the required typical to maximum $R_{DS(on)}$ margin in the final datasheets for CoolSiC™ Gen2 MOSFETs.

In high-voltage devices, a higher Rdson is typically a consequence of design choices made to increase the blocking voltage, as described in Figure 7. While this higher on-resistance leads to increased conduction losses, it also provides several advantages: the device can safely block higher voltages, exhibits lower off-state leakage current, and demonstrates improved ruggedness and thermal stability under voltage surges. Essentially, the trade-off of higher Rdson is accepted in exchange for enhanced voltage-handling capability and robustness, which are critical in high-voltage power electronics applications.

Technology parameters

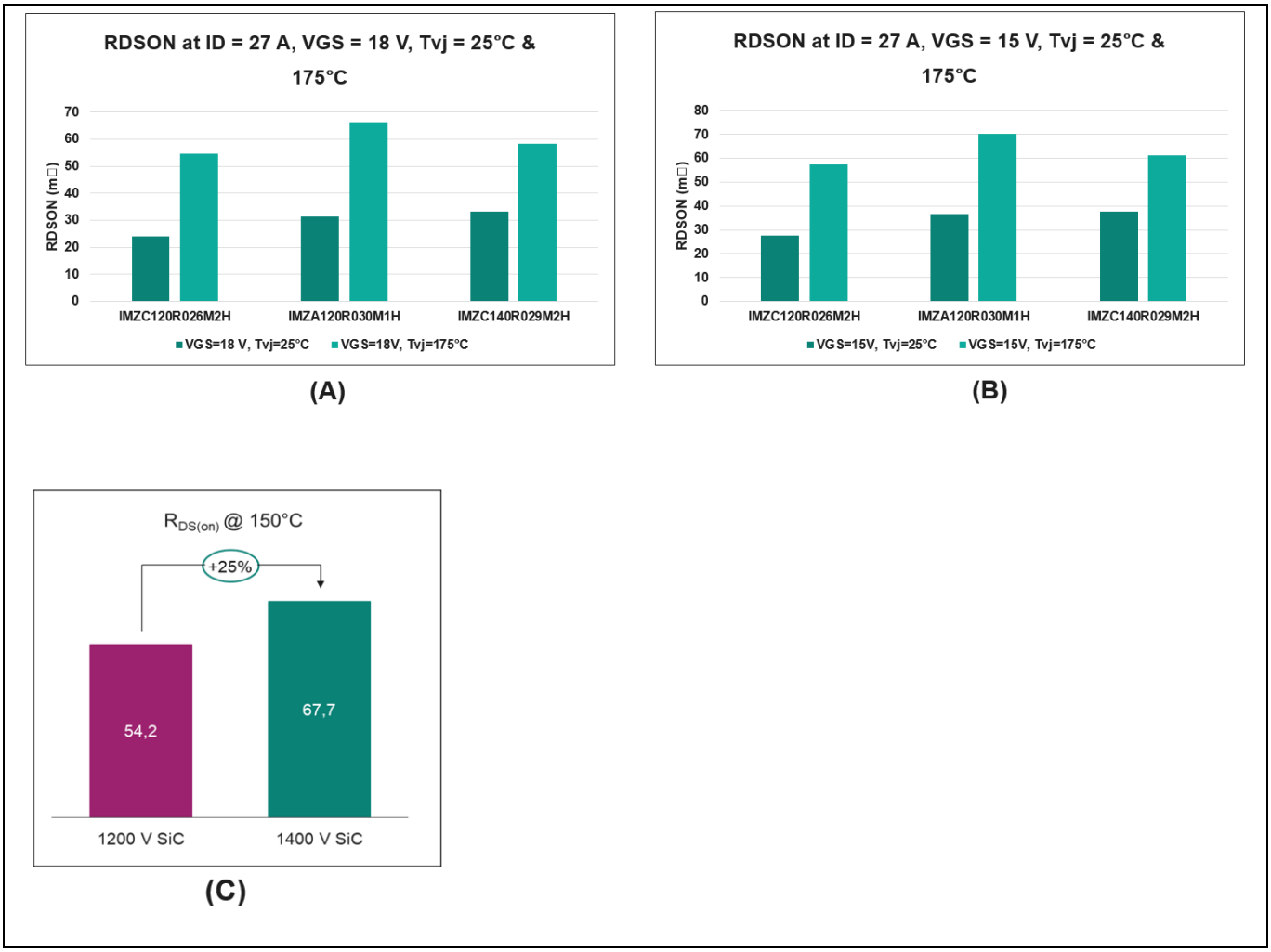


Figure 7 On-resistance comparison for Gen1 vs Gen2 (A)VGS =18 V (B) VGS = 15V (C) Rdson comparison for 1200 V vs 1400 V at 150°C

In summary, increasing the blocking voltage of a SiC MOSFET requires a coordinated modification of its drift region, cell structure, gate oxide, and termination design. These changes collectively improve breakdown strength and high-voltage robustness but come at the cost of higher conduction resistance, altered capacitances, and—often—a larger chip area. Understanding these trade-offs is essential for selecting or designing SiC MOSFETs optimized for applications such as grid-connected converters, industrial motor drives, and high-voltage DC systems.

4 CoolSiC™ switching behavior

Switching performance is one of the key optimization factors for 1400 V Gen2 technology. Due to the reduced chip area (for the same RDSon), the device capacitances reduced significantly as shown in Figure 8 for the 26 mΩ part vs 1400 V 29mΩ part. Both switch-on and switch-off energy values of a higher voltage device are compensated by reducing the Rg. This allows for a much higher switching frequency (and therefore smaller inductors) for the same switching losses, or much lower switching losses (and lower cooling effort) for the same switching frequency.

High-voltage devices are designed to withstand large voltages, which necessitates a thicker and lightly doped drift region . While this structure increases the device's robustness and allows it to safely block high voltages, it also comes with inherent drawbacks. The thicker region increases the $R_{DS(on)}$ and contributes to larger internal capacitances, C_{iss} and C_{oss}. These increased capacitances slow the charging and discharging process during switching events, leading to longer turn-on and turn-off times, as well as increased rise and fall times of current and voltage waveforms. Consequently, high-voltage devices inherently exhibit higher switching losses, as energy is dissipated over a longer transition period.

The same applies to the output capacitance C_{oss}, improved by 21% for 1200 V Gen2, and on the other hand, there is an improvement by a factor of 2 versus a 1200 V Gen 1 device. The 10% reduction in input capacitance C_{iss} means that less gate driving power is required to control the MOSFET, resulting in a cheaper gate driver and reduced driving losses. The reduced C_{rss} and C_{rss}/C_{iss} ratio help against parasitic turn-ons by minimizing the parasitic transients on the gate caused by high output dv/dt (more details on this topic are discussed in Chapter 4.2).

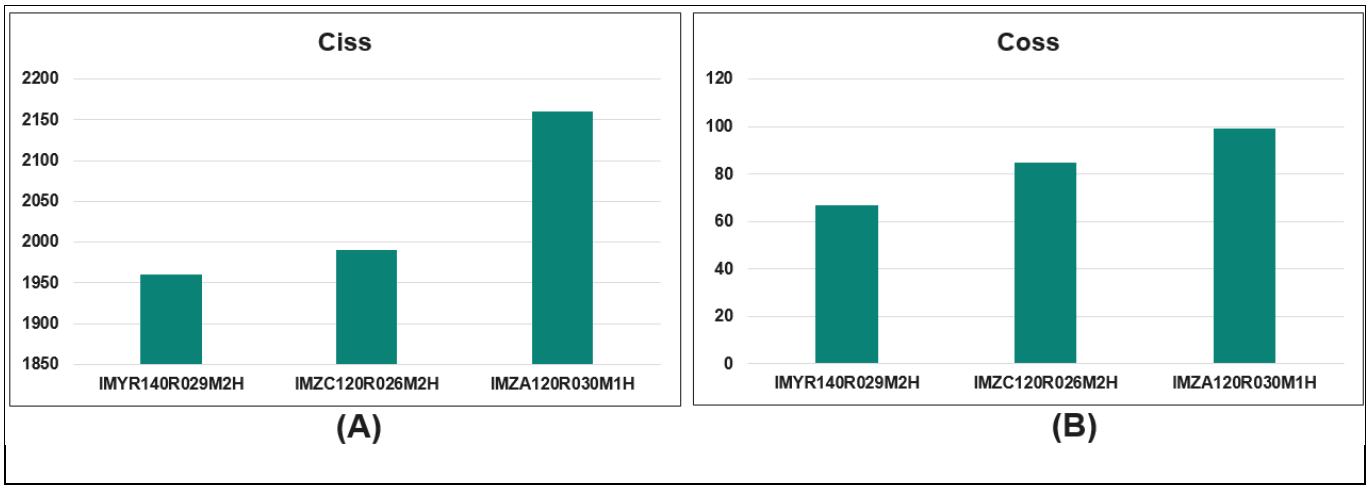


Figure 8 Improvements in switching parameter (A) Input capacitance (B) Output capacitance

One of the fundamental design considerations for these devices is their blocking voltage, which defines the maximum voltage the device can withstand in the off-state without breakdown. However, increasing the blocking voltage of a device introduces significant implications for its switching performance, affecting parameters like turn-on time, turn-off time, rise and fall times, and switching losses.

In contrast, low-voltage devices are optimized for speed. The drift region is much thinner, which reduces RDS(on) and internal capacitances. These devices require less gate charge (Qg) to switch fully, resulting in faster transitions, shorter rise and fall times, and lower switching losses. Additionally, they can tolerate higher dv/dt and di/dt rates, allowing for rapid switching in high-frequency applications. The trade-off, however, is their limited ability to block high voltages, making them unsuitable for high-voltage power systems.

The relationship between blocking voltage and switching parameters highlights an important design trade-off. While high-voltage devices are essential for applications requiring robust voltage handling, they must be

carefully managed to mitigate slower switching speeds and increased losses. Conversely, low-voltage devices are ideal for high-speed, high-frequency circuits but cannot be used in high-voltage environments. This interplay between voltage rating and switching performance dictates the choice of power devices for specific applications, balancing efficiency, robustness, and speed requirements.

4.1 Switching performance

In a half-bridge topology of 75 nH stray inductance, both devices - IMYR140R029M2H and IMZC120R026M2H are tested to perform the switching behavior. Different currents selected up to 2 x INOM under different gate voltages: 0 V and -5 V. The 1400 V device has more margin to switch with lower gate resistance, which results in lower power losses: Up to 60% @ turn-off and Up to 20% @ turn-on. As shown in Figure 9, the results show that the 1400-volt device has more margin compared to the 1200-volt device. This allows the 1400-volt device to operate with lower gate resistances, resulting in lower losses.

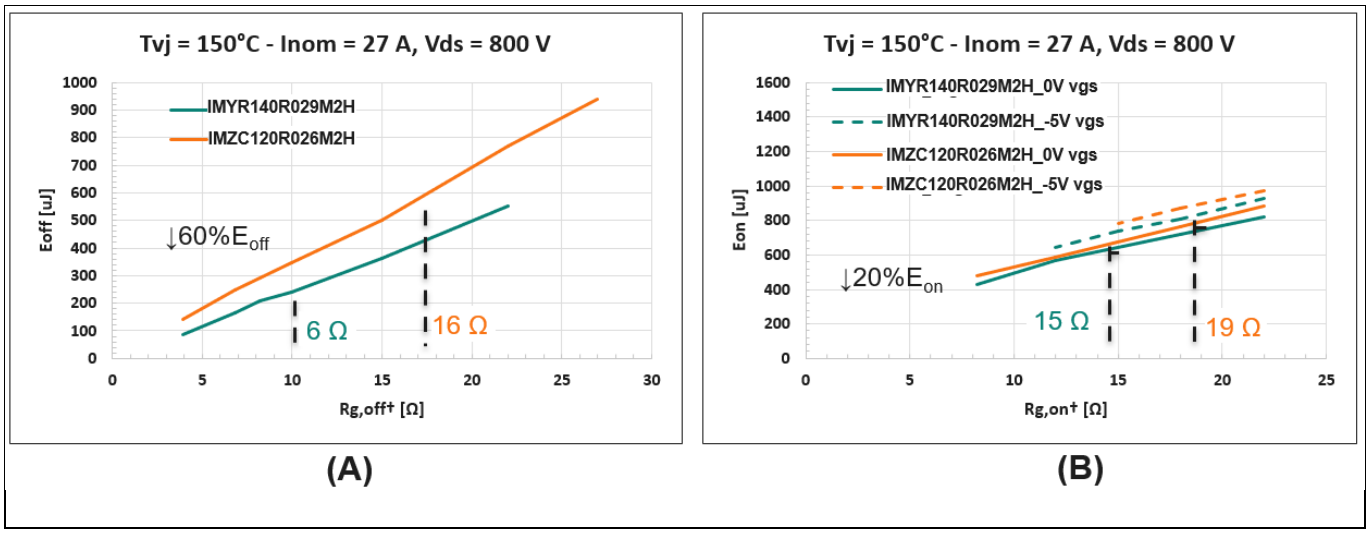


Figure 9 Switching losses vs Gate resistance (A) Turn-off losses (B) Turn-on losses

Figure 10 shows the overshoot behavior of the device. As explained before, the trade-off with higher blocking voltage generally results in higher losses, so it will affect the efficiency. On the other hand, as shown, the higher blocking voltage has a higher margin for overshoot, which allows the device to switch with lower Rg, resulting in faster switching as well as better efficiency of the system.

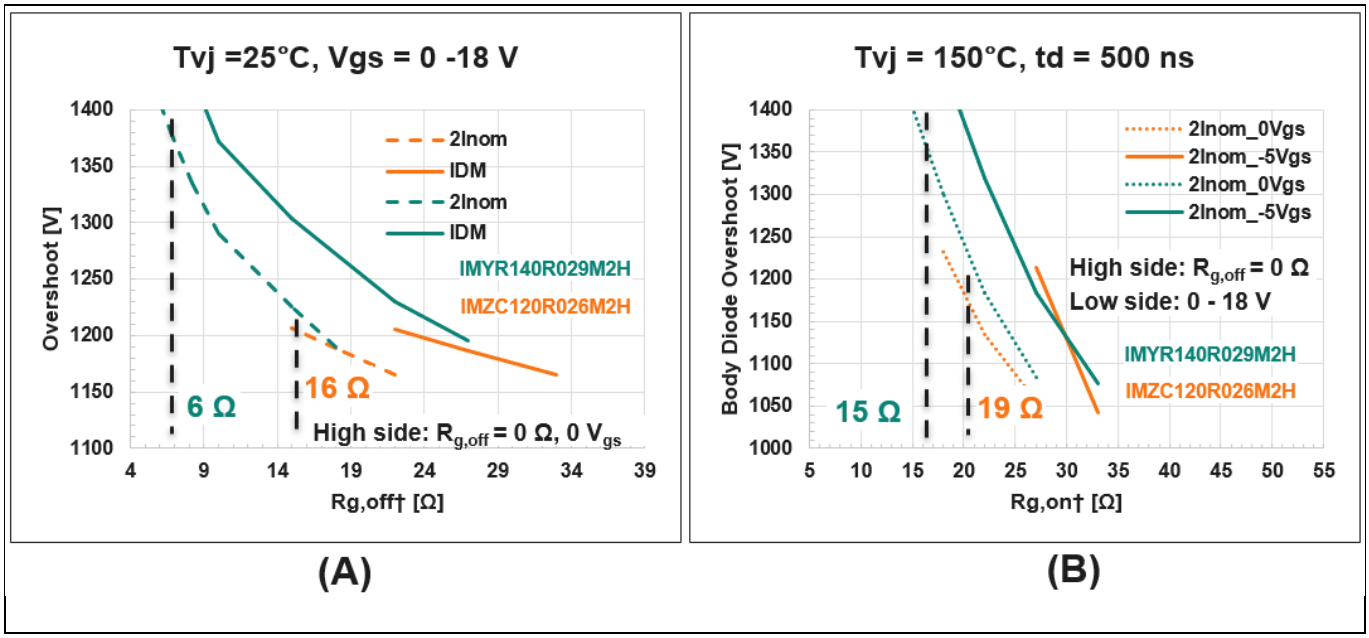


Figure 10 Overvoltage behaviour (A) overshoot vs Rgoff (B) Body diode overshoot vs Rgoff

4.2 Parasitic Turn-On

Parasitic turn-on is an unwanted phenomenon in power semiconductor devices—particularly fast-switching wide-bandgap devices such as SiC MOSFETs—where the OFF-state switch in a half-bridge unintentionally turns ON due to high dv/dt or induced gate voltage. This effect can lead to cross-conduction, excessive switching losses, overshoot, and potential device failure. controlling parasitic turn-on is critical for fast switching applications.

C_{iss}/C_{gd} ratio and $R_{g(off)}$ are major control parameters to prevent parasitic turn-on. A higher input capacitance ratio is favorable for reducing parasitic turn-on. C_{gd} is directly responsible for induced gate voltage spikes. As shown in Figure 11, the 1400 V SiC Gen2 devices have ~20% higher Ciss/Cgd compared to 1200 V devices. This indicates better dv/dt immunity for higher-voltage devices. As $R_{DS(on)}$ increases, the ratio remains relatively stable, suggesting consistent device design across the range.

To maintain the same dv/dt performance, higher-voltage devices require better gate control, often with slightly higher $R_{g(off)}$. As dv/dt increases to very high levels (>50–100 V/ns), both devices require minimal gate resistance to avoid excessive switching loss, and their behavior becomes similar.

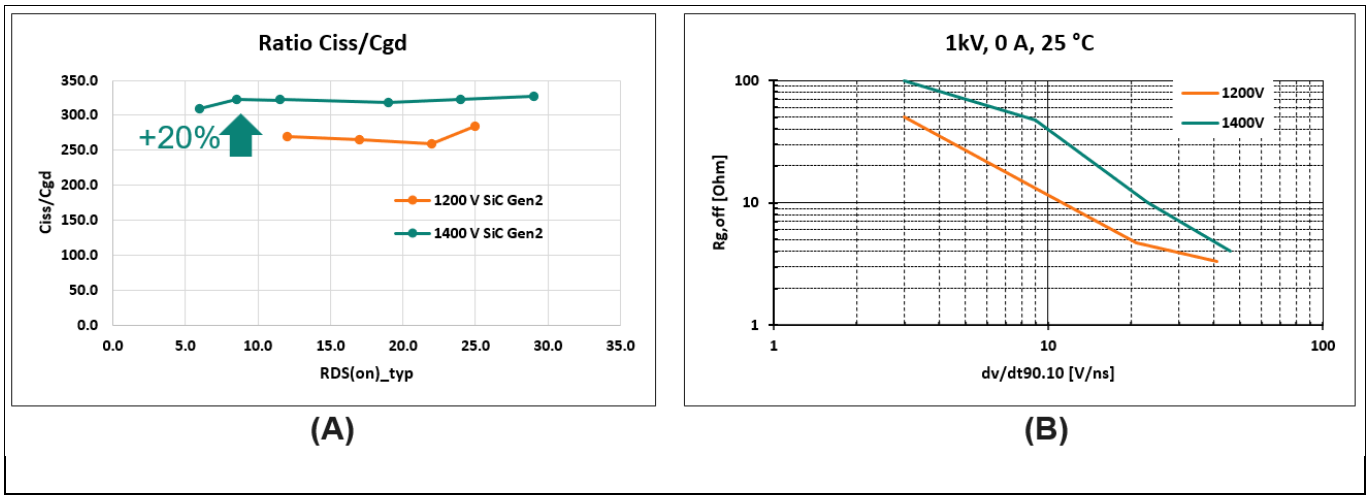


Figure 11 Parasitic Turn-on (A) input capacitance ratio (B) Rgoff vs dv/dt

A higher Ciss/Cgd ratio indicates improved immunity to unintended activation, and this is evident in the 1400 V Gen2 devices. However, controlled dv/dt using gate resistance remains essential, as shown in the Rg(off) vs dv/dt relationship. Understanding and balancing these factors is critical in designing reliable, high-performance SiC power converters, especially in high-voltage, high-frequency switching environments.

4.3 Choosing the right gate driving voltage for 1400 V CoolSiC™ MOSFET

CoolSiC™ MOSFETs from Infineon do not need negative gate drive voltage because the PTO factor is very low and show the best behavior with respect to re-turn-on on the market. However, due to second source possibility, CoolSiC™ Gen2 MOSFETs have an improved gate oxide allowing negative gate source voltage as the turn-off voltage. Because a lot of SiC MOSFETs on the market can only perform at VGS = –5 V, this new gate oxide is introduced. This results in an even easier-to-use and easier-to-drive CoolSiC™ Gen2 MOSFETs.

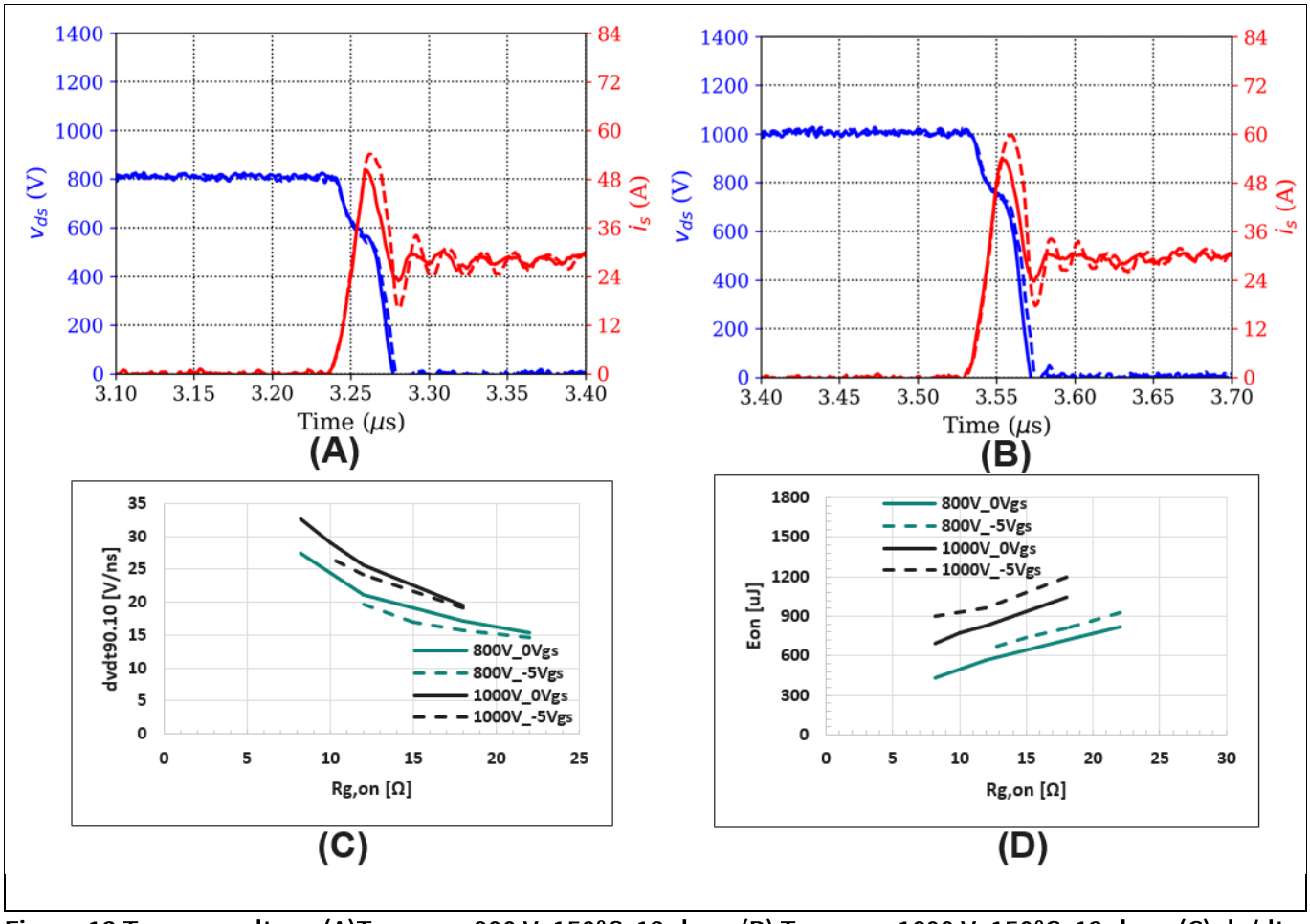


Figure 12 Turn on voltage (A)Turn on - 800 V, 150°C, 12ohms (B) Turn on - 1000 V, 150°C, 12ohms (C) dv/dt vs Rg(on) (D) Turn on losses vs Rg(on)

As shown in Figure 12, driving at 1000 V is more beneficial than driving with a 0 V gate voltage than 800 V at the same dv/dt. Overvoltage gets more pronounced at -5 V gate voltage, limiting the $R_{g(on)}$. In addition, CoolSiC™ Gen2 MOSFETs allow voltage peaks down to –10 V, allowing headroom for voltage peaks coming from high dV/dt or parasitic inductances from the PCB design [4].

5 Package

Offering the new 1400 V Gen2 CoolSiC™ MOSFETs in T0247-4 pin packages addressed the demand for higher system power density and a simpler PCB assembly process. In this chapter, the specific features and variants of the TO247-4 HC package used for this product family are discussed, such as the T0247-4-17 package (Standard High creepage package) and T0247-4-18 package (Reflow capable), increased lead thickness, and improved Rth(j-c) due to reflow soldering, significant thermal considerations, and assembly recommendations.

5.1 New T0247-4 package variants for higher blocking voltage

The outer shapes of a new TO247-4-18 with wide clearance & creepage distances, and the standard TO247-4-17 package, are compared in Figure 13. The standard TO247-4 HC package has minimum clearance and creepage distances of 3.5 mm and 5.2 mm, respectively. On the other hand, the new TO247-4 reflow package has 5.3 mm and 10.8 mm of enhanced clearance and creepage distances, respectively, through the groove of the package body and thicker lead structures, which will significantly improve the isolation voltage, and higher current handling capability and system reliability can be improved as a result.

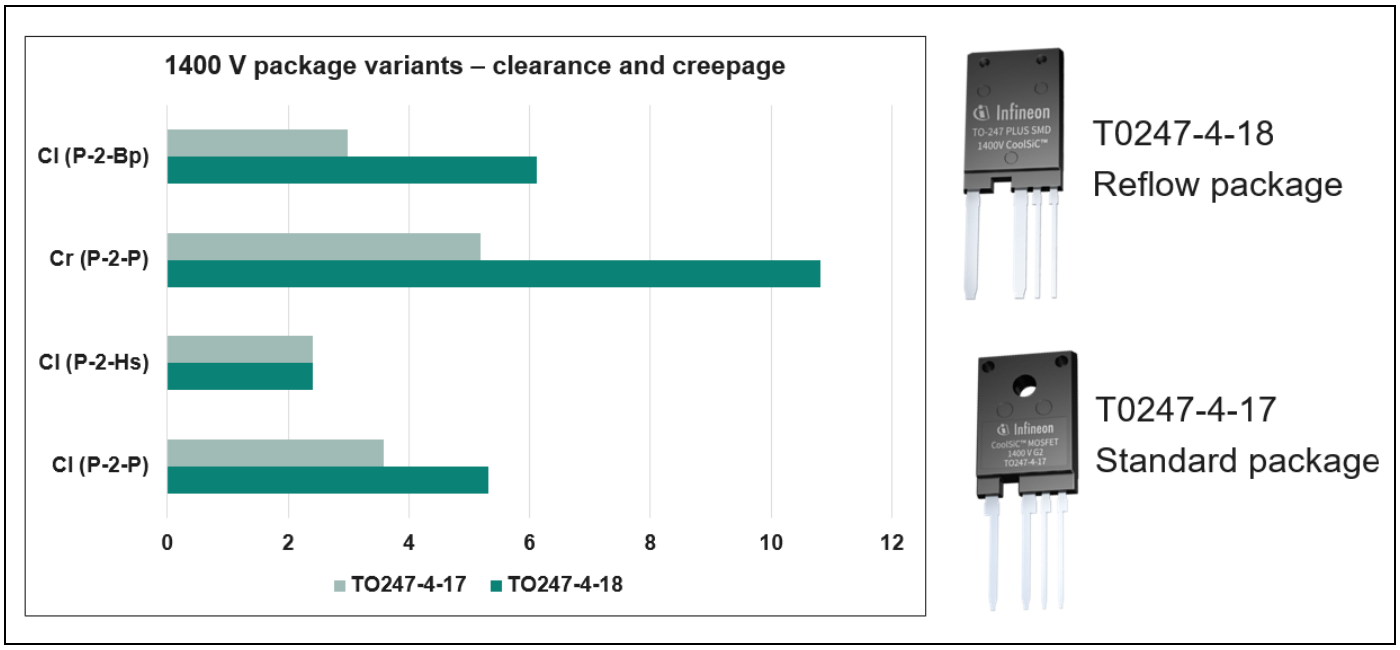


Figure 13 New T0247-4 pin package variants for a higher blocking voltage device

Despite the wider clearance and creepage distances, the new TO247-4-18 package is fully compatible with liquid-cooling systems and can withstand 3 times the reflow soldering cycle, enabling lower $R_{th(c-h)}$. On the other hand, the standard 1400 V package is fully compatible with the PCB design for the existing 1200 V design because the same pin pitches are used. In addition, the reflow-capable version has much wider leads than the standard version to handle much higher current.

5.2 Lead current handling capability

The current carrying capacity of any package, including the TO-247, ultimately depends on the temperature factor. The most important temperature to consider is the junction temperature. However, this is not directly related to the PCB design. Another critical factor is the temperature of the wire bonds. Nevertheless, this is already accounted for in the package design to meet the device's maximum rating specifications. The preliminary analysis was conducted using a simulation with unconservative input parameters as shown in Table 2. The current-carrying capacity of the TO-247 standard HC package and the TO-247 reflow package is

compared across different scenarios, as shown in Figure 14. The TO-247-4-18 reflow device can handle a wider current range of 18% to 22%, compared to the TO-247-4-17 standard HC package.

Table 2 Simulation boundary conditions for current capability

Simulation Boundary Conditions			
PCB standard FR4	2 layers (power traces)		
	2 mm thickness		
	Copper thickness	70 um	105 um
Package lead lengths	6.5 mm	13 mm	
Heatsink temperature	50°C		
Cooling	Natural convection	Forced Air cooling	

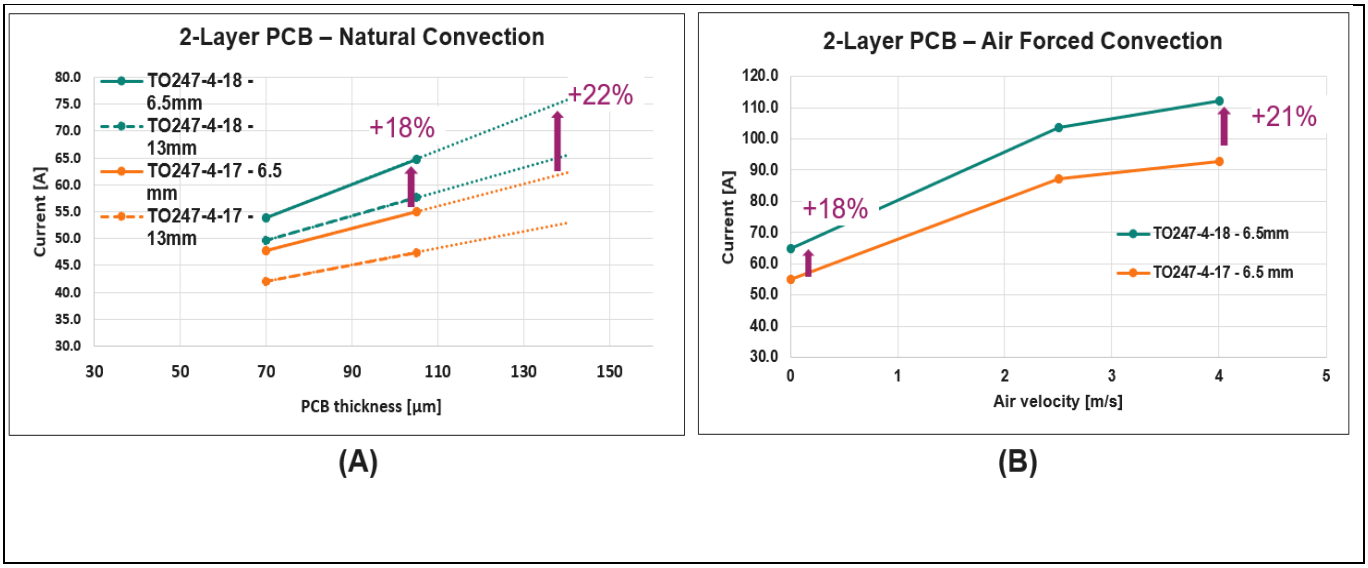


Figure 14 Lead current handling capability (A) Natural convection (B) Forced Air convection

5.3 Thermal Management Solutions

There are multiple thermal stack solutions available. Based on the application and the requirements, the thermal management might change, which will impact the performance of the system. As shown in Figure 15, there are three different thermal stack techniques:

- Indirect cooling – Assembly 1– typical method followed in the industry using thermal grease and Al2O3
- Indirect cooling – Assembly 2 - device soldered to DCB and TIM between DCB and heatsink
- Direct cooling – Assembly 3 – 2x solder – device + DCB and DCB + heatsink

Package

There are several challenges in indirect cooling, like poor thermal conductivity, High mechanical pressure, High contact resistance, or additional BOM and assembly cost. On the other hand, direct cooling offers the advantage of automated assembly and can achieve higher power due to its better thermal conductivity.

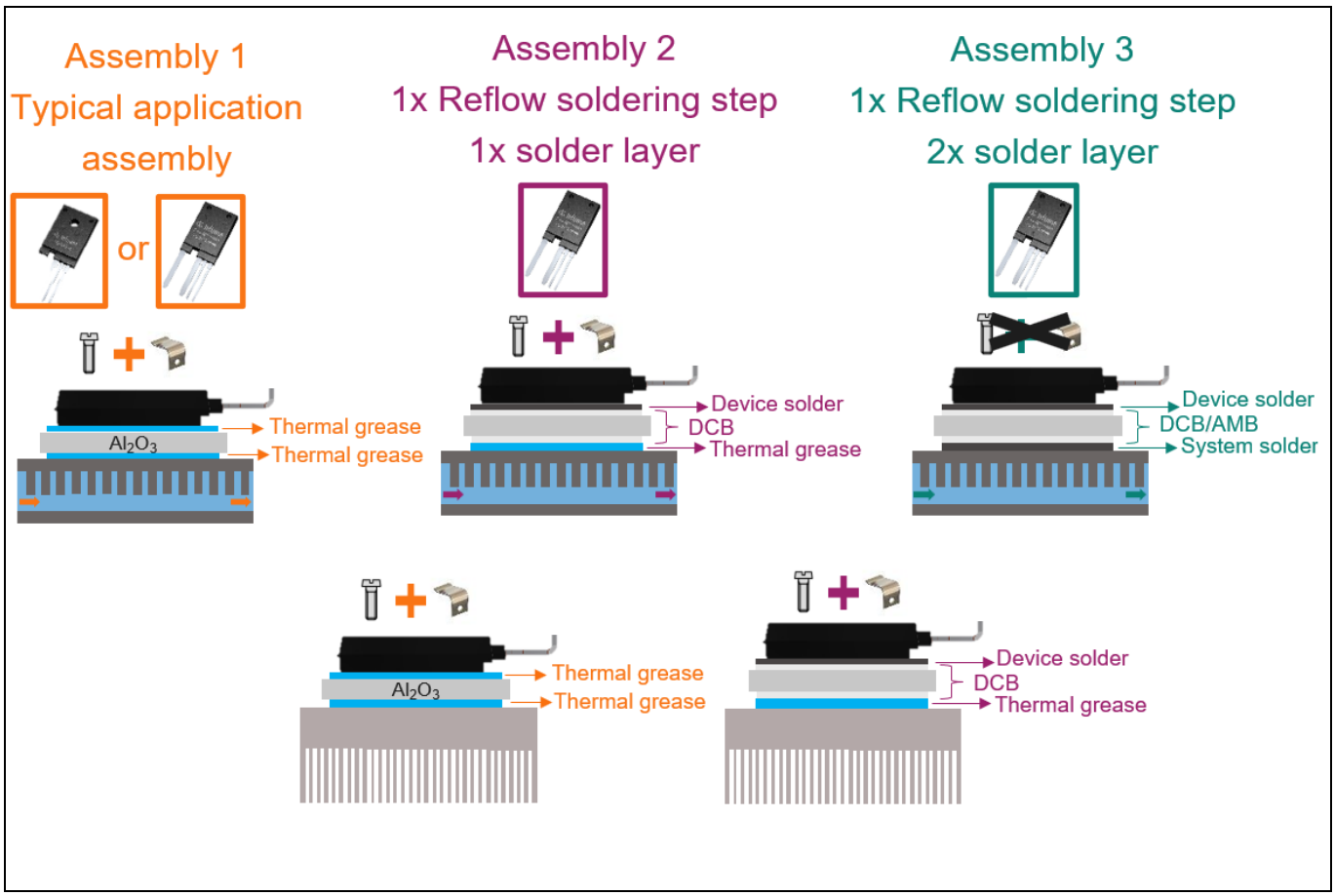


Figure 15 Different thermal management solutions for both liquid and air-cooling systems

Table 3 Thermal simulation for different assembly configurations

Product	Cooler Type	Thermal resistance [k/W]			
		Assembly 1	Assembly 2	Assembly 3	
IMYR140R008M2H	Liquid	1.15	0.98	0.78	0.69 (AMB)
	Air	1.58	1.41	-	
IMYR140R029M2H	Liquid	1.71	1.53	1.27	1.16 (AMB)
	Air	2.08	1.9	-	

The assembly 2 method results in a 10-15% lower thermal resistance than assembly 1. However, several challenges in indirect cooling were explained earlier. So, the third assembly, which uses direct cooling, results in a 20-30% lower thermal resistance than the second method when using active metal brazing, and a 15-20% lower thermal resistance when using DCB, Table 3.

Package

Figure 16 shows that the reflow assembly (liquid cooling) offers a better value proposition than a typical assembly (air cooling). The benefit decreases to 16% for low ohmic devices. Whereas in liquid cooling, Output power improves from 14% to 35% depending on the interface (no screw, no clip), wider lead package to carry more current, and potentially fewer parallel devices.

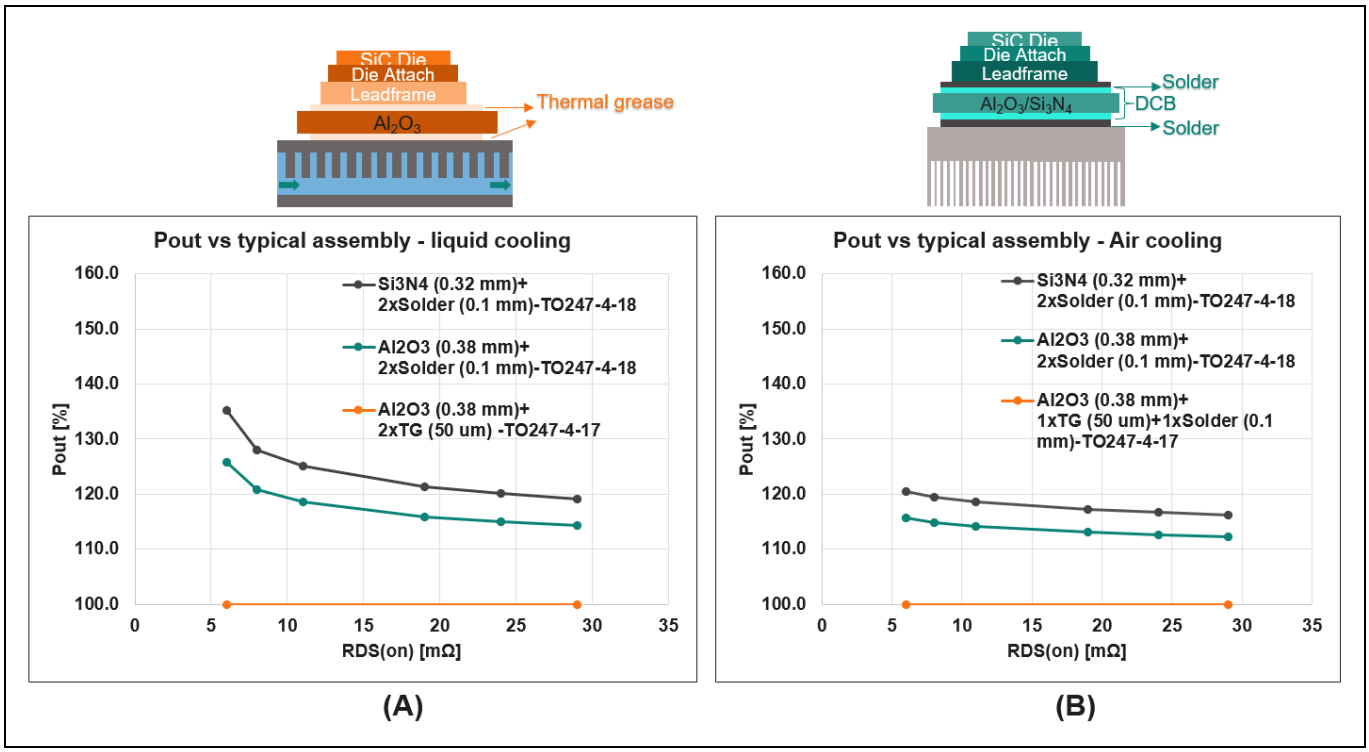


Figure 16 Output power vs Reflow and Typical assembly (A) Liquid cooling (B) Air cooling

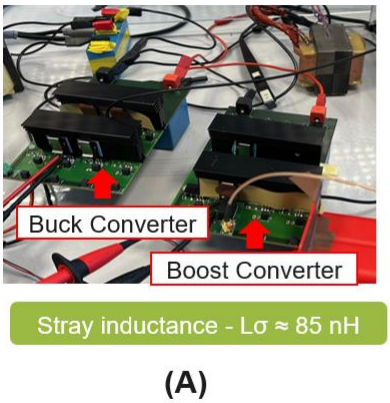
6 Application performance

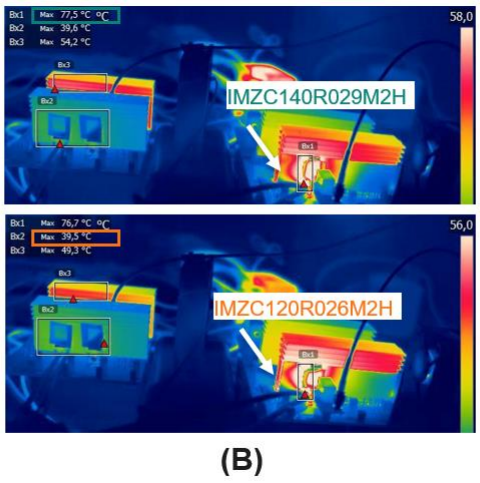
This section presents the application performance of the 1400 V device, benchmarked against the 1200 V CoolSiC™ MOSFET, in both hard- and soft-switching applications, focusing on the Buck-Boost and LLC converters.

6.1 Hard switching: Buck-Boost converter

PV hybrid inverters are moving towards higher VDC. From 1100 V DC to 1250 V DC. Compared with a 1100 V DC system at the same power rating, a 1250 V PV inverter reduces the number of MPP trackers (DC-DC) by two, which translates into a reduction in string inverter components such as switches, SiC diodes, current sensors, terminals, EMI filters, and more, while also lowering the requirements for string DC cables, DC breakers, and mechanical and electrical installation efforts, resulting in significant overall cost savings.

At the same number of MPPTs, the 1250 V PV inverter enables a 20% higher DC-AC ratio, increasing the PV installation's energy yield and directly enhancing profitability through higher energy generation. Now with Gen2's higher blocking-voltage capability, the 1400 V SiC MOS achieves a lower $R_{g,off}$. This allows for maintaining total losses in MPPT, eliminating the need for any thermal management modification.





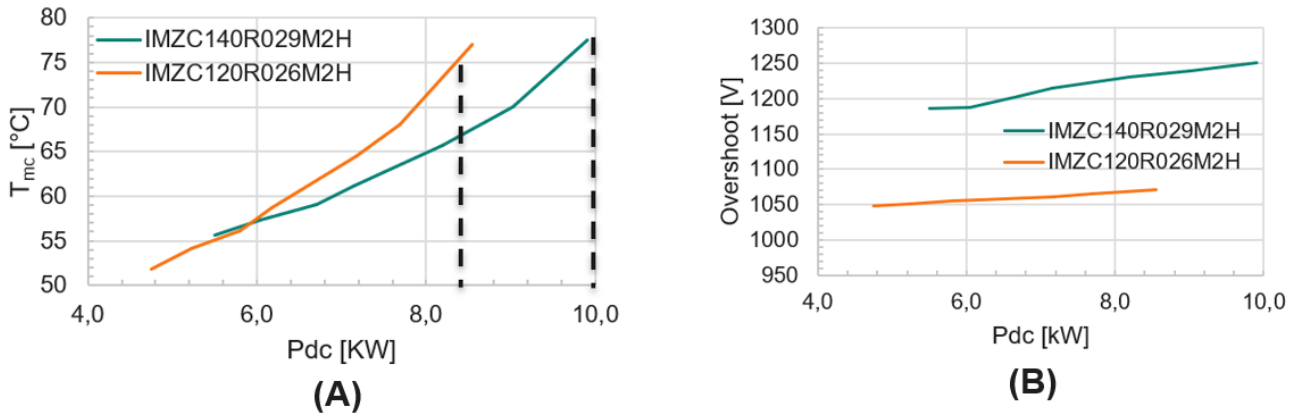
Experimental test conditions	
V_{gs} [V]	-3 -18
Duty cycle	0.5
f_{sw} [kHz]	32
L_{boost} [µH]	480
Ta [°C]	25
TIM	Pad - K10
Forced Air Cooling	

(C)

Figure 17 Buck/Boost converter (A)Test setup (B) Thermal image of the setup (C) Test condition

Figure 17 shows the test setup for the DUTs. For a similar case, temperature and voltage margin, the 1400 V device offers 16% higher output power compared to the 1200 V device, as shown in Figure 18. For the PV application, this can be translated into the same number of MPPT and increase the total power or similar power like before with reduced MPPT. As shown in Figure 19, an application test under the same Vdc shows that the efficiency of the 1400 V will increase due to less overshoot, and the switching frequency can be increased. Higher reliability due to higher blocking voltage (spikes, leakage current, and cosmic robustness).

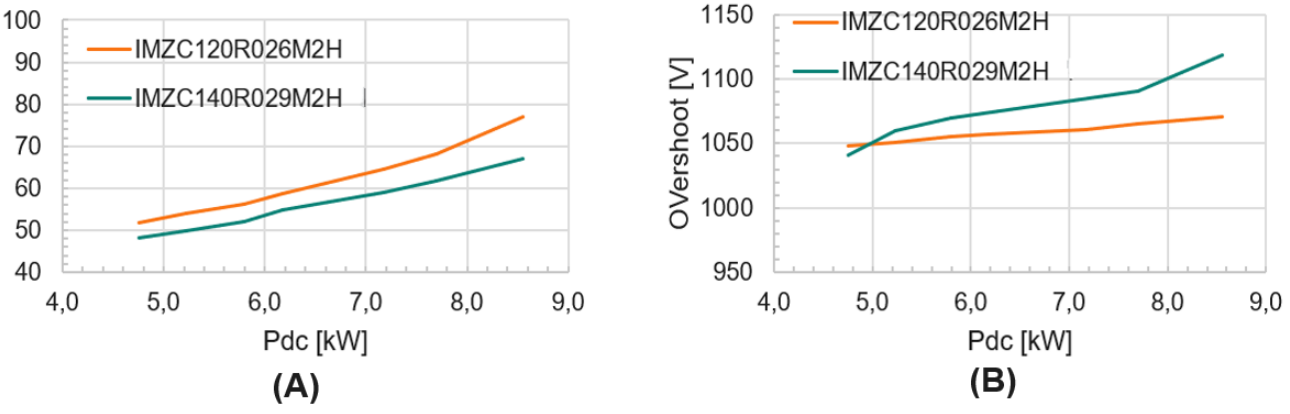
Application performance



DUT	$R_{g,off}$ [Ω]	$R_{g,on}$ [Ω]	dvdt10.90 [V/ns]	dvdt90.10 [V/ns]	Vdc [V]
IMZC140R029M2H	12	15	40	40	1100
IMZC120R026M2H	22	15	24	34	950

(C)

Figure 18 1400 V vs 1200 V performance under different Vdc (A) case temperature (B) overshoot in the system (C) DUT conditions



DUT	$R_{g,off}$ [Ω]	$R_{g,on}$ [Ω]	dvdt10.90 [V/ns]	dvdt90.10 [V/ns]
IMZC120R026M2H	22	15	24	34
IMZC140R029M2H	7	15	43	33

(C)

Figure 19 1400 V vs 1200 V performance under similar Vdc (A) case temperature (B) overshoot in the system (C) DUT conditions

6.2 Soft switching: LLC converter

EV charging application one of the key valuable propositions is efficiency, where the 1400 V device helps by having lower energy losses due to $R_{g(off)}$ reduction. On other hand increased voltage margin at worst case turn-off current will simply snubber design.

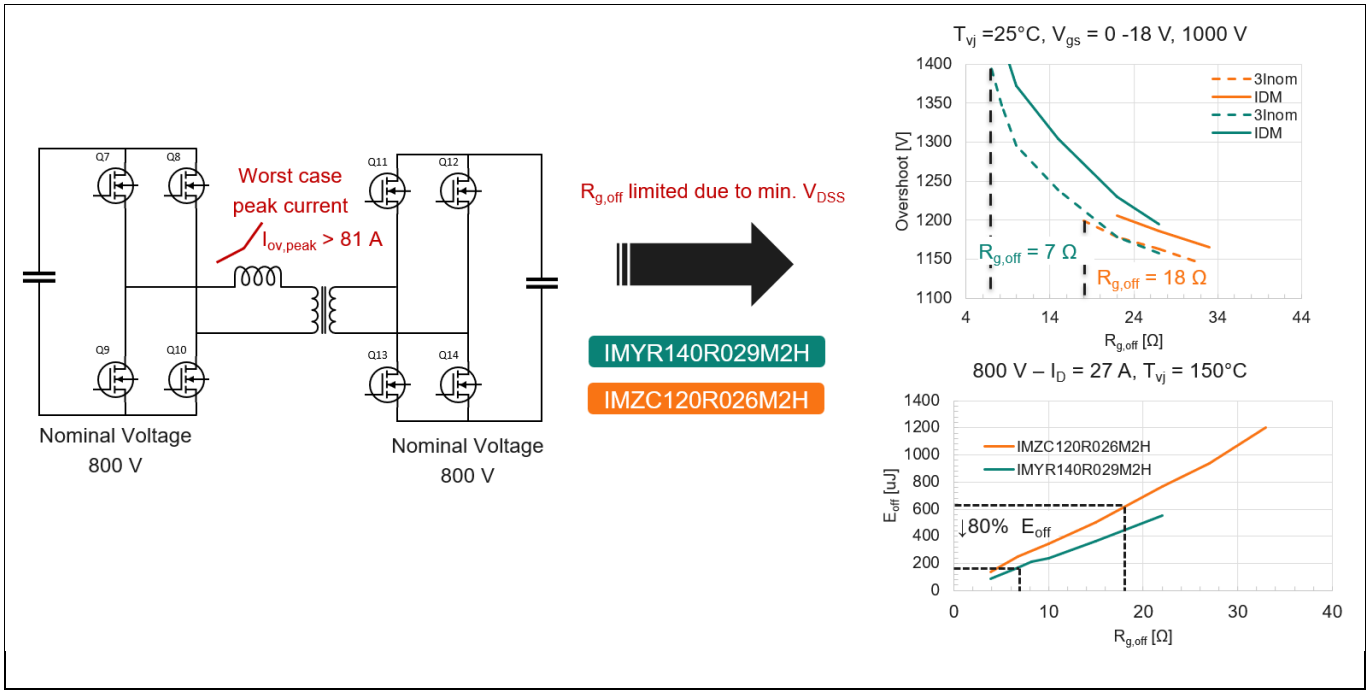


Figure 20 Soft switching (A) overshoot vs Rg(off) (B) Eoff vs Rg(off)

In comparison with the hard-switching use case in a soft-switching topology, the main losses consist of conduction and turn-off portions of switching losses. Figure 20 shows the overshoot behavior between the 1400 V and 1200 V devices. When the application operates at the upper voltage limit, close to 1000 V, and the worst-case peak current occurs, for example, in the case of 3Inom, which is 81 A, the $R_{g(off)}$ has to be limited due to the minimum V_{DSS}. The 1400 V, a considerably lower $R_{g(off)}$ can be used, which in turn results in 80% lower turn-off losses at 800 V and nominal current.

7 Summary

This document describes the need for higher blocking voltage Gen2 of CoolSiC™ MOSFETs in comparison with the state-of-the-art system. The TO-247 reflow package variant allowed users to increase power density and system power, as well as fast design with the standard package variant. High voltage class increases the robustness of the system as well as improves efficiency compared to the state-of-the-art 1200 V system. Furthermore, the technology parameters have improved dramatically, leading to an enhanced behavior in the end-user application, reaching the highest efficiency and ease of use.

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