CoolGaN™ hybrid driving evaluation board with EiceDRIVER™ 1EDB7275F and 1EDN7550B

Ordering code: EVAL_HB_GAN_HYBRID

Products: CoolGaN™ IGLD60R070D1, EiceDRIVER™ 1EDB7275F and 1EDN7550B

About this document

Scope and purpose

This application note explains how to use EVAL_HB_GAN_HYBRID to evaluate hybrid driving together with CoolGaN™ gate injection (GIT) high electron mobility transistors (HEMTs) in high-voltage (HV) half-bridge (HB) configuration to achieve a low bill of materials (BOM) and a cost-effective solution to drive a non-isolated HB stage.

The EVAL_HB_GAN_HYBRID board enables testing of both GIT and Schottky gate (SG) GaN HEMTs in a DFN 8 x 8 package, while the hybrid driving approach allows taking advantage of two single-channel gate drivers to have more layout flexibility, optimize driving loops and reduce BOM for the low-side (LS) bias supply.

The board also allows flexibility to configure and test different bias supply solutions: bipolar non-isolated hybrid driving, bipolar isolated auxiliary supply and unipolar with bootstrap are possible. By means of an external inductor the EVAL_HB_GAN_HYBRID board enables double-pulse testing and continuous operation.

Intended audience

This document is intended for R&D engineers, application engineers and hardware designers interested in comparing the switching performance of GaN HEMTs with hybrid driving vs. other bias supply approaches.

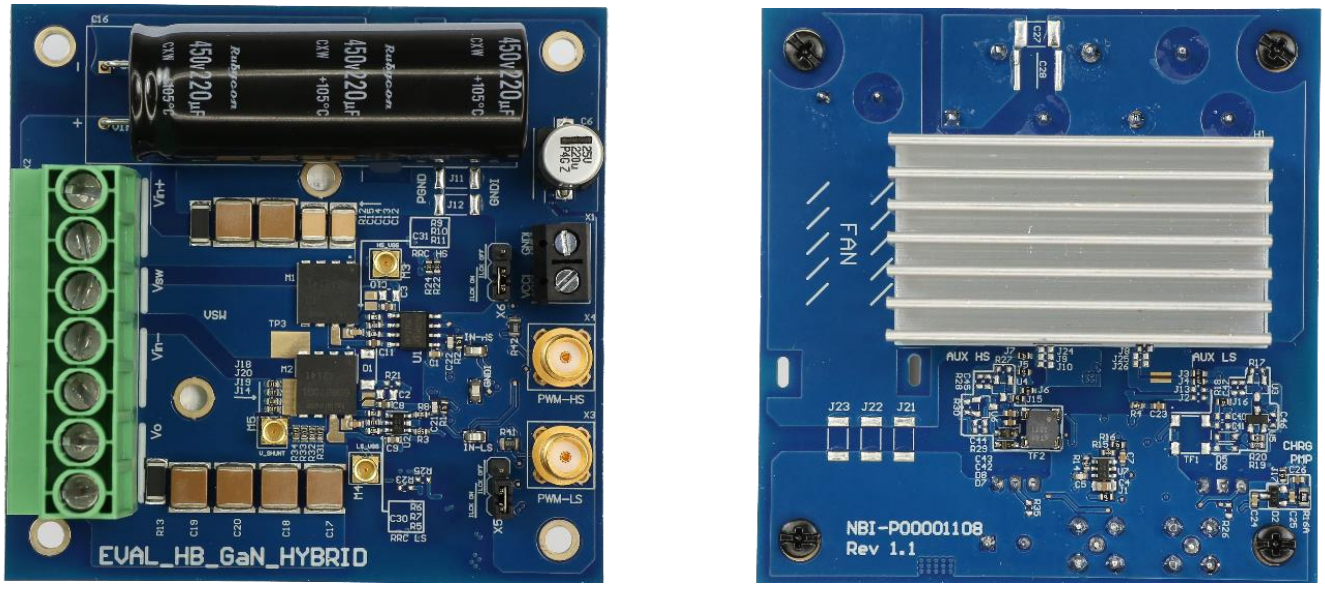

Figure 1 EVAL_HB_GAN_HYBRID board overview – top (left) and bottom (right) sides

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1 Introduction

The EVAL_HB_GAN_HYBRID board is a standalone testing platform enabling double-pulse measurements for Infineon's CoolGaN™ HEMTs and similar HEMTs in DFN 8 x 8 package, along with different bias supply approaches using the isolated driver EiceDRIVER™ 1EDB7275F and the truly differential input (TDI) EiceDRIVER™ 1EDB7550B EiceDRIVER™ 1EDB7550B. A generalized block diagram of EVAL_HB_GAN_HYBRID is shown in Figure 2.

Two CoolGaN™ IGLD60R070D1 HEMTs are configured as HB, and the power stage is accessible through a seven-port connector via pins V_{IN+}, V_{IN-} and V_{SW}. It is configurable to perform double-pulse testing or continuous operation depending on the pulse-width modulation (PWM) driving pattern and the external connection of the filter inductor. Output filter capacitors are also provided on the board and accessible via the V_{OUT} power pin to avoid the need for an additional external capacitor during buck or boost operation. Section 2 shows how to properly configure the board for each configuration.

The HB stage can be controlled by two PWM signals provided via arbitrary waveform generator (AWG), and connected to the board via the PWM SMA connectors. Interlocking function can be enabled on the board to provide shoot-through protection (STP) by cross-connecting the PWM inputs of the driver ICs, while proper dead time (DT) must be ensured via AWG timing.

Several test points are available on the board to provide access to the main signals of interest and measure the switching waveforms of the GaN stage together with Infineon gate driver ICs. Three MMCX connectors provide direct access to the gate-source and shunt resistor voltages.

Several bias supply options (e.g., bipolar or unipolar, isolated or non-isolated) are possible for the driver by powering the V_{DDI} to GNDI voltage, without requiring an additional supply. Section 2.4 and Section 3.1 show in more detail the position of the measurement points and the auxiliary supply configurations.

The output and bus voltage can range up to 450 V, limited by the capacitor rating. The HB maximum current, operating frequency and mode are limited only by the maximum current rating and the thermal dissipation of the power switches.

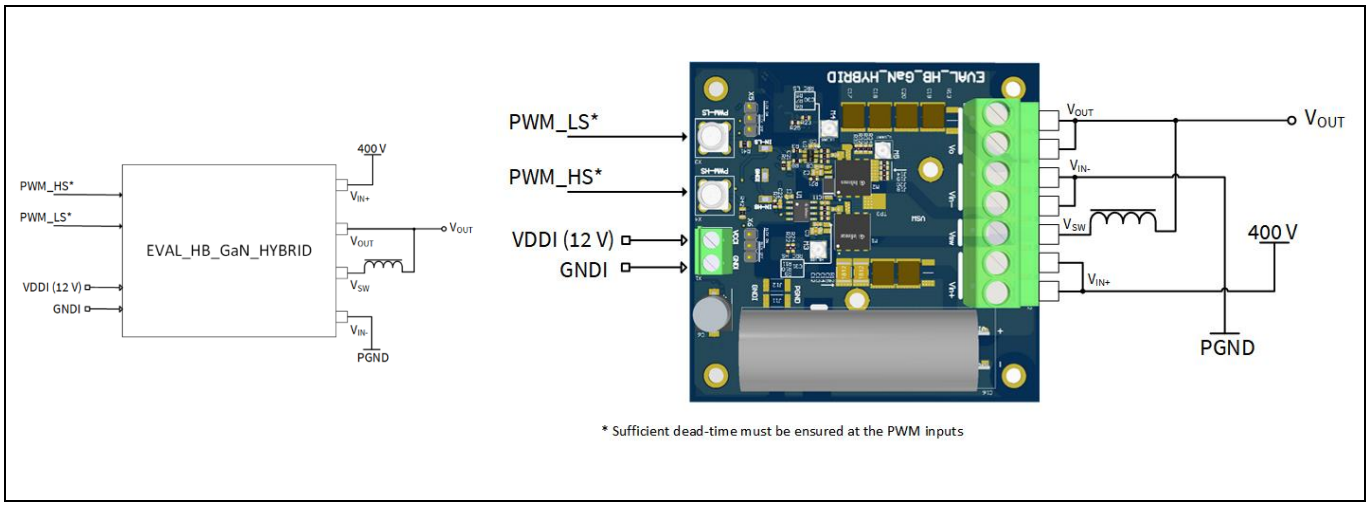


Figure 2 EVAL_HB_GAN_HYBRID block diagram and connections – buck configuration example

1.1 Absolute maximum ratings

Attention: ***Stresses beyond the values listed under absolute maximum ratings may cause permanent damage to the board.***

Attention: ***This evaluation board has exposed HV contacts. Use appropriate protective measures to avoid shocks.***

Table 1 Absolute maximum ratings

Parameter		Values			Unit	Note
		Min.	Typ.	Max.		
V_{CCI}	Logic supply voltage	6	12	18	V	*Value can be changed if different bias supply voltages are needed*
I_{VCCI}	V_{CCI} input current	–	27	30	mA	*V_{CCI} = 12.0 V; OUTx = low; Config. A*
		–	39	43	mA	*V_{CCI} = 12.0 V; f_{SW} = 100 kHz; Config. A*
V_{INH}	PWM inputs (INA, INB) high logic level	4.8	5	5.2	V	
t_{PW}	Minimum applicable PWM pulse width	25	–	–	ns	
t_{PD}	Driver propagation delay PWM to V_{GS} voltage	–	45	–	ns	*Turn-on and turn-off transitions*
Z_{PWM}	PWM inputs impedance	–	50	–	Ω	*Impedance at X3 and X4*
V_{IN+}	Voltage at pin V_{IN+}	0	400	450	V	*Referred to V_{IN-}, limited by voltage ratings of capacitors on V_{IN+}*
V_{OUT}	Voltage at pin V_{OUT}	0	–	450	V	*Referred to V_{IN-}, limited by voltage ratings of capacitors on V_{OUT}*
V_{SW}	Voltage at pin V_{SW}	0	–	600	V	*Referred to V_{IN-}, including overshoots*
V_{IN-}	Voltage at pin V_{IN-} with respect to logic ground GNDI	-60	–	+60	V	*V_{INH} = 5 V; referred to pin GNDI; PGND and GNDI disconnected*
I_{SW_PK}	Switch pulsed current, drain to source	–	–	60	A	*See footnote* [1]
dV_{SW}/dt	Switching node slew rate	–	–	250	V/ns	*See footnote* [2]
f_{SW}	Operating frequency	–	0.25	2.0	MHz	
T_{SW_C}	Switch case temperature	–	–	125	°C	*See footnote* [3]

[1] Maximum board current limit. This value can be lower, depending on the current capability of the switches (e.g., 35 A for IGLD60R070D1). Exceeding the current rating of the GaN HEMTs can damage the devices permanently.

[2] This value can be lower, depending on the switch used (e.g., 200 V/ns for IGLD60R070D1). Exceeding the rating of the GaN HEMTs during operation can damage the devices permanently.

[3] Limited by GaN junction temperature. Exceeding maximum temperature during operation can damage the power stage permanently.

2 Board description and setup

2.1 Power stage

EVAL_HB_GAN_HYBRID is equipped with a seven-port terminal block allowing several connection options and testing in different configurations. Typical connection block diagrams for testing double-pulse, reverse double-pulse, buck mode and boost mode are shown in Figure 3, Figure 4, Figure 5, and Figure 6, respectively.

A standard low-voltage (LV) power supply and an arbitrary waveform generator are needed to power the driving stage and generate the gate-to-source signals for the two GaN transistors. The HV DC-link of the HB can be supplied with a HV (400 V) DC power supply. To test at high power in buck and boost mode configurations, a programmable DC electronic load is needed.

The list of the probing points is shown in Section 2.4, with main test points provided on the board together with probing sockets for high-CMRR optical differential probes.

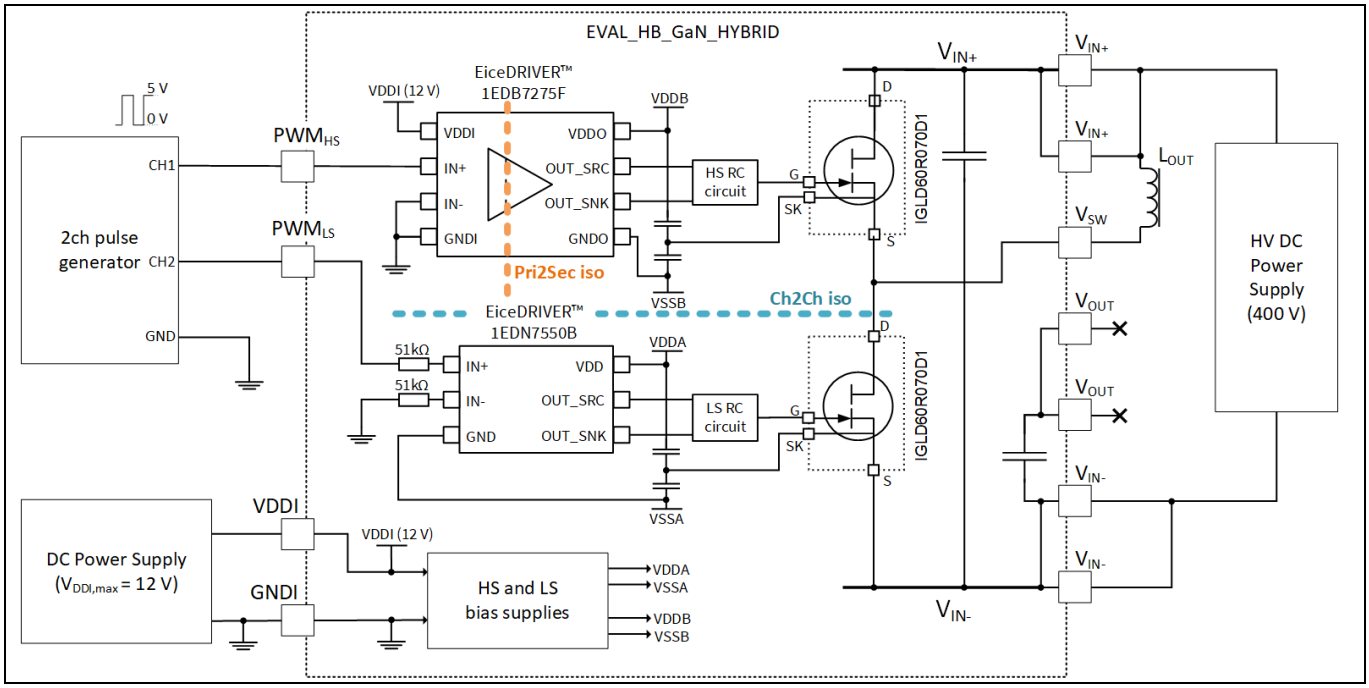


Figure 3 Board configuration for double-pulse test setup

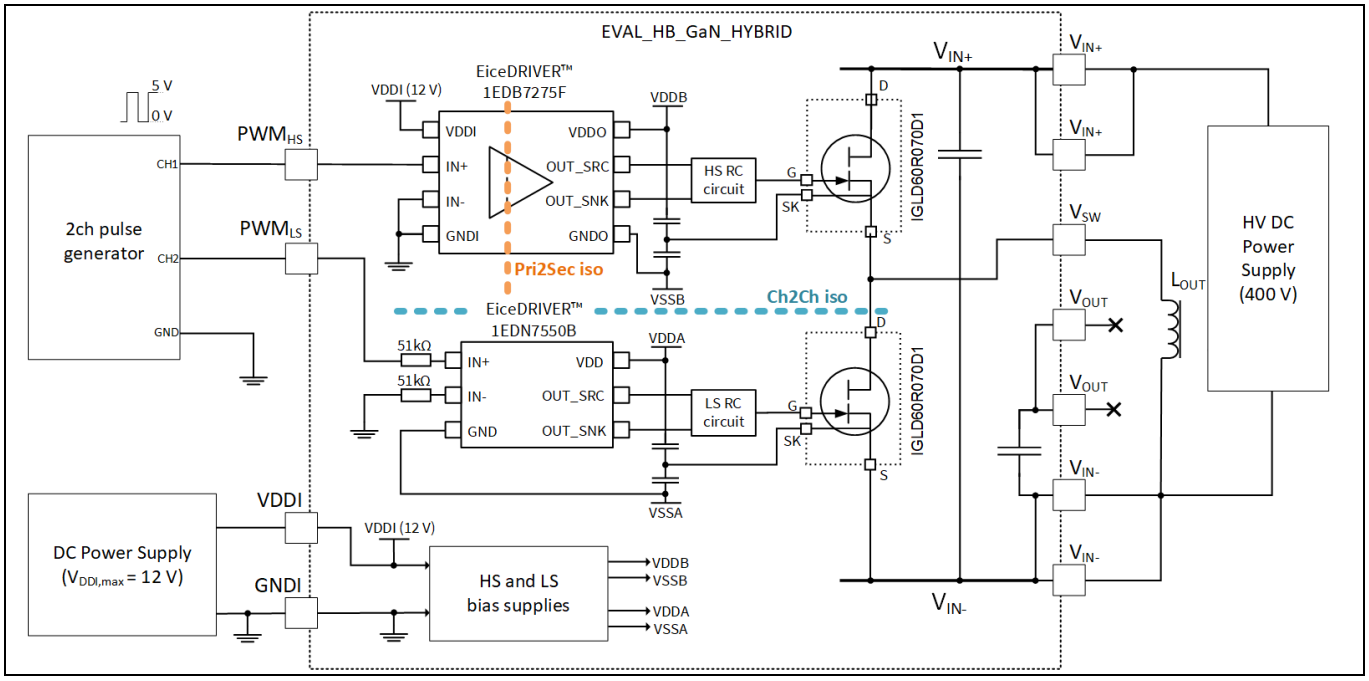


Figure 4 Board configuration for reverse double-pulse test setup

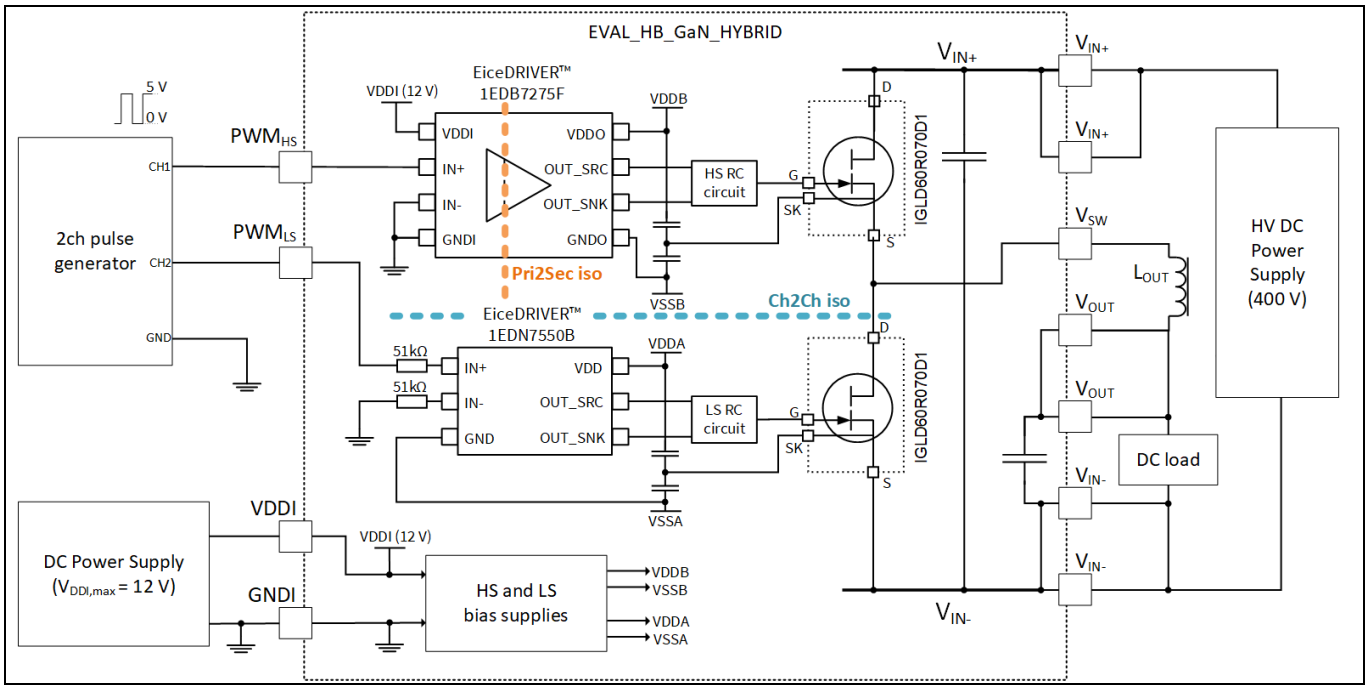


Figure 5 Board configuration for DC-DC buck configuration

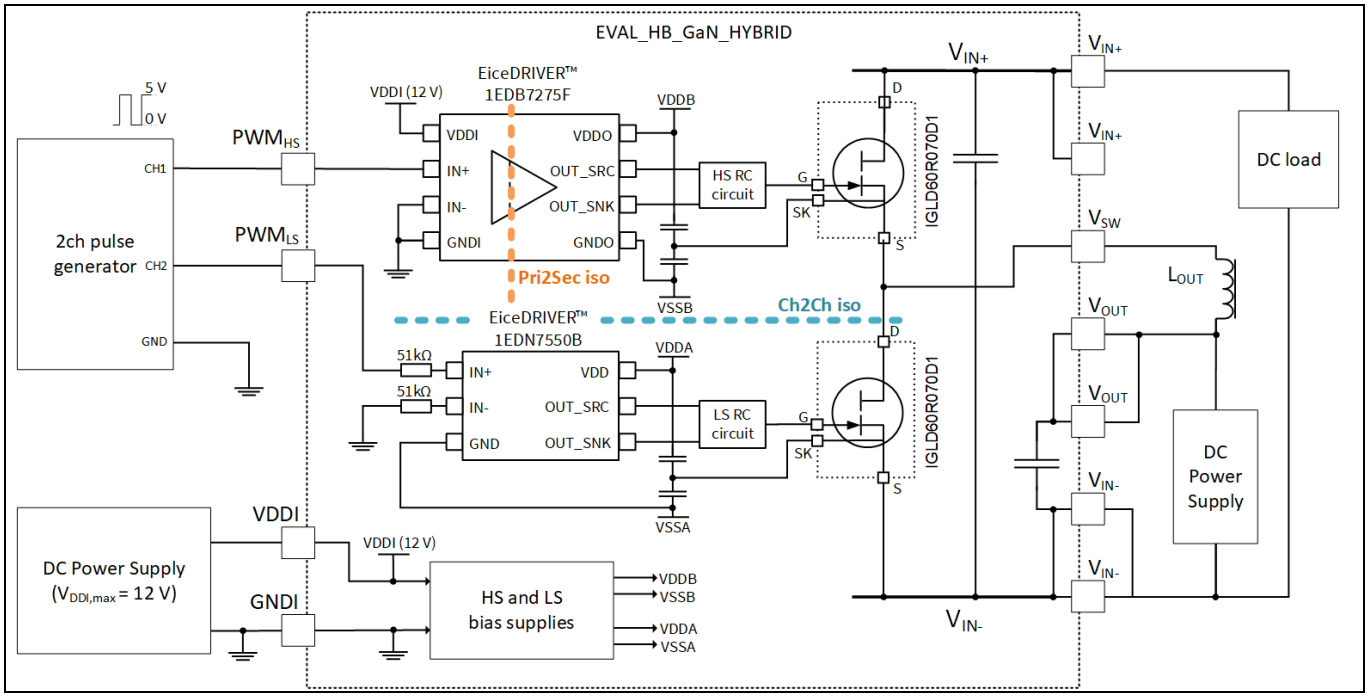


Figure 6 Board configuration for DC-DC boost configuration

2.2 Bias supply

In the proposed hybrid driving scheme, galvanic isolation is not provided[1] for the LS switch, therefore a LS non-isolated bias supply using a charge pump (CP) to provide the negative bias voltage is more suitable for this driving scheme. Hybrid driving complements the auxiliary driving circuit already proposed for GaN switches [1], [2], [4].

EVAL_HB_GAN_HYBRID however allows configurability of different bias supply solutions, apart from the hybrid driving scheme (default). The high-side (HS) and low-side (LS) GaN HEMTs of the power stage can be driven with either unipolar or bipolar gate-source voltages. The following configurations are possible, as shown in Figure 7:

- bipolar hybrid bias supply (HS via isolated AUX, LS via CP)
- bipolar bias supply via AUX transformers
- unipolar bias supply via bootstrapping.

Table 2 Overview of the three bias supply approaches

Bias supply configuration	Negative bias available	Galvanic isolation	Low-side bias supplied via	High-side bias supplied via
A – hybrid (default)	✔	Non-isolated [2]	V_{DDI} + CP	Isolated AUX
B – ISO AUX	✔		Isolated AUX	Isolated AUX
C – bootstrap			V_{DDI}	Bootstrap

[1] EiceDRIVER™ 1EDN7550B is a non-isolated gate driver IC with TDI capability to reject common mode between signal ground GNDI and power ground GND

[2] Galvanic isolation, if needed, can be achieved with auxiliary supplies [2] or by means of ISOFACE™ 2DIB0400F (see Section 7).

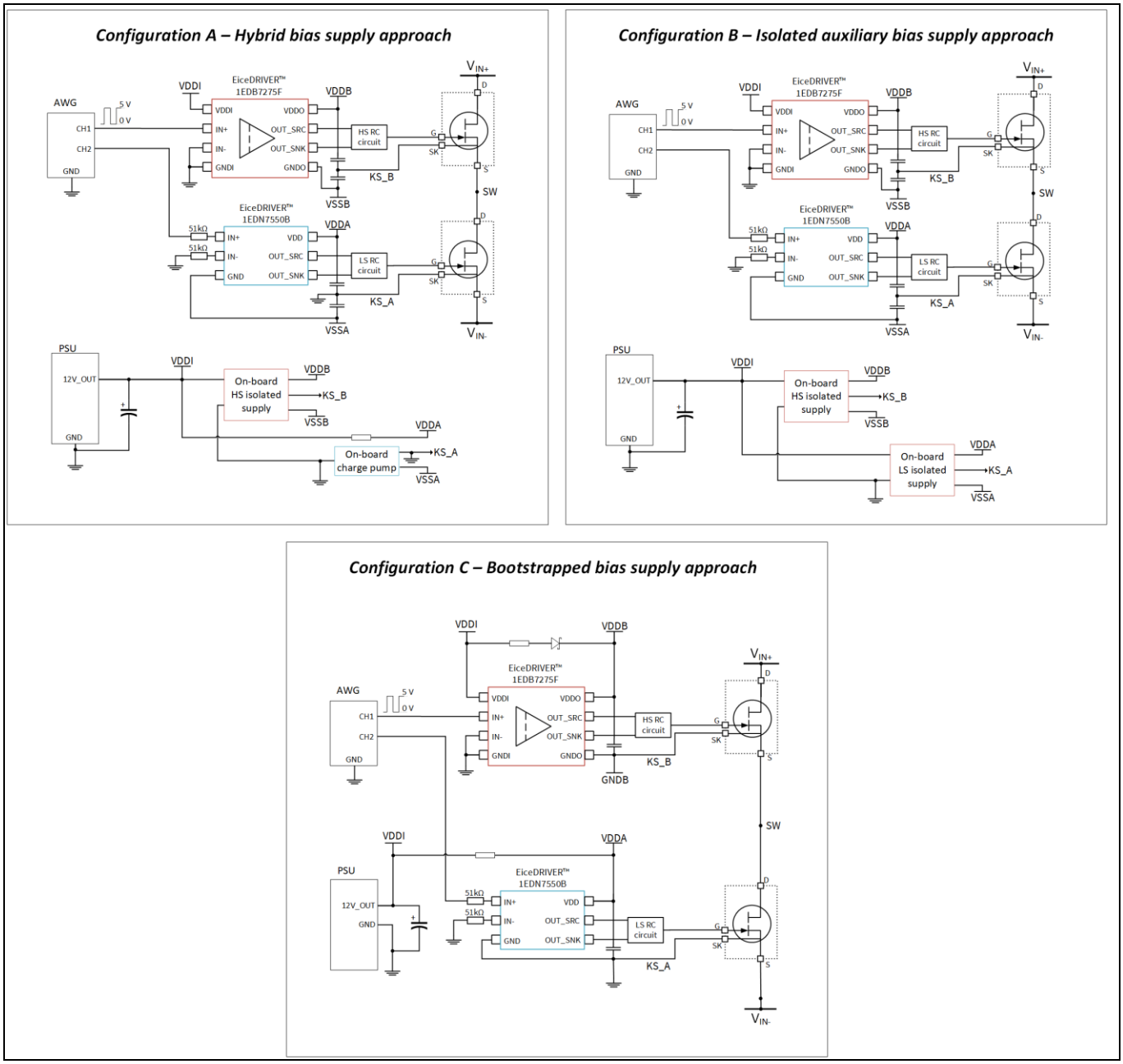


Figure 7 Block diagram – available bias supply configurations in EVAL_HB_GAN_HYBRID

2.2.1 Selecting the bias supply

The bias supply configuration can be selected by means of jumpers. Table 3 shows the minimum required changes to be made to the board in order to select the proper bias supply configuration.

Figure 8, Figure 9, and Figure 10 visualize the minimum layout changes required (highlighted red or green areas), and the circuitry which can be removed in a final setup is shown for each configuration (shaded red).

Table 3 Jumper/components configuration for bias supply selection

Bias supply configuration			Populated jumpers/components	NO_BOM jumpers/components
	HS	**LS**		
Config. A (default) *Bipolar hybrid bias* Figure 8	Isolated AUX	V_{DDI} + CP	- ***TOP**: C8, C9, C10, C11* - ***BOTTOM**: J3, J4, J5, J6, J7, J15, J16, J17, R4, C23* ***Note**: AUX HS and CP circuits must be populated*	- ***TOP**: D1, C2, C3, R21* - ***BOTTOM**: J2, J8, J9, J10, J13, J24, J25, J26* ***Note**: AUX LS circuit can be not in BOM*
Config. B *Bipolar isolated bias* Figure 9	Isolated AUX	Isolated AUX	- ***TOP**: C8, C9, C10, C11* - ***BOTTOM**: J2, J3, J4, J5, J6, J7, J15, J16* ***Note**: N/A*	- ***TOP**: D1, C2, C3, R21* - ***BOTTOM**: J8, J9, J10, J13, J17, J24, J25, J26, R5, R16A, C23* ***Note**: Charge pump LS circuit can be not in BOM*
Config. C *Unipolar bias with bootstrap* Figure 10	Bootstrap	V_{DDI}	- ***TOP**: D1, C2, C3, R21* - ***BOTTOM**: J8, J9, J10, J13, J24, J25, J26, R4, C23* ***Note**: SP1 and SP2 shorting is recommended to improve unipolar driving loop*	- ***TOP**: C8, C9, C10, C11* - ***BOTTOM**: J2, J3, J4, J5, J6, J7, J15, J16, J17, R16A* ***Note**: SP3 shorting is recommended to improve unipolar driving loop; both AUX supplies and CP circuit can be not in BOM*

Appendix A reports the full schematic. Configurations A, B and C are managed as variants in the Altium design files.

In Figure 8, Figure 9, and Figure 10: the yellow rectangles denote the area of rework. Sharp red markers highlight the jumpers (or components) to be removed, sharp green the jumpers (or components) to be mounted, and light red shading identifies the components which can be not in the BOM.

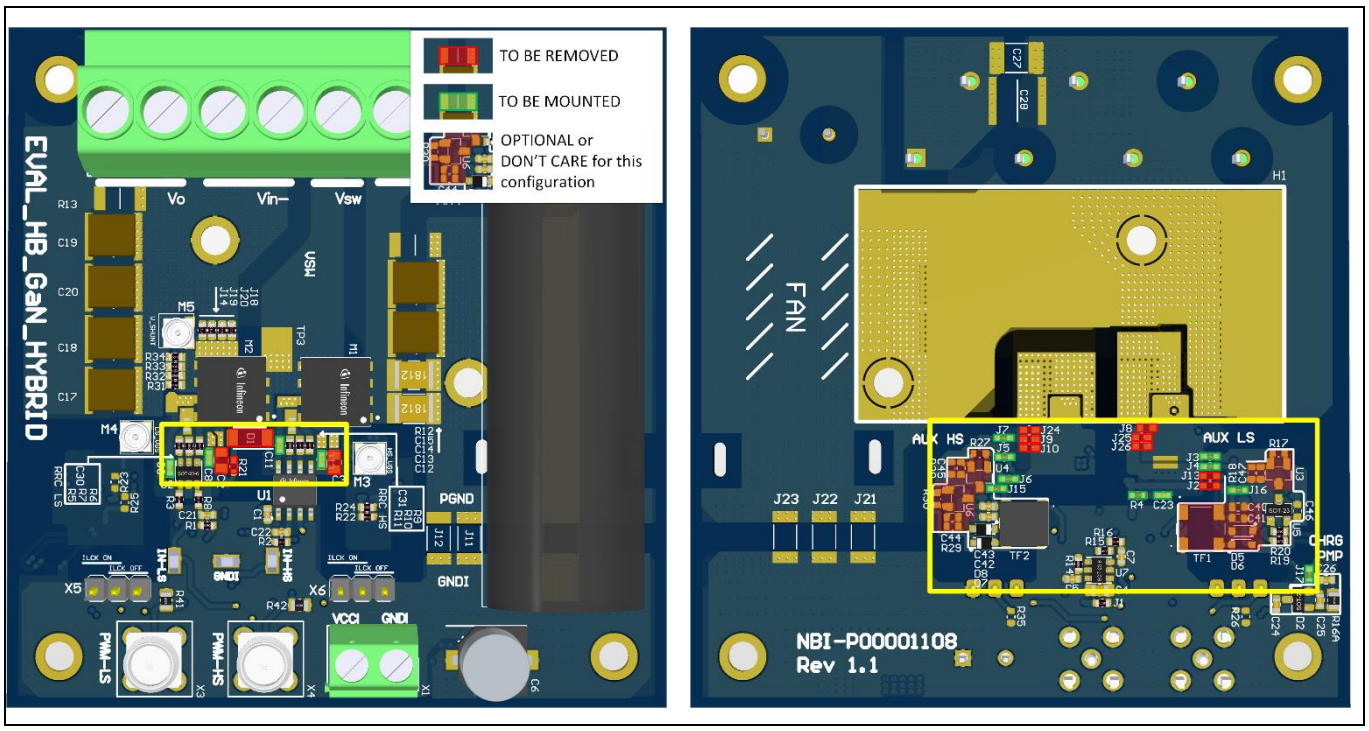


Figure 8 Jumper placement for Config. A – hybrid bipolar bias supply (default)

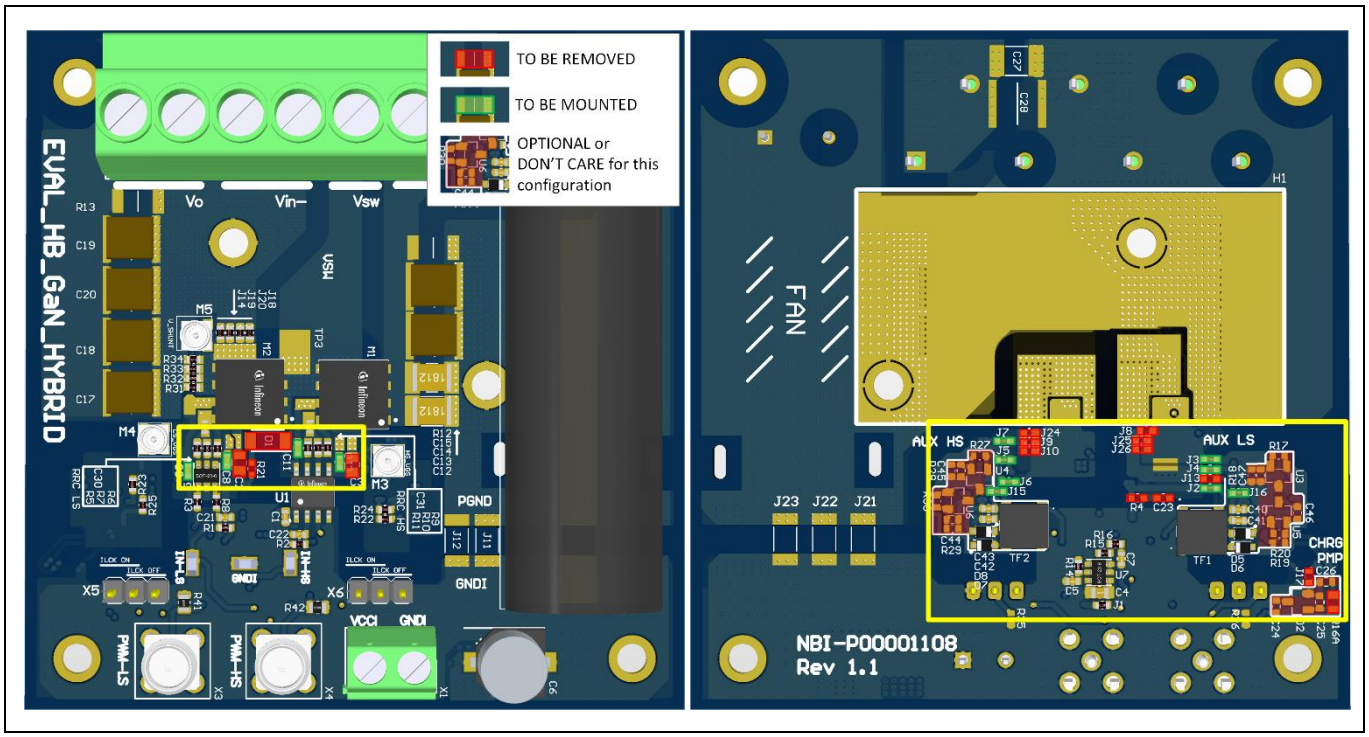


Figure 9 Jumper placement for Config. B – isolated auxiliary bipolar bias supply

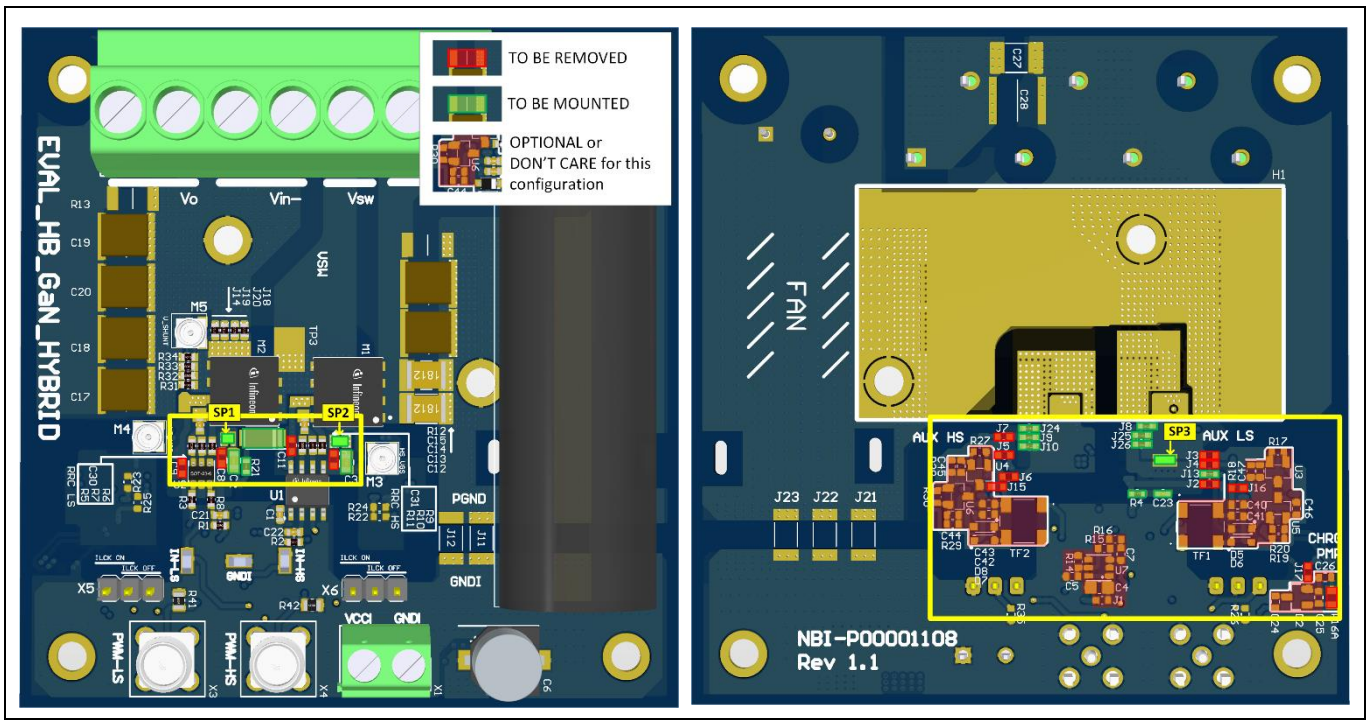


Figure 10 Jumper placement for Config. C – unipolar bootstrap bias supply

2.3 STP via interlocking

The EVAL_HB_GAN_HYBRID board features STP by interlocking the HS and the LS GaN HEMTs. The two-jumper switches X5 and X6 control the STP as described in Table 4.

Table 4 Interlocking truth table

Jumper switch status		Interlocking status
X5 – LS interlock	X6 – HS interlock	
OFF	OFF	STP OFF
OFF	ON	STP ON *HS PWM ignored (lower priority) during overlapping PWMs*
ON	OFF	STP ON *LS PWM ignored (lower priority) during overlapping PWMs*
ON	ON	STP ON *Both HS and LS switch OFF during overlapping PWMs*
High-Z state of X5 and X6 is not allowed and must be avoided		

Note: Do not leave the connectors X5 and X6 without jumpers because High-Z condition is not allowed.

2.4 Access and measurement points

Table 5 reports the access points on the board through which PWM signals and power can be provided. Figure 11 shows their location on the PCB. The connector name is also reported on the board silkscreen.

Table 5 Access points and connectors

Access point	Description	Comments
X1	V_{DDI} power supply connector	
X2	Seven-port power connector	Connect according to required setup as described in Section 2.1
X3	SMA connector – LS switch PWM	Terminated 50 Ω via R41
X4	SMA connector – HS switch PWM	Terminated 50 Ω via R42
X5	Interlocking selector – LS switch	Please see Section 2.3
X6	Interlocking selector – HS switch	

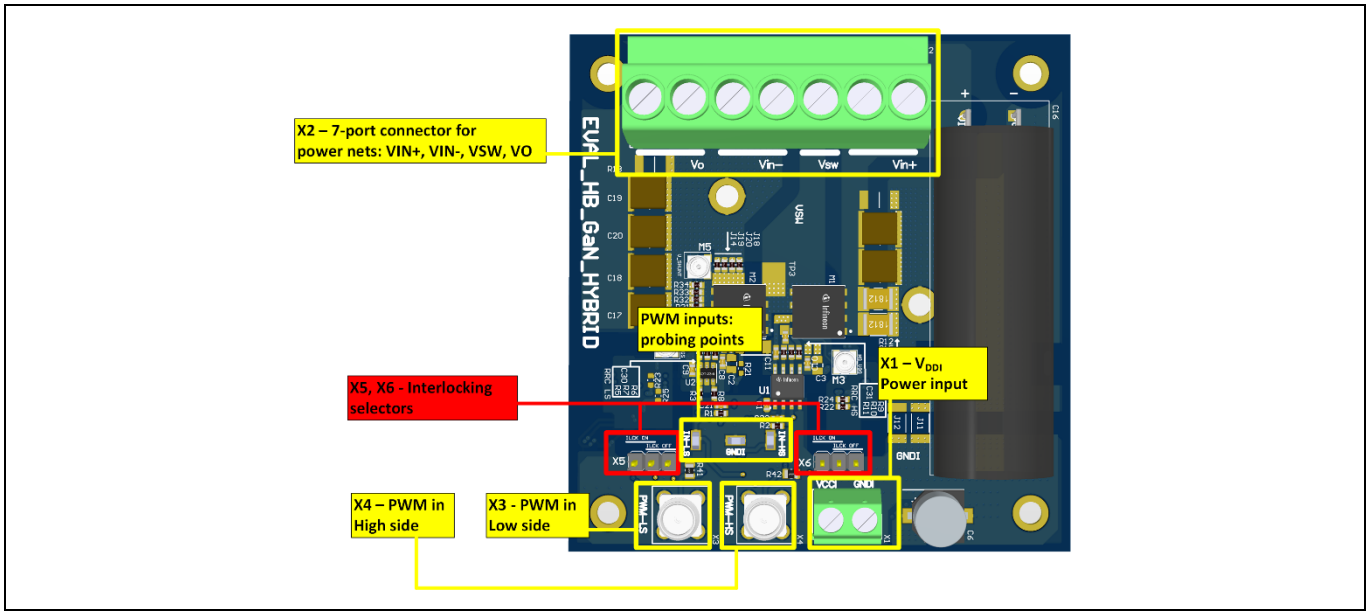


Figure 11 PCB location of the access points and connectors

Table 6 shows the measurement points available on the board through which the resulting signals can be measured. The suggested measurement setup/configuration is also indicated. Figure 12 shows the location on the PCB.

Note: The following considerations are employed for all the measurements shown in this application note, unless otherwise specified. Ensure that the scope ground is connected to an isolated supply.

Table 6 Measurement points and suggested probes

Measurement point	Associated signal(s)/net(s)	Comments	Suggested probe/setup
TP1A	V_{G_LS} LS gate contact	Soldermask openings [1]	1 GHz, 300 V passive probe (e.g., Tektronix TPP1000)
TP1B	V_{KS_LS} LS Kelvin source contact		Scope ground
TP2A	V_{G_HS} HS gate contact		Recommended to use M3. If needed, use a HV isolated differential probe.
TP2B	V_{KS_HS} HS Kelvin source contact		
TP3	V_{SW} switching node contact		400 MHz, HV passive probe (e.g., PHV1000 or TPP0850)
M2	V_{S_LS} LS source contact		Alternative GND access point
M3	V_{G_HS} to V_{KS_HS} HS gate-to-source voltage	MMCX connector, grounded to V_{SW}	1 GHz isolated HV differential probe (e.g., Tektronix TIVP1)
M4	V_{G_LS} to V_{KS_LS} LS gate-to-source voltage	MMCX connector, grounded to V_{S_LS}	1 GHz, 300 V passive probe (e.g., Tektronix TPP1000)
M5	GND to V_{S_LS} shunt voltage (8 x 1 Ω resistors)	MMCX connector, grounded to V_{S_LS}	1 GHz, 300 V passive probe (e.g., Tektronix TPP1000)

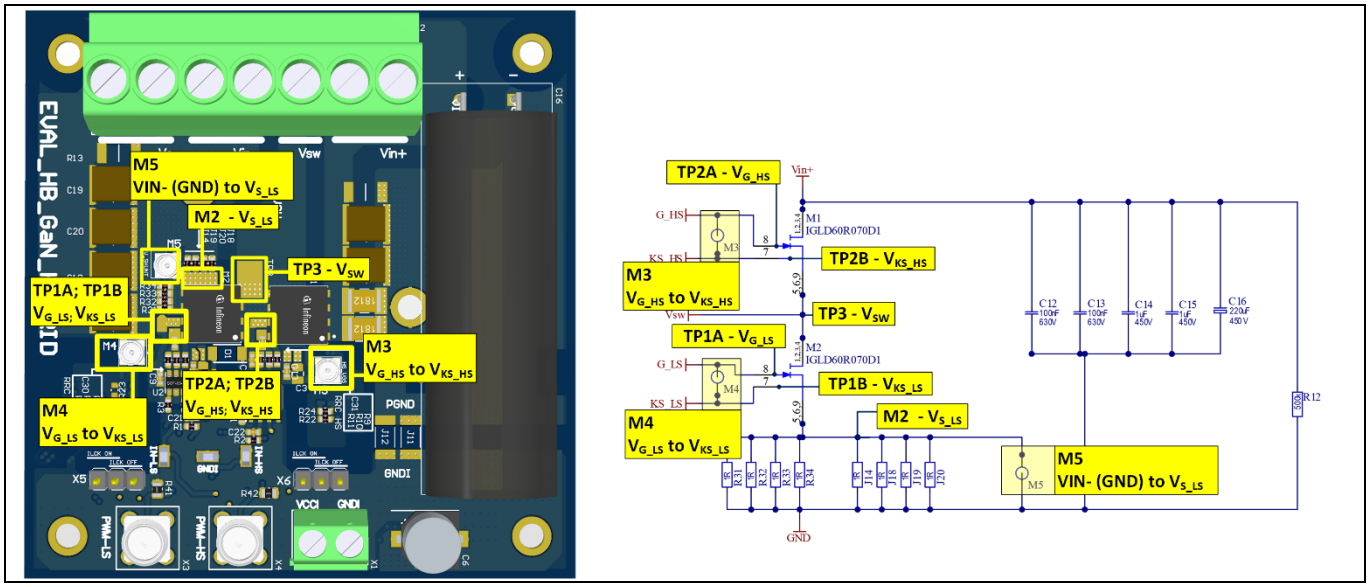


Figure 12 PCB location of the measurement points

[1] **Soldermask openings:** To measure these signals, it is suggested to solder a small one-pin receptacle for each soldermask opening, and use the tip and barrel method to minimize the grounding loop. The probe and the ground terminals can be inserted into the two receptacles, also acting as probe holders.

3 The hybrid driving concept

The introduction of wide-bandgap (WBG) semiconductors and the associated increase of switching speeds requires careful optimization of the PCB layout to minimize parasitic inductances in both driving loop and power loop. To achieve this target while keeping the solution low cost, a two single-channel gate driver ICs approach can be followed in order to have convenient placement of the drivers and reduce the distance in between the driver IC and the switch being driven.

The proposed hybrid driving concept is enabled by the isolated EiceDRIVER™ 1EDB7275F and the non-isolated TDI EiceDRIVER™ 1EDN7550B gate drivers. The isolated EiceDRIVER™ 1EDB7275F drives the HS switch, and the non-isolated TDI EiceDRIVER™ 1EDN7550B drives the LS GaN HEMT.

Similar propagation delays over the whole temperature range make possible the use of two different gate driver ICs to have an optimized layout of the driving stage, while keeping the solution cost-effective by replacing the isolated LS driver (see [2]) with a TDI gate driver IC.

Figure 13 shows the hybrid driving concept in EVAL_HB_GAN_HYBRID to drive CoolGAN™ GIT HEMTs. The board also allows testing of GaN HEMTs from other vendors, provided that VDDx and VSSx are properly configured according to the switch V_{GS} requirements.

It is important to notice that a similar driving approach can be followed to drive SiC- and Si-based power stages if there is no need for galvanic isolation.

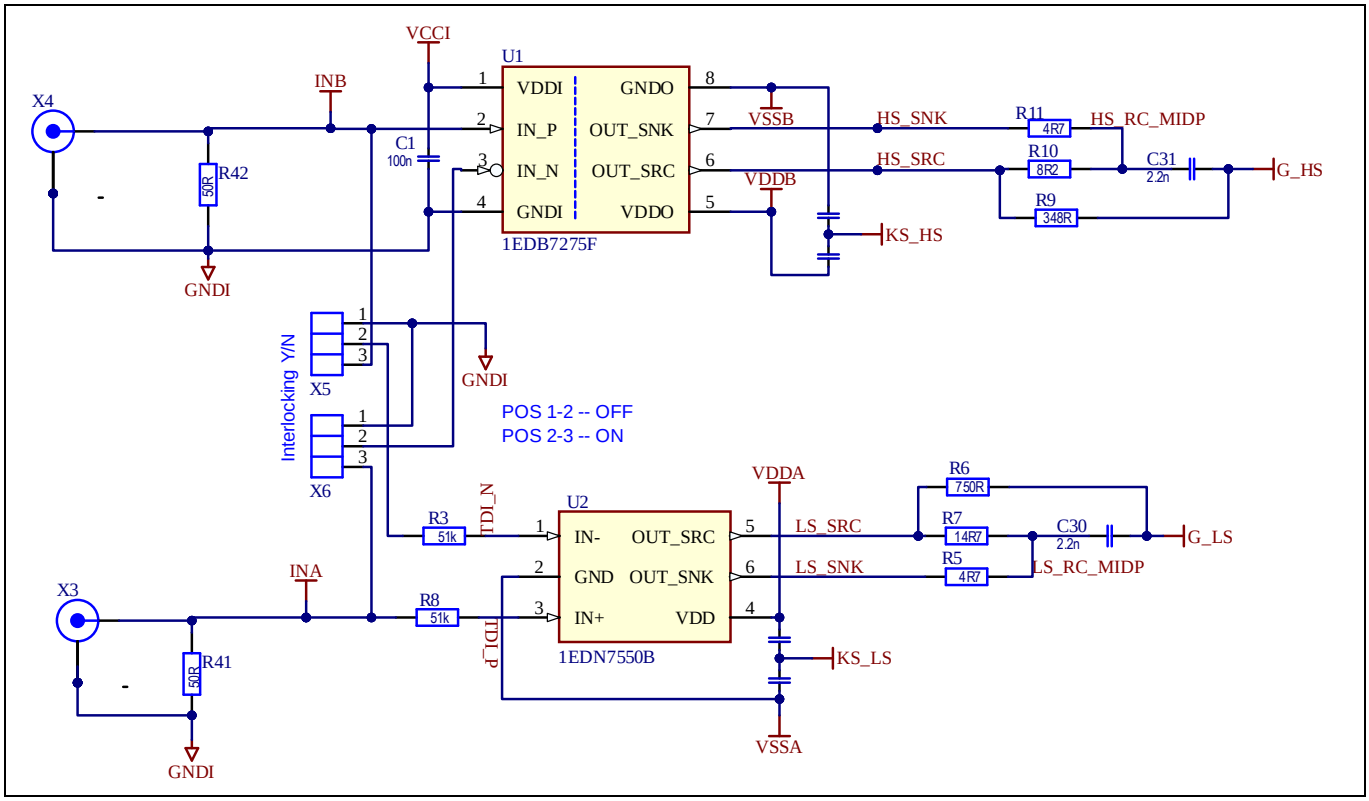


Figure 13 Simplified schematic of the hybrid driving configuration for GaN HEMT (Config. A is shown)

3.1 Configuring the bias supply voltage

The following bias supply circuits are available on EVAL_HB_GAN_HYBRID:

a) Open-loop isolated auxiliary supply – for both HS and LS switches

b) Post-regulated isolated auxiliary supply – for both HS and LS switches

c) Post-regulated negative voltage via CP – for LS switch

Solution a) is discussed in Section 3.1.1, and solutions b) and c) exploit a similar local shunt regulation, and are discussed together in Section 3.1.2.

3.1.1 Isolated open-loop bias supply

The isolated auxiliary bias supply circuit shown in Figure 14 realizes a simple and cost-effective galvanically isolated DC-DC converter. It can be used to deliver power while keeping galvanic isolation for both HS and LS switches, as reported for Config. A and Config. B.

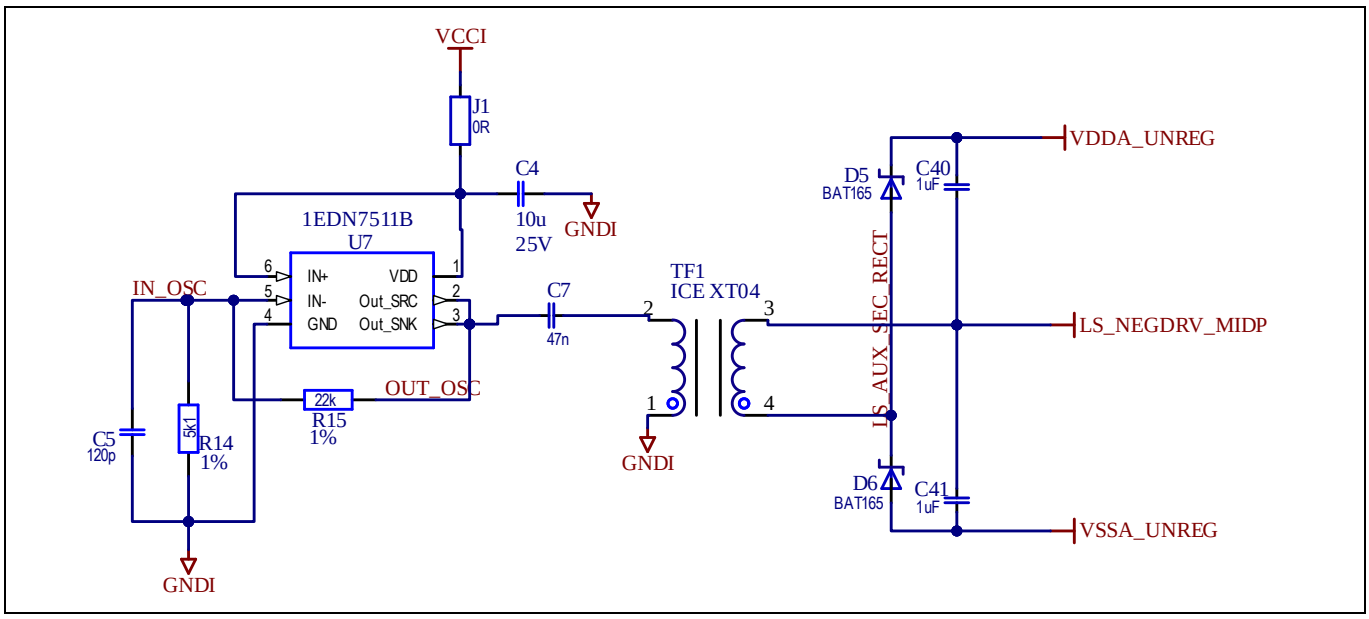


Figure 14 Simplified equivalent schematic of the isolated auxiliary supply

A single-channel LS gate driver EiceDRIVER™ 1EDN7511B operates as a free-running oscillator by providing feedback to the inverting pin IN-. The driver output OUT_OSC therefore switches as a result of the charging/discharging of C5 connected to IN_OSC: when the voltage at IN_OSC hits the driver comparator thresholds V_{INH} = 2.1 V and V_{INL} = 1.0 V, the output changes state accordingly. Using the internal trimmed thresholds of the EiceDRIVER™ 1EDN7511B allows for stable and predictable behavior of the circuit over temperature.

Galvanic isolation can be achieved by the ICE XT04 transformer, which features a small size and low interwinding capacitance (less than 4 pF) to enable high dV/dt of WBG switches, and provides 3 mm creepage between the primary and secondary sides.

The output voltage of the bias supply in open-loop configuration as in Figure 14 is set by the duty cycle of the voltage on the primary side of the transformer. Post-regulation is not needed in this case, which further reduces the component count and therefore costs. Indeed, the open-loop configuration is good enough for GIT GaN

HEMTs like CoolGaN™, which do not require overvoltage protections to prevent gate damage due to their self-clamping gate behavior.

If necessary, the oscillator frequency can be changed by acting on R14, R15 and C5, and the bias voltage rails can be varied by changing the duty cycle via tuning of R14. The default configuration as shown in Figure 14 uses V_{DDI} = 12 V and provides two bias supply rails with +8 V/-4 V output. A different split of V_{DDx}/V_{SSx} can be obtained by changing the duty cycle via R14 only, as reported in Table 7.

A full characterization of the isolated auxiliary supply circuit for GaN HEMTs can be found in [4].

Table 7 Dimensioning of R14 vs. required bias voltage and available V_{DDI}

Required bias supply rails		V_{DDI} available on TF1 primary	R14 value to set
V_{DDx}	V_{SSx}		
+8 V	-4 V	+12 V	5.1 kΩ[1]
+8 V	-6 V	+15 V	4.3 kΩ
+9 V	-5 V	+15 V	3.9 kΩ

3.1.2 Post-regulation of the bias voltage

In some cases, post-regulation of the voltage could be needed in order to supply the gate driver ICs with a very precise voltage level. For instance, it could be required to get tight +/-1 percent accuracy on the positive bias rail when using SG GaN HEMTs (to prevent gate damage) or to regulate the negative voltage rail for the LS switch if generated via CP, as reported in Config. A of Figure 7.

If tight accuracy is required for V_{DDx} and V_{SSx}, post-regulation is possible via TL431 (see RefDes U3 and U5, reported in the full schematic Figure 43).

In these cases, a simple shunt regulator like TL43x can be used to provide a more precise supply voltage, suppress potential transients applied to the gate, or deal with dropout voltage when generating the negative rail with a CP circuit.

3.1.3 Negative LS bias voltage via CP

A simplified equivalent schematic, including the CP circuit for the generation of the negative driving voltage for the LS switch, is shown in Figure 15. On the EVAL_HB_GAN_HYBRID board, the post-regulation circuit of the LS auxiliary supply can be reused in order to regulate the negative driving voltage.

The CP circuit uses the capacitor C24 to reverse the polarity of the V_{CCI} voltage. As a result, the open-circuit output voltage of the CP without post-regulation tends to $V_{CP,OPEN} \approx -|V_{CCI}|$, and its dynamic behavior depends only on the switching frequency of the driver, provided that the RC constant of the CP circuit is much lower than the on-time duration.

[1] This configuration can be used, with proper post-regulation, to supply +5 V on the positive bias supply rail for SG GaN HEMTs.

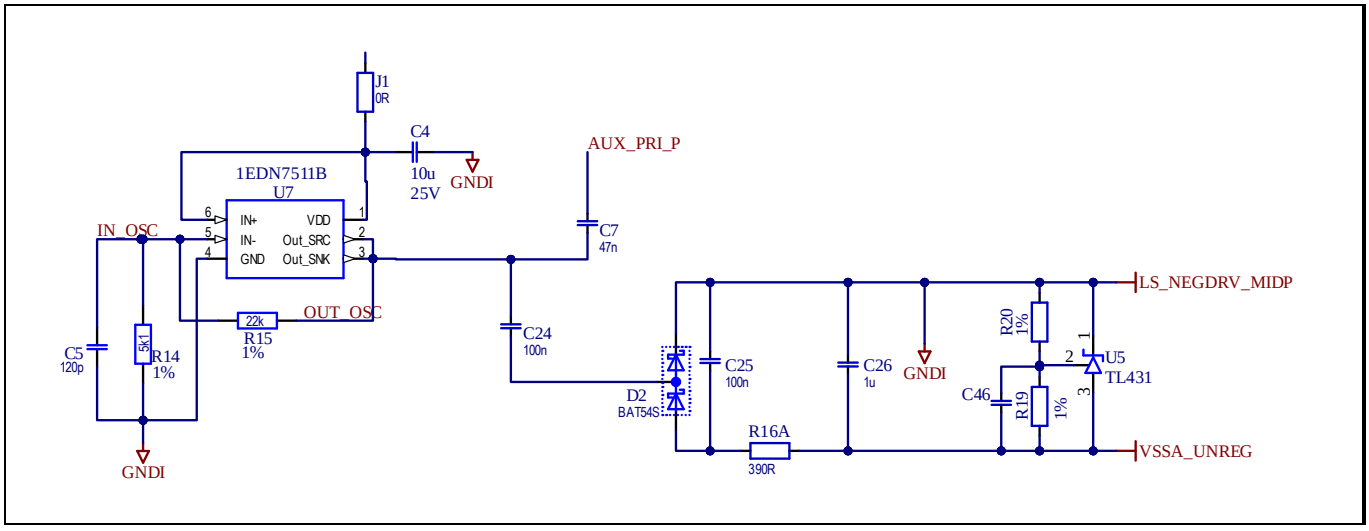


Figure 15 Simplified equivalent schematic of the CP circuit with post-regulation (Config. A)

The post-regulation circuit can be applied also to the secondary side of the isolated auxiliary supply to improve regulation in case of the need for 1 percent accuracy on the bias supply.

The proposed CP circuit is capable of providing the required -4 V negative voltage for the LS switch without the need for an isolation transformer TF1, as reported in **Figure 15**. The efficiency of the CP circuit is mainly dominated by the shunt post-regulation circuit, and is reported for various values of the flying capacitor C24 and shunt resistor R16A for V_{CCI} = 12 V and V_{SSA} = -4 V.

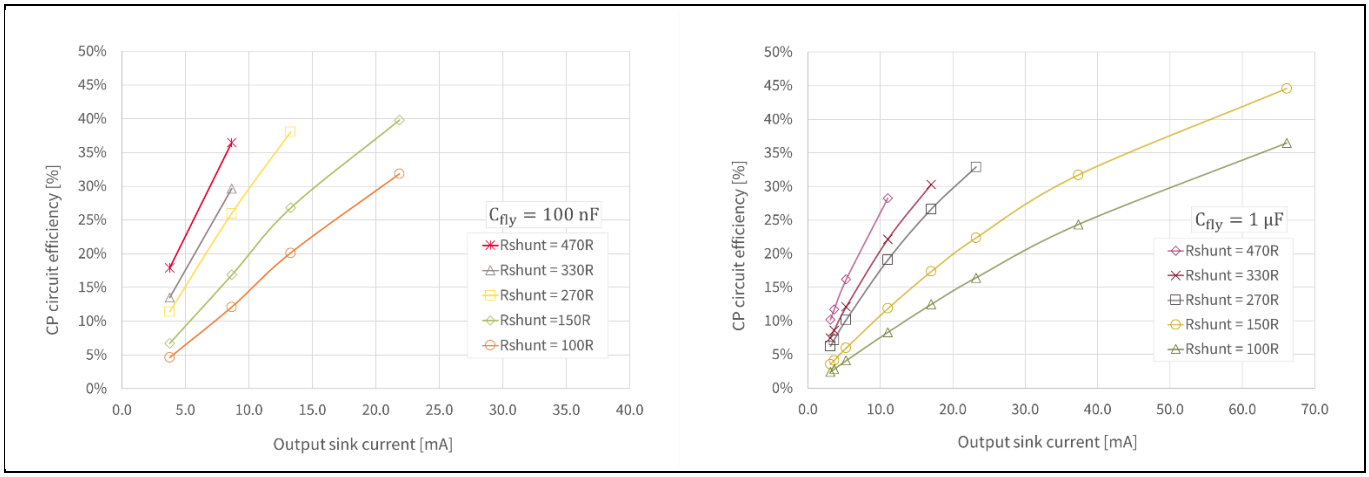


Figure 16 CP circuit efficiency for V_{CCI} = 12 V, V_{SSA} = -4 V for flying capacitor C24 and shunt resistor R16A

Considering that GaN HEMTs drain little power at turn-off from the negative bias supply, the CP circuit could be optimized and dimensioned for the required amount of current, to maximize efficiency and keep the impact on the overall SMPS efficiency negligible: 100 nF C_{fly} and 390 Ω R_{shunt} have been selected to maximize the efficiency at maximum expected output power (i.e., 40 mW at 1 MHz switching frequency).

Since isolation is not required, the positive bias supply for the LS switch can be directly provided via V_{DDI} after proper filtering, as shown in the schematic.

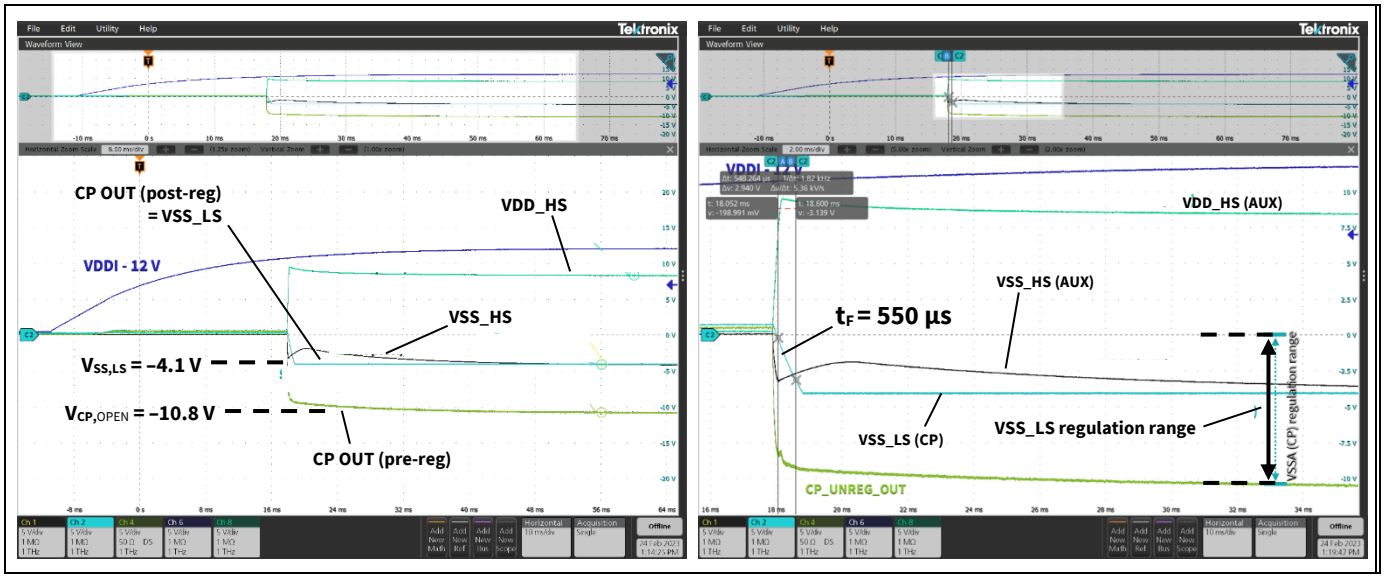


Figure 17 Hybrid bias power supply during start-up (left) and zoomed transient (right)

The VSSA voltage provided via CP circuit can be tuned as long as |VSSA| is less than |CP_UNREG_OUT|, which is the negative voltage provided by the circuit. Power dissipation at corner case temperatures must be analyzed, and the proper power rating should be selected for R_{shunt} to ensure effective power dissipation.

It is also important to notice that VSSA is available within 550 µs from V_{DDI} start-up, ensuring proper negative bias before the power stage starts switching.

3.2 Equalization of HS and LS driving with hybrid bias voltage

When providing the positive bias supply to the LS switch via V_{DDI} = 12 V, and HS switch via V_{DDB} = 8 V the gate currents to enhance CoolGaN™ GIT GaN HEMT are different for the LS and the HS switches if the same R_{SS} is used. Therefore, an asymmetric RC circuit is required for this specific configuration. Examples of RC circuit values that can be adopted for EVAL_HB_GAN_HYBRID at different positive bias rails are reported in Table 8.

Table 8 Example of RC circuit configurations when using different bias voltage levels

Switch	Configuration	Bias supply generation	Bias supply		R_{SS} (R6, R9)[1]	R_{SOURCE} (R7, R10)[1]	R_{SINK} (R5, R11)[1]	C_C (C30, C31)[1]
			VDDx	VSSx				
HS	A	ISO AUX	8 V	-4 V	348 Ω	8.2 Ω	4.7 Ω	2.2 nF
LS		V_{DDI} + CP	12 V	-4 V	750 Ω	14.7 Ω	4.7 Ω	2.2 nF
HS	B	ISO AUX	8 V	-4 V	470 Ω	14.7 Ω	4.7 Ω	2.2 nF
LS								

The R_{SS}, the R_{SOURCE} and C_C are the main parameters to be tuned in the RC GaN driving circuit. To fine-tune the GIT GaN RC circuit of CoolGaN™ HEMTs, a reference guide is included in [5]. The main formulas to calculate R_{GG} and C_C are reported below for the reader's convenience.

$$R_{SS} = \frac{V_{DDx} - V_{fw}}{I_G} \qquad \text{[Eq. 1]}$$

[1] RefDes refers to Figure 13.

$$V_{GS,OFF} = -|V_{SSx}| - \frac{C_C \cdot (V_{DDx} - V_{GS}) - Q_{Geq}}{C_C + C_{GS}} \quad \text{[Eq. 2]}$$

Where V_{FW} is the GIT gate diode forward voltage drop at I_G gate current during on-state, V_{DDx} and V_{SSx} are respectively the positive and the negative bias supply rail voltages for the HEMT (HS or LS), Q_{Geq} is an application-specific equivalent gate charge (i.e., $Q_{Geq} \approx Q_{GS} + Q_{GD}$ for hard-switching, $Q_{Geq} \approx Q_{GS}$ for soft-switching transitions) and C_{GS} gate-source capacitance of the considered HEMT [9].

The required I_G can be selected from the HEMT characteristics. A gate current of ≈15 mA minimum has been chosen to properly enhance the channel of the GaN HEMT. Figure 18 shows $I_G(V_{GS})$ and $R_{DS(on)}(I_D, I_G)$ for CoolGaN™ IGLD60R070D1, and a clear $R_{DS(on)}$ benefit is shown when moving to more than 10 mA gate current.

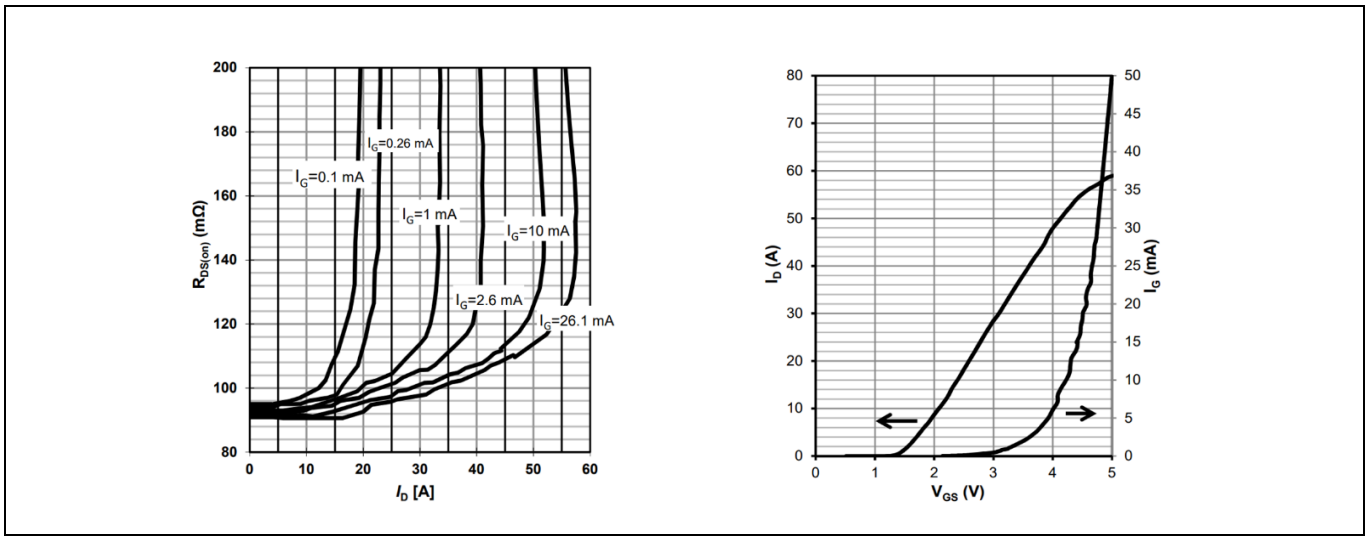


Figure 18 Typical $R_{DS(on)}(I_D, I_G)$ on-resistance (left), and $I_G(V_{GS})$ (right) for IGLD60R070D1 at 125°C

3.3 Current consumption of the hybrid driving stage

Current consumption of the driving stage with Config. A over frequency is shown in Figure 19.

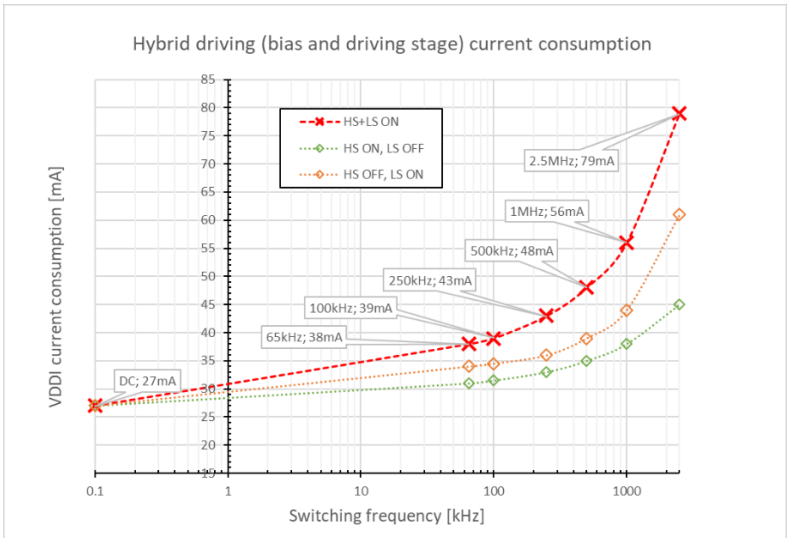


Figure 19 Current consumption hybrid driving: Config. A with V_{DDI} = 12 V, driving IGLD60R070D1. No DC-link voltage applied to the power stage.

3.4 STP via interlocking

The EVAL_HB_GAN_HYBRID has inherent interlocking functionality that ensures the device safely turns off if PWM signals are overlapping at the gate driver input(s). This feature can be implemented due to the good propagation delay matching of EiceDRIVER™ 1EDBx275F and 1EDNx550B both at 25°C and over temperature, as shown in Figure 20. Thanks to minimal difference in delays, safe operation can be ensured via interlocking of PWM signal for STP.

The four possible interlocking modes to implement STP are discussed in Section 2.3, and Figure 21 shows the V_{GS} wafevorms in all the four cases.

Note: Do not leave the connectors X5 and X6 in High-Z state without jumpers.

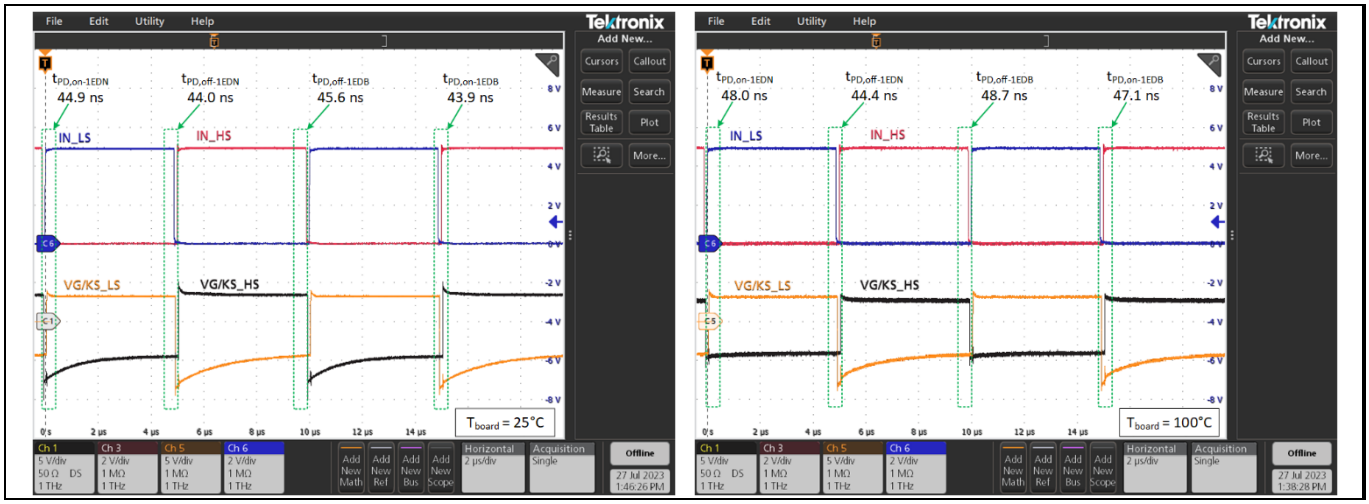


Figure 20 Propagation delay temperature variation: delays at 25°C case temperature (left) and 100°C case temperature (right) for EiceDRIVER™ 1EDN7550B and 1EDB7275F

Figure 21 PWM inputs and driving voltages with different interlocking configurations

4 Double-pulse test

Attention: ***Since no output overcurrent protection is available on the board, please ensure the PWM pattern is properly chosen (T_{ON}, T_{OFF}, DTs) to keep switch and inductor currents within ratings. Cross-conduction can be avoided by enabling STP functionality via interlocking.***

4.1 Reference waveforms

Figure 22 shows a waveform overview during double-pulse test (setup in Figure 3) and reverse double-pulse test (setup in Figure 4), respectively. Tests are executed with Config. A – hybrid bias supply, 400 V bus voltage and 50 µH load inductor to replicate testing conditions in [2].

In double-pulse and reverse double-pulse configurations, the board can be used to check the switching waveforms and tune the RC circuit according to the switching transients required.

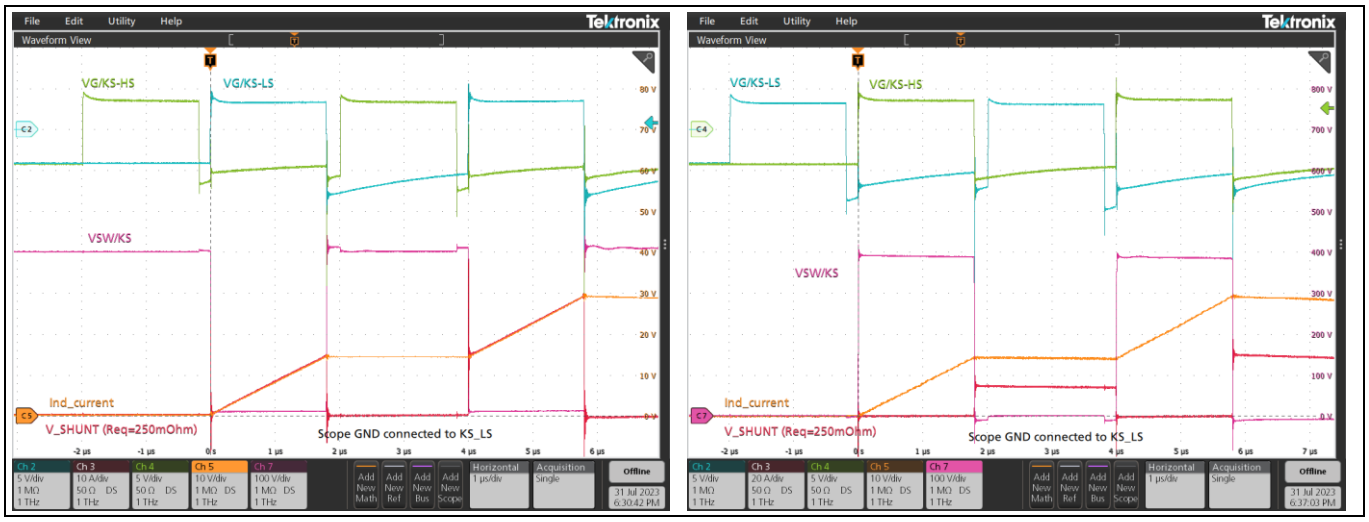


Figure 22 Double-pulse (left) and reverse double-pulse (right) test results. Test inductor L_{OUT} = 50 µH.

Zoomed waveforms during reverse double-pulse are shown as example in Figure 23 and Figure 24. The switching node is represented in violet (Ch.7) and LS GaN source current in orange (Ch.5). The switching node slew rate (dV/dt) is measured from 20 to 80 percent of the bus voltage.

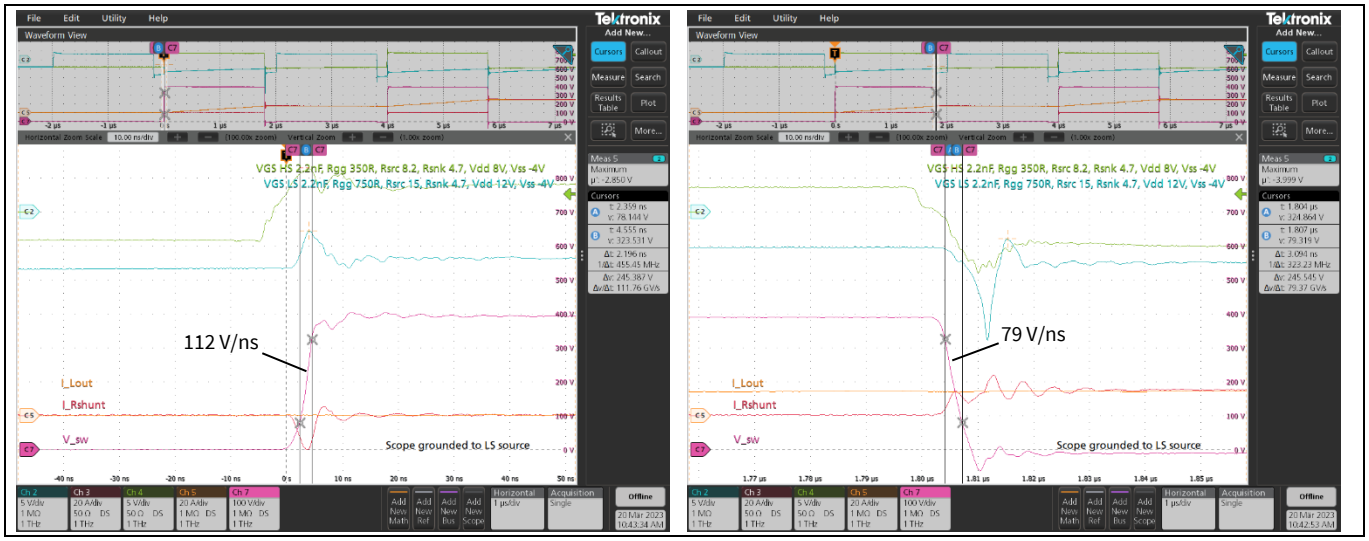


Figure 23 Reverse double-pulse test – first and second pulses

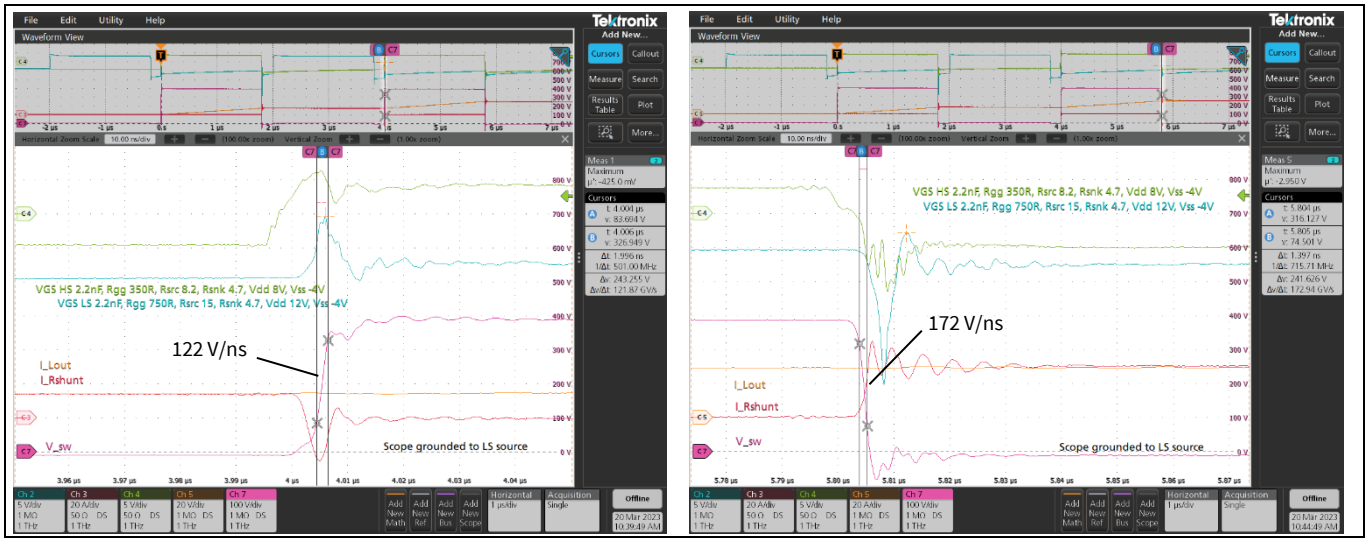


Figure 24 Reverse double-pulse test – third and fourth pulses

4.2 Considerations on negative V_{GS} driving with hybrid configuration

In the reverse double-pulse test the HS GaN HEMT is the active device and therefore it experiences hard-switching turn-on, while the LS GaN HEMT is in diode mode during the DT. Consequently, the LS HEMT could experience a voltage rise on the $V_{gs,LS}$ during turn-on of the HS HEMT due to Miller effect and consequent displacement currents in the $C_{gd,LS}$ capacitances, especially during the first pulse and hard turn-on commutations. Figure 25 shows these two worst cases, and how negative driving is effective in keeping the $V_{gs,LS} < 0$ V to avoid re-turn-on.

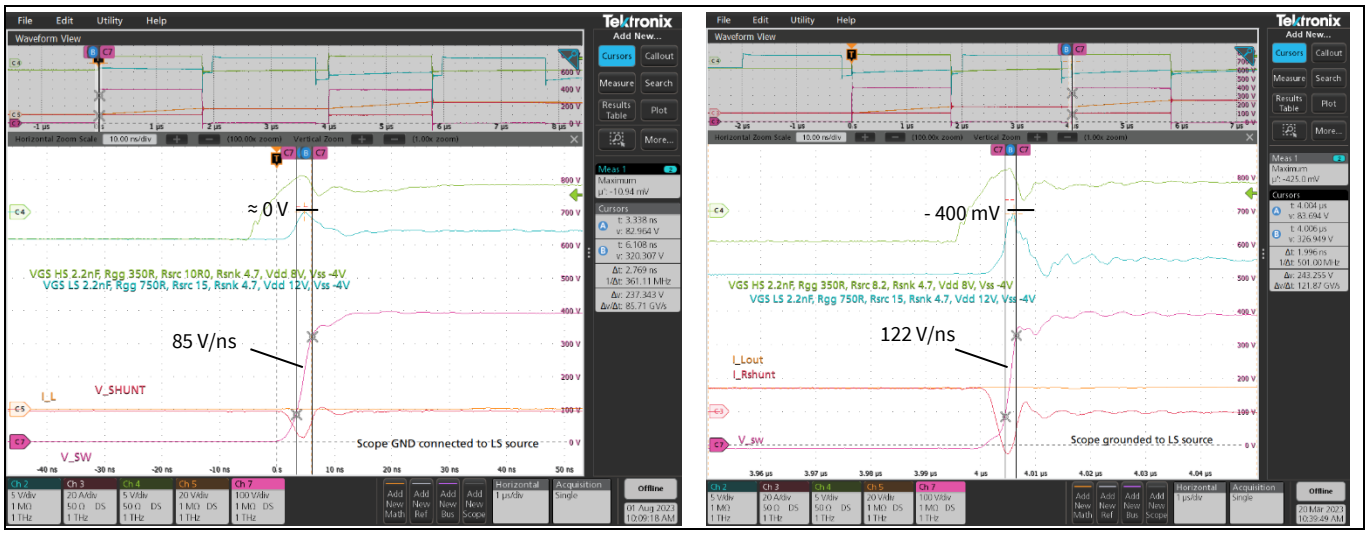


Figure 25 Overvoltage on the $V_{GS,\,LS}$ during first and third hard commutations

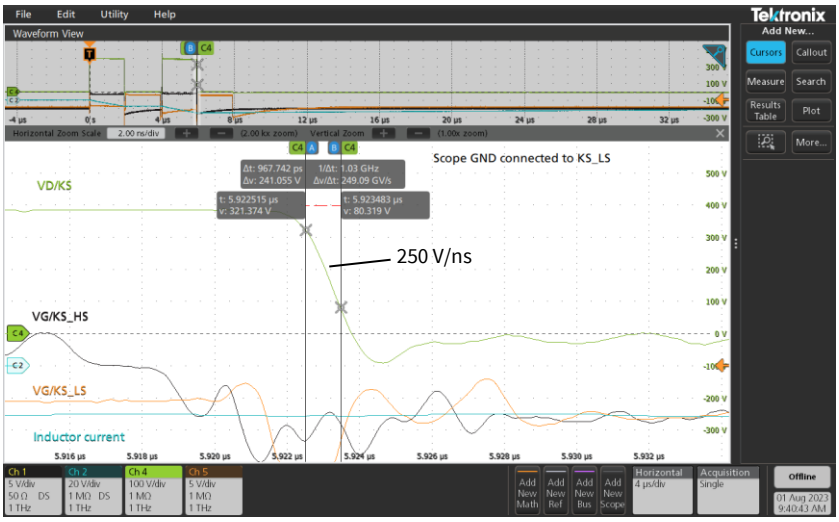


Figure 26 Maximum dV/dt achieved with hybrid configuration and proposed layout[1]

The very high common mode transient immunity (CMTI) of EiceDRIVER™ 1EDB7275F (more than 300 V/ns), the TDI capability of the EiceDRIVER™ 1EDN7550B and high dV/dt of CoolGaN™ IGLD60R070D1 (200V/ns) allow very high switching speeds. With the proposed layout (Appendix B: Layout) that minimizes gate drive loop inductance, 250 V/ns has been proven (Figure 26).

The high dV/dt level achieved in absence of parasitic re-turn-on effects proves that the hybrid driving solution is robust and allows high switching speeds (for instance to reduce switching losses during hard commutations).

4.3 Detecting shoot-through

By making use of the shunt resistors J14, J18, J19, J20, R31, R33, R34, and R35 it is possible to estimate if the power stage is experiencing cross-conduction by checking the total charge, as discussed in Section 3.2.3 of [2].

An example of waveform to check shoot-through in the GaN power stage is reported below. During each transition, Q_{OSS} can be measured by integrating the shunt current with the “Area” option between the cursors on the scope to check for shoot-through scenarios.

In Figure 27 the Q_{OSS} charge is detected and measured during the fourth pulse, leading to $Q_{OSS,meas}$ = 62 nC. This value is slightly higher than $Q_{OSS,DS}$ = 47 nC as specified in [10]. The excess contribution comes from the charge of the parasitic capacitances on the switching node. This means shoot-through is not happening for the selected transition.

The shunt current can be measured by accessing directly with a passive probe a MMCX connector (M5) with Kelvin connection to the shunt resistors listed above.

Note: The probing point M5 is referenced to the Kelvin-source (KS) contact of the LS switch, therefore M5 provides the GND (V_{IN-}) to KS_LS voltage, as shown in Figure 44.

[1] Note: in this and all the following measurements, the inductor current is measured with 1 V/A gain, unless specified.

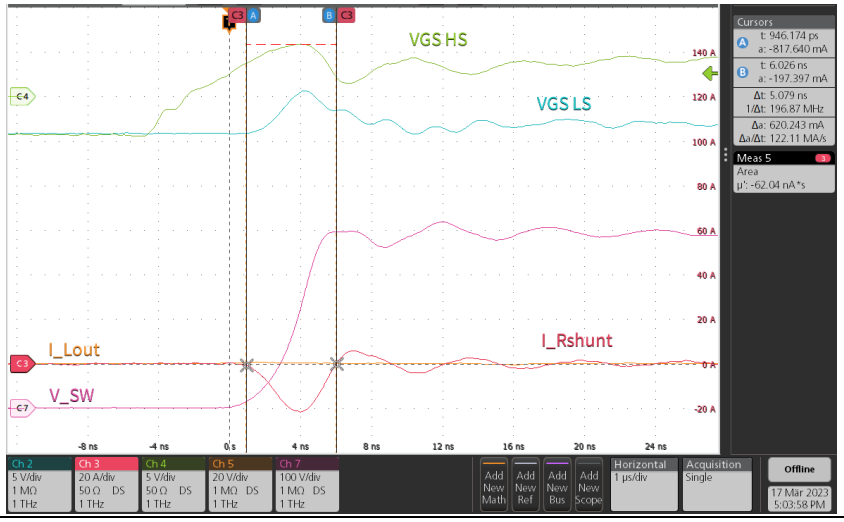


Figure 27 Charge C_{oss} detected during the fourth pulse (≈62 nC)

5 Continuous operation

Attention: ***No soft-start circuit is available on the board. The start-up sequence must be followed for continuous operation. Before applying the DC-link voltage, please ensure the PWM pattern is available at $V_{GS,\,HS}$ and $V_{GS,\,LS}$ to avoid inrush current.***

Attention: ***Please short the 1 Ω shunt resistors (J14, J18, J19, J20, R31, R33, R34 and R35) between power ground (node GND) and the source of the LS GaN HEMT (node S_LS) before executing continuous operation tests. Resistor power ratings are not suitable for steady-state.***

In the following sections, the results obtained with EVAL_HB_GAN_HYBRID in triangular current mode (TCM) buck are described. Section 5.2 shows behavior at zero DC current, and Section 5.3 shows maximum power transfer achieved at 100 kHz and 2 MHz switching frequencies with 50 µH and 5 µH test inductors, respectively.

During the following tests, the scope ground is referenced to the LS KS connection TP1B, the LS gate-KS voltage is sensed with a 300 V, 1 GHz passive probe via M4, the switching node is sensed with a 1 kV, 400 MHz passive probe at TP3, the HS gate-KS voltage is sensed with ISOVU TIVP1 1 GHz differential probe at M3, and current is measured with a 30 A, 120 MHz TCP0030 inline current probe.

A list of the probing points is provided in Table 5.

5.1 Start-up sequence

To avoid exceeding current ratings in the GaN switches and inductor saturation, it is suggested to implement the start-up sequence as shown in Figure 28. Please also ensure proper setup of the heatsink and fan operation where required.

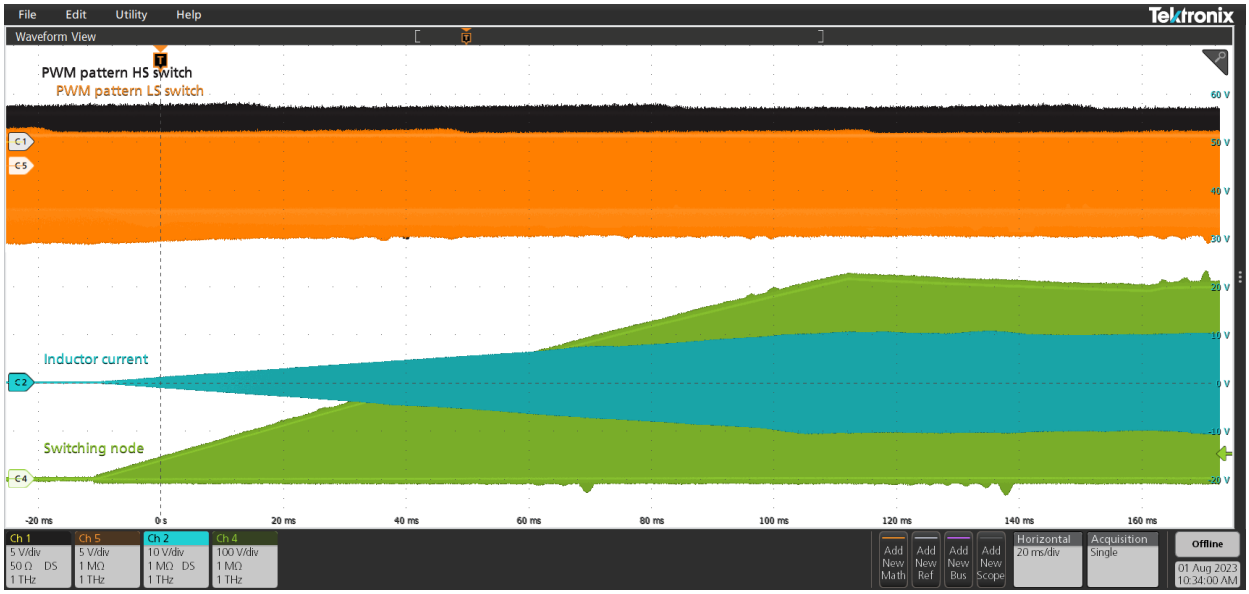


Figure 28 Example of start-up sequences with 100 kHz PWM pattern (black, orange) available before powering the DC-link (green)

5.2 TCM operation without DC load

With zero DC current drained from the V_{OUT} connector, soft-switching can be observed and compared to results in [2]. Section 5.2.1 and Section 5.2.2 report the tests performed at 100 kHz and 2 MHz switching frequency, respectively.

5.2.1 Operation at 100 kHz

First, a 100 kHz switching test was performed as depicted in Figure 29. For this test, a 50 µH filter inductor was used in series between the V_{SW} and V_{OUT} connectors as per the configuration in Figure 5. A function generator with f_{SW} = 100 kHz and duty cycle of DC = 50 percent and proper DT was used to drive the hybrid stage.

As expected, with 400 V DC bus the output settles at 200 V, the peak-to-peak current ripple in the inductor is about 20 A and the power stage experiences zero-voltage switching (ZVS). Therefore, the inductor current drives the switching node total capacitance at equal slew-rates (≈30 V/ns) from 400 V to 0 V and vice-versa.

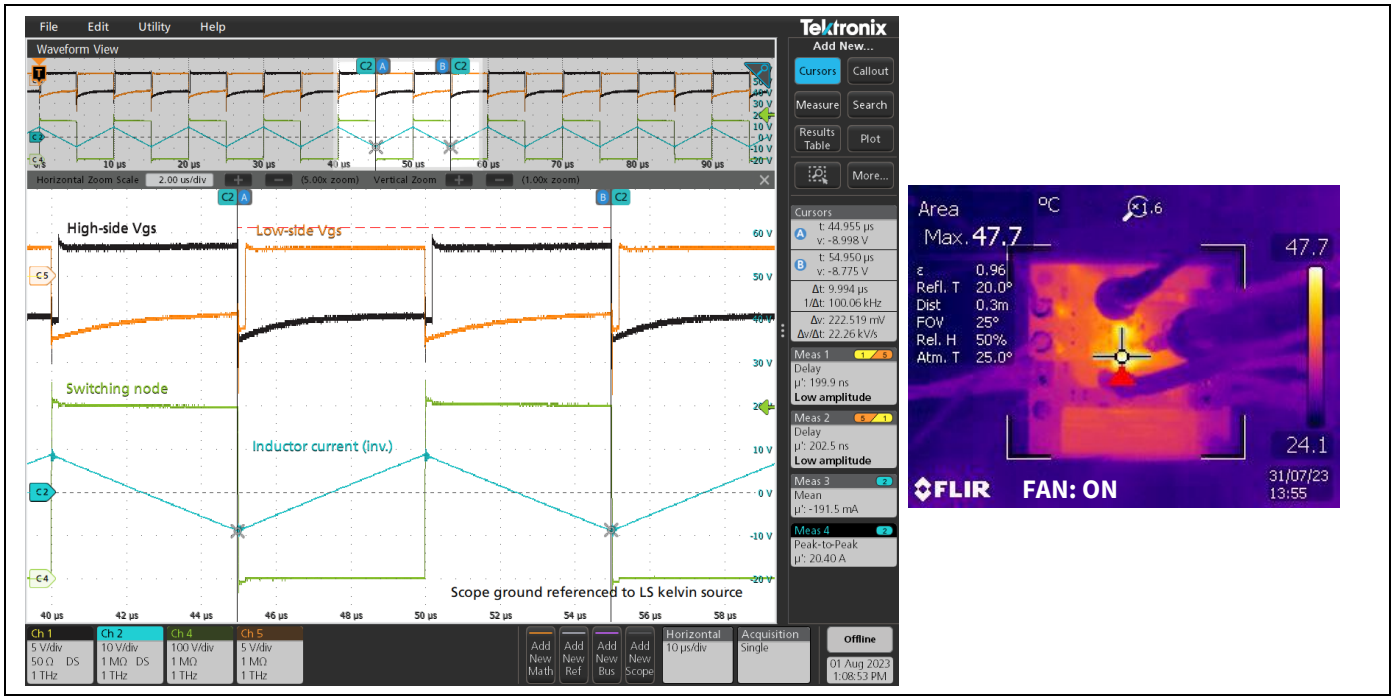


Figure 29 Soft-switching behavior at 100kHz, 200 ns DT, 50 µH inductive load, no DC output current: waveforms (left) and power stage max. temperature (right)

It must be noted that voltage spikes are present on the V_{GS} of both the HS and LS HEMTs. These events relate to the transitions of the switching node at high dV/dt through the C_{gd} and C_{gs} capacitances. As an example, for the LS a capacitive voltage divider $C_{gd}/(C_{gd} + C_{gs}) = C_{rss}/C_{iss}$ is created, resulting in positive (and negative) spikes when V_{SW} moves from 0 V to 400 V (400 V to 0 V). The HS V_{GS} experiences similar behavior.

Lastly, it is important to notice that while C_{iss} is linear over V_{DS}, C_{rss} is highly dependent on V_{DS} [10]. Indeed, the reverse transfer capacitance has constant magnitude from 400 V to 200 V, and sudden increases of about two orders of magnitudes from 200 V to 0 V, which is why the spike is shifted in the second half of the V_{DS} transition.

Figure 30 100 kHz soft-switching with 200 ns DT, inductive load 50 µH, no DC load (zoom)

5.2.2 Operation at 2 MHz

A 2 MHz switching test was performed and reported in Figure 31. For this test, a 5 µH filter inductor was used in series between the V_{SW} and V_{OUT} connectors as per the configuration in Figure 5. A function generator with f_{SW} = 2 MHz, duty-cycle of DC = 50 percent and 60 ns DT was used to drive the hybrid stage.

As expected, with 400 V DC bus the output settles at 200 V, the peak-to-peak current ripple in the inductor is about 10 A and the power stage experiences ZVS. Therefore, the inductor current drives the switching node total capacitance at equal slew rates (≈18 V/ns) from 400 V to 0 V and vice-versa.

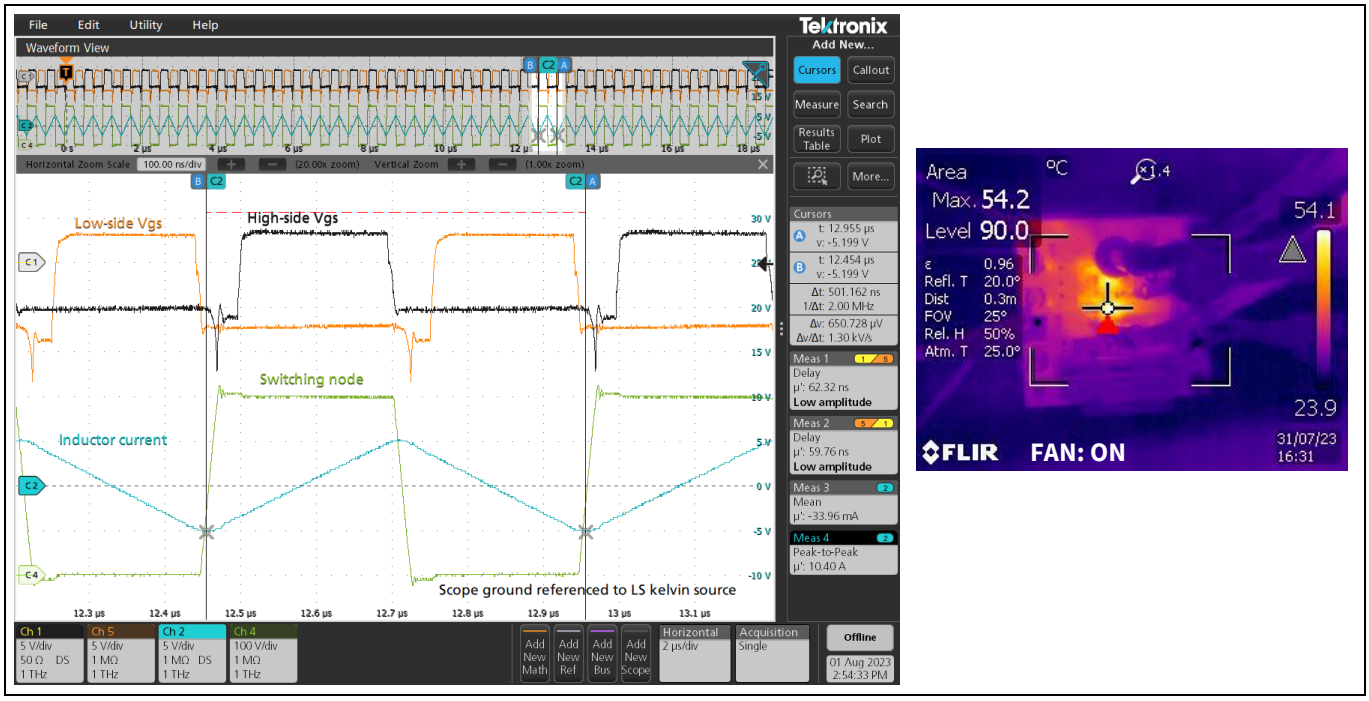


Figure 31 2 MHz soft-switching with 60 ns DT, inductive load 5 µH, no DC load: waveforms (left) and power stage max. temperature (right)

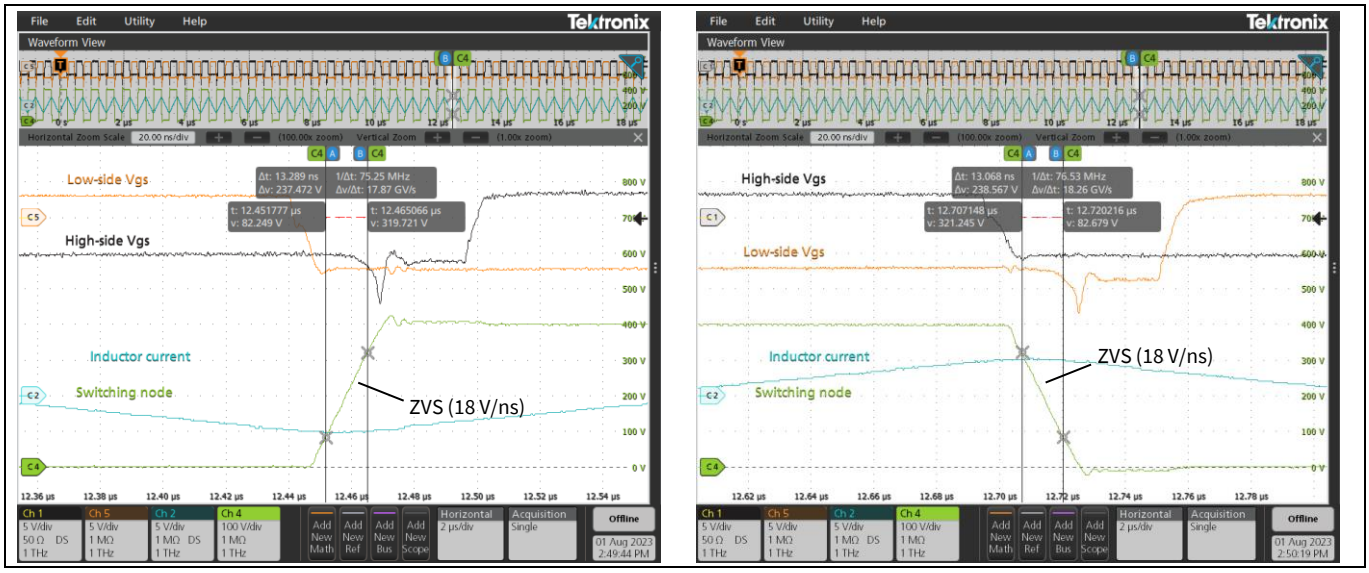


Figure 32 **2 MHz soft-switching with 60 ns DT, inductive load 5 µH, no DC load (zoom)**

5.3 TCM operation with DC load

Attention: ***Please check DTs and short shunt-sensing resistors before operating the board at higher power levels.***

By connecting a DC load to the output and configuring the external inductor as shown in Figure 5, the EVAL_HB_GAN_HYBRID board can be configured to transfer power in TCM and operate as a buck converter.

5.3.1 Operation at 100 kHz

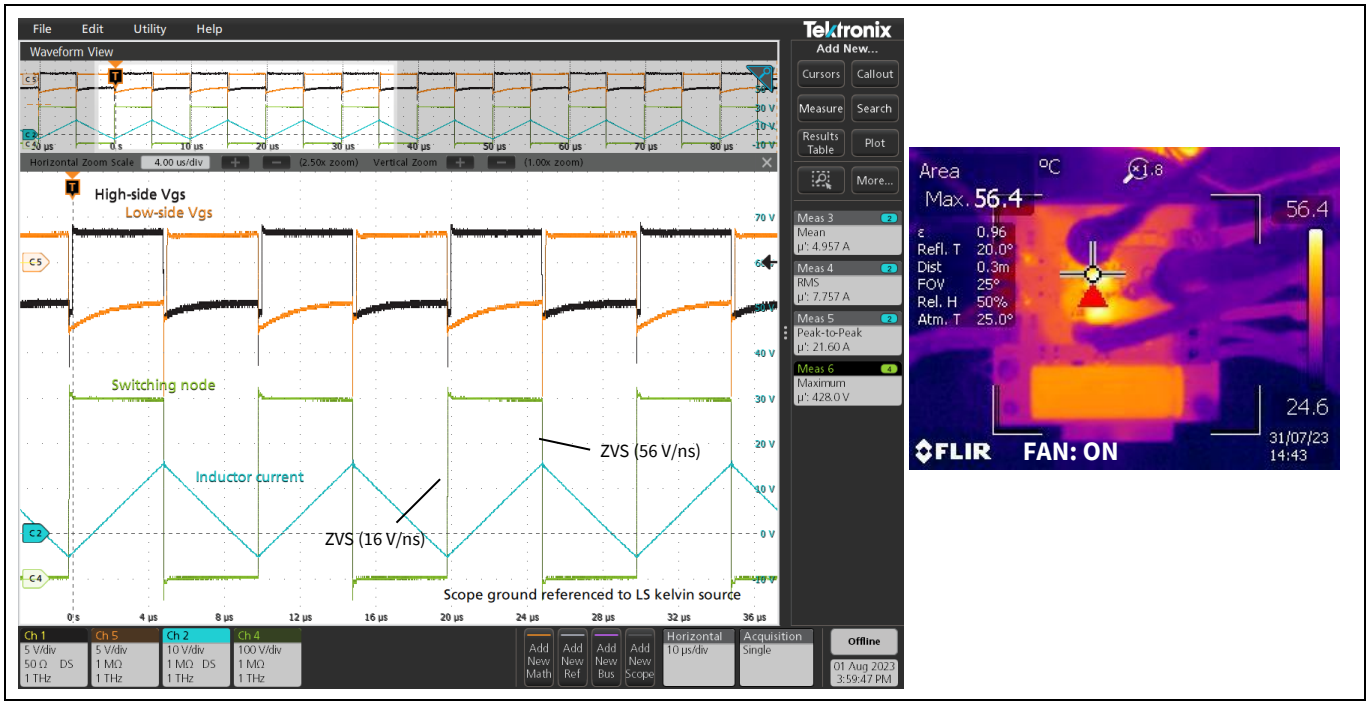


Figure 33 **TCM buck mode operation, P_{OUT} = 1 kW, f_{SW} = 100 kHz, 50 µH filter inductor: waveforms (left) and power stage max. temperature (right)**

Continuous operation

With this configuration the board can be operated at different power levels up to 2 kW output power, as shown in Figure 35. Intermediate power points at 1.0 kW and 1.5 kW are also reported in Figure 33 and Figure 34, respectively.

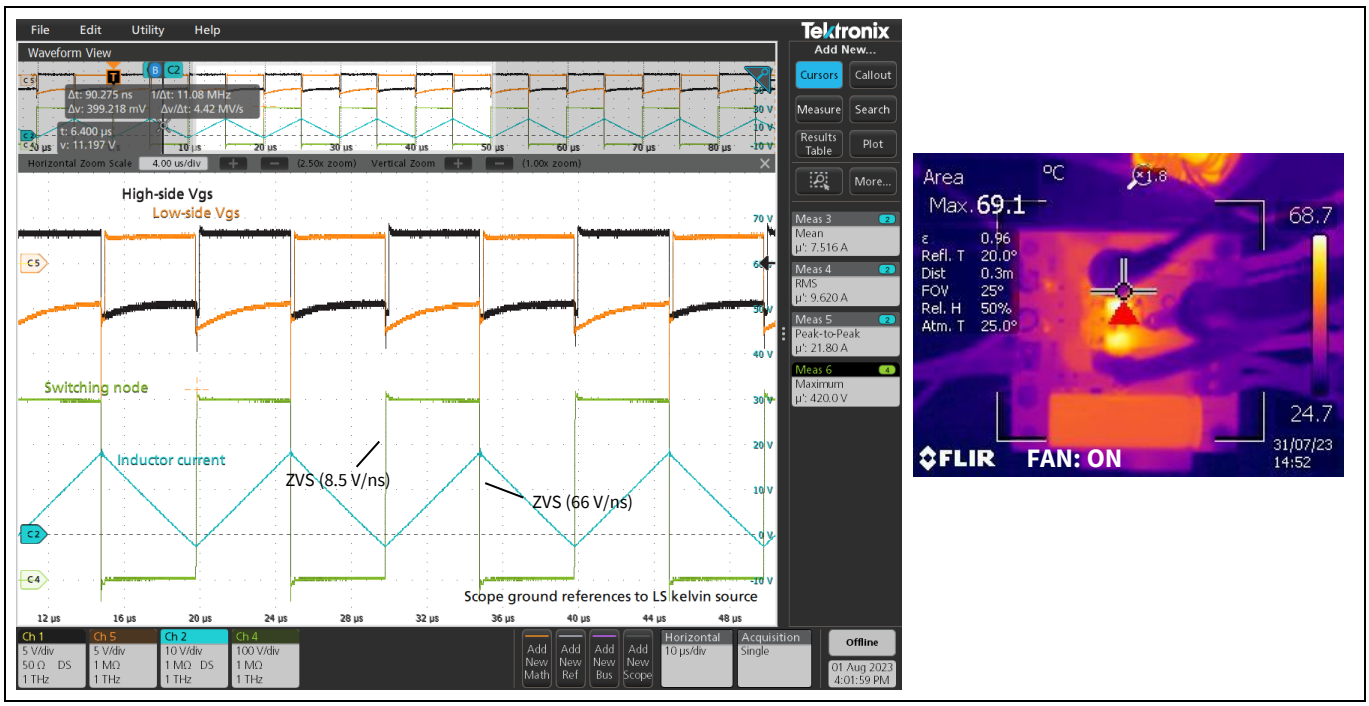


Figure 34 TCM buck mode operation, P_{OUT} = 1.5 kW, f_{SW} = 100 kHz, 50 µH filter inductor: waveforms (left) and power stage max. temperature (right)

At 2 kW output power, a partial hard-switching turn-on of the HS was observed because of the lower (negative) current at this point. DTs can be adjusted to achieve full soft-switching.

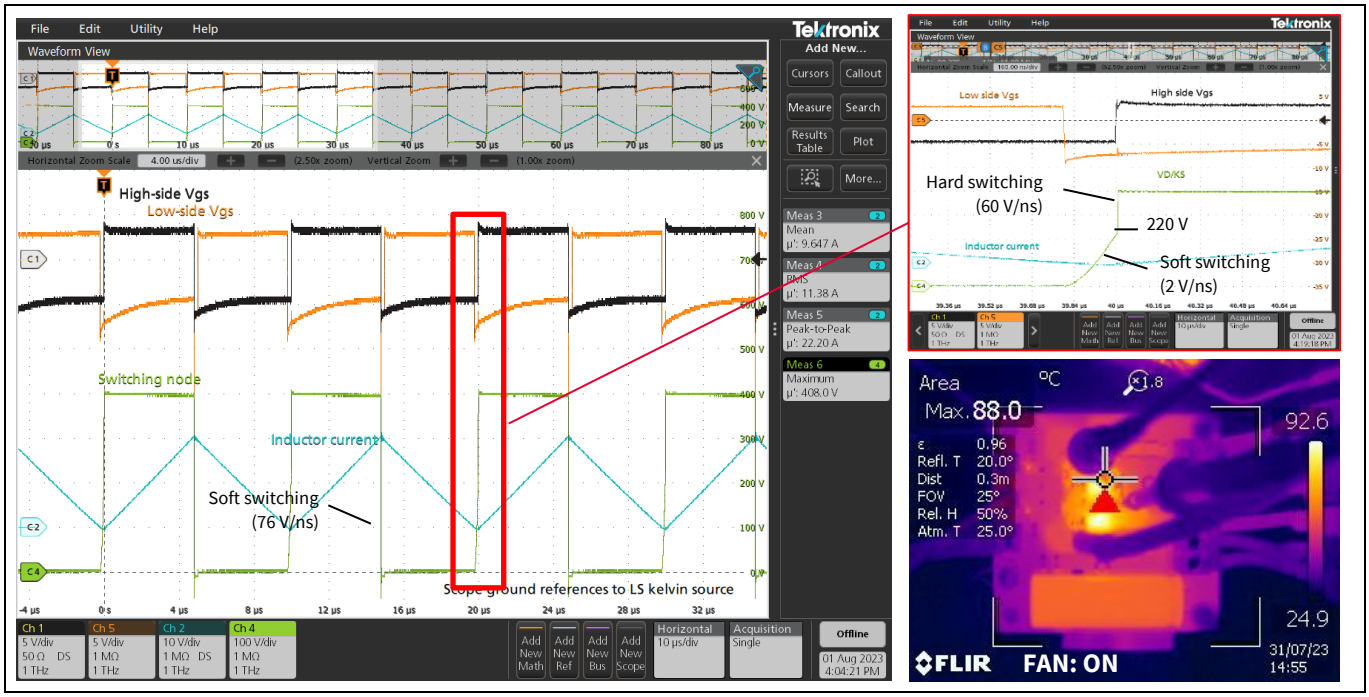


Figure 35 TCM buck mode operation, P_{OUT} = 2 kW, f_{SW} = 100 kHz, 50 µH filter inductor: waveforms (left) and power stage max. temperature (right)

5.3.2 Operation at 2 MHz

With this configuration the board can be operated at different power levels up to 620 W output power, as shown in Figure 38. Intermediate power points at 300 W and 600 W are reported in Figure 36 and Figure 37.

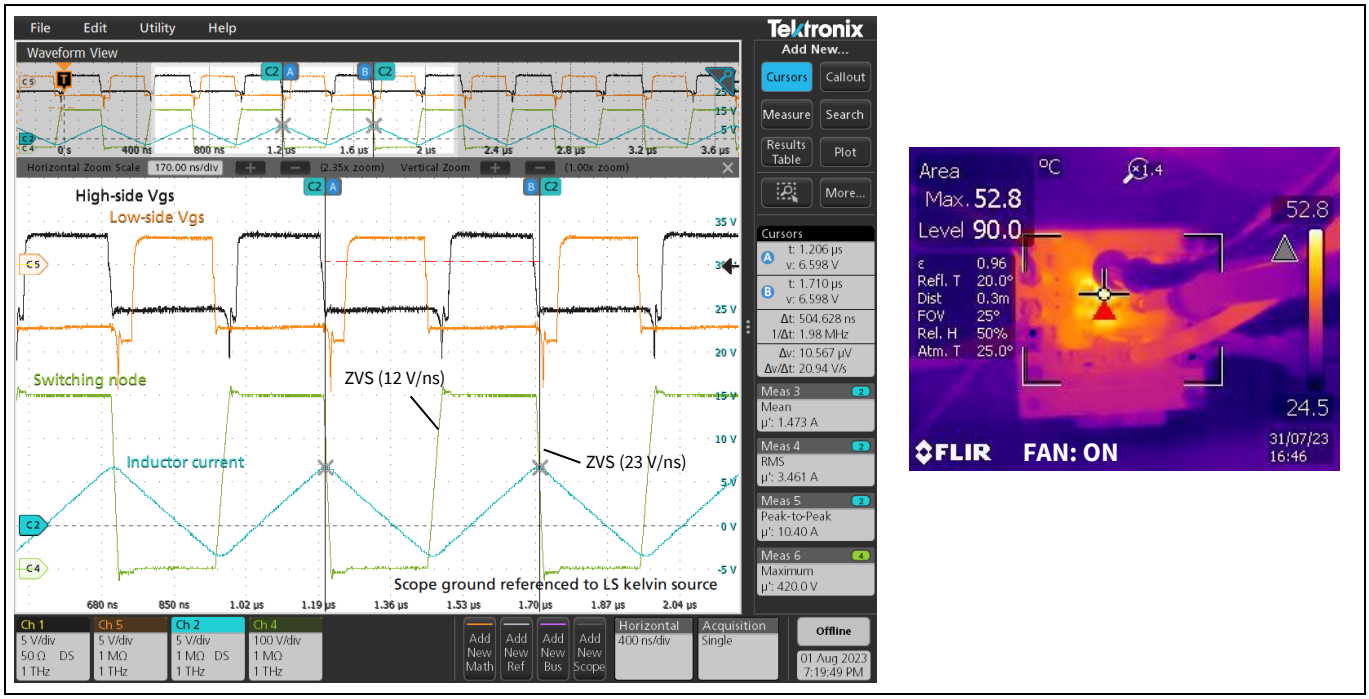
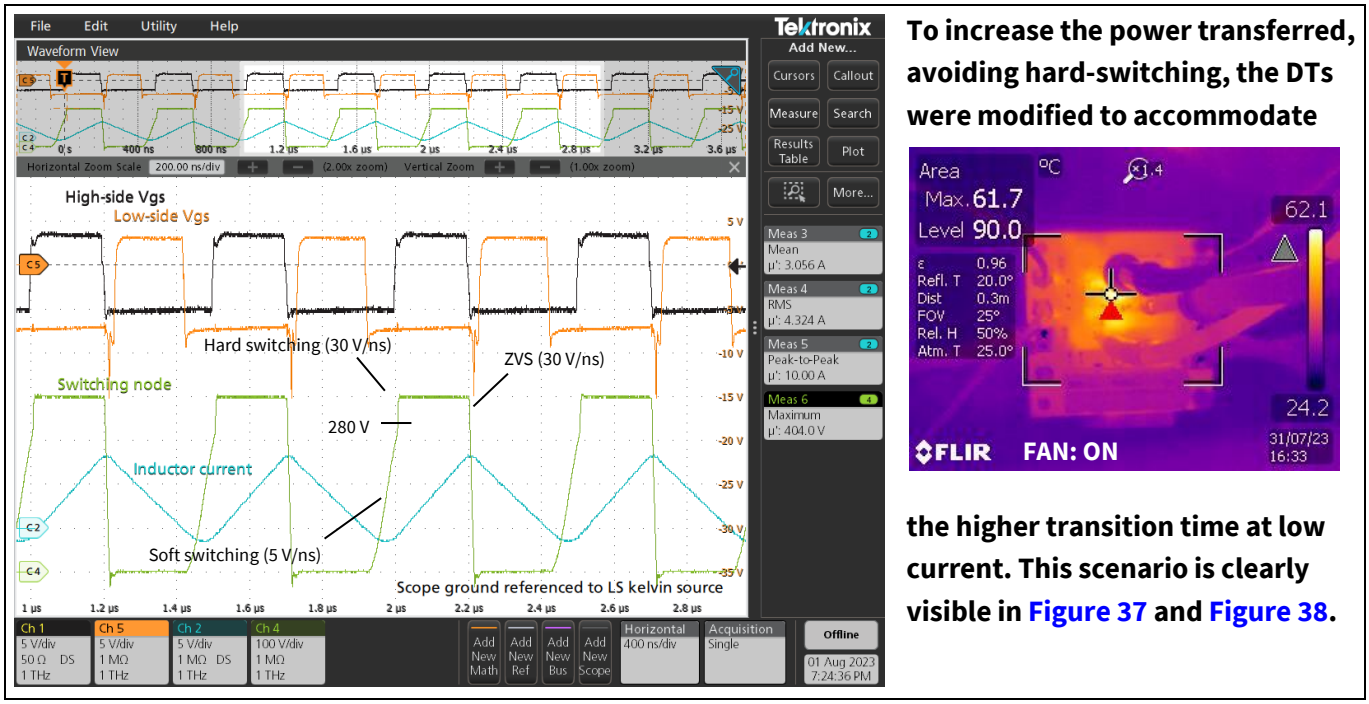


Figure 36 TCM buck mode operation, P_{OUT} = 300 W, f_{SW} = 2 MHz, 5 µH inductor: waveforms (left) and power stage max. temperature (right)



To increase the power transferred, avoiding hard-switching, the DTs were modified to accommodate the higher transition time at low current. This scenario is clearly visible in Figure 37 and Figure 38.

Figure 37 TCM buck mode operation, P_{OUT} = 600 W, f_{SW} = 2 MHz, 5 µH filter inductor: waveforms (left) and power stage max. temperature (right)

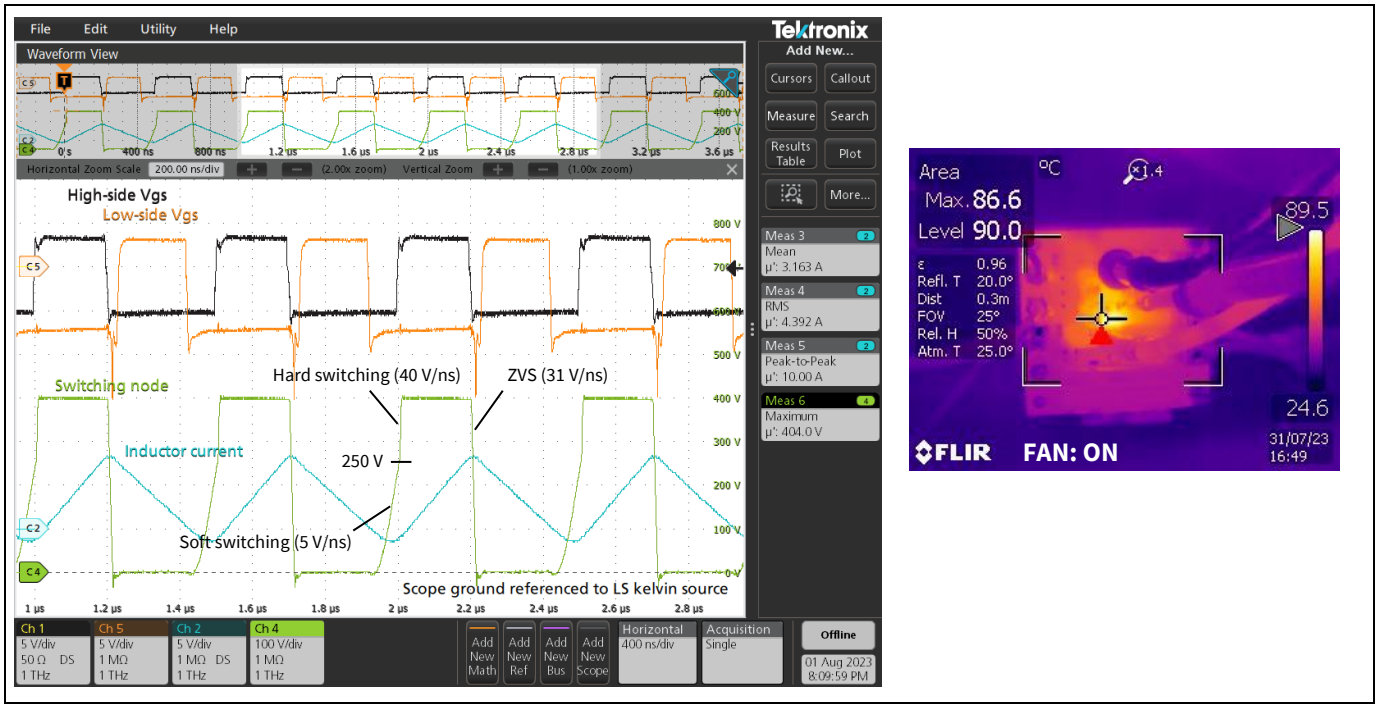


Figure 38 **TCM buck mode operation, P_{OUT} = 620 W, f_{SW} = 2 MHz, 5 µH filter inductor: waveforms (left) and power stage max. temperature (right)**

6 Layout considerations

Routing gate drive traces for GaN HEMTs is critical to achieve lower switching losses (via fast V_{SW} transients, resulting in high dV/dt) and reliable operation. Therefore, when designing with GaN HEMT, it is important to reduce as much as possible the parasitic inductance in series with the gate loop, and make sure the driver–switch connection is not a bottleneck for the switching speed.

Before listing layout best practices, it is important to keep in mind that the DC and the high-frequency (HF) current paths are different. Indeed, while DC currents flow through the lowest-resistance path, HF currents tend to flow/distribute such that the magnetic energy associated with the parasitic inductances is minimized. In most cases, this implies that the return path for the HF currents happens on the return copper trace/plane closest to the signal routing. As an example, the driving loop of the HS HEMTs for bipolar V_{GS} of EVAL_HB_GAN_HYBRID is reported in Figure 39. If the gate drive loop is implemented with the gate signal trace on layer 1 (L1) and the return path is implemented with a plane on layer 2 (L2), the HF return current will not distribute over the whole return plane, but will flow on the plane on L2 just below the trace L1 as a typical microstrip transmission line.

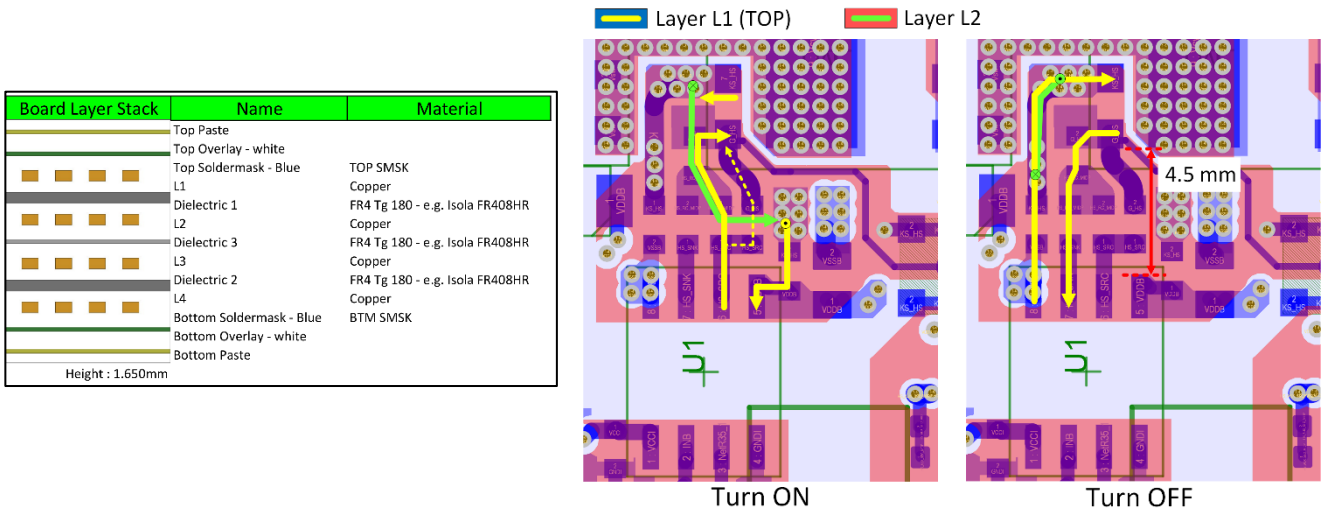


Figure 39 Stackup example (left), HSloop (right) in EVAL_HB_GAN_HYBRID. HF currents are represented with straight lines; DC with dashed lines.

Driving currents during the switching transients are essentially HF currents, therefore it is important to ensure proper signal and return paths. In the case of EVAL_HB_GAN_HYBRID (Figure 39) the gate signal path is connected with a trace on L1 (blue) having 700 µm thickness and 4.5 mm length, and the return path is done on layer L2 (red) with a copper plane referenced to the KS contact.

6.1 Guidelines

The following points should be considered when routing the driving loop for GaN HEMTs:

1. The series parasitic inductance reduces with increasing trace width and decreasing trace length:
    - Place the gate driver IC as close as possible to the GaN HEMT to be driven (consider a microstrip 250 µm wide with 300 µm distance from reference plane introduces ≈400 pH/mm).
    - Use relatively thick copper width for the gate trace, and a return plane if possible.
2. Consider using at least two layers for the gate loop implementation. This allows proper routing of the gate node (e.g., on the top layer) and makes the relative return path as short as possible.
3. Also place the return path as close as possible to the gate signal trace. In case of plane return loop, place it on an adjacent layer.
4. Avoid layer jumps, if possible. If this is unavoidable, ensure a reasonable number of vias in parallel to connect the signals in order to reduce parasitic inductance (consider that a 250 µm via adds around 750 pH/mm depending on via height).
5. Place the decoupling capacitor(s) for V_{DD} (and V_{SS}) as close as possible to the gate driver IC, and in particular in such a way that the HF current paths are minimized.
6. Make use of the separate SNK and SRC pins of the single-channel drivers to optimize the RC circuit. A possible implementation is shown in Figure 39.

In the case of the EVAL_HB_GAN_HYBRID, the driving loop layout is optimized for bipolar supply, plus a good enough optimization for unipolar supplies: the two supply approaches require different decoupling capacitors (one for unipolar, two for bipolar, respectively). A full layout of EVAL_HB_GAN_HYBRID is shown in Appendix B: Layout. Further considerations about GaN driving can also be found in [11].

7 Implementing isolation with ISOFACE™ digital isolators

ISOFACE™ 2DIBx40xF and 4DIR040xH is a family of high-performance digital isolators enabling robust data transmission over a galvanic isolation barrier thanks to Infineon's coreless transformer (CT) technology. It offers high reliability with IEC 60747-17 certification and CMTI of more than 100 V/ns, which makes it the best fit to achieve isolation with hybrid driving. The ISOFACE™ 2DIBx40xF is available in a DSO-8 narrow-body 150 mil package and withstands up to 3000 V_{RMS} basic isolation voltage (V_{ISO}). The ISOFACE™ 4DIR040xH is available in a DSO-16 narrow-body 300 mil package and withstands up to 5700 V_{RMS} reinforced isolation voltage (V_{ISO}).

Each side of the digital isolator can be independently supplied with any voltage between 2.7 V and 6.5 V, which allows shifting the power stage PWM signals to 5 V level. Furthermore, 2DIR and 4DIR allow keeping tight time matching due to their 3 ns maximum channel-to-channel delay difference.

Figure 40 and Figure 41 show a possible implementation of the hybrid driving with 2DIRx and 4DIRx for HB and full-bridge (FB) driving applications, respectively.

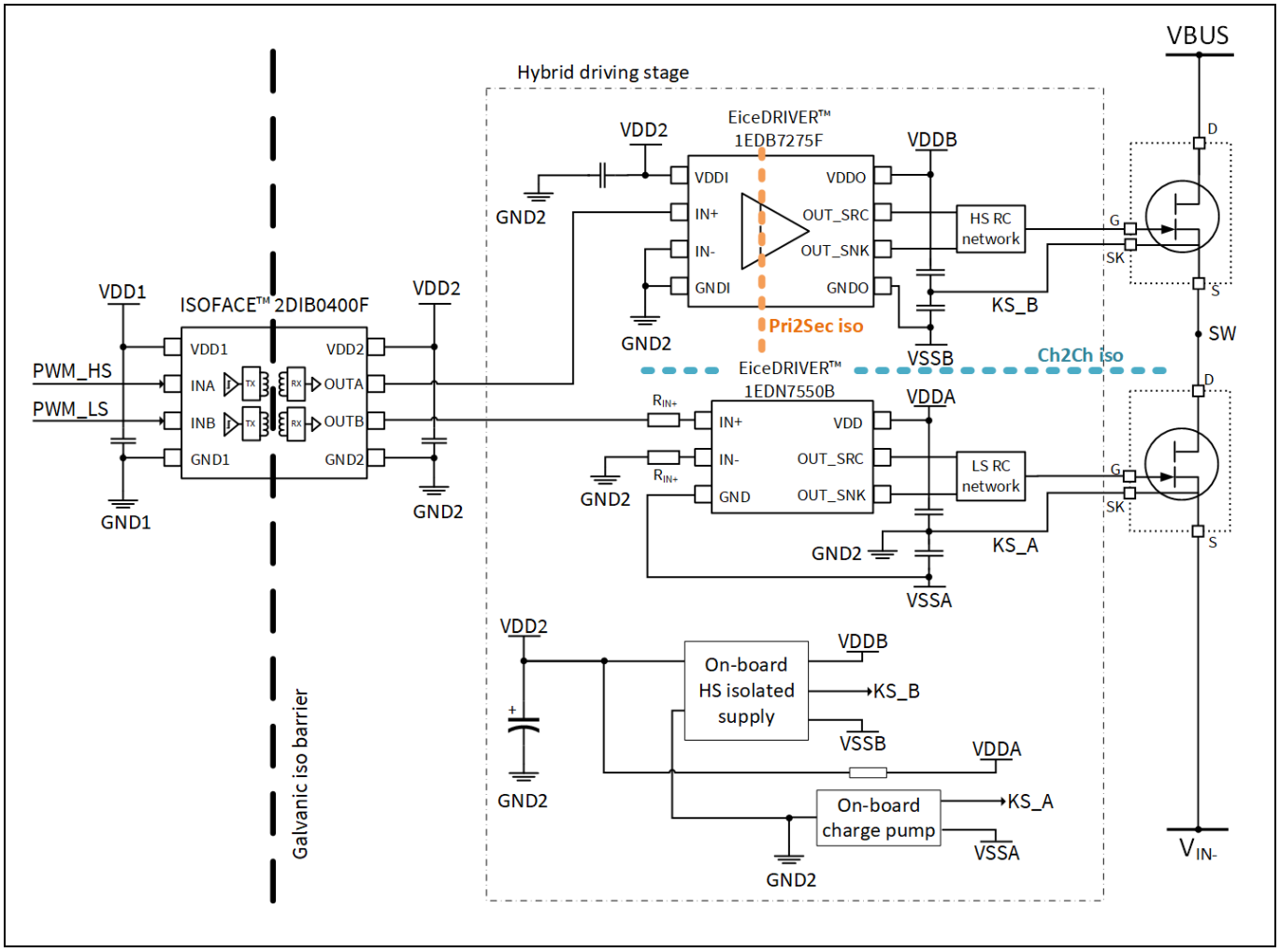


Figure 40 Basic isolated HB implementation with ISOFACE™ 2DIBx and hybrid driving

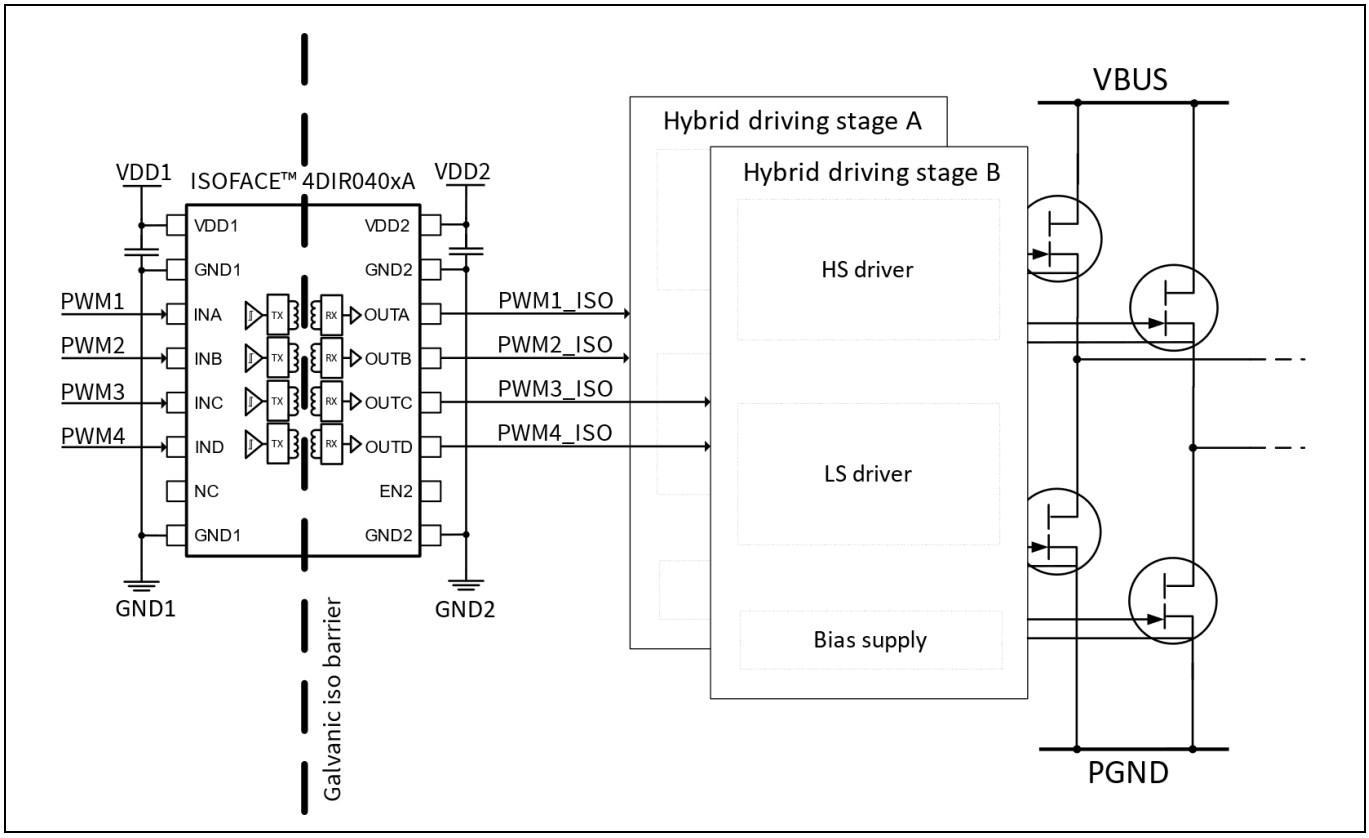


Figure 41 Reinforced isolated FB implementation with ISOFACE™ 4DIRx and hybrid driving

Table 9 summarizes possible implementations of the isolation partitioning with the latest Infineon EiceDRIVER™ and ISOFACE™ products.

Table 9 Possible driving schemes and galvanic isolation implementation strategies

Isolation partitioning	Pros	Cons	Infineon products
Digital isolator with level-shifter driver	- Good enough solution for some use cases	- Two-chip solution - Low layout flexibility - Limited CMTI capability - No negative bias	2EDL drivers 2DIx and 4DIx isolators
Digital isolator with hybrid driving[1]	- High layout flexibility - Negative bias possible - Very high CMTI - High channel-to-channel creepage	- Three-chip solution	1EDN-TDI driver 1EDB isolated driver 2DIx and 4DIx isolators

[1] This work

Isolation partitioning	Pros	Cons	Infineon products
2x single channel isolated driver	- High layout flexibility - Very high CMTI - High channel-to-channel creepage	- Two-chip solution	1EDB isolated driver 2DIx and 4DIx isolators
1x dual channel isolated driver	- Single-chip solution - Adequate CMTI	- Low layout flexibility	2EDi isolated drivers

From all the considerations above, the hybrid driving approach turns out to be an easily scalable solution for FB stages, and represents the most cost-effective two-chip solution when no galvanic isolation is required.

In case of galvanic isolation requirements Figure 40 and Figure 41 show two possible implementations with hybrid driving. Table 9 shows alternative solutions from Infineon with pros and cons, and therefore different approaches can be followed in order to optimize the most critical parameters according to the application.

8 Appendix A: Schematic

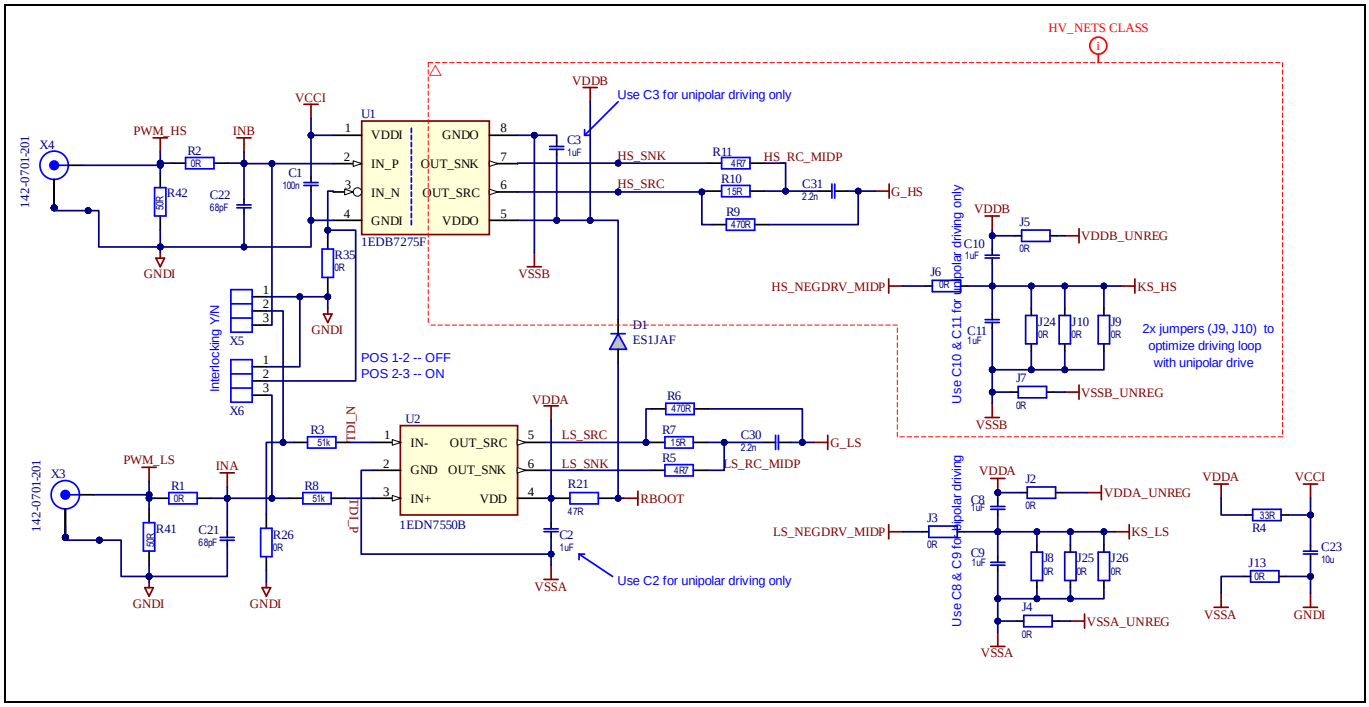


Figure 42 Configurable driving stage

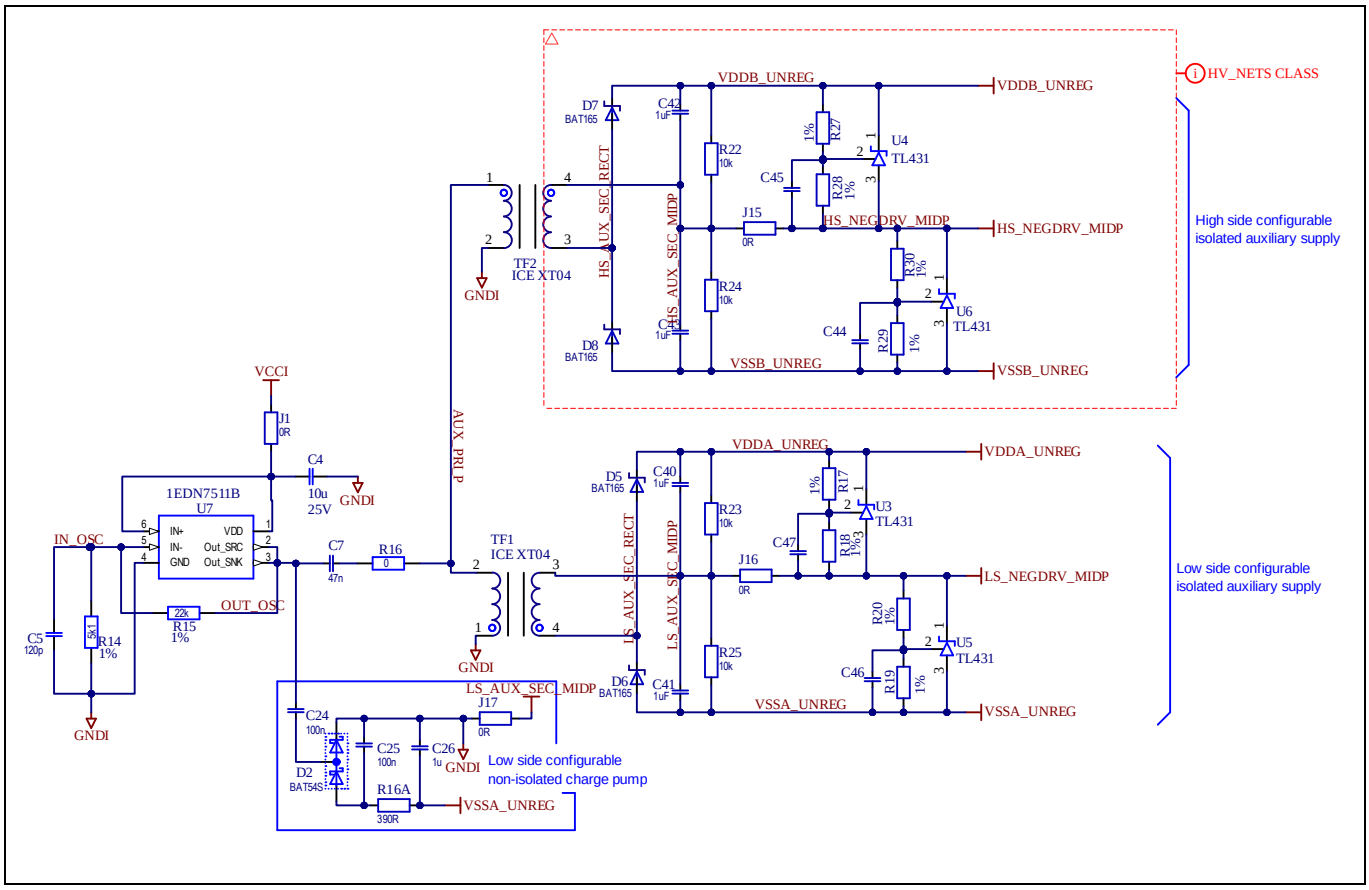


Figure 43 Configurable bias supply

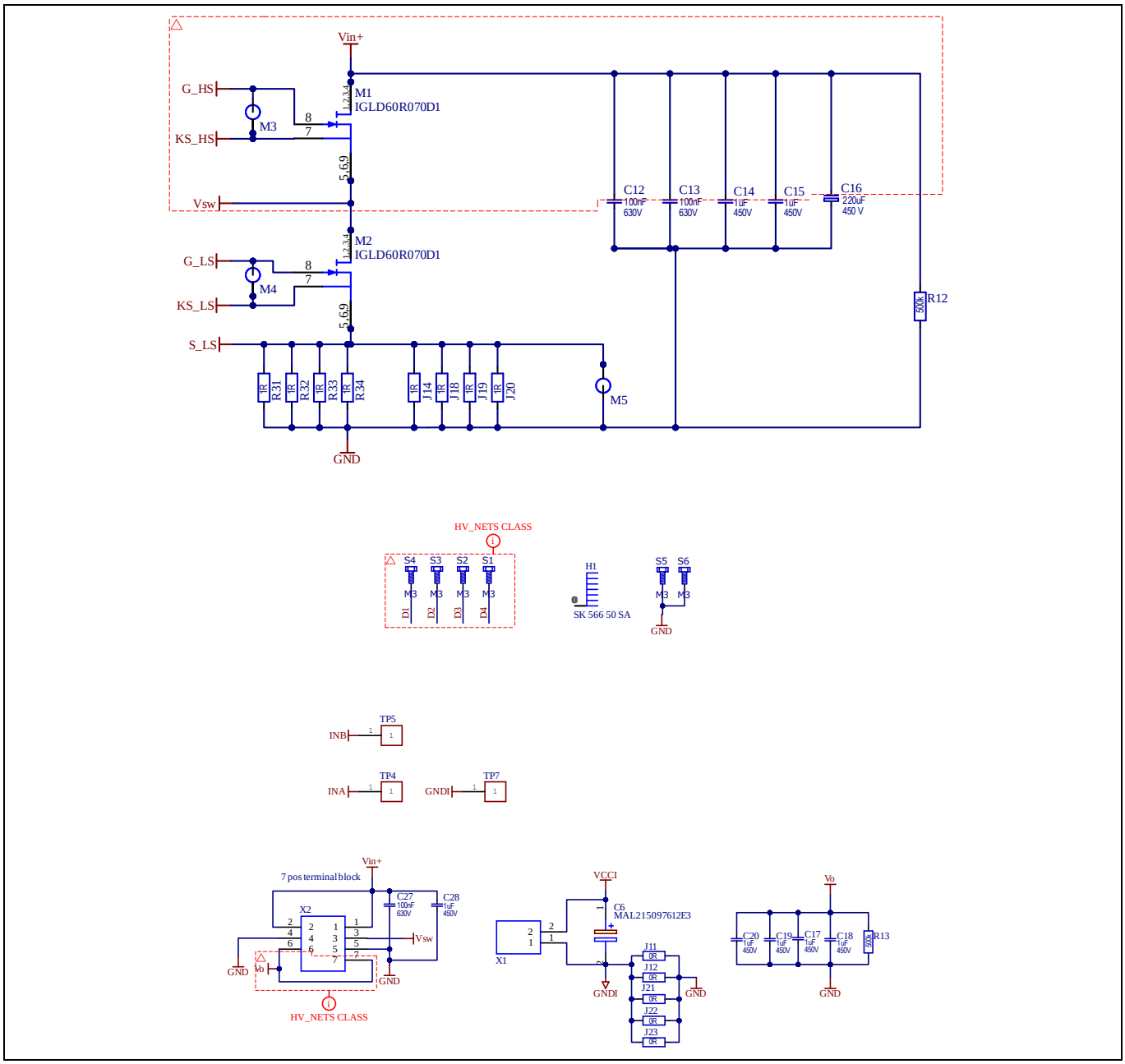


Figure 44 GaN HB power stage and connectors

9 Appendix B: Layout

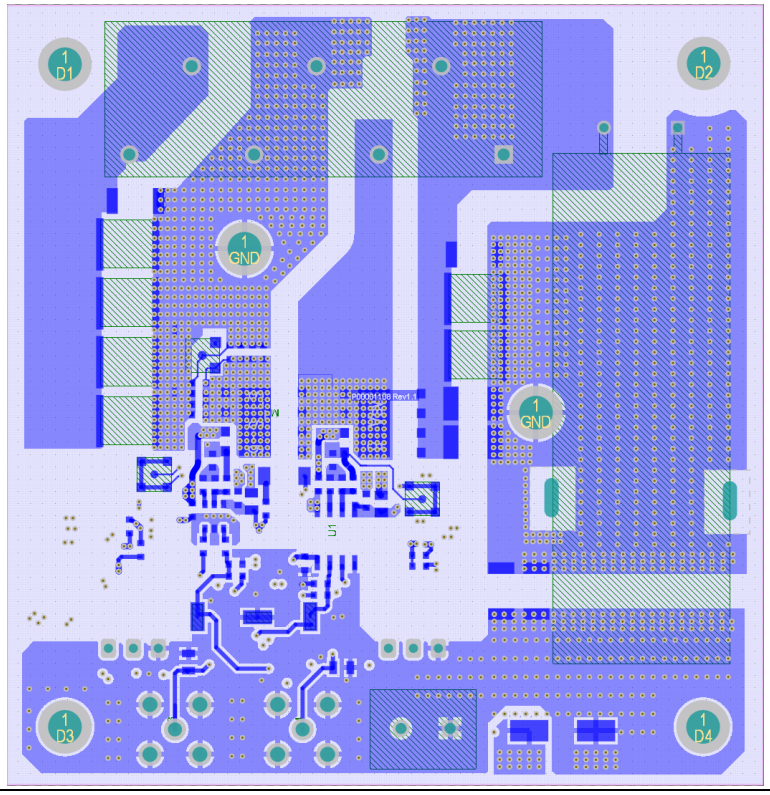


Figure 45 EVAL_HB_GAN_HYBRID – layer L1 (TOP)

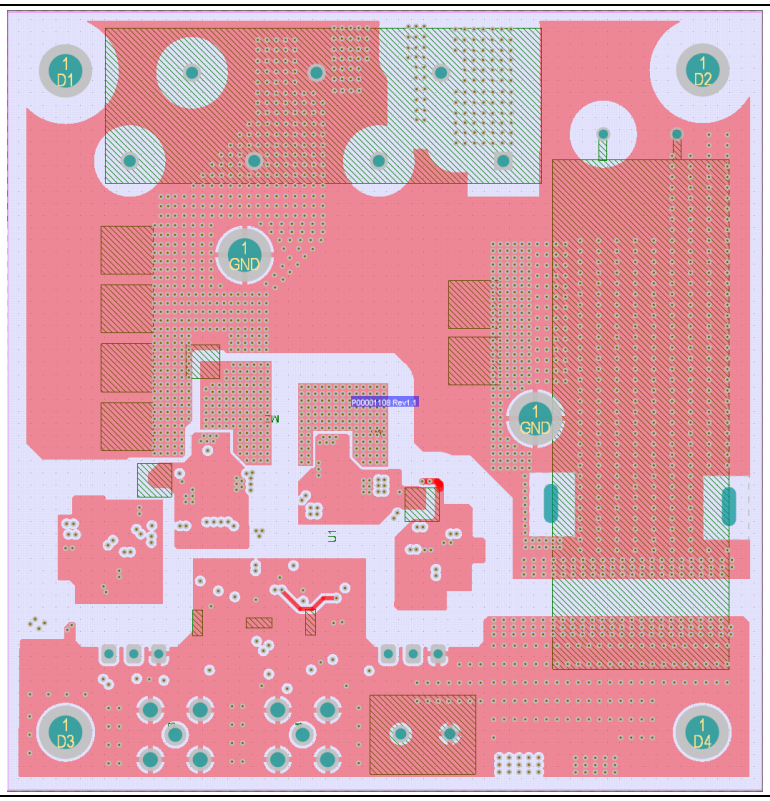


Figure 46 EVAL_HB_GAN_HYBRID – layer L2

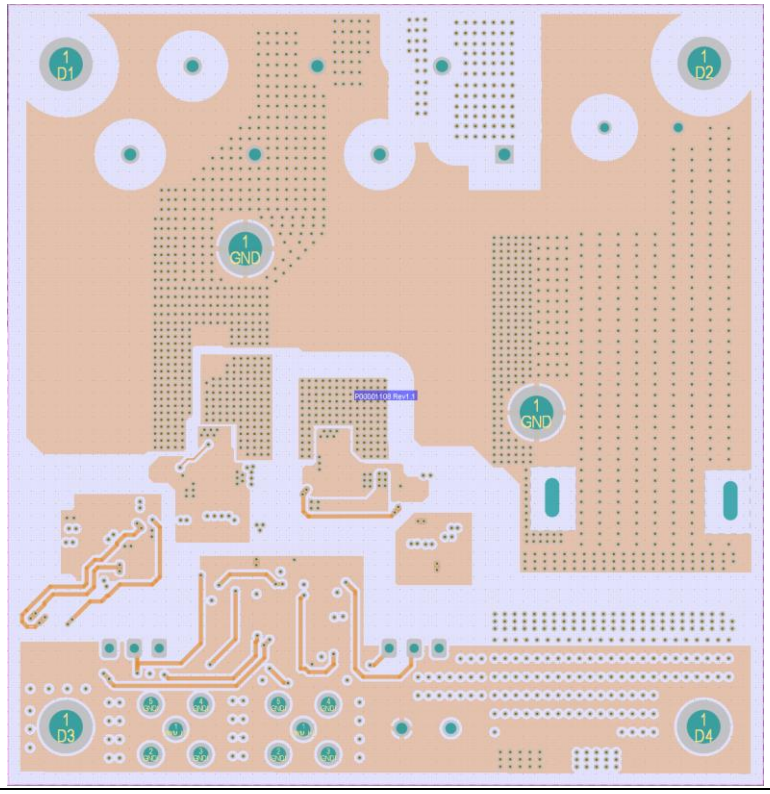


Figure 47 EVAL_HB_GAN_HYBRID – layer L3

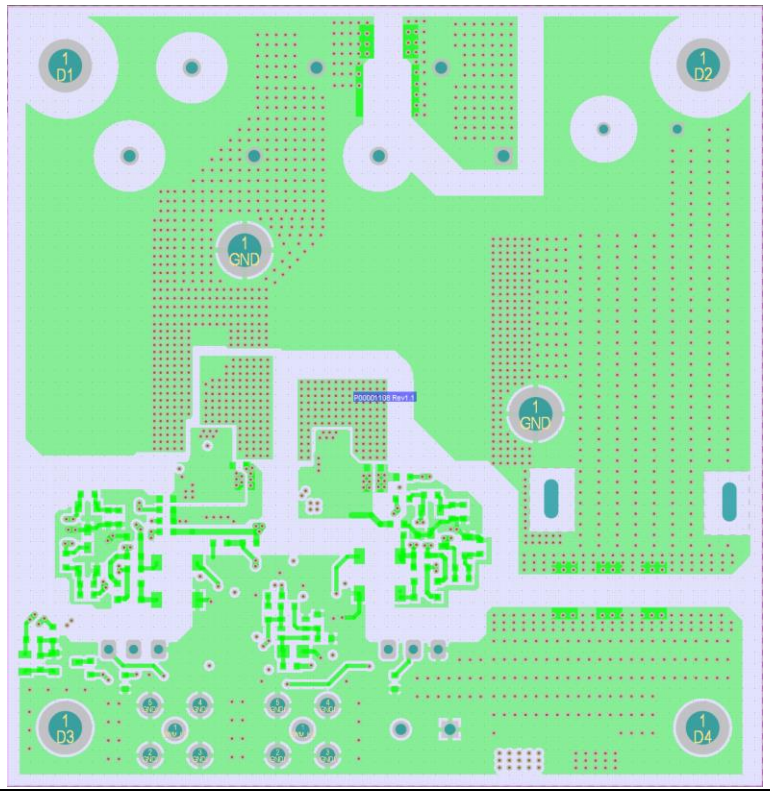


Figure 48 EVAL_HB_GAN_HYBRID – layer L4 (BOTTOM)

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List of abbreviations

AUX	Auxiliary supply
AWG	Arbitrary waveform generator
CP	Charge pump
CrCM	Critical conduction mode
DFN	Dual-flat no-leads package
DT	Dead time
GaN	Gallium nitride
GIT	Gate injection transistor
HEMT	High electron mobility transistor
HS	High-side
IC	Integrated circuit
LS	Low-side
MMCX	Micro-miniature coaxial connector
OCP	Overcurrent protection
PCB	Printed circuit board
PSU	Power supply unit
PWM	Pulse-width modulation
SG	Schottky-gate
SiC	Silicon carbide
SMA	Sub-miniature Version A connector
SMPS	Switched-mode power supply
STP	Shoot-through protection
TCM	Triangular current mode
TDI	Truly differential input
WBG	Wide bandgap
ZVS	Zero-voltage switching

Revision history

Document revision	Date	Description of changes
V 1.0	2023-09-29	Initial release

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Edition 2023-09-29

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference

AN_2308_PL21_2309_151257

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