Circuit use cases for small signal MOSFETs - showing a circuit behavior in SPICE simulation

About this document

Scope and purpose

In electrical appliances, the role of the microcontroller unit (MCU) is becoming increasingly important every year. Recently, thanks to mobile applications and rapid internet developments, demand for electrical appliances with MCUs is increasing, and the MCU's tasks are becoming more complicated. Every semiconductor manufacturer that produces MCUs competes for calculation speed and integration level. But even now there are several devices that cannot be integrated into an MCU because of the particular manufacturing process. Infineon small-signal products are used for such devices, composed of auxiliary circuits for an MCU in a wide range. Several use cases for auxiliary circuits with small-signal MOSFETs are introduced in this application note, which is intended to help application engineers designing electrical applicances. Specifically, this application note shows SPICE simulations to visualize circuit behaviors, in which current, voltage and temperature are not measurable, even in a lab. These are intended to help the reader understand how such a circuit would work. Chapter 5 explains how to read the symbols in SPICE simulation schematics. It is recommended to refer to this as necessary.

Intended audience

Application engineers.

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1 Overview

Figure 1 shows the typical configuration of an MCU and the auxiliary circuits around it. In this document the auxiliary circuits are split into three categories: Power, Connectivity and Peripherals. These three parts reflect the supportive functions of an MCU, without which it could not operate as expected. These three parts work with higher current and higher voltage than an MCU or a corresponding digital controller, and are so-called “analog circuits”. They consist of analog devices that are difficult to integrate into an MCU because they are built on different semiconductor technologies. Another reason is that using external analog components allows for a variety of options and flexibility in the design of an application. One example of such an external analog device is a small signal MOSFET, explained in more detail in the following chapters.

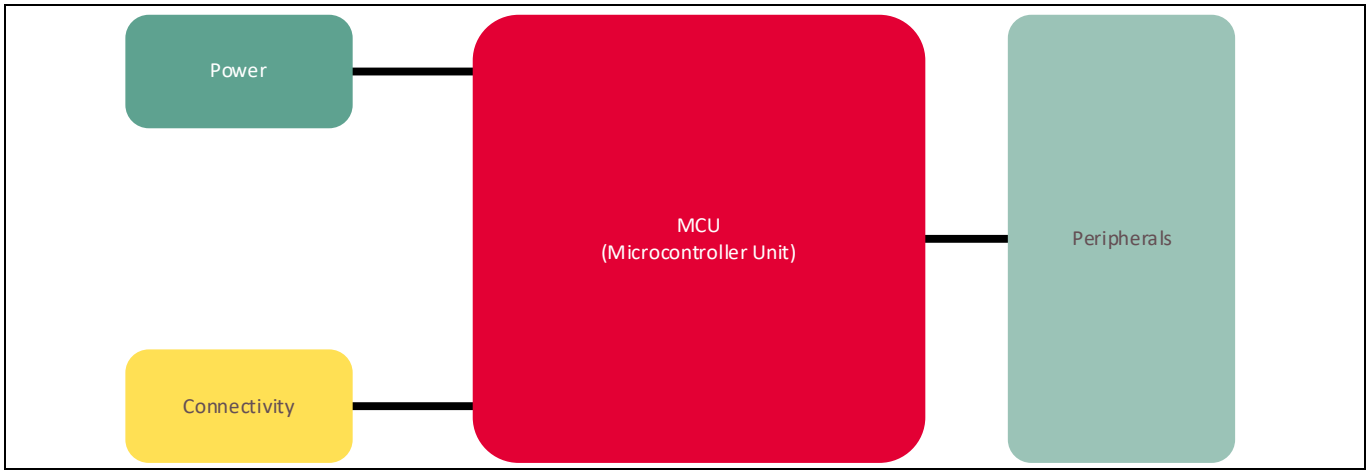


Figure 1 Typical subcircuit around an MCU

2 Power

An integrated cicuit (IC) is highly integrated to save design space and cost. But one of the disadvantages of this is low repairability. Once part of a component gets damaged, even a small part, it must be replaced by a whole new component. In order to prevent such damage, many electronic systems have current protection, soft-start and reverse polarity protection functions.

2.1 Load switch

These protection circuits have to be external circuits rather than being integrated into an MCU. Figure 2 is an example taken from [4] comprising a bidirectional load switch with two p-channel MOSFETs. Depending on the power dissipation requirement, the type of package should be selected accordingly. Small-signal MOSFETs offer a good solution in terms of package size and power dissipation performance. Usually, a load switch uses a p-channel MOSFET for practical reasons; the MOSFET conducts when gate voltage is lower than the one at the source. This circuit has fewer switching events than MOSFETs in a DC-DC converter, and therefore it requires static performance rather than dynamic performance such as safe operating area (SOA) characteristics.

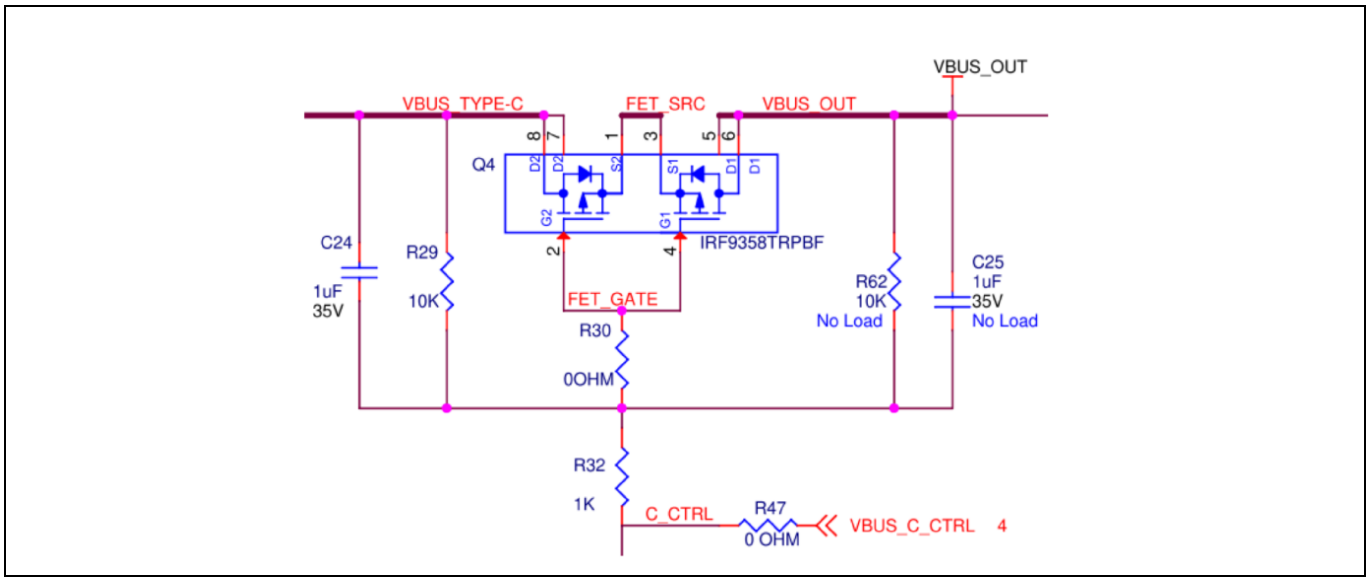


Figure 2 Bidirectional load switch with two p-channel MOSFETs

Figure 3 and Figure 4 show a schematic and a result of a SPICE simulation of a load switch as the example shown in Figure 2. Usually a p-channel MOSFET is driven by an n-channel MOSFET, as shown in Figure 3. A digital signal coming from an MCU to “Signal” termination (in Figure 3) triggers the n-channel MOSFET to turn on the p-channel MOSFET. When the n-channel MOSFET is conducting, the gate voltage of the p-channel MOSFET is lower than the source voltage, which turns-on the p-channel MOSFET and activates a load switch. After the current starts flowing into the powerrail, the junction temperature of the p-channel MOSFET rises because of current flowing from source to drain. In the turn-on transition, inrush current over 35 A as a peak value can beseen. The design of power dissipation should be considered as well according to the target value referred to in the SOA diagram in the datasheet. Figure 5 shows the SOA diagram of BSL307, in which, according to pulse width, I_d current and V_{DS} voltage in the condition, the safety operating area for the product should be confirmed under the limit lines. As R2 increases from 1 kΩ to 3 kΩ, the gate voltage switching speed decreases because of the RC filter effect, as shown in Figure 6. The more relaxed V_{GS} transition during turn-on reduces inrush current peak value. Initially, the current was violating the SOA parameters, but it was reduced from 35 A to 21 A after changing the value of R2. Such an example gives an interesting indication about load switch design, in which fast switching speed would cause trouble for a system powered through the load switch.

Power

Designers could refer to [1] to find out about SOA diagrams and linear mode operation. Regarding inrush current and short-circuit protection assessment on the SOA diagram, refer to [2].

Formatting examples

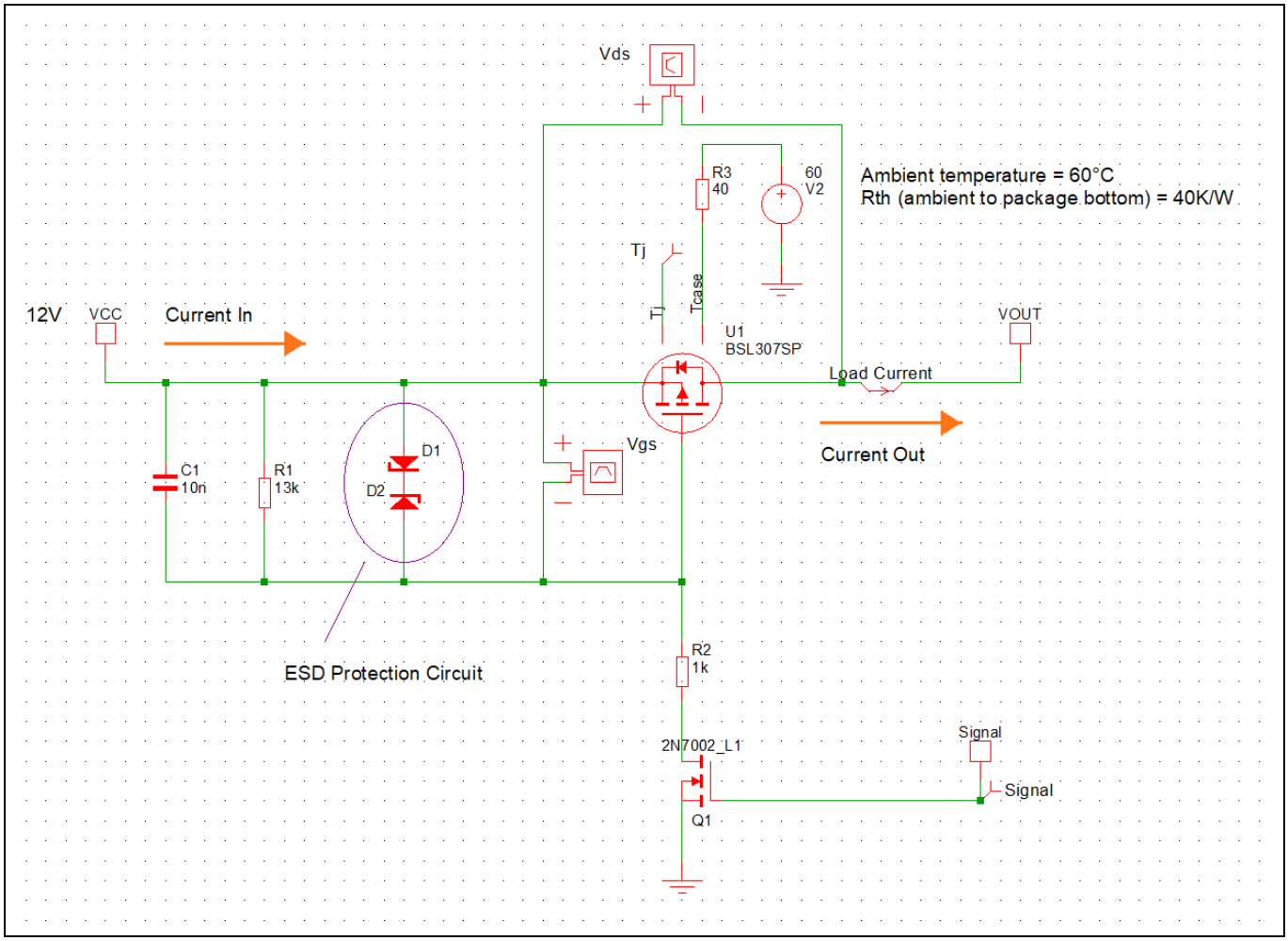


Figure 3 SPICE simulation schematic of typical load switch with PMOS

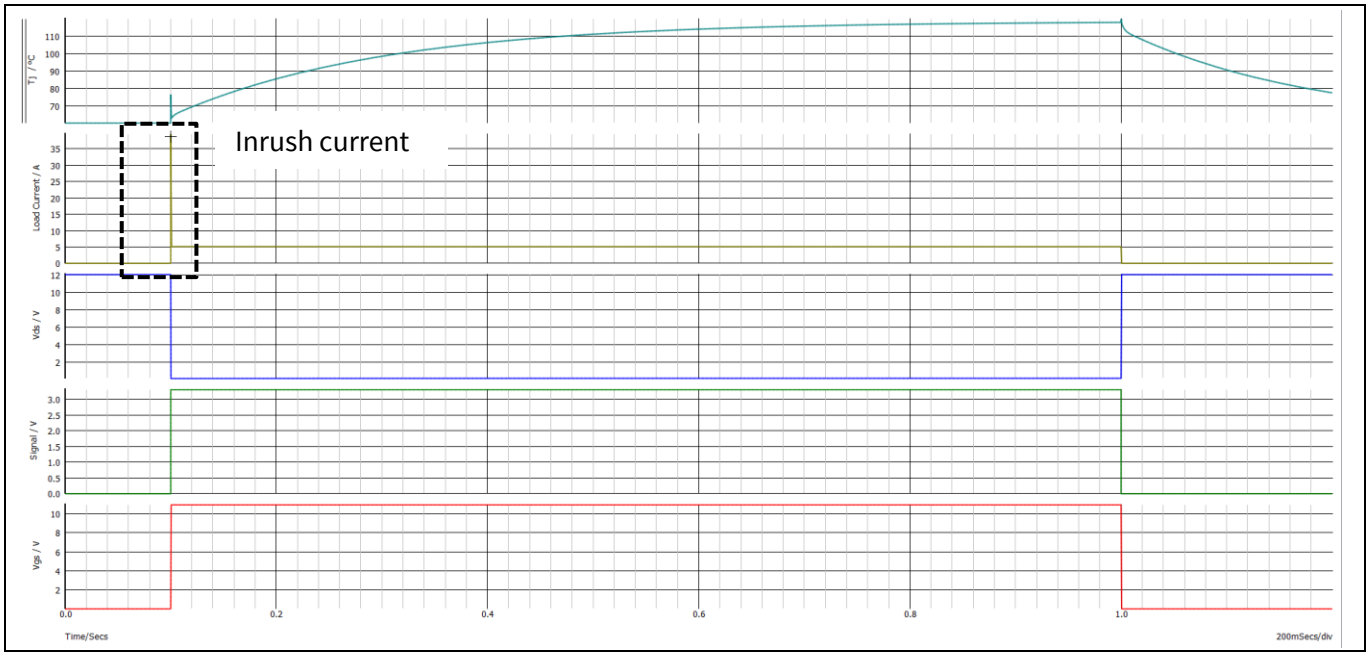


Figure 4 SPICE simulation result of typical load switch with PMOS

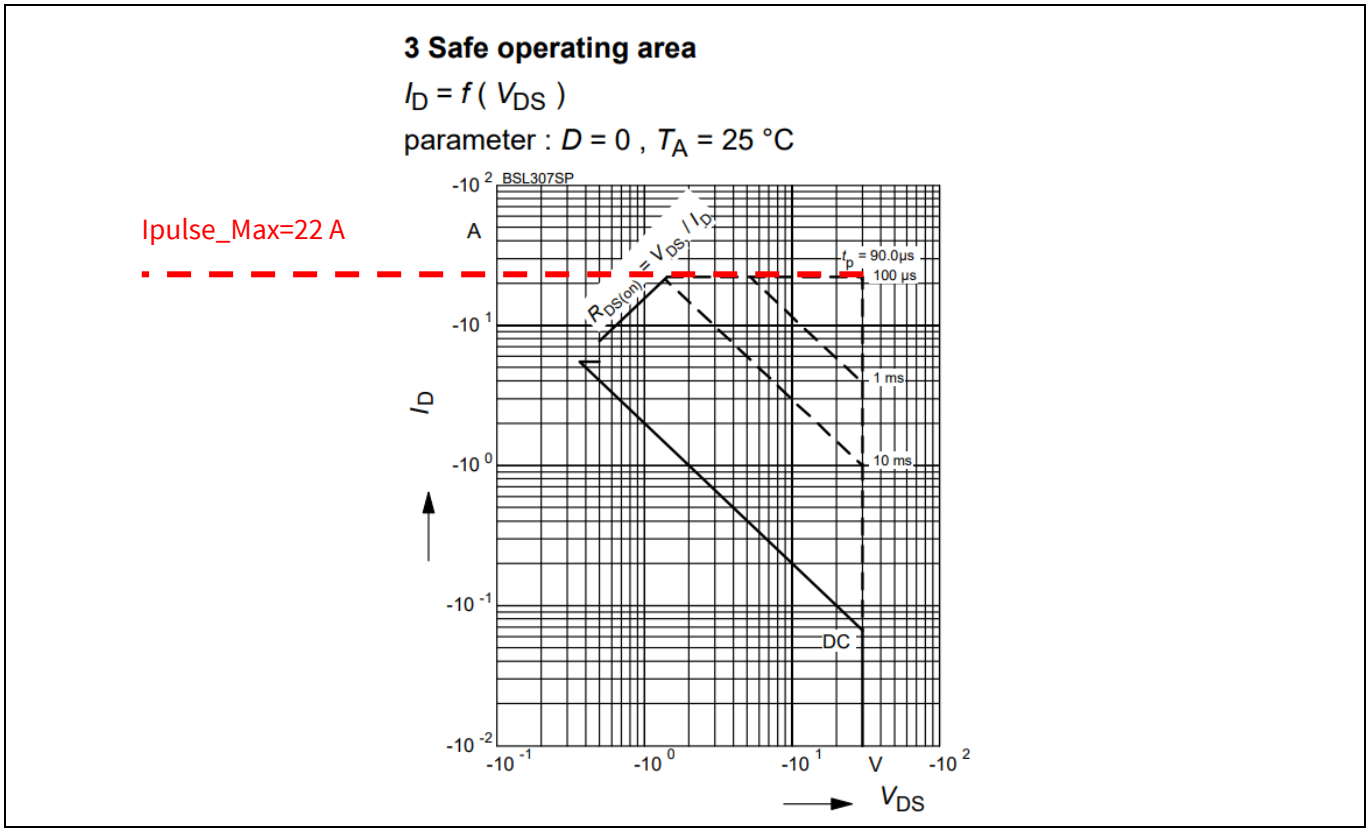


Figure 5 SOA assessment

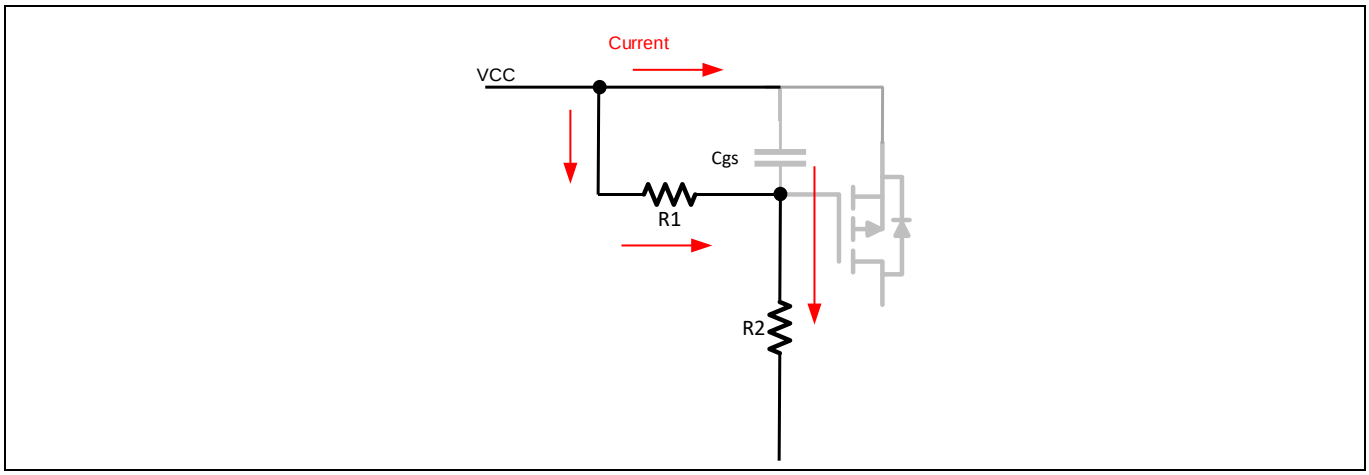


Figure 6 Gate circuit current and RC filter effect

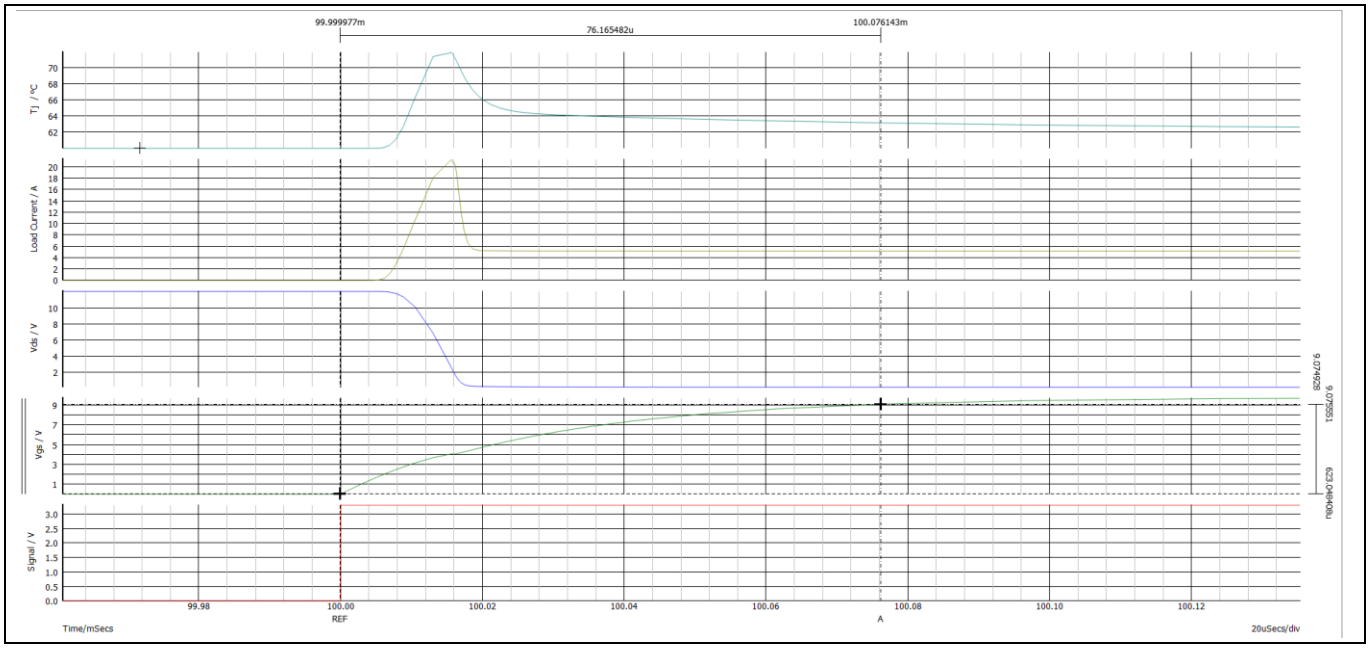


Figure 7 Turn-on event with R2 = 3 kΩ

When a power line has a long path to cover, for example if it is connected through a long harness, parasitic inductances are created. Figure 8 and Figure 9 show a schematic and a result of a SPICE simulation in an assumed scenario, in which there are parasitic inductances on power lines. Switching speed between Signal+ and Signal- is set in 20 ns and then L1 and L2 have 1 nH of parasitic inductance at first. After the simulation is run with L1 swept from 1 nH to 200 nH, Figure 9 shows that V_{DS} reaches avalanche voltage according to increased parasitic inductances. Looking at the temperature of the MOSFET, the temperature of the T_j (junction temperature) doesn't yet reach critical values but it is assumed that an avalanche current causes latch-up effect with potentially damaging effects. The length of the power line and the switching speed of the MOSFET should be considered carefully – [3] could help for better understanding of the avalanche issue.

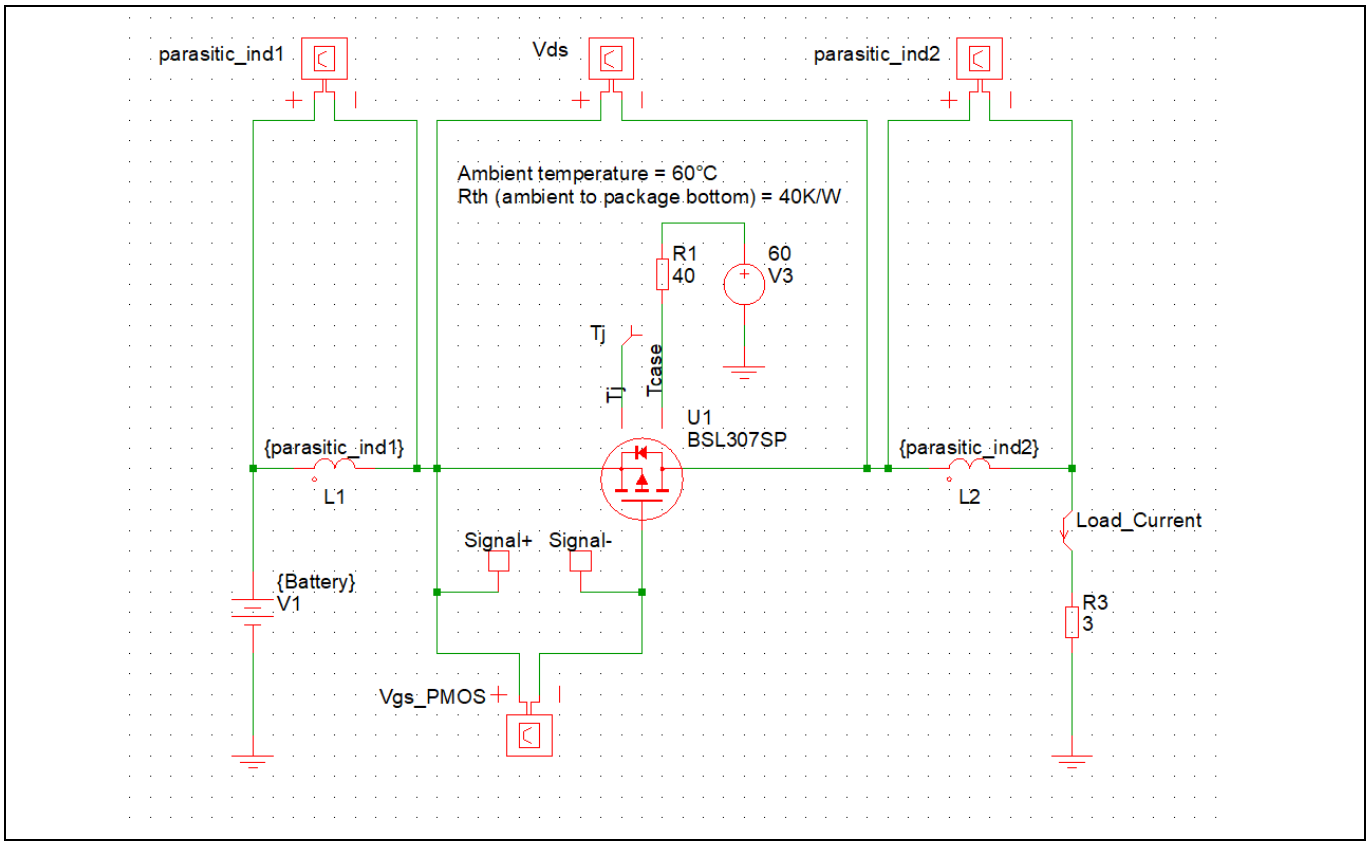


Figure 8 SPICE simulation schematic of a load switch with parasitic inductance

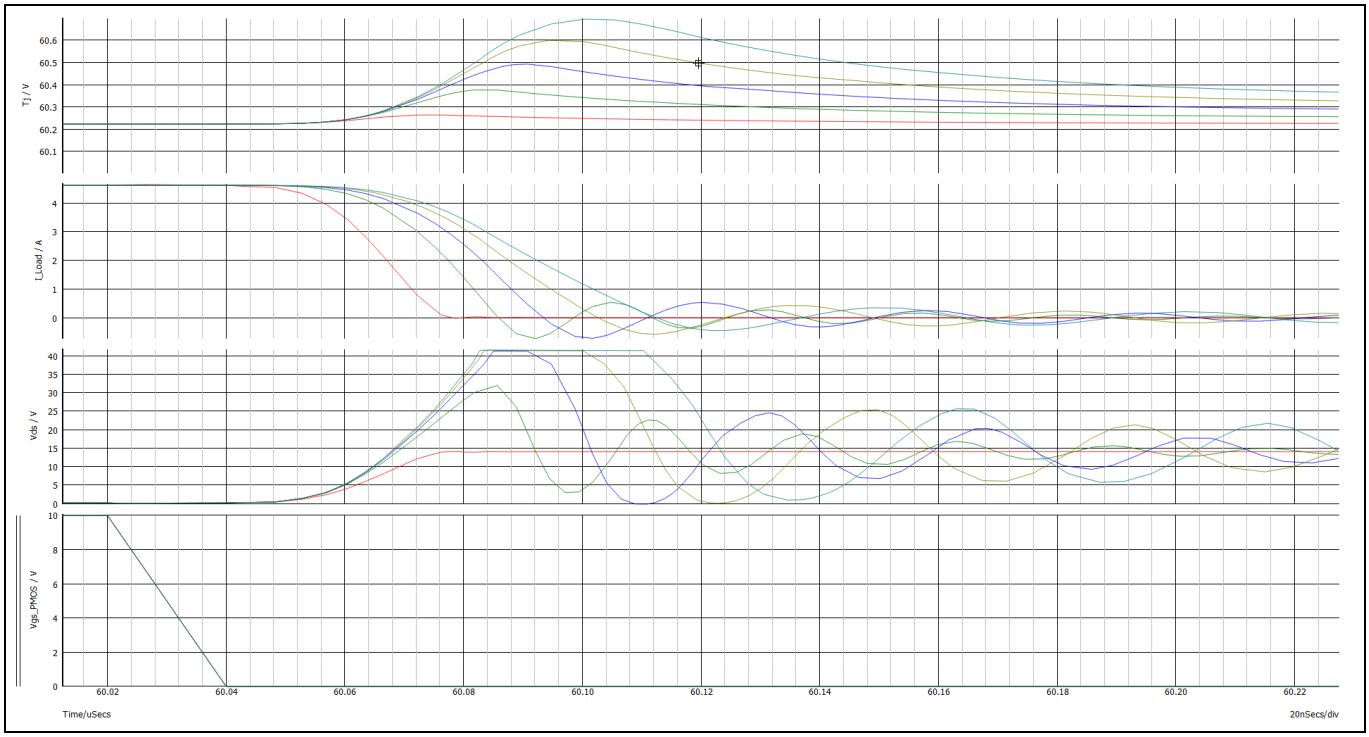


Figure 9 SPICE simulation result of a load switch with parasitic inductance

Figure 10 shows an example of a load switch with current protection taken from [5] that is composed of a silicon-controlled rectifier (SCR or thyristor). Figure 11 is a simulation schematic of a similar circuit as an example in Figure 9 that comprises small-signal products. Figure 12 shows the result of the simulation. In this

case BSL207SP is selected because of the low threshold level. In order to gain enough low $R_{DS(on)}$ in 5 V application, the load switch with p-channel MOSFET needs to have threshold voltage in the range of logic level or ultra logic level. When a plug is inserted at J11 in Figure 10 Q3 is activated and it triggers to conduct Q1. Current starts flowing from J11 to the VCC_5V node and the VBUS node. As Figure 12 shows, when voltage of the DC jack exceeds Zener voltage at D1, voltage generated by R1 activates a Silicon Controlled Rectifier (SCR). Once the SCR is activated, unrequired current is bypassed through an SCR and voltage drop occurs on the DC jack voltage generated by internal resistance of the DC_JACK voltage source. Once the SCR is activated in this topology, it continues to be activated unless I_SCR_B turns off, which means the DC_JACK level has to be 0.

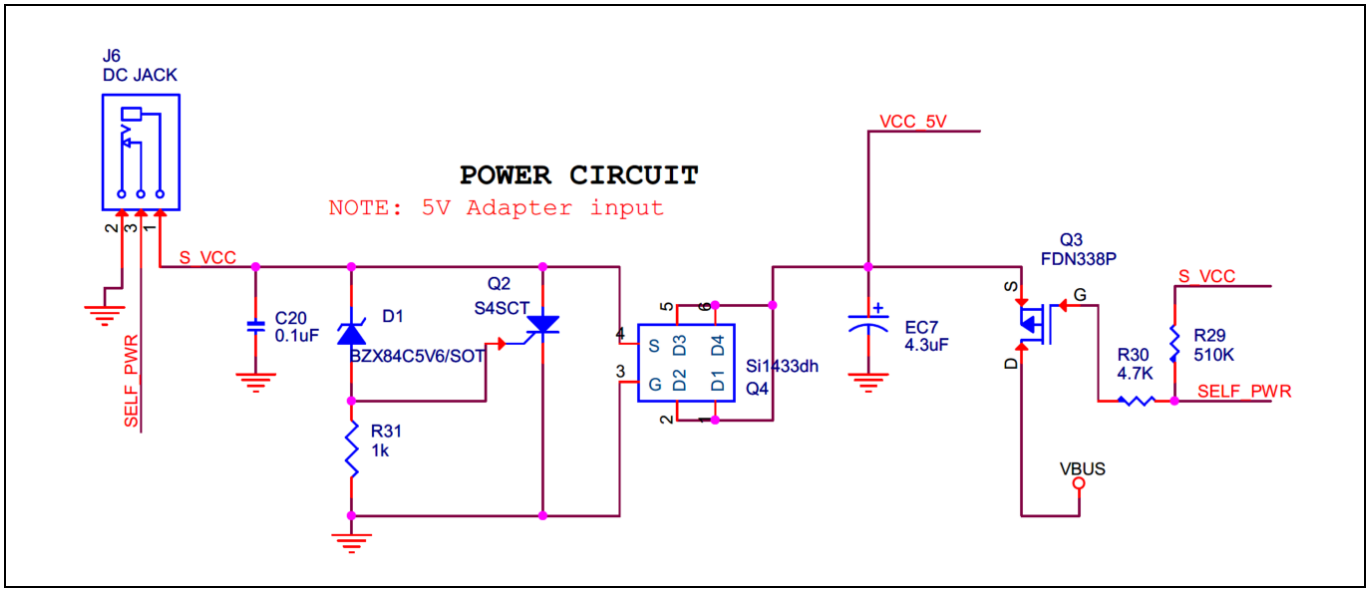


Figure 10 Load switch circuit with an overvoltage protection function

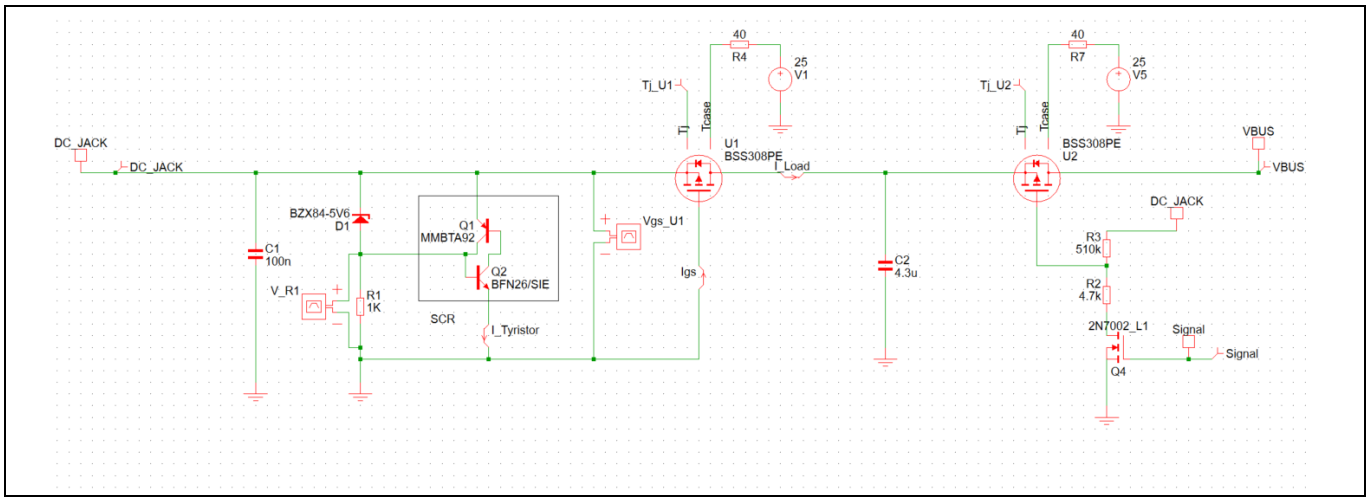


Figure 11 SPICE simulation schematic of a load switch with SCR

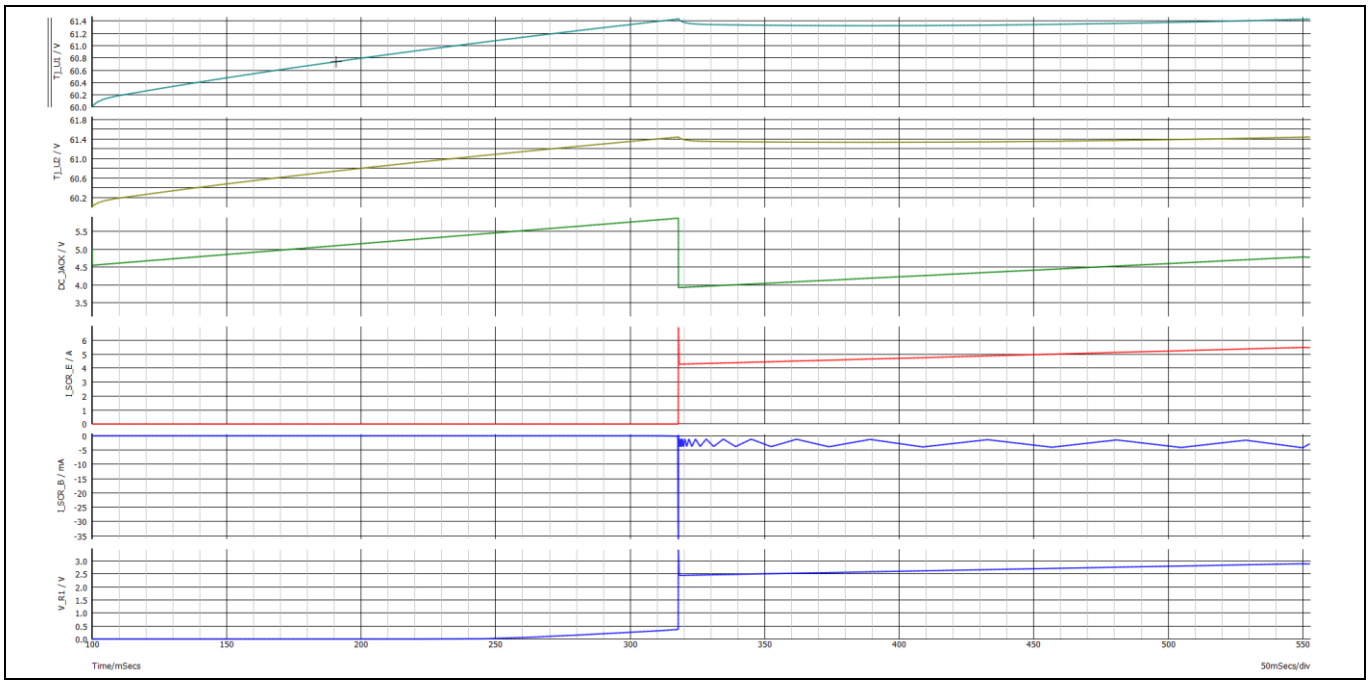


Figure 12 SPICE simulation result of a load switch with SCR

Figure 13 shows another example of a load switch taken from [6]. In this case Q2 enables signals coming from Hall sensors through connector “HALL”.

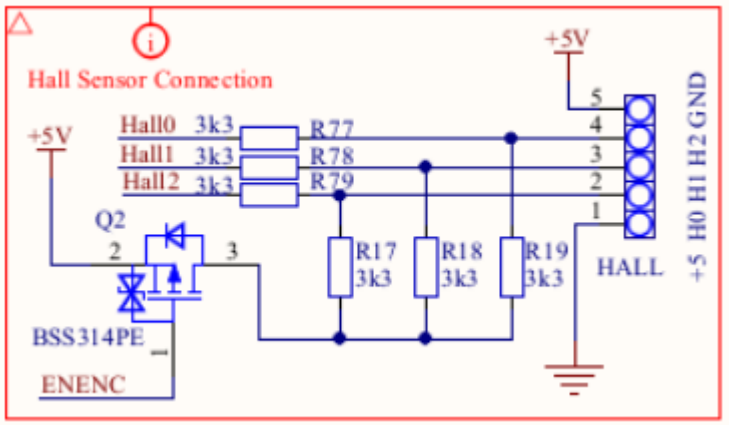


Figure 13 Load switch example

Figure 14 shows a typical configuration of a Hall sensor, in which a sensor signal is amplified through a device “A” and connected to a transistor with an open collector (or open drain) configuration, which allows flexible signal level according to voltage level through pull-up resistors.

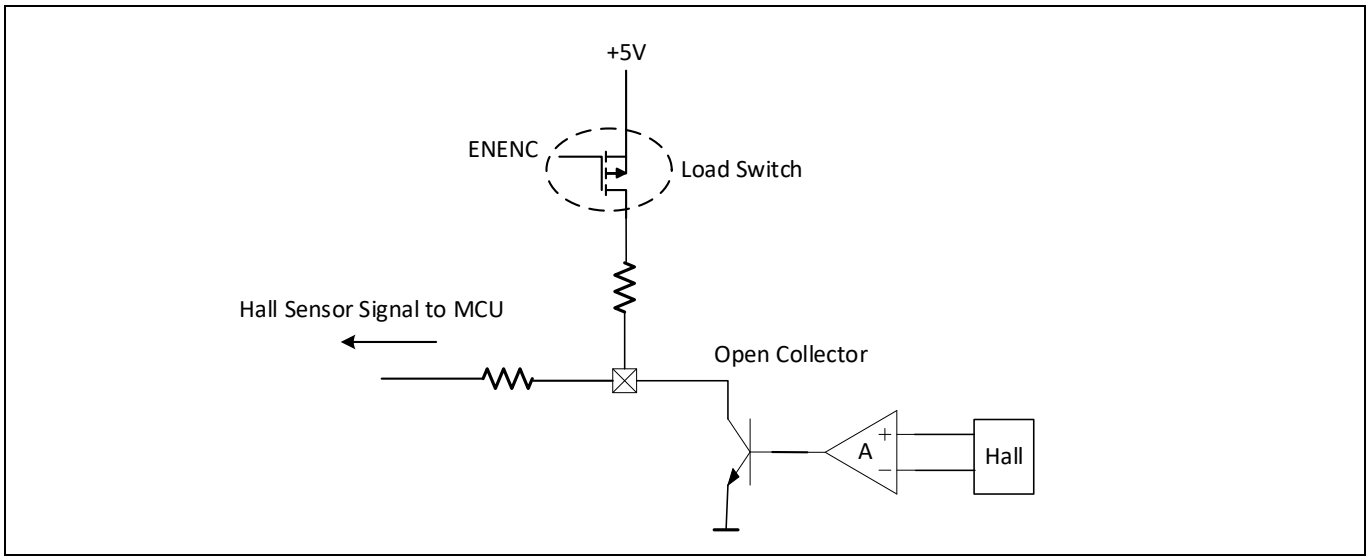


Figure 14 Hall sensor interface configuration

2.2 Overvoltage protection circuit

Figure 15 is an overvoltage protection (OVP) circuit taken from [4] which is a variation of a load switch circuit. Q1 and Q3 act as the load switch which current flows through, and when KP_VBUS_IN has a voltage level more than the V_{th} level of Q1, Q1, and Q3 conduct automatically because gate is connected to GND.

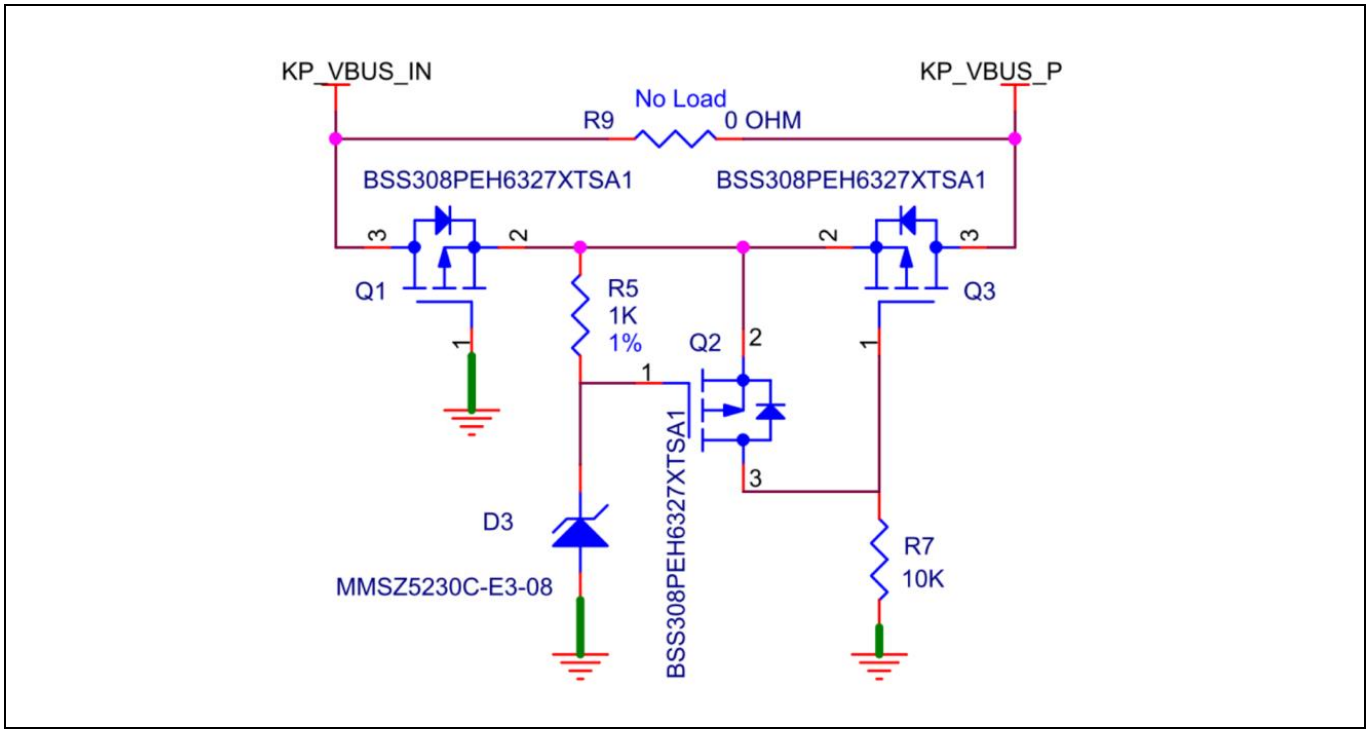


Figure 15 OVP circuit

Figure 19 shows a simulation schematic of the same circuit as the example in Figure 15. When KP_VBUS_IN or KP_VBUS_P has a higher voltage than the Zener voltage at D1, reverse current starts flowing through D1 and it generates voltage drop through R2. The voltage drop switches on Q3 and conducts the source and the drain, which switches off U2 and cuts load line between KP_VBUS_IN and KP_VBUS_P. Figure 17 shows the result of the simulation, when input voltage (in this case KP_VBUS_IN) reaches a certain voltage level, the OVP function

is activated in the sequence described above. R2 regulates activation speed. Because load switch U1 U2 is working in linear mode during the transition, designers must pay attention to the SOA characteristic of a MOSFET and the avalanche voltage that could be generated by fast switching transition, which is described in Section 2.1.

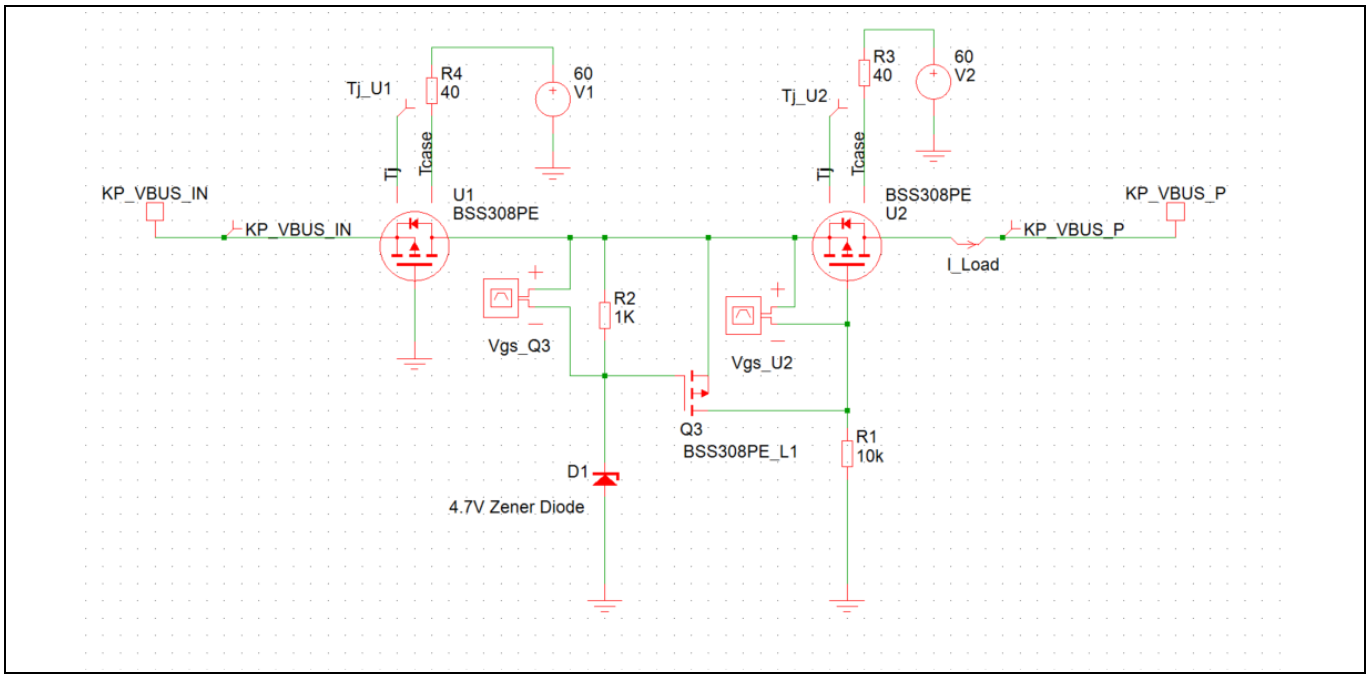


Figure 16 SPICE simulation schematic of a load switch with OVP

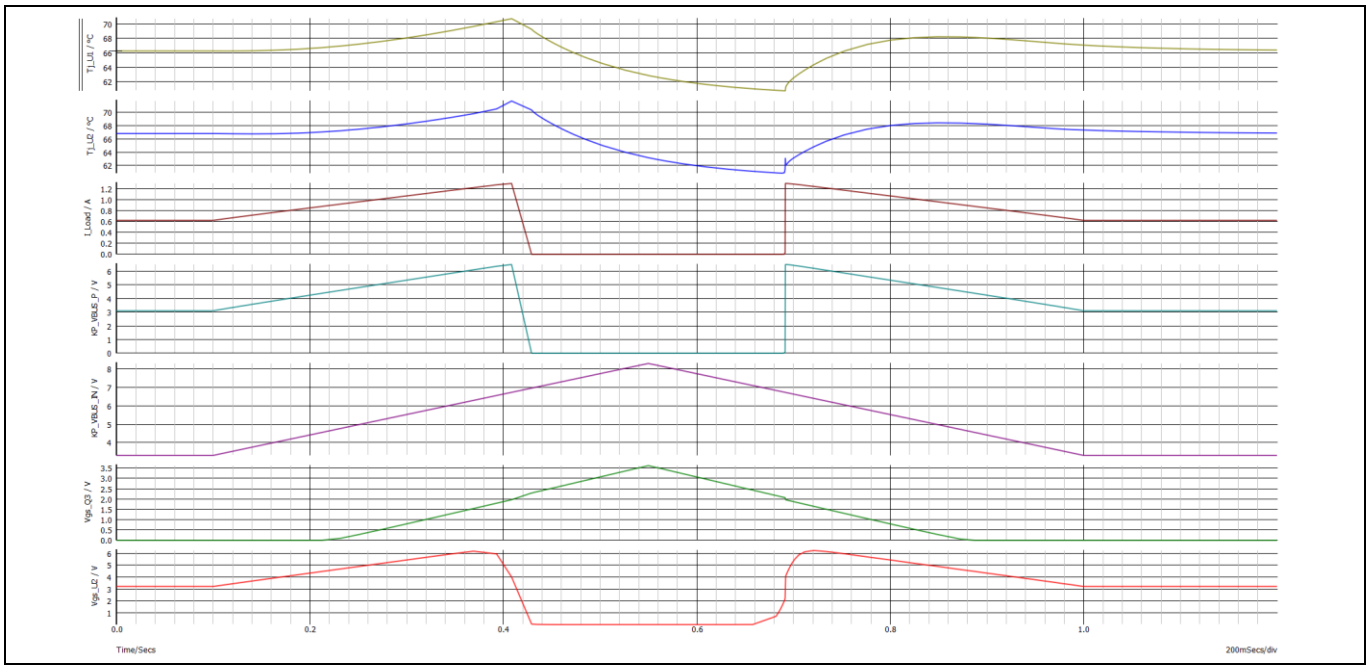


Figure 17 SPICE simulation result of a load switch with OVP

2.3 Start-up circuit

Figure 18 shows a use case of a depletion mode MOSFET in a start-up circuit. It has a flyback converter configuration. A depletion mode MOSFET has negative threshold voltage. In the configuration below, when current is not flowing through R, the MOSFET conducts. Current from V_{in} passes through the MOSFET as I_d current. After a while, according to negative threshold voltage generated by R and the I_d current, the I_d current is graduately decreased and reaches close to 0 A. The circuit below using this initial I_d current acts as kick-start current for an IC that generates a pulse-width modulation (PWM) signal. Once the IC generates PWM signal and the transformer has voltage at the secondary side, the IC is supplied operating VDD voltage through the transformer. The IC continues to operate even after the initial I_d current from the depletion MOSFET fades out. The initial I_d current through the depletion MOSFET has a gentle curve and is often used for a soft-start circuit. It protects the IC from inrush current caused by sudden start-up.

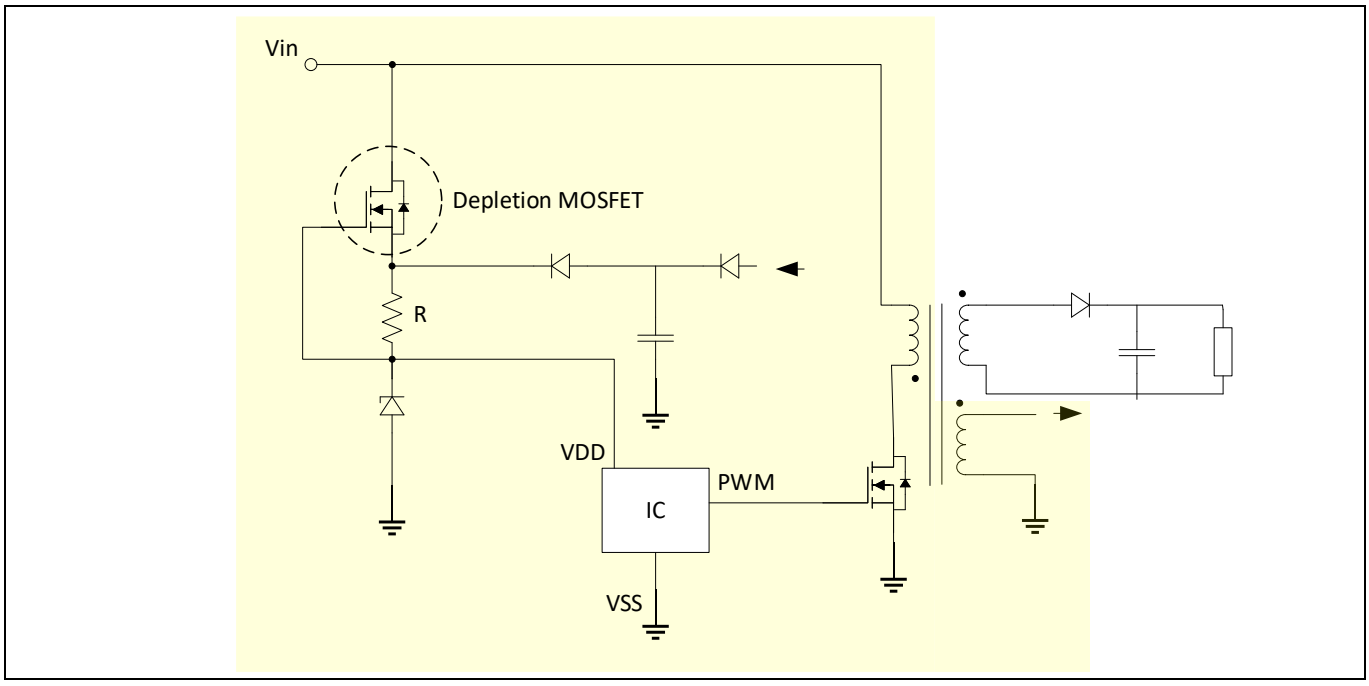


Figure 18 Typical start-up cuircuit with a depletion mode MOSFET

Figure 19 shows a simulation schematic of the circuit highlighted above in yellow. As shown in Figure 20, after V_{in} is presented, I_MOSFET starts flowing through the MOSFET and after activation of U2 this current is replaced by I_Secondary coming from the secondary part of the transformer. Until the initial I_d current of U1 is stopped by changing the voltage level of the soure, the current is controlled by R1 and softly supplieds power to U2.

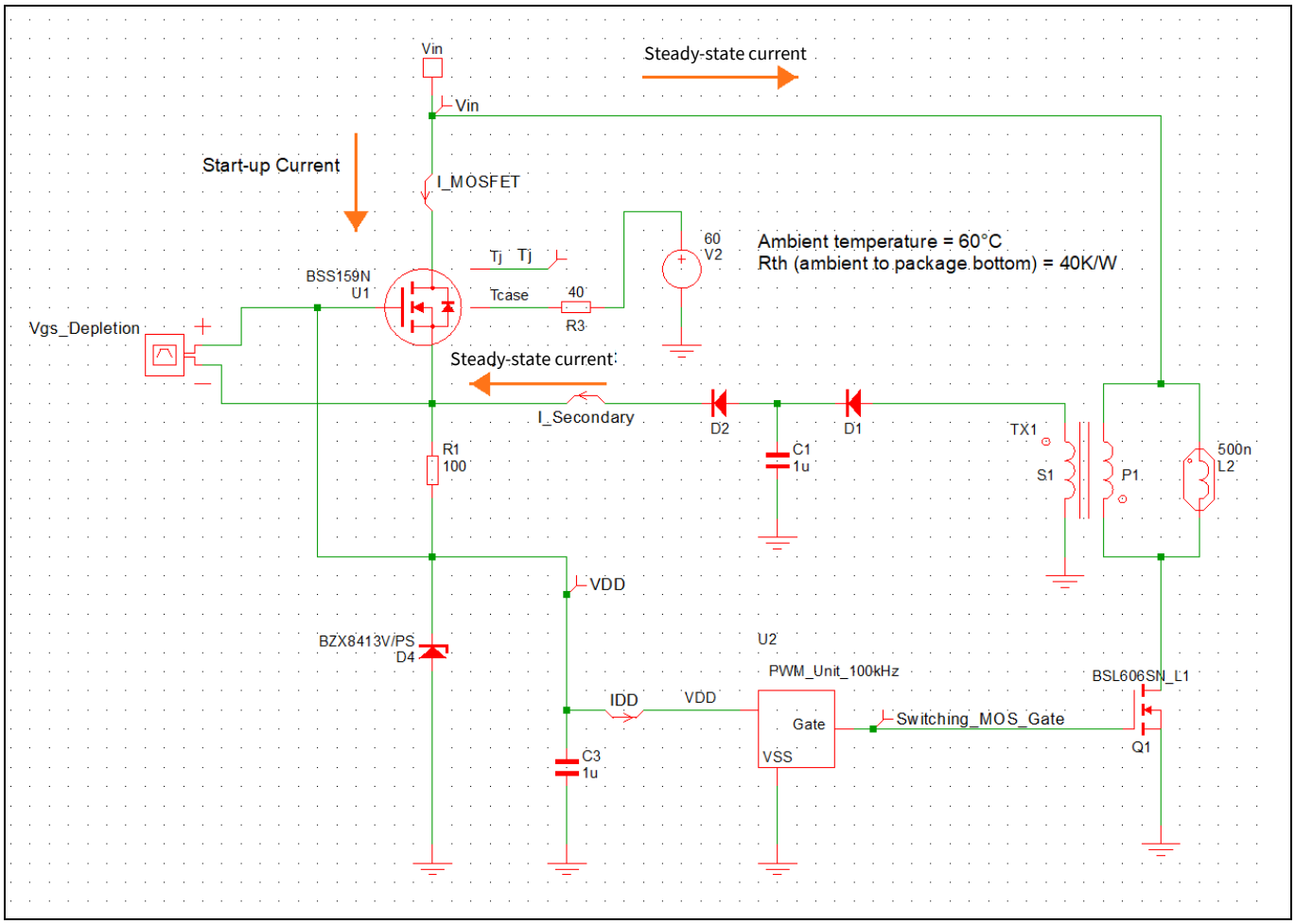


Figure 19 SPICE simulation schematic of start-up circuit with a depletion mode MOSFET

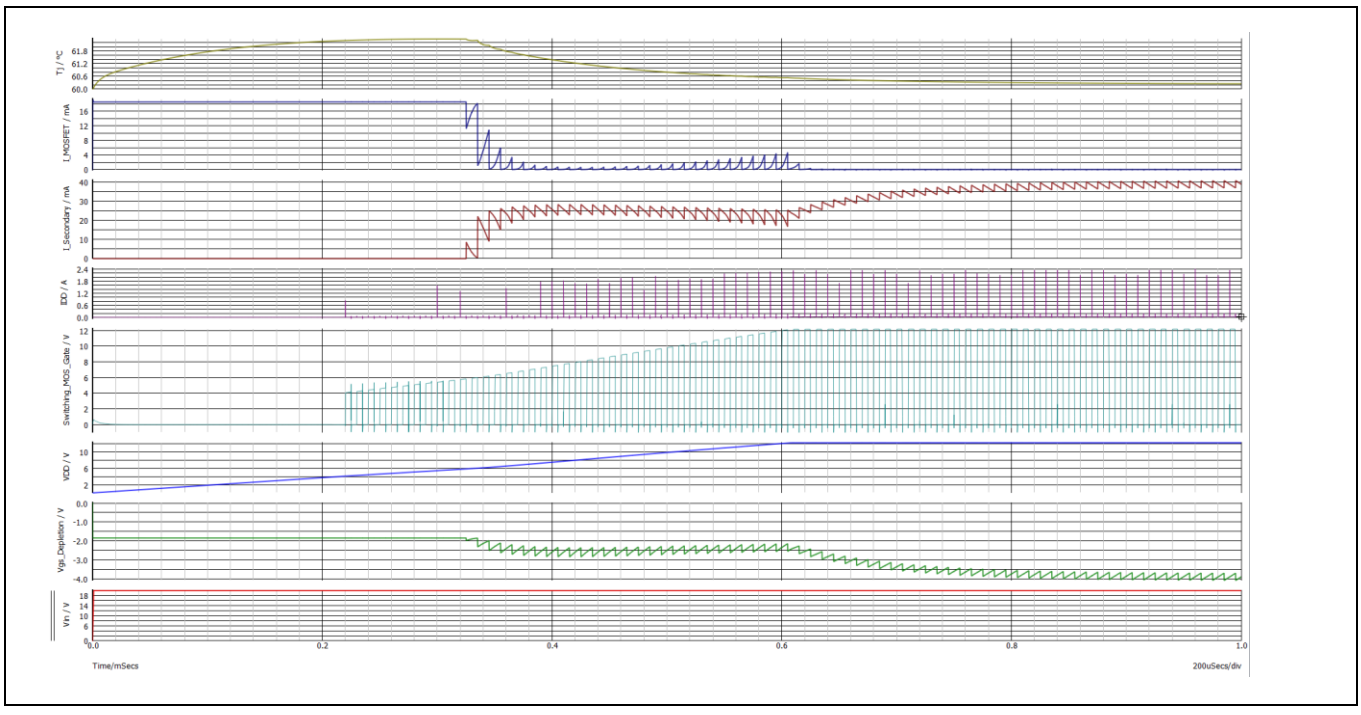


Figure 20 SPICE simulation result of start-up circuit with a depletion mode MOSFET

3 Connectivity

When an MCU communicates with other devices through a serial communication protocol such as I^2C, SPI, etc., logic levels of each interface have to be considered carefully, otherwise it may cause a communication error, which blocks stable communication. Each digital device has its own physical voltage level that allows the device to distinguish between high and low levels. Figure 21 shows a popular logic level that is frequently used in electrical applicances. Except where a high-speed signal has more than 100 MHz of clock frequency, for example Ethernet, PCIe, InfiniBand, etc., a level shifter circuit is often used for adjusting different logic levels in the communication category.

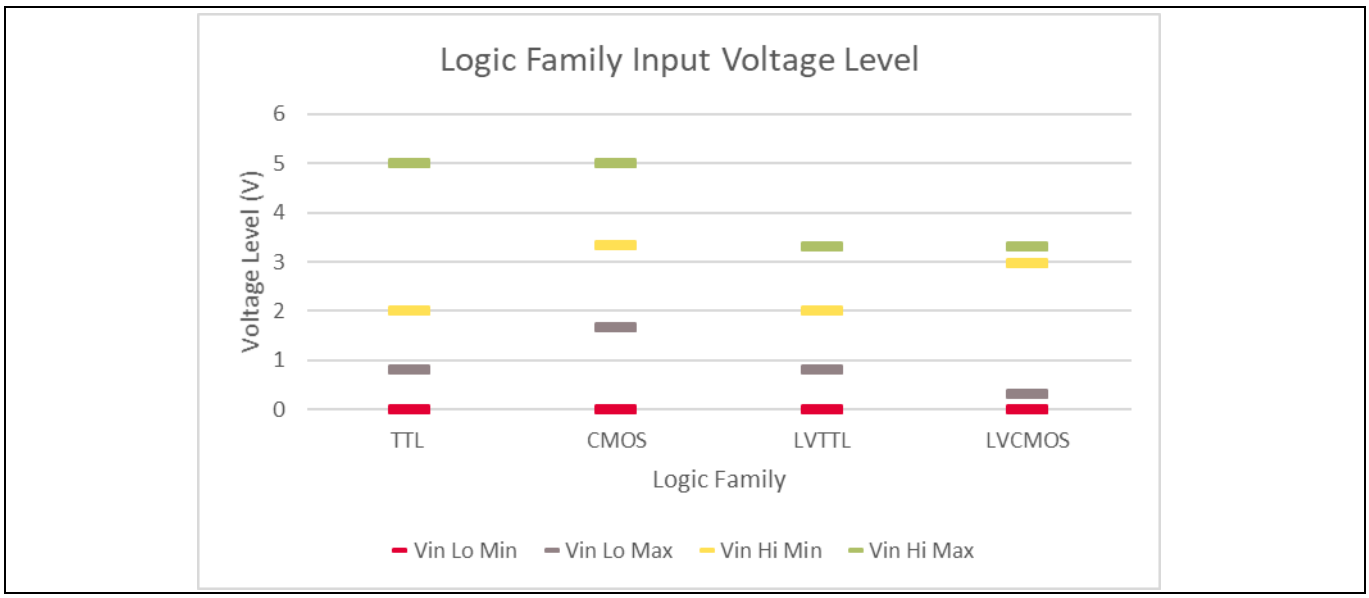


Figure 21 Logic family input voltage level

Figure 22 shows an example of a level shifter used in a computing board. 5 V and 3.3 V are frequently used voltage levels in general electrical appliances. But several digital components that require fast processing, like CPUs, usually use low voltage of less than 1 V. The digital signal doesn't need to have high drive current but it does need fast switching speed. In this use case, devices that have low Q_{gs} and low Q_{oss} are prefered.

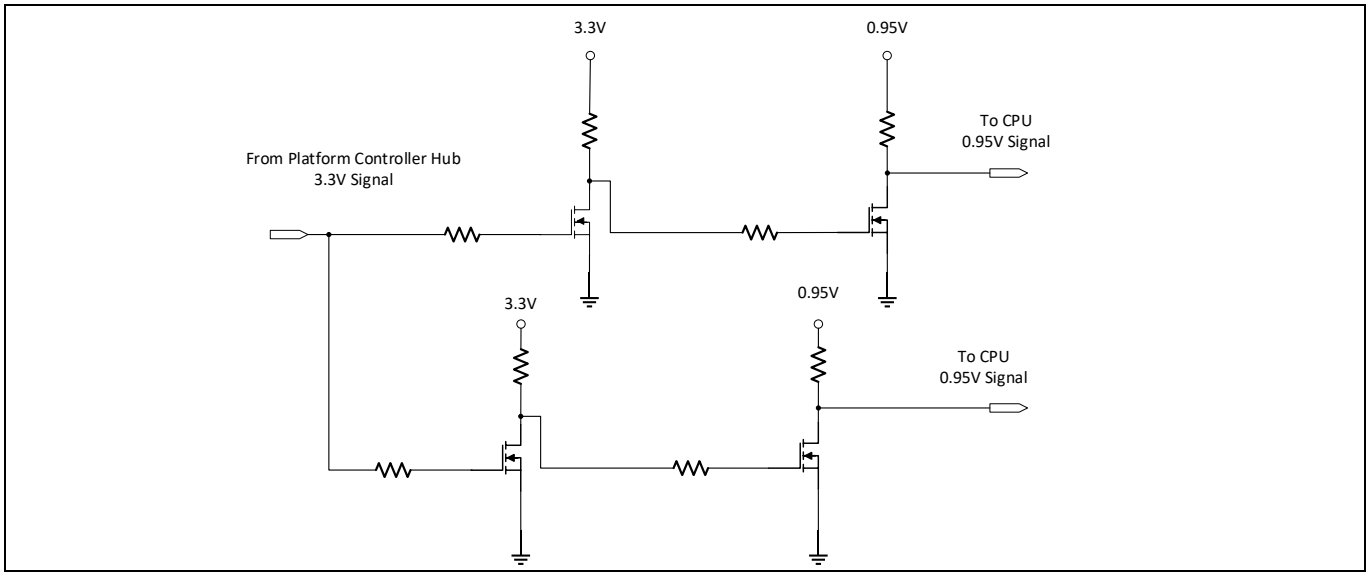


Figure 22 Level shifter between PCH and CPU signal

Figure 23 shows a use case of a MOSFET for a bus isolator circuit. Usually, this configuration is used when a board needs to be protected from standby signal that has to be isolated from mains power. In the example, unless VCC 3.3 V is powered, standby signal is blocked by the MOSFETs and components in a main board are protected before VCC 3.3 V is powered. This configuration works as a level shifter as shown in the simulation schematic in Figure 24.

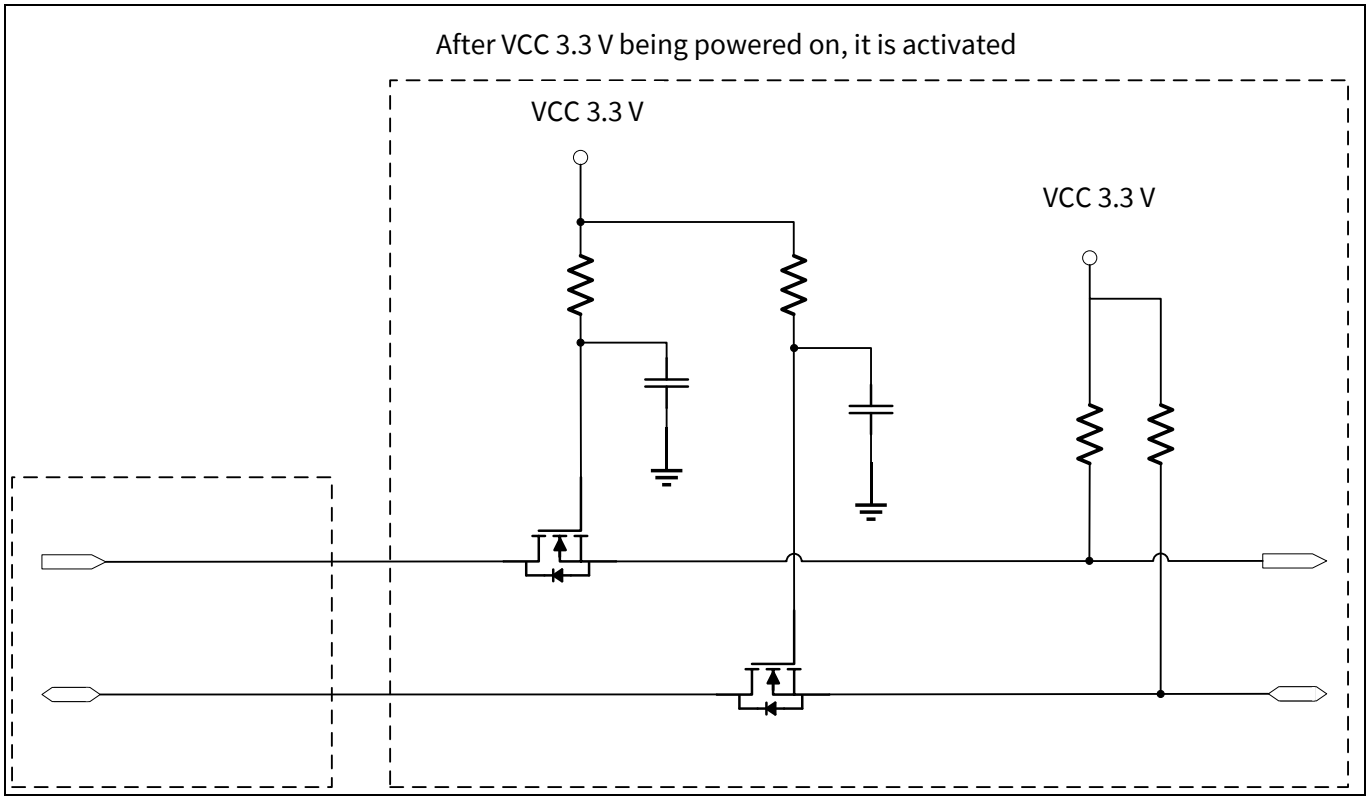


Figure 23 STDBY SM BUS isolator

Connectivity

This is an example of a level shifter from 3.3 to 5 V. It is often used for serial communication. Nowadays the communication speed is increased more than previously. I^2C has transmission speed with a range of 100 bps ~ 400 bps (50 kHz ~ 200 kHz) in normal mode, and fast mode reaches more than 1 Mbps. SPI is often used in 5 MHz ~ 10 MHz. Values of R3 and R4 adjust signal switching speed as shown in Figure 25, in which, according to the value of pull-up resistors R3 and R4, rise time and fall time of the signals are changing.

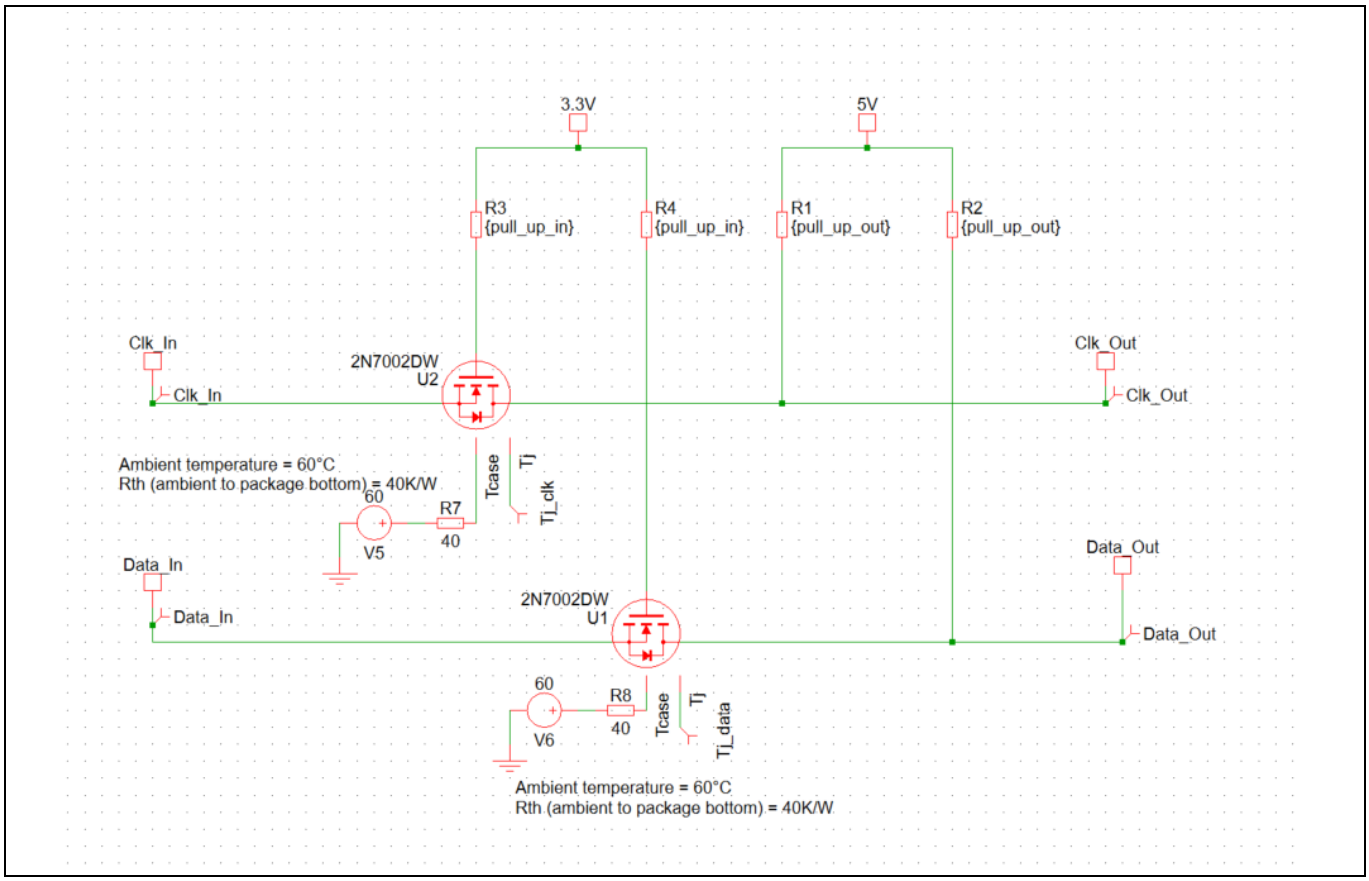


Figure 24 SPICE simulation schematic of a level shifter circuit

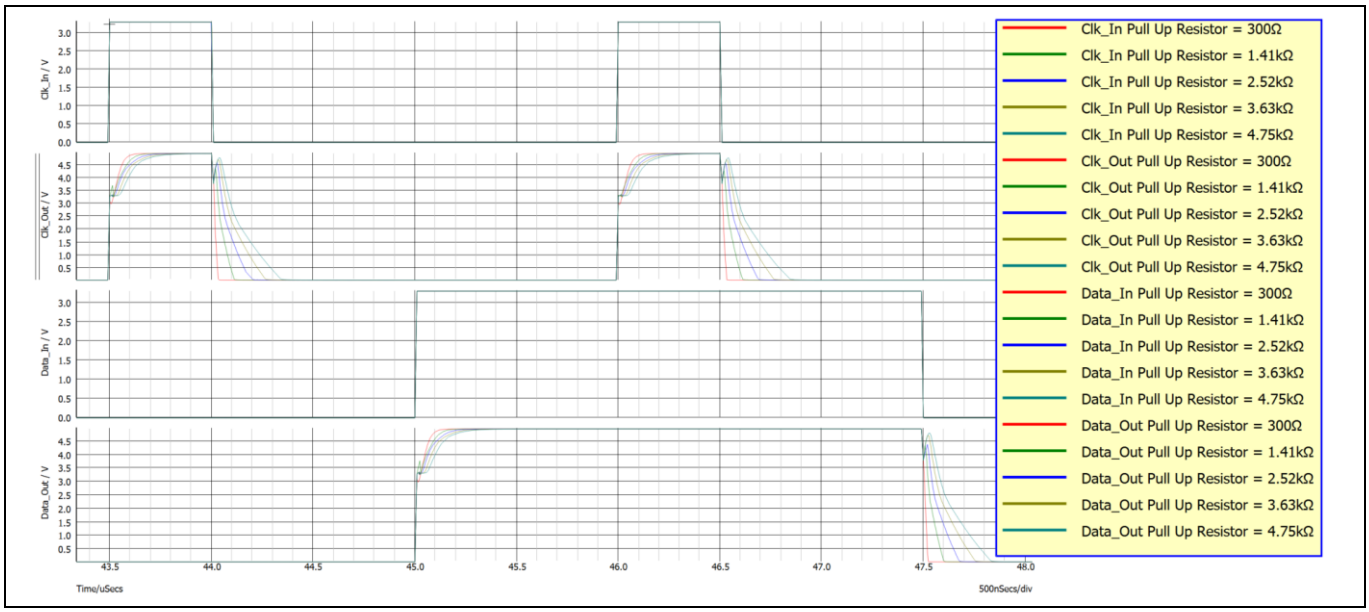


Figure 25 SPICE simulation result of a level shifter circuit

4 Peripherals

4.1 DC-DC

An MCU has peripheral functions. These are designed for specific purposes such as DC-DC converting, motor drive, and lighting. There are a lot of standalone digital controllers customized for this specific device as well. Infineon has published many application notes and released power MOSFET products targeted for SMPS application. Most of the technical information is therefore available elsewhere. In this application note, the concepts of cost and space saving configurations are introduced. Figure 26 is a block diagram of EVR in [7] and [8] (EVR switch mode topology (e) – 3.3 V single supply). This is a step-down DC-DC converter with buck converter topology. This application note is using a complementary MOSFET that has a p-channel and n-channel MOSFET inside. Other small-signal products can be applied in this configuration. It has a few components, so it saves on cost and space.

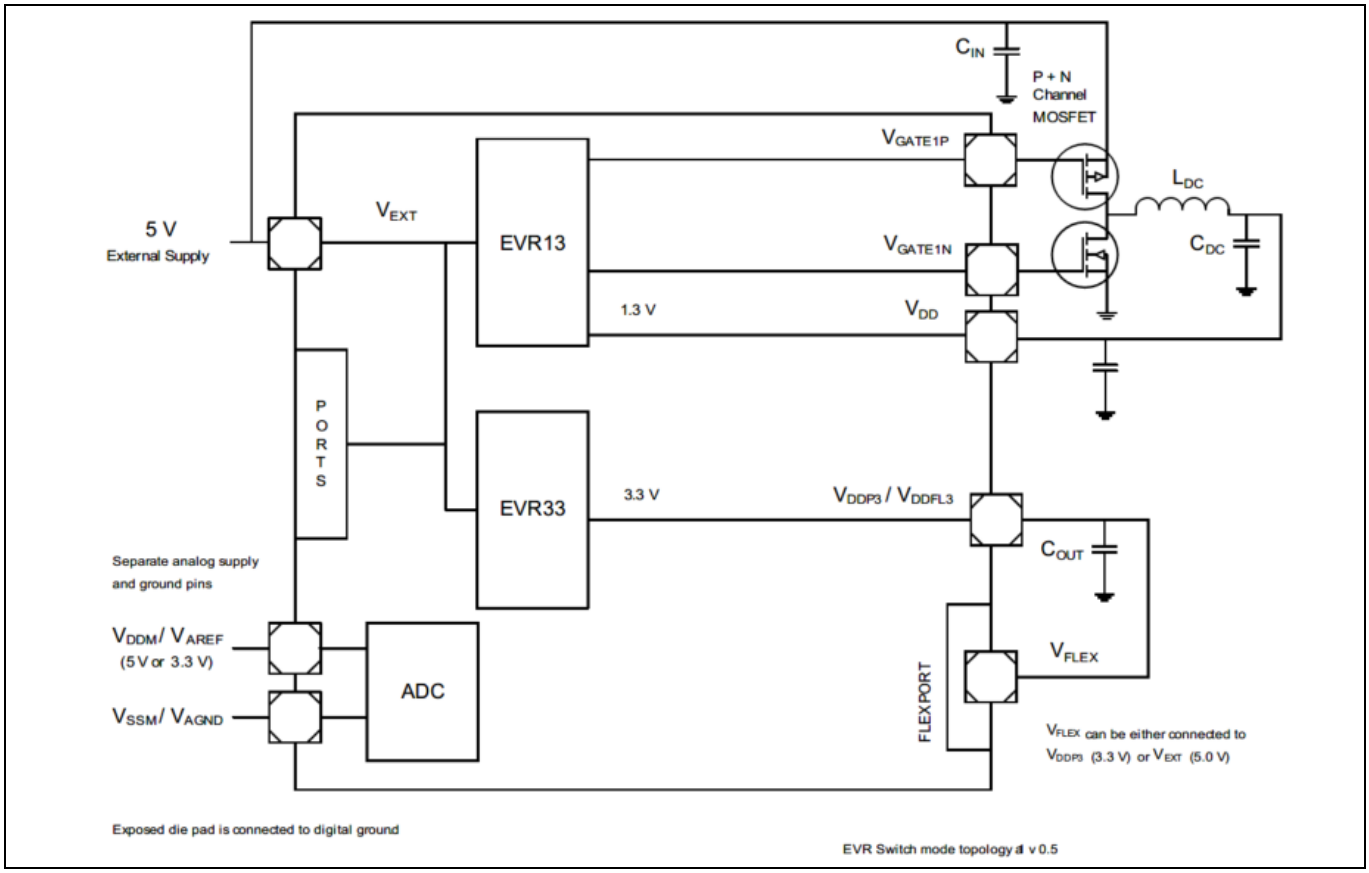


Figure 26 Block diagram of EVR

Figure 27 shows a simulation schematic of the same circuit as shown in Figure 26. Figure 28 shows the result of the simulation.

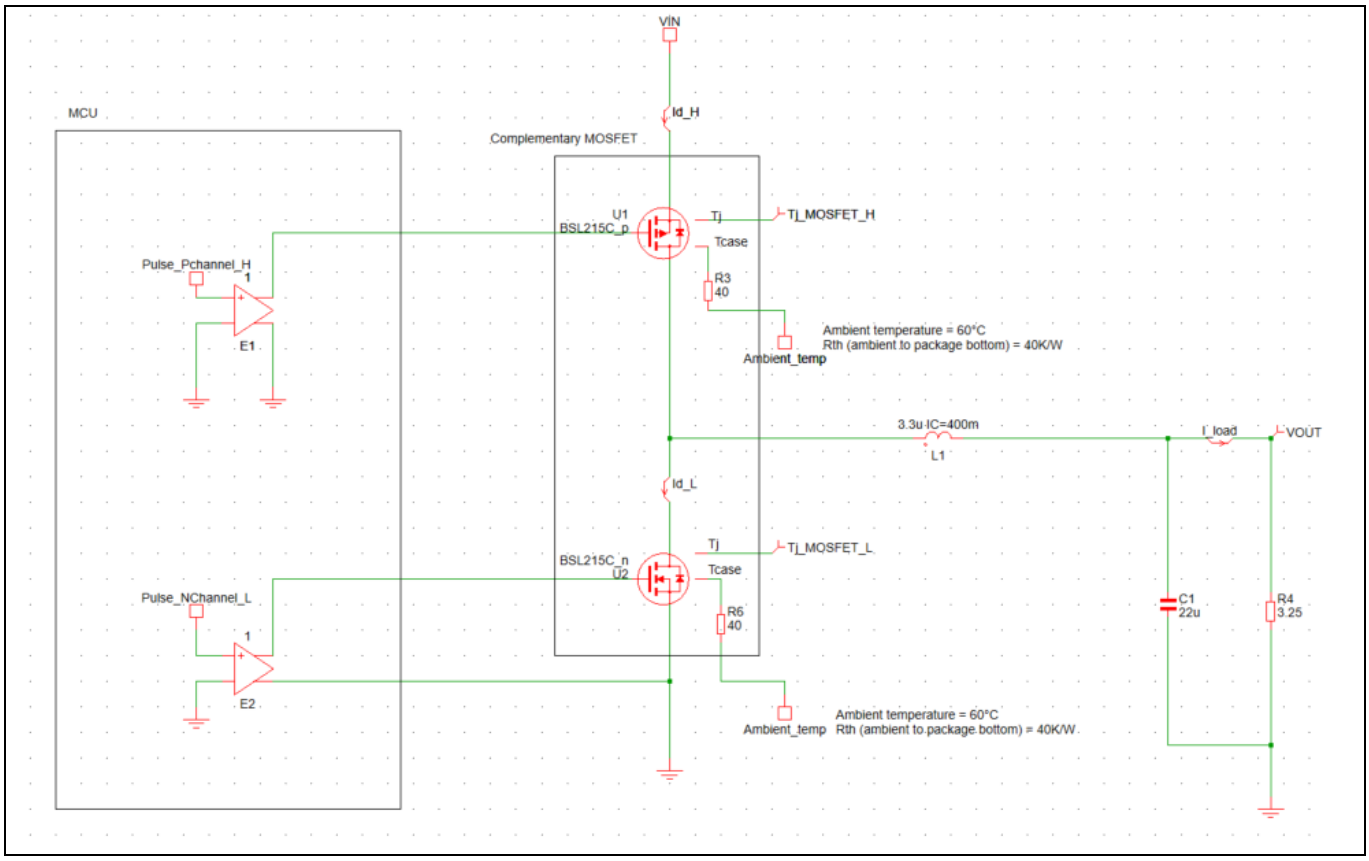


Figure 27 SPICE simulation schematic of buck converter with a complementary MOSFET

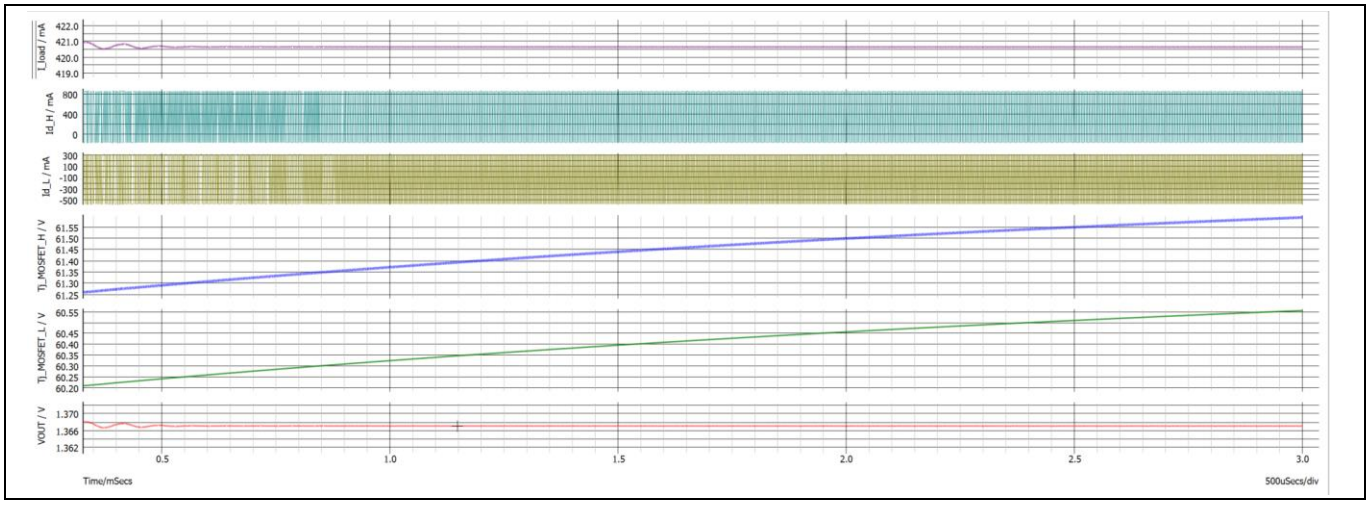


Figure 28 SPICE simulation result of buck converter with a complementary MOSFET

When a p-channel and n-channel MOSFET are used at high-side and low-side respectively in buck topology, short dead time settings cause an unexpected shoot-through issue, in which current flows through from high-side to low side because both sides are conducted at the same time. To avoid this, a proper period of dead time is required. Figure 29 and Figure 30 show different results of the dead time, in which Figure 30 shows a shoot-through event with insufficient dead time.

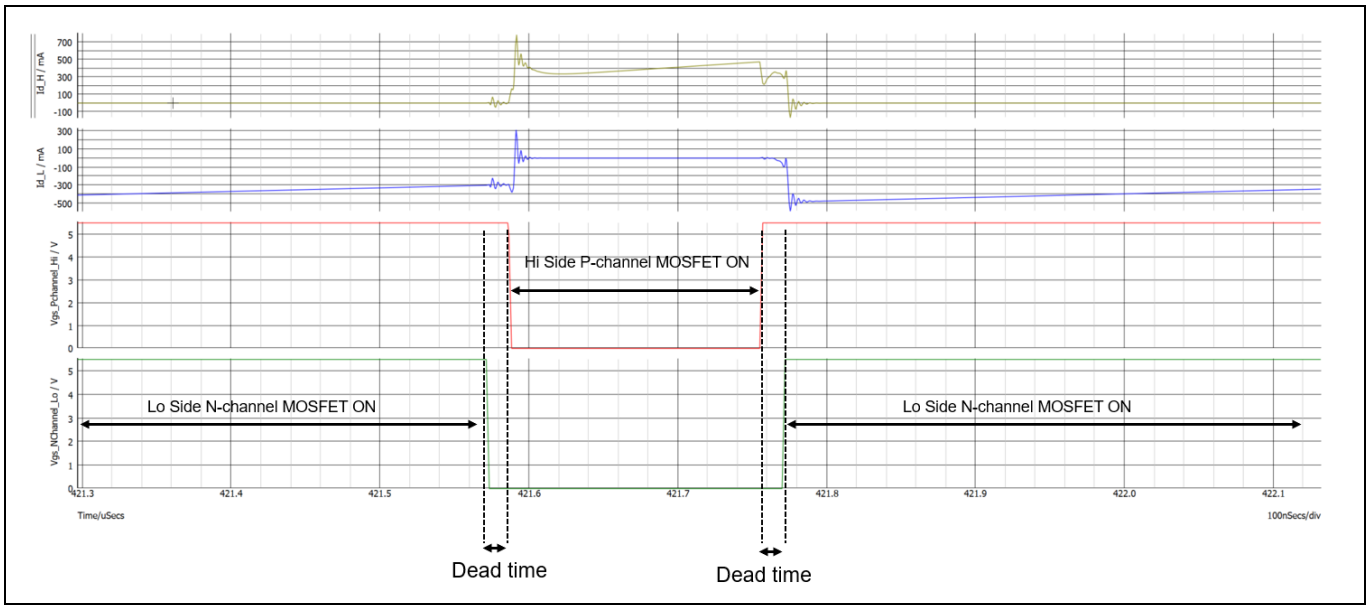


Figure 29 With proper dead time

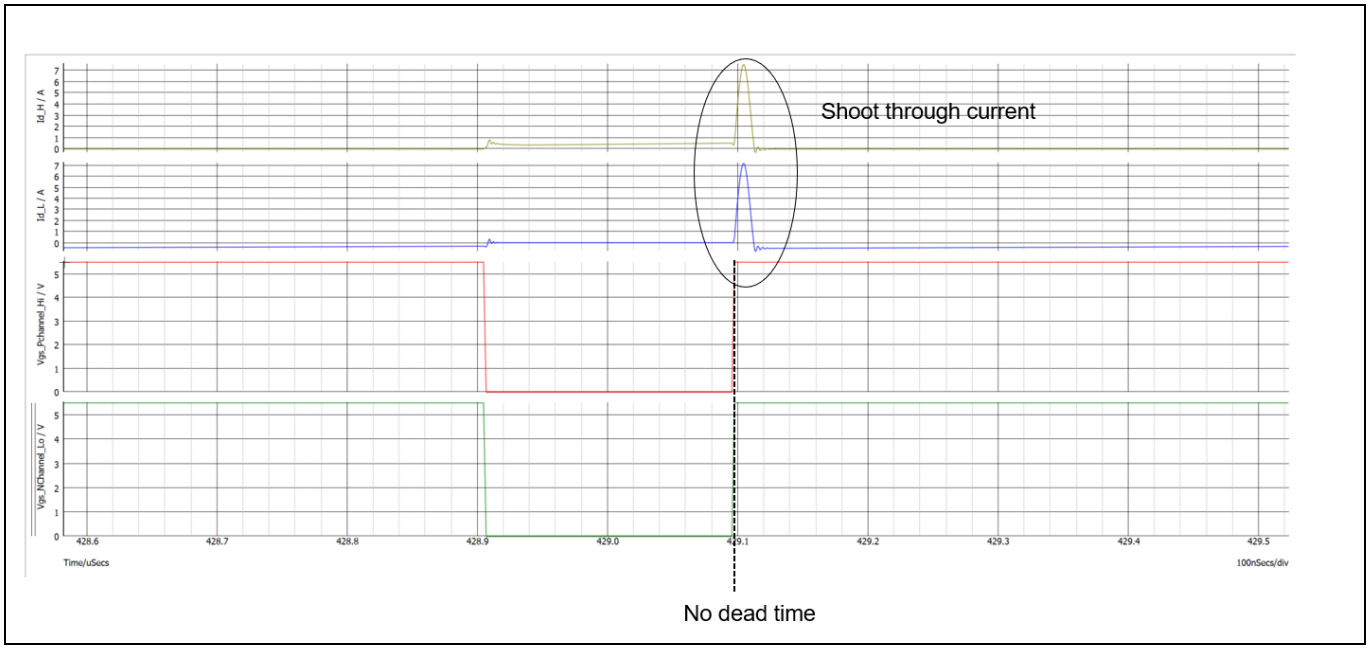


Figure 30 Without dead time

One of the benefits of this configuration is that it allows driving high-side and low-side with the same gate driver. (Routing on a PCB should be done carefully to preserve signal integrity.) Figure 31 and Figure 32 show a simulation schematic and the result in such a case. As shown, adjusting R_g is one of the methods for increasing dead time period.

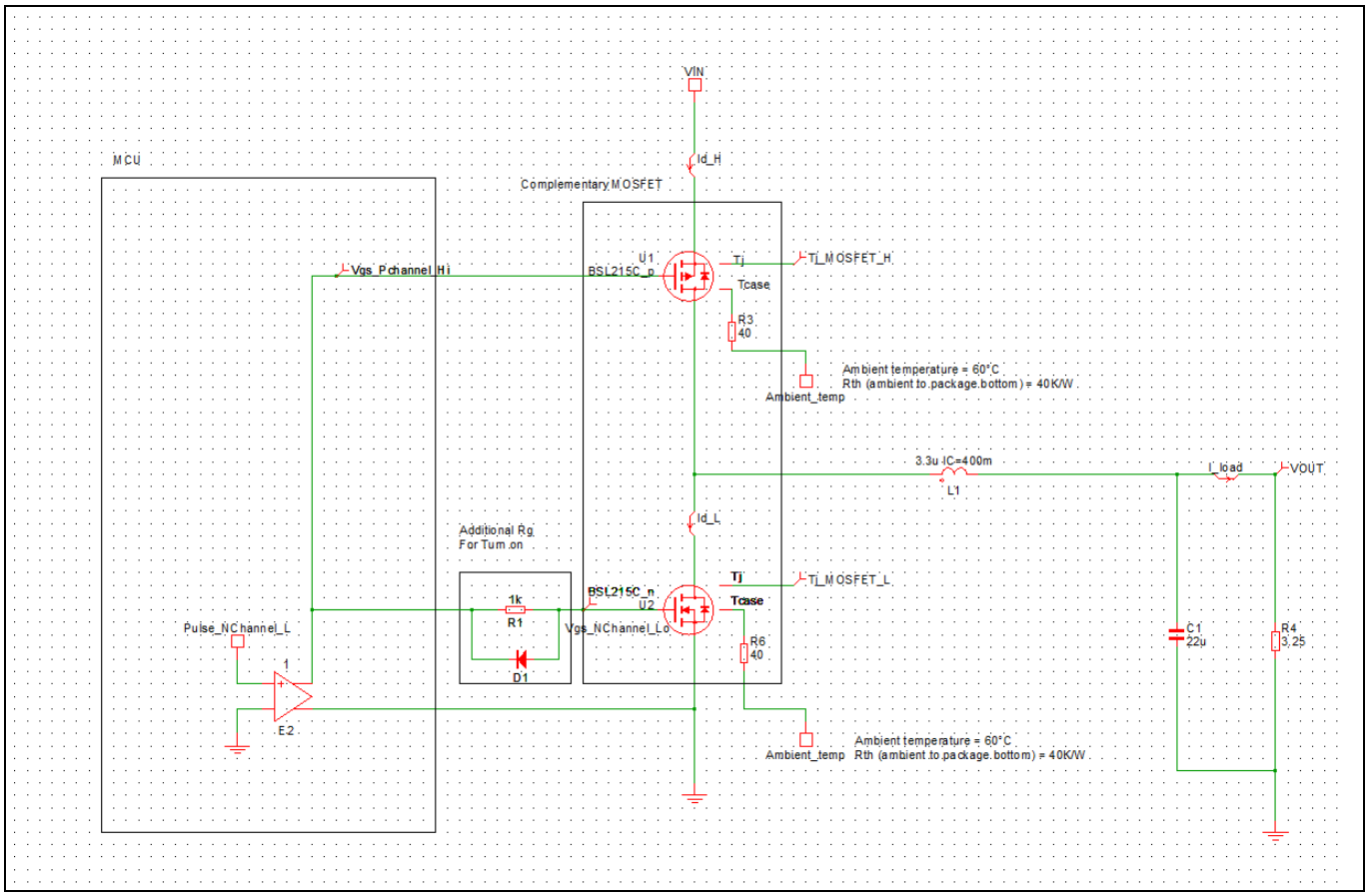


Figure 31 SPICE simulation schematic of buck converter with one gate driver

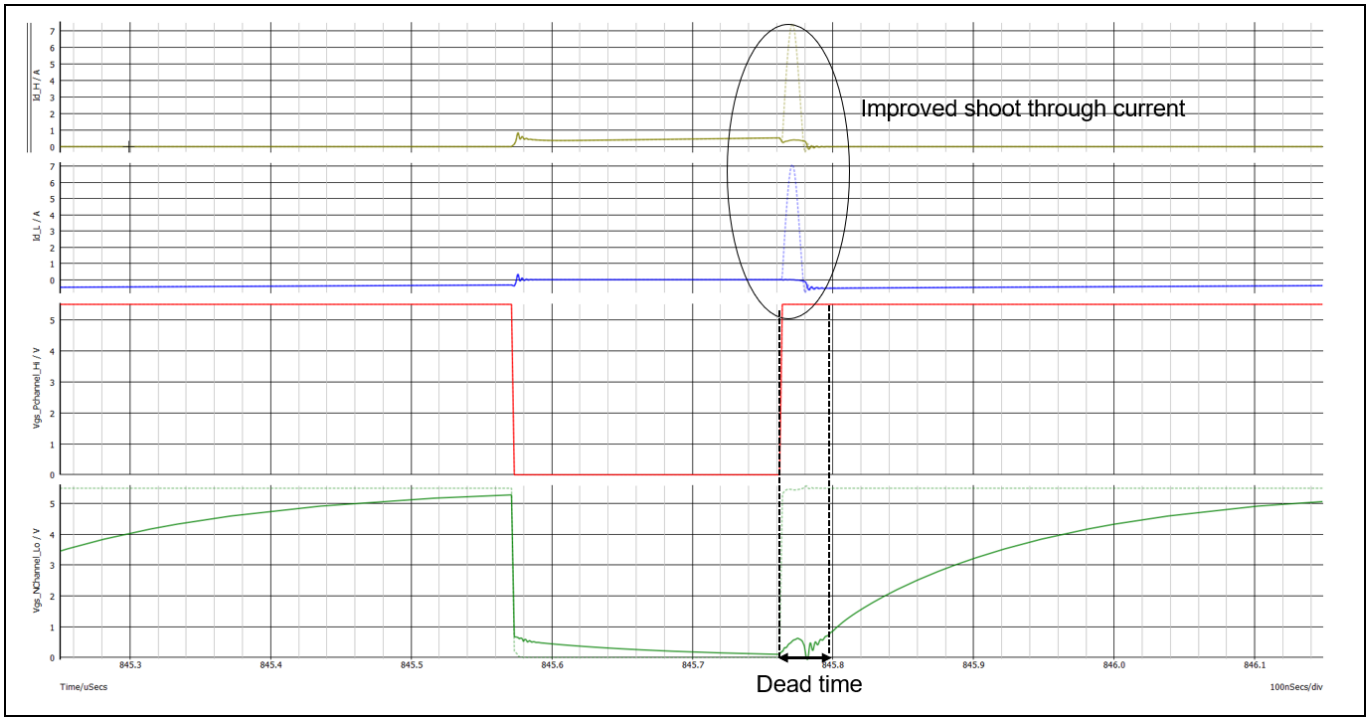


Figure 32 SPICE simulation result of buck converter with one gate driver

4.2 Drive

As before, for conventional technical information for drive applications, refer to other application notes published by Infineon. Here, further space and cost saving methods are introduced. Figure 33 shows typical applications requiring a computing board. One is an alarm system with a speaker, and the other is a cooling fan. Both of them need to drive a speaker and a fan with higher current. Small-signal products are often used for these applications.

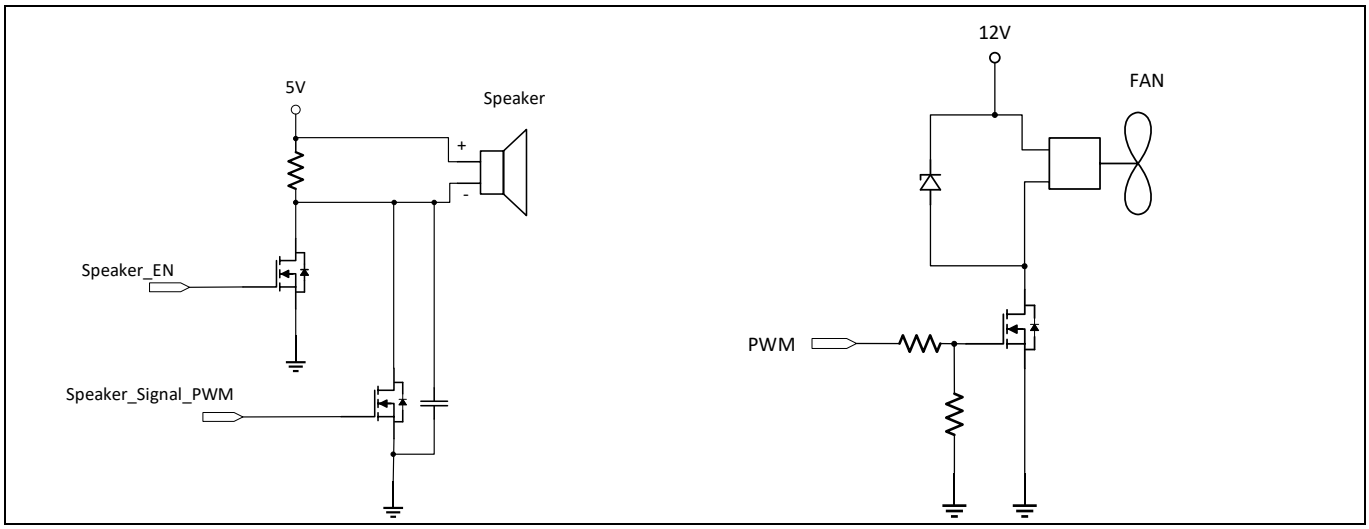


Figure 33 Example of current drive applications for a computing board

Figure 34 and Figure 35 show a simulation schematic and the result of a motor drive circuit. In this simulation a very simple driving technique was used. Regarding more sophisticated motor drive techniques, Infineon has published many useful application notes, which can be referred to. In motor applications, a MOSFET that drives high current has an inductive load. The value of R_g should be considered to avoid an aggressive ringing spike in the V_{DS} waveform. The heat dissipation path should also be designed carefully.

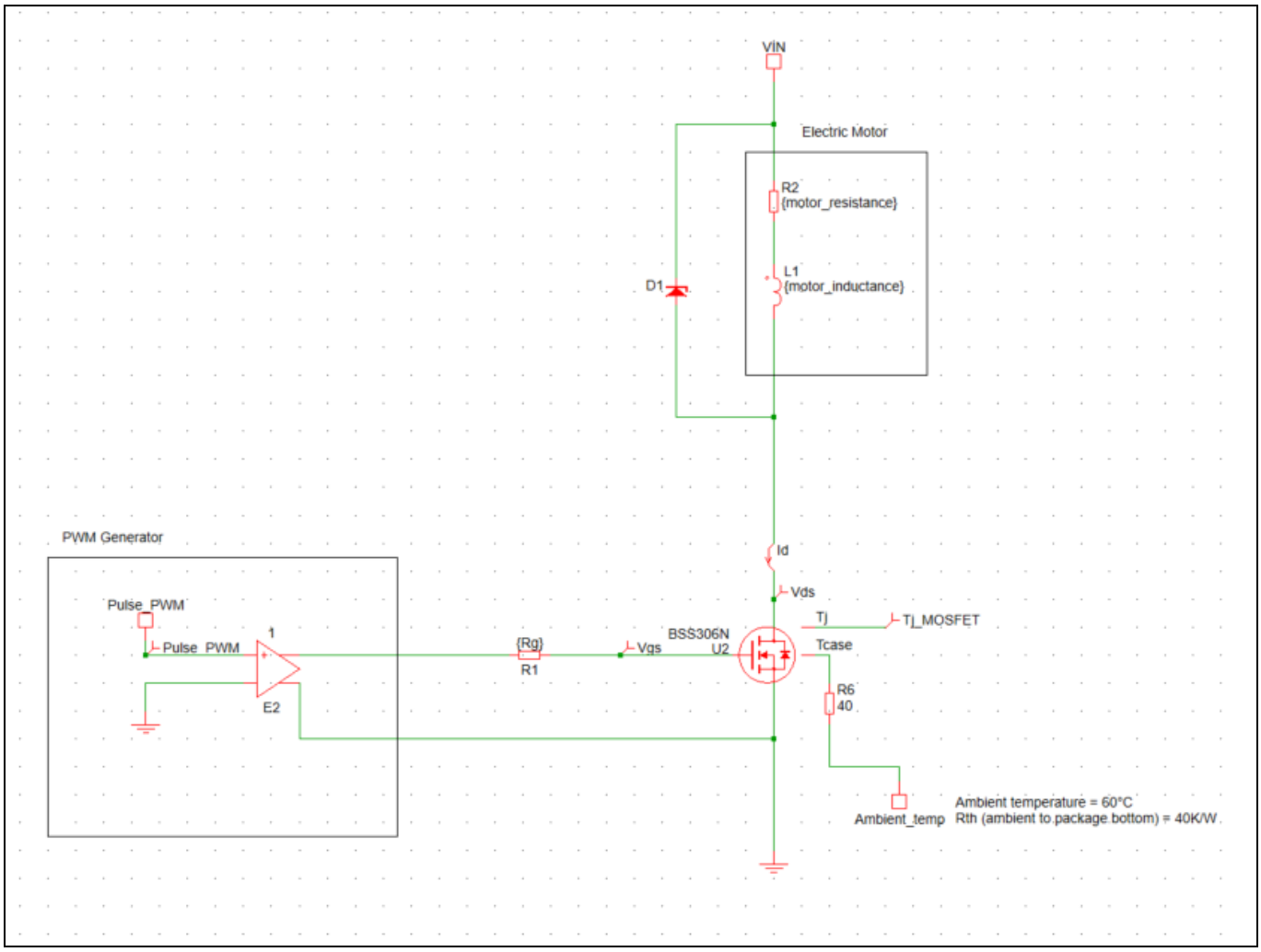


Figure 34 SPICE simulation schematic of a simple motor drive circuit

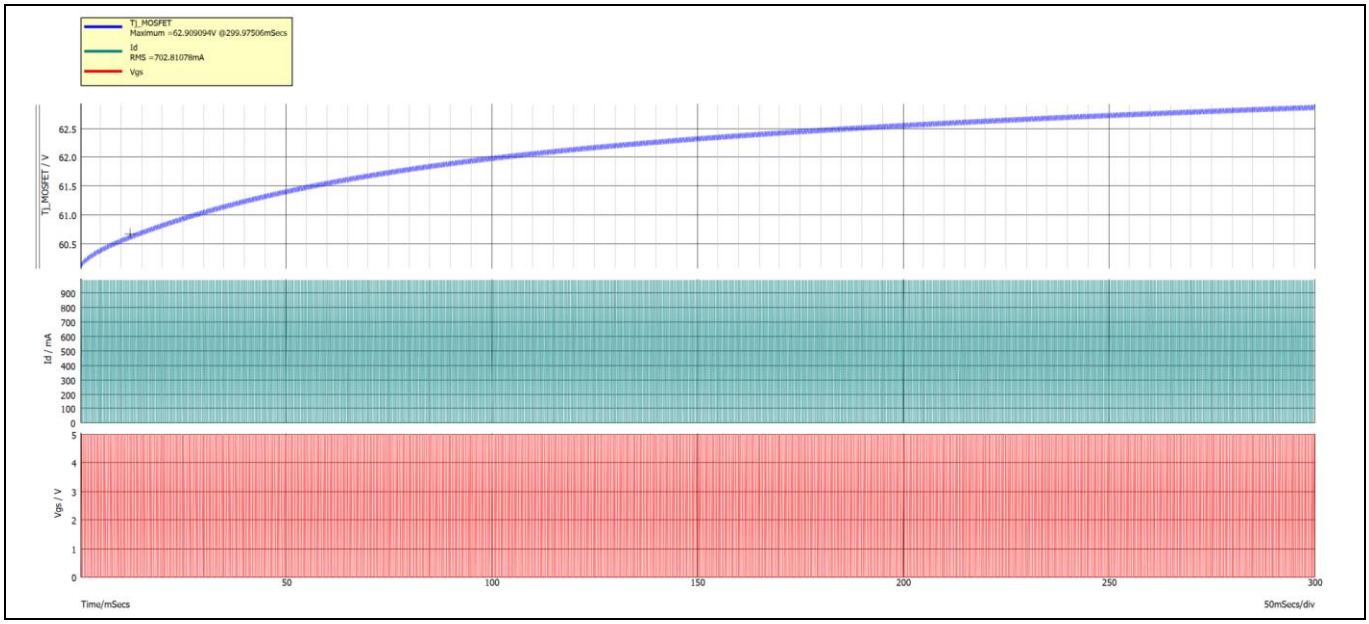


Figure 35 SPICE simulation result of a simple motor drive circuit

4.3 Lighting

Lighting is a highly demanding application for small-signal products. Because of small package size and low cost, they are preferred over other power MOSFETs. Figure 36 shows a typical driving method for LED. Theoretically these have a similar configuration as DC-DC in order to maintain constant current and high efficiency. A dimming technique can be used to adjust the brightness of LEDs except for drive current.

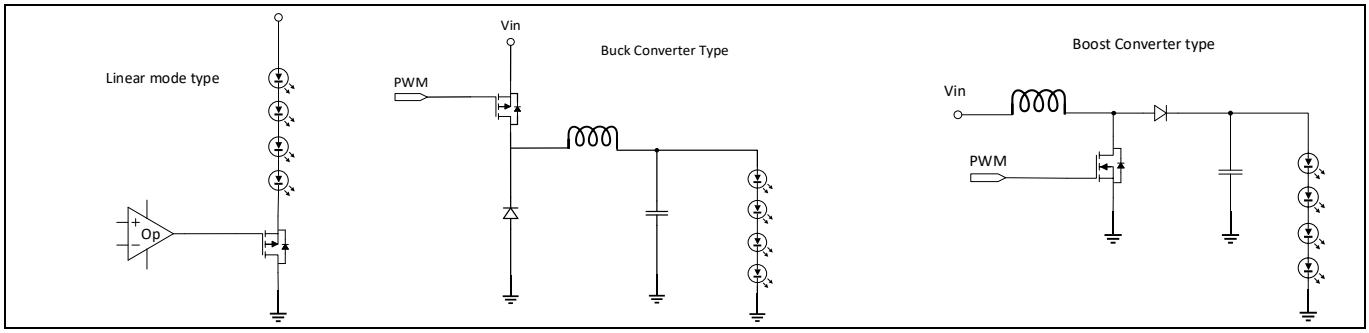


Figure 36 Examples of LED drive circuits

Figure 37 shows a simulation schematic of a buck converter type with a p-channel MOSFET for dimming pulse. An n-channel MOSFET switches at higher frequency than a p-channel MOSFET and acts as a switching MOSFET in a buck converter. A p-channel MOSFET acts as the dimming control. Drive current for LEDs flows only when the p-channel MOSFET is switched on. PWM sending to a p-channel MOSFET controls the brightness of the LEDs.

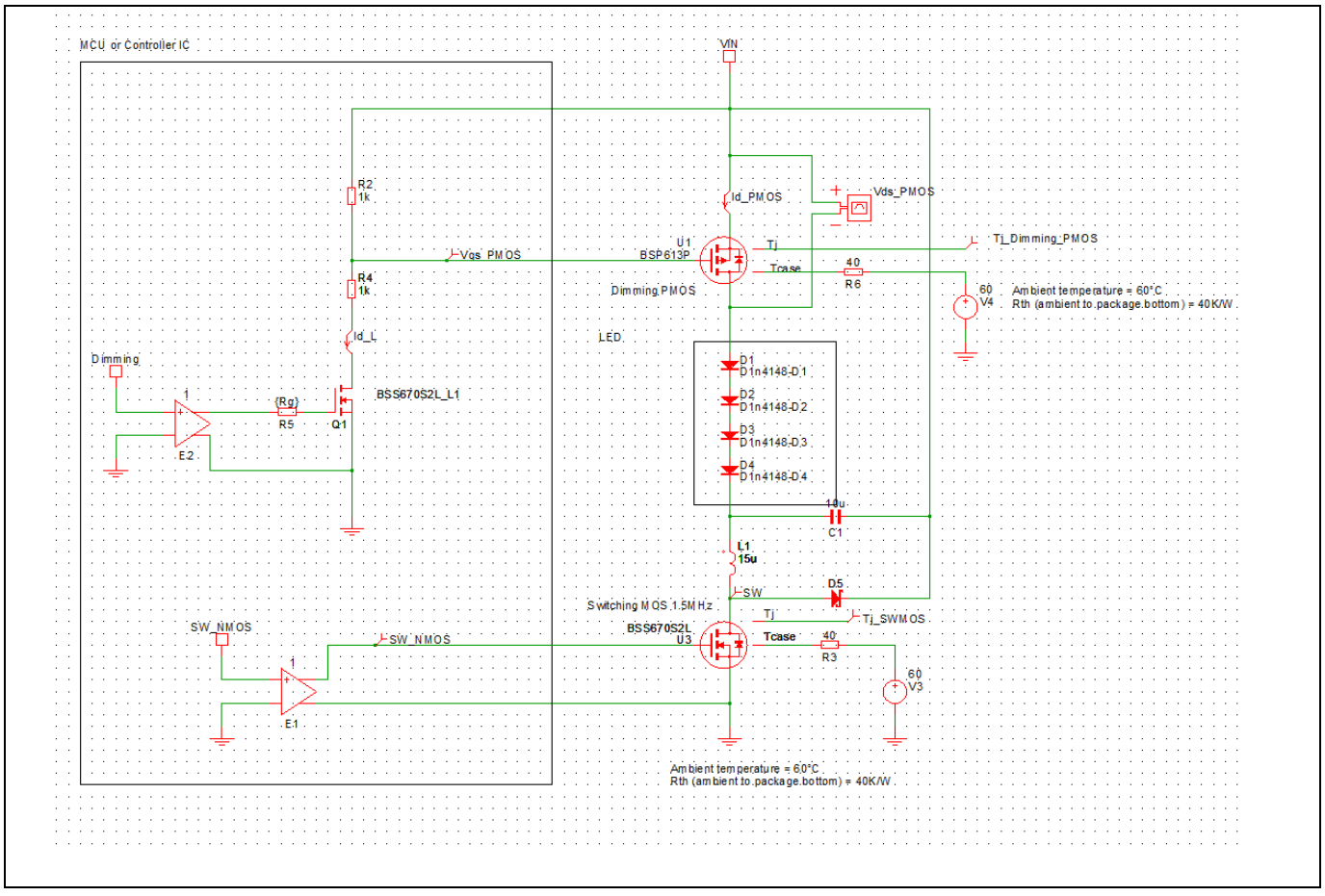


Figure 37 SPICE simulation schematic of buck converter LED drive circuit

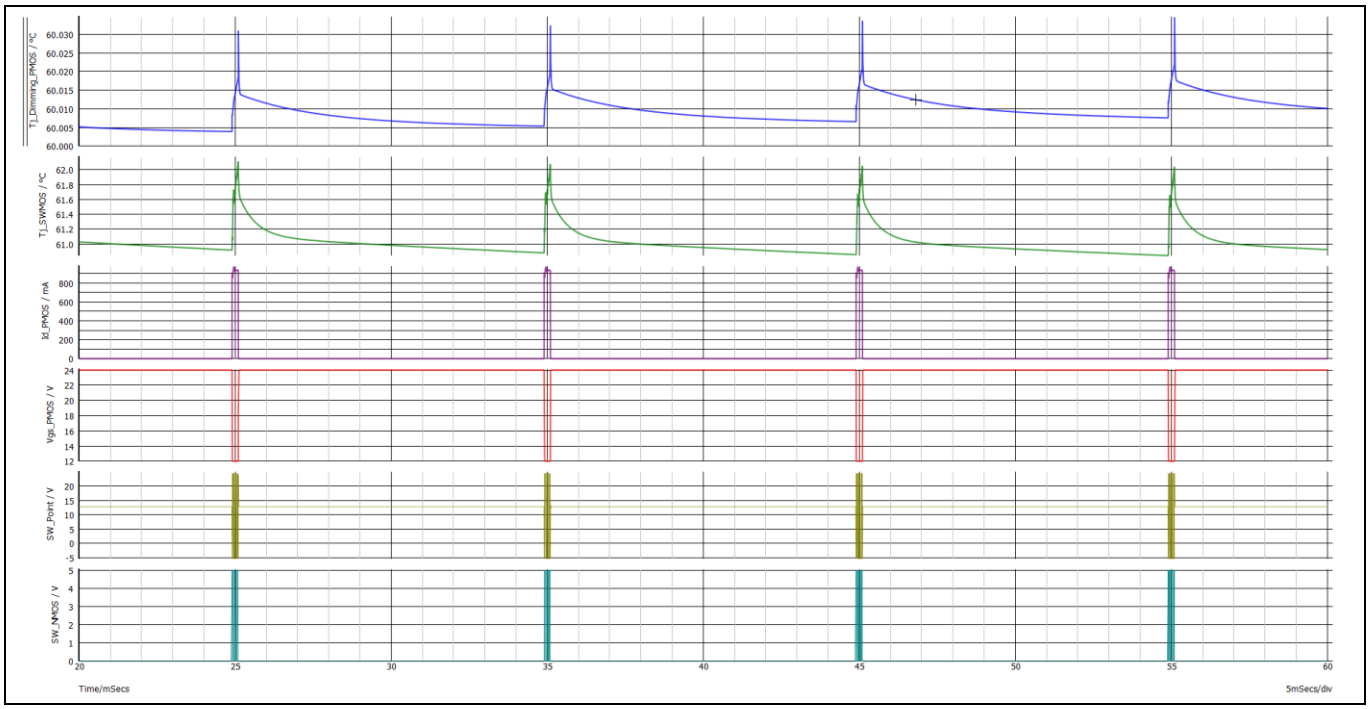


Figure 38 SPICE simulation result of buck converter LED drive circuit

5 How to see probing points in SPICE simulation example

Figure 39 shows the probe symbols used in a schematic and how this might be shown in a graph as a simulation result. In this application note all of the simulations are done in transient analysis, and it shows the time sequence of each probing point in each unit. The graph shows how each value is changing in the same time frame.

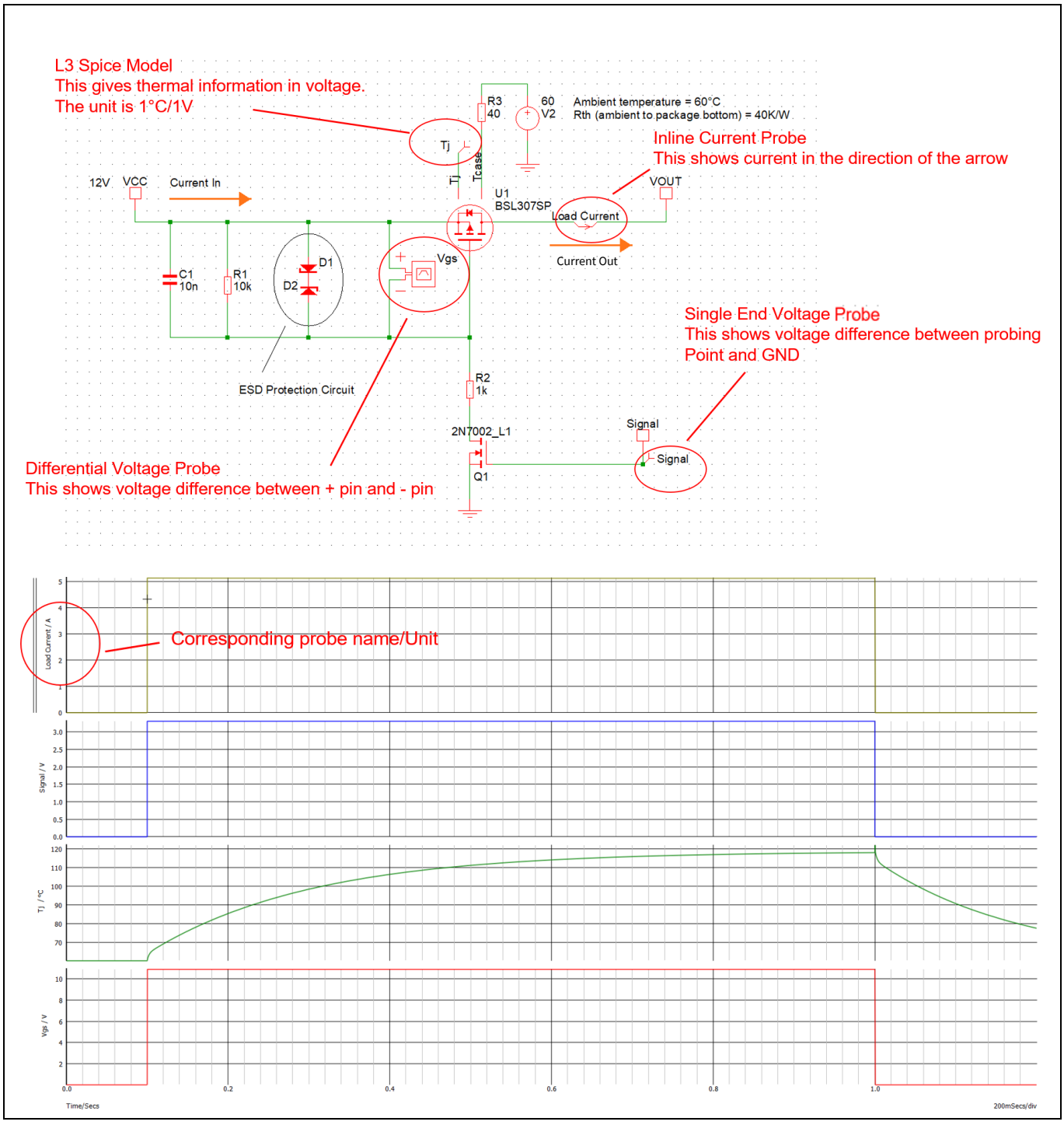


Figure 39 SPICE simulation of probing points and result

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V 1.0	2024-02-29	Initial release

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