CIPOS™ Prime products technical description

About this document

Scope and purpose

This application note describes the CIPOS™ Prime molded modules and the basic requirements for operating these products in the recommended mode. It includes information about the integrated components and the design of the required external circuitry.

Intended audience

The intended audiences for this document are design engineers, technicians, and developers of electronic systems.

Key points

- Internal circuitry
- Package inductance
- Interface circuit and layout

About this product family

Product family

The CIPOS™ Prime products offer an integrated solution for high-frequency power conversion applications. The power modules include four or six SiC MOSFETs and an NTC to enable high power density. The direct copper bonding (DCB) substrate enables optimal thermal performance as well as electrical insulation. The package, meanwhile, is designed to ensure a high creepage distance.

Target applications

- On-board chargers (OBC): Application web page
- DC-DC converters: Application web page
- Electric vehicle (EV) charging: Application web page
- AC-DC and DC-AC power conversion: Application web page

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1 Introduction

CIPOS™ Prime products are available in 4-pack and 6-pack configurations with different pin maps. Table 1 gives an overview.

1.1 Product lineup

Table 1 Products covered in this application note

Product name	Rated voltage	$R_{DS(on)}$ at 25°C	Configuration
AMM12S18LB1Z	1200 V	18 mΩ	6-pack type 1
AMM12S25LB1Z		25 mΩ	
AMM12S36LB1Z		36 mΩ	
AMM12S54LB1Z		54 mΩ	
AMM12S62LB1Z		62 mΩ	
AMM12S36LB1Z2		18 mΩ + 36 mΩ	6-pack type 1 2 x 18 mΩ + 4 x 36 mΩ
AMM12S54LB2Z		54 mΩ	6-pack type 2
AMM12S62LB2Z		62 mΩ	
AMF12S18LB2Z	1200 V	18 mΩ	4-pack type 2
AMF12S25LB2Z		25 mΩ	
AMF12S36LB2Z		36 mΩ	
AMF12S54LB2Z		54 mΩ	
AMF12S62LB2Z		62 mΩ	

1 Introduction

1.2 Nomenclature

The nomenclature of the CIPOS™ Prime products is shown in Figure 1.

1	2	3	4		5	6		7	8	9		
A	M	M	1	2	S	1	8	L	B	(x)	(x)	(x)

1. Qual grade

A	Automotive
(blank)	Industrial

2. Gate driver option

I	IPM: with integrated gate driver
M	MM: molded module without gate driver

3. Configuration

F	4-pack
M	6-pack

4. Voltagte class

1 2	1200 V

5. Power switch technology

S	SiC
G	GaN

6. On resistance

1 8	18 mOhm

7. Package option

L	DIP 44x28DA
M	

8. Derivatives

B	The second generation of SiC MOSFET

9. Other options

1			Pin map 1
2			Pin map 2
	Z		Zig-zag pin
		2	Two different chips

Figure 1 CIPOS™ Prime product nomenclature

2 Internal components and package technology

2.1 1200 V CoolSiC™ MOSFET

Silicon carbide (SiC) as a compound semiconductor material is formed by silicon (Si) and carbon (C). SiC has ten times the electric breakthrough field, allowing for thinner epitaxial layers to support higher blocking voltage in power devices compared to Si. The thinner and highly doped drift layer leads to a much lower drift resistance. This results in low forward voltage and low conduction loss, while maintaining the high blocking voltage. With a high electric breakthrough field, SiC can be used specially in high-voltage unipolar devices such as MOSFETs and Schottky diodes, providing low switching loss. Infineon has introduced a truly “normally off” SiC MOSFET using the trench technology under the trademarked name, CoolSiC™. The second generation, G2, of the CoolSiC™ MOSFET, reduces power loss and extends the gate-source voltage range while maintaining the high reliability of G1.

2.2 Thermistor

In the CIPOS™ Prime, the thermistor is located on the DCB. The T1 and T2 pins provide direct access to the thermistor. Table 2 shows the thermistor’s resistance depending on the temperature.

Table 2 Raw data of the thermistor used in CIPOS™ Prime

Temperature [°C]	R_{min} [kΩ]	R_{typ} [kΩ]	R_{max} [kΩ]	Temperature [°C]	R_{min} [kΩ]	R_{typ} [kΩ]	R_{max} [kΩ]
-40	291.8	307.6	324.1	60	2.397	2.479	2.562
-35	215.8	226.8	238.3	65	2.002	2.074	2.147
-30	160.9	168.7	176.7	70	1.68	1.743	1.808
-25	120.9	126.4	132.1	75	1.417	1.472	1.529
-20	91.55	95.45	99.47	80	1.199	1.248	1.298
-15	69.31	72.06	74.9	85	1.021	1.064	1.108
-10	52.92	54.88	56.89	90	0.8721	0.9104	0.95
-5	40.73	42.13	43.57	95	0.7481	0.7821	0.8173
0	31.59	32.59	33.62	100	0.6442	0.6744	0.7057
5	24.63	25.36	26.1	105	0.557	0.584	0.6119
10	19.36	19.88	20.42	110	0.4834	0.5074	0.5324
15	15.33	15.71	16.09	115	0.4209	0.4424	0.4648
20	12.22	12.49	12.77	120	0.3676	0.3869	0.407
25	9.8	10	10.2	125	0.3223	0.3396	0.3577
30	7.879	8.056	8.234	130	0.2834	0.299	0.3153
35	6.372	6.529	6.687	135	0.25	0.264	0.2788
40	5.184	5.321	5.46	140	0.2211	0.2338	0.2471
45	4.24	4.361	4.48	145	0.1961	0.2076	0.2197
50	3.486	3.592	3.699	150	0.1743	0.1848	0.1957
55	2.883	2.976	3.071				

2 Internal components and package technology

2.3 Package technology

The ceramic layer of the DCB in the CIPOS™ Prime package provides excellent thermal contact with the heat sink while providing electric insulation. Figure 2 shows the external view of the CIPOS™ Prime package. Please refer to the application note AN-2026-01 [1] for details.

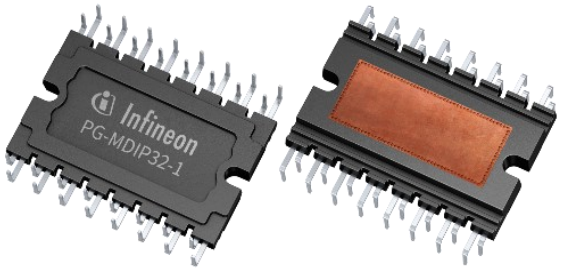


Figure 2 External view of the CIPOS™ Prime package

3 Product overview

3.1 Internal circuitry

Figure 3 shows the internal block diagram of the CIPOS™ Prime modules. There are two topology variants – the 4-pack and the 6-pack.

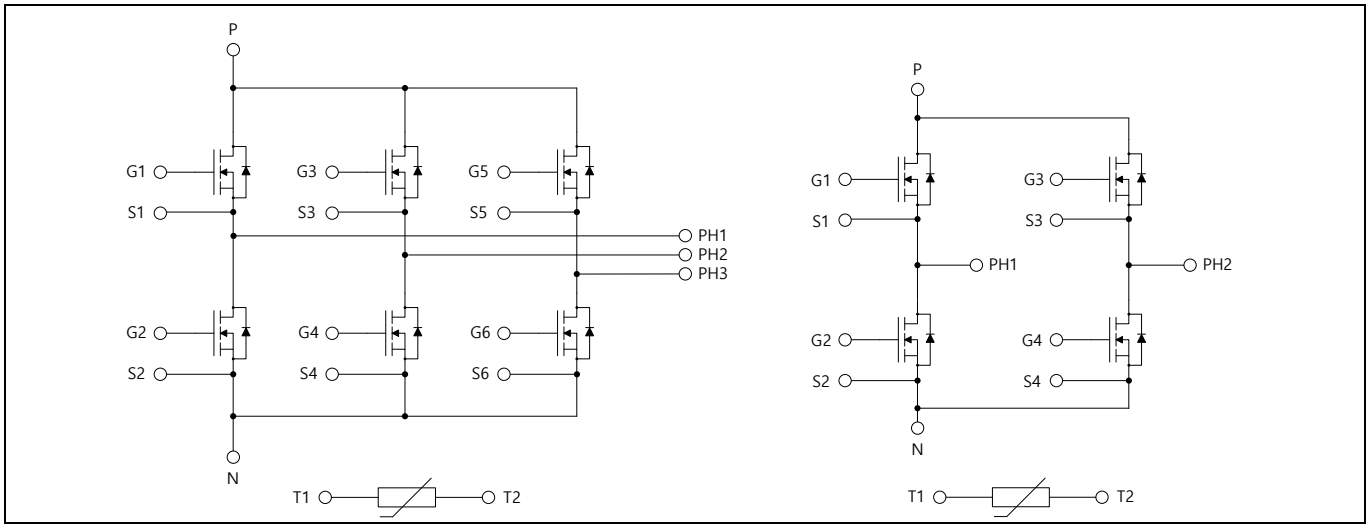


Figure 3 Internal block diagram, 6-pack (left) and 4-pack (right)

3.2 Pin description

3.2.1 6-pack type 1

Figure 4 shows the pin map of the 6-pack type 1 products listed in Table 1.

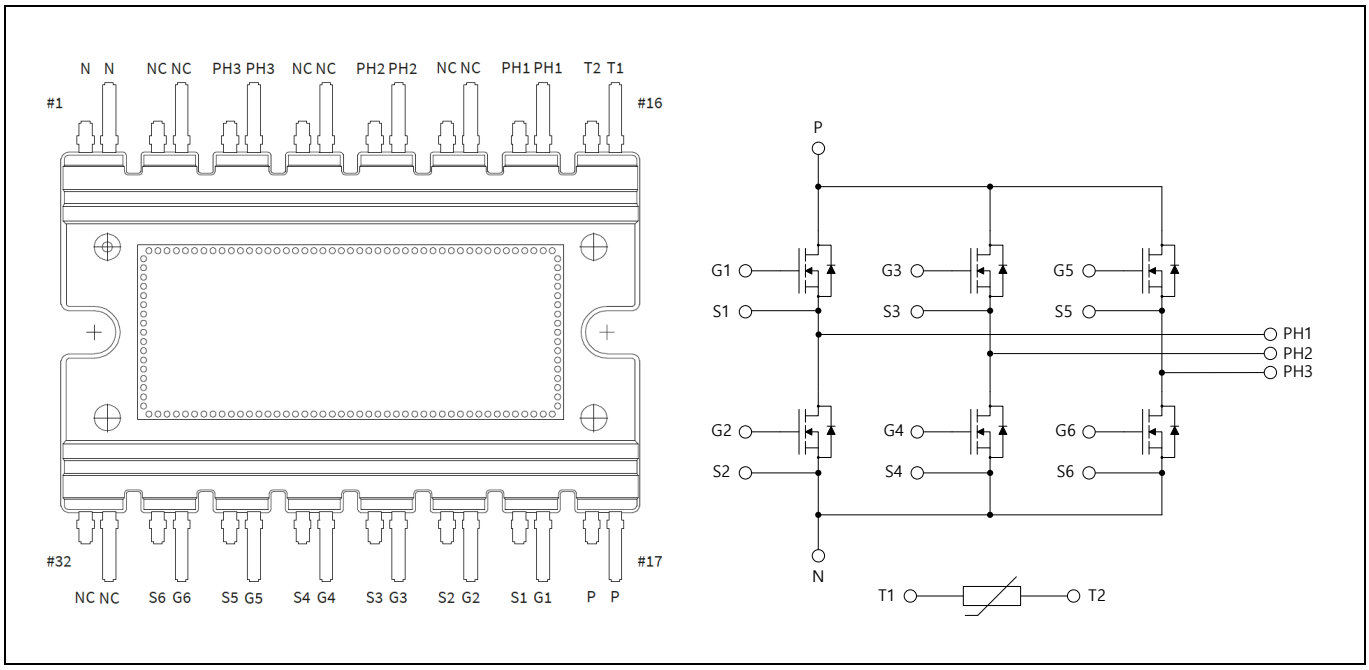


Figure 4 6-pack type 1

3 Product overview

3.2.2 6-pack type 2

Figure 5 shows the pin map of the 6-pack type 2 products listed in Table 1.

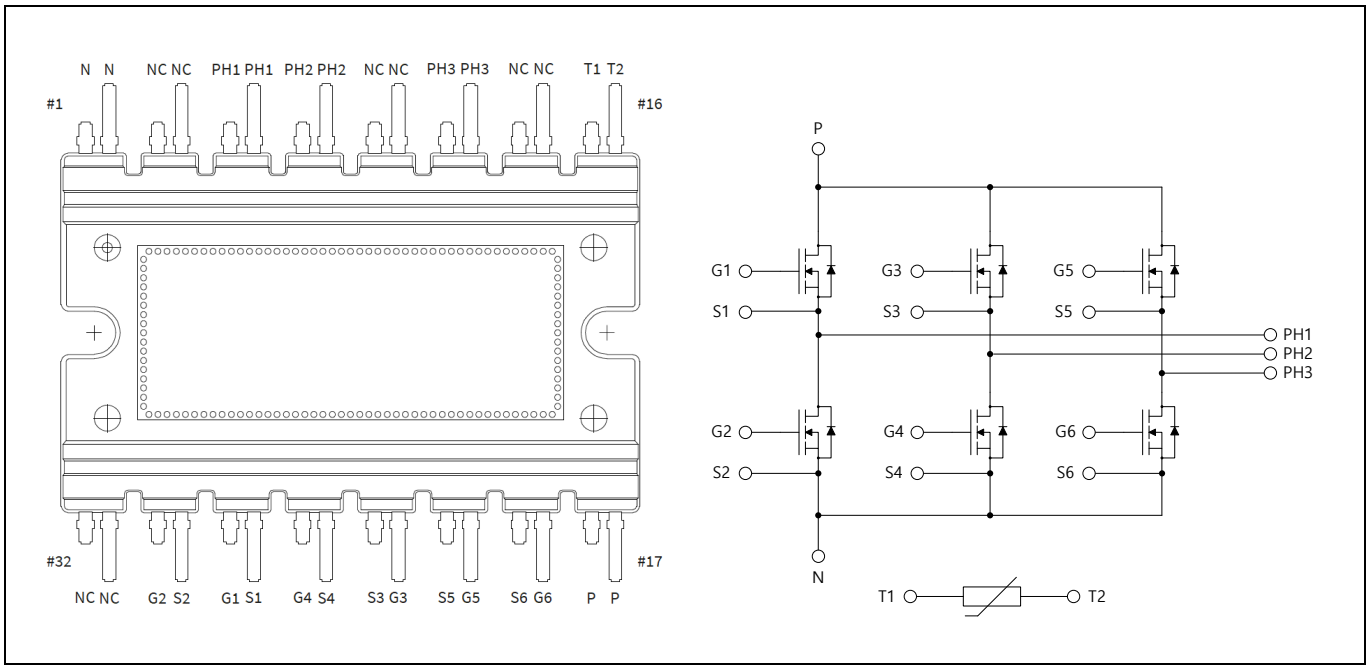


Figure 5 6-pack type 2

3.2.3 4-pack type 2

Figure 6 shows the pin map of the 4-pack type 2 products listed in Table 1.

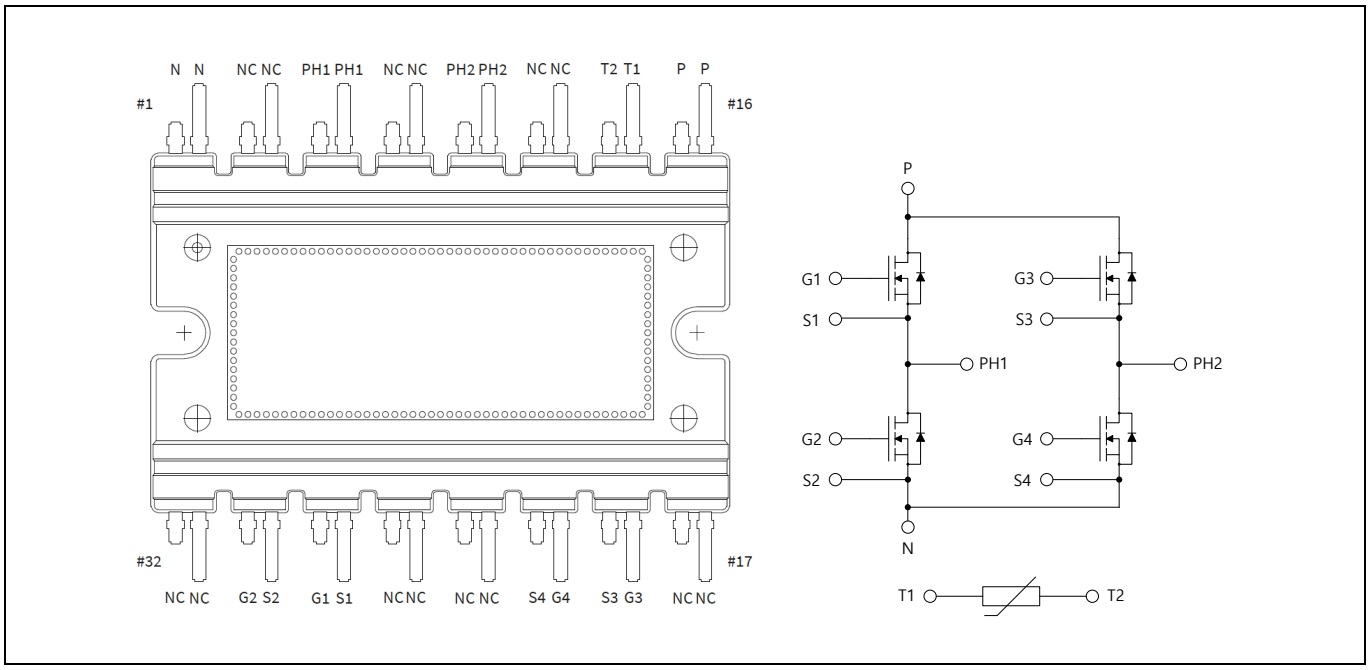


Figure 6 4-pack type 2

3.3 Chip coordiantes

Table 3 shows the center position of the chips inside the module. They are referenced to the bottom right corner of the package body when viewed from top, as shown in Figure 7 and Figure 8. Chip 1 is the rightmost chip.

Table 3 The center of each SiC MOSFET (unit: [mm])

Topology	Product	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6	Thermistor
6-pack	AMM12S18LB1Z	9.63, 13.22	14.58, 13.22	19.53, 13.22	24.48, 13.22	29.43, 13.22	34.38, 13.22	6.54, 19.03
	AMM12S25LB1Z	9.63, 12.75	14.58, 12.75	19.53, 12.75	24.48, 12.75	29.43, 12.75	34.38, 12.75	
	AMM12S36LB1Z	9.63, 12.51	14.58, 12.51	19.53, 12.51	24.48, 12.51	29.43, 12.51	34.38, 12.51	
	AMM12S36LB1Z2	9.63, 12.51	14.58, 12.51	19.53, 12.51	24.48, 12.51	29.43, 13.22	34.38, 13.22	
	AMM12S54LB1Z	9.63, 12.33	14.58, 12.33	19.53, 12.33	24.48, 12.33	29.43, 12.33	34.38, 12.33	
	AMM12S62LB1Z	9.63, 12.33	14.58, 12.33	19.53, 12.33	24.48, 12.33	29.43, 12.33	34.38, 12.33	
	AMM12S54LB2Z	9.63, 13.13	14.58, 13.13	19.53, 13.13	24.48, 13.13	29.43, 13.13	34.38, 13.13	
	AMM12S62LB2Z	9.63, 12.92	14.58, 12.92	19.53, 12.92	24.48, 13.03	29.43, 13.03	34.38, 13.03	
4-pack	AMF12S18LB2Z	10.28, 9.9	15.63, 9.9	26.95, 9.42	33.25, 9.42			10.69, 19.02
	AMF12S25LB2Z	10.28, 9.43	15.63, 9.43	27.43, 9.43	33.73, 9.43			
	AMF12S36LB2Z	10.04, 9.19	15.39, 9.19	27.66, 9.19	33.96, 9.19			
	AMF12S54LB2Z	9.86, 9.01	15.21, 9.01	27.84, 9.01	34.14, 9.01			
	AMF12S62LB2Z	9.76, 9.01	15.11, 9.01	27.84, 8.91	34.14, 8.91			

3 Product overview

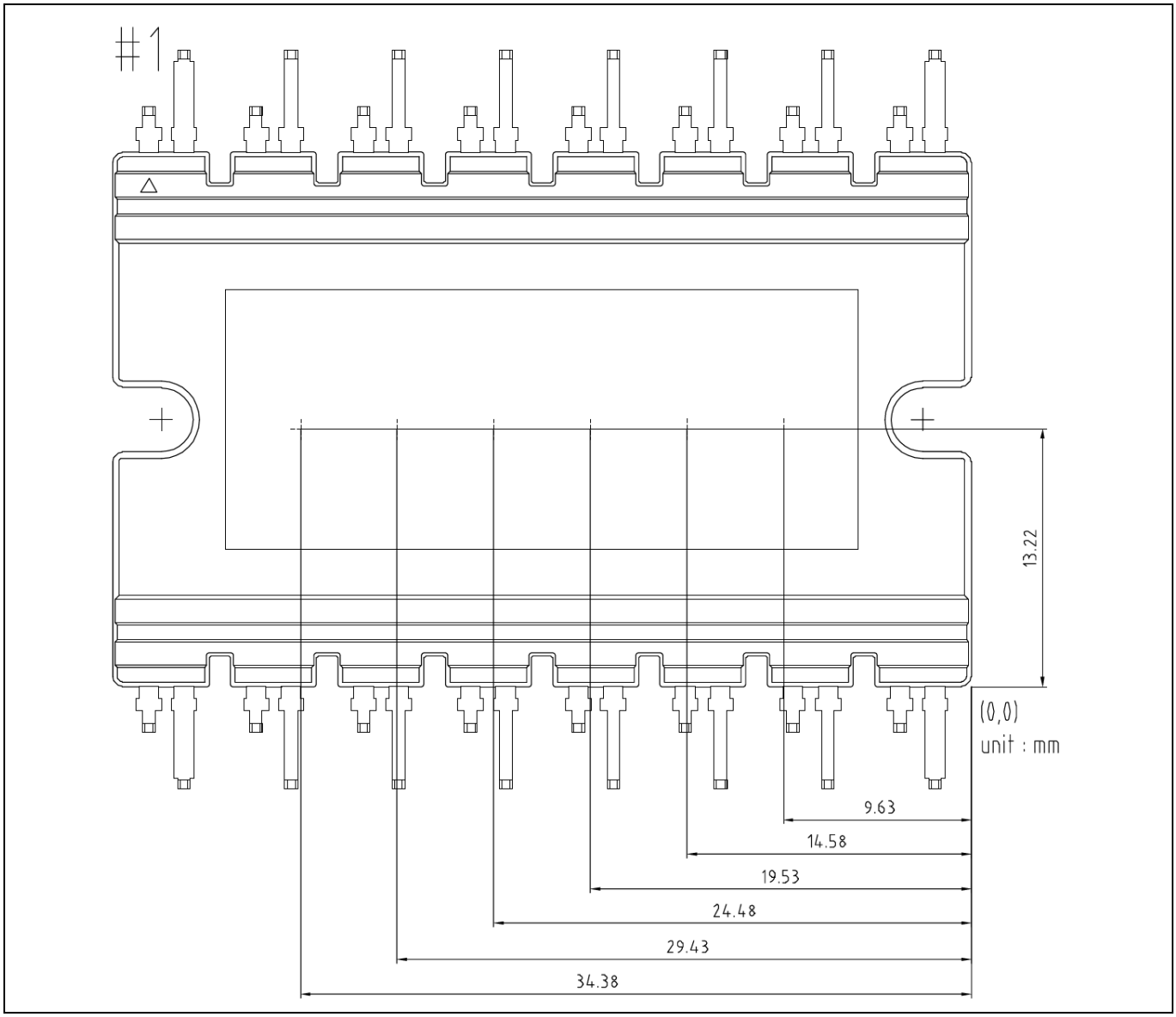


Figure 7 Chip coordinates of AMM12S18LB1Z

3 Product overview

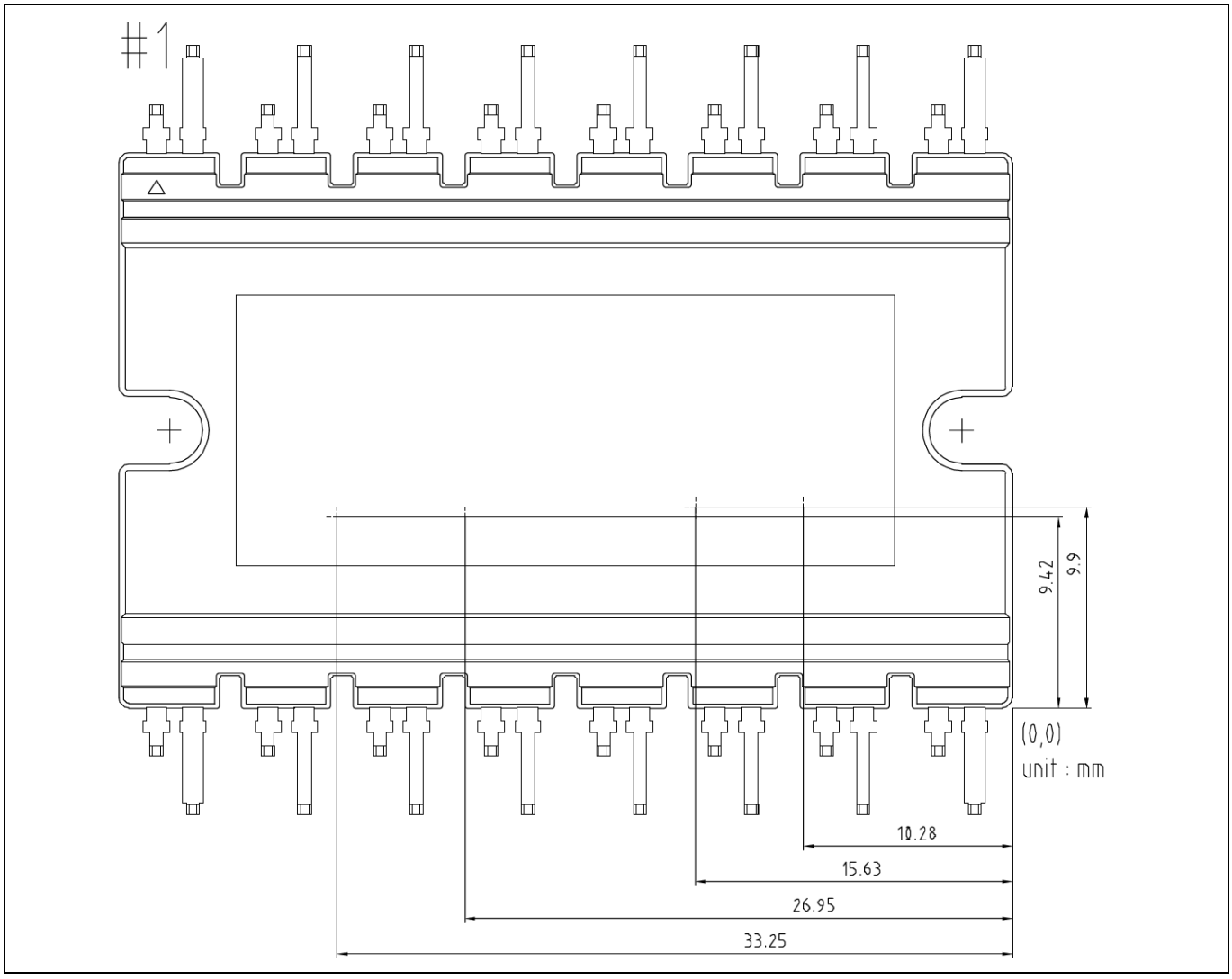


Figure 8 Chip coordinates of AMF12S18LB1Z

3.4 Parasitic inductance of package

Wires and copper patterns within the package create parasitic inductance. This parasitic inductance affects the switching behavior and therefore the allowable voltage across the switches, and the power loss. Figure 9 shows the equivalent circuitry of the CIPOS™ Prime modules including parasitic inductance in each current path. For 4-pack products, the components in the third leg can be disregarded.

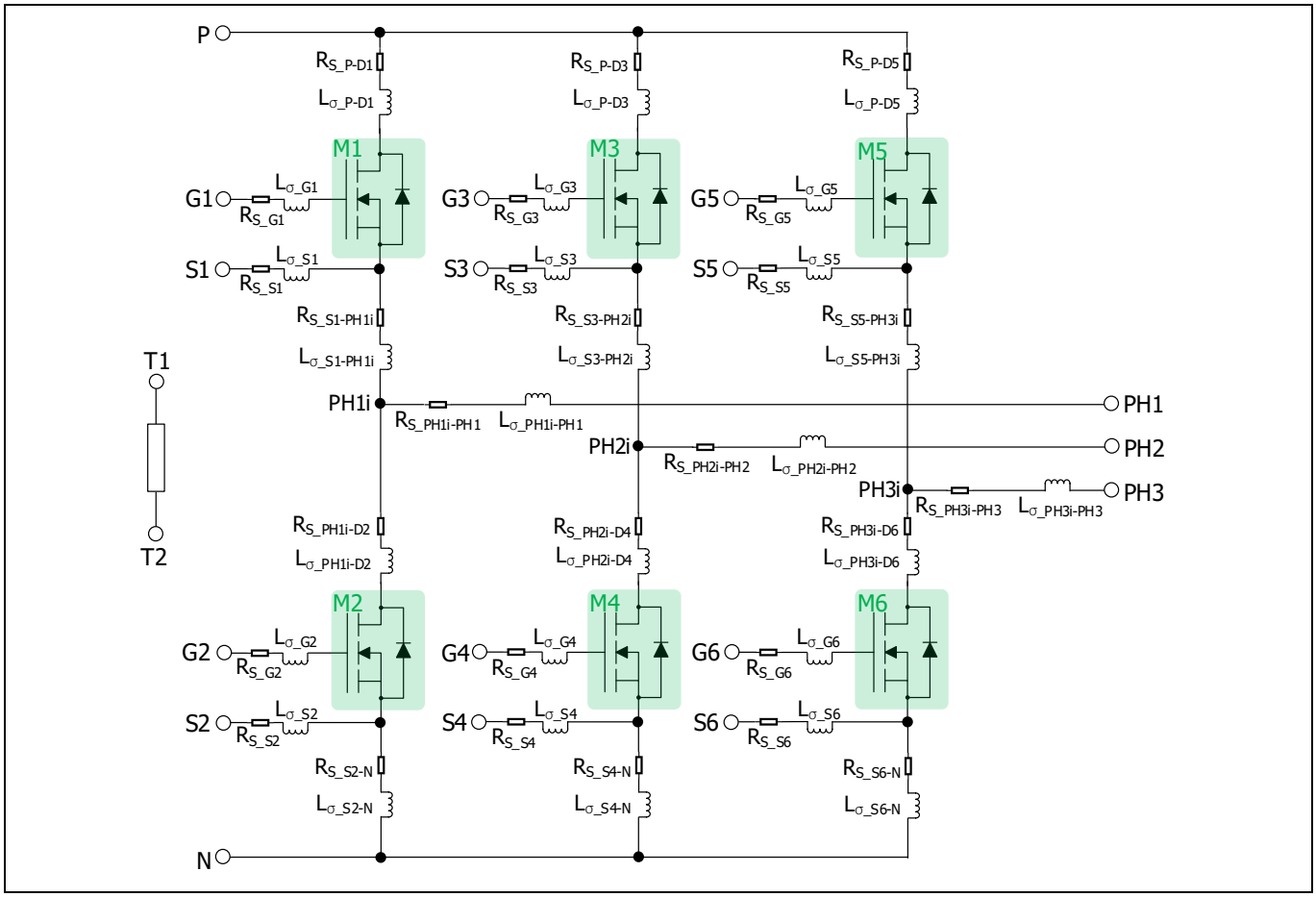


Figure 9 Equivalent circuitry of the 6-pack

3 Product overview

Table 4 Parasitic inductance value (unit: [nH])

	6-pack type 1	6-pack type 2	4-pack type 2
Ls_G1	17.4	15.6	11.6
Ls_S1	14.9	15.6	11.8
Ls_P-D1	10.5	22.6	21.9
Ls_S1-PH1i	2.2	2.4	3.5
Ls_G2	17.1	15.9	11.2
Ls_S2	14.6	15.9	11.7
Ls_PH1i-D2	2.0	2.3	3.7
Ls_S2-N	24.5	13.2	16.8
Ls_PH1i-PH1	7.9	8.4	10.3
Ls_G3	17.0	18.0	12.8
Ls_S3	14.5	13.2	9.0
Ls_P-D3	16.3	15.7	14.3
Ls_S3-PH2i	2.2	2.5	3.0
Ls_G4	17.0	15.6	12.7
Ls_S4	14.5	15.5	9.0
Ls_PH2i-D4	2.1	2.3	1.8
Ls_S4-N	18.0	18.6	25.4
Ls_PH2i-PH2	7.8	9.2	12.6
Ls_G5	17.1	18.3	
Ls_S5	14.6	13.6	
Ls_P-D5	23.3	13.3	
Ls_S5-PH3i	2.2	2.6	
Ls_G6	17.3	18.8	
Ls_S6	14.9	13.8	
Ls_PH3i-D6	2.1	2.7	
Ls_S6-N	12.8	29.1	
Ls_PH3i-PH3	7.9	8.4	

3.4.1 Allowable P-N voltage and parasitic inductance

When designing the gate driving circuitry, the parasitic inductance and the switching di/dt should be considered together. During switching, the voltage is induced across the parasitic inductance (V_{ind} = L*di/dt). This induced voltage is added to the voltage between the P and N terminals, V_{PN}. As the V_{DSS} rating is 1200 V, V_{PN} + V_{ind} should be maintained below 1200 V.

While V_{PN} can be measured at the P and N terminals, V_{ind} should be evaluated based on the inductance value given in Table 4, and the measured value of the switching di/dt of the application. Figure 10 shows an example of the turn-off di/dt by R_G. When the allowable V_{PN} is assumed to be 1100 V, the allowable turn-off di/dt becomes 100 V/40.4 nH = 2475 A/µs. To keep V_{DSS} within 1200 V, the external R_G should be 5 Ω or more. As the switching di/dt varies by gate driving circuitry, the drain-current level, and the PCB layout, users should evaluate it in

3 Product overview

their own applications. The allowable V_{PN} is determined by the PCB layout, the snubber circuitry, and the DC-link voltage. An optimized layout enables lower V_{PN} at a given DC-link voltage and therefore provides more room for V_{ind}. This eventually leads to faster switching speed or lower switching losses.

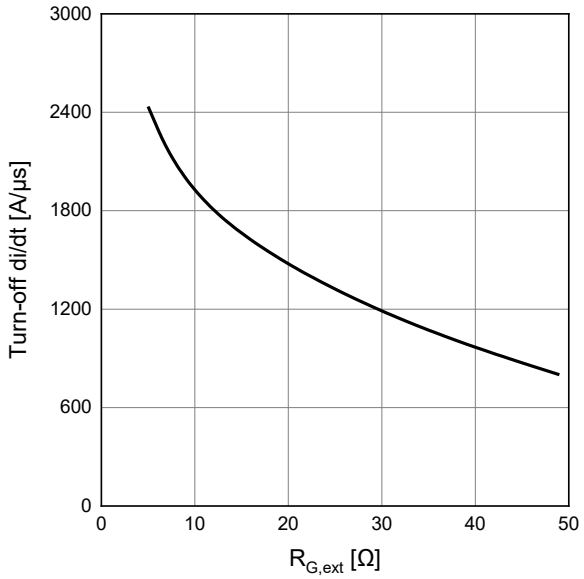


Figure 10 Turn-off di/dt by R_G at 74.8 A and 25°C in AMM12S18LB1Z

4 Interface circuit and layout

4.1 Layout guidelines

In the PCB layout, it is most important to minimize the parasitic inductance in the commutation loop (blue part in Figure 11) as the di/dt is high there.

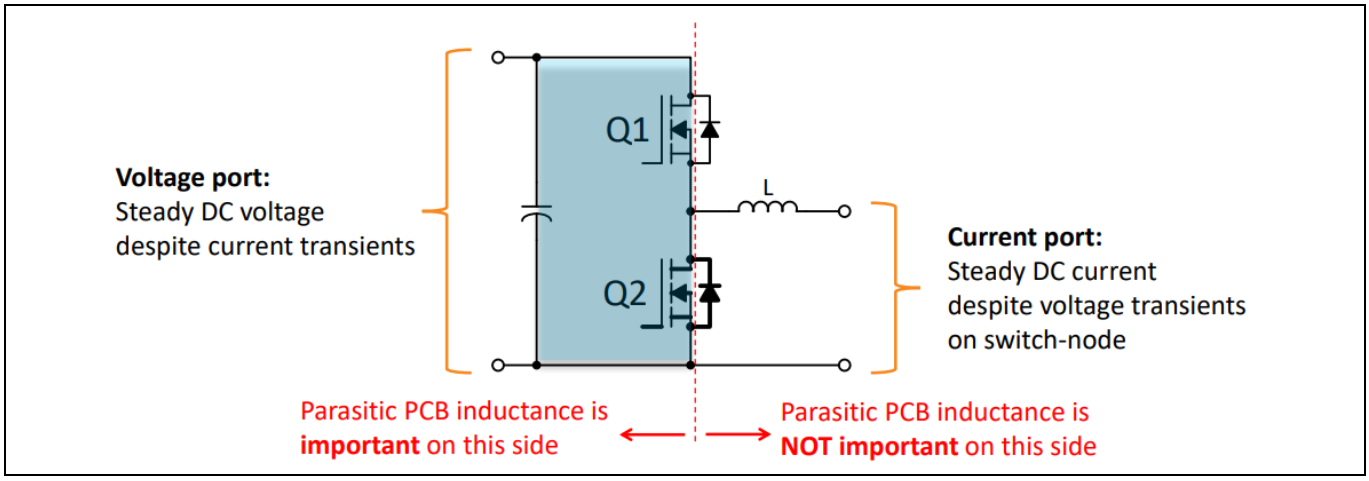


Figure 11 Commutation loop [2]

One of the critical factors for achieving low inductance is utilizing the mutual inductance. Figure 12 shows theory of mutual inductance. To increase mutual inductance, paths with opposite current flow should be routed in parallel and as close to each other as possible.

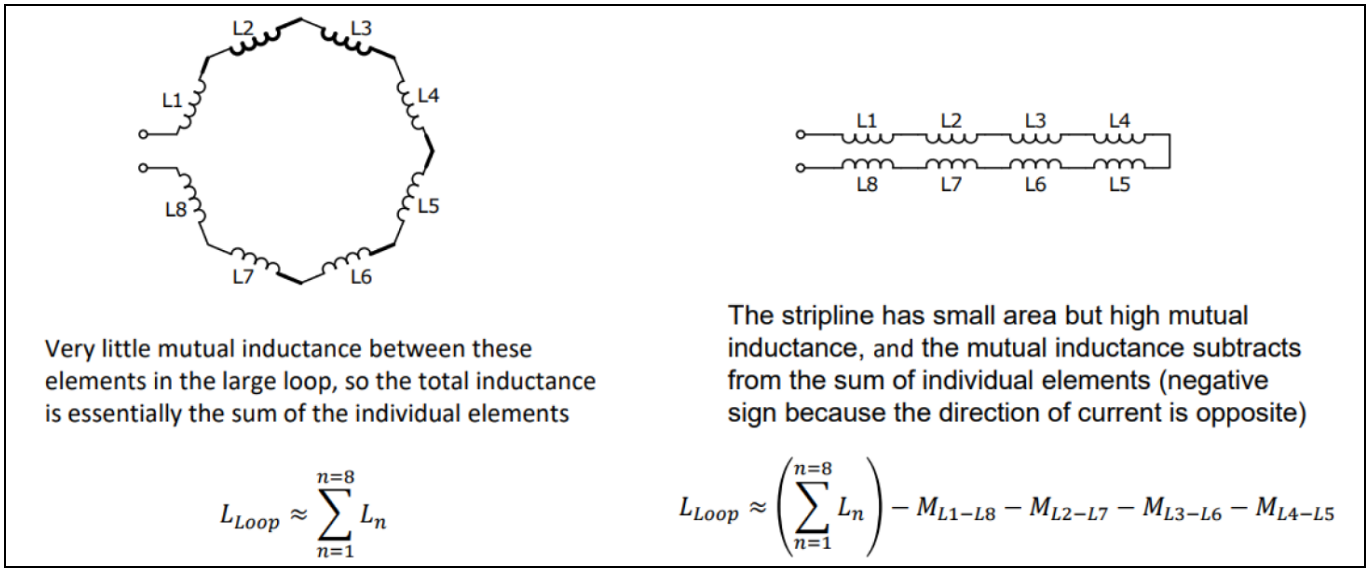


Figure 12 Theory: partial and mutual inductance [2]

4 Interface circuit and layout

Layout recommendation for CIPOS™ Prime are shown in Figure 13 and Figure 14.

- DC-link capacitors are placed on the short side of the module to minimize the lateral loop
- High mutual inductance due to anti-parallel routing of the return current on the closest PCB layers possible
- The top layer and the first inner layer under the module are used to route the return current
- Total inductance of this set-up is around 30 nH as measured in a double-pulse test

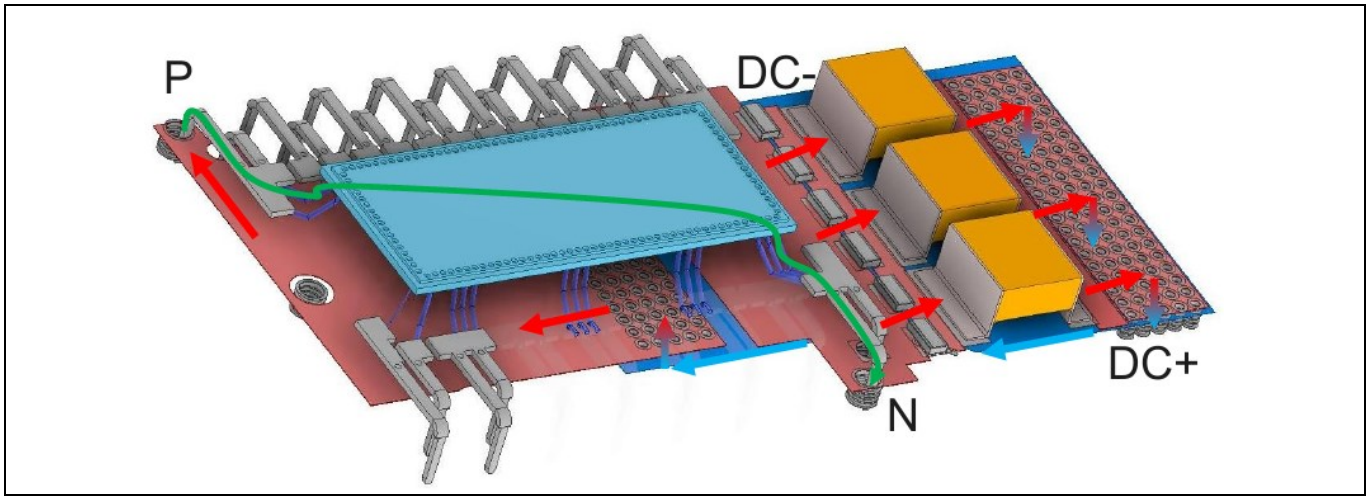


Figure 13 Isometric view of CIPOS™ Prime's commutation loop layout

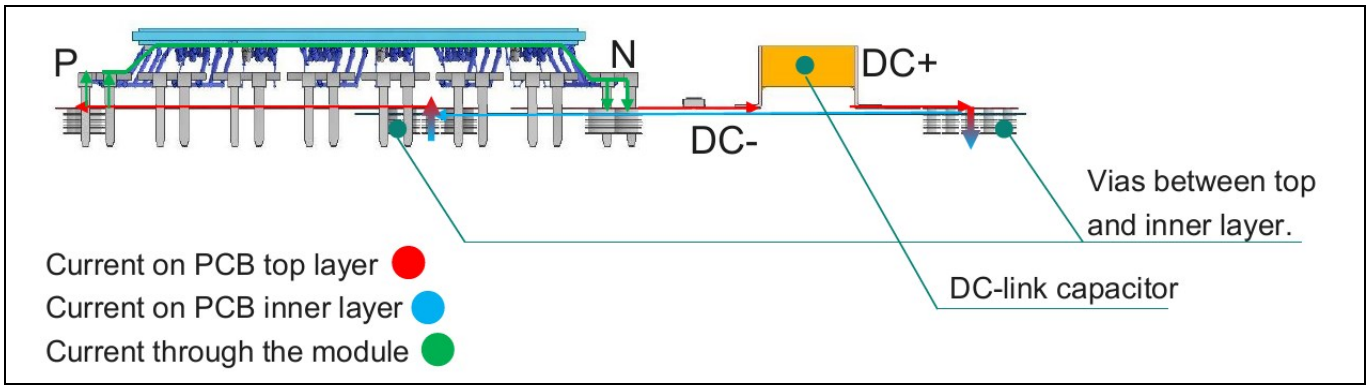


Figure 14 Cross-section view of CIPOS™ Prime's commutation loop layout

4.2 Temperature monitoring

The CIPOS™ Prime products have a thermistor on the DCB to monitor the operating temperature. A typical interface circuitry comprises a voltage divider consisting of the thermistor and a fixed resistor, as shown in Figure 15. A small bypass capacitor can be added parallel to the thermistor to filter out noises and stabilize the voltage reading at the microcontroller's analog-to-digital converter (ADC). The thermistor is insulated from the other components inside the CIPOS™ Prime package. Therefore, isolation between the thermistor and the ADC is not a must-have. Users can consider including additional isolation based on their requirements.

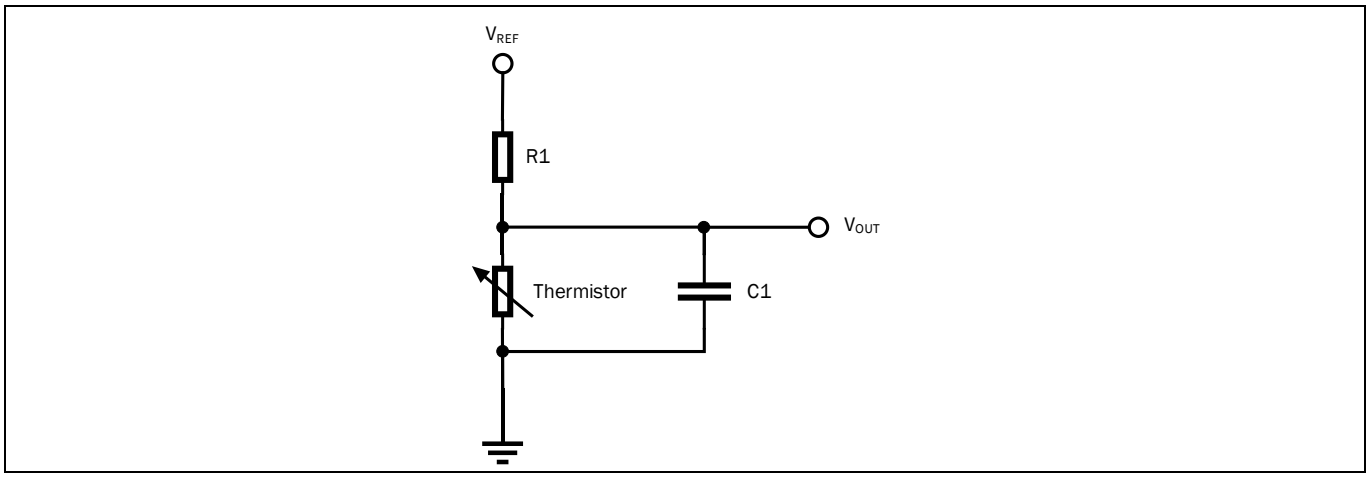


Figure 15 Application circuitry of the thermistor

Figure 16 show an example of the thermistor voltage based on temperature with a 4.7 kΩ pull-up resistor and V_{REF} of 3.3 V and 5 V. Users can define the temperature that is of interest to them, such as the temperature for activating overtemperature protection (OTP), or the appropriate ADC voltage at OTP, and then set the pull-up resistor value for it.

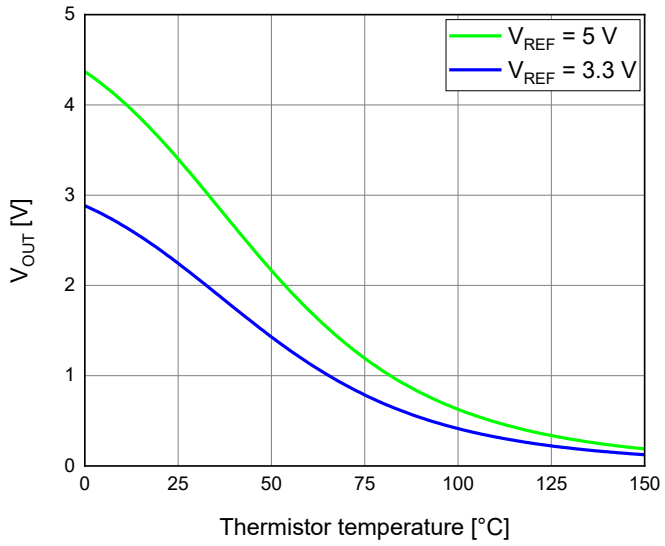


Figure 16 Voltage reading according to the thermistor temperature

4 Interface circuit and layout

Although the thermistor is located on the DCB along with SiC MOSFET chips, there is a certain distance between them. Figure 17 shows the location of the thermistor inside the module with red squares. Heat from the power devices is transferred to the thermistor through the package and the heat sink. This creates a gap between the temperatures of the thermistor and the power devices. Figure 18 shows an example from the thermal simulation. Boundary conditions for the simulation were as follows:

- Thermal interface material (TIM): Thickness = 50 µm and thermal conductivity = 0.9 W/mK
- Cooling block: Fixed temperature = 65°C, thermal conductivity = 96 W/mK, heat transfer coefficient = 3000 W/m^{2}K, heat sink size = 63.3 x 36.5 x 5 mm

This gap or connection between the junction temperature of the power devices (T_J) and the thermistor's output (T_{NTC}) is highly dependent on the environment, e.g., cooling conditions, power dissipation, and so on. Users should define this association for their applications.

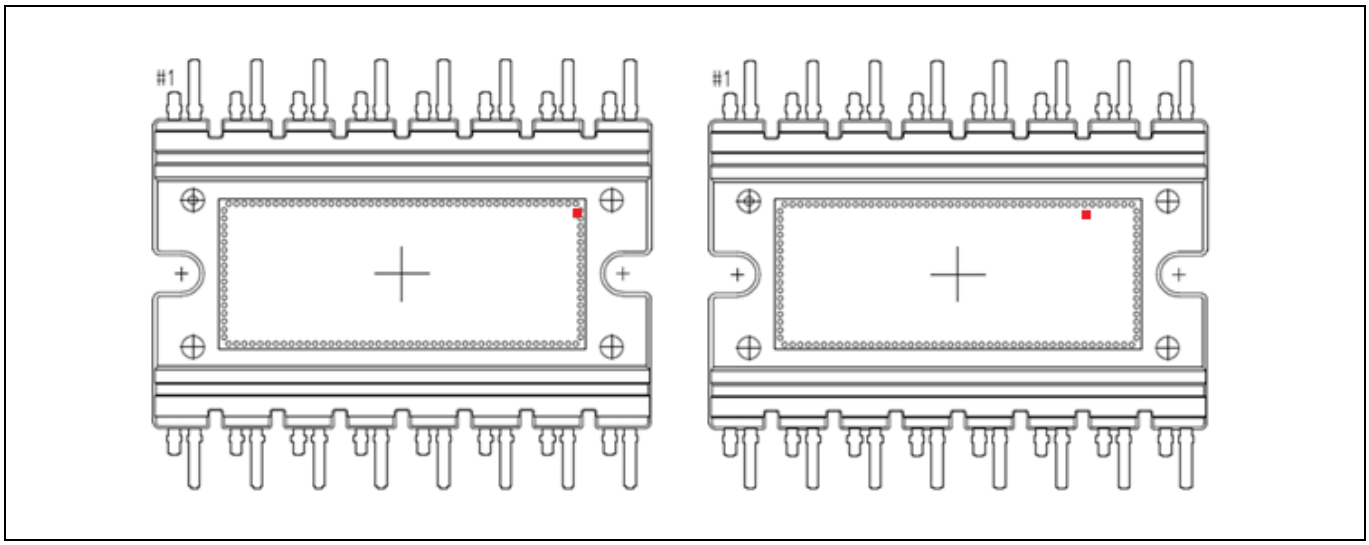
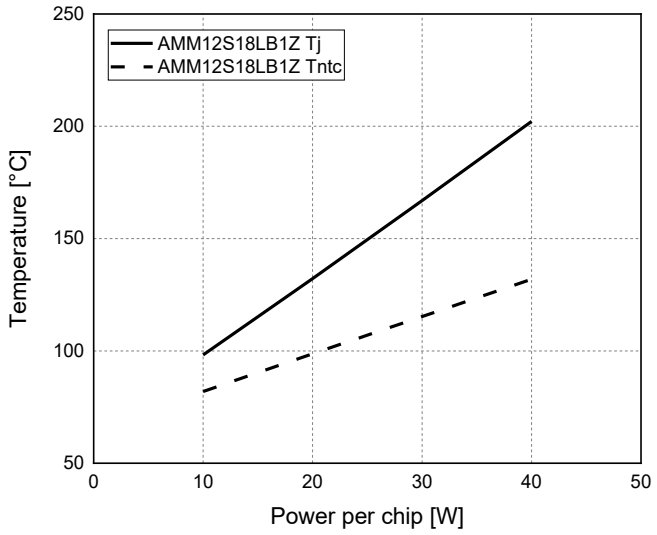


Figure 17 Location of the thermistor. On the 6-pack (left), and on the 4-pack (right)

4 Interface circuit and layout



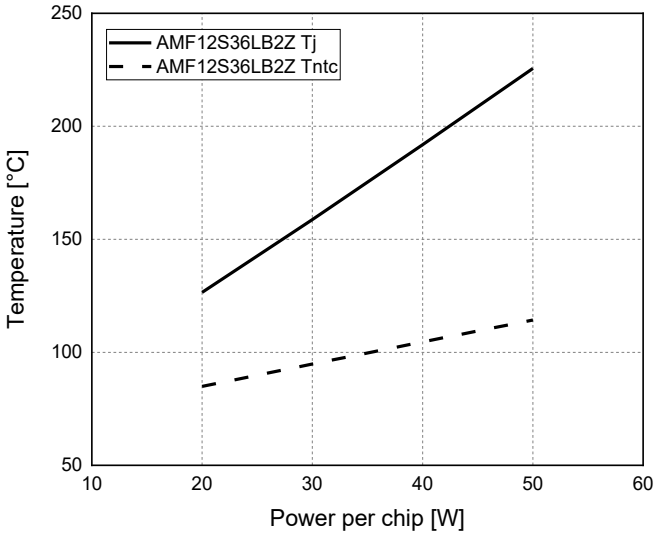


Figure 18 Example of the interconnection between T_J and T_{NTC}

4.3 Pin and screw hole coordinates

Please refer to AN-2026-01 [1] for details.

5 Heat sink assembly

Please refer to AN-2026-01 [1] for details.

6 Related resources

- CIPOS™ Prime product family: Link to web page
- Infineon developer community

References

[1] Infineon Technologies application note AN-2026-01

[2] Eric Persson, “Optimizing PCB Layout for HV GaN Power Transistors”, IEEE Power Electronics Magazine, Volume 10, Issue 2, 2023

Revision history

Document revision	Date	Description of changes
1.0	2026-05-15	Initial release

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