The CIPOS™ Mini IPM

IM06BxxxC1 series application note

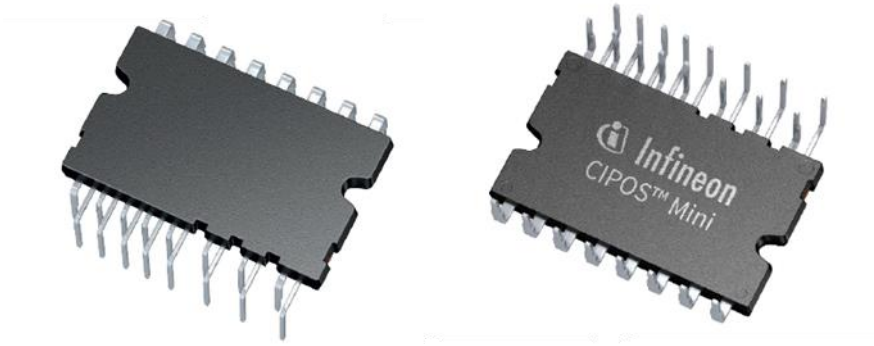
About this document

Scope and purpose

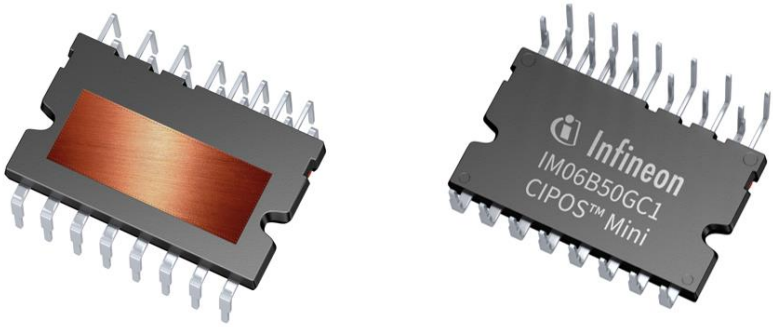
The application note describes the IM06BxxxC1 product group of the CIPOS™ Mini family and provides the basic requirements for operating the products in the recommended mode. This document also provides information about the integrated components such as the IGBTs, the diodes, and the gate driver IC, as well as on the design of the necessary external circuitry, such as bootstrap and interfacing.

Intended audience

The intended audiences for this document are design engineers, technicians, and developers of electronic systems.



[CIPOS™ Mini full package]



[CIPOS™ Mini DCB package]

Table of contents

About this document **1**
Table of contents **2**
1 Scope **4**
1.1 Product lineup 5
1.2 Nomenclature 5
2 Internal components and package technology **6**
2.1 Power transistor technology 6
2.1.1 650 V TRENCHSTOP™ IGBT7 6
2.1.2 600 V emitter-controlled diode 6
2.2 Single-control 600 V 6-channel gate driver IC 6
2.3 Thermistor 7
2.4 Package technology 8
3 Product overview **9**
3.1 Internal circuit and features 9
3.2 Maximum electrical ratings 10
3.3 Electrical characteristics 11
3.4 Characteristics of the short-circuit safety operation area (SCSOA) 12
3.5 Description of the input and output pins 13
3.6 Pin assignment 13
3.7 Outline drawing 17
3.8 Marking 19
3.9 Chip position 20
4 Interface circuit and layout guide **22**
4.1 Input and output signal connection 22
4.2 Internal dead time 23
4.3 Cross-conduction prevention circuitry 24
4.4 Advanced input filter 24
4.5 Matching propagation-delay time 25
4.6 Example of a general interface circuit 26
4.7 Recommended rated output current of power supply 27
4.8 Recommended layout pattern for overcurrent protection and short-circuit protection 27
4.9 Recommended wiring of the shunt resistor and snubber capacitor 28
4.10 Pin and screw-hole coordinates for IM06BxxxC1 29
5 Protection features **30**
5.1 Undervoltage protection 30
5.2 Overcurrent protection 31
5.2.1 Timing chart of the overcurrent protection 31
5.2.2 Selecting a current-sensing shunt resistor 32
5.2.3 Delay time 33
5.3 Fault-output circuit 34
5.4 Sleep function 34
5.5 Temperature monitoring and thermal protection 35
6 Bootstrap circuit **37**
6.1 Bootstrap circuit operation 37
6.2 Internal bootstrap functionality characteristics 37
6.3 Initial charging of a bootstrap capacitor 38

6.4 Bootstrap circuit design 38
6.4.1 Bootstrap capacitor 38
6.4.2 Bootstrap voltage variance under inverter operating conditions 39
7 Thermal system design 41
7.1 Introduction 41
7.2 Power loss 42
7.2.1 Conduction losses 42
7.2.2 Switching losses 43
7.3 Thermal impedance 43
7.4 Factors for the temperature rise and sample calculations 45
7.5 Heatsink selection guide 46
7.5.1 Required heatsink performance 46
7.5.2 Heatsink characteristics 46
7.5.2.1 Heat transfer from the heat source to the heatsink 47
7.5.2.2 Heat transfer within the heatsink 47
7.5.2.3 Heat transfer from the heatsink surface to the ambient 47
7.5.3 Selecting a heatsink 49
8 Heatsink mounting and soldering method 50
8.1 Electrical spacing 50
8.2 Mounting the heatsink 52
8.2.1 General guidelines 52
8.2.1.1 Recommended tightening torque 52
8.2.1.2 Tightening the screws to the heatsink 54
8.2.1.3 Mounting screw 55
8.3 Soldering conditions 56
8.3.1 Wave soldering 56
8.3.2 Manual soldering 57
9 Package handling guidelines 58
9.1 Recommended storage conditions 58
9.2 Packing specification 59
References 60
Revision history 61

1 Scope

To meet the strong demand for smaller size and higher power density, Infineon Technologies has developed a new family of highly integrated intelligent power modules (IPMs) that contain nearly all the semiconductor components required to drive electronically controlled variable-speed electric motors. These IPMs incorporate a 3-phase inverter power stage with a silicon-on-insulator (SOI) gate driver and Infineon's leading-edge 650 V TRENCHSTOP™ IGBTs and the 600 V emitter-controlled diode. Integrating discrete power semiconductors and gate driver ICs into one package allows design engineers to reduce the time and effort spent on design.

The application note covers the following products:

- IM06B15AC1
- IM06B20AC1
- IM06B30AC1
- IM06B50GC1

IM06BxxxC1 is a product group in the CIPOS™ Mini IPM family that is designed for motor drives in home appliances, such as air conditioners, washing machines, low-power general-purpose inverters (GPI), and pump applications.

1.1 Product lineup

Table 1 Lineup of the IM06BxxxC1 products

Part number	rating		inverter circuit	package	isolation voltage [V_{rms}]	main applications
	current [A]	voltage [V]				
IM06B15AC1	15	600	open emitter	fully molded, dual in-line (DIL) module	2000 V_{rms}/60 Hz (sinusoidal, 1 min. All pins shorted – heatsink)	Air conditioners, general-purpose inverter
IM06B20AC1	20					
IM06B30AC1	30					
IM60B50GC1	50			Direct copper bonding (DCB) DIL module		

1.2 Nomenclature

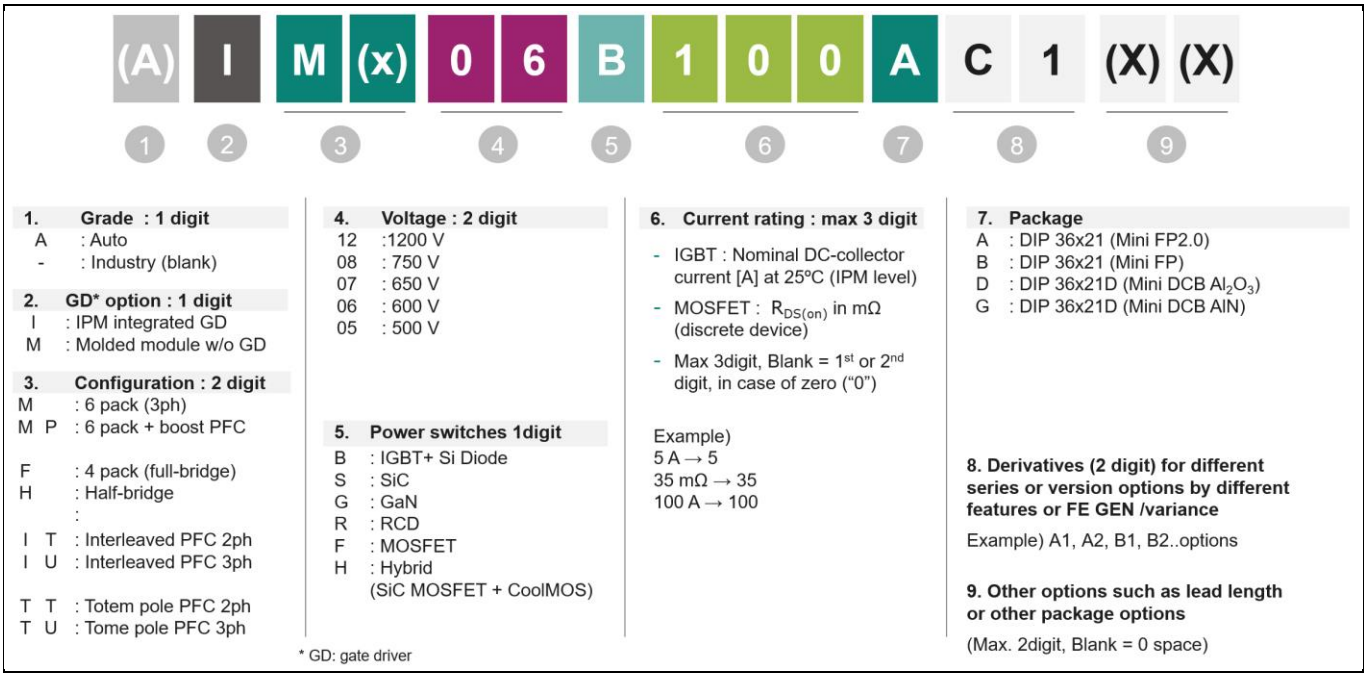


Figure 1 The IM06BxxxC1 product group nomenclature

2 Internal components and package technology

2.1 Power transistor technology

2.1.1 650 V TRENCHSTOP™ IGBT7

Infineon Technologies introduced the TRENCHSTOP™ IGBT7 technology in 2018 [1]. This technology has led to significant improvements in the static and dynamic performance, due to the combination of the trench-stop cell and field-stop concepts. The combination of IGBTs and soft-recovery emitter-controlled diodes further minimizes the turn-on losses. The highest efficiency is achieved due to the optimum trade-off between the switching and conduction losses. This technology continues to possess the well-known robust characteristics of Infineon IGBTs, such as short-circuit withstand capability and maximum junction temperature.

2.1.2 600 V emitter-controlled diode

The emitter-controlled diode uses the unique fast-recovery diode technology from Infineon. The ultrathin wafer and field-stop technology lowers the turn-on losses of the IGBT with soft recovery, making these emitter-controlled diodes ideal for consumer applications.

2.2 Single-control 600 V 6-channel gate driver IC

The thin-film silicon-on-insulator (SOI) technology in gate driver ICs provides additional benefits such as lower power consumption and higher immunity to radioactive radiation or cosmic rays [2]. The basic feature of the SOI technology is the separation of the active silicon from the base material by a buried silicon oxide layer. The buried silicon oxide provides an insulation barrier between the active layer and the silicon substrate, reducing the parasitic capacitance tremendously. This insulation barrier also disables leakage or latch-up currents between adjacent devices. It prevents the latch-up effect even in the case of high dv/dt switching under elevated temperature, making it more robust. One monolithic single-control IC for all six IGBTs offers extra advantages such as bootstrap circuitry, matched propagation delay times, built-in dead time, and cross-conduction prevention. All the six IGBTs turn off under fault situations, such as undervoltage lockout and overcurrent.

2.3 Thermistor

In IM06BxxxC1, the thermistor is integrated into the internal PCB. It is connected between the V_{FO} and V_{SS} pins. A circuit proposal using a thermistor for overtemperature protection is discussed in Section 5.5.

Table 2 Raw data of the thermistor used in IM06BxxxC1

T [°C]	R_{min} [kΩ]	R_{typ} [kΩ]	R_{max} [kΩ]	Tol. [%]	T [°C]	R_{min} [kΩ]	R_{typ} [kΩ]	R_{max} [kΩ]	Tol [%]
-40	2809.57	2974.023	3146.12	5.7	45	35.432	36.690	37.970	3.5
-35	2011.21	2125.363	2244.59	5.5	50	29.151	30.157	31.178	3.4
-30	1458.73	1539.042	1622.76	5.3	55	24.100	24.908	25.727	3.3
-25	1070.96	1128.164	1187.68	5.2	60	20.018	20.669	21.329	3.2
-20	795.189	836.413	879.24	5.0	65	16.701	17.229	17.763	3.1
-15	596.671	626.698	657.83	4.9	70	13.994	14.424	14.858	3.0
-10	452.131	474.223	497.084	4.7	75	11.774	12.125	12.479	2.9
-5	345.771	362.178	379.125	4.6	80	9.946	10.234	10.523	2.8
0	266.724	279.016	291.692	4.5	85	8.434	8.670	8.908	2.7
5	207.427	216.712	226.271	4.3	90	7.177	7.373	7.569	2.7
10	162.553	169.621	176.886	4.2	95	6.130	6.292	6.454	2.6
15	128.312	133.732	139.294	4.1	100	5.253	5.388	5.523	2.5
20	101.980	106.165	110.453	4.0	105	4.510	4.629	4.748	2.6
25	81.580	84.833	88.160	3.9	110	3.884	3.990	4.096	2.7
30	65.664	68.208	70.806	3.8	115	3.356	3.449	3.544	2.7
35	53.165	55.166	57.207	3.7	120	2.908	2.991	3.075	2.8
40	43.286	44.869	46.481	3.6	125	2.527	2.601	2.676	2.9

2.4 Package technology

IM06BxxxC1 offers the smallest size with a high-power density of up to 600 V, 50 A by employing IGBTs and diodes with 6-channel gate driver ICs. It contains all the power components such as IGBTs and diodes and isolates them from each other and from the heatsink. All low-power components such as the gate driver IC and thermistor are assembled on a PCB.

The electric insulation is provided by the mold compound. To decrease the thermal impedance further, the internal lead frame design has been optimized [3]. Figure 2 shows the external view and internal structure of the IM06BxxxC1 package.

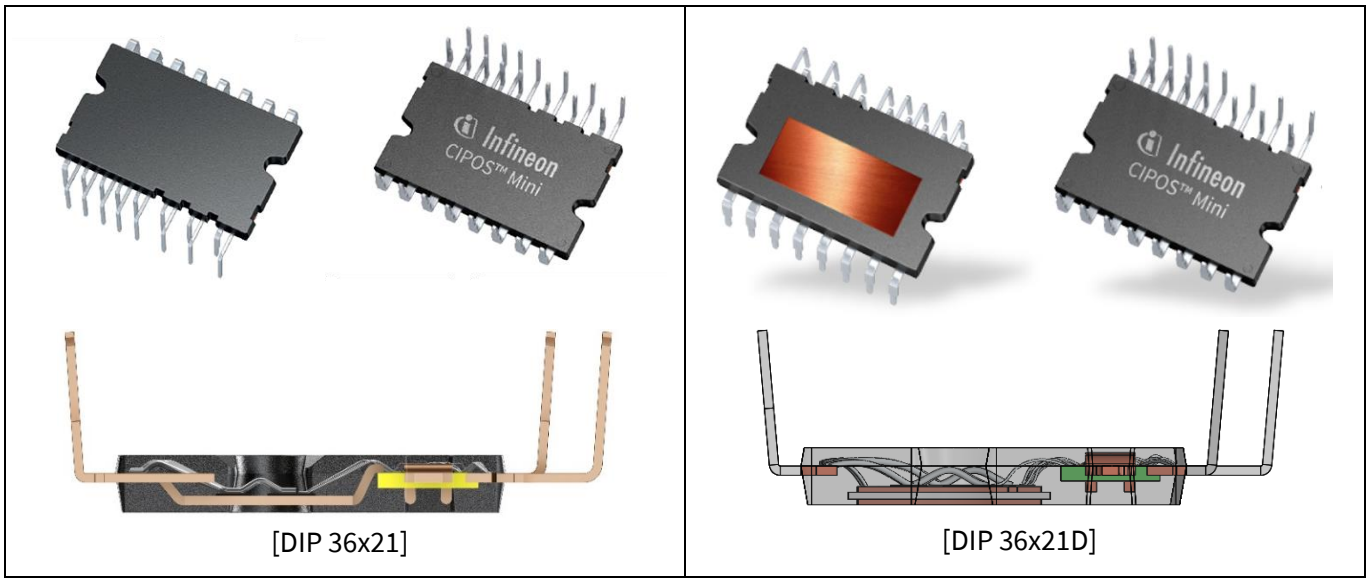


Figure 2 External view and internal structure of the IM06BxxxC1 packages (DIP 36x21 and 36x21D)

Figure 3 shows the internal view of the dummy pins. The pins are on the side of the package and are used to fix the inner PCB. They have no connection with the internal circuit. This means that the dummy pins have no electrical function and are isolated in the package.

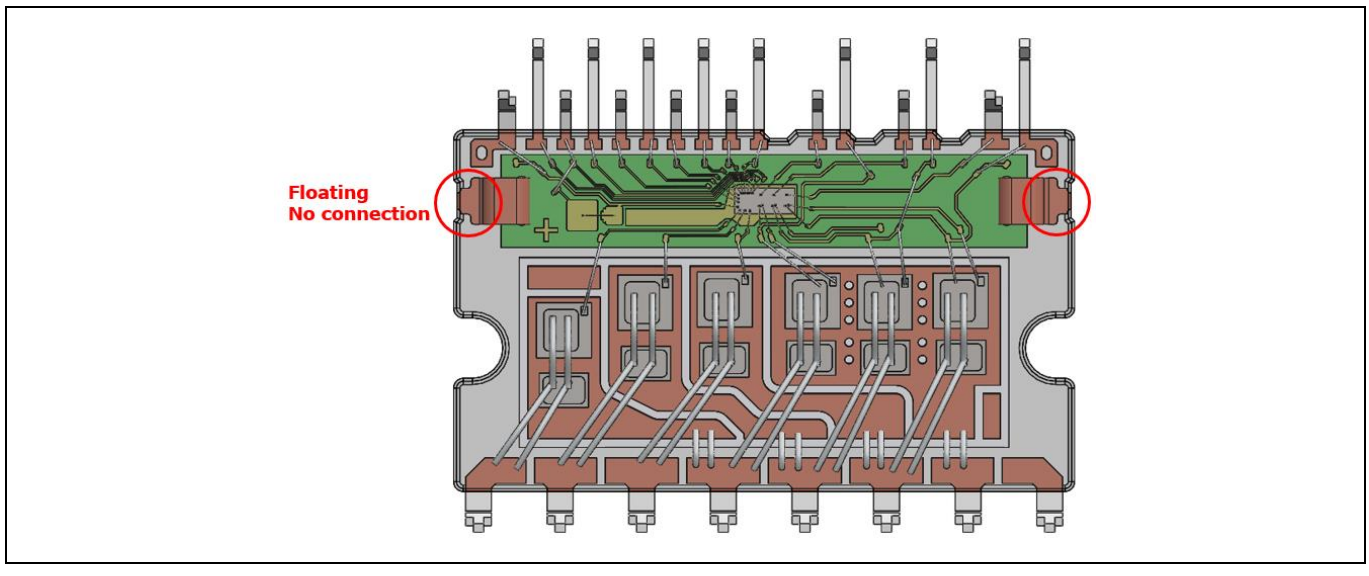


Figure 3 Internal view of the dummy pins

3 Product overview

3.1 Internal circuit and features

Figure 4 illustrates the internal block diagram of IM06BxxxC1. It consists of a 3-phase inverter circuit and a gate driver IC with control functions.

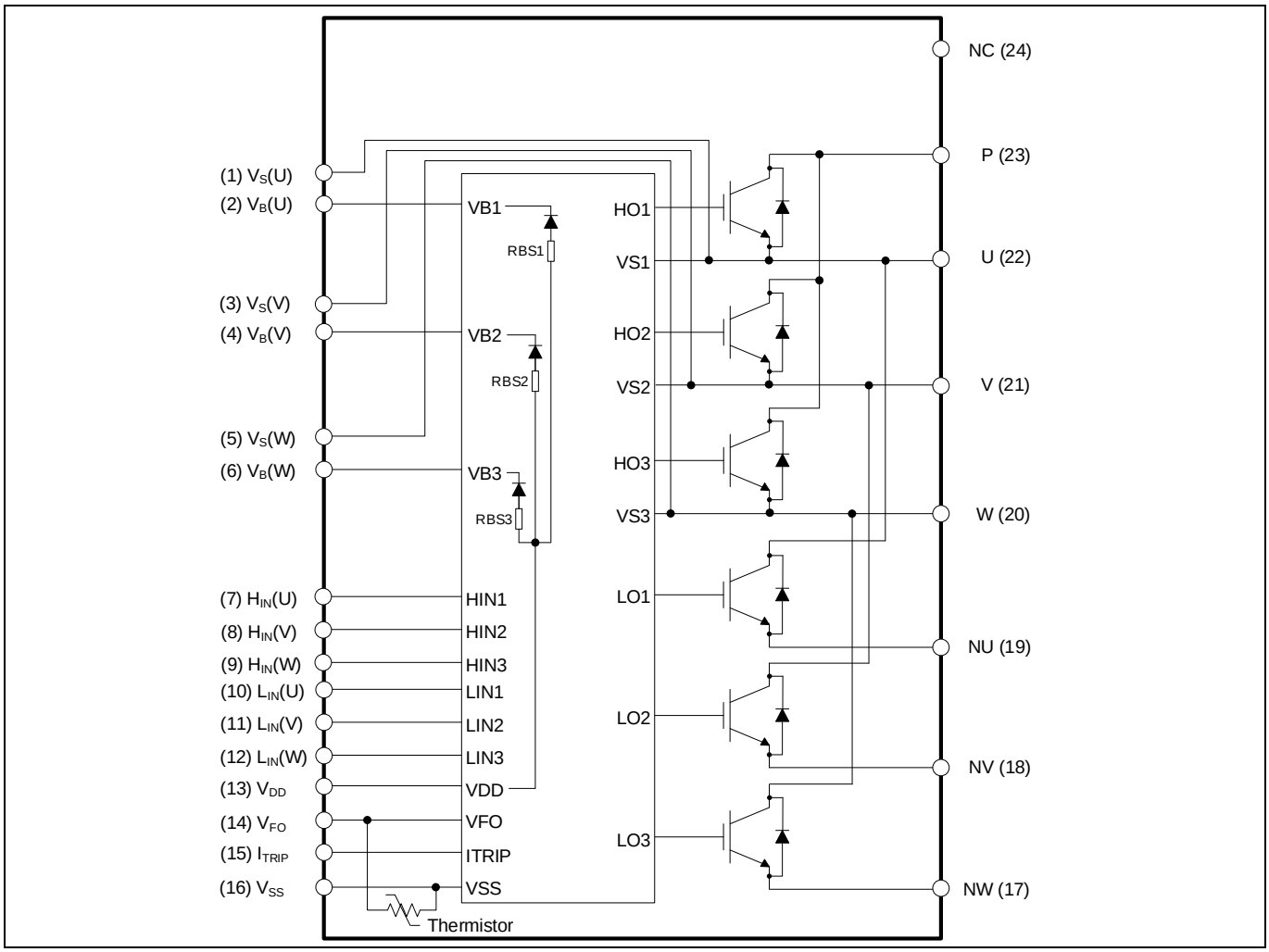


Figure 4 Internal circuit (3-phase inverter with an open emitter)

The detailed features and integrated functions of IM06BxxxC1 are as follows:

Features

- 600 V/15 A, 20 A, 30 A, and 50 A rating in one physical package size (mechanical layouts are identical)
- Fully isolated, dual in-line (DIL) molded module
- 650 V TRENCHSTOP™ IGBT7 with anti-parallel diode (600 V emitter-controlled diode)
- Rugged SOI gate driver technology with stability against transient and negative voltage
- Integrated bootstrap functionality
- Matched delay times for all channels/built-in dead time
- Lead-free terminal plating; RoHS compliant

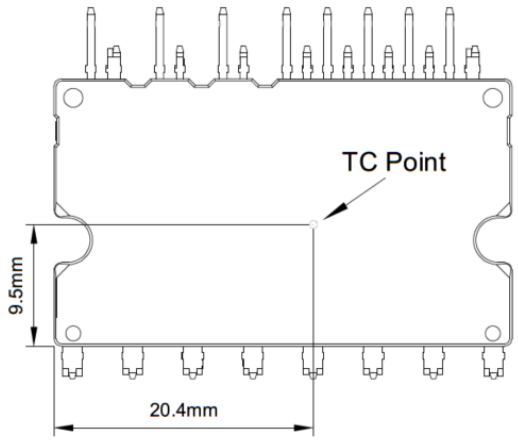
Functions

- Overcurrent shutdown
- Built-in, UL-certified NTC thermistor for temperature monitoring
- Undervoltage lockout for all channels
- Low-side emitter pins accessible for current monitoring
- Cross-conduction prevention
- All six switches turn off during protection

3.2 Maximum electrical ratings

Table 3 Detail description of absolute maximum ratings (IM06B15AC1)

Item	Symbol	Rating	Description
Maximum blocking voltage	V_{CES}	650 V	The sustained collector-emitter voltage of internal IGBTs
DC collector current	I_C	±15 A	The allowable IGBT DC collector current at T_C = 25°C
		±10 A	The allowable IGBT DC collector current at T_C = 80°C
Junction temperature	T_J	-40 ~ 150°C	Considering temperature ripple on the power chips, the maximum junction temperature rating of the IPM is 150°C
Maximum junction temperature	$T_{J.switch, max}$	175°C	The maximum junction temperature rating of built-in power chips is 175°C under this condition: maximum 10 seconds every 10 minutes for a maximum of 1 hour, cumulative over their lifetime
Operating case temperature range	T_C	-40 ~ 125°C	The T_C (case temperature) is defined as the temperature of the package surface underneath the specified power chip. Mount a temperature sensor onto the heatsink surface at the defined position, shown in Figure 5, to get an accurate temperature reading. All IPMs Tc point are different, please note to the datasheet.



[IM06B15AC1]

Figure 5 T_C measurement point from top view (Unit: [mm])

3.3 Electrical characteristics

Table 4 and Table 5 show the static and dynamic characteristics of IM06B15AC1.

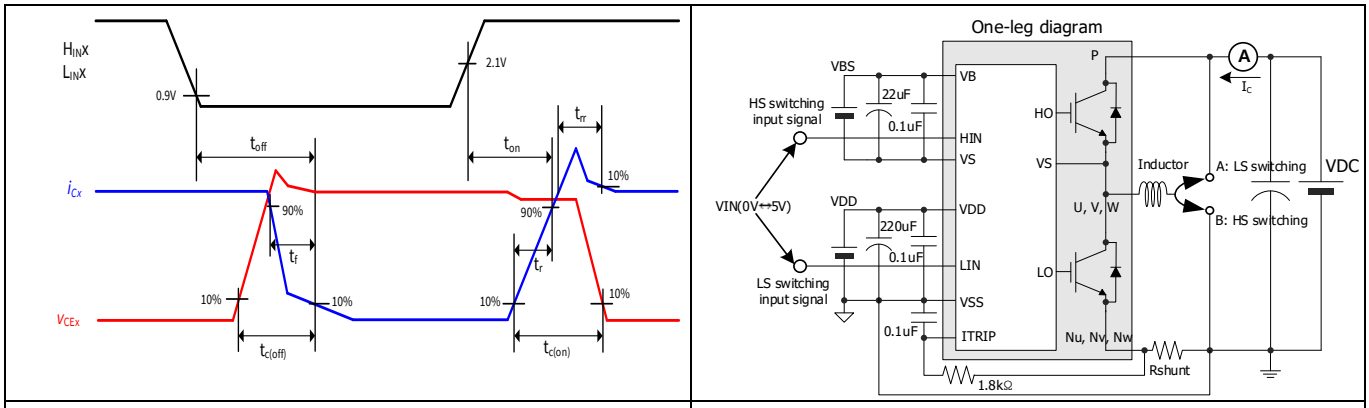
Table 4 Static characteristics of IM06B15AC1 (at V_{DD} = V_{BS} = 15 V)

Description	Symbol	Condition		Value			Unit
				Min.	Typ.	Max.	
Collector-emitter saturation voltage	$V_{CE(Sat)}$	V_{IN} = 5 V, I_C = 15 A	T_J = 25°C	-	1.35	1.7	V
			T_J = 150°C	-	1.5	-	
Diode's forward voltage	V_F	V_{IN} = 0 V, I_F = 15 A	T_J = 25°C	-	1.75	2.2	V
			T_J = 150°C	-	1.75	-	

Table 5 Dynamic characteristics of IM06B15AC1 (at V_{DD} = 15 V, T_J = 25°C)

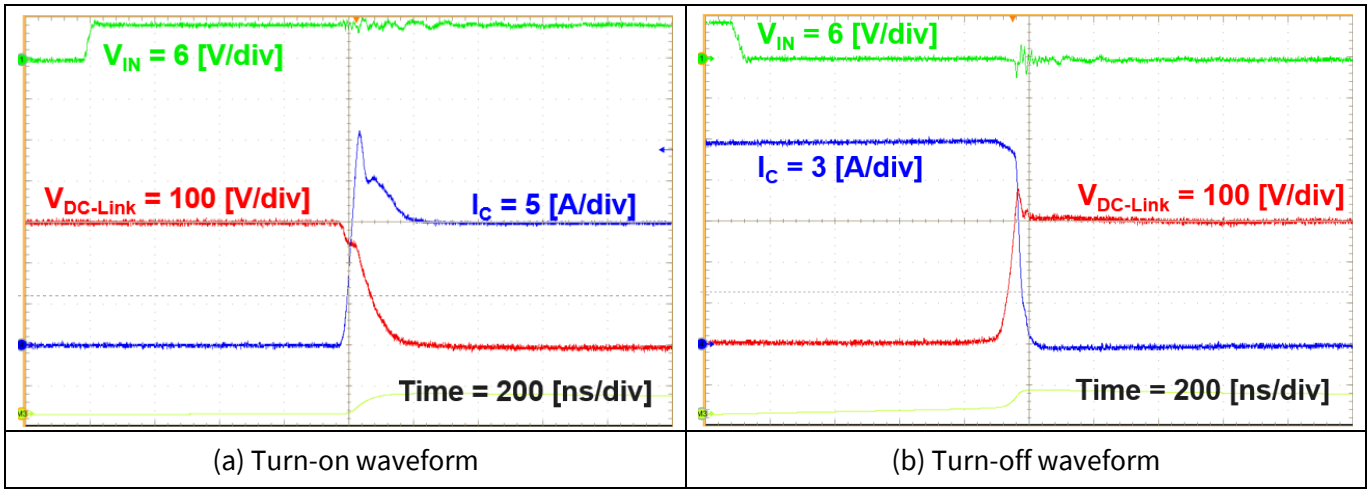
Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Turn-on propagation delay time	t_{on}	$V_{LIN, HIN}$ = 0 V → 5 V I_C = 15 A V_{DC} = 300 V	-	795	-	ns
Turn-on rise time	t_r		-	25	-	ns
Turn-on switching time	$t_{c(on)}$		-	135	-	ns
Reverse recovery time	t_{rr}		-	105	-	ns
Turn-off propagation delay time	t_{off}	$V_{LIN, HIN}$ = 5 V → 0 V I_C = 15 A V_{DC} = 300 V	-	985	-	ns
Turn-off fall time	t_f		-	30	-	ns
Turn-off switching time	$t_{c(off)}$		-	80	-	ns

The definition of switching time and the evaluation method are shown in Figure 6 (a) and (b). Switching characteristics are measured by a half-bridge circuit with inductive load. Figure 7 shows the typical switching waveforms of IM06B15AC1.



(a) Switching time definition | (b) Inductive load-switching test circuit

Figure 6 Switching time definition and evaluation circuit for switching test

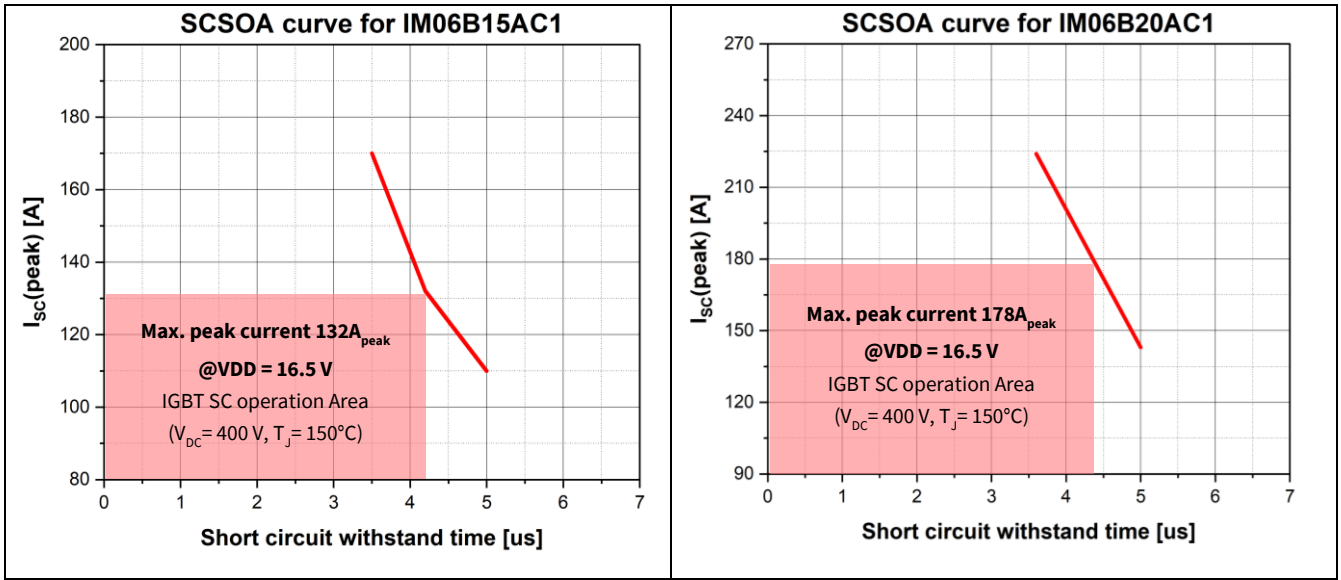


(a) Turn-on waveform | (b) Turn-off waveform

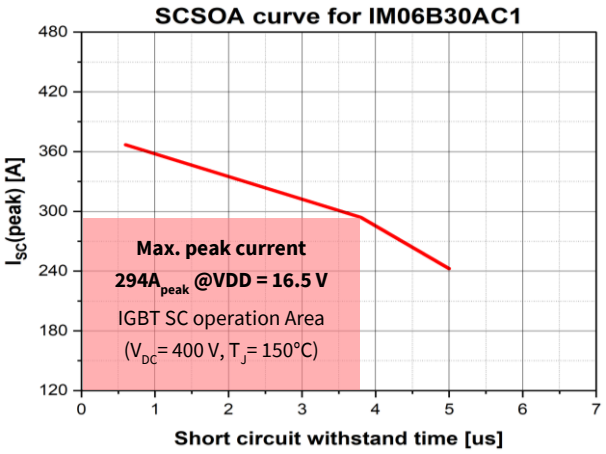
Figure 7 The typical switching waveforms of IM06B15AC1 (V_{DC} = 300 V, V_{DD} = 15 V, I_C = 15 A, T_J = 150°C, inductive load)

3.4 Characteristics of the short-circuit safety operation area (SCSOA)

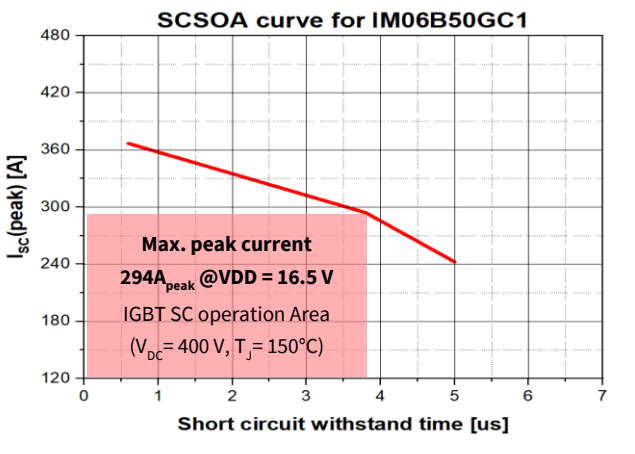
Figure 8 shows the typical (not guaranteed) SCSOA performance graph of the IM06BxxxC1 products during a short circuit event under the given conditions. In the case of IM06B30AC1, the graph illustrates that if the short circuit time is less than 3.8 µs, the IGBT can turn off safely. The IGBT can shut down a short-circuit current (non-repetitive) of about 294 A_{peak} under a controlled supply voltage of 16.5 V.



(a) IM06B15AC1 | (b) IM06B20AC1



(c) IM06B30AC1



(d) IM06B50GC1

Figure 8 The typical SCSOA graph of IM06BxxxC1 products (at V_{DC} = 400 V, $V_{PN\ (surge)}$ < 600 V, T_J = 150°C)

3.5 Description of the input and output pins

Table 6 lists the input and output pins of IM06BxxxC1. Detailed functional descriptions are given after Table 6.

3.6 Pin assignment

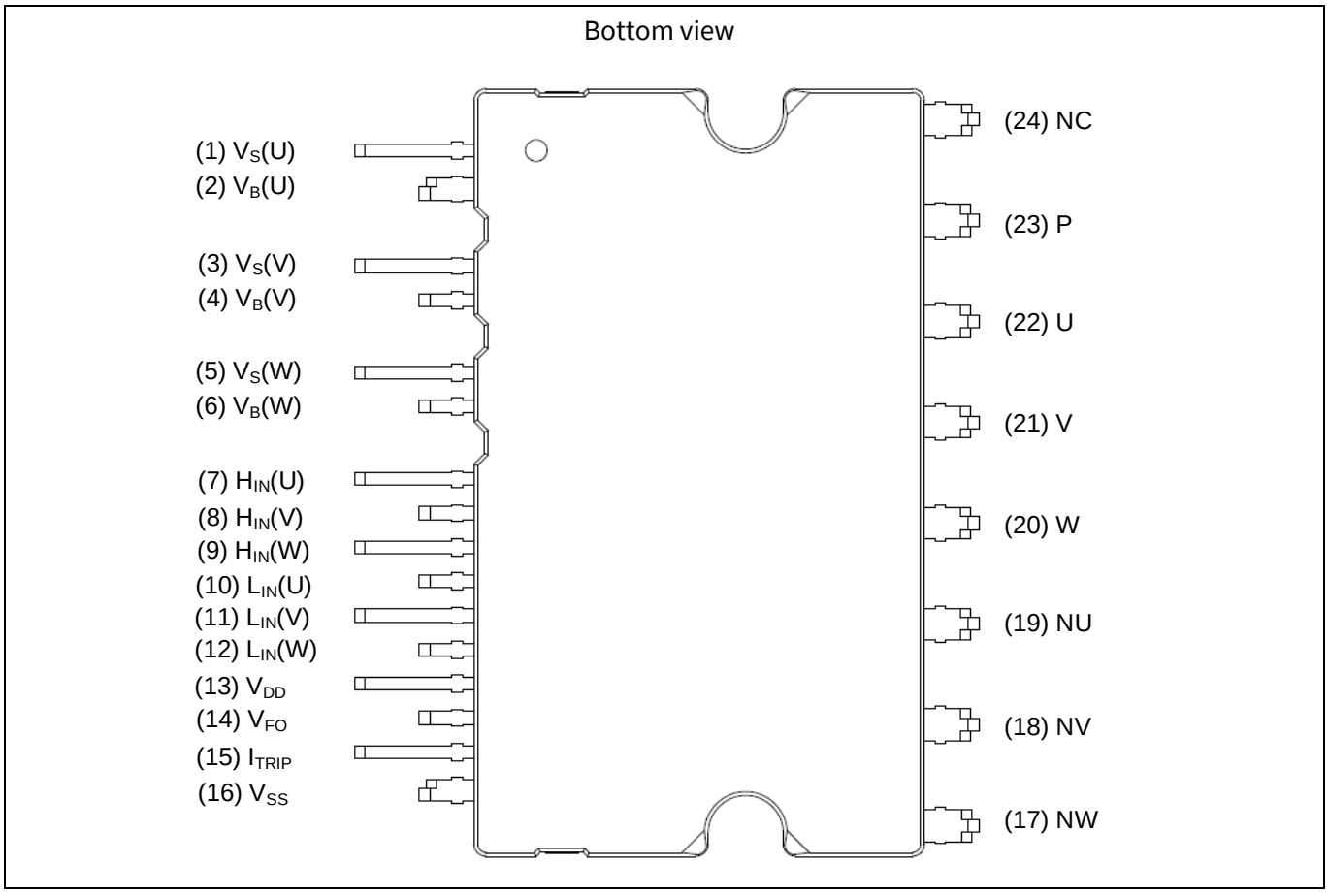


Figure 9 Pin assignment

Table 6 Pin descriptions for IM06BxxxC1

Pin number	Pin name	Pin description
1	V_S(U)	U-phase high-side floating IC supply offset voltage
2	V_B(U)	U-phase high-side floating IC supply voltage
3	V_S(V)	V-phase high-side floating IC supply offset voltage
4	V_B(V)	V-phase high-side floating IC supply voltage
5	V_S(W)	W-phase high-side floating IC supply offset voltage
6	V_B(W)	W-phase high-side floating IC supply voltage
7	H_{IN}(U)	U-phase high-side gate driver input
8	H_{IN}(V)	V-phase high-side gate driver input
9	H_{IN}(W)	W-phase high-side gate driver input
10	L_{IN}(U)	U-phase low-side gate driver input
11	L_{IN}(V)	V-phase low-side gate driver input
12	L_{IN}(W)	W-phase low-side gate driver input
13	V_{DD}	Low-side control supply
14	V_{FO}	Fault output/temperature monitor
15	I_{TRIP}	Overcurrent shut down input
16	V_{SS}	Low-side control negative supply
17	NW	W-phase low-side emitter
18	NV	V-phase low-side emitter
19	NU	U-phase low-side emitter
20	W	Motor W-phase output
21	V	Motor V-phase output
22	U	Motor U-phase output
23	P	Positive bus input voltage
24	NC	No connection

High-side bias voltage pins for driving the IGBT

Pins: V_B (U, V, W) – V_S (U, V, W)

- These pins provide gate-drive power to the high-side IGBTs
- The ability to utilize a bootstrap circuit scheme for the high-side IGBTs eliminates the need for external power supplies
- Each bootstrap capacitor is charged from the V_{DD} supply during the on-state of the corresponding low-side IGBT or the freewheeling state of the low-side freewheeling diode
- To prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low equivalent series resistors and inductance) filter capacitor should be mounted very close to these pins

Low-side bias voltage pin

Pin: V_{DD}

- This is the control supply pin for the internal IC
- To prevent malfunctions caused by noise and ripples in the supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted very close to this pin

Low-side common-supply ground pin

Pin: V_{SS}

- This pin connects the control ground to internal IC

Signal input pins

Pins: H_{IN} (U, V, W), L_{IN} (U, V, W)

- These pins are used to control the operation of the internal IGBTs
- They are activated by the voltage input signals. The terminals are internally connected to a Schmitt trigger circuit composed of 3.3 V/5.0 V class complementary metal oxide semiconductor (CMOS)
- The signal logic of these pins is active-high. The IGBT associated with each of these pins turns on when a sufficient logic voltage is applied to these pins
- The wiring of each input should be as short as possible to protect IM06BxxxC1 against noise influences
- To prevent signal oscillations, an RC coupling is recommended as shown in Figure 17

Overcurrent detection pin

Pin: I_{TRIP}

- The current sensing shunt resistor should be connected between the N pin (emitter of the low-side IGBT) and the power ground to detect short-circuit current (refer to Figure 22). An RC filter should be connected between the shunt resistor and the I_{TRIP} pin to eliminate noise
- The integrated comparator is triggered if the voltage V_{ITRIP} is higher than 0.525 V. The shunt resistor selected should meet this level in the application. In the case of a trigger event, the voltage at the RFE pin is pulled down to LOW
- The connection length between the shunt resistor and the I_{TRIP} pin should be minimal

Fault-output and temperature-monitoring pin

Pin: V_{FO}

- This is the fault-output alarm pin. An active low output is given on this pin for the fault-state condition in the CIPOS™ Mini. The alarm conditions are overcurrent detection and low-side bias undervoltage operation
- The V_{FO} output is open drain configured. The V_{FO} signal line should be pulled up to the logic power supply (5 V/3.3 V) with proper resistance considering temperature monitoring with a thermistor connected in parallel between V_{FO} and V_{SS} pins (optional)

Positive DC-link pin

Pin: P

- This is the DC-link positive power supply pin
- It is internally connected to the collectors of the high-side IGBTs

- To suppress the surge voltage caused by the DC-link wiring or PCB-pattern inductance, connect a smoothing filter capacitor close to this pin. Typically, metal film capacitors are used

Negative DC-link pins

Pins: NU, NV, NW

- These are the DC-link negative power supply pins (power ground) of the inverter
- These pins are connected to the low-side IGBT emitters of each phase

Inverter power-output pins

Pins: U, V, W

- These are inverter output pins to connect to the inverter load (e. g., the motor)

3.7 Outline drawing

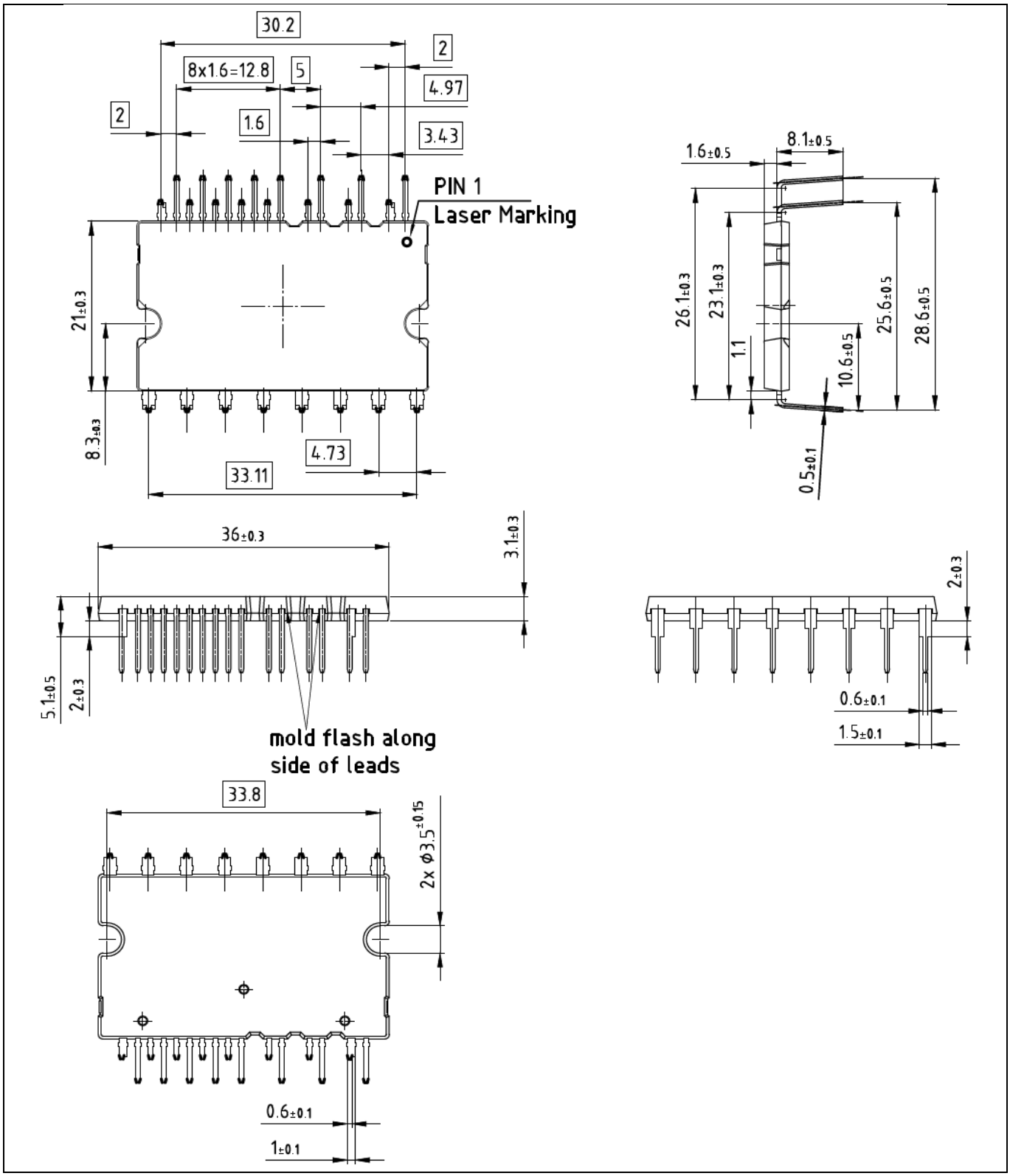


Figure 10 The package outline with dimensions of DIP 32x21 (Unit: [mm])

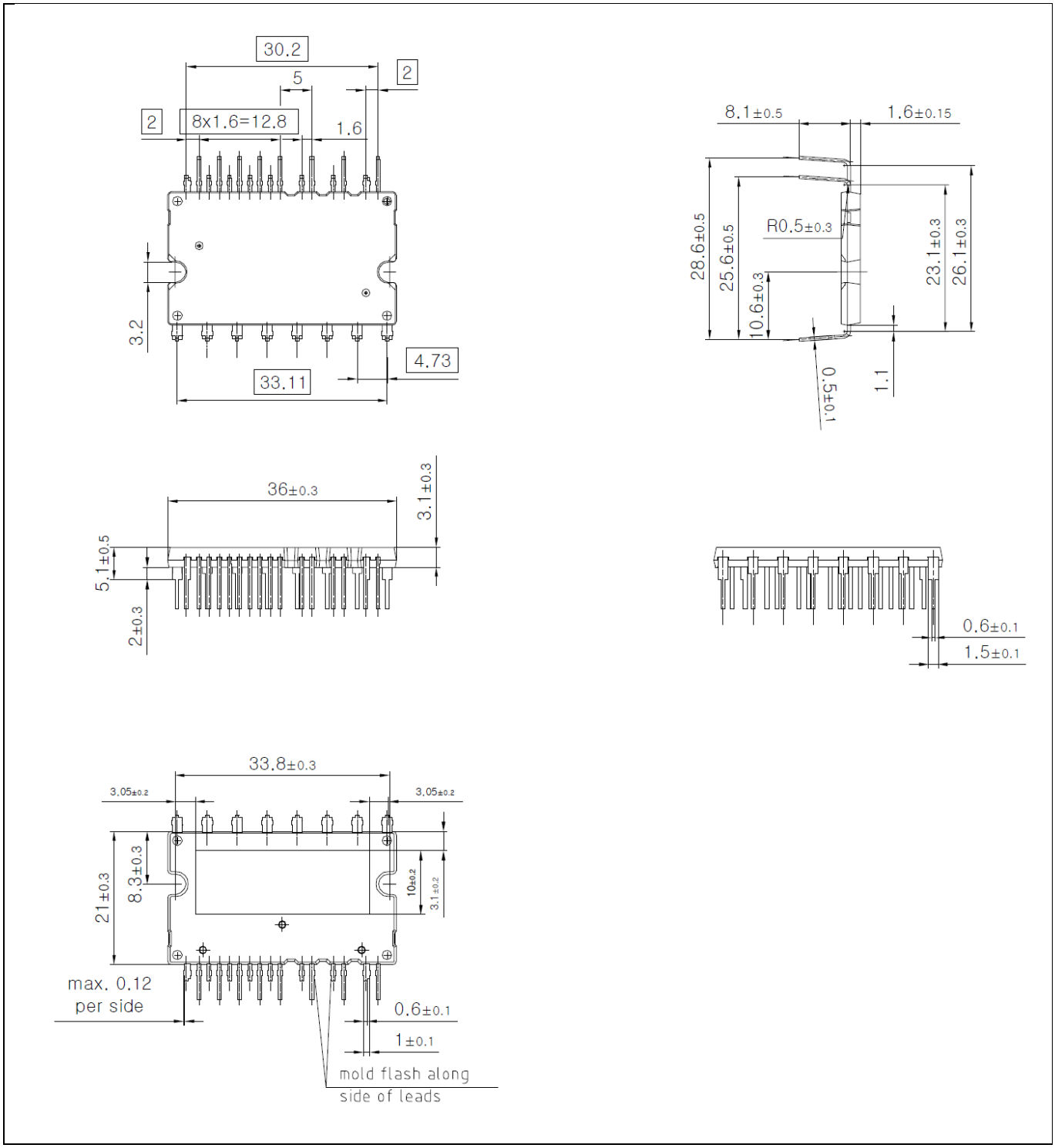
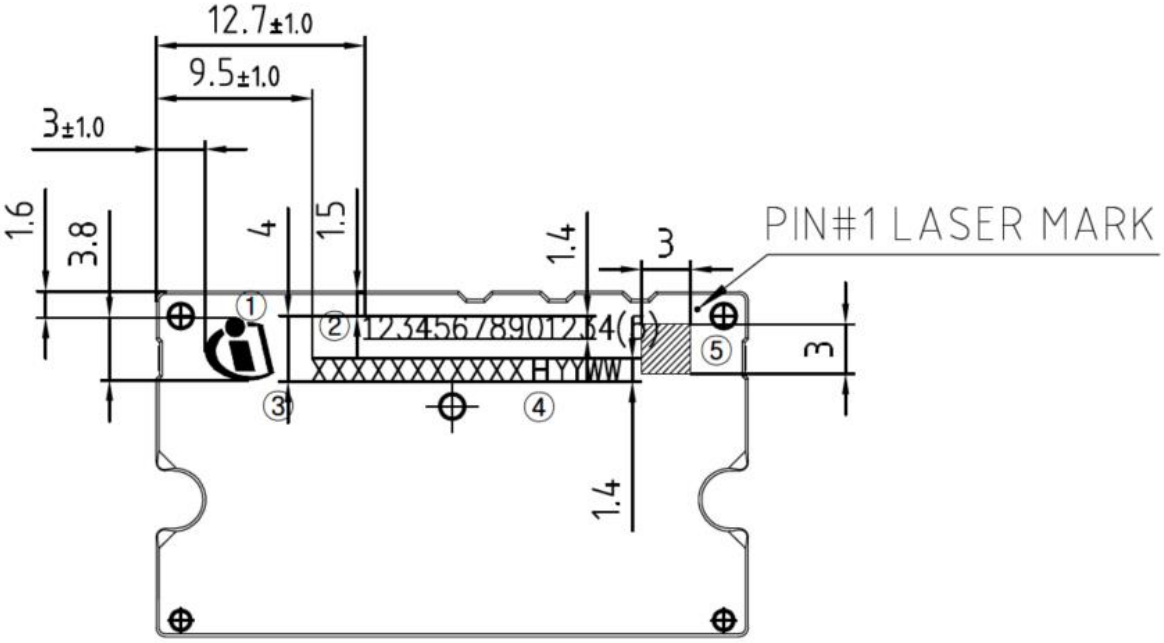


Figure 11 The package outline with dimensions of DIP 32x21D (Unit: [mm])

3.8 Marking

Figure 12 shows the laser marking specifications for IM06BxxxC1. The company logo, the device type, the lot number, the date code, and the matrix code (2D) are marked on the upper side of the module.



<MARKING INFORMATION>

① : Company Logo

② : Product(Device) name
PICTURE NO1: 14 DIGITS; PICTURE NO 2: 15 DIGITS

③ : Lot number

④ : Date code

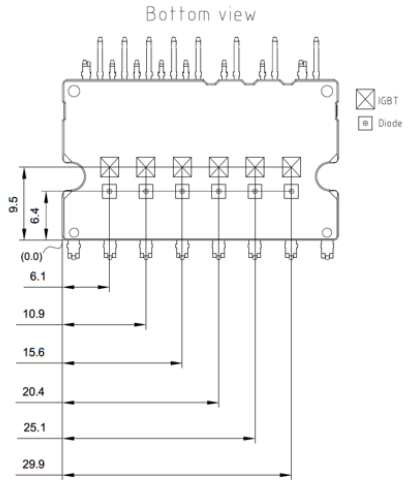
⑤ : Data-matrix code
DATA MATRIX CODE 47x47 DOTS (3x3mm)
(DOT SIZE: 0.0638 mm)

Figure 12 Marking information

3.9 Chip positions and locations

Figure 13 to Figure 16 show the chip positions and location of each product.

Chip position



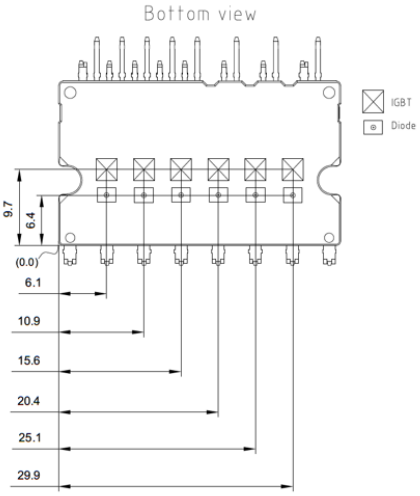
Chip location

Note: Chip location is from (0,0).

Item	Chip location (X,Y) (mm)		T_C point
	IGBT	Diode	
Chip 1 (Low-side W-phase)	6.1, 9.5	6.1, 6.4	
Chip 2 (Low-side V-phase)	10.9, 9.5	10.9, 6.4	
Chip 3 (Low-side U-phase)	15.6, 9.5	15.6, 6.4	IGBT
Chip 4 (High-side W-phase)	20.4, 9.5	20.4, 6.4	
Chip 5 (High-side V-phase)	25.1, 9.5	25.1, 6.4	
Chip 6 (High-side U-phase)	29.9, 9.5	29.9, 6.4	

Figure 13 Chip position and location of IM06B15AC1

Chip position



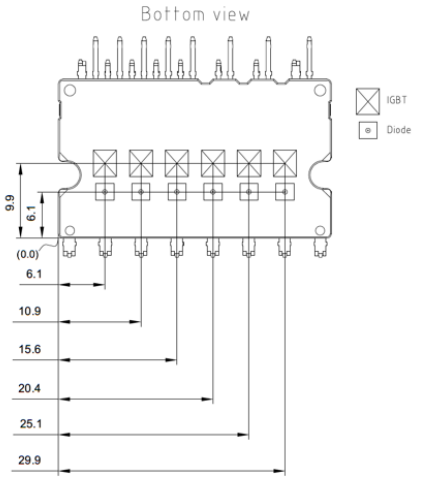
Chip location

Note: Chip location is from (0,0).

Item	Chip location (X,Y) (mm)		T_C point
	IGBT	Diode	
Chip 1 (Low-side W-phase)	6.1, 9.7	6.1, 6.4	
Chip 2 (Low-side V-phase)	10.9, 9.7	10.9, 6.4	
Chip 3 (Low-side U-phase)	15.6, 9.7	15.6, 6.4	IGBT
Chip 4 (High-side W-phase)	20.4, 9.7	20.4 6.4	
Chip 5 (High-side V-phase)	25.1, 9.7	25.1, 6.4	
Chip 6 (High-side U-phase)	29.9, 9.7	29.9, 6.4	

Figure 14 Chip position and location of IM06B20AC1

Chip position



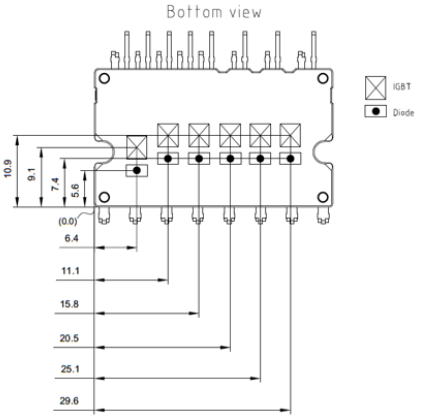
Chip location

Note: Chip location is from (0,0).

Item	Chip location (X,Y) (mm)		T_C point
	IGBT	Diode	
Chip 1 (Low-side W-phase)	6.1, 9.9	6.1, 6.1	
Chip 2 (Low-side V-phase)	10.9, 9.9	10.9, 6.1	
Chip 3 (Low-side U-phase)	15.6, 9.9	15.6, 6.1	IGBT
Chip 4 (High-side W-phase)	20.4, 9.9	20.4 6.1	
Chip 5 (High-side V-phase)	25.1, 9.9	25.1, 6.1	
Chip 6 (High-side U-phase)	29.9, 9.9	29.9, 6.1	

Figure 15 Chip position and location of IM06B30AC1

Chip position



Chip location

Note: Chip location is from (0,0).

Item	Chip location (X,Y) (mm)		T_C point
	IGBT	Diode	
Chip 1 (Low-side W-phase)	6.4, 9.1	6.4, 5.6	
Chip 2 (Low-side V-phase)	11.1, 10.9	11.1, 7.4	
Chip 3 (Low-side U-phase)	15.8, 10.9	15.8, 7.4	IGBT
Chip 4 (High-side W-phase)	20.5, 10.9	20.5, 7.4	
Chip 5 (High-side V-phase)	25.1, 10.9	25.1, 7.4	
Chip 6 (High-side U-phase)	29.6, 10.9	29.6, 7.4	

Figure 16 Chip position and location of IM06B50GC1

4 Interface circuit and layout guide

4.1 Input and output signal connection

Figure 17 shows the I/O interface circuit between the microcontroller unit (MCU) and the IPM. The IPM's input logic is active-high with internal pull-down resistors. No external pull-down resistors are needed. The VFO output is open drain configured. This signal should be pulled up to the positive side of the 5 V or 3 V external-logic power supply using a pull-up resistor. The value of the pull-up resistor should be selected properly. For example, 3.6 kΩ with a thermistor connected in parallel between the V_{FO} and V_{SS} pins.

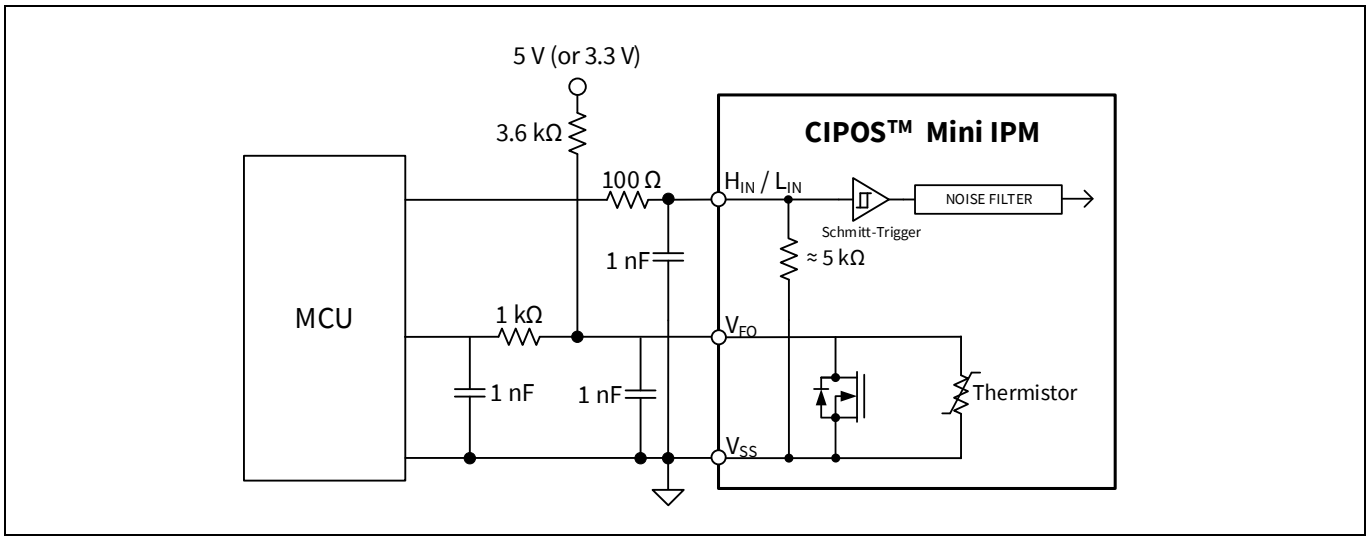


Figure 17 The recommended MCU I/O interface circuit

Table 7 Maximum input ratings

Item	Symbol	Condition	Value	Unit
Module supply voltage	V_{DD}	Applied between V_{DD} – V_{SS}	-1 ~ 20	V
High-side floating supply voltage	V_{BS}	Applied between V_B (U, V, W) – V_S (U, V, W)	-1 ~ 20	V
Input voltage	V_{IN}	Applied between H_{IN} (U, V, W) – V_{SS}, L_{IN} (U, V, W) – V_{SS}	-1 ~ V_{DD}+0.3	V

The maximum ratings for the input voltages are listed in Table 7. As the input voltage rating is V_{DD}+0.3 V, a 15 V supply interface is possible. However, it is recommended that the input signal be configured with a 5.0 V or 3.3 V logic supply to connect directly to the MCU. It is recommended that the bypass capacitors be placed as close as possible to the signal lines from the MCU as well as the IPM.

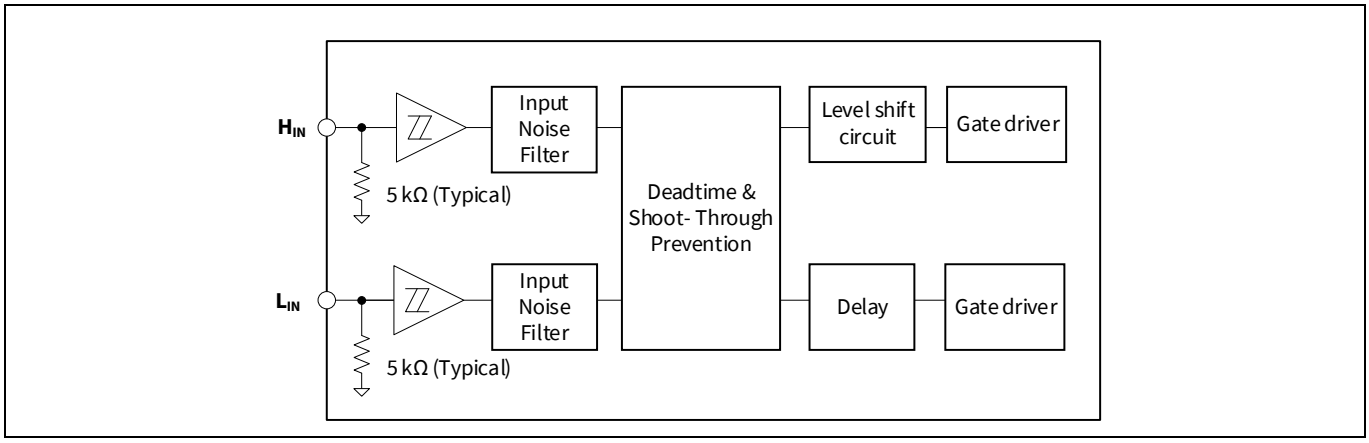


Figure 18 Simplified block diagram of the IM06BxxxC1 gate driver IC

The IM06BxxxC1 products employ active-high input logic. Therefore, the power sequence restriction between the control supply and the input signal during startup or shutdown operations does not exist. This makes the system fail-safe. Additionally, as pull-down resistors are built into each input circuit, external pull-down resistors are not required. This reduces the required external component count. Schmitt trigger for the input, noise filter, and the dead time and shoot-through prevention functions provide beneficial noise cancellation for short input pulses.

The inputs of IM06BxxxC1 are compatible with standard the CMOS and TTL outputs. The gate driver IC of IM06BxxxC1 has been designed to be compatible with 3.3 V and 5.0 V logic-level signals. Therefore, by lowering the turn-on and turn-off threshold voltage of the input signal, as shown in Table 8, a direct connection to the 3.3 V/5.0 V class MCU is possible.

Table 8 Threshold voltage of the input (at V_{DD} = 15 V, T_J = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic “1” input voltage (L_{IN}, H_{IN})	V_{IH}	H_{IN} – V_{SS}	1.7	2.0	2.3	V
Logic “0” input voltage (L_{IN}, H_{IN})	V_{IL}	L_{IN} – V_{SS}	0.7	0.9	1.1	V

As shown in Figure 18, the input signal section of IM06BxxxC1 integrates a 5 kΩ (typical) pull-down resistor. Therefore, when using an external filtering resistor between the MCU output and the IPM input, notice the signal voltage drop at the IPM input terminals. It should fulfill the requirements of the logic “1” input voltage. For example, R = 100 Ω and C = 1 nF for the parts shown in Figure 17.

4.2 Internal dead time

The gate driver IC of IM06BxxxC1 features integrated dead time protection circuitry. The dead time for gate driver IC is fixed. The dead time feature inserts a time (a minimum dead time) during which both the high-side and low-side power switches are held off. This is done to ensure that the power switch being turned off has fully turned off before the second power switch turns on.
This minimum dead time is automatically inserted whenever the external dead time is shorter than DT_{IC}. Any external dead time larger than DT_{IC} is not modified by the gate driver IC.

Table 9 Internal dead time (at V_{DD} = 15 V, T_J = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal dead time	DT_{IC}	V_{IN} = 0 V or V_{IN} = 5 V	-	360	-	ns

4.3 Cross-conduction prevention circuitry

The gate driver IC of IM06BxxxC1 is equipped with a shoot-through protection circuitry (also known as the cross-conduction prevention circuitry or interlock circuitry). Figure 19 shows how this protection circuitry prevents both the high-side and the low-side switches from conducting at the same time.

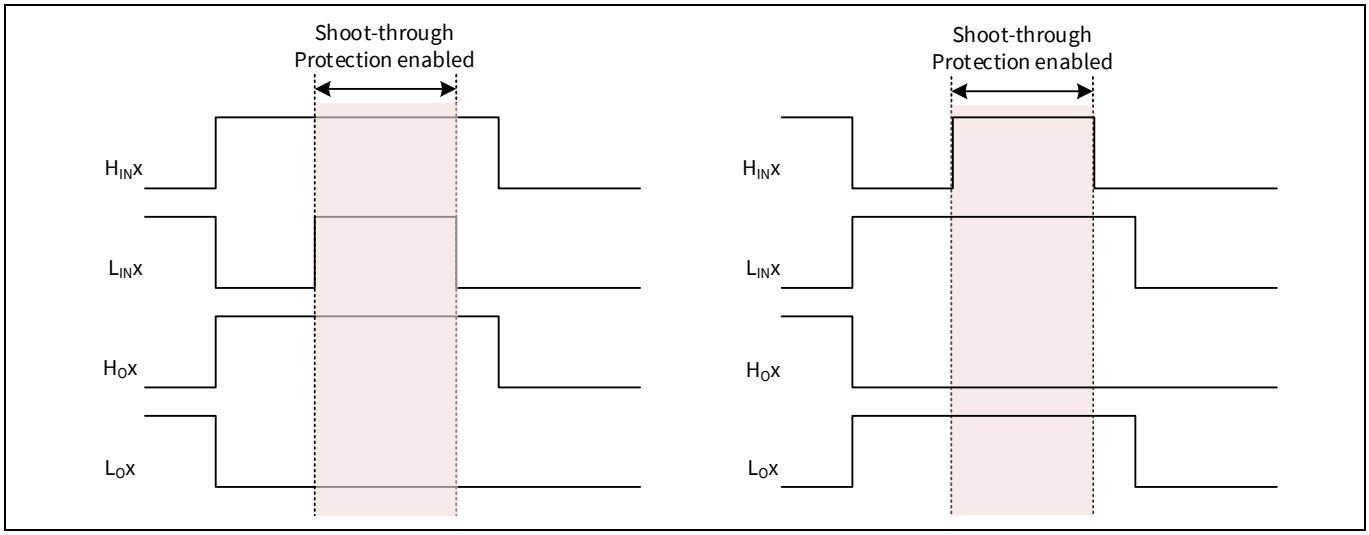


Figure 19 illustration of a shoot-through protection circuitry

4.4 Advanced input filter

The advanced input filter improves the input/output pulse symmetry of the gate driver IC and helps eject noise spikes and short pulses. This input filter is applied to the H_{IN} and L_{IN} inputs. The working principle of this new filter is shown in Figure 20.

Figure 20 (a) shows a typical input filter and the asymmetry of the input and output. The upper pair of waveforms (Example 1) shows an input signal width with a duration much longer than $t_{FIL,IN}$. The resulting output is approximately the difference between the input signal and the $t_{FIL,IN}$.

The lower pair of waveforms (Example 2) shows an input signal with a duration slightly longer than $t_{FIL,IN}$; the resulting output is approximately the difference between the input signal and the $t_{FIL,IN}$.

Figure 20 (b) shows the advanced input filter of IM06BxxxC1 and the symmetry between the input and output. The upper pair of waveforms (Example 1) show an input signal with a duration much longer than $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal.

The lower pair of waveforms (Example 2) shows an input signal with a duration slightly longer than $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal.

Table 10 Input filter time (at V_{DD} = 15 V, T_J = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input filter time at L_{IN}, H_{IN} for turn-on and off	$t_{FIL,IN}$	$V_{LIN,HIN}$ = 0 V or 5 V	-	290	-	ns

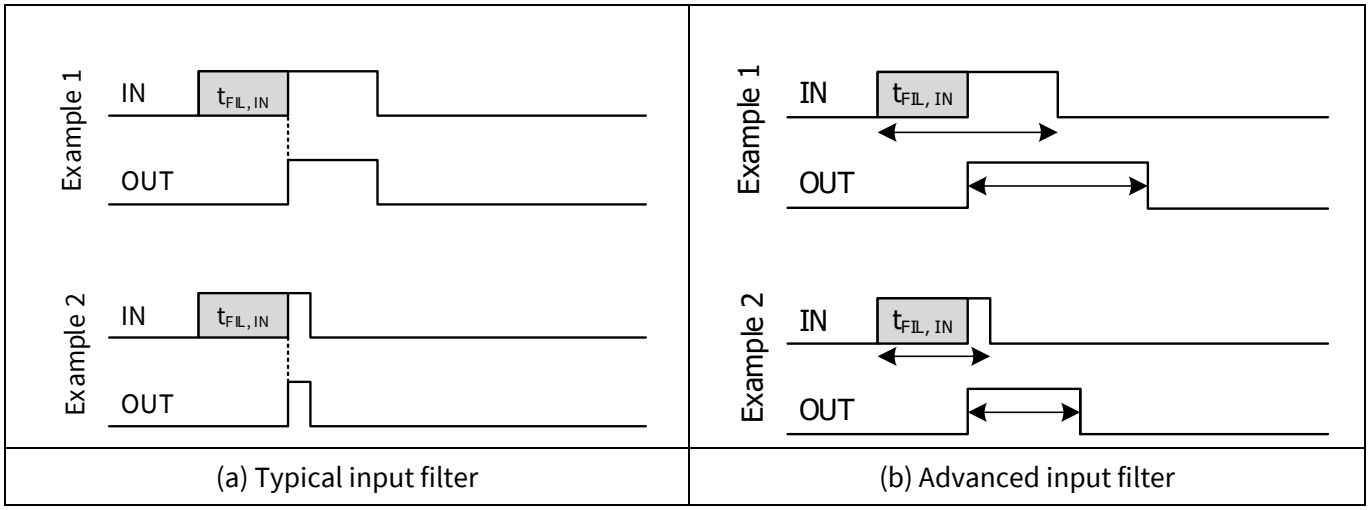


Figure 20 Characteristics of the internal input filter

4.5 Matching propagation-delay time

The gate driver IC of IM06BxxxC1 is designed with a propagation-delay matching circuitry. With this feature, the internal gate driver IC's response at the output to a signal at the input requires approximately the same time (t_{ON}, t_{OFF}) for both the low-side and the high-side channels. The maximum difference is specified by the delay-matching parameter (M_T). The propagation turn-on delay (t_{ON}) of IM06BxxxC1 matches with the propagation turn-off delay (t_{OFF}). The delay-matching turn-on/off between the high-side and the low-side means that there is a time difference between the L_O and H_O outputs when each output has reached 10% of its maximum (during turn-on), or when each output has decreased to 90% of its maximum (during turn-off), assuming that $H_{IN}x$ and $L_{IN}x$ are simultaneously applied. The shorter the delay-match time, the better the circuit performance.

Table 11 Matching propagation-delay time (at V_{DD} = 15 V and T_J = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Matching propagation delay time (On and Off) all channels	M_T	External dead time > 500 ns	-	20	-	ns

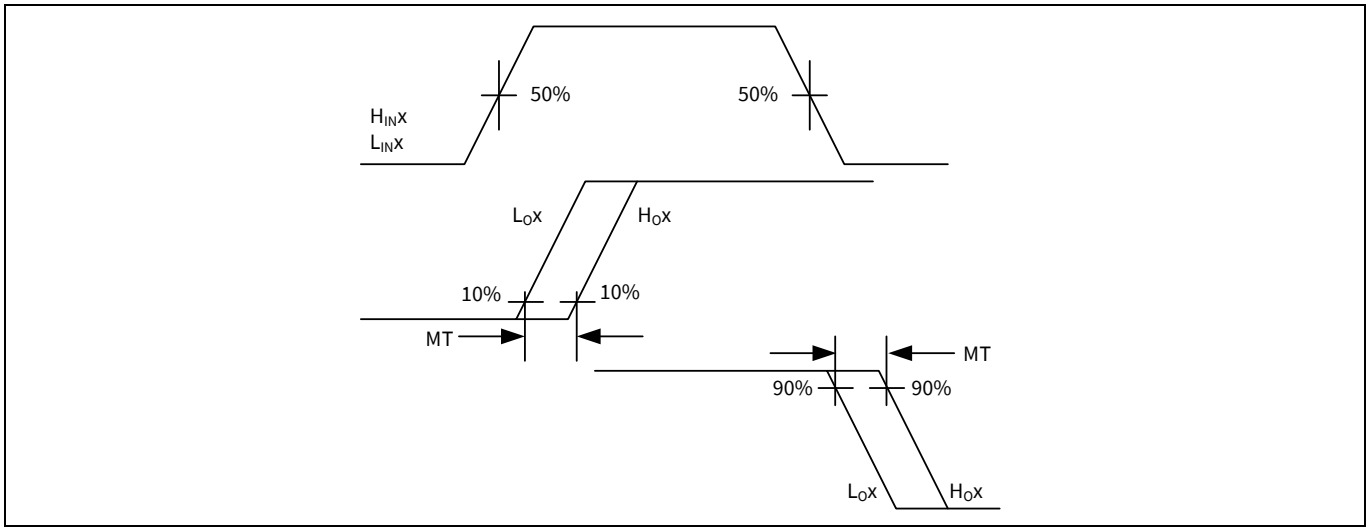


Figure 21 Definition of a delay-matching waveform

4.6 Example of a general interface circuit

Figure 22 shows the typical application circuit of IM06BxxxC1 for interface schematic with control signals connected directly to an MCU.

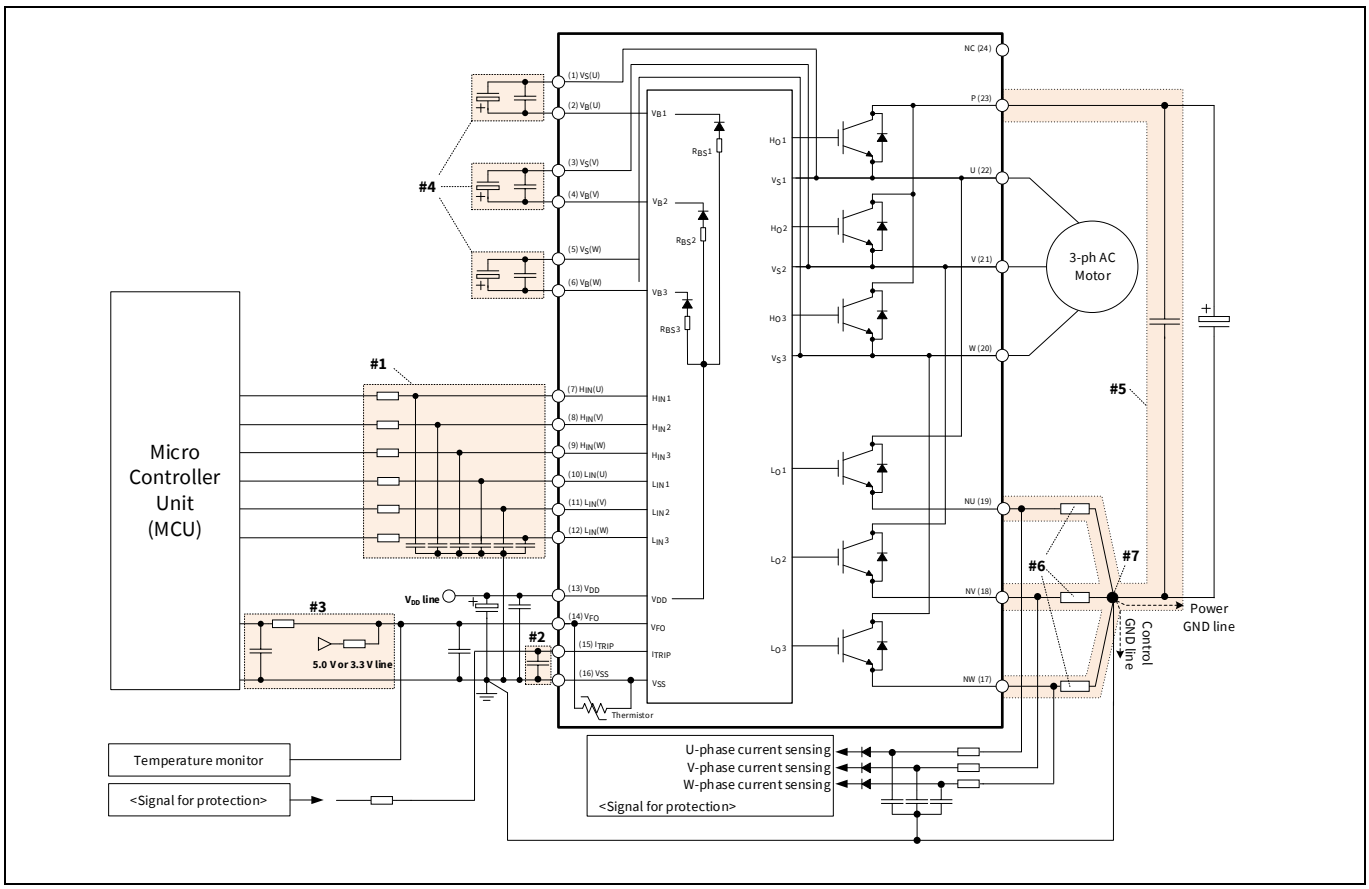


Figure 22 Example of an application circuit

1. Input circuit
   - To reduce the input signal noise by high-speed switching. The R_{IN} and C_{IN} filter circuit should be mounted (100 Ω, 1 nF)
   - C_{IN} should be placed as close to the V_{SS} pin as possible
2. I_{TRIP} circuit
   - To prevent protection function errors, C_{ITRIP} should be placed as close to the I_{TRIP} and V_{SS} pins as possible
   - To prevent fault operation of the protection function, an RC filter of around 1.5 ~ 2.0 µs is recommended (68 Ω, 22 nF, “Signal for protection” in the schematic leads the signal into the micro controller unit”)
3. V_{FO} circuit
   - V_{FO} is an open-drain output. This signal line should be pulled up to the positive side of the 5 V/3.3 V logic power supply with a proper resistor
   - It is recommended that the RC filter be placed as close to the controller as possible
4. V_B - V_S circuit
   - Capacitor for the high-side floating supply voltage should be placed as close to the V_B and V_S pins as possible
5. Snubber capacitor
   - The wiring between IM06BxxxC1 and the snubber capacitor (including shunt resistor) should be as short as possible

6. Shunt resistor
   - An SMD type shunt resistor should be used to reduce stray inductance
7. Ground pattern
   - The ground pattern should be separated at only one point on the shunt resistor. its connection to VSS and N of the DC-link should be as short as possible

4.7 Recommended rated output current of power supply

The control and gate-drive power for IM06BxxxC1 are normally provided by a single 15 V supply that is connected to the module's V_{DD} and the V_{SS} terminals. The circuit current of the 5.0 V logic power supply (V_{FO} and input terminals) is about 5 mA and the circuit current of IM06B30AC1's control supply (V_{DD}) is listed in Table 12.

Table 12 The circuit current of IM06B30AC1's control power supply (Unit: [mA])

Item		Static (typ.)	Dynamic (typ.)	Total (typ.)
V_{DD} = 15 V	f_{SW} = 5 kHz	1.17	2.97	4.14
	f_{SW} = 15 kHz	1.17	8.91	10.08
V_{DD} = 20 V	f_{SW} = 20 kHz	1.61	11.88	13.49

The recommended minimum circuit current values for the power supply are listed in Table 13. These take into consideration the ripple current and sufficient margins during the worst-case scenarios. Therefore, the circuit current should be estimated to be approximately five times higher than the calculated values.

Table 13 The recommended minimum circuit current for the power supply (Unit: [mA])

Item	The circuit current of +15 V control supply	The circuit current of +5 V logic supply
$V_{DD} \leq 20$ V, $f_{SW} \leq 20$ kHz	67.5	25.0

4.8 Recommended layout pattern for overcurrent protection and short-circuit protection

It is recommended that the connection between the I_{TRIP} filter capacitor and the IM06BxxxC1 pins be as short as possible. The I_{TRIP} filter capacitor should be connected to the V_{SS} pin directly without overlapping ground pattern. The signal ground and power ground should be as short as possible and connected at only one point via the filter capaciter of the V_{DD} line.

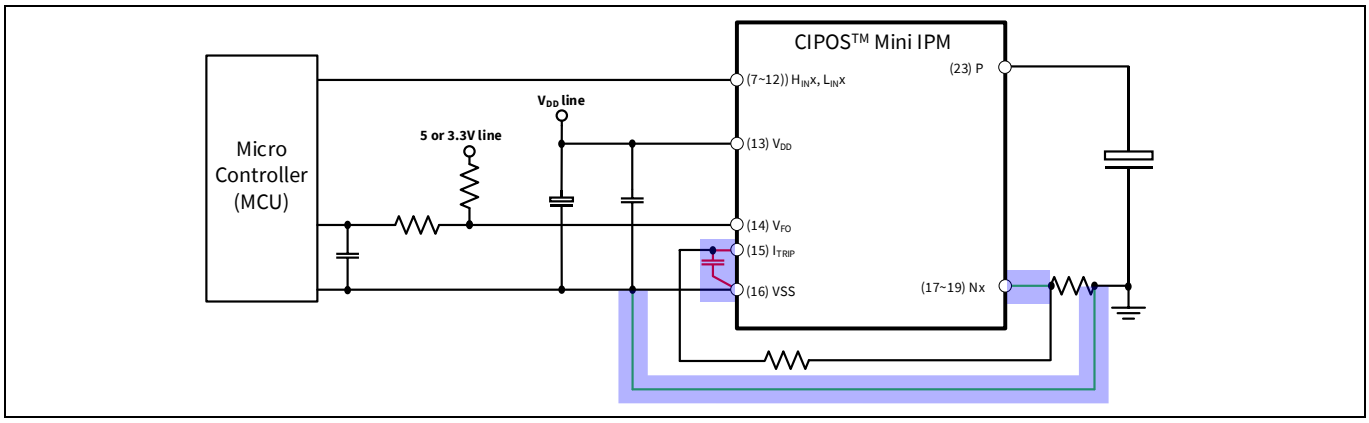


Figure 23 Recommended layout pattern for the overcurrent protection and short-circuit protection functions

4.9 Recommended wiring of the shunt resistor and snubber capacitor

External current-sensing resistors are applied to detect overcurrent during phase currents. A long wiring pattern between the shunt resistors and IM06BxxxC1 can cause excessive surges that might damage the IM06BxxxC1's internal IC and current-detection components. This may also distort the sensing signals. To decrease pattern inductance, the wiring between the shunt resistors and IM06BxxxC1 should be as short as possible.

As shown in Figure 24, snubber capacitors should be installed in the right location to suppress surge voltages effectively. Generally, a high frequency non-inductive capacitor of around 0.1 ~ 0.22 µF is recommended. If the snubber capacitor is installed in the wrong location '1' as shown in Figure 24, the snubber capacitor will not be able to suppress the surge voltage effectively. If the capacitor is installed in location '2', the charging and discharging currents generated by the wiring inductance and the snubber capacitor will appear on the shunt resistor. This will impact the current-sensing signal and the short-circuit protection level will be lower than the calculated design value. The surge suppression effect at position '2' is better than that at positions '1' or '3'. Position '3' is a reasonable compromise with better suppression than at location '1' and without impacting the accuracy of the current-sensing signal.

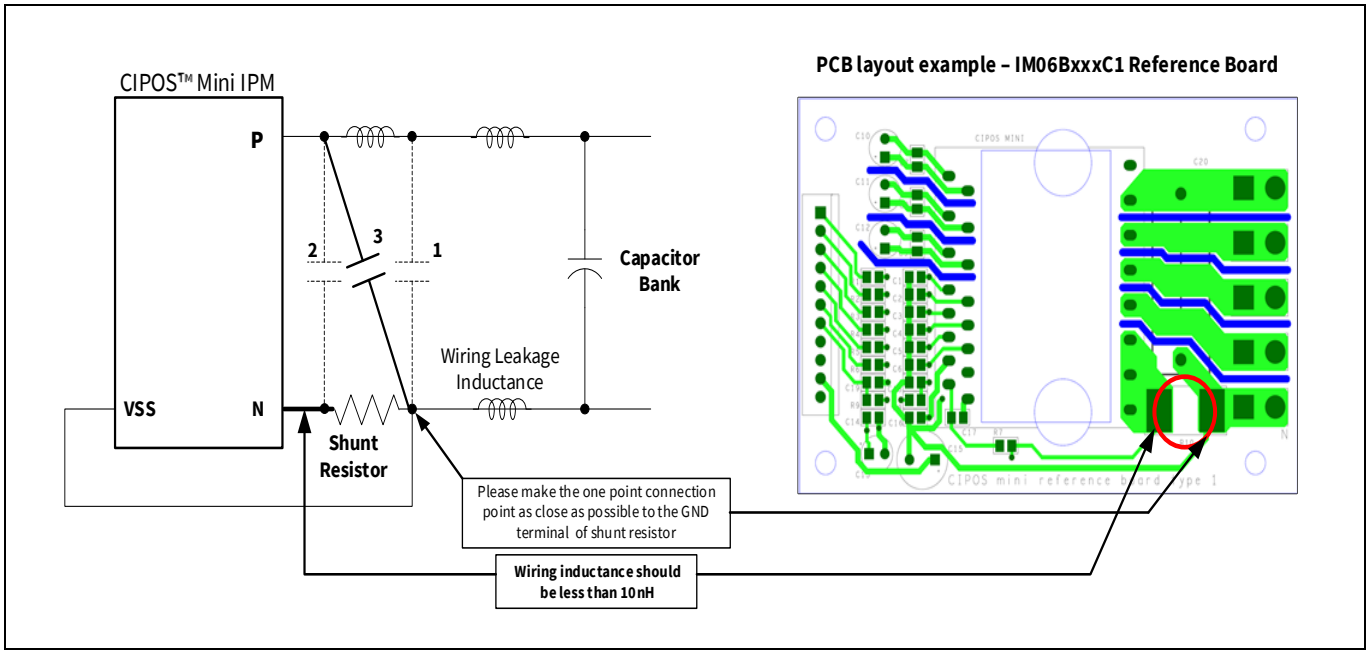


Figure 24 Recommended wiring of the shunt resistor and snubber capacitor

4.10 Pin and screw-hole coordinates for IM06BxxxC1

Figure 25 shows the position of IM06BxxxC1 on the PCB to indicate the center coordinates of each pin and screw holes listed in Table 14.

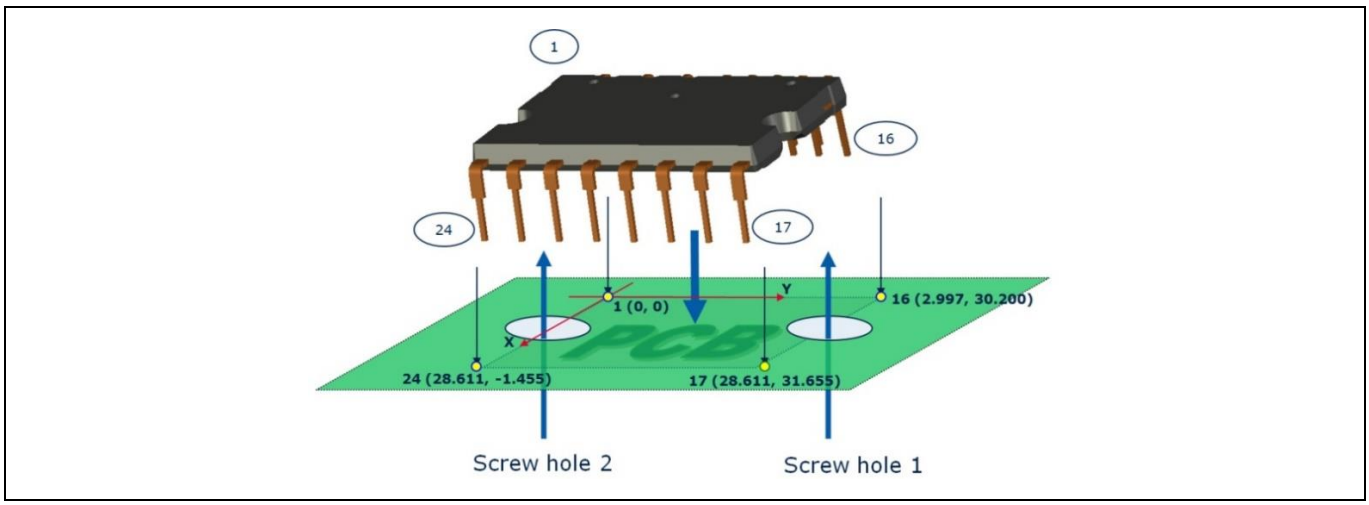


Figure 25 IM06BxxxC1 position on a PCB (Unit: [mm]) and example of a pad design (1 ~ 24pin)

Table 14 Pin and screw holes coordinates for the IM06BxxxC1 footprint (Unit: [mm])

Pin number		X	Y	Pin number		X	Y
Signal pin	1	0.000	0.000	Signal pin	14	2.997	26.600
	2	2.997	2.000		15	0.000	28.200
	3	0.000	5.400		16	2.997	30.200
	4	2.997	7.000	Power pin	17	28.611	31.655
	5	0.000	10.400		18	28.611	26.925
	6	2.997	12.000		19	28.611	22.195
	7	0.000	15.400		20	28.611	17.465
	8	2.997	17.000		21	28.611	12.735
	9	0.000	18.600		22	28.611	8.005
	10	2.997	20.200		23	28.611	3.275
	11	0.000	21.800		24	28.611	-1.455
	12	2.997	23.400	Screw hole	25	17.950	32.000
	13	0.000	25.000		26	17.950	-1.800

5 Protection features

5.1 Undervoltage protection

The control and gate-drive power for IM06BxxxC1 are normally provided by a single 15 V supply that is connected to the module's V_{DD} and V_{SS} terminals. For the module to operate properly, this voltage should be regulated to 15 V ± 10%. Table 15 describes the behavior of IM06BxxxC1 at various control supply voltages. The control supply should be well filtered with a low-impedance electrolytic capacitor and a high-frequency decoupling capacitor connected at the IM06BxxxC1's pins.

High-frequency noise on the supply side might cause the internal control IC to malfunction and generate erroneous fault signals. To avoid this problem, the maximum ripple on the supply should be less than ± 1 V/µs.

There is a difference in potential between the V_{SS} terminal and the N-power terminal due to a voltage drop across the sensing resistor. All the control circuits and power supplies MUST be referred to this point and not to the N terminal. If the circuits are not connected properly, the additional current flowing through the sense resistor might adversely affect the operation of the short-circuit protection function. In general, it is a best practice to make the common reference (V_{SS}) a ground plane in the PCB layout.

The main control power supply is also connected to the bootstrap circuits to generate floating supplies for the high-side gate drivers.

When the control supply voltage (V_{DD} and V_{BS}) falls under the undervoltage lockout level, the IGBTs ignore the input signal and turn off.

Table 15 IM06BxxxC1 functions versus control power-supply voltage

Control voltage range [V]	Effect on functions
0.0 to 12.4	As the UVLO function is activated the control input signals are blocked and a fault signal V_{FO} is generated
12.4 ~ 13.0	The IGBTs will operate according to the control gate input. The driving voltage is below the recommended range, so the $V_{CE(Sat)}$ and the switching losses are larger than under normal conditions. The high-side IGBTs cannot operate after the initial charging of V_{BS} because V_{BS} cannot reach V_{BSUV+}.
13.0 ~ 17.5	Normal operation. This is the recommended operating condition. V_{DD} = 15 V is recommended when only the integrated bootstrap circuitry is used.
17.5 ~ 20.0	IGBTs still operate because the driving voltage is above the recommended range. However, the IGBTs switch faster. This increases the system noise, and the peak short-circuit current might be too large for the short-circuit protection feature to work properly.
Over 20.0	Control circuit in IM06BxxxC1 can get damaged.

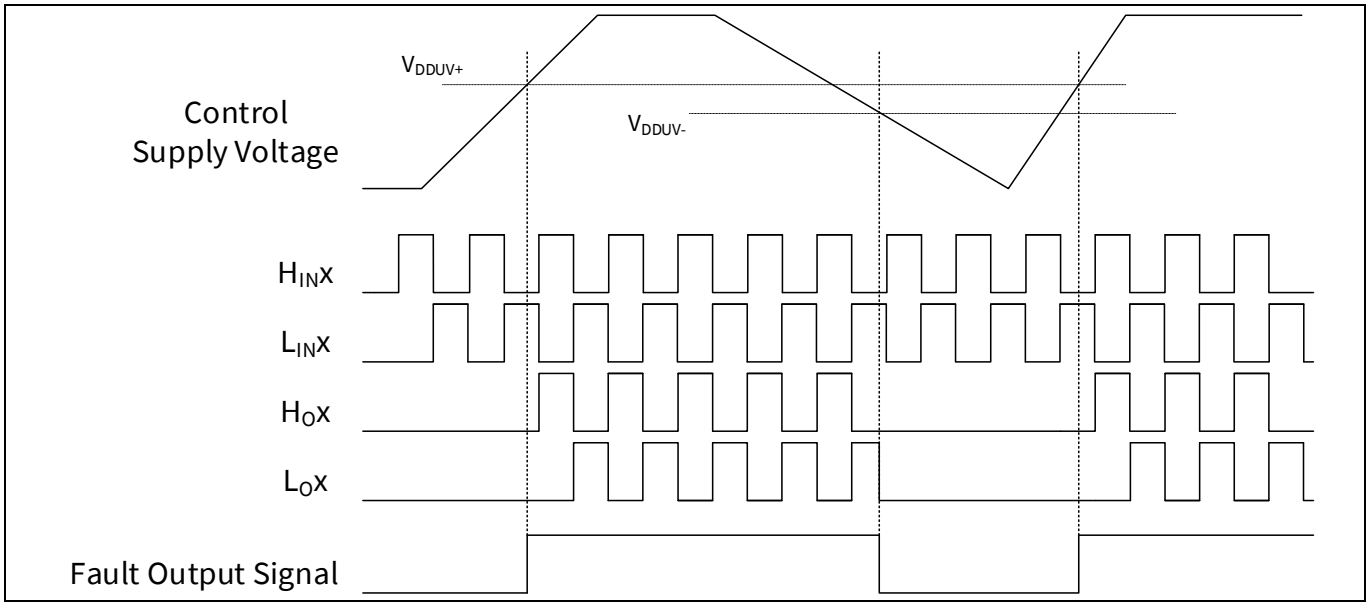


Figure 26 Timing chart of the low side undervoltage protection function

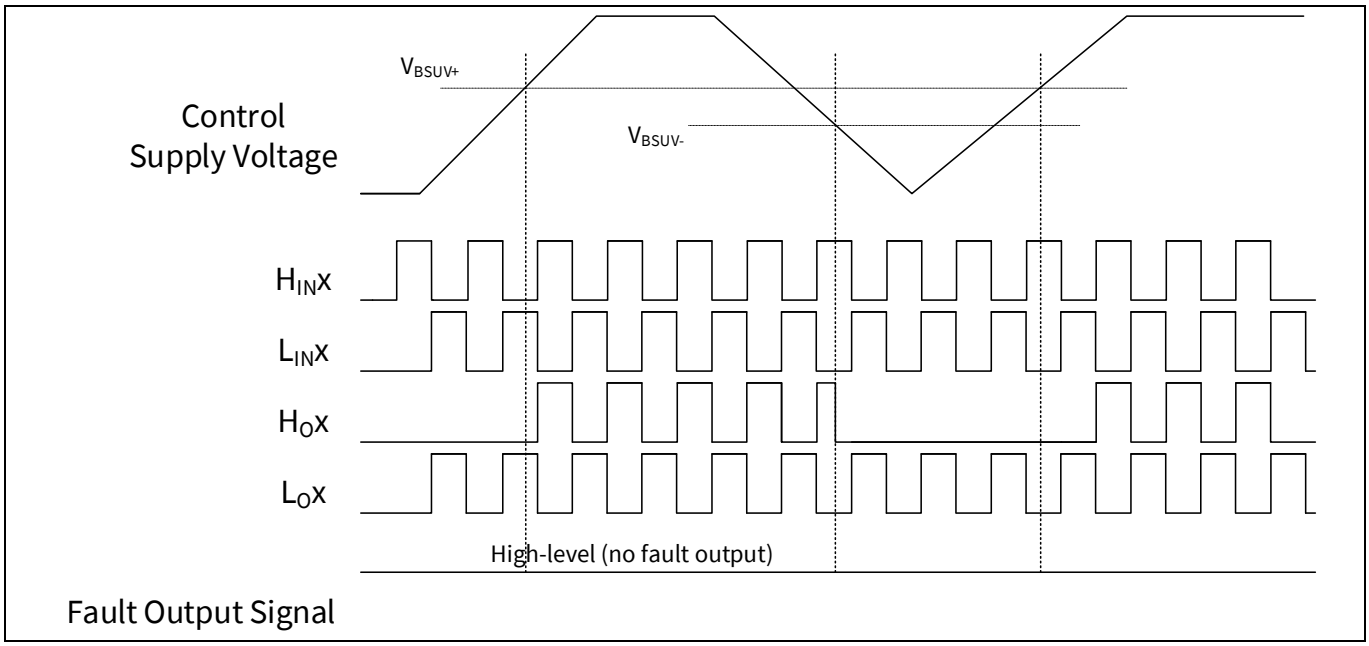


Figure 27 Timing chart of the high side undervoltage protection function

5.2 Overcurrent protection

5.2.1 Timing chart of the overcurrent protection

IM06BxxxC1 has an overcurrent shutdown function. Its internal IC monitors the voltage of the I_{TRIP} pin. If the voltage exceeds the $V_{IT,TH+}$ value specified in the device datasheets, a fault signal is activated and all IGBTs are turned off. Typically, the maximum short-circuit current magnitude is gate-voltage dependent. A higher gate voltage results in a larger short-circuit current. To avoid this problem, the maximum overcurrent trip level is usually set two times below the nominal rated collector current. The timing chart of overcurrent protection is shown in Figure 28.

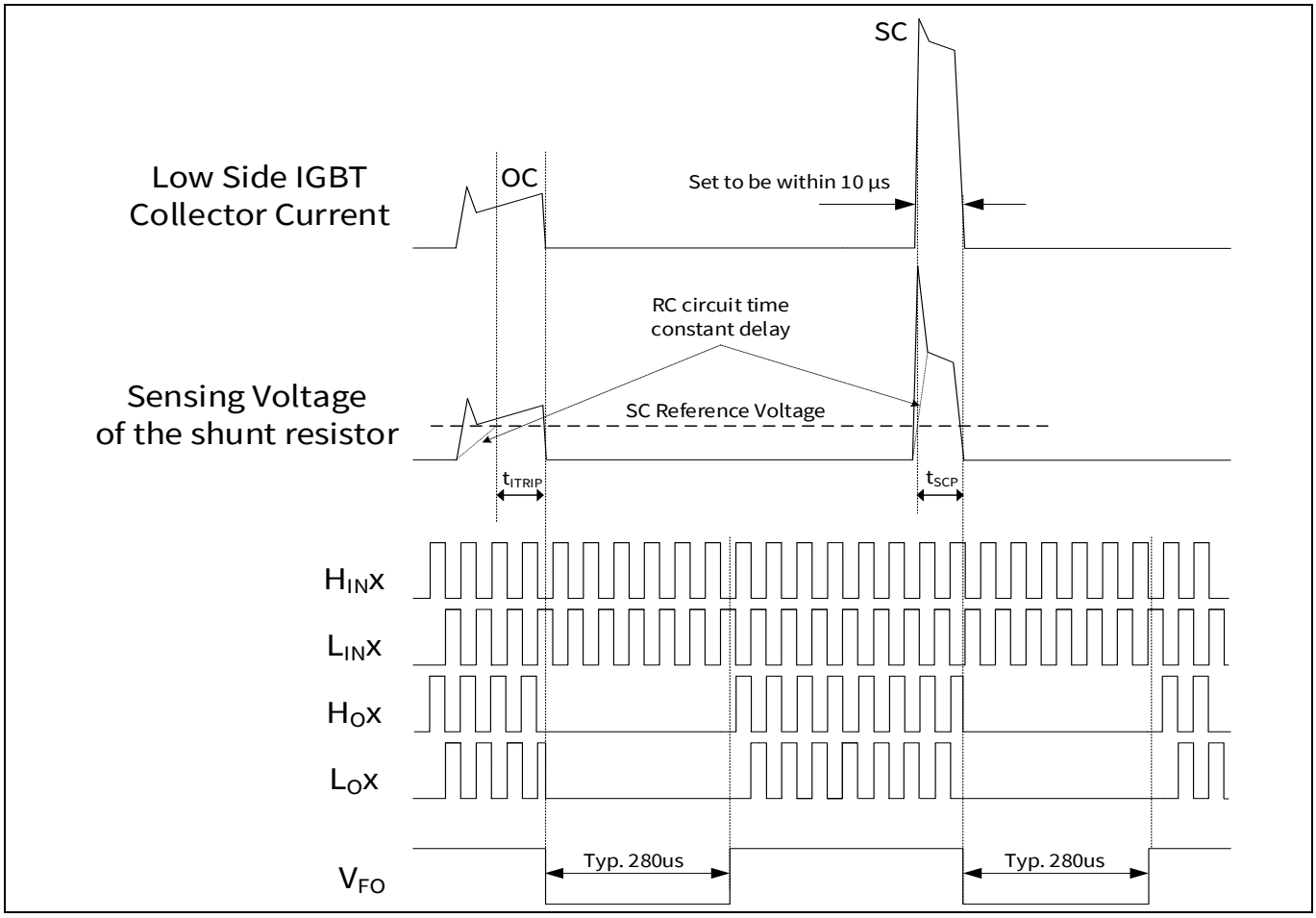


Figure 28 Timing chart of the overcurrent protection function

5.2.2 Selecting a current-sensing shunt resistor

The value of the current sensing resistor is calculated by the following expression:

$$R_{SH} = \frac{V_{IT,TH+}}{I_{OC}} \quad (1)$$

Here, $V_{IT,TH+}$ is the I_{TRIP} positive-going threshold voltage of IM06BxxxC1. It is typically 0.525 V. I_{OC} is the overcurrent detection level.

The maximum value of the overcurrent protection level should be set lower than the repetitive peak collector current in the datasheet. While setting this value, consider the tolerance of the shunt resistor. For example, the maximum peak collector current of IM06B15AC1 is 30 A and thus the recommended value of the shunt resistor can be calculated as:

$$R_{SH(\min)} = \frac{0.525}{30} = 0.0175\ \Omega$$

To set the power rating of the shunt resistor, the following should be considered:

- Maximum load current of inverter (I_{rms})
- Shunt resistor value at T_C = 25°C (R_{SH})
- Power derating ratio of the shunt resistor at T_{SH} = 100°C as per the manufacturer's datasheet
- Safety margin

The shunt resistor's power rating is calculated by the following equation.

$$P_{SH} = \frac{I_{rms}^2 \times R_{SH} \times margin}{derating\ ratio} \quad (2)$$

For example, in the case of IM06B15AC1 where:

- R_{SH} = 17.5 mΩ
- Maximum load current of the inverter: 7 A_{rms}
- Power derating ratio of the shunt resistor at T_{SH} = 100°C: 80%
- Safety margin: 30%

…the power rating can be calculated as follows:

$$P_{SH} = \frac{7^2 \times 0.0175 \times 1.3}{0.80} \approx 1.39\ W$$

A correct power rating of the shunt resistor exceeds 1.39 W, e.g., around 2 W.

Note that an appropriate resistance value and a power rating higher than the minimum value should be chosen considering the overcurrent protection level required for an application.

Based on the previous equations, conditions, and calculation methods, the minimum shunt resistance and resistor power of IM06BxxxC1 products are listed in Table 16.

Table 16 Minimum R_{SH} and P_{SH}

Product	Max. peak current	Min. shunt resistance, R_{SH}	Min. shunt resistor power, P_{SH}
IM06B15AC1	30 A	17.5 mΩ	2.0 W
IM06B20AC1	40 A	13.1 mΩ	3.0 W
IM06B30AC1	60 A	8.75 mΩ	4.0 W

5.2.3 Delay time

The RC filter is necessary in the overcurrent sensing circuit to prevent the overcurrent protection function from malfunctioning due to noise. The RC time constant is determined by considering the noise duration and the capability of the IGBT to withstand the short-circuit time.

When the sensing voltage on the shunt resistor exceeds the I_{TRIP} positive-going threshold ($V_{IT,\,TH+}$), then this voltage is applied to the I_{TRIP} pin of the IPM via the RC filter. Table 17 lists the specification for the overcurrent-protection reference level. The filter delay time (t_{Filter}) until which the input voltage of the I_{TRIP} pin rises to the I_{TRIP} positive threshold voltage is defined by equations (3) and (4).

$$V_{IT,TH+} = R_{SH} \cdot I_C \cdot \left(1 - \frac{1}{e^{\frac{t_{Filter}}{\tau}}}\right) \quad (3)$$

$$t_{Filter} = -\tau \cdot \ln\left(1 - \frac{V_{IT,TH+}}{R_{SH} \cdot I_C}\right) \quad (4)$$

Where, $V_{IT,\,TH+}$ is the I_{TRIP} pin input voltage, I_C is the peak current, R_{SH} is the shunt resistor value, and τ is the RC time constant. In addition, there is a short-circuit propagation delay time of I_{TRIP} (t_{SCP}) which is defined by the propagation delay time from $V_{IT,\,TH+}$ to 10% of I_{SC}. Please refer to Table 18.

Table 17 Specification for overcurrent protection reference level $V_{IT,\,TH+}$

Item	Symbol	Min.	Typ.	Max.	Unit
I_{TRIP} positive-going threshold	$V_{IT,\,TH+}$	0.475	0.525	0.570	V

Table 18 Shutdown propagation delay

Item		Condition	Min.	Typ.	Max.	Unit
Short-circuit propagation delay time (t_{SCP})	IM06BxxxC1	From $V_{IT,TH+}$ to 10% I_{SC}	-	1430	-	ns

Therefore, the total time from I_{TRIP} positive-going threshold ($V_{IT,TH+}$) to the shutdown of the IGBT is:

$$t_{total} = t_{Filter} + t_{SCP} \quad (5)$$

The short-circuit propagation delay can be changed by changing the operating conditions, such as operating temperature and V_{DD}, V_{DC}. The total delay must be less than 3 µs of the short-circuit withstand time (t_{SC}) given in the datasheet.

5.3 Fault-output circuit

Table 19 Fault-output maximum ratings

Item	Symbol	Condition	Value	Unit
Fault-output supply voltage	V_{FO}	Applied between V_{FO} and V_{SS}	-0.5 V~V_{DD} +0.5	V
Fault-output current	I_{FO}	Sink current at the V_{FO} pin	10	mA

Table 20 Electric characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Fault-output voltage	V_{FO}	I_{FO} = 10 mA, V_{ITRIP} = 1 V	-	0.35	-	V
Fault-output current	I_{FO}	V_{ITRIP} = 0 V, V_{FO} = 5 V	-	60	-	uA

As V_{FO} uses an open-drain type, it must be pulled up to a high level using a pull-up resistor. The resistor has to be calculated according to the abovementioned specifications.

5.4 Sleep function

The sleep function is activated after each trigger of I_{TRIP} or undervoltage lockout. A new edge of each individual control signals $L_{IN}x$ and $H_{IN}x$ is mandatory for activating the outputs $L_O x$ or $H_O x$ after the V_{FO} signal is released. Figure 29 shows a description of the timing diagram.

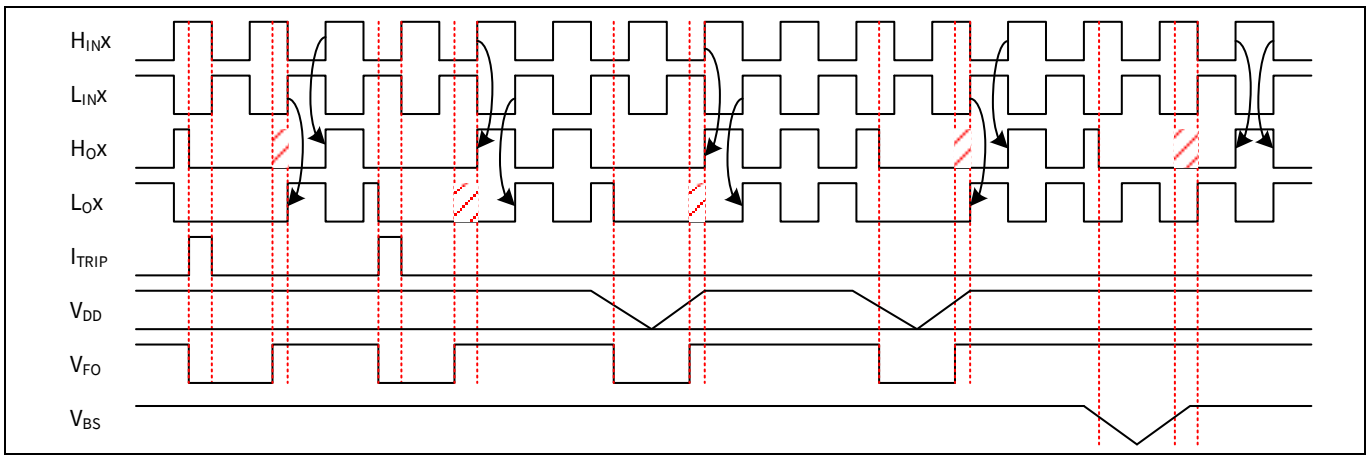


Figure 29 Sleep-function timing diagram I_{TRIP} and UVLO

5.5 Temperature monitoring and thermal protection

IM06BxxxC1 has one pin for both fault output and temperature sensing. The built-in thermistor is directly connected to the V_{SS} internally. The typical application circuit looks like Figure 31. An external pull-up resistor connected to V_{ctr} ensures that the resulting voltage can be directly connected to the MCU.

Figure 32 shows the thermistor voltage according to temperature at a pull-up resistor of 3.6 kΩ when the control voltage is 5 V and 3.3 V. V_{FO} voltage becomes 3.0 V and 1.95 V respectively for 5 V and 3.3 V when the thermistor temperature is 100 °C.

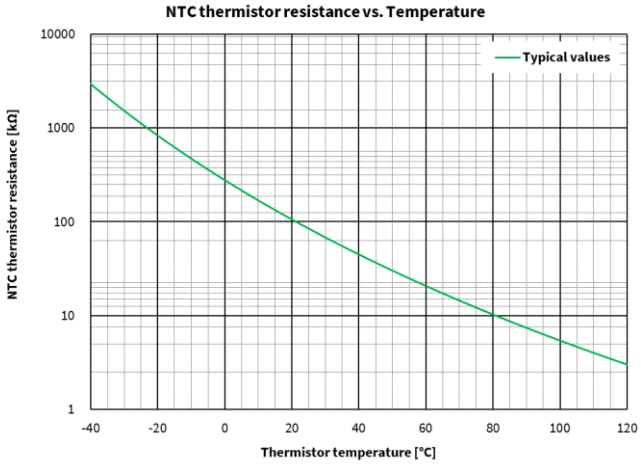


Figure 30 Internal thermistor resistance characteristics as a function of the thermistor's temperature

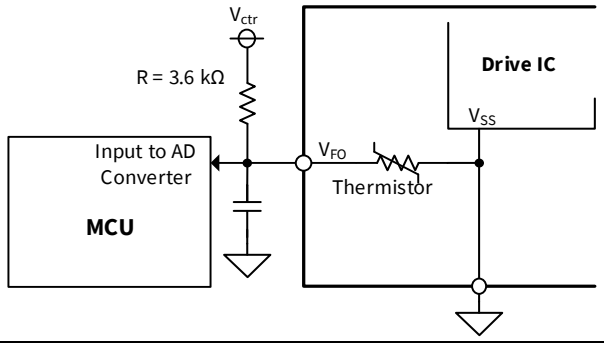


Figure 31 Circuit proposals for overtemperature protection

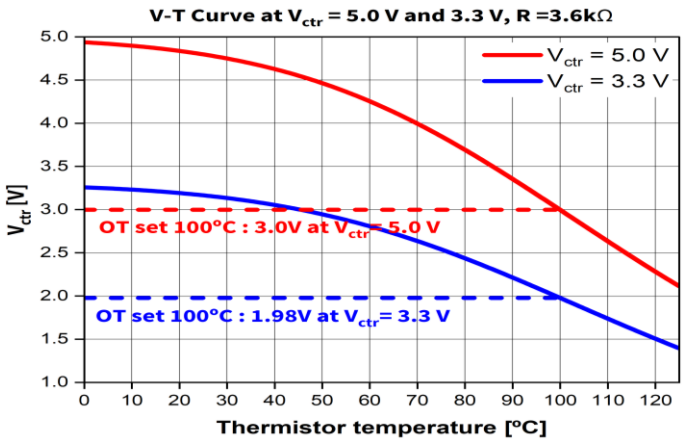
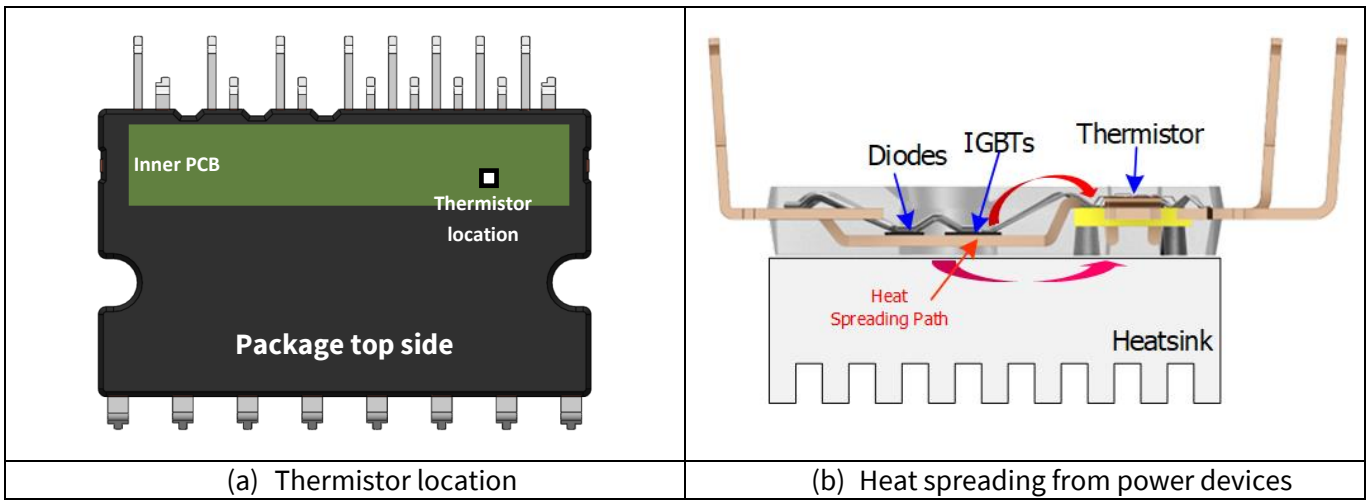


Figure 32 Voltage of V_{FO} pin according to the thermistor temperature

The NTC thermistor is located on the inner PCB of the IPM as shown in Figure 33(a). So, the temperature of the thermistor does not reflect on the power chip's temperature directly. When the IPM is operated, the heat of power devices is transferred to the thermistor through the heat sink and the package as seen in Figure 33(b).

Figure 34 shows the relationship between $T_{J\,(avg.)}$ (the average junction temperature of the IGBT), T_C (the case temperature of the IPM), and T_{NTC} (temperature of the thermistor) under conditions specified. However, this relationship is just one of examples. This relationship also depends on system conditions such as the size of the heatsink, the cooling system used, the control scheme, and so on. To know the relationship between $T_{J\,(avg.)}$, T_C, and T_{NTC} on their systems, users should themselves define the relationship for their systems.



(a) Thermistor location | (b) Heat spreading from power devices

Figure 33 Thermistor location and heat spreading from power devices

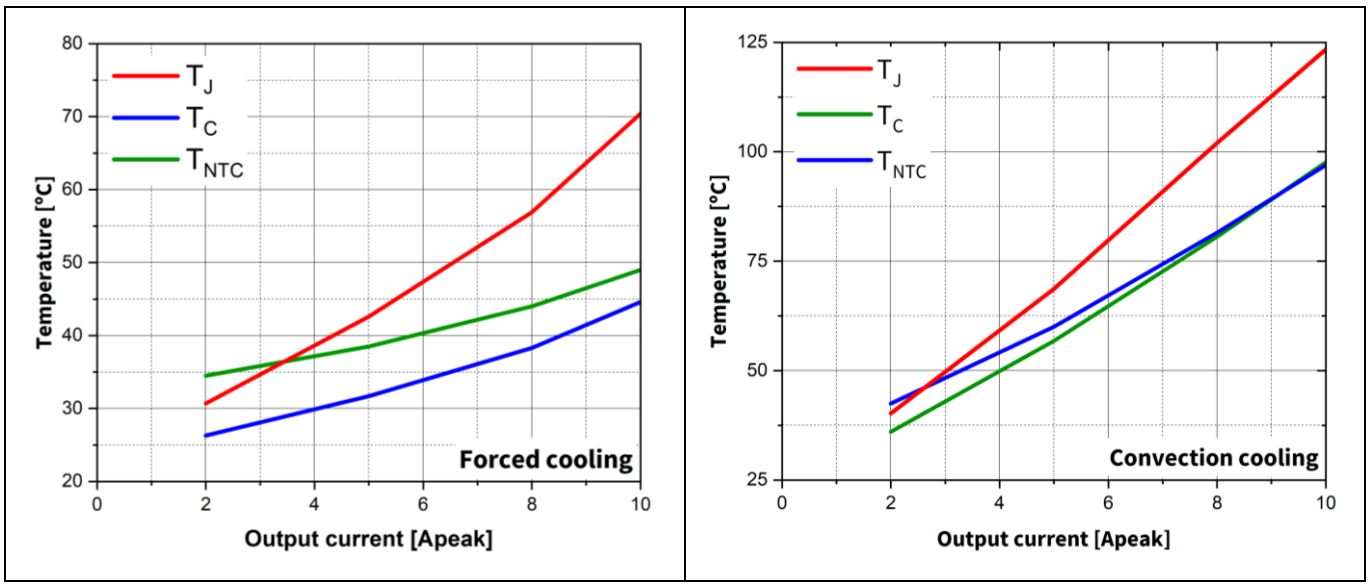


Figure 34 Example of the relationship between T_J, T_C, and T_{NTC} (Test conditions: V_{DC} = 340 V, V_{DD} = 15 V, I_O = 2 ~ 10 A_{peak}, F_{SW} = 6 kHz, F_O = 60 Hz, SVPWM. DUT is IM06B15AC1. Forced and convection cooling conditions. T_J is measured by an infrared camera. For the T_C measurement point, refer to Figure 5

6 Bootstrap circuit

6.1 Bootstrap circuit operation

The V_{BS} voltage, which is the voltage difference between V_B (U, V, W) and V_S (U, V, W), provides the supply to the high-side gate driver IC within IM06BxxxC1. The recommended range for this supply voltage (V_{BS}) is 13.0 ~ 18.5 V to ensure that the gate driver IC can fully drive the high-side IGBT. IM06BxxxC1 includes an undervoltage detection function for the V_{BS} to ensure that the IC does not drive the high-side IGBT if the V_{BS} drops below the voltage specified in its datasheet. This function prevents the IGBT from operating in a high dissipation mode. Please note that the undervoltage lockout function of any high-side section acts only on the triggered channel without any feedback to the control level.

There are several ways in which the V_{BS} floating supply can be generated. One of them is the bootstrap method described in this chapter. This method has the advantage of being simple and cheap. However, the duty cycle and on-time are limited by the requirement to refresh the charge in the bootstrap capacitor. The bootstrap supply is formed by a combination of a diode (D_{BS}), a resistor (R_{BS}), and a capacitor (C_{BS}) as shown in Figure 36 (a). The current flow path of the bootstrap circuit is shown in Figure 36 (a). When V_S is pulled down to the ground (either through the low side or the load), the bootstrap capacitor (C_{BS}) is charged through the bootstrap diode (D_{BS}) and the resistor (R_{BS}) from the V_{DD} supply.

6.2 Internal bootstrap functionality characteristics

IM06BxxxC1 includes three bootstrap functionalities in the internal gate driver IC, which consist of three diodes and three resistors, as shown in Figure 4. The typical value of an internal bootstrap resistor is 37 Ω at room temperature. For more information, please refer to Figure 35 and Table 21.

A V_{DD} of 15 V is recommended when only the integrated bootstrap circuitry is used.

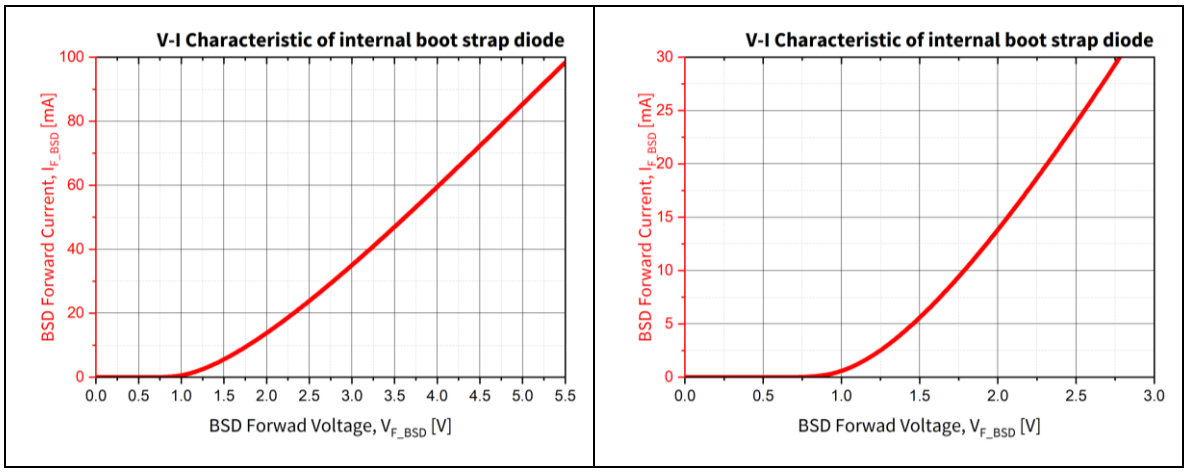


Figure 35 Internal bootstrap diode I_F - V_F characteristics

Table 21 Electrical characteristics of internal bootstrap parameters

Description	Condition	Symbol	Value			Unit
			Min.	Typ.	Max.	
Repetitive peak reverse voltage		V_{RRM}	600	-	-	V
Diode resistance	Between V_F = 4 V and V_F = 5 V	R_{BSD}	-	37	-	Ω
Diode's forward voltage	I_F = 0.3 mA	$V_{F, BSD}$	-	1.0	-	V

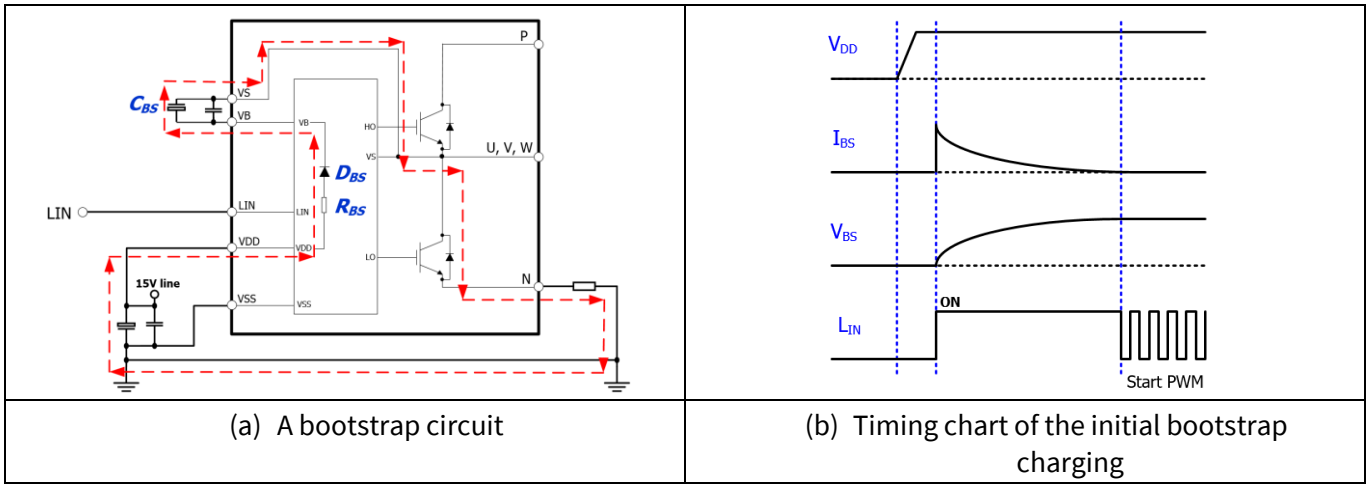
6.3 Initial charging of a bootstrap capacitor

For initial bootstrap charging, and adequate on-time duration of the low-side IGBT is required to charge the bootstrap capacitor fully. The initial charging time (t_{charge}) can be calculated from the following equation:

$$t_{charge} \geq C_{BS} \times R_{BS} \times \frac{1}{\delta} \times \ln\left(\frac{V_{DD}}{V_{DD} - V_{BS(min)} - V_{FD} - V_{LS}}\right) \quad (5)$$

- V_{FD} = Forward-voltage drop across the bootstrap diode
- $V_{BS(min)}$ = The minimum value of the bootstrap capacitor voltage
- V_{LS} = Voltage drop across the low-side IGBT
- δ = Duty ratio of the PWM

Initial charging needs to be performed until the value of V_{BS} (voltage of C_{BS}) exceeds the recommended minimum bootstrap voltage ($V_{BS\,(min)}$) of 13.0 V. Charging as much as possible is recommended considering the voltage drop between the end of charging and the beginning of inverter operation.



(a) A bootstrap circuit

(b) Timing chart of the initial bootstrap charging

Figure 36 Bootstrap circuit operation and initial changing

6.4 Bootstrap circuit design

When designing the IM06BxxxC1 series for bootstrap circuit, it is necessary to consider various conditions such as temperature characteristics, change by lifetime variation, and so on. Notes for designing these devices are provided in the following sections. For detailed information about driving via a bootstrap circuit, please refer to the application note, AN2020-14, “Bootstrap circuit design for CIPOS™ IPM series” [4].

6.4.1 Bootstrap capacitor

Electrolytic capacitors are generally used for C_{BS}. Nowadays, multilayer ceramic capacitors (MLCC) with large capacitance are also being used. However, the DC bias characteristics of the MLCC when applying DC voltage are considerably different from that of the electrolytic capacitor, especially the large capacitance type. Some differences in the capacitance characteristics of the electrolytic and ceramic capacitors are listed in Table 22.

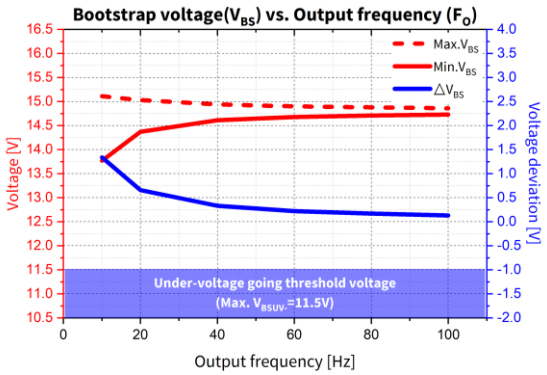
Table 22 Difference in capacitance characteristics of electrolytic and ceramic capacitors

Item	Electrolytic capacitor	MLCC
Temperature characteristics (T_A: -20 ~ 85°C)	- Aluminum type: Low temp.: -10%, High temp.: +10% - Conductive polymer aluminum solid type: Low temp.: -5% High temp.: +10%	Difference due to temperature characteristics: Low temp.: -5% ~ 0% High temp.: -5% ~ -10% (with X5R, X7R)
DC bias characteristics (applying DC 15 V)	Nothing within the rating voltage	Difference due to temperature characteristics, rating voltage, package size and so on -50% ~ -15% (with X7R, 50 V_{DC} rating)

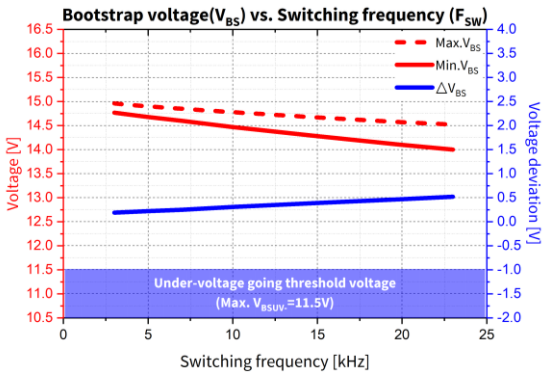
6.4.2 Bootstrap voltage variance under inverter operating conditions

When a bootstrap circuit is designed, the bootstrap voltage (V_{BS}) variance needs to be considered with respect to the inverter operating conditions, such as output current and frequency, switching frequency, modulation scheme, voltage ripple of V_{BS}, and so on. A lower bootstrap voltage can lead to high dissipation of the high-side IGBT or trigger the undervoltage lockout (UVLO) protection mode. Figure 37 shows sample trends of the variance in bootstrap voltage under given conditions based on simulation.

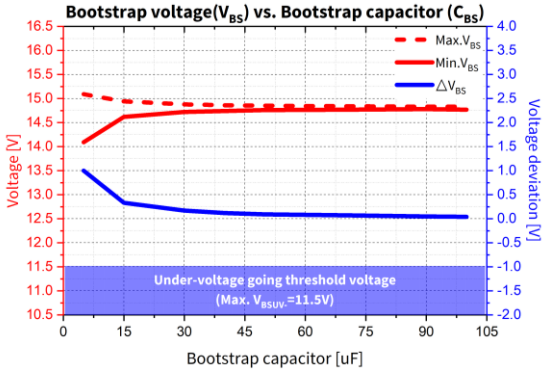
Conditions: IM06B15AC1, V_{DC} = 340 V, V_{DD} = 15 V, I_O = 10 A_{peak}, SVPWM, ΔV_{BS} < 2.0 V, T_C = 25°C, R_{SH} = 20 mΩ, MI = 0.8, PF = 0.9, (a) C_{BS} = 22 µF, F_{SW} = 5 kHz, (b) C_{BS} = 22 µF, F_O = 60 Hz, (c) F_{SW} = 5 kHz, F_O = 60 Hz.



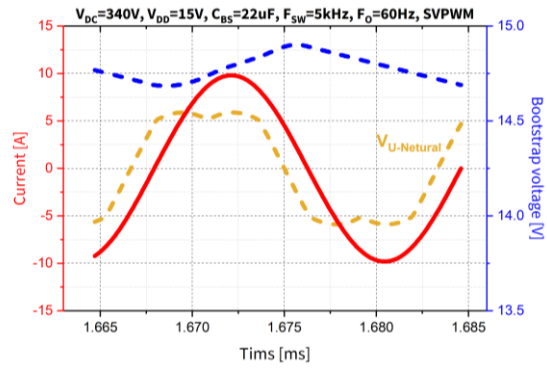
(a) Bootstrap voltage vs. output current frequency



(b) Bootstrap voltage vs. switching frequency



(c) Bootstrap voltage vs. bootstrap capacitance



(d) Example waveform

Figure 37 Variance in bootstrap voltage (V_{BS}) under inverter operating conditions

According to Figure 37, except the bootstrap capacitance (C_{BS}), the main operating conditions affecting the bootstrap voltage (V_{BS}) are:

- Output current frequency, f_O
- Switching frequency, f_{SW}

Note that these results are only examples. It is necessary to consider enough data and evaluation at the system design level because the bootstrap voltage is also affected by other operating conditions such as the PWM scheme (e.g., discontinuous PWM), power factor, modulation index, power switches (IGBT and MOSFET), and so on.

7 Thermal system design

7.1 Introduction

The system's thermal design is an important consideration for IM06BxxxC1 which is included in electronic systems such as drives. To avoid overheating and/or to increase reliability, two design criteria are important:

- Low power losses
- Low thermal resistance from junction to ambient

The first criterion is already fulfilled when IM06BxxxC1 is chosen as the intelligent power module in an application. To get the most out of the system, choosing the correct heatsink is necessary. A good thermal design either allows the maximization of power or increases the reliability of the system (by reducing the maximum temperature). This chapter provides a short introduction to power losses and heatsinks that will help in understanding the mode of operation and finding the right heatsink for an application.

Requirements for the thermal design:

- The maximum power losses ($P_{sw,i}$) of each power switch
- The maximum junction temperature ($T_{J,max}$) of the power semiconductors
- The junction-to-ambient thermal resistance impedance ($Z_{th,J\text{-}A}$). For stationary considerations, the static thermal resistance ($R_{th,J\text{-}A}$) is sufficient. This thermal resistance comprises:
    - The junction-to-case thermal resistance ($R_{th,J\text{-}C}$), as given in the datasheets
    - The case-to-heatsink thermal resistance ($R_{th,C\text{-}HS}$) that accounts for the heat flow through the thermal interface material between the heatsink and the power module
    - The heatsink-to-ambient thermal resistance ($R_{th,HS\text{-}A}$).

  Each of these thermal resistances can be extended to their corresponding thermal impedance by adding thermal capacitances.
- The maximum allowable ambient temperature ($T_{A,max}$)

Furthermore, all heat flow paths need to be identified. Figure 38 presents a typical simplified equivalent circuit for the thermal network. This circuit is simplified, as it omits the thermal capacitances and the typically negligible heat paths such as the heat transfer from the module's surface directly to the ambient through convection and radiation.

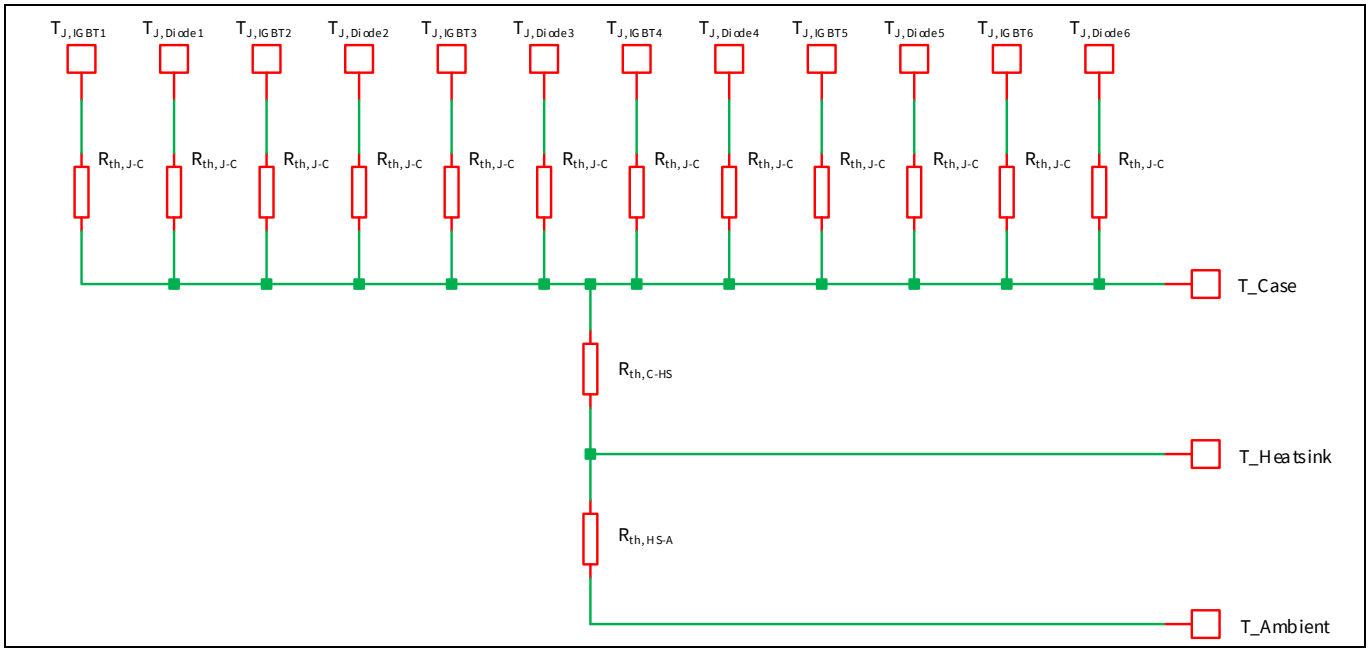


Figure 38 Simplified thermal equivalent circuit

7.2 Power loss

The total power losses in IM06BxxxC1 are composed of conduction and switching losses in the IGBTs and diodes. The loss during the turn-off steady state can be ignored because it is very small and has little effect on increasing the device temperature. The conduction loss depends on the DC-electrical characteristics of the device, i.e., saturation voltage. Therefore, it is a function of the conduction current and the device's junction temperature. On the other hand, the switching loss is determined by dynamic characteristics such as turn-on and turn-off time and overvoltage/overcurrent. Hence, to obtain the accurate switching loss, the DC-link voltage of the system, the applied switching frequency, and the layout of the power circuit layout should be considered in addition to current and temperature. In this section, based on a PWM inverter system for motor-control applications, detailed equations are shown for calculating both losses for IM06BxxxC1 in a three-phase continuous sinusoidal PWM.
For other cases, such as three-phase discontinuous PWMs, please refer to [5].

7.2.1 Conduction losses

The typical characteristics of forward-drop voltage can be approximated by the following linear equations for the IGBT and the diode, respectively.

$$V_{\mathrm{IGBT}} = V_I + R_I \cdot i \tag{6}$$

$$V_{\mathrm{DIODE}} = V_D + R_D \cdot i \tag{7}$$

- V_I = Threshold voltage of the IGBT
- V_D = Threshold voltage of the anti-parallel diode
- R_I = On-state slope resistance of the IGBT
- R_D = On-state slope resistance of the anti-parallel diode

If the switching frequency is high, the output current of the PWM inverter can be assumed to be sinusoidal. That is:

$$i = I_{\text{peak}}\cos(\theta - \varphi) \quad (8)$$

Here φ is the phase angle difference between the output voltage and the current. Using equations (6), (7), and (8), the conduction loss of one IGBT and its anti-parallel diode can be obtained as follows:

$$P_{\text{con.I}} = \frac{1}{2\pi}\int_0^{\pi} \xi(V_{\text{IGBT}} \times i)\mathrm{d}\theta = \frac{I_{\text{peak}}}{2\pi}V_I + \frac{I_{\text{peak}}}{8}V_I \text{MIcos}\phi + \frac{{I_{\text{peak}}}^2}{8}R_I + \frac{{I_{\text{peak}}}^2}{3\pi}R_I \text{MIcos}\phi \quad (9)$$

$$P_{\text{con.D}} = \frac{1}{2\pi}\int_0^{\pi} (1-\xi)(V_{\text{DIODE}} \times i)\mathrm{d}\theta = \frac{I_{\text{peak}}}{2\pi}V_D - \frac{I_{\text{peak}}}{8}V_D \text{MIcos}\phi + \frac{{I_{\text{peak}}}^2}{8}R_D - \frac{{I_{\text{peak}}}^2}{3\pi}R_D \text{MIcos}\phi \quad (10)$$

$$P_{\text{con}} = P_{\text{con.I}} + P_{\text{con.D}} \quad (11)$$

Here ξ is the duty cycle in the given PWM method.

$$\xi = \frac{1+\text{MIcos}\theta}{2} \quad (12)$$

Here, MI is the PWM modulation index (MI). It is defined as the peak phase voltage divided by half the DC-link voltage. Note that the inverter's total conduction losses are six times the value of P_{con}.

7.2.2 Switching losses

Different devices have different switching characteristics, which also vary according to the handled voltage/current and the operating temperature/frequency. However, the turn-on/turn-off energy loss (in joules) can be experimentally measured indirectly by multiplying the current and voltage and integrating it over time, under a given circumstance. Therefore, the linear dependency of the switching energy loss on the switched current during one switching period is expressed as follows:

$$\text{Swtitching energy loss} = (E_I + E_D) \times \text{i [joule]} \quad (13)$$

$$E_I = E_{\text{I.ON}} + E_{\text{I.OFF}} \quad (14)$$

$$E_D = E_{\text{D.ON}} + E_{\text{D.OFF}} \quad (15)$$

Here E_I i is the switching energy loss of the IGBT and E_D i is the switching energy loss for its monolithic body diode. E_I and E_D can be, approximately, considered a constant.

As mentioned in the equation (8), the output current can be considered a sinusoidal waveform. The switching loss occurs every PWM period in continuous PWM schemes. Therefore, depending on the switching frequency (f_{SW}), the switching loss of one device is represented by the following equation (16):

$$P_{\text{sw}} = \frac{1}{2\pi}\int_0^{\pi} (E_I + E_D)\cdot i \cdot f_{\text{sw}}\mathrm{d}\phi = \frac{(E_I+E_D)\cdot f_{\text{sw}}\cdot I_{\text{peak}}}{\pi} \quad (16)$$

Here, E_I is a unique constant of the IGBT related to the switching energy; different IGBTs have different E_I values. E_D is one for diode. These should be derived from experimental measurement. From equation (16), the switching losses are a linear function of current and directly proportional to the switching frequency.

7.3 Thermal impedance

In practical operation, the power loss (P_D) is cyclic and therefore the transient impedance needs to be considered. The thermal impedance is typically represented by an RC equivalent circuit (Foster model) shown in Figure 39. For pulsed power loss, the thermal capacitance effect delays the rise in the junction temperature and thus permits a heavier loading of IM06BxxxC1. Figure 40 shows thermal impedance from the junction-to-case curves of IM06B15AC1, IM06B20AC1, IM06B30AC1 and IM06B50GC1. The thermal resistance values listed in Table 23 enter saturation in about 10 seconds. Other kinds of IM06BxxxC1 also show similar characteristics.

Table 23 Thermal resistance of IM06BxxxC1 products

Description	Symbol	Condition		Value			Unit
				Min.	Typ.	Max.	
Single IGBT thermal resistance, junction to case	R_{thJC}	Low-side U-phase IGBT (See Figure 5 for the T_C measurement point)	IM06B15AC1	-	-	4.1	K/W
			IM06B20AC1			3.9	
			IM06B30AC1			3.7	
			IM06B50GC1			0.6	
Single diode thermal resistance, junction to case	$R_{thJC,D}$	Low-side U-phase diode (See Figure 5 for the T_C measurement point)	IM06B15AC1	-	-	5.4	K/W
			IM06B20AC1			5.0	
			IM06B30AC1			4.6	
			IM06B50GC1			1.0	

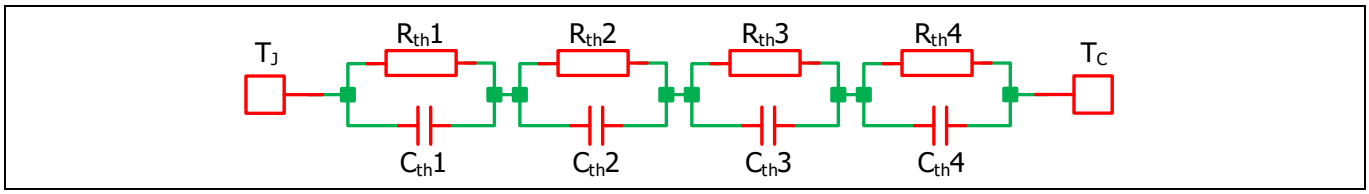
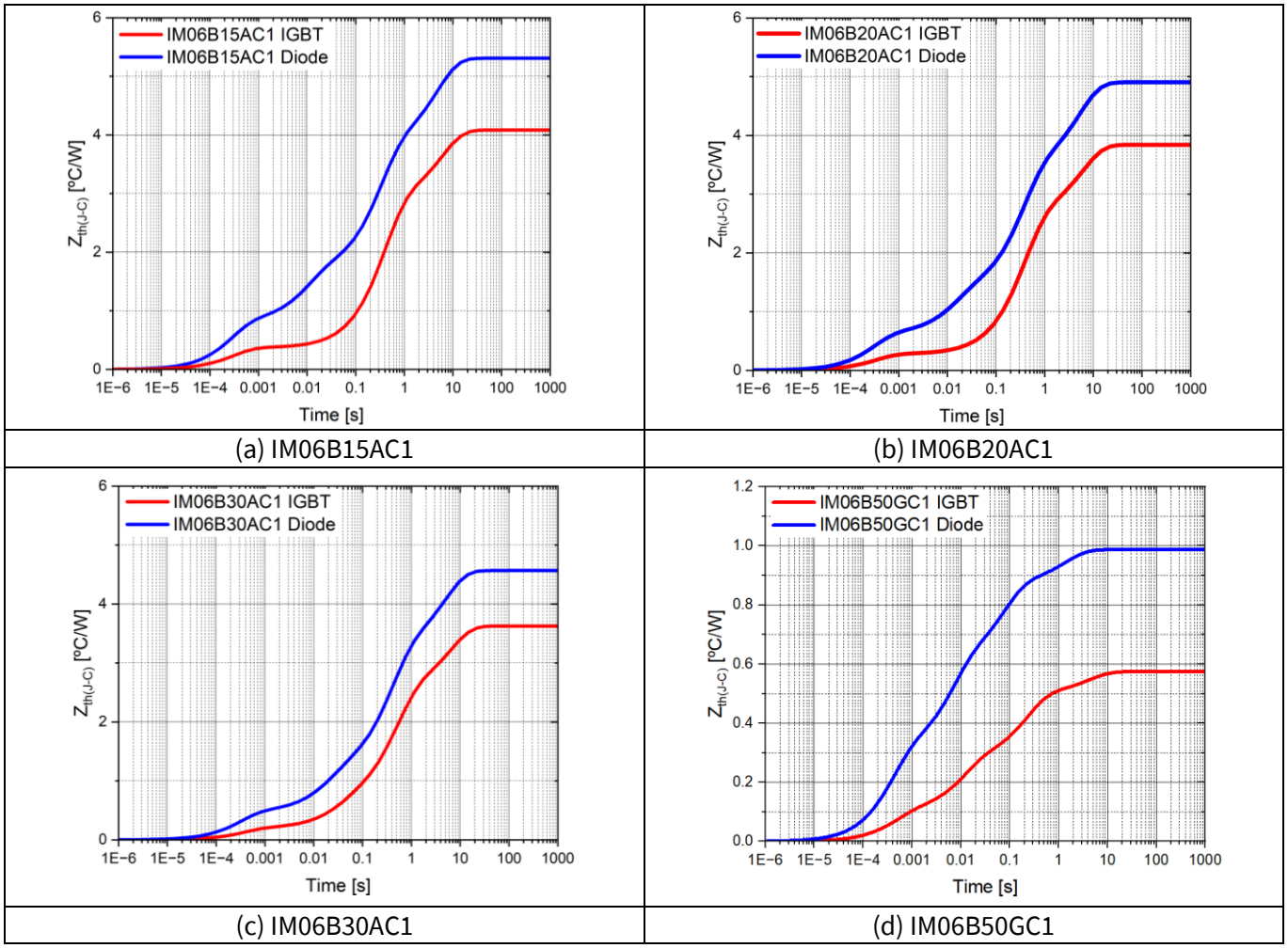


Figure 39 Thermal impedance RC equivalent circuit (Foster model)



(a) IM06B15AC1 (b) IM06B20AC1

(c) IM06B30AC1 (d) IM06B50GC1

Figure 40 Thermal impedance curves of the IM06BxxxC1 series (based on single-chip heating)

7.4 Factors for the temperature rise and sample calculations

Infineon IPOSIM [6] is an online power simulation program for calculating loss and thermal performance of Infineon power modules and discrete devices. It helps in selecting the right product for any given application topology, simulating the switching and conduction losses. The result includes an assessment of the thermal performance based on your given cooling conditions and a comparison between the performances of various products and input specifications. IPOSIM offers over 25 topologies to choose from, clustered by power conversion type. IPM was selected from the inverter topology. The results of loss and temperature calculations using representative characteristics provide simulations for various IPM product families.

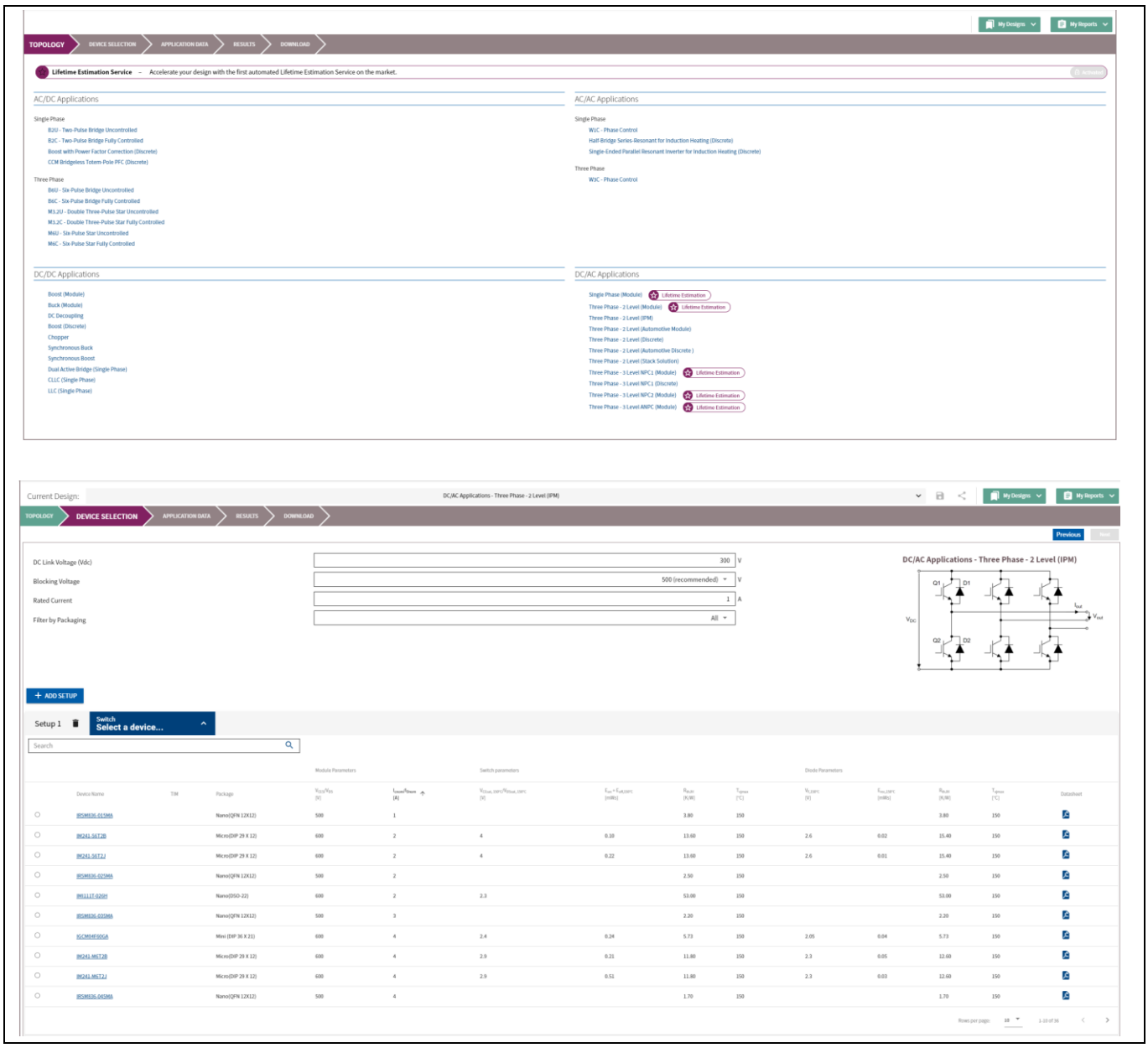


Figure 41 IPOSIM simulation for CIPOS™ IPM [6]

7.5 Heatsink selection guide

7.5.1 Required heatsink performance

If the power losses P_{swi}, $R_{th(J-C)}$ and the maximum ambient temperature are known, the required thermal resistance of the heatsink and the thermal interface material can be calculated based on Figure 39 from:

$$T_{\mathrm{J,max}} = T_{\mathrm{A,max}} + \sum_i P_{\mathrm{sw,i}} \cdot R_{\mathrm{th,HS-}A} + \sum_i P_{\mathrm{sw,i}} \cdot R_{\mathrm{th,C-HS}} + \mathrm{Max}(P_{\mathrm{sw,i}} \cdot R_{\mathrm{th,JC,i}}) \quad (17)$$

For three-phase bridges, it can be assumed that all power switches dissipate the same power and all have the same $R_{th,J-C}$. This gives the required case-to-ambient thermal resistance.

$$R_{\mathrm{th,C-}A} = R_{\mathrm{th,C-HS}} + R_{\mathrm{th,HS-}A} = \frac{T_{\mathrm{J,max}} - P_{\mathrm{sw}} \cdot R_{\mathrm{th,JC}} - T_{\mathrm{A,max}}}{\sum P_{\mathrm{sw}}} \quad (18)$$

For example, the power switches of a washing machine drive dissipate a maximum of 3.5 W power each. If the maximum ambient temperature is 50°C, the maximum junction temperature is 150°C, and the $R_{th(J-C)}$ is 3 K/W. It results in:

$$R_{\mathrm{th,C-}A} \leq \frac{150°C - 3.5\mathrm{W} \cdot 3\frac{K}{W} - 50°C}{6 \cdot 3.5\mathrm{W}} = 4.3\frac{K}{W}$$

If the heatsink temperature shall be limited to 100°C, an even lower thermal resistance is required:

$$R_{\mathrm{th,C-}A} \leq \frac{100°C - 50°C}{6 \cdot 3.5\mathrm{W}} = 2.4\frac{K}{W}$$

Smaller heatsinks with higher thermal resistance may be acceptable if the maximum power is only required for a short duration (below the time constant of the thermal resistance and the thermal capacitance). However, this requires a detailed analysis of the transient power and the temperature profiles. The larger the heatsink, the larger the thermal capacitance and the longer it takes to heat up the heatsink.

7.5.2 Heatsink characteristics

Heatsinks are characterized by three parameters:

- Heat transfer from the power source to the heatsink
- Heat transfer within the heatsink (to all the surfaces of the heatsink)
- Heat transfer from the heatsink surfaces to ambient

7.5.2.1 Heat transfer from the heat source to the heatsink

There are two factors that need to be considered to provide a good thermal contact between the power source and the heatsink:

- **Flatness of the contact area**

  Due to the unevenness of surfaces, a thermal interface material needs to be supplied between the heat source and the heatsink. Such materials usually have a rather low thermal conductivity (< 10 K/W); hence they should be as thin as possible. But they also need to fill out the space between the heat source and the heatsink, so the unevenness of the heatsink should be as less as possible. In addition, the particle size of the interface material must fit into the grooves of the module and the heatsink surfaces. Particles that are too large will unnecessarily increase the thickness of the interface layer and hence increase the thermal resistance. Particles that are too small will not provide a good contact between the two surfaces and it will also lead to a higher thermal resistance.
- **Mounting pressure**

  The higher the mounting pressure, the better the interface material disperses. Also, excessive interface material is squeezed out, resulting in a thinner interface layer with a lower thermal resistance.

7.5.2.2 Heat transfer within the heatsink

The heat transfer within the heatsink is mainly determined by:

- **Heatsink material**

  The material of the heatsink should be a good thermal conductor. Most heatsinks are made of aluminum (λ ≈ 200 W/(m*K)). Copper is heavier and more expensive but also nearly twice as efficient (λ ≈ 400 W/(m*K)).
- **Fin thickness**

  If the fins are too thin, the thermal resistance from the heat source to the fin is too high and the efficiency of the fin decreases. Hence, it does not make sense to make the fins as thin as possible to make more fins and therefore increase the surface area.

7.5.2.3 Heat transfer from the heatsink surface to the ambient

Heat transfers to the ambient mainly by convection. The corresponding thermal resistance is defined as:

$$R_{\mathrm{th,conv}} = \frac{1}{\alpha \cdot A} \tag{19}$$

Here, α is the heat-transfer coefficient and A is the surface area.

Hence there are two important parameters:

- **Surface area**

  Heatsinks require a huge surface area to transfer heat to the ambient easily. The heat source is assumed to be concentrated at one point and not uniformly distributed. Therefore, the total thermal resistance of the heatsink does not change linearly with length. Also, increasing the surface area by increasing the number of fins does not necessarily reduce the thermal resistance as discussed in section 7.5.2.2.
- **Heat transfer coefficient (aerodynamics)**

  This coefficient depends strongly on the air flow velocity as shown in Figure 42. If there is no externally induced flow, it means natural convection. Otherwise, it is forced convection. Heatsinks with very small fin spacing do not allow for a good air flow. If a fan is used, the fin gap may be lower than required for natural convection because the fan forces the air through the space between the fins.

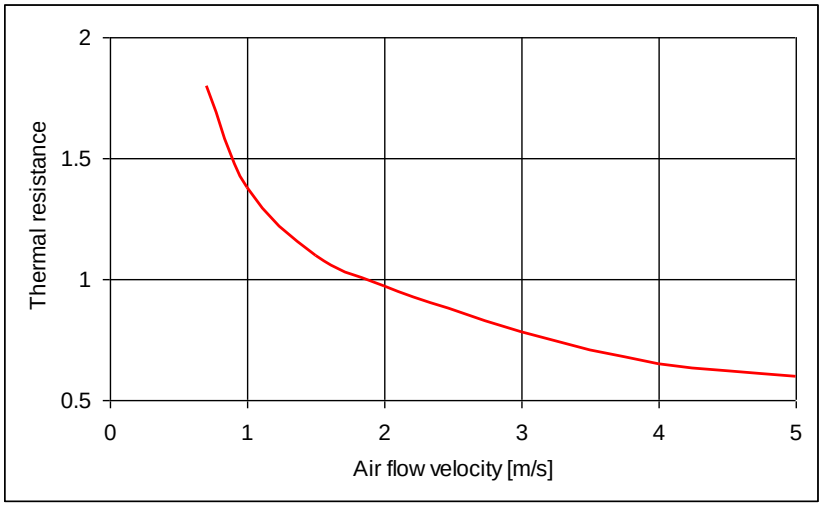


Figure 42 Thermal resistance as a function of the air flow velocity

Furthermore, in the case of natural convection, the efficiency of the heatsink depends on the temperature difference between the heatsink and ambient, i.e., on the dissipated power. Some manufacturers, such as Aavid Thermalloy, provide a correction table that allows users to calculate the thermal resistance depending on the temperature difference. Figure 43 shows the degradation in the heatsink's efficiency due to natural convection, based on [7]. Please note that the thermal resistance is 25% higher at 30 W than at 75 W.

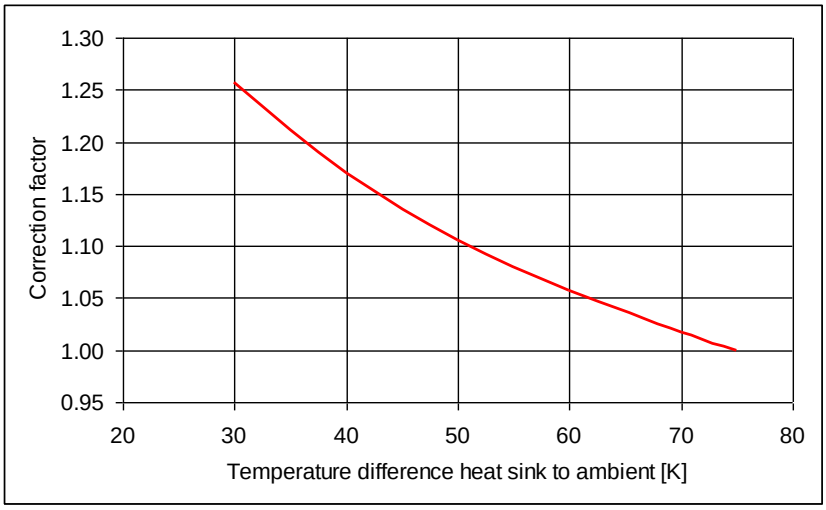


Figure 43 Correction factors for the temperature

The positioning of the heatsink also plays an important role in the aerodynamics. In the case of natural convection, the best mounting is done with vertical fins, as the heated air tends to move upwards due to buoyancy. It should also be ensured that there are no significant obstructions impeding the air flow.

Radiation also supports the transfer of heat from the heatsink to the ambient. To increase radiated heat, anodized heatsinks with a black surface can be used. However, this decreases the thermal resistance of the heatsink only by a few percentage points in the case of natural convection. Radiated heat is negligible in the case of forced convection. Hence, blank heatsinks can be used if no fan is used with the heatsink.

The discussions so far clearly show that a single thermal resistance value cannot be assigned to any heatsink.

7.5.3 Selecting a heatsink

Unfortunately, there are no straightforward formulas for selecting heatsinks. Finding an appropriate heatsink is an iterative process of choosing and testing heatsinks. To get a first rough estimate of the required volume of the heatsink, start with the estimated volumetric thermal resistances given in Table 24 (taken from [8]). This table provides only the initial values. Actual resistance may vary depending on many parameters such as actual dimensions, type, orientation, and so on.

Table 24 Volumetric thermal resistance

Flow conditions [m/s]	Volumetric resistance [cm³ °C/W]
Natural convection	500 ~ 800
1.0	150 ~ 250
2.5	80 ~ 150
5.0	50 ~ 80

It can be roughly assumed that the volume of a heatsink needs to be quadrupled to halve its thermal resistance. This can indicate whether natural convection is sufficient for the available space, or if forced convection is required.

To get an optimized heatsink for any given application, heatsink manufacturers or consultants can be contacted. Further hints and references can be found in [8].

When contacting heatsink manufacturers to find a suitable heatsink, please note the conditions under which the given thermal resistance values are valid. They might be given either for a point source or for a heat source which is evenly distributed over the entire base area of the heatsink. Also take care that the fin spacing is optimized for the corresponding flow conditions.

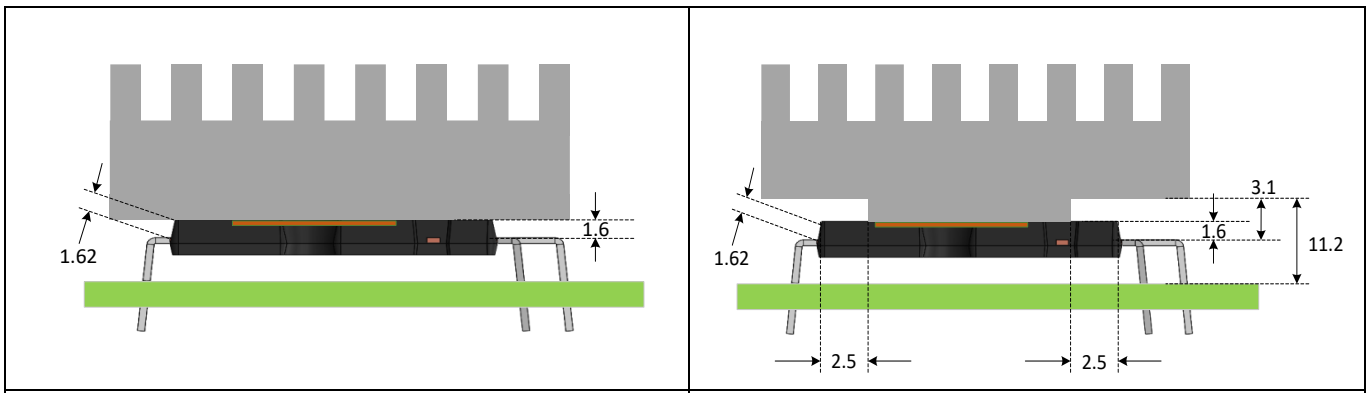
8 Heatsink mounting and soldering method

8.1 Electrical spacing

The electric spacing specifications of IM06BxxxC1 are listed in Table 25. The IM06BxxxC1 package does not satisfy the requirements for clearance and creepage distance between the pins and the heatsink (earthed), and the creepage distance on the PCB between signal pins such as (2) to (3), (4) to (5), and (6) to (7). Based on IEC and UL standards, to secure the clearance and creepage distance between the pins and the heatsink (unearthed), a stepped heatsink, as shown in Figure 44, is required. A PCB slot between the power and the signal pins is required on the PCB.

Table 25 Electrical spacing (*not compliant to IEC) at working voltage 400 V with PD2

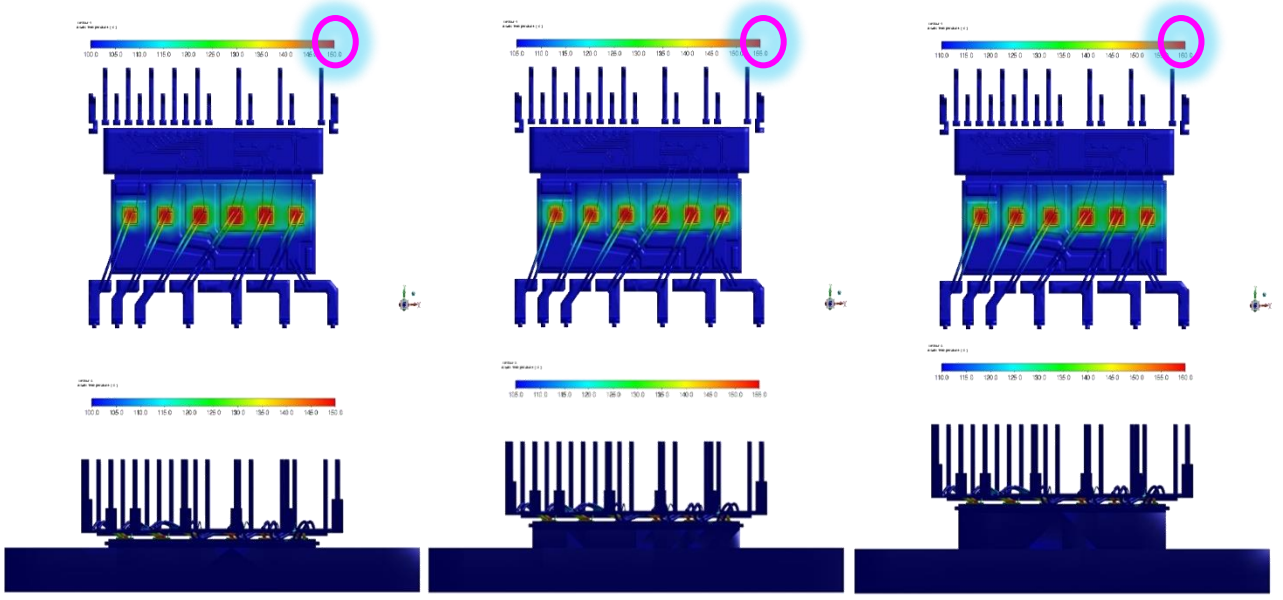
Standard and CIPOS™ Mini	IPM unit				PCB		Remarks
	Pin-to-heatsink (unearthed) basic insulation [mm]		Functional insulation between pins [mm]		PWB (solder-to-solder) [mm]		
	Clearance	Creepage	Clearance	Creepage	Clearance	Creepage	
IEC60335-1 IEC60664-1 IEC67800-5-1 UL840	1.5	2.0 (2.8)	1.5	2.0 (2.8)	2.0	2.0	CTI I (CTI II)
CIPOS™ Mini IM06BxxxC1 IPM	1.6	*1.62	Power pins: 3.03 Signal pins: 2.6	Power pins: 3.21 Signal pins: 3.21	Power pins: 3.03 Signal pins: 2.6	Power pins: 3.21 Signal pins: 3.21	PCB slot is necessary



(a) Normal heatsink (b) Stepped heatsink

Figure 44 Recommended heatsink shape to get the required creepage and clearance distance between the pins and the heatsink

As shown in Figure 45, in terms of thermal performance for each condition, the thermal gap is below 2%.



Step: 0 mm ***Step: 2 mm*** ***Step: 4 mm***

	Step: *0 mm* (Reference)	Step: *2 mm*	Step: *4 mm*
Power [W]	33.22 (Total : 199.35W)	33.22 (Total : 199.35W)	33.22 (Total : 199.35W)
T_{vj} [°C]	150.176	152.384	158.052
T_c [°C]	127.652	129.433	134.997
T_a [°C]	40	40	40
R_{th-jc} [K/W]	0.678	0.691	0.694
R_{th-jc} ratio [%]	100%	101.9%	102.4%

Figure 45 Thermal simulation with various heatsinks (using the Maxi package)

8.2 Mounting the heatsink

8.2.1 General guidelines

An adequate heatsink capability of the IPM can only be achieved if the heatsink is suitably mounted. This is the fundamental requirement for meeting the electrical and thermal performance criteria of the module. The following general points should be observed when mounting the IPM on a heatsink. Ensure that:

- There are no burrs on the aluminum or copper heatsinks
- The screw holes are countersunk
- There is no unevenness or scratches on the heatsink
- The surface of the module is completely in contact with the heatsink
- There is no oxidation, stain, or burrs on the heatsink surface

To improve thermal conductivity, apply silicone grease on the contact surface between the IPM and the heatsink. Spread a homogenous layer (thickness of 100 µm) of the silicone grease over the IPM substrate's surface. Non-planar surfaces of the heatsink may require a thicker layer of thermal grease. Please refer to the specifications from the heatsink manufacturer. It is important to note here that the heatsink covers the complete backside of the module. The functional behavior may differ if any portion of the module's backside is not in contact with the heatsink.

To prevent loss through heat dissipation due to the warping of the substrate, tighten the mounting screws gradually and sequentially while maintaining a left and right balance in the pressure applied.

The design of the application's PCB must ensure that the plane of the module's back side and the plane of the heatsink are parallel to achieve minimal package tension and an optimal contact between the module and the heatsink. Please refer to the datasheets for the mechanical specifications of the module.

It is a good engineering practice to verify the functional and thermal conditions through detailed measurements. It is best to use a final application inverter system that has been assembled with the final production process. It helps in achieving high-quality applications.

8.2.1.1 Recommended tightening torque

As shown in Table 26, the tightening mounting-torque of M3 screws (MS) is specified for a minimum of MS = 0.59 N·m and a maximum of MS = 0.78 N·m. The screw holes must be aligned with the screw openings in the mold compound such that the screws do not contact the mold compound. If an insulating sheet is used, it should be larger than the IPM and should align accurately when attached. It is important to ensure that no air is enclosed by the insulating sheet. Insulating sheets are used in the following cases:

- When the ability to withstand primary and secondary voltages is required to achieve the safety standards required against hazardous situations
- When IM06BxxxC1 must be insulated from the heatsink
- To reduce radiated noise or eliminate other signal-related problems when measuring the module

Table 26 Mechanical characteristics and ratings

Item	Condition		Value			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw: M3		0.59	0.69	0.78	N·m
Back-side curvature	(See Figure 46)	IM06BxxAC1	-50	-	+100	µm
		IM06B50GC1	0	-	+150	
Heatsink flatness	(See Figure 47)		0	-	+100	µm
Weight	IM06BxxAC1		-	5.92	-	g
	IM06B50GC1		-	6.60	-	

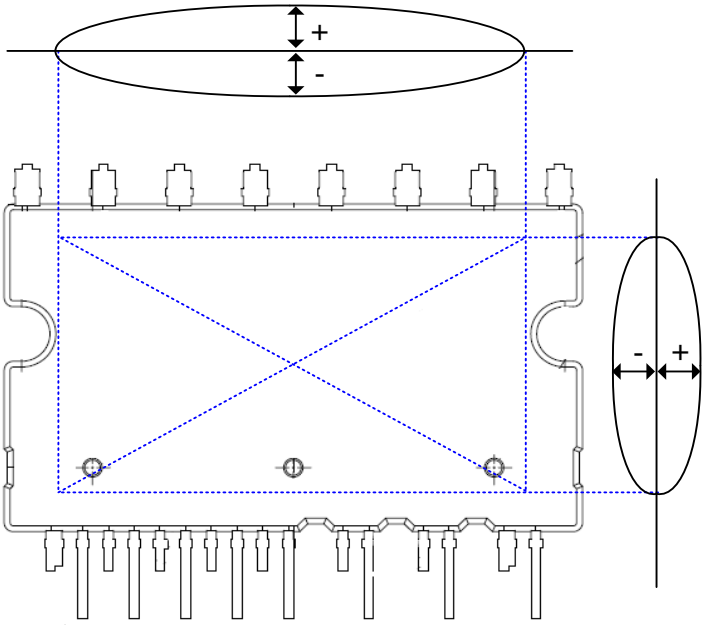


Figure 46 Measurement position for the back-side curvature

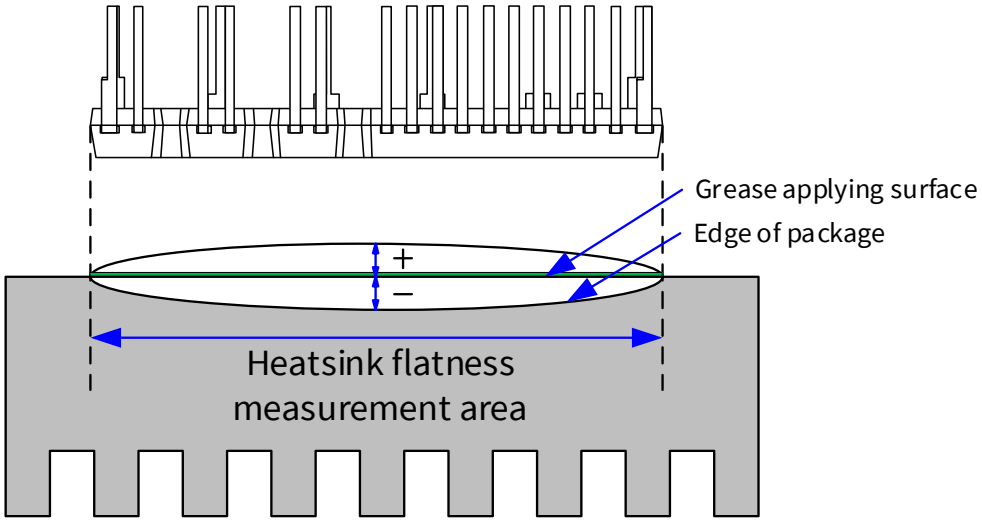


Figure 47 Measurement position for the heatsink flatness

8.2.1.2 Tightening the screws to the heatsink

The tightening of screws is the main process for attaching a module to the heatsink. Generally, a thermal interface material (TIM) is attached to the heatsink surface, which extends to the edge of the module and is in the fixing holes. It is recommended that M3 fixing screws be used together with a spring washer and a plain washer. The spring washer must be assembled between the plain washer and the screw head. The screw torque must be monitored by the fixing tool.

Tightening process:

1. Align the module with the fixing holes.
2. Insert screw A with washers to touch only the position (pre-screwing).
3. Insert screw B with the washers (pre-screwing).
4. Tighten screw A to the final torque.
5. Tighten screw B to the final torque.

Note: The pre-screwing torque is set to 20 ~ 30% of the maximum torque rating.

When installing a module to the heat sink, using excessive and uneven tightening force might stress the chips inside. This can break or degrade the device.

Some basic guidelines to follow are:

- Do not over torque when mounting the screws. Excessive mounting torque may damage the module holes, the screws, and the heatsink
- Avoid one-sided tightening stress. Uneven mounting can damage the module holes
- For effective heat dissipation, enlarge the contact area as much as possible. This also minimizes the contact thermal resistance
- Ensure that the thermal conductive grease is applied properly over the contact surface between the module and the heatsink. This also protects the contact surface from corrosion. The grease should be of stable quality and have long-term durability over a wide range of operating temperatures
- Use a torque wrench to tighten till the specified torque rating. Exceeding the maximum torque limitation may damage or degrade the module
- Make sure that there is no dirt on the contact surface between the module and the heatsink
- All equipment used to handle or mount the IPM must comply with the relevant ESD standards. This includes transportation, storage, and assembly. The module itself is an ESD-sensitive device. It may, therefore, get damaged in case of ESD shocks
- Do not shake or grasp the heatsink. Avoid any shock to the PCB by grasping only the heatsink. This can create cracks or break the package

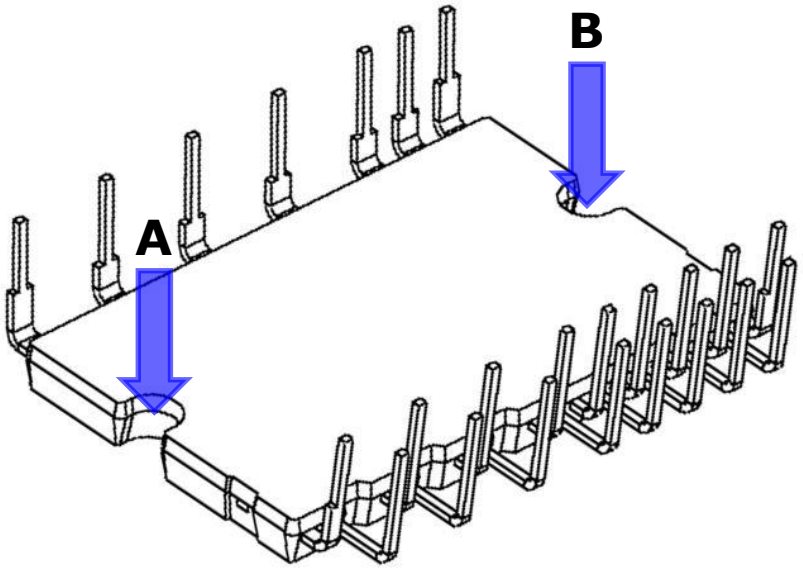


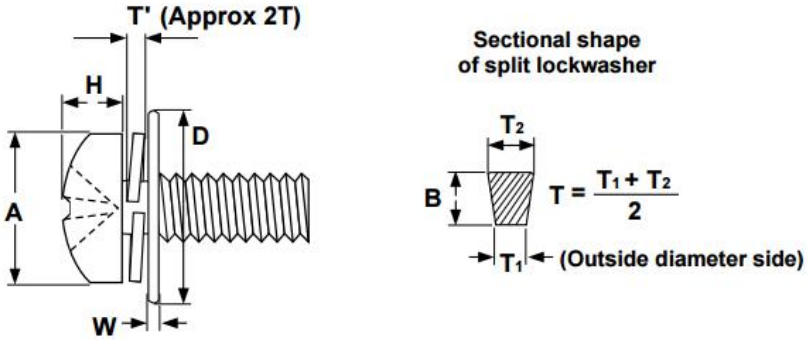
Figure 48 Recommended screw-tightening order: Pre-screwing A → B, final screwing A → B

8.2.1.3 Mounting screw

Using M3 SEMS screws (JIS B1256/JIS B1188) is recommended for attaching the module to the heatsink, as listed in Table 27.

Table 27 Recommended screw specifications (Typical)

Screw dimensions				Flat washer		Spring washer	
Size	Thread pitch	A Head diameter	H Head height	D Outer diameter	W Thickness	D1 Outside diameter	B x T
M3	0.5	5.2	2.0	7.8	0.58	5	1.1 x 0.7



8.3 Soldering conditions

8.3.1 Wave soldering

Wave soldering is a large-scale soldering process through which electronic components are soldered onto a PCB to form an electronic assembly. The name is derived from the soldering process — a tank is used to hold a quantity of molten solder, the components are inserted into or placed on the PCB and then the loaded PCB is passed across a pumped wave or cascade of the solder. The solder wets the exposed metallic areas of the board (those not protected with solder mask) creating a reliable mechanical and electrical connection.

The leads of trough-hole devices (THD) are long and straight at the end. Therefore, they can be inserted into the drill holes in the PCBs and be attached by wave soldering. Only the leads that extend through the drill holes in the PCB meet the hot solder. The body of the package is heated by the hot leads [8].

This method has two consequences:

- The package body stays cooler than in the case of reflow soldering
- The temperature gradient between the leads and the body and inside the package is greater than in the case of reflow soldering

Therefore, in a wave-solderable THD the heat resistance is tested according to JESD22-B106 and IEC668 2-20 (typically 260°C, 10 s).

Immersing the entire package body into the molten solder is not recommended because THDs are generally not suited for such harsh temperature shocks.
Dual-wave soldering is the most used wave-soldering method (see Figure 49). The peak temperatures, ramp rates, and time used depend on the material and the wave-soldering equipment.

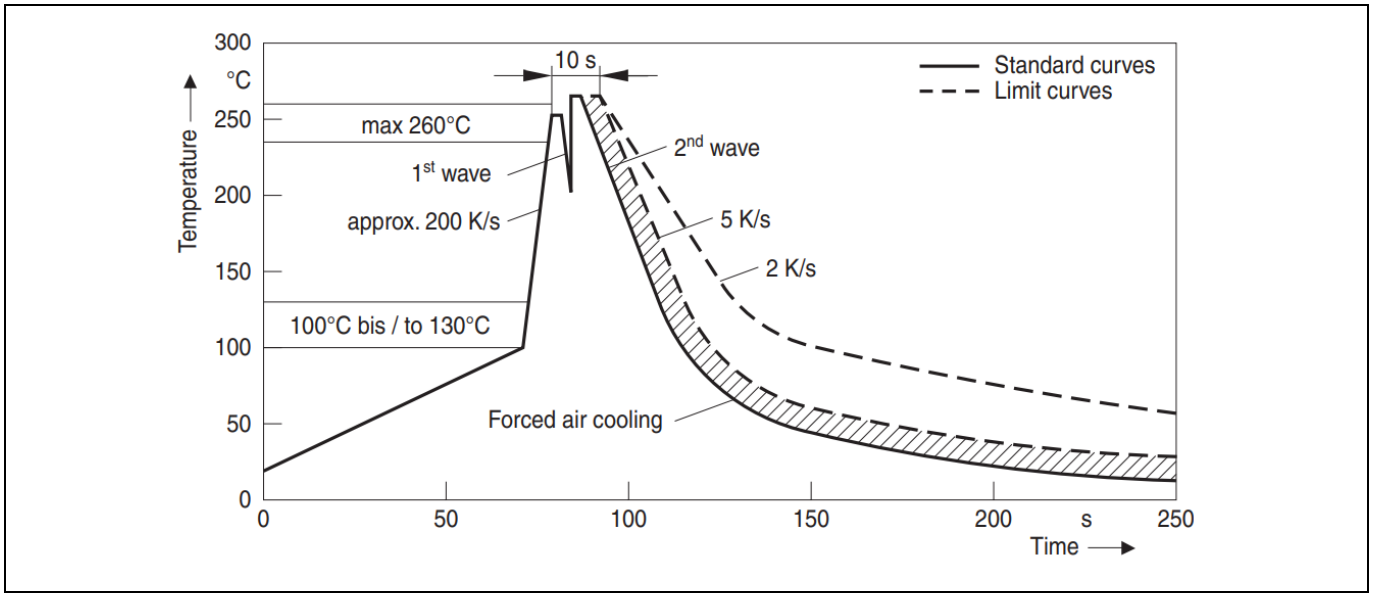


Figure 49 Typical dual wave soldering profile

8.3.2 Manual soldering

Considering the glass-transition temperature (T_g) of the package mold resin and the thermal-withstand capability of the internal chips and assembly, the temperature of the lead root should be kept below 150°C. The iron tip should touch the lead only at its tip, away from the package mold body. It is recommended that the soldering time be as short as possible.

Testing method with a manual solder iron: ATC-2450-3 (ARIM), 50 W:

- Put the soldering tip of the 50 W iron (temperature set to upper conditions) on the terminal (within 1 mm of the terminal end point) and measure the temperature rise in the root part of the terminal using the thermocouple installed on the terminal root

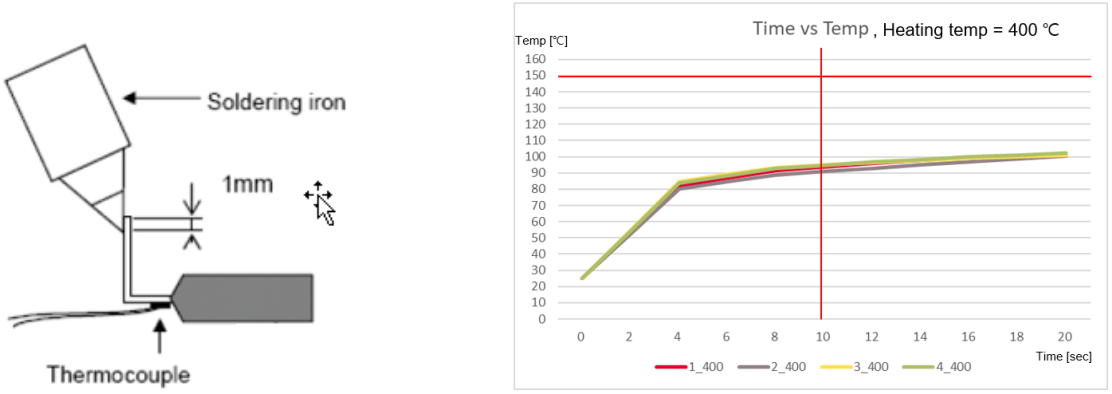


Figure 50 Heating and measuring point, temperature alteration of the terminal root (example)

Recommendations for manual soldering of the CIPOS™ Mini IPM series:

- The available range of temperature is 350 – 400°C (for 10 seconds)
- A temperature over 400°C is not recommended as it can delaminate the lead after soldering
- Mass production is not recommended as it may be difficult to control the amount of solder applied

9 Package handling guidelines

9.1 Recommended storage conditions

Temperature: 5 – 40°C

Relative humidity:-10 – 75%

- Avoid leaving the CIPOS™ IPM exposed to moisture or direct sunlight. Be particularly careful during rainfall or snowfall
- Use storage areas that have minimal temperature fluctuation. Rapid temperature changes can create condensation on the stored CIPOS™ IPM, resulting in lead oxidation or corrosion and degraded soldering ability.
- DCB substrates are designed with a copper layer that is directly exposed to air, leading to natal oxidation process, but oxidized copper layers have no impact on the thermal performance [9].
- Do not allow the CIPOS™ IPM to be exposed to corrosive gasses or dusty conditions
- While storing, ensure that no excessive external forces or load is applied on the CIPOS™ IPM
- If storing the modules for a long time (more than one year), ensure they are kept dry
- Before using a module that has been in storage for a long time, ensure that there are no visible flaws, stains, or rust on the exterior

9.2 Packing specification

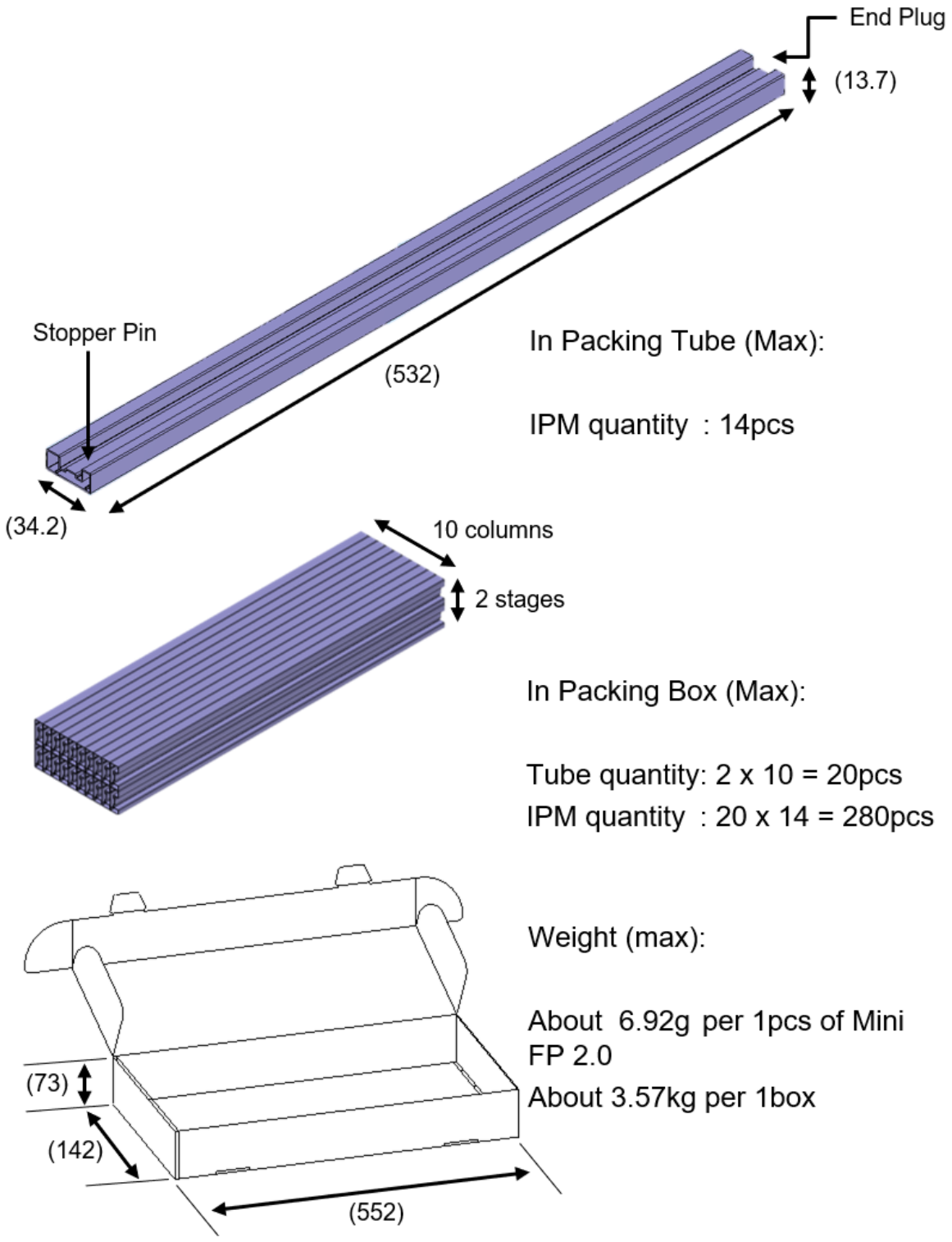


Figure 51 Packing information

References

[1] S. Shen, B. Sahan, C. Jaeger, A. Puyadena, A. Brodt, A. Lenze, and C. Müller, “Higher efficiency and power density of variable speed drives with new TRENCHSTOPTM IGBT7”, PCIM Asia, Shanghai, China, 2018

[2] R. Keggenhoff, Z.Liang, Andre Arens, P. Kanschat, and R. Rudolf, “Novel SOI Driver for Low Power Drive Applications”, Power Systems Design Europe Nov. 2005

[3] W. Frank, J. Oehmen, A. Arens, D. Chung, and J. Lee, “A new intelligent power module for home appliances”, Proceedings of PCIM 2009, Nuremberg, Germany

[4] Infineon Technologies AG. AppNote Number AN2020-14, “Bootstrap circuit design for CIPOS™ IPM series”, www.infineon.com

[5] D. Chung and S. Sul, “Minimum-Loss Strategy for three-Phase PWM Rectifier”, IEEE Transactions on Industrial Electronics, Vol. 46, No. 3, June 1999

[6] IPOSIM, http://www.infineon.com/IPOSIM

[7] Aavid Thermalloy, http://www.aavidthermalloy.com/technical/correct.shtml

[8] S. Lee, “How to select a heatsink”, Electronics Coolings, Vol.1, No.1, June 1995

[9] Infineon Technologies AG. AppNote Number AN20205-01, “Oxidized copper layer on CIPOS™ IPMs and MMs products”, www.infineon.com

Revision history

Version number	Revision date	Revision description
1.00	2024-11-20	Initial release
2.00	2025-03-28	Added information about IM06B50GC1, chip positions, and corrected typographical errors

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2025-03-28

Published by

Infineon Technologies AG

817 26 Munich, Germany

© 2025 Infineon Technologies AG. All Rights Reserved.

Do you have a question about this document?

Email: erratum@infineon.com

Document reference
AN2024-08

IMPORTANT NOTICE

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (**www.infineon.com**).

Please note that this product is not qualified according to the AEC Q100 or AEC Q101 documents of the Automotive Electronics Council.

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.