Application Note AN-990

IGBT Characteristics

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This application note covers some of the major issues normally encountered in the design of an IGBT power circuits. It is the companion to AN-983, "IGBT Characteristics," which covers the details of the device, rather than its application.

1. Gate drive Requirements

A. Impact of the impedance of the gate drive circuit on switching losses

As shown in the equivalent circuit of Figure 1, the IGBT consists of a PNP driven by an N-Channel MOSFET in a pseudo-Darlington configuration. The gate drive circuit controls directly the MOSFET channel of the IGBT and, through the drain current of the MOSFET, the base current of its bipolar portion. Since the turn-on characteristics of an IGBT are determined, to a large extent, by its MOSFET portion, the turn-on losses will be significantly affected by the gate drive impedance. Turn-off characteristics, on the other hand, are chiefly determined by the minority carrier recombination mechanism, which is only indirectly affected by the MOSFET turn-off.

As a result, gate charge parameters of an IGBT do not provide meaningful indication of switching performance, as they do in power MOSFETs. Gate charge remains, however, a useful parameter to design the gate drive circuit.

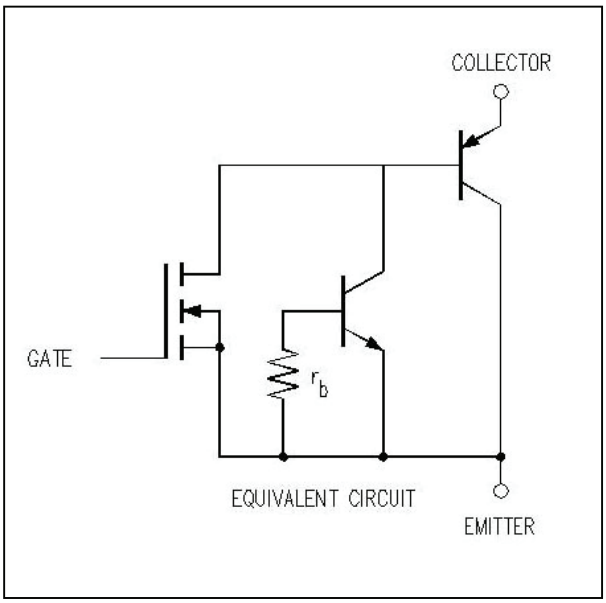

Figure 1. IGBT equivalent circuit. The terminal called *collector* is actually the *emitter* of a PNP transistor. The MOSFET drives the base of the PNP and determines the turn-on speed of the IGBT and its voltage drop.

An increase in gate drive impedance prolongs the Miller plateau and delays the current fall. The impact of the gate drive impedance on total switching losses depends on the design of the IGBT and its speed. The impact on *turn-on losses* is appreciable for all IGBTs from International Rectifier, regardless of speed. The impact on

turn-off losses depends on the speed of the device and its technology: trench IGBT and high speed IGBTs are more sensitive to gate drive impedance. In any event, *additional* gate drive impedance has a lower *marginal* impact, i.e. the same amount of additional drive impedance will have a lower effect if the gate drive impedance is already high.

Gate drive impedance is frequently increased for a practical reason: to reduce the current spike and ringing at turn-on caused by the reverse recovery of the diode. This resistance can be safely bypassed with an anti-parallel diode to reduce the turn-off losses, as shown in Figure 28 of AN-978. In several instances a judicious use of this network may actually reduce the turn-on losses.

The specific dependence of the switching energy on gate drive resistance is shown in most data sheets.

B. Impact of the gate drive impedance on noise sensitivity

In MOS-gated devices (IGBTs, FETs, etc.) any dv/dt that appears on the collector is coupled to the gate through a capacitive divider consisting of the Miller capacitance and the gate-to-emitter capacitance (Figure 2a).

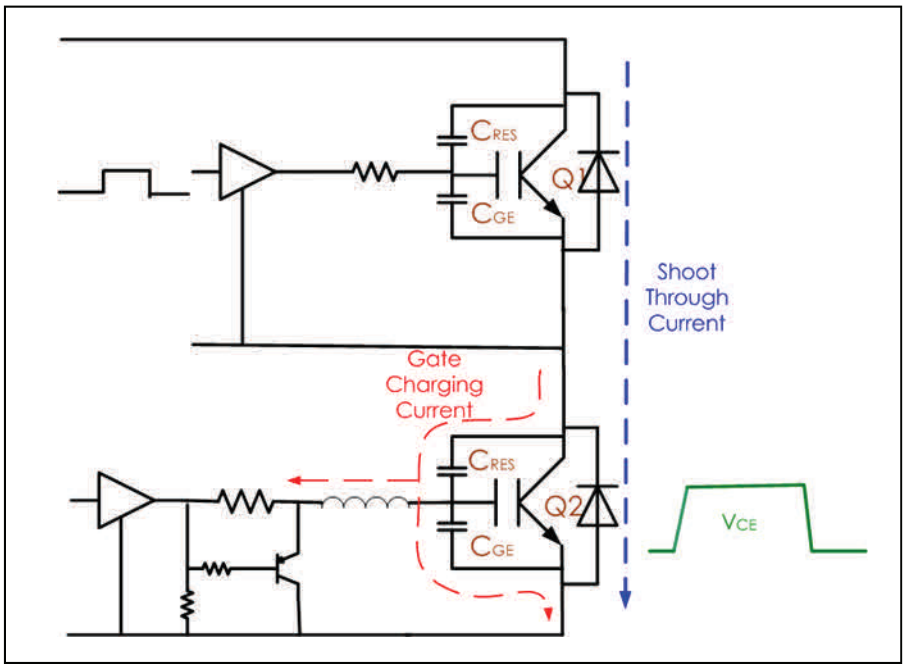

Figure 2a. A dv/dt on the collector of the lower IGBT is reflected to the gate through the capacitive divider C_{rss}/C_{gss}. The spike may be high enough to turn-on the IGBT, depending on the ratio of these two capacitances and the internal impedance of the gate drive (Z_G).

If the gate is not solidly clamped to the emitter, a large enough dv/dt takes the gate voltage beyond its threshold and the IGBT conducts. As the IGBT goes into conduction it clamps the dv/dt that is causing it to conduct so that the gate voltage never goes much beyond the threshold voltage, as it is evident from Figure 2b. The end result is a limited amount of "shoot-through" current, with an increase in power dissipation.

Notice that the “shoot-through current” in Figure 2b includes a capacitive charging current that cannot be completely separated from the shoot-through current. The shoot-through current only flows after the gate exceeds the threshold voltage (approximately 3 to 5V), while the capacitive current flows as soon as the dv/dt appears on the collector.

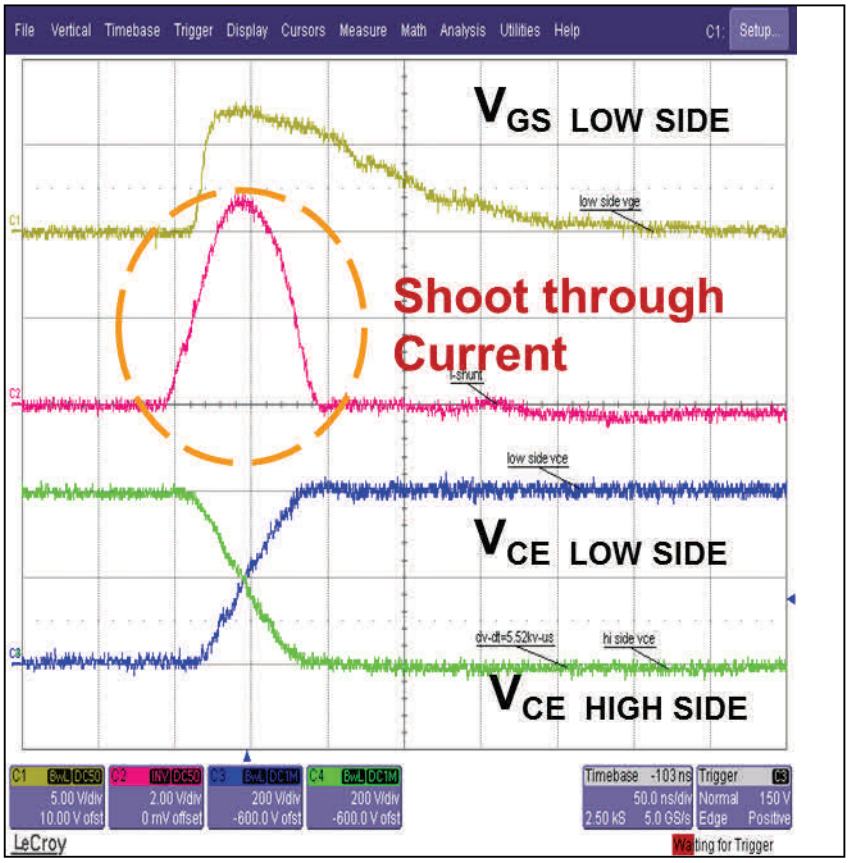

Figure 2b. The dv/dt on the collector of the low-side IGBT is coupled to the gate and causes some shoot-through current to flow. Part of the shoot-through current charges the device capacitances.

To reduce noise sensitivity and the risk of this dv/dt-induced turn-on, the gate drive impedance must be very low when the device is in the off-state and the gate voltage is close to zero. The small PNP transistor shown in Figure 2a is frequently used to clamp a positive-going dv/dt that appears on the gate.

Gate drive circuits in high power application swing positive (+15) to negative (-5 or -15V). This provides an added measure of noise immunity and improves switching performance. However, this requires additional isolated supplies for the high-side IGBTs and increases the cost of the gate drive. If the only concern is immunity

to dv/dt induced turn-on, a capacitor from gate to source or the solution in Figure 2a may be enough to solve the problem. In any event, the inductance of the gate charge/discharge loops should be minimized with parallel PCB tracks or twisted wires.

In some cases the effects of a contained amount of dv/dt induced turn-on, i.e. a small increase in power dissipation, can be an appealing alternative to the added complexity of the negative gate bias.

For most applications, the circuit shown in Figure 3 provides a simple, low cost, high performance solution to the gate drive requirements. IR has a large selection of gate drivers to address different circuit requirements. As an example, the gate driver shown in Figure 4 performs the current limiting and short circuit protection function by controlling the gate voltage.

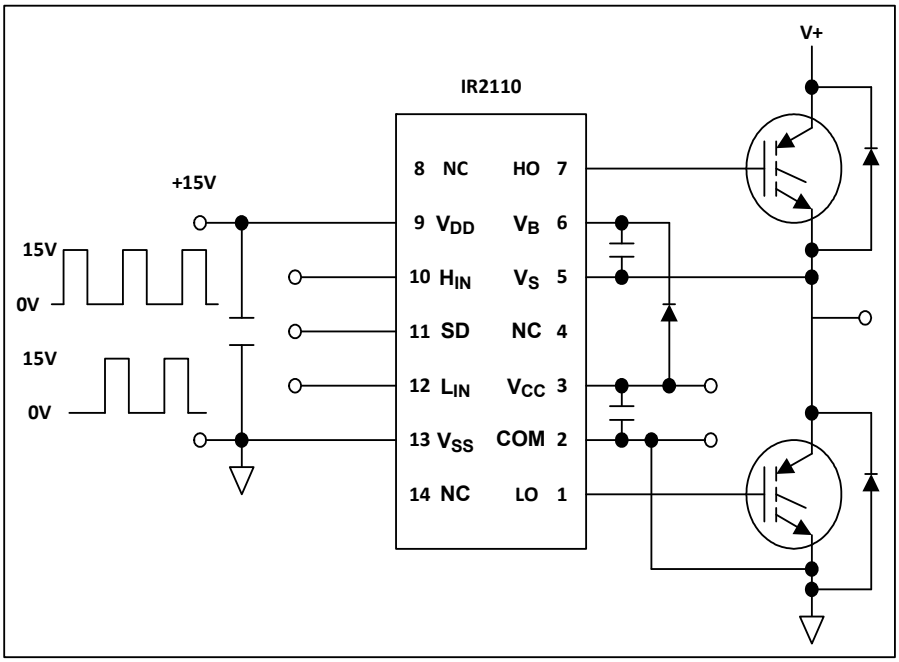

Figure 3. The IR2110 provides a simple, high performance, low cost solution to the problem of driving a Half-Bridge

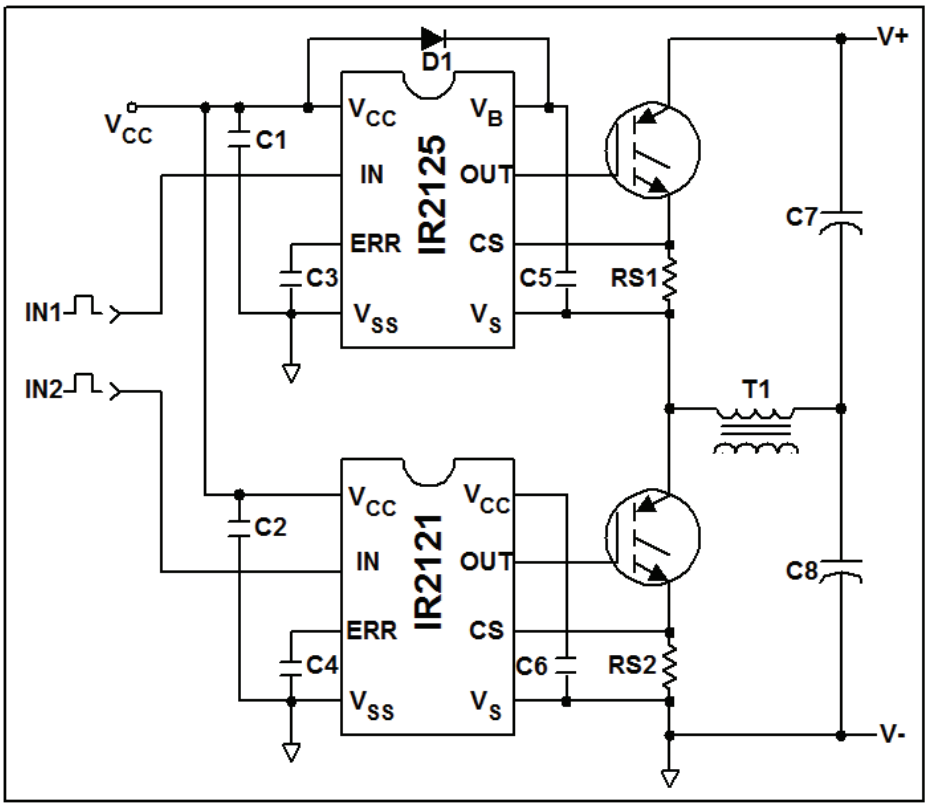

Figure 4. Short circuit protection performed with MOS gate driver ICs

C. Contribution of "common emitter inductance" to the impedance of the gate drive circuit

The "common emitter inductance" is the inductance that is common to the collector circuit and the gate drive circuit (Figure 5a). This inductance establishes a feedback from the collector circuit to the gate circuit that is proportional to $L di_C/dt$. The voltage developed across this inductance subtracts from the applied gate voltage during the turn-on transient and adds to it during turn-off. In so doing, it slows down the switching.

This phenomenon is similar to the Miller effect, except that it is proportional to the di/dt of the collector current rather than the dv/dt of its voltage. In both cases the feedback is proportional to the transconductance of the IGBT, a function of die size and technology. A di_C/dt of 0.7A/ns is quite common in IGBT circuits and voltages in the order of 7V could be expected in 10 nH of common emitter inductance. As it happens, the feedback mechanism slows down the turn-on process, thereby limiting the di_C/dt.

Simple layout precautions can reduce the common emitter inductance to the bare minimum that is already inside the package. Separate wires to the emitter pin should be provided for the flow of the collector current and for the gate return, as shown in Figure 5b. The gate lead and the gate return lead should be twisted or

run on parallel PCB tracks to minimize inductance in the gate drive path. This improves immunity to dv/dt induced turn-on and reduces ringing in the gate.

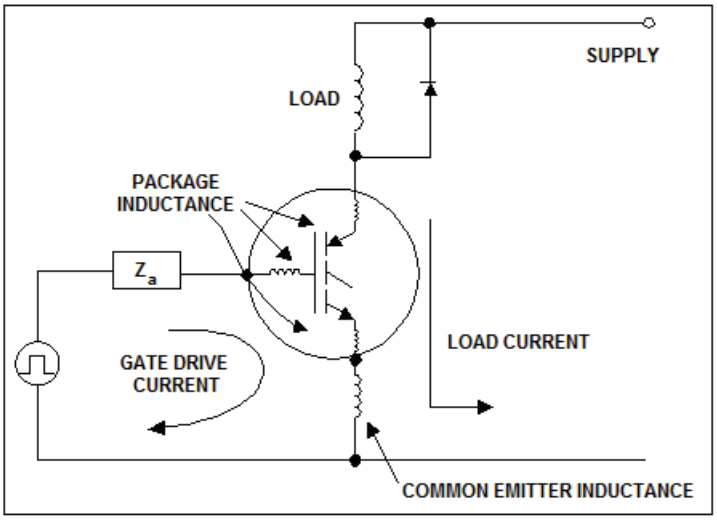

Figure 5a. "Common Emitter Inductance" is the inductance that is common to the collector current and the gate drive current

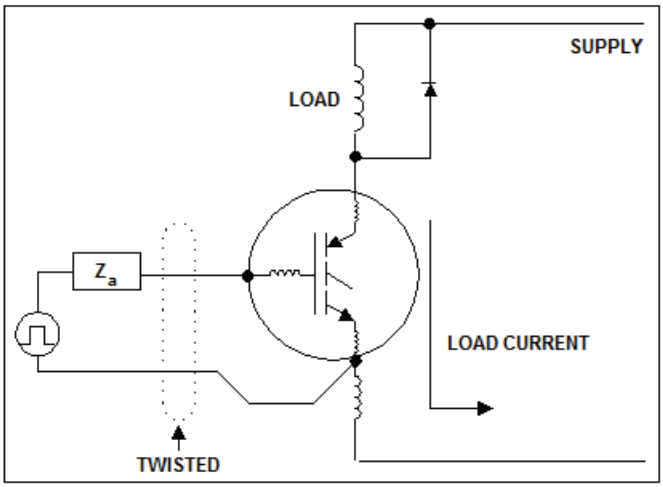

Figure 5b. "Common Emitter Inductance" can be eliminated by running separate wires to the emitter pin, one for the emitter, the other for the gate drive return.

2. Switching Trajectories and Safe Operating Area

Minority carrier devices, when subjected to high levels of voltage and current, can experience uneven current distributions within the die that, taken beyond safe limits, can cause device failure. Section 6 of AN-983 gives an overview of the three operating conditions where this could happen.

The distribution of current within the die is different, depending on the sign of the di/dt associated with it. Hence, the Safe Operating Area curve, which was devised as a convenient representation of this limitation, is frequently differentiated into "Forward Biased SOA" and "Reverse-Biased SOA".

The Forward Biased SOA curve applies to linear operation in Class A, Class B or during short circuit which can be considered an extreme case of Class B operation. Thermal limitations for pulsed operation are frequently included in this curve, even though the Transient Thermal Response curve provides this same information in a more comprehensive and accurate way. Due to the limited use of IGBTs in linear operation, the FBSOA curve is normally omitted from the data sheet.

The Reverse Biased SOA (also called "clamped IL") applies when switching off a clamped inductive load, including the turn-off from a short circuit condition. Figure 6 shows the importance of this rating. During the turn off of a clamped inductive load, the voltage across the transistor goes from the low value of $V_{CE(sat)}$ to the full supply voltage while the collector current stays constant. After the collector voltage exceeds the supply voltage by a diode drop, the diode goes in conduction, thereby taking over the inductor current from the transistor. Thus the trajectory of the operating point moves along a constant current line until it intercepts the supply voltage, at which point a voltage overshoot normally occurs, whose magnitude depends on the amount of stray inductance L_S and the turn-off speed.

It will be appreciated that, for a safe commutation of the load current, the entire trajectory must lay within the turn-off SOA and that any limitation in the RBSOA will translate into a limitation of turn-off capability of inductive loads.

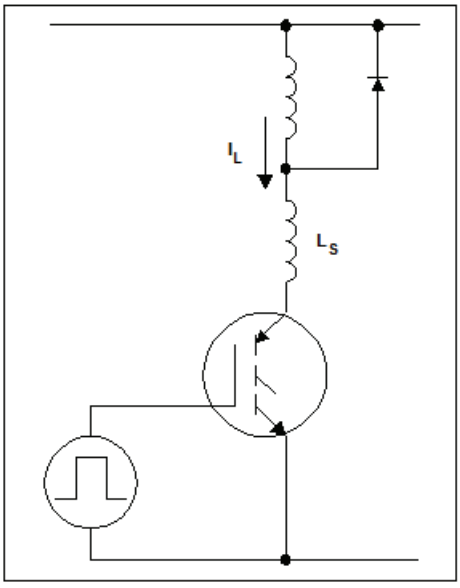

Figure 6a. Typical Clamped Inductive load

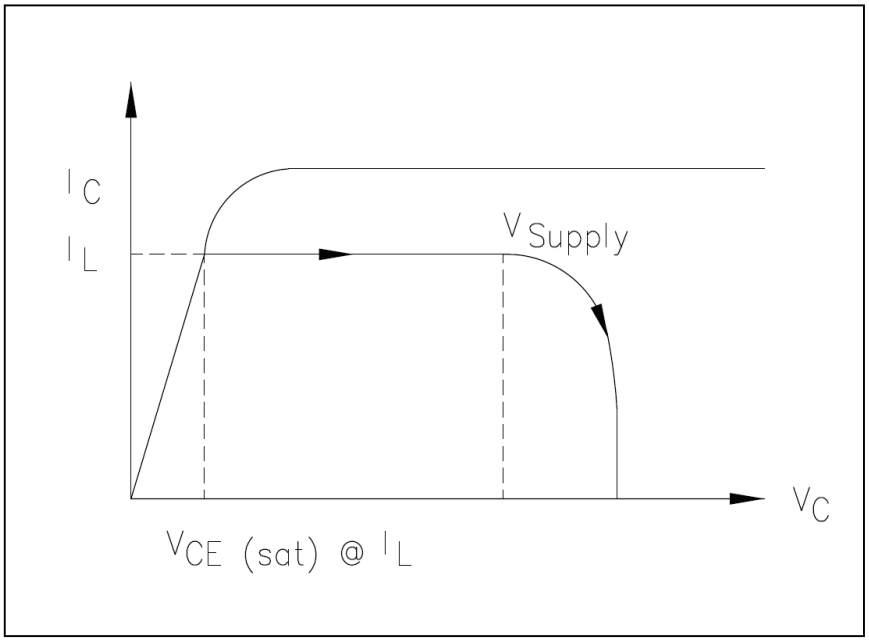

Figure 6b. Trajectory of the operating point during a turn-off transient. This trajectory should be within the SOA curve of the IGBT.

The second breakdown of IGBTs occurs at current and voltage levels that are significantly higher than what is normally encountered in a practical application, as shown in the data sheets. Notice that the values therein contained apply at high temperature and that load-shaping snubbers are not necessary, as long as the switching trajectory is confined within the turn-off SOA. Snubbers are frequently used to limit overshoots and/or reduce EMI. This function is not related to SOA.

3. Conduction Losses

At any given time, the energy dissipated in the IGBT can be obtained with the following expression:

$$E = \int_0^t V_{CE}(i)i(t)\,dt$$

where t is the length of the pulse. Power is obtained by multiplying energy by frequency, if applicable. When the transistor is off i(t) ≅ 0 and losses are negligible. Unfortunately, no simple expression can be found for the voltage and current functions when the IGBT is conducting. Hence, for analytical expediency, we resort to the distinction between conduction and switching losses.

We define conduction losses the losses that occur between the end of the turn-on interval and the beginning of the turn-off interval, as defined for the switching losses characterization. Since the turn-on energy is measured from 5% of the test current to 5% of the test voltage and the turn-off energy is measured starting from 5% of the test voltage, conduction losses occur when the voltage across the IGBT is less than 5% of the test or supply voltage (see AN-983, Section 8.4). The function $V_{CE}(i)$ in the formula above characterizes the conduction behavior of the IGBT. This information is provided in the data sheet with graphs and specific values.

The tabular information in the data sheet provides a few limit points that, with the help of the graphs, can be used to generate the information necessary to calculate the conduction losses. To obtain the max voltage drop at any current and temperature, from the data sheet values, a two-step procedure can be followed:

1) Obtain a typical value for the collector voltage by interpolating a curve in the Collector Voltage vs. Collector current figure of the data sheet at the desired current level and the appropriate junction temperature.
2) To obtain a maximum value, the voltage drop read from this curve at the appropriate junction temperature is multiplied by the ratio between maximum and typical from the Table of Electrical Characteristics.

Finally, conduction losses must be multiplied by conduction time (if the desired result is energy) or duty cycle (if the desired result is power).

If the current waveform is not constant during the conduction interval, it should be broken up into smaller intervals, calculating the losses for each sub-interval and summing the results, rather than averaging or taking its RMS value. An appealing alternative would be to generate a simple function by means of a curve-fitting algorithm. This function could be easily integrated by mathematical routines.

4. Losses in Hard Switching

Losses in hard switching have been broken down into two components that will be analyzed separately: turn-on losses and turn-off losses.

Like conduction losses, "hard switching" operation is characterized with tabular information and with graphs in the data sheet.

As explained in AN-983, Section 8.4, the Switching Energy reported in the data sheet makes specific reference to a test circuit that simulates a clamped inductive load.

It is important to remember that switching energy changes significantly with temperature and all calculations should be carried out with numbers that are appropriate for the operating temperature.

Turn-on and turn-off losses can be calculated with the same two-step technique described in the previous section, complemented by the following additional corrections:

1) The energy loss thus obtained must be scaled with voltage. Data sheet measurements have been taken with a defined supply voltage that may or may not be the same as the supply voltage of the specific application.
2) Similarly, the gate drive resistance of the test circuit in the data sheet may be different from what is used in the actual application. Recent data sheets have a figure that correlates switching energy with gate drive impedance.
3) Switching energy must be multiplied by frequency to obtain power losses.

The turn-on transient of a clamped inductive load is complicated by the reverse recovery of the anti-parallel diode of the complementary device. When the IGBT turns on it will take over the entire load current *plus* the reverse recovery current of the diode that was carrying the load current when the IGBT turns on. Switching energy data in recent data sheets include the “diode induced” losses.

Earlier data sheets used a different test circuit with an “ideal diode”. This test circuit measured turn-on energy without the diode induced losses. It follows that, to obtain the total turn-on losses two components have to be calculated separately and added together.

Figure 7 shows a typical turn-on waveform. Notice how the reverse recovery of the diode increases the turn-on energy in two ways:

- it adds to the turn-on current when the collector voltage is still close to the supply voltage
- it delays the collapse of the gate voltage.

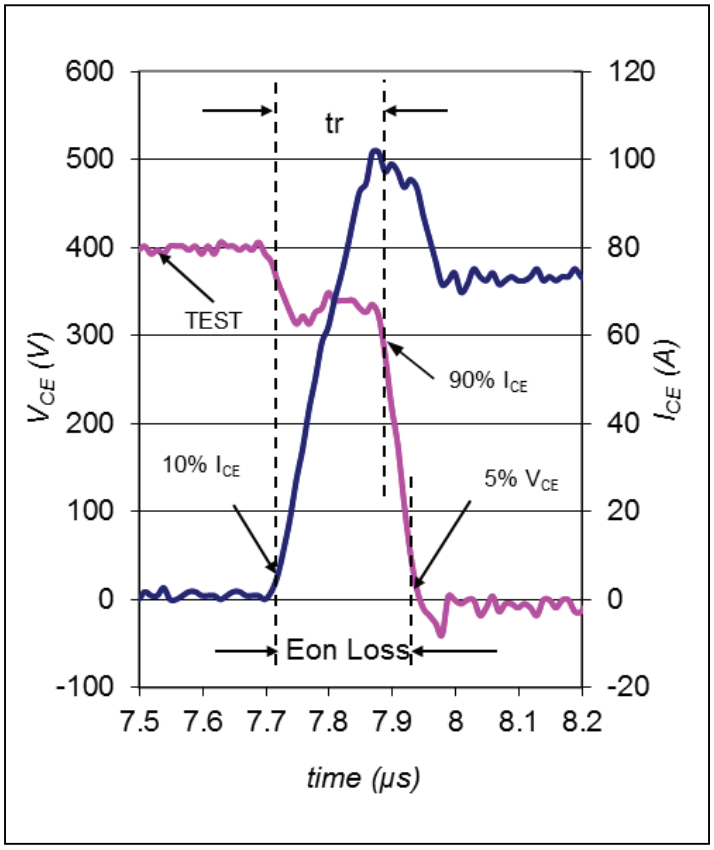

Figure 7. The reverse recovery current builds on top of the load current and makes a significant contribution to the turn-on energy (IRGP4066D, 400V, 75A, 175°C)

Like conduction losses, switching losses can be handled with relatively simple analytical algorithms

5. Trade-off between Conduction and Switching Losses: Device Optimization

To maximize the value to the user of its IGBT technology, IR has introduced a number of application-specific devices. Some are optimized for motor drives, some for induction heating and some for plasma displays.

This development and the proliferation of part numbers has made the selection of an IGBT a complex iterative process that requires evaluation of many parameters that cannot be simplified into a single metric, like on -resistance. Switching losses must be traded against conduction losses and both against short circuit requirements.

To make this task easier, IR developed a webtool that suggests a short list of parts that meet the constraints of the application. It provides an estimate of losses and comparative prices. The tool can be found at:

http://mypower.irf.com/IGBT

To quantify these considerations a simple method has been developed comparing different power devices in a typical switchmode environment. This figure is application-related in so far as it takes into account the thermal environment, as well as the electrical operating conditions. It is one of the most useful tools to select the optimal IGBT for a specific application.

The popular half-bridge operated with a clamped inductive load was chosen as the benchmark circuit to compare the Performance of different IGBTs. Operating conditions are listed in Figure 8 and they can all be changed to suit a specific application. Fly-back or resonant circuits could be used in place of the half-bridge to obtain results that are specifically tailored to a given application. This figure shows in a clear and concise way to what extent higher switching frequencies impact the current output of the pair. It also provides a simple way of selecting the optimum device for the application, which is the one that gives the highest output current at the specific operating frequency.

Once the thermal constraints are properly factored into the operating conditions, the graph carries important application information. In a motor control, the RMS component of the fundamental is directly related to torque. In a power supply, on the other hand, the total RMS content of the square wave contributes to power. The ratio between the two is 1:11. This figure is present in most data sheets as Figure 1.

As an example, Figure 8 compares the following IGBTs:

- The IRG7PC35SD is a high-density trench device specifically targeted for low voltage drop (resonant applications). As it should be expected, its low-frequency current-carrying capability is remarkable.

- The IRGB20B50PD1 is a Gen 5 planar device, introduced in the late nineties. It may still be the best device at high frequency, in spite of the fact that its voltage drop is higher than trench devices.

- The IRGP4069D is a general purpose trench device for hard-switching applications.

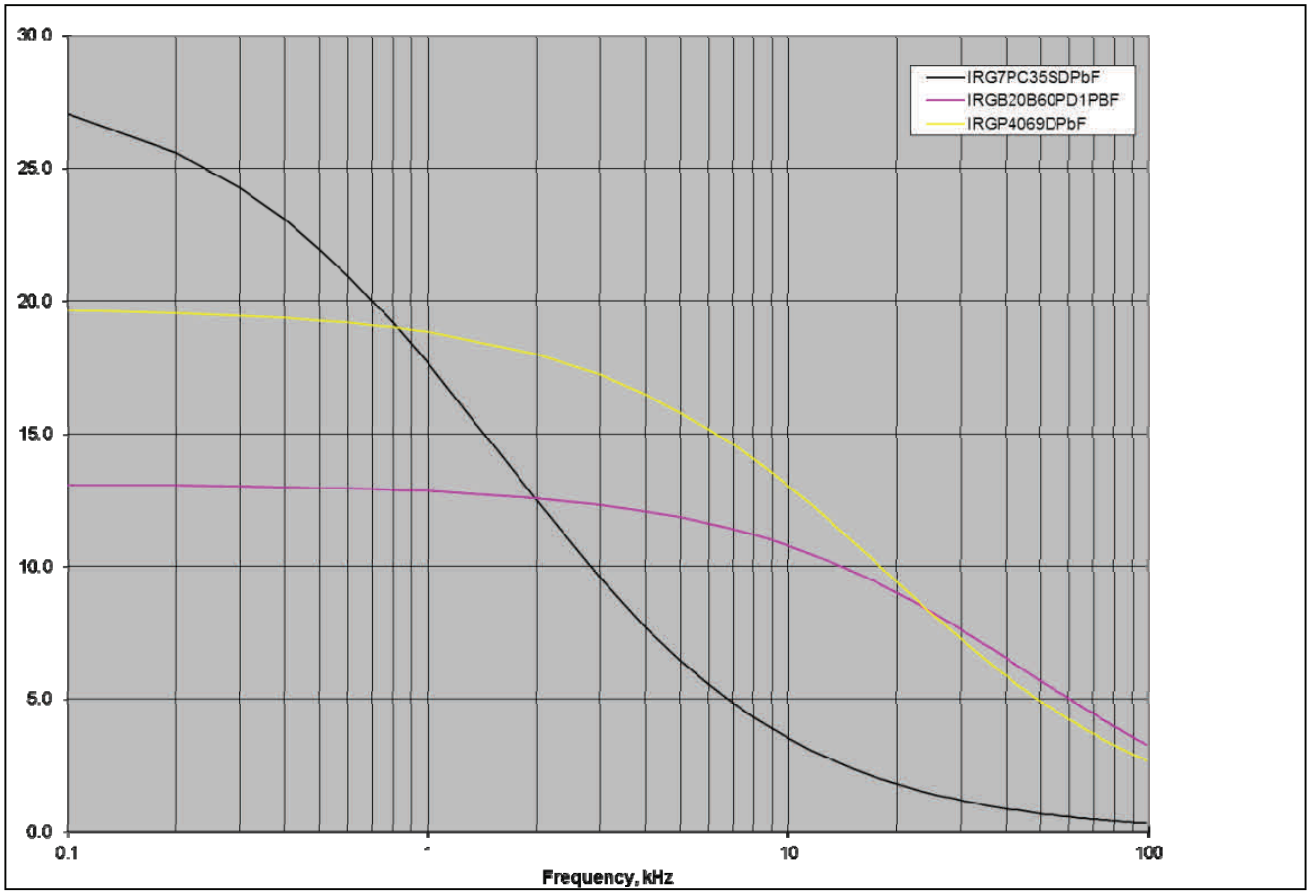

Figure 8. This Current vs. Frequency curve compares the performance of three different IGBTs in a hard-switched half-bridge. Junction temperature: 150°C, Thermal resistance of insulator: 1°C/W, Thermal resistance of common heatsink: 2°C/W, Ambient temperature: 55°C, Switching voltage: 400V.

6. Thermal Design

IGBTs, like power MOSFETs and thyristors, are thermally limited and a good thermal design is the key to their cost effective utilization. This topic is covered in detail in AN-1057.

In general, the objective of the thermal design is the selection of the best device-heatsink combination. This may require a number of calculations, as indicated in AN-949. The entire selection process can be sped-up significantly with the help of simple device models plugged into an application-specific spreadsheet.

In order to obtain a thermal resistance case-to-sink that is close to the data sheet value, the mounting torque should be approximately the value specified in the data sheet. An excessive mounting torque causes the package to bow and may crack the die. An inadequate mounting torque, on the other hand, results in poor thermal performance.

The temperature rise due to pulses of short duration can be calculated with the transient thermal response curve in the data sheet. The section "Peak Current Rating" in AN-949 describes the procedure in detail

For short pulses (5ms or less) the temperature rise calculated with the transient thermal response curve tends to be on the conservative side. A more accurate method to calculate temperature rise requires a Finite Element Analysis simulation.

7. Replacing MOSFETs with IGBTs

Many high voltage applications do not take advantage of the superior switching capabilities of MOSFETs, due to EMI constraints and stray inductances. In these applications IGBT can be an appealing alternative for a number of reasons:

- Much lower conduction losses that are substantially constant over temperature.
- Smaller die area with lower input capacitance, simpler gate drive and lower cost.
- Smooth di/dt and dv/dt with minimal EMI signature and low overshoots.
- The diode co-packaged with the IGBT has much superior switching characteristics than the integral body diode of high voltage MOSFET and generates lower current spikes. This is a distinct advantage in those topologies that rely on an anti-parallel diode.

Because the package style and the pin-outs of MOSFETs and IGBTs are identical, no mechanical or layout changes are required.

The gate drive requirement for IGBTs is similar to MOSFETs. A gate voltage between 12V and 15V is sufficient for turn-on, and no negative voltage required at turn-off. The value of the series gate resistor may have to be increased to avoid ringing at the gate of IGBT due to the lower input capacitances.

8. Guidelines on Paralleling

Paralleling reduces conduction losses and junction to case thermal resistance. However, switching losses may increase. If they are the dominant losses, only a thermal resistance improvement will be achieved by paralleling.

Power MOSFETs parallel relatively well due to the positive temperature coefficient of their dominant losses (conduction), while switching losses are largely independent from temperature. The IGBT, on the other hand, has a temperature coefficient of the conduction losses that is largely independent from temperature, while switching losses have a significant positive temperature coefficient. This is why paralleling of IGBTs is not as straightforward as paralleling of MOSFETs.

The issues involved in paralleling MOSFETs have been covered in detail in AN-941 and they remain valid for IGBTs. The following considerations cover only what is specific to IGBTs and assume that the reader is familiar with the content of AN-941.

The $V_{CE(on)}$ of an IGBT is a weak function of current and temperature, as compared to the $V_{DS(on)}$ of a MOSFET that is very sensitive to both. When two IGBTs are operated in parallel, the $V_{CE(on)}$ across both devices is forced to be the same. Thus, for a given load current, one IGBT will carry more current than the other, resulting in a current unbalance that, *a*t very low currents, can be quite high: 75-100%. Current unbalance is not critically important in itself, but in its implications for junction temperature and switching losses, as explained below.

Junction temperature: Since the voltage drop is the same for both IGBTs, the device that carries more current has a higher power dissipation and junction temperature. This is mitigated by three factors:

a. Fairly extensive testing has shown that the current unbalance tends to diminish as the current increases. This is because the voltage drops tend to converge as current increases. Very large unbalances at low current become small unbalances at high current.
b. Tight thermal coupling between dice insures that temperature differentials are contained within few degrees, in spite of significant unbalances.
c. IGBTs with slightly positive temperature coefficient have been widely available for a number of years. They are the devices of choice when paralleling is required.

Switching unbalance: The IGBT that carries more current will also be switching a higher current. Hence, it has higher conduction, as well as higher switching losses.

Thus, it would appear that a regenerative process is in place that will quickly take the junction temperature of the IGBT with lower conduction losses (higher current) beyond its rated limits and that this regenerative process is accelerated by the operating frequency.

However, analytical and experimental analysis has shown that, as the current increases, the current unbalance decreases and temperature unbalances decrease to a few °C. This is mostly due to the converging voltage drops at higher currents and the resulting reduction in unbalance.

Device selection is an effective method to reduce de-rating that is normally associated with paralleling. A significant contributor to unbalance is a difference in threshold voltage, particularly with trench IGBTs. Matching $V_{CE(on)}$ and $V_{GS(th)}$ is an effective way of reducing conduction and switching unbalances.

In addition to the screening suggested in the previous paragraph, it is advisable to follow the following guidelines mentioned in AN-941:

- Use individual gate resistors to eliminate the risk of parasitic oscillation.
- Ensure that paralleled devices have a tight thermal coupling.
- Equalize common emitter inductance and reduce it to a value that does not greatly impact the total switching losses at the frequency of operation.
- Reduce stray inductance to values that give acceptable overshoots at the maximum operating current.
- Ensure the gates are looking into a stiff (voltage) source with as little impedance as practical.
- Zener diodes in gate drive circuits may cause oscillations. When needed, they should be placed on the driver side of the gate decoupling resistor(s).
- Capacitors in gate drive circuits slow down switching, thereby increasing the switching unbalance between devices and may cause oscillations.
- Stray components are minimized by a tight layout and equalized by symmetrical position of components and routing of connections.