600 V CoolMOS™ G7 and 650 V CoolSiC™ G6 come in a new top-side cooling package – the DDPAK

A new option for integration

About this document

Scope and purpose

This document describes Infineon's new top-side cooled Double DPAK (DDPAK) Surface Mount Device (SMD) package for HV applications, fitted with the high-performance 600 V CoolMOS™ G7 Superjunction (SJ) MOSFET and 650 V CoolSiC™ G6 Schottky diode technologies. The major advantages of a top-side cooled SMD package for high voltage and high-power applications are the possibility of increasing power density to the next level, to enable low parasitic switching, and reduced PCB temperatures, which you can read about in detail in the following chapters. The document will focus on applying CoolMOS™ and CoolSiC™ in the high voltage DDPAK SMD package to increase power density and optimize switching performance.

Intended audience

For SMPS designers and engineers who want to improve their HV applications to achieve increased power density and the highest energy efficiency.

Keypoints

- Explains how top-side cooled DDPAK enables higher power density and thermal decoupling in high-voltage SMPS designs
- Describes assembly guidelines, soldering profiles, and cooling concepts for reliable integration of DDPAK packages
- Provides thermal performance insights, including R_{thJC} improvements and interface material selection for optimized heat management
- Demonstrates efficiency benefits of 4-pin Kelvin source configuration in PFC and LLC topologies
- Summarizes application results showing compact form factor and compliance with high-efficiency standards in server power supplies

About this product family

Product family

Infineon's CoolMOS™ is a high-voltage N-channel silicon power MOSFET that is designed to provide excellent thermal performance, lowest switching and conduction power losses, and optimal RDS(on) for increased system efficiency, supporting a range of application from low power levels to high power levels.

Infineon's CoolSiC™ MOSFET offer exceptional performance in switching behavior and total losses. These devices are designed to offer high efficiency and optimal reliability, while also boasting a low on-resistance that remains stable and reproducible even in large-scale production. Its ability to turn off the device with zero gate bias makes the CoolSiC™ transistor concept the only true "normally-off" device.

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About this product family

Target applications

- Consumer electronics
- Industrial applications
- Home appliances
- Server
- Telecom
- Renewables
- Energy Storage Systems
- Industrial drives
- Motor control and drives
- UPS

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1 Introduction

The last decade of SMPS development was dominated by the trend toward higher power density and cost optimization.

Fastest switching, highest efficiency, optimized board space at minimized Total Cost of Ownership (TCO) are among the critical challenges facing today's power supply designers. By driving down on-state resistance, improving gate charge and reducing switching losses the latest SJ MOSFET technologies in combination with the improved CoolSiC™ diode technologies hold the key to addressing these challenges in modern hard- and soft-switching applications.

Until now the most common packages on the market were the well-established Through-Hole Devices (THDs), such as TO-220 and TO-247. Based on the steadily increasing requirements in the semiconductor market a trend toward using SMD packaged devices to support fast-switching and reduce the parasitic inductance associated with the long leads on many THD packages can be seen. Despite all the advantages of the available SMDs, they still present a significant challenge with regard to cooling. This remains one of the major challenges for high-power Power Factor Correction (PFC) circuits and is the main reason that TO-220 and TO-247 are still the main package types used for high-power SMPS applications. In the DC-DC stage, like LLC or ITTF, SMD packages have already been used for years.

This application note describes how the DDPAK in combination with the latest 600 V CoolMOS™ G7 and 650 V CoolSiC™ G6 technologies offers the possibility to move away from through-hole packages toward SMD solutions, and further shapes the trend of highest efficiency and power density levels by enabling:

- The very first top-side cooled SMD system solution for high-power PFC circuits
- The very first top-side cooled SMD high-end efficiency MOSFET solutions for soft-switching topologies such as LLC

1.1 Target applications and topologies

Infineon's 600 V CoolMOS™ G7 SJ MOSFET technology in general addresses the high-end efficiency market by offering best-in-class switching performance and highest efficiency levels. It is designed to address high-power SMPS applications such as server and telecoms, PC power and solar.

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Introduction

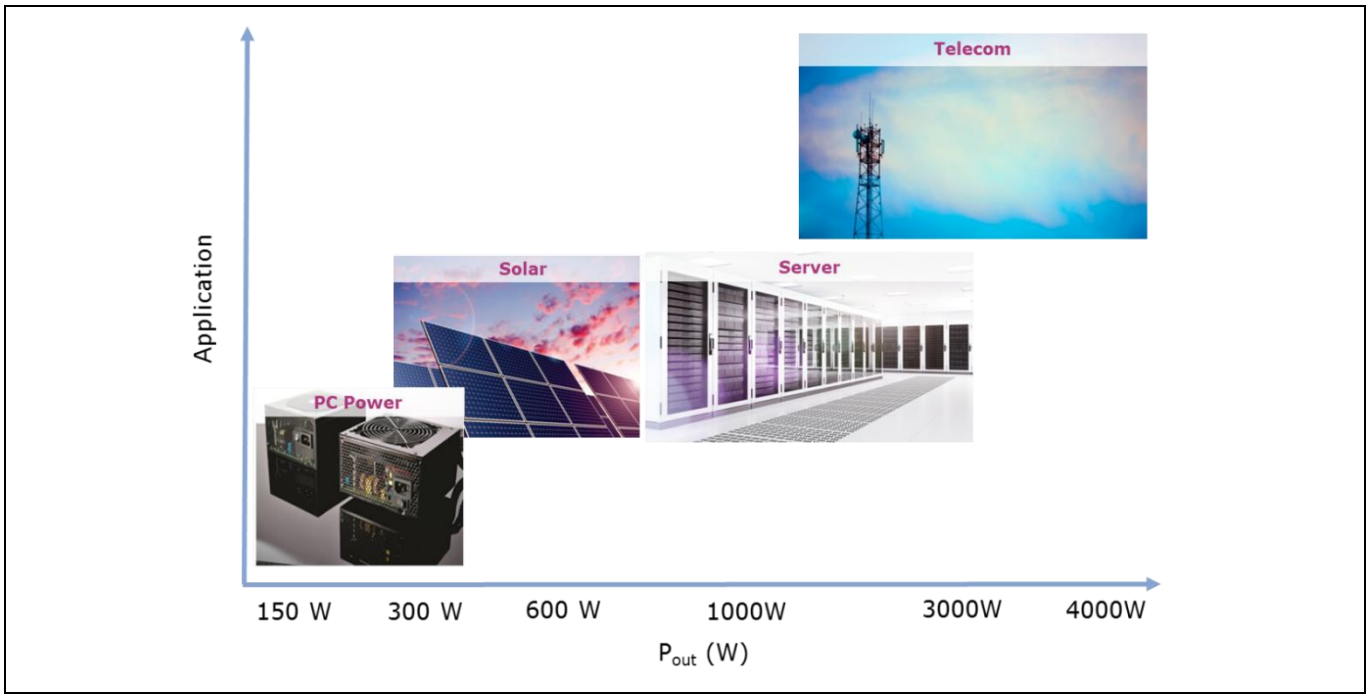


Figure 1 Target applications for the 600 V CoolMOS™ G7 DDPAK

The 600 V CoolMOS™ G7 technology, besides hard-switching topologies like PFC, is also suitable for high-end LLC designs. In the PFC stage Infineon offers a system solution by combining its CoolMOS™ 7 families with the latest 650 V CoolSiC™ G6 Schottky diode. To drive the 600 V CoolMOS™ G7 to its best performance we recommend the combination of CoolMOS™ with Infineon's EiceDRIVER™ products including driver solutions for hard- and soft-switching topologies. As the DDPAK comes with 4-pin functionality the perfect fit is the single-channel low-side gate-driver family with truly differential inputs (1EDN7550/1EDN8550) which can offer +/-150 V dynamic ground shift and +/-70 V static ground shift immunity. The whole system offering is completed by the LV OptiMOS™ and several different controller products.

More information can be found at:

- Driver – www.infineon.com/gatedriver
- OptiMOS™ – www.infineon.com/optimos
- Controller – www.infineon.com/controller

Introduction

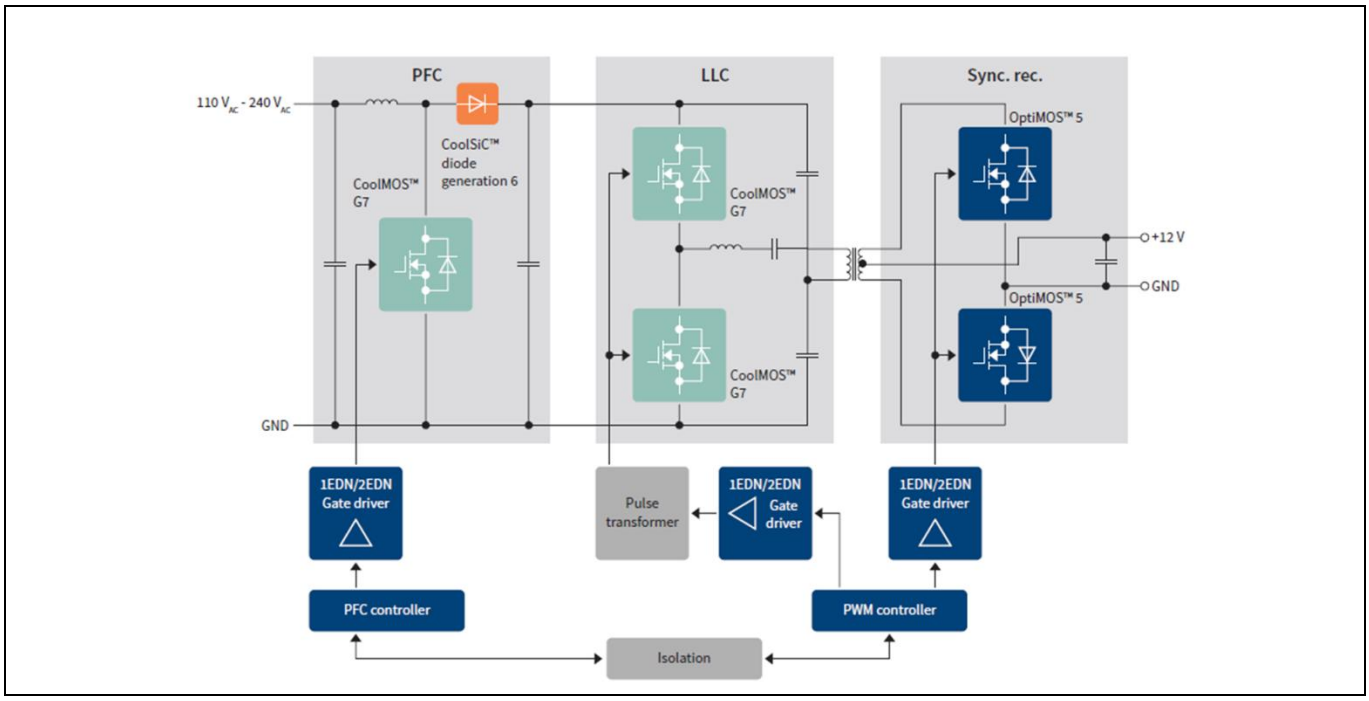


Figure 2 600 V CoolMOS™ G7 DDPAK addresses hard-switching as well as soft-switching topologies

As shown in Figure 2, Infineon offers a full system solution to enable fully optimized and balanced AC-DC conversion.

1.2 600 V CoolMOS™ G7 performance

The G7 silicon technology is based on the well-known 650 V CoolMOS™ C7 that was introduced in early 2013. Since then, continued development has further improved the technology. One of the major evolutions of the C7 technology is the reduction of energy stored in the output capacitance of the MOSFET (E_{oss}), as seen in Figure 3. For hard-switching applications this energy is always lost because it is converted into heat once the device is turned on the next time with a positive gate signal. All the improvements offered by the G7 technology result in reduced switching losses and, very importantly, also in reduction of the thermal resistance (R_{thJC}) of the device.

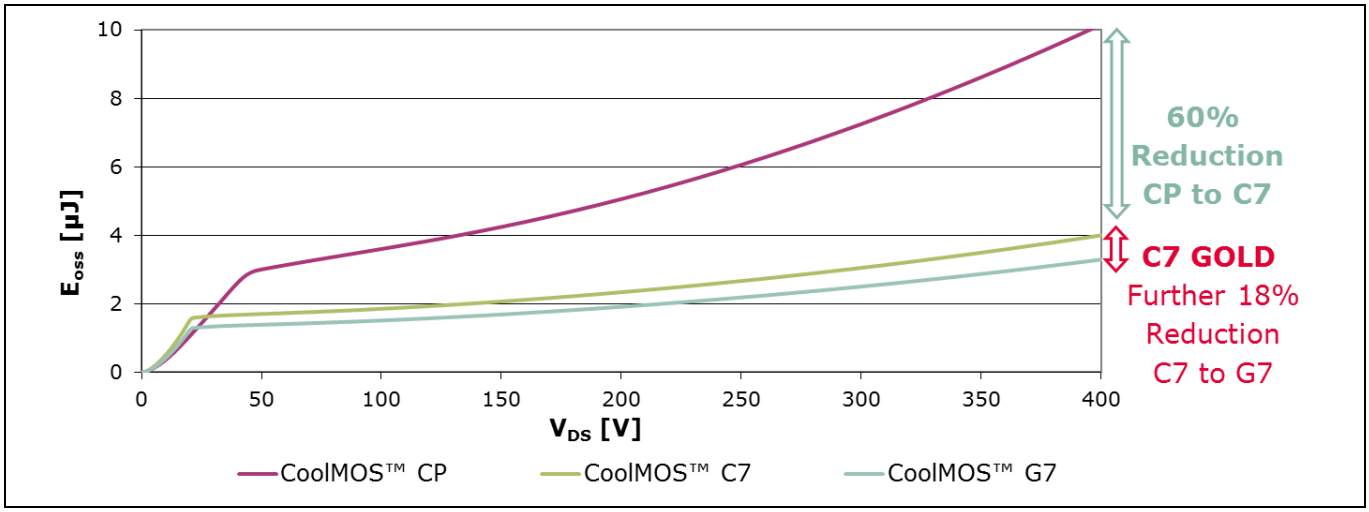


Figure 3 Stored E_{oss} in the output capacitance for different technologies

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The new G7 will be available with $R_{DS(on)}$ from 50 mΩ up to 190 mΩ. The 50 mΩ devices offer the best-in-class $R_{DS(on)}$ for a DDPAK device worldwide. It is the perfect use case for a high-power hard-switching PFC as well as for low switching and conduction loss-dominated bridge-rectifier replacement.

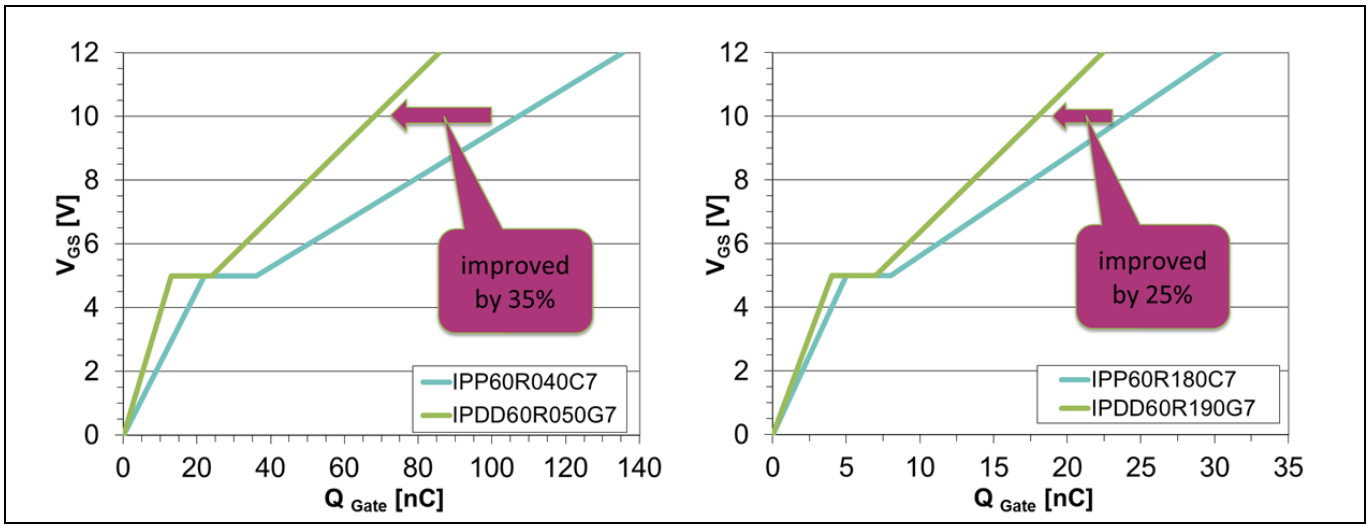


Figure 4 E_{oss} comparison for 50 mΩ and 190 mΩ

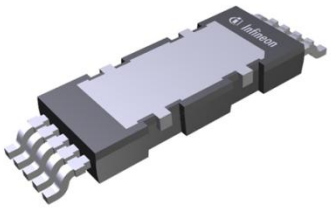
The E_{oss} reduction has a very high impact on the performance of conventional PFC topologies where the hard-switching of the MOSFET is dominant. For this application the E_{oss} energy will turn into power losses during the turn-on phase of the switch. The higher the switching frequency the more impact this performance improvement will have on overall energy efficiency.

In fact, the switching losses of the 600 V CoolMOS™ G7 are reduced similar to the $R_{DS(on)}$ step within the 600 V CoolMOS™ C7 technology. This means that the 50 mΩ G7 device exhibits the same switching losses as the 40 mΩ C7 devices. It is now possible to use (for the same power range) one step lower $R_{DS(on)}$ to reduce the overall power losses but retain the same light-load efficiency. Nevertheless, a different and adapted thermal concept has to be accepted to guarantee the best possible system performance.

1.2.1 G7 DDPAK portfolio

The latest-generation 600 V CoolMOS™ G7 comes in the new DDPAK SMD package, meeting the needs of future markets.

CoolMOS™ G7	
$R_{DS(on)}$ max. [mΩ]	Part name
190	IPDD60R190G7
150	IPDD60R150G7
125	IPDD60R125G7
102	IPDD60R102G7
80	IPDD60R080G7
50	IPDD60R050G7



Package dimensions: 21.1x6.6x2.35mm (LxBxH)

Figure 5 G7 DDPAK portfolio

1.3 650 V CoolSiC™ G6 Schottky diode performance

Infineon's 650 V CoolSiC™ G6 Schottky diodes deliver the best price-performance and customer value in the market, leveraging advanced silicon carbide production facilities, a solid track record, the highest quality, and a very granular and complete combined G5/G6 portfolio.

Targeting high-power SMPS applications such as server and telecoms, PC power and solar, the latest-generation 650 V CoolSiC™ G6 diodes have many suitable applications.

The performance measurements of the 650 V CoolSiC™ G6 diodes were carried out using the 800 W Platinum® server evaluation board from Infineon, which can be found on the Infineon support pages.

- Board support page - (EVAL_800W_130PFC_C7)

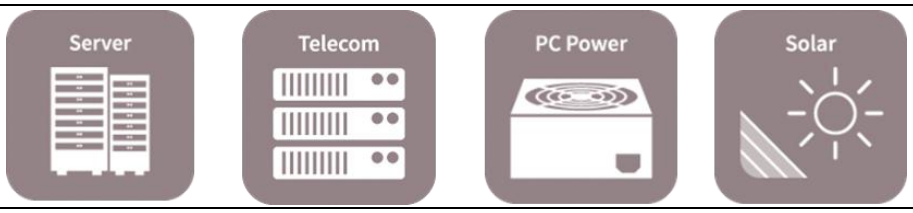


Figure 6 Target applications for CoolSiC™ diodes

1.3.1 Price–performance

Infineon has engaged in a consistent technological effort to make CoolSiC™ diodes cheaper and also perform better across several generations (Figure 7).

Introduction

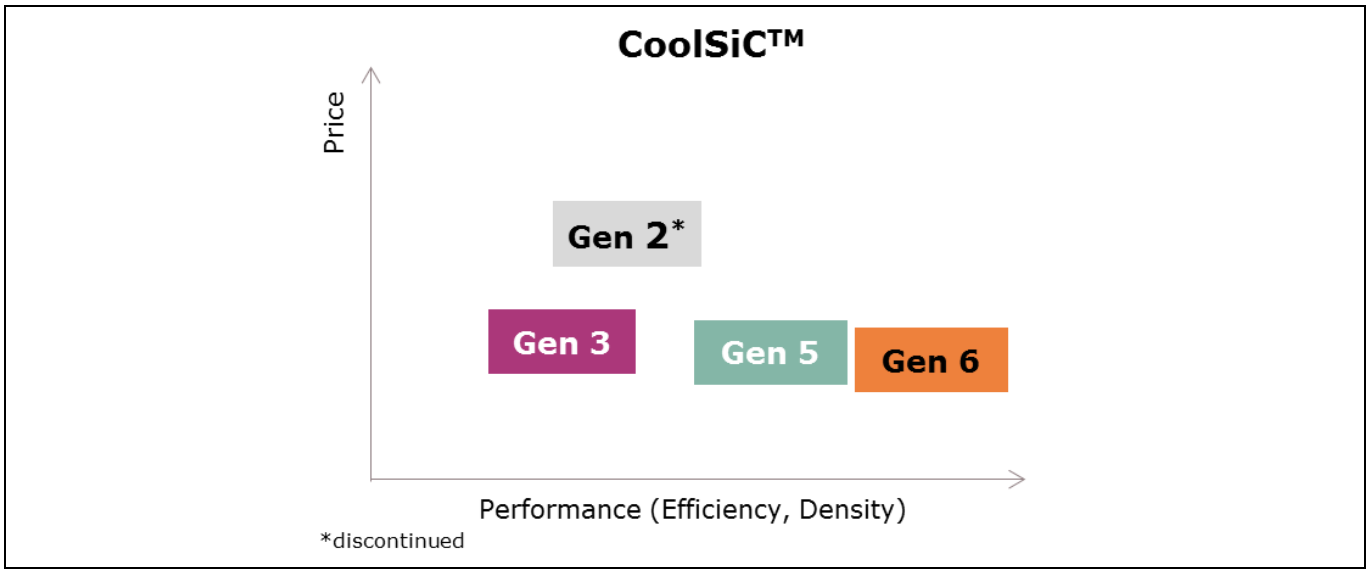


Figure 7 Price-performance illustration of CoolSiC™ diodes

1.3.2 Lowest V_F across all generations

Several studies have proven that the lower forward voltage of the Schottky diode is a key parameter in achieving high efficiency and consequently improving high-density PFC designs.

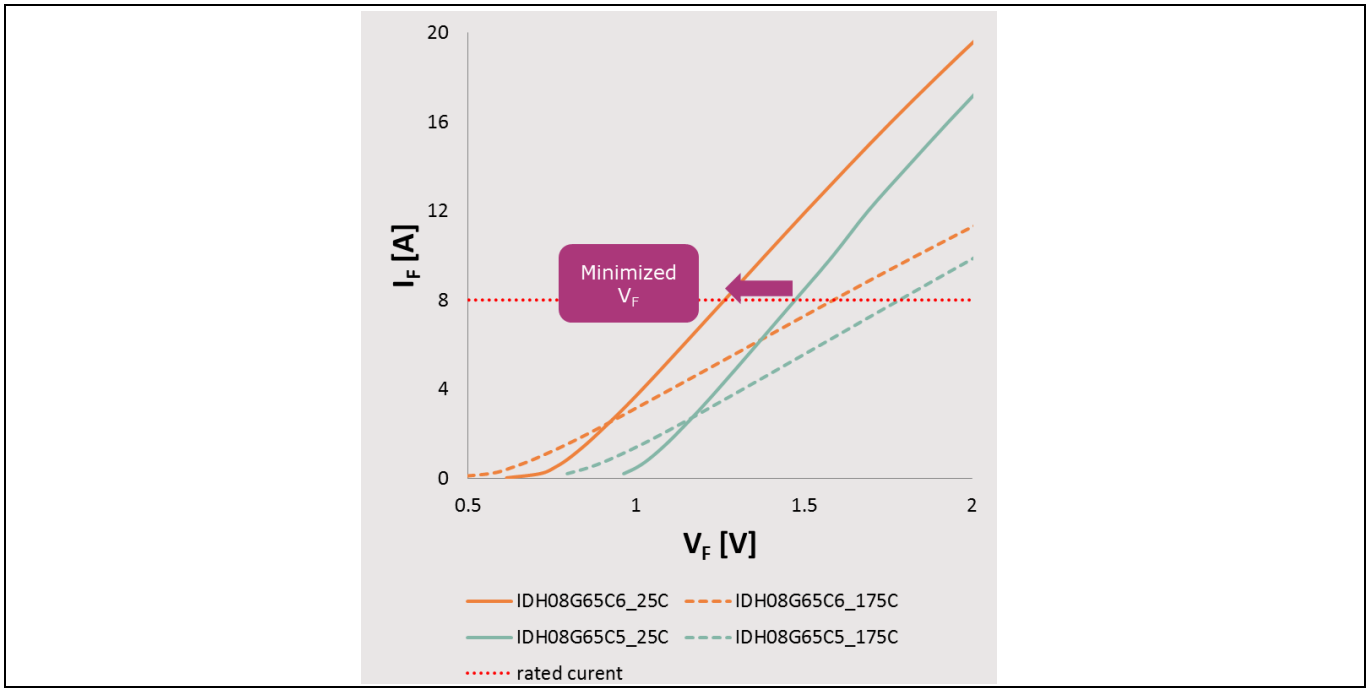


Figure 8 I_F vs. V_F of 650 V CoolSiC™ G6 diode

The lower forward voltage of the 650 V CoolSiC™ G6 Schottky diode enables lower conduction losses, which help to achieve:

- Higher efficiency
- Lower junction temperature of the device

Introduction

The Schottky diode enables shaping of the efficiency curve with selection of the proper diode current rating. Furthermore, with world record V_F = 1.25 V (1.5 V at 150°C) the latest generation sets a new benchmark on the market (Figure 8).

The power supply designer can therefore optimize cost and efficiency according to the application requirements by choosing the correct diode and the right current rating.

Additionally, thermal analysis gave better results for the 650 V CoolSiC™ G6 Schottky diode thanks to the lower forward voltage drop V_F, and consequently lower conduction losses. Although the 650 V CoolSiC™ G6 has increased thermal resistance R_{th}, the sixth generation remains cooler than the previous generation thanks to lower conduction losses and established diffusion soldering process.

1.3.3 Lowest Figure of Merit (FOM) $V_F \times Q_c$

With the latest generation of diodes, the FOM $V_F \times Q_c$ was also further improved and is benchmarked within all Infineon generations (Figure 9), adding to their performance against competitors.

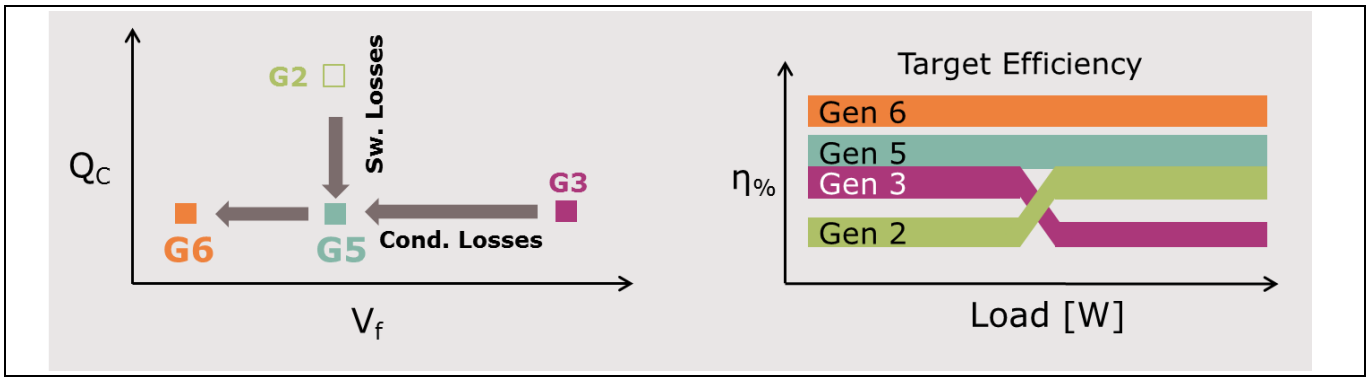


Figure 9 FOM $V_F \times Q_c$ CoolSiC™

To summarize the value for the customer, the 650 V CoolSiC™ G6 Schottky diode delivers:

- Outstanding efficiency and enabling higher power density
  - A best-in-class FOM, reduced by around 17 percent, results in more efficiency under all load conditions compared to the fifth generation
- Cost-effectiveness
  - Lower price and system cost compared to previous CoolSiC™ generations, with an increase in efficiency
- Highest quality and reliability
  - Based on previous CoolSiC™ generations, failure in time (FIT) rate of ~0.2, and only five failures over 60 million shipped parts
- Ease of system integration
  - Designed to complement our latest 650 V and 600 V CoolMOS™ C7, G7, and P7 families, meeting the most stringent application requirements

1.3.4 CoolSiC™ Schottky diode portfolio

The latest generation of CoolSiC™ diodes is aimed at leaded and SMD packages, meeting the needs of existing and future markets.

CoolSiC™ G6	
Amp [A]	Part name
4	IDDD04G65C6
6	IDDD06G65C6
8	IDDD08G65C6
10	IDDD10G65C6
12	IDDD12G65C6
16	IDDD16G65C6
20	IDDD20G65C6

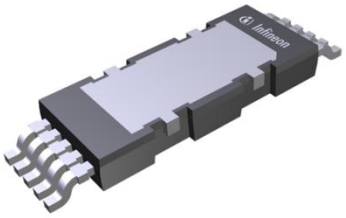


Figure 10 650 V CoolSiC™ G6 diode DDPAK

- For information and collaterals, visit: https://www.infineon.com/coolsic
- Additional benchmarking is available inside all demo board application notes from CoolSiC™ G5/6 and 600 V CoolMOS™ G7: https://www.infineon.com/demoboards

2 DDPAK package as a perfect fit for MOSFET and diode

CoolMOS™ and CoolSiC™ in the DDPAK package enable a new approach to systems in high-power SMPS solutions with top-side cooled SMDs.

This powerful combination for the first time enables the following options:

- Top-side cooled SMD system solution for PFC topologies
- Top-side cooled SMD high-end efficiency MOSFET solution for LLC topologies

2.1 DDPAK dimensioning and SMD “replacement” for TO-220

The DDPAK (PG-HDSOP-10-1) package is the latest Infineon SMD package optimized for high-power, HV and high-reliability applications with the benefit of top-side cooling.

The package is suitable for containing either MOSFETs or SiC diodes, leading to a new direction in terms of system integration.

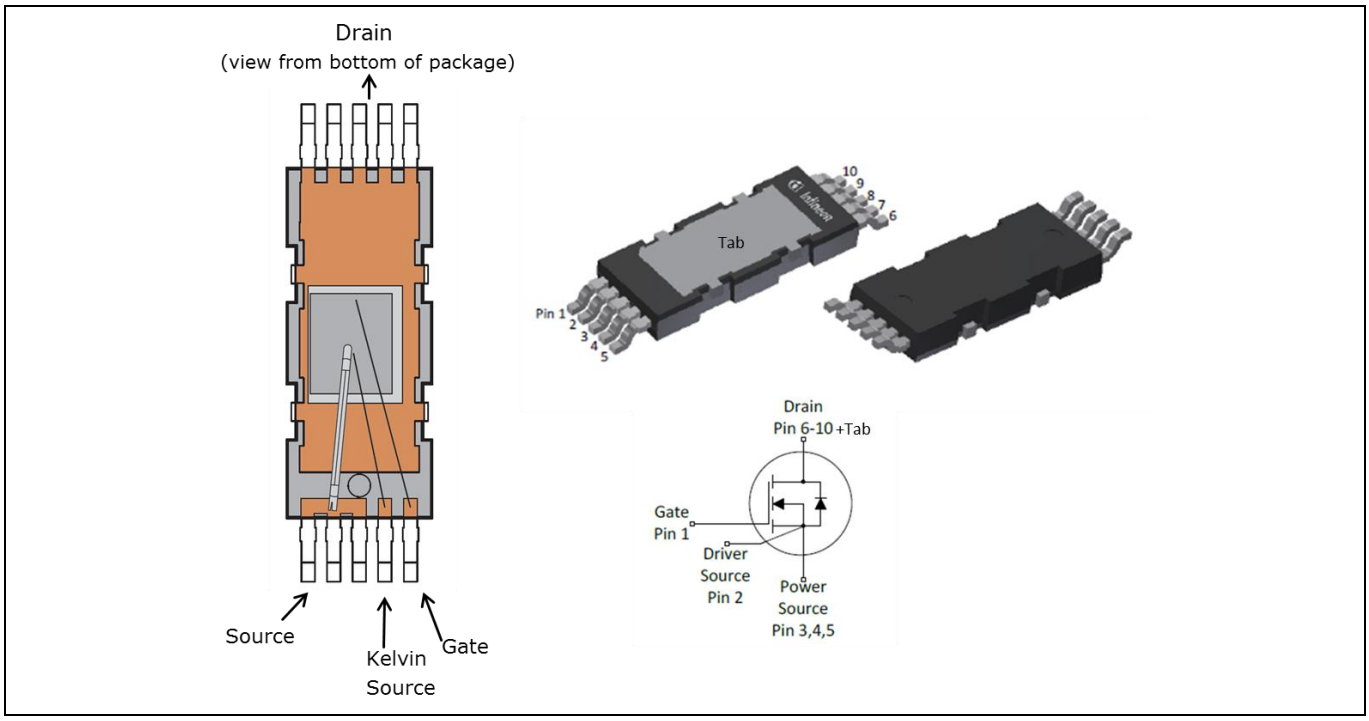


Figure 11 DDPAK drawing (inside view showing bottom, top and pin-out)

One of the best aspects of the DDPAK package is the Thermal Cycling On Board (TCOB) reliability – especially when focused on FR4 PCB assembly. See Section 4.3 for more information on TCOB.

All mechanical details shown in the following chapters and a general recommendation for how to handle Infineon’s SMDs can be found at www.infineon.com/packages.

Detailed mechanical information about the DDPAK (PG-HDSOP-10-1) is also available at http://www.infineon.com/smd-topsidecooling.

In terms of replacing a lead package, the height and width of the new solution are important; see the benefits of a top-side cooled package in the comparison below (Figure 12).

A new option for integration

DDPAK package as a perfect fit for MOSFET and diode

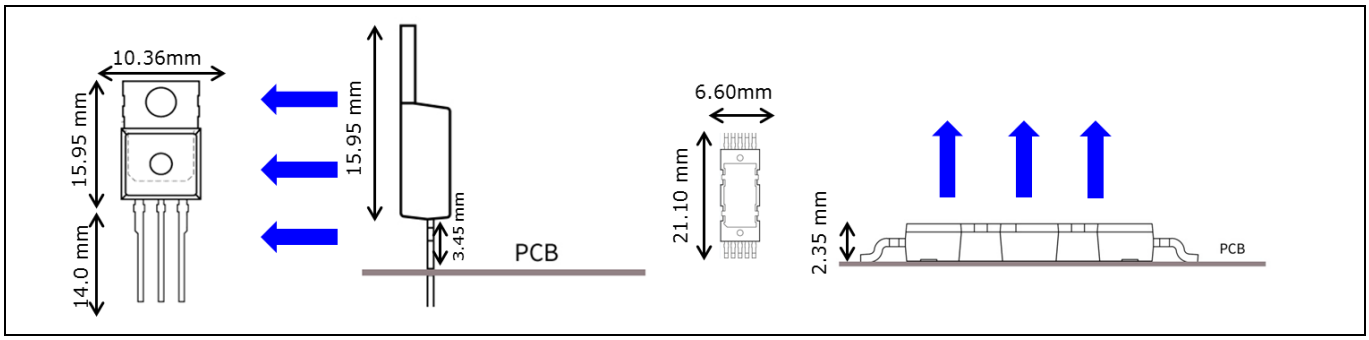


Figure 12 Size comparison – TO-220 vs DDPAK

It's clear that a switch from a lead package to an SMD package benefits from smaller form factor and less height but requires different cooling concepts.

Whether horizontal or vertical, the positioning inside the SMPS is most often driven by the cooling concept. With the new top-side cooled DDPAK, new methods of cooling and new form factors can be factored into the design.

In the following table (Figure 13), you can see the main differentiators between a standard TO-220 package and the DDPAK.

Parameter	TO220	DDPAK	Comparison
Height [mm]	19.40 mm	2.53 mm	86% height reduction
Thickness	4.75mm	2.53mm	46% thickness reduction
Cooling area [mm²]	118 mm²	56 mm²	50% less cooling area
Rthjc* [°C/W]	1.83 °C/W	1.65 °C/W	10% less Rthjc
Inductance	8nH	4nH	50% less inductance

*for Rthjc IPP60R180C7 and IPDD60R190G7 are compared

Figure 13 Parameter comparison – TO-220 vs DDPAK

The reduction of height and inductance gives the designer the opportunity to make the design much thinner and much more power dense.

The reduced cooling area seems to be a drawback at first, but with the reduced R_{thJC} (which is directly related to the heat transfer from chip to package) the major portion of the lower area in the application itself, with a proper cooling concept (as shown in the application section later on), results in nearly equal performance, with the benefit of a much more compact realizable size.

In the thermal design of the power board a lot of boundary conditions must be considered. A thermal optimization on the MOSFET level in a dedicated application requires the lowest possible thermal resistance of the overall system (R_{thja}) in combination with the highest possible junction temperature (T_j) of the switching devices.

This can be achieved through:

- Maximizing the heat flow into the heatsink

- Minimizing the heat flow into the PCB

This normally requires a THD and limits the use of SMDs, but with the DDPAK approach and the top-side cooling concept, a new power density integration solution is enabled (see Figure 14).

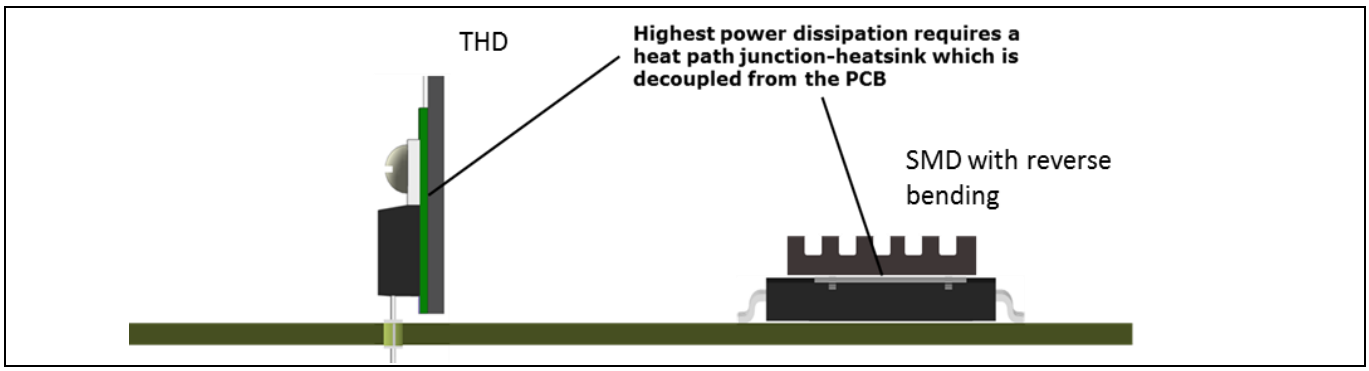


Figure 14 Thermal design – THD vs SMD

2.2 R_{thjc} improvement

The thermal resistance (R_{thJC}) of the device is a very important measure for the cooling performance of the device. The R_{thJC} improvement of G7 is shown in Figure 15. For the same $R_{DS(on)}$, there is a 20 percent improvement achieved.

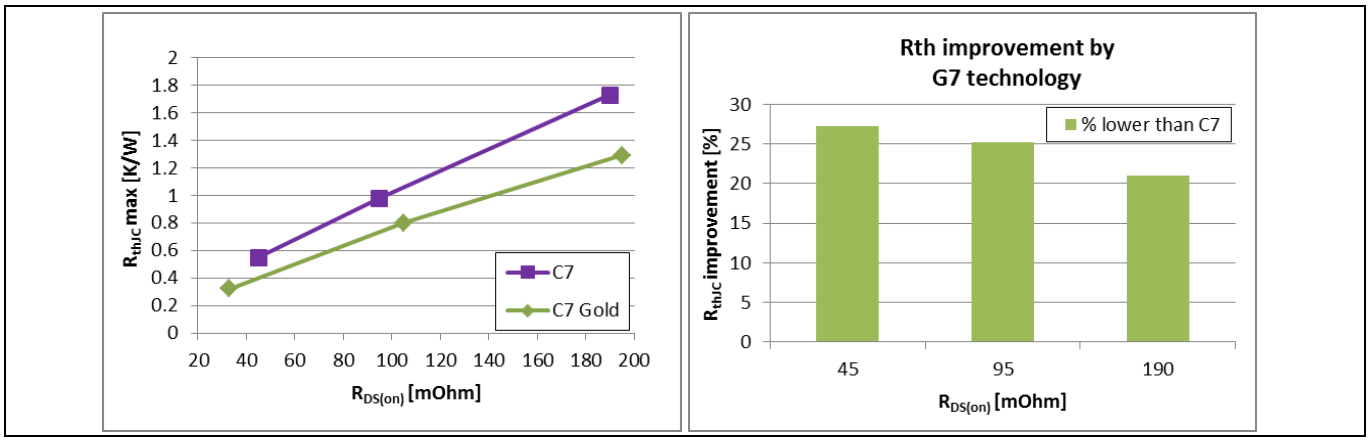


Figure 15 R_{thJC} vs. $R_{DS(on)}$ comparison between C7 Gold in the DDPAK and C7 TO-220 package

The R_{thJC} improvement shown in Figure 15 results (according to the equation shown in Figure 16) in lower silicon temperatures for same level of heat transfer or power losses. The chart on the right shows the normalized improvement as a percentage based on interpolated $R_{DS(on)}$ for the G7 devices against the $R_{DS(on)}$ the C7 technology offers. This will result in lower $R_{DS(on)}$, as the $R_{DS(on)}$ significantly increases with the temperature of the device.

$$R_{thJC} = \frac{\Delta_T}{P_v} \gg \Delta T = R_{thJC} \times P_v$$

Figure 16 R_{thJC} impact on temperature difference

Knowing the lower temperature of the device it is possible to either reduce the cooling effort or to increase the power range for a given configuration.

Alternatively, a designer might consider increasing the reliability by maintaining a lower temperature within the system.

2.3 4-pin functionality

The DDPAK package offers five connections for the drain current, three connections for the source and one source sense connection for the gate-reference potential; additionally the single-pin connection for the standard gate driver (Figure 17).

This source-sense connection is designed for the gate charging power and should not be used to carry the main drain current as it does not have the current handling capability of the other six power source connections. It is possible to connect all the source (power and sense) connections together without using the 4-pin functionality of the package.

The most important reason to use a separate source sense pin for controlling the gate is to improve efficiency by reducing switching losses and therefore minimizing heat generation. Reducing switching time is a well-understood method for improving efficiency – the faster a switch turns on and off, shorter the time period during which a voltage exists across it and a current is flowing through it. Voltage multiplied by current is equal to power (loss), hence a switch that spends less time dissipating power is a more efficient switch.

As well as this important advantage of the 4-pin functionality, the gate waveforms will be much cleaner by using the source sense connection as the means of driving the gate, as the induced voltage peaks on the power source inductance will not feed back into the driving circuit as would happen in the standard configuration with only a single source connection to the MOSFET.

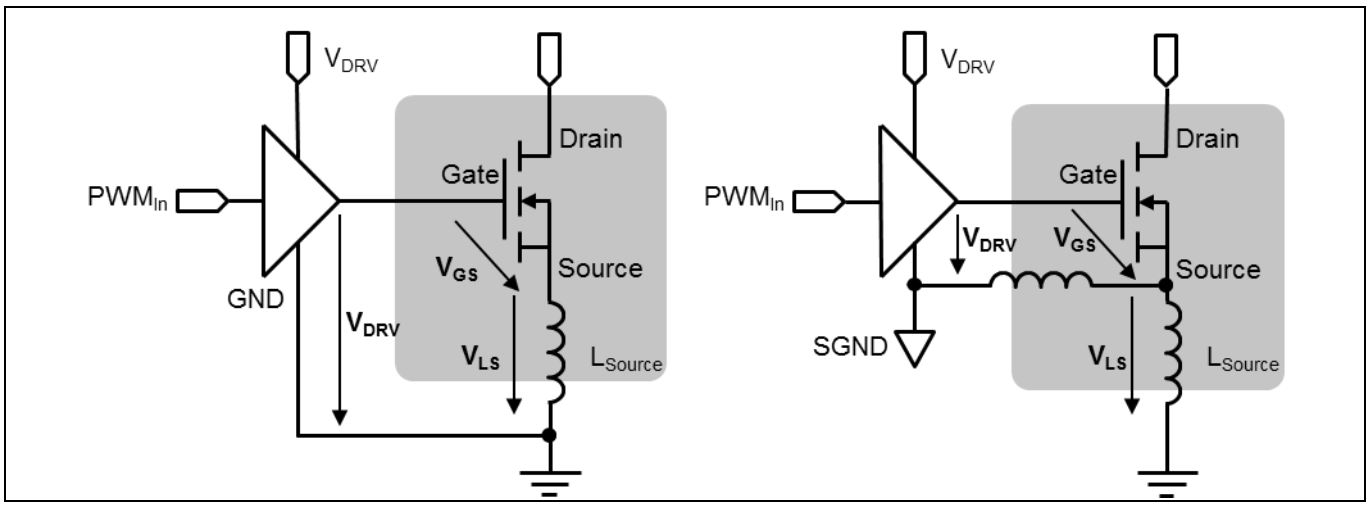


Figure 17 Driving scheme comparison for standard and 4-pin set-up

Due to the low pin inductance of the DDPAK package (approximately 4 nH) the bouncing of the signal ground is at a much lower level compared to the TO-220 package, where the source inductance is approximately 8 nH, which causes higher voltage peak at the turn-on and turn-off of the transition (Figure 16).

To sum up, with the separated “source sense” pin you will be able to reach higher efficiency levels at full load due to undisturbed signal to driver (see Figure 18 - magenta signal) and much lower parasitic switching due to the DDPAK package itself.

A new option for integration

DDPAK package as a perfect fit for MOSFET and diode

The evaluation has been performed in a special ringing test set-up to check the benefit of the sense source. The voltage across the drain-source of the MOSFET is shown in green, the driver signal in magenta, which shows in the range of 5 V to 6 V less over-shoot compared to the normal 3-pin packages, and the current in yellow.

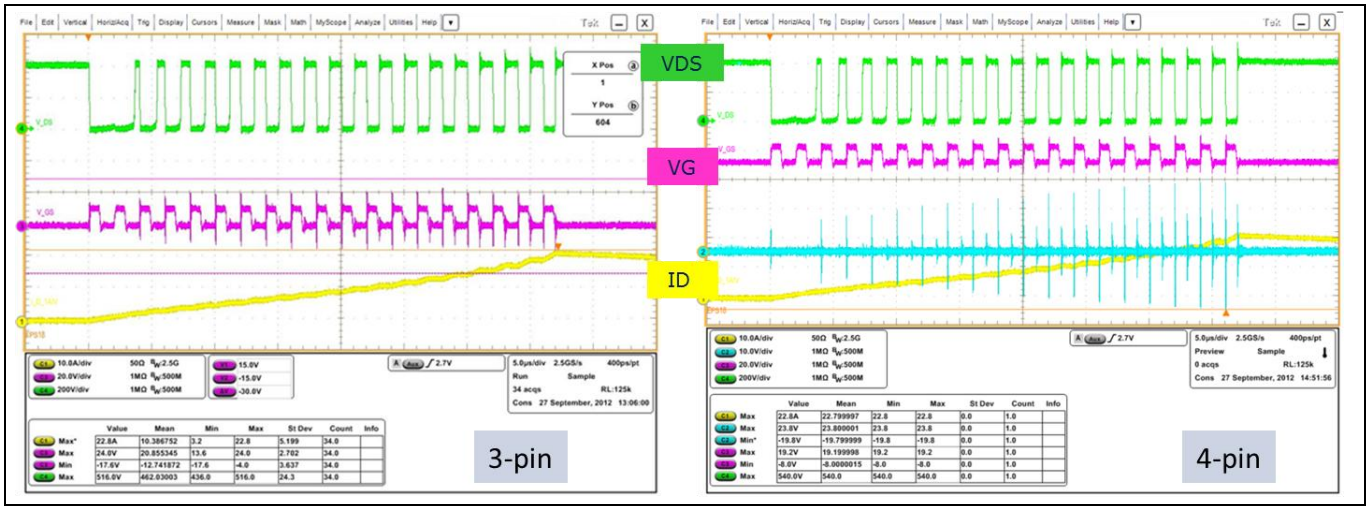


Figure 18 3- vs 4-pin waveforms (ringing test set-up)

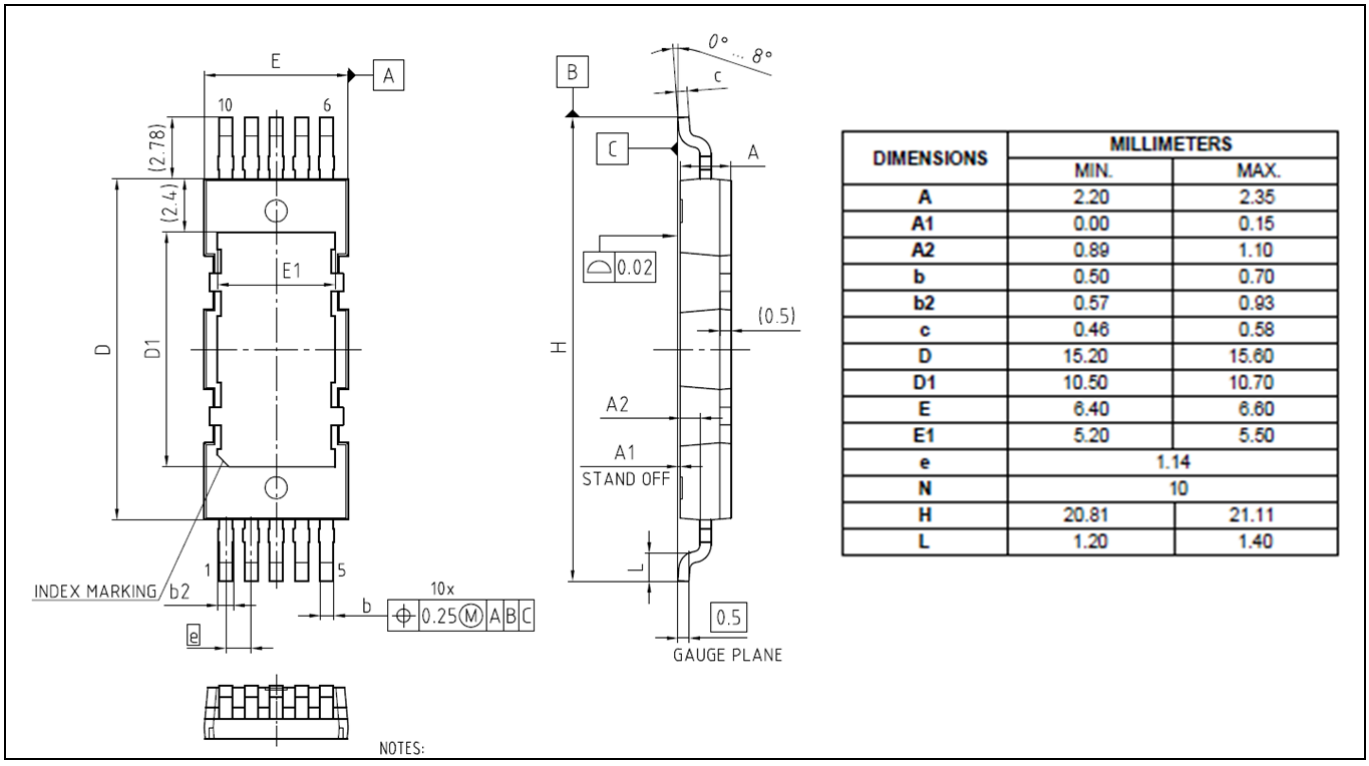
There is more detailed information about the 4-pin features and application considerations in various 4-pin application notes at www.infineon.com/4pin.

3 Assembly considerations for the DDPAK

The assembly process for SMDs offers advantages in mass production. Firstly, SMDs save space on the board, and secondly the placement can be automated while most THDs are inserted manually, which increases cost and reduces quality.

The PCB design and construction are key factors for achieving highly reliable solder joints. For example, TOLL packages should not be placed in the same location on opposite sides of the PCB (if double-sided mounting is used), because this results in a stiffening of the assembly, which can lead to earlier solder joint failure when compared to a design where the component locations are offset. Furthermore, it is known that board stiffness has a significant influence on the reliability (temperature cycling) of the solder joint, if the system is used in fluctuating temperature conditions. For a DDPAK package, this has no influence at all because package and PCB are decoupled, giving an advantage over other SMD variants.

The outline of the DDPAK device is shown in Figure 19. More detailed information about the physical dimensions is available in the relevant datasheets available on the Infineon website.



DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.20	2.35
A1	0.00	0.15
A2	0.89	1.10
b	0.50	0.70
b2	0.57	0.93
c	0.46	0.58
D	15.20	15.60
D1	10.50	10.70
E	6.40	6.60
E1	5.20	5.50
e	1.14	
N	10	
H	20.81	21.11
L	1.20	1.40

Figure 19 Outline drawing of the DDPAK (PG-HDSOP-10-1)

Figure 20 shows the recommended PCB pad designs (including appropriate dimensions) for the DDPAK. This design is also used for TCOB testing according to IPC9701 standards at Infineon.

Please note that the recommendations can only give dimensions for the solder-mask openings. Generally, the copper dimensions depend on the capability of the board manufacturer. For high-current applications, the copper dimensions for drain and source pads should be as large as possible to increase the conductor cross-sectional area.

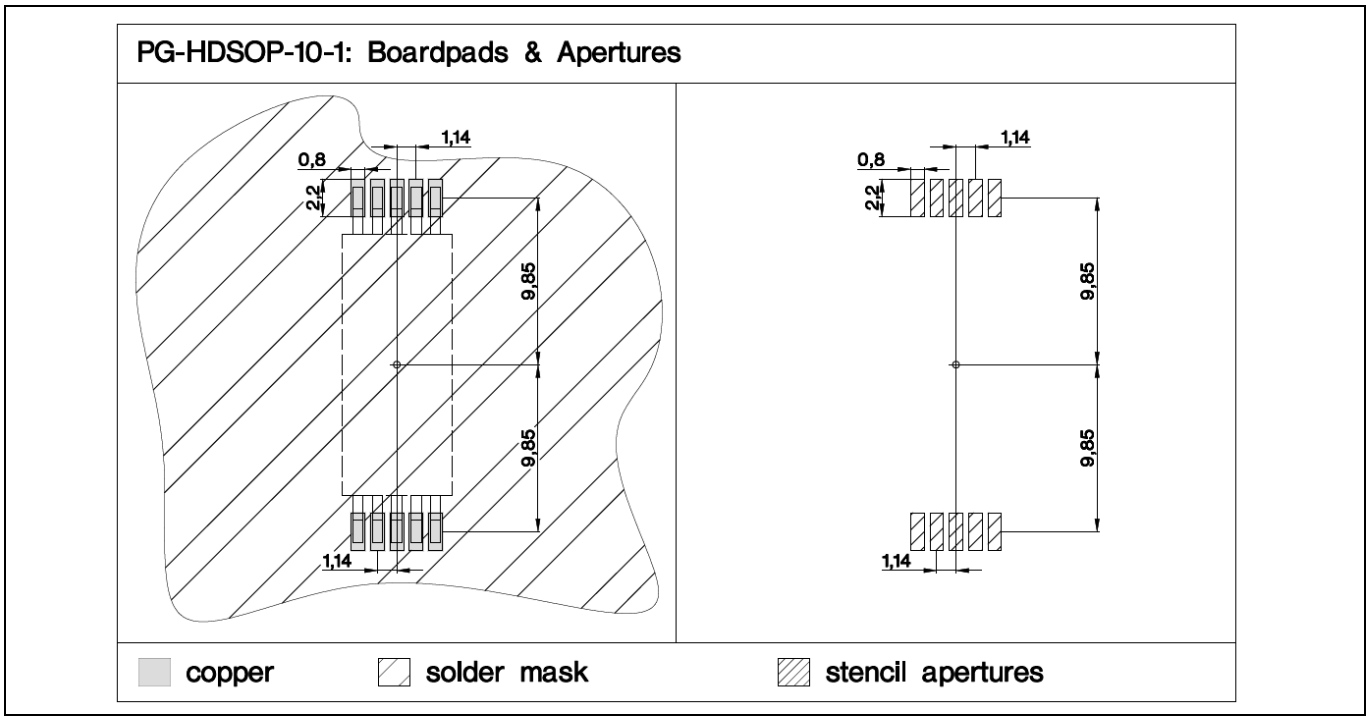


Figure 20 Footprint and stencil recommendation for PCB assembling

In Figure 20, the final footprint and stencil recommendations for the PCB assembly are shown. For more details and tolerances, check the last page of the final datasheets (also check the revision number) for the specific part in the dedicated DDPAK package.

The drain copper area on the top side of the DDPAK package further allows a direct soldering of the external heatsink. In Figure 20, the stencil recommendation can be found and an example build-up with the DDPAK soldered onto the PCB including a small copper heatsink on top is presented in Figure 22.

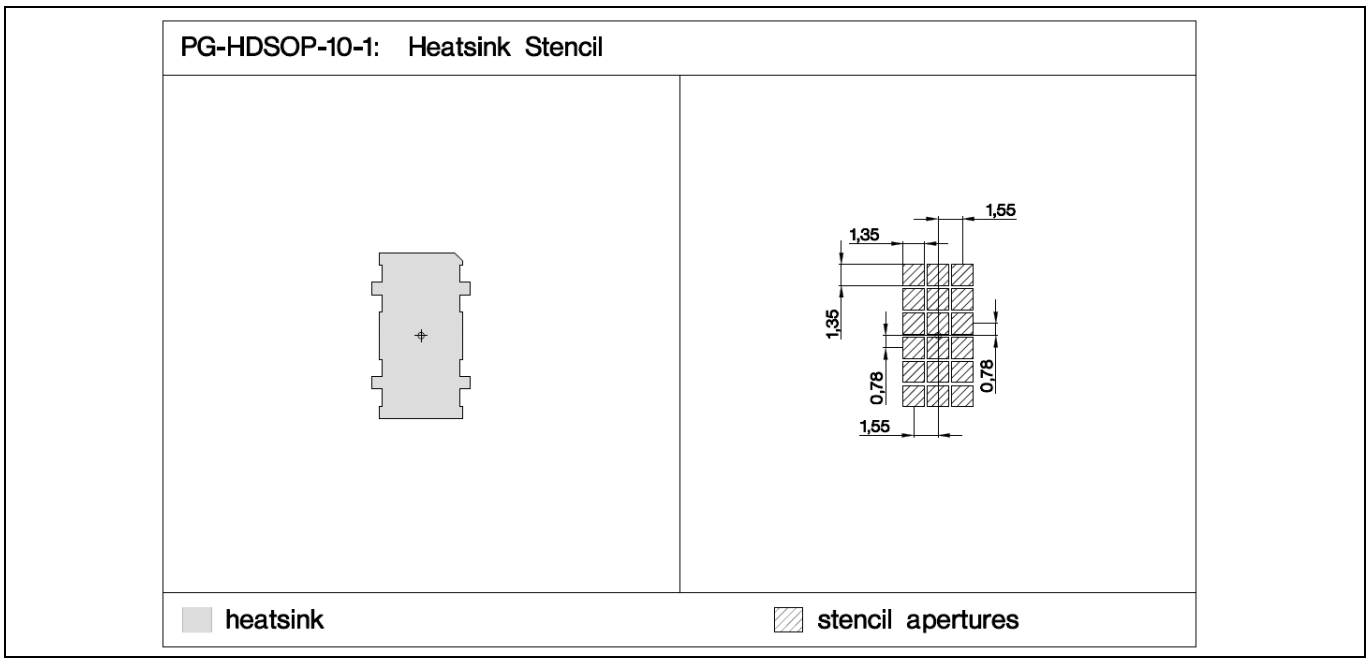


Figure 21 Stencil recommendation for top-side soldering (drain potential)

Details shown in Figure 21 can be understood as an Infineon recommendation for how to solder small heatsinks on the top side of this package while not destroying or shortening the package and its pins. Every soldering should be done in separate steps with time for cooling down to avoid making cracks in the material (see an example in the next chapter).

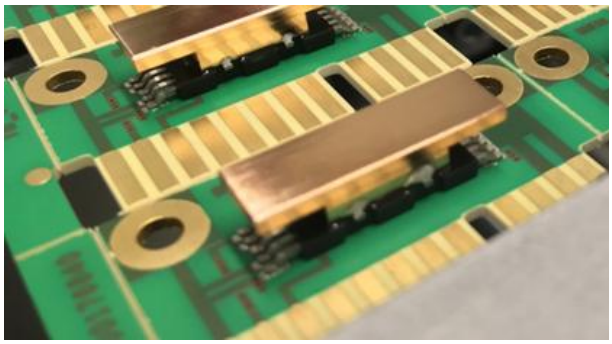


Figure 22 DDPAK soldering example with heat spreader on top side (drain potential)

It must be considered when soldering heatsinks or copper blocks that there is HV potential present on the top side (drain potential). Creepage and clearance requirements besides the isolation to housing should also be considered.

Furthermore, an eye must be kept on how a heatsink soldered on top of the package affects temperature cycling and weight. The temperature cycling on board level, short TCOB performance (see Section 4.3) must be checked in detail. With increased weight of the heatsink the TCOB performance will reduce since the package is only connected to the board via the pins.

3.1 Top-side soldering investigation (including profile)

The drain lead-frame can be used to connect several DDPAK MOSFETs in parallel by soldering a conductive heatsink on top of it. The next chapter explains step by step how this can be realized.

The test board and its dimensions are shown in Figure 23.

- Copper 35 µm
- PCB thickness 1.6 mm
- Standard FR4 PCB material

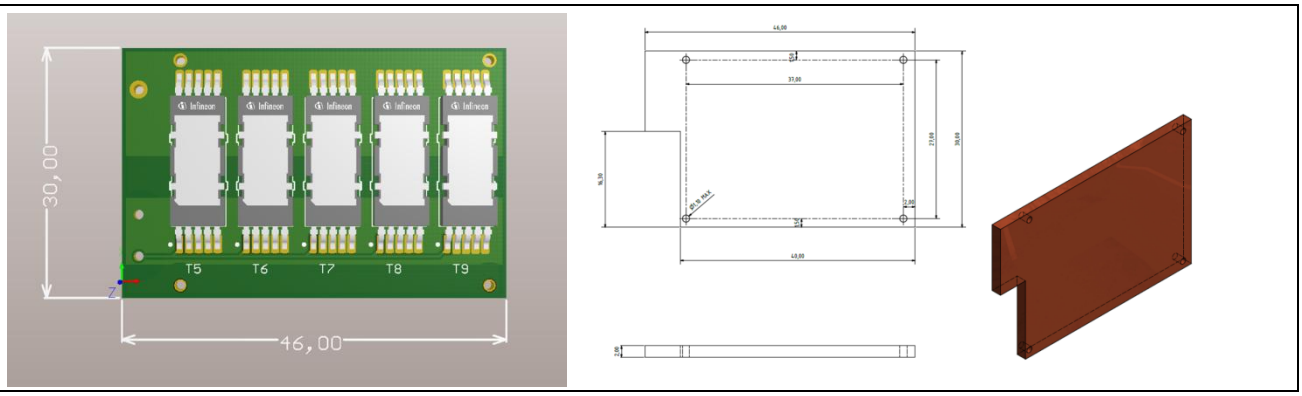


Figure 23 DDPAK top-side soldering evaluation board with copper plate

A new option for integration

Assembly considerations for the DDPAK

The top surface of the DDPAK allows heatsinks to be soldered to it as an additional step after soldering the package to the PCB. Therefore, the heatsink should be covered with tin (Sn) for better solder results. Pure copper showed worse results compared to the tinned one.

- Tin specification: Galvanic tin 99.9 percent

For special creepage and clearance requirements, ensure that the copper plate does not cover the connection pins of the package, or the pins covered earlier.

The module was soldered in a reflow oven with the profile as shown (Figure 24).

- Solder paste used: KOKI SnAg0.4Bi57.6
- Stencil thickness: 125 µm

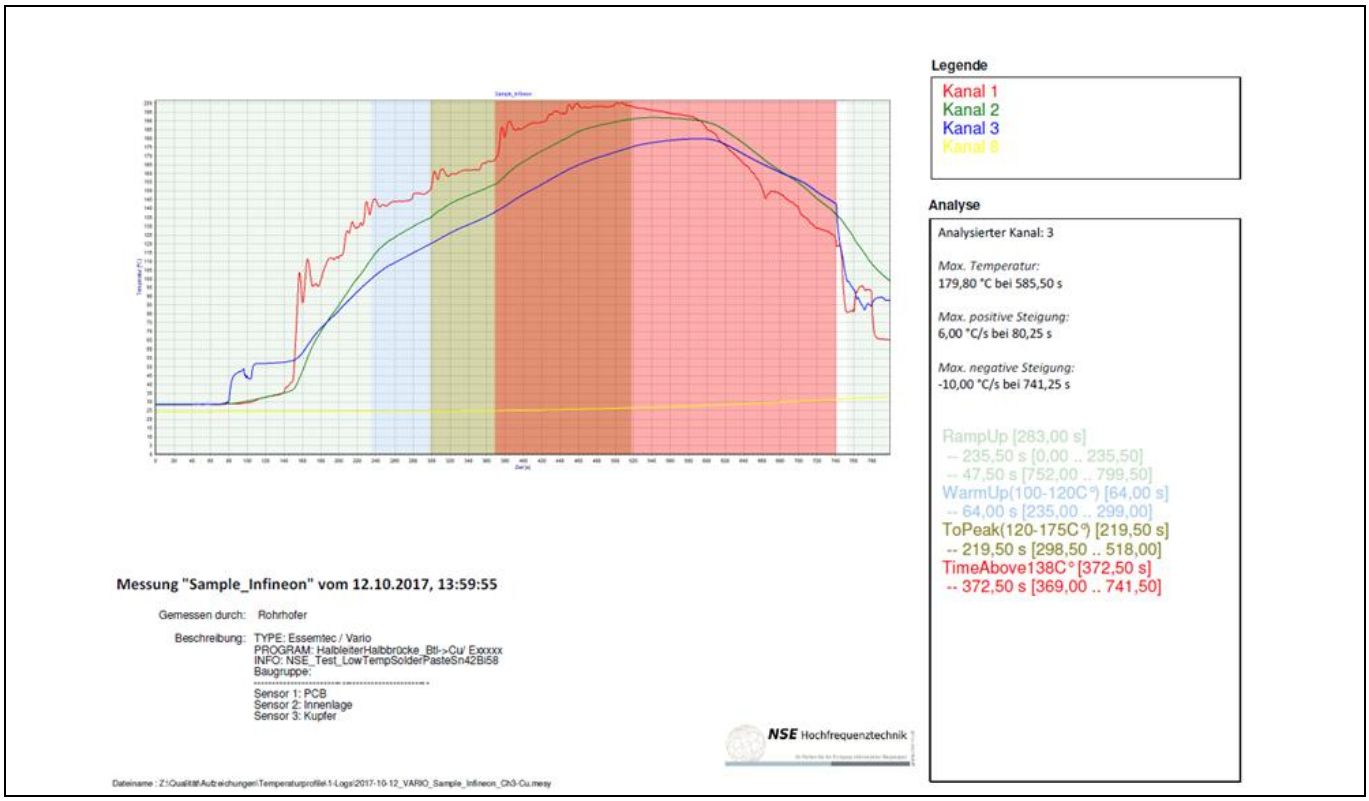


Figure 24 Solder profile heatsink on top

After applying the soldering process, the evaluation PCB was tested electrically and passed all tests. The copper plate is on HV potential (drain) and current transfer can now be done over several PCB layers, or the soldered copper material can be used as a high-power current path.

The best results were realized when the heatsink itself was pressed onto the packages (less than 10 kg). Also, an X-ray inspection was performed and showed an acceptable void.

3.2 Soldering specification (reflow)

As described in the last chapter, soldering of the DDPAK is possible, onto the PCB or combined with the heatsink on top. The only limitation is that wave soldering is not accepted and released with this package (only reflow soldering is allowed). The specification for soldering can be found in the dedicated datasheet of the product and is also shown in Figure 25.

Reflow soldering temperature	T_{sold}	-	-	260	°C	reflow MSL1

Figure 25 Reflow soldering temperature specification for the DDPAK package

What can happen if wave soldering is used without any special solder masks (as used when soldering SMDs combined with micro-controllers or processors) can be seen in Figure 26.

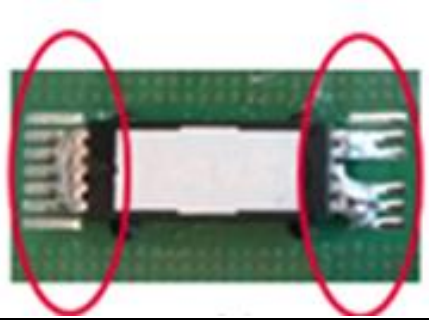


Figure 26 DDPAK experiment with wave soldering – short on pins (not allowed)

A possible solution to overcome the short-circuits on the pins (due to too-narrow pin distance) is the use of soldering masks, which are well established and already used in the market. These masks enable a selective wave soldering to hide the protected components under it.

But the DDPAK is not designed for this process, and it adds an additional step in the assembly procedure. Anything other than the designated soldering method (reflow) can lead to failures. The customer therefore proceeds at their own risk.

4 Thermal handling

In the last few years there has been a move from THDs to SMDs due to the need for increasing power density.

This trend is not only coming from the application side but also from the need to reduce costs and to fully automate mass production.

The integration density that has been achieved so far, as well as newly developed functions, results in very large amounts of lost heat.

This situation has become ever more critical as smaller packages will be used in future, which represents a problem in terms of heat dissipation (from package to surroundings, or external cooling area) and requires great innovation and creativity to achieve heat reduction.

There is now the difficulty that with high packing densities on the PCBs, the large copper areas required are not suitable for heat reduction and the SMD component advantage would disappear.

Therefore, the DDPAK, with its top-side cooling opportunity, not touching the PCB anymore, led to a new innovative possibility for getting rid of heat (see Figure 27).

The system can be driven to higher power levels compared to other SMD packages (e.g. TOLL) while not violating e.g. FR4 thermal limits since the package body is decoupled from the PCB. On the right side a thermal picture was taken to show the homogeneous heat spreading through the package, driving the package to its limits (not application relevant; the temperature of the body was set at 150°C).

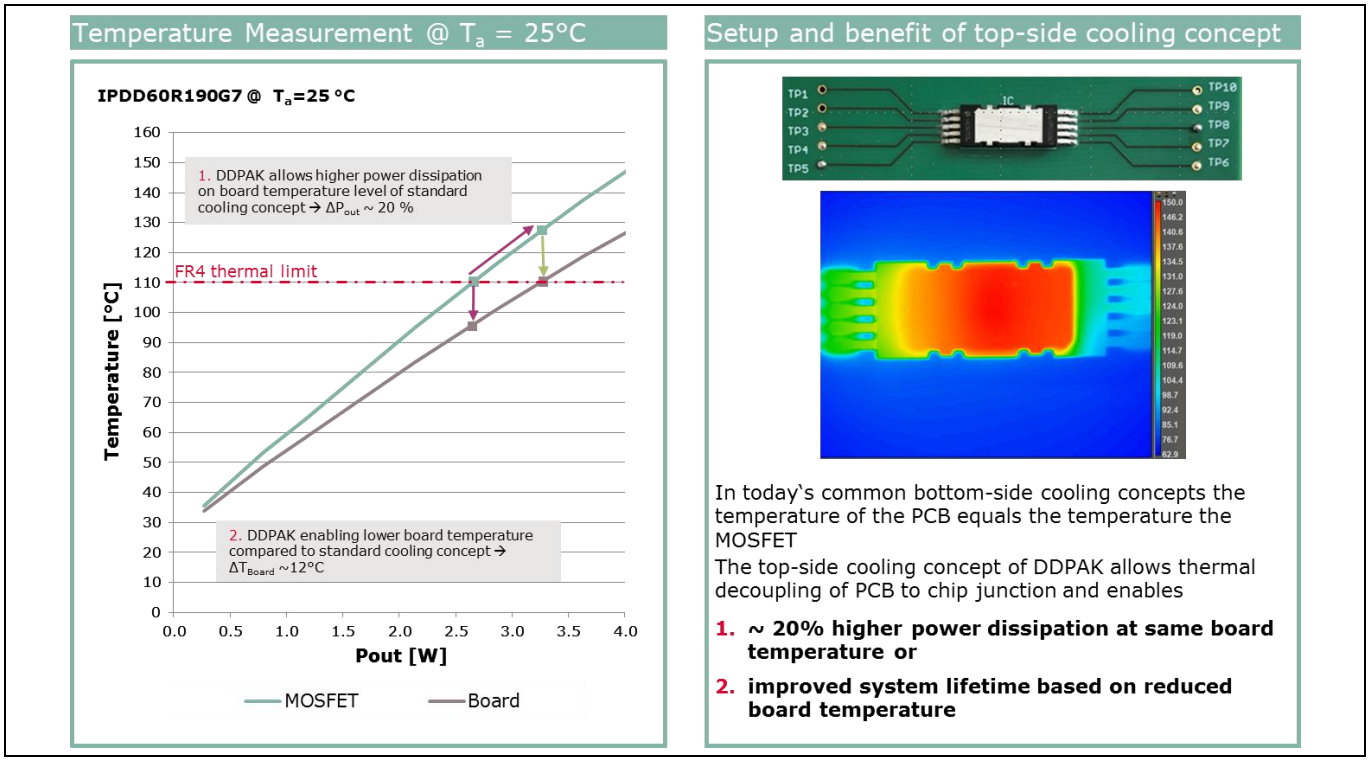


Figure 27 Package vs board temperature

If the use of heatsinks is now considered for the heat reduction of the SMD components, the type of fixing, tolerances on the package (see Figure 28) and board level must be clarified.

Further parameters like thermal resistance, dimensions (volume) and weight of the heatsink have to be taken into account to apply a suitable cooling concept to the entire system.

4.1 Height differences on board level

When designing with surface mount components (switches, passive components), only the correct solder pad size and footprint should be used.

Internal investigations were done to analyze the height tolerances resulting from soldering several DDPAKs in parallel on the same PCB enabling higher power density without sacrificing the possible output power of one single device.

The set-up used was a laser scanner in a dedicated Infineon laboratory to create reproducible and reliable results and give an indication of where extra focus was needed when designing with new package variants.

In the next section packages in two different variants will be described to give an idea of how big the difference can be in a real customer use case, with several soldered parts on one common PCB.

Figure 28 shows the roughness of the DDPAK package's top side and the maximum possible bending across the length and the width of the package (~40 µm). This extra tolerances of the package itself has to be considered when choosing the appropriate thermal interface (much greater than 50 µm thickness).

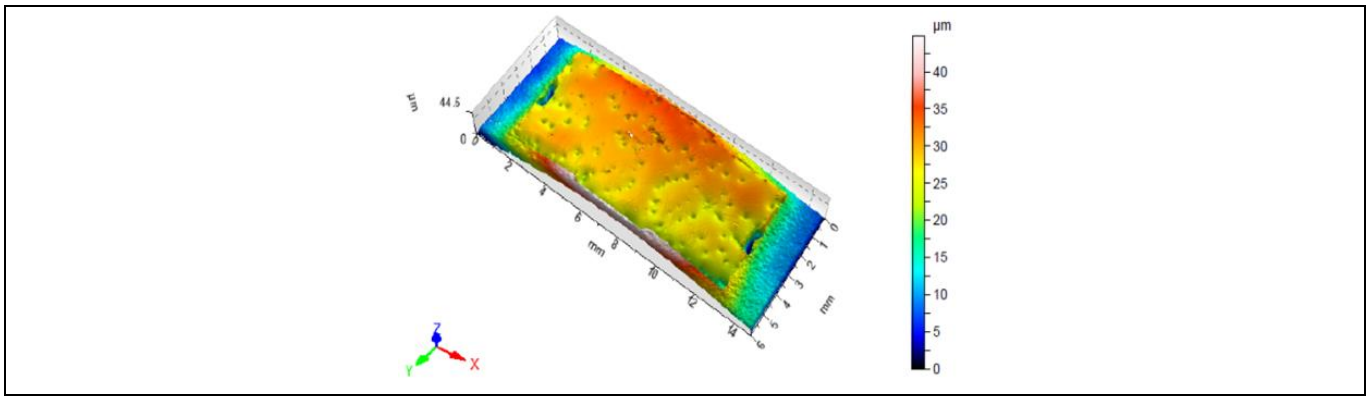


Figure 28 DDPAK top-side profile (roughness)

4.1.1 Test board 1 (three packages in parallel)

To check the height difference in a customer near use case three DDPAKs have been soldered onto one PCB with the following specifications.

Board specification (Figure 29):

- 35 µm copper
- 35 × 36 mm
- 1.6 mm PCB thickness
- PFC

For the following analysis the inspection with the laser was repeated several times and the tolerances are negligible.

The outcome of the laser inspection is a diagram which can be seen in Figure 29 on the right-hand side.

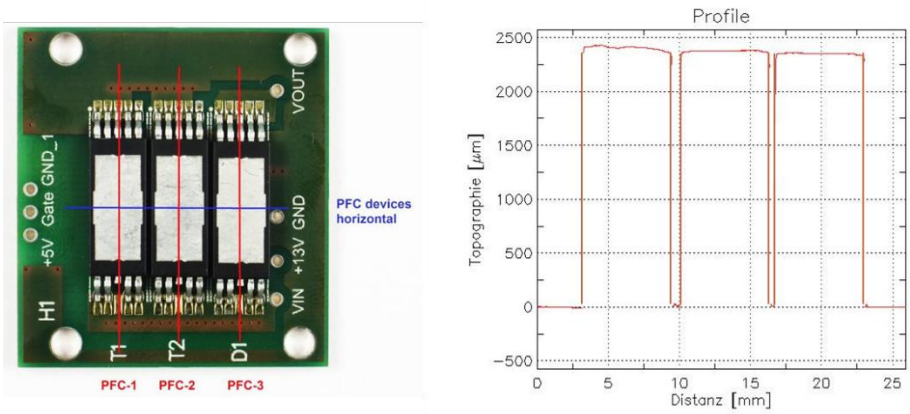


Figure 29 Height differences test board and profile (three packages in parallel)

From the application (for example, PFC stage, realized using 2 × PFC MOSFETs in parallel and 1 × diode) and thermal connection point of view, the maximum height difference can be seen as follows:

Results of the first test:

- Maximal height: 2393 µm
- Average height: 2376 µm
- Maximal difference: 22 µm
- Average difference: 14 µm
- Thermal foil: More than 50 µm

When paralleling at least three packages on a PCB with robust/appropriate thickness the maximum height difference is less than 30 µm.

For the cooling and the thermal interface (if needed) this means that a thermal foil must be able to compensate for this minimal tolerance to guarantee the best connection of every single device to a heatsink or directly to the housing of the SMPS.

4.1.2 Test board 2 (eight packages in parallel)

A second example board was tested during qualification and evaluation with a higher number of soldered devices.

In this case, a PFC combined with an LLC stage was chosen (2 × PFC MOSFETs, 2 × diodes, 2 × high-side MOSFET LLCs, 2 × low-side MOSFET LLCs).

Board specification (Figure 30):

- 35 µm copper
- 60 × 28 mm
- 1.6 mm PCB thickness

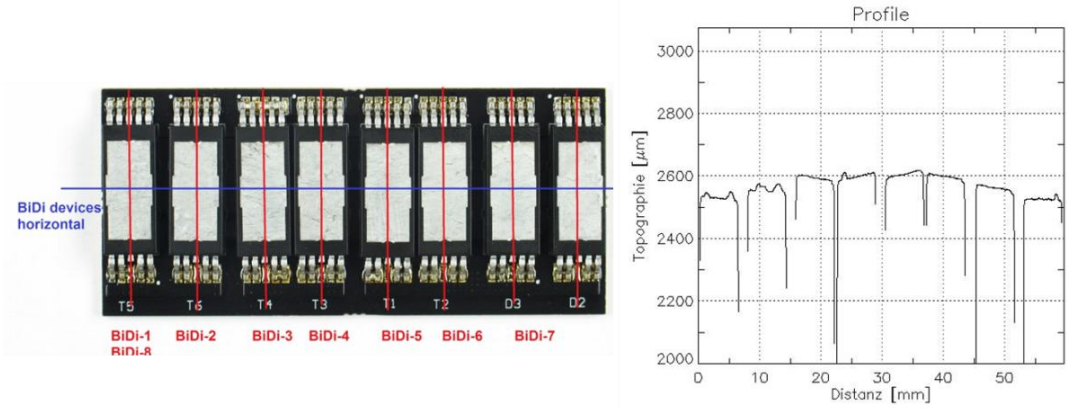


Figure 30 Height differences – test board and profile (eight packages in parallel)

Results of the first test:

- Maximal height: 2664 µm
- Average height: 2613 µm
- Maximal difference: 45 µm
- Average difference: 30 µm
- Thermal foil: Much more than 50 µm

The analysis of the use cases showed that there is a difference between paralleling one, two or more DDPAKs. In the case of paralleling more than two DDPAKs the thermal interface must be able to compensate for at least a tolerance of around 50 µm to guarantee a suitable connection between all devices.

In the specification of the DDPAK we have 150 µm of stand-off distance (see datasheet package specification and tolerances) which leads to possible height balancing over the springs of the package body itself. The limitation here is the force which can be applied on one single device soldered together with others on a PCB. This means it can be a problem to use this 150 µm stand-off margin in all devices.

This was evaluated and proved in previous investigations. Without a dedicated stand-off we would need to equalize the 50 µm with a thermal interface only. Due to the stand-off, we can even go below this if the proper pressure is applied. Therefore, the thermal interface must be chosen carefully, which will be also described in one of the following chapters.

4.2 Cooling concepts

Thermal management plays a dominant role in the design process of electronic products. Component sizes get reduced while performance and functional demands increase, resulting in more power dissipation on smaller surfaces.

Dealing with these growing thermal challenges, industry continuously seeks cooling equipment with improved heat transfer performance. However, as thermal engineering is traditionally considered toward the end of the design process, the applied cooling solutions are often simply mounted onto the product. As such, cooling equipment for electronics is growing out of proportion compared to the electronic component it is supposed to cool.

In the following two sections, the most common use and mounting options of the new DDPAK will be illustrated to give an overall idea of how to improve the overall form factor of the system while not violating any thermal constraints.

4.2.1 Cooling with heatsink springs and copper plate

A standard way of mounting TO-220 (leaded) packages to a heatsink is over springs which are fitted in a milled nut equivalent to the heatsink, or simply by pressing the TO-220 against a cooling plate.

These springs can also be used to connect the daughter card (as can be seen in Figure 31) with an isolation foil to a copper cooling plate, even when trying out different variants, giving the benefit of an easy and quick change of MOSFET platine. This would be a simple and effective solution to achieve wide heat-spreading and good cooling performance (shown later with Infineon's 1600 W server PSU).

Board specification (Figure 31):

- 35 µm copper
- 60 × 30 mm
- 1.6 mm PCB thickness
- PFC + LCC on one board
- Isolation foil: Bergquist 1500ST

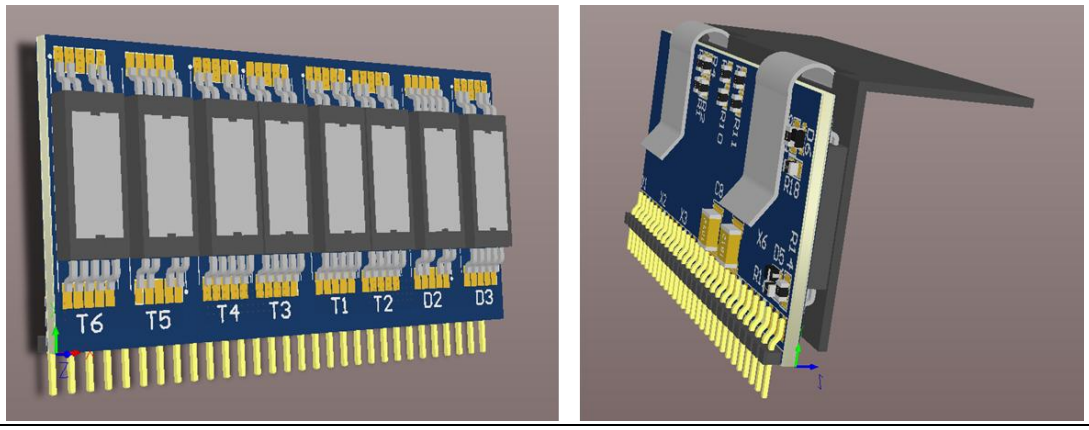


Figure 31 DDPAK module with TO-220 spring connection to copper cooling plate

4.2.2 Cooling with heatsink and push-pins

An approach which is well known and often applied is a connection via push-pins. This method benefits the overall system height.

In several experiments it was shown that such a system can replace the TO-220 FP parts, and the long heatsink installation inside a TV power supply.

- 35 µm copper
- 70 × 35 mm
- 1.6 mm PCB thickness
- Three-phase PFC
- Isolation foil: Bergquist 1500ST

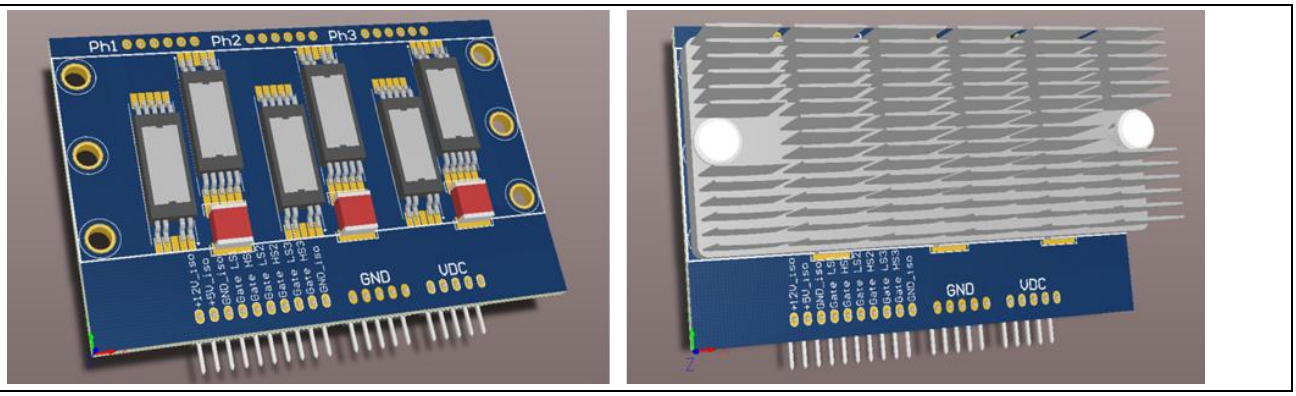


Figure 32 DDPAK module with push-pin heatsink connection

In Figure 32, a sample build for a three-phase PFC power stage is shown. On the right-hand side the connection of the heatsink to the power board is handled over only two separate push-pins (white), giving enough contact pressure to realize a reasonable heat transfer from the package to the heatsink (cooling fins).

4.2.3 Cooling with thermal adhesives

As shown in Figure 22, where the heatsink was soldered directly to the DDPAK package without any isolation, another option would be the connection between MOSFET and heatsink with an isolation foil without the use of special fasteners.

An example solution is bond-ply, which is shown in Figure 33. More details on the different variants and thermal characteristics of such materials can be found here:

- Henkel/Bergquist bond-ply (Link)

Liquid adhesives create a mechanical attachment between a component and a heatsink. Additionally, the thermal transfer properties are guaranteed, and the need for additional fasteners is obsolete. Furthermore, the low-modulus silicone design effectively absorbs mechanical stresses induced by the assembly process, as well as shock and vibration, while providing exceptional thermal performance and long-term reliability.



Figure 33 DDPAK module with bond-ply attachment

4.3 TCOB reliability of the DDPAK package

IPC9701 defines the thermal cycling test at the PCB level. The TCOB test is designed to detect failure modes, which are due to the thermo-mechanical mismatch between devices and the PCB. These are mainly solder joint fatigue but also include potential internal package defects from the stress related to the Coefficient of Thermal Expansion (CTE) mismatch to the PCB (e.g. delamination, cracks or anything else).

A standard failure criteria during in-situ monitoring is a resistance increase of the daisy chain (contact resistance monitoring between two contacts) of more than 20 percent (according to IPC9701). In the case of very small daisy-chain resistances, a higher resistance threshold is used and documented within the test report.

TCoB Test Setup used for Evaluation of 2nd Level Reliability of the PG-HDSOP-10 Package

Topic	Description		Comment
	Value	Unit	
Test Vehicle			
PG-HDSOP-10	16 x 6.5	mm²	
Chip	12	mm²	CoolMOS
Stress Boards			
Board material	high T_g FR4	-	Std. TCoB test board PMM
Board thickness/ layer	1.6 mm/ 4-layer	-	
Finishing	Chem. Sn	-	
Solder material	SAC305	-	
Stencil thickness	120	µm	
Stress Condition			
Temperature range	-40° C ... 125° C	° C	1 cycle/ hour according to IPC 9701
Monitoring	Electrical readout & Cross sectioning	-	Online readout

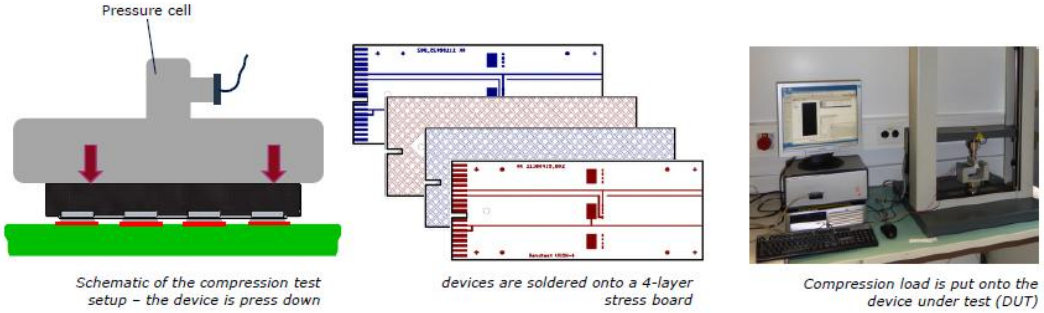
Figure 34 TCOB test set-up specification for the DDPAK

In Figure 34, specifications for the TCOB test is shown. The tests were performed for four-layer PCB and FR4 material.

- For the PCB version: no electrical failure and no optical objection were detected up to 2000 cycles

4.4 Compression reliability of the DDPAK

Furthermore, a test is performed to check the mechanical capability of the top-side heatsink mounting (single-device study).



Schematic of the compression test setup – the device is press down

devices are soldered onto a 4-layer stress board

Compression load is put onto the device under test (DUT)

Figure 35 Compression test set-up

A new option for integration

Thermal handling

Devices are soldered onto a test PCB, which will be fixed in an automatized pressure set-up.

- Online read-out equipment is connected to the test PCB
- Pressure is applied on top of the devices until the device fails/maximum possible force is reached

Compression Test Setup for PG-HDSOP-10 devices

Topic	Description		Comment
	Value	Unit	
Test Vehicle			
PG-HDSOP-10	16 x 6.5	mm²	
Chip	12	mm²	CoolMOS
Stress Boards			
Board material	high T_g FR4	-	
Board thickness/ layer	1.6 mm/ 4-layer	-	
Finishing	Chem. AuSn	-	
Solder material	SAC305	-	
Stencil thickness	120	µm	
Stress Condition			
Load Force	0 ... 2500	N	Ramp up to max load -> ramp down
Monitoring	Online electrical readout	-	Check for electrical fail during stress test

Figure 36 Specification of compression test set-up for the DDPAK

Summary of compression stress test:

- PG-HDSOP-10-1 device is soldered onto a test board and put into a compression test
- Load stress was increased up to machine limit (2500 N)
- All devices passed the compression test up to the maximum stress limit (machine limit)

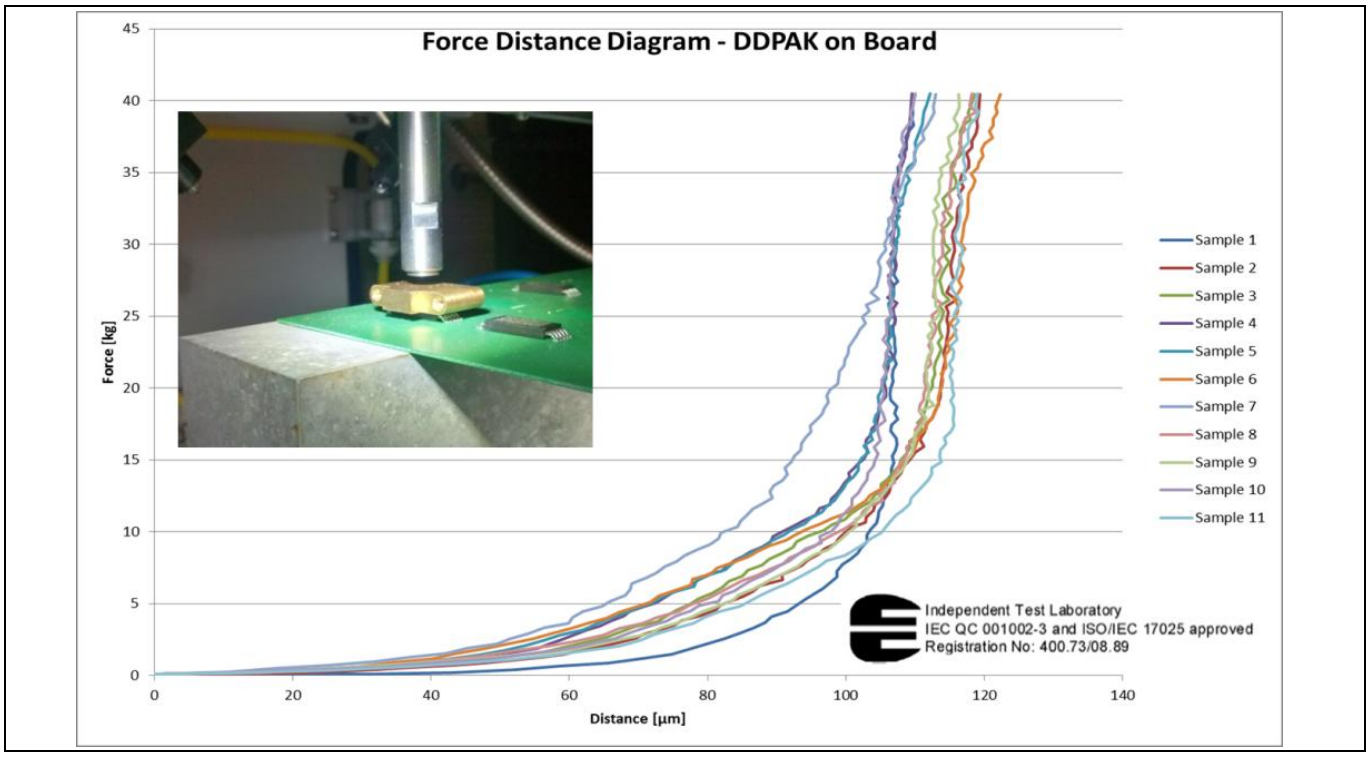


Figure 37 Force distance diagram – DDPAK on board

In Figure 37, it can be seen that with a force of around 10 kg the distance between the body and the PCB is already going toward “0” (which means that the body of the DDPAK is touching the PCB surface).

This shows impressively the benefit of the package and its pins, because the pins are acting like small springs compensating for the differences in the package heights and/or PCB tolerances.

4.5 Moisture Sensitivity Level (MSL)

For moisture-sensitive packages, it is necessary to control the moisture content of the components. Penetration of moisture into the package molding compound is generally caused by exposure to ambient air. In many cases, moisture absorption leads to moisture concentrations in the component that are high enough to damage the package during the reflow process. Thus, it is necessary to dry moisture-sensitive components, seal them in a moisture-resistant bag, and only remove them immediately prior to assembly to the PCB. The permissible time (from opening the moisture barrier bag until the final soldering process) that a component can remain outside the bag is a measure of the sensitivity of the component to ambient humidity (MSL). The most commonly applied standard IPC/JEDEC J-STD-033* defines MSLs for different heights.

Please refer to the “Moisture Sensitivity Caution Label” on the packing material, which contains information about the MSL of our products. IPC/JEDEC J-STD-20 specifies the maximum reflow temperature that should not be exceeded during board assembly.

Level	Floor Life (out of bag)	
	Time	Conditions
1	Unlimited	≤30°C/85% RH
2	1 year	≤30°C/60% RH
2a	4 weeks	≤30°C/60% RH
3	168 hours	≤30°C/60% RH
4	72 hours	≤30°C/60% RH
5	48 hours	≤30°C/60% RH
5a	24 hours	≤30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤30°C/60% RH

Figure 38 MSL (according to IPC/JEDEC J-STD-033, RH = relative humidity)

If moisture-sensitive components have been exposed to ambient air for longer than the permitted time according to their MSLs, or the humidity indicator card indicates too much moisture after opening a moisture barrier bag, the components must be baked prior to the assembly process. Please refer to IPC/JEDEC J-STD-033* for details. Baking a package too often can cause solderability issues due to oxidation and/or intermetallic growth on the open contact areas. In addition, packing material (e.g. trays, tubes, reels, tapes, etc.) may not withstand higher baking temperatures. Please refer to imprints/labels on the packing to determine the maximum allowable temperature.

For Pb-free components, two MSLs can be given: One for a lower reflow peak temperature (Pb-containing process) and one for a higher reflow peak temperature (Pb-free). Each one is valid for the respective application.

The new G7 technology and 650 V CoolSiC™ G6 support the highest moisture sensitivity level – MSL1. Therefore, it can be stored in this respect for unlimited time.

4.6 Isolation material differences

In several laboratory tests different isolation materials have been tested to check pros and cons, and strengths and weaknesses of changed materials.

The commonly used thermal foils can be seen in Figure 39. The foils differ not only in their thermal impedance but also in their softness and hardness, which is directly related to their compensation qualities.

As seen in the previous chapters, height tolerances must be compensated for, so a too-hard foil may not be the right choice when mounting more than one component on the same PCB connected to a single heatsink.

	Sil-Pad K-10	Sil-Pad 1500ST	Tgard 100	Tgard 220
Manufacturer	Bergquist	Bergquist	Laird	Laird
Surface	Hard	Soft	Medium	Medium
Thermal impedance [°C-in²/W]	0.41 (@50psi)	0.23 (@50psi)	0.279 (@50psi)	0.35 (@100psi)
Thermal Conductivity [W/mK]	1.3	1.8	3.5	5
Foil thickness [mm]	0.15	0.20	0.4	0.51
Dielectric Breakdown Voltage [Vac]	6000	3000	6000	10000

Figure 39 Thermal foil comparison (different manufacturer)

A new option for integration

Thermal handling

All listed foils have been compared in a PFC stage (the detailed description can be seen in Figure 40), where a MOSFET and a diode have been soldered together on one PCB.

As input voltage 90 V AC_{in} was chosen due to the fact the MOSFET sees the highest possible current, and the system was driven up to 1 kW with a 50 mΩ switching device and a 20 A diode to keep the losses as small as possible.

It is obvious that every foil behaves in a different manner approaching the full-load point at 1 kW. Checking this maximum point of load, a difference in MOSFET temperature illustrated by the four lines shows a delta in possible temperature of 23°C (measured at 1 kW, 80°C with 1500ST and 103°C with Tgard220).

This measurement illustrates impressively how important it is to choose different thermal interfaces during your application evaluation, and to test out new SMD packages with totally different thermal connections (drain cooling plain onto the DDPAK package).

In terms of isolation and safety, the dielectric breakdown voltage must be chosen carefully each time.

Nevertheless, the final decision is in the designer's hands, because besides lifetime and temperature constraints inside the SMPS itself, commercial considerations also must be considered.

Furthermore, the 1500ST showed the best performance in terms of compensating for height differences out of the soft characteristics of the foil itself. The main constraint with its usage is that it can and should be used only once – which is no issue in mass production, but it is when using it in the evaluation phase and when trying out new combinations (more or fewer components in parallel). This foil must be exchanged with every test because with increased pressure it starts to deform a little bit, which helps in case of the thermal performance, but on the other hand has the drawback of reusability.

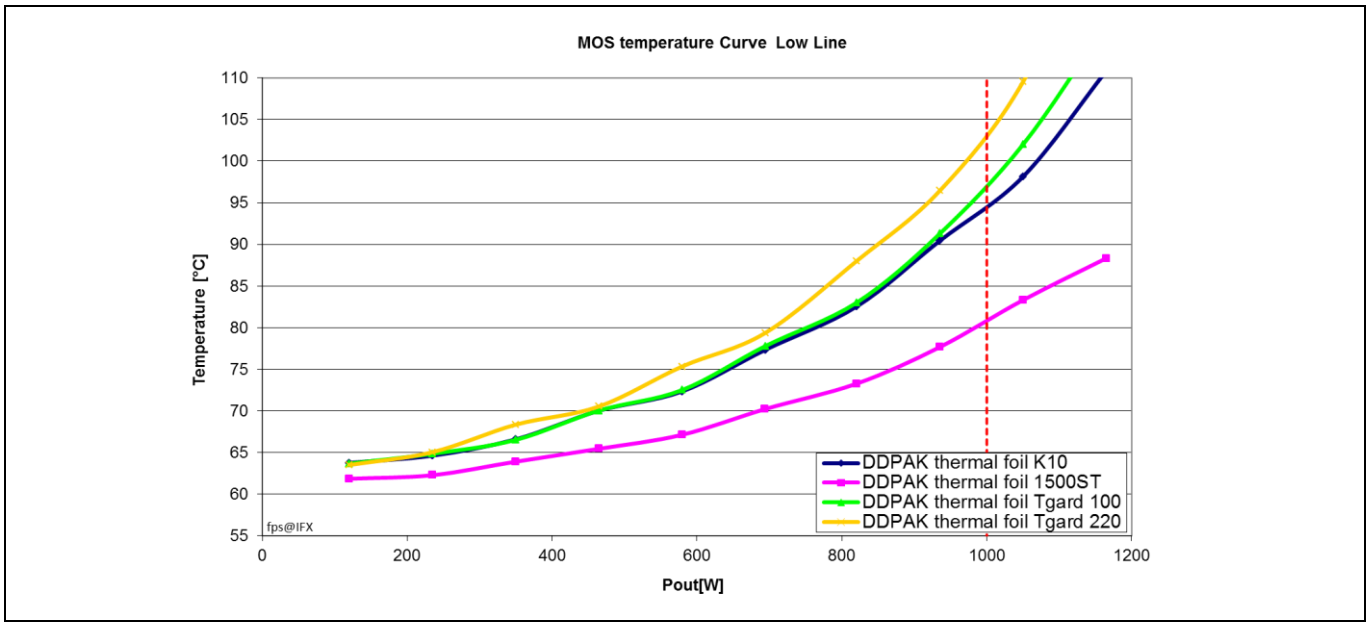


Figure 40 Thermal measurement of the DDPAK MOSFET (IPDD60R050G7, 90 V AC, 65 kHz, R_G, ext. 10 Ω)

A new option for integration

Thermal handling

The application-relevant output power with this combination and the board capability is around 1000 W (red dotted line) at low-line (90 V AC_{in}), but nevertheless the test has been performed up to nearly 1200 W to see the absolute limits of the board and the parts themselves. The limiting factor in this case is the maximum allowed temperature of the FR4 material for long-lasting temperature stress, which is 110°C.

A second test with the highest $R_{DS(on)}$ part in the portfolio was performed and the experiments showed quite similar results as before.

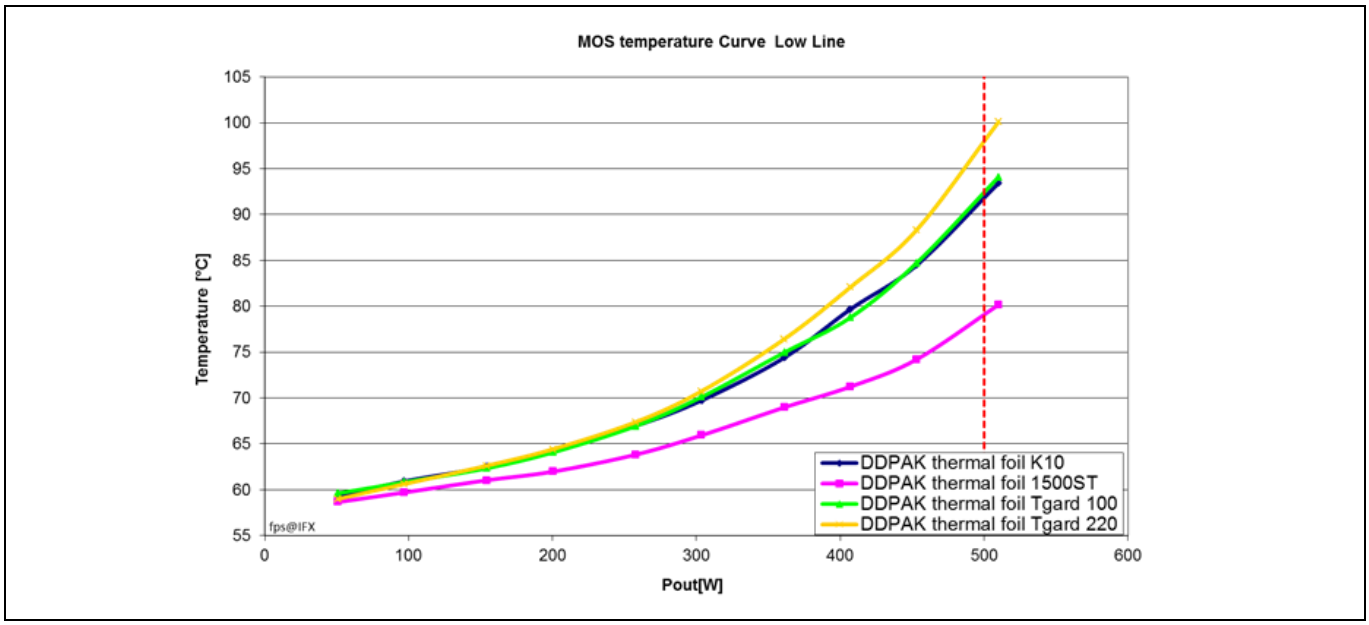


Figure 41 Thermal measurement of the DDPAK MOSFET (IPDD60R190G7, 90 V AC, 65 kHz, R_G, ext. 10 Ω)

In this case, the application-relevant output power with this combination and the board capability is around 500 W (red dotted line) at low-line (90 V AC_{in}), where a difference of around 20°C was the maximum delta appearing.

There are several more thermal interface materials used; these tests have been performed to demonstrate the great influence of and the possible performance waste resulting from a wrongly chosen foil.

5 Application results

Application testing is the key in developing and evaluating new concepts, especially when you have an innovative package like the DDPAK in combination with the 600 V CoolMOS™ G7 and the latest generation of SiC Schottky diode.

In the following sections two application measurements in different platforms will be described. For the first feasibility study, a test board was chosen. This board gives on the one hand the possibility of measuring and evaluating different package variants and, on the other hand, the freedom to easily access and change external components like $R_{G,ext}$ or setting different frequency levels.

Additionally, and to prove the new hardware in a more specific and real-world application segment, Infineon decided to do a state-of-the-art form factor power supply with increased power density to show the strength of the new package.

5.1 2.5 kW Infineon Continuous Conduction Mode (CCM) PFC evaluation board

The application testing for the G7 devices shown in this document is performed by adding a daughter board to the 2.5 kW PFC evaluation board – including the Infineon CCM PFC controller (ICE3PCS01G), as shown in Figure 42.

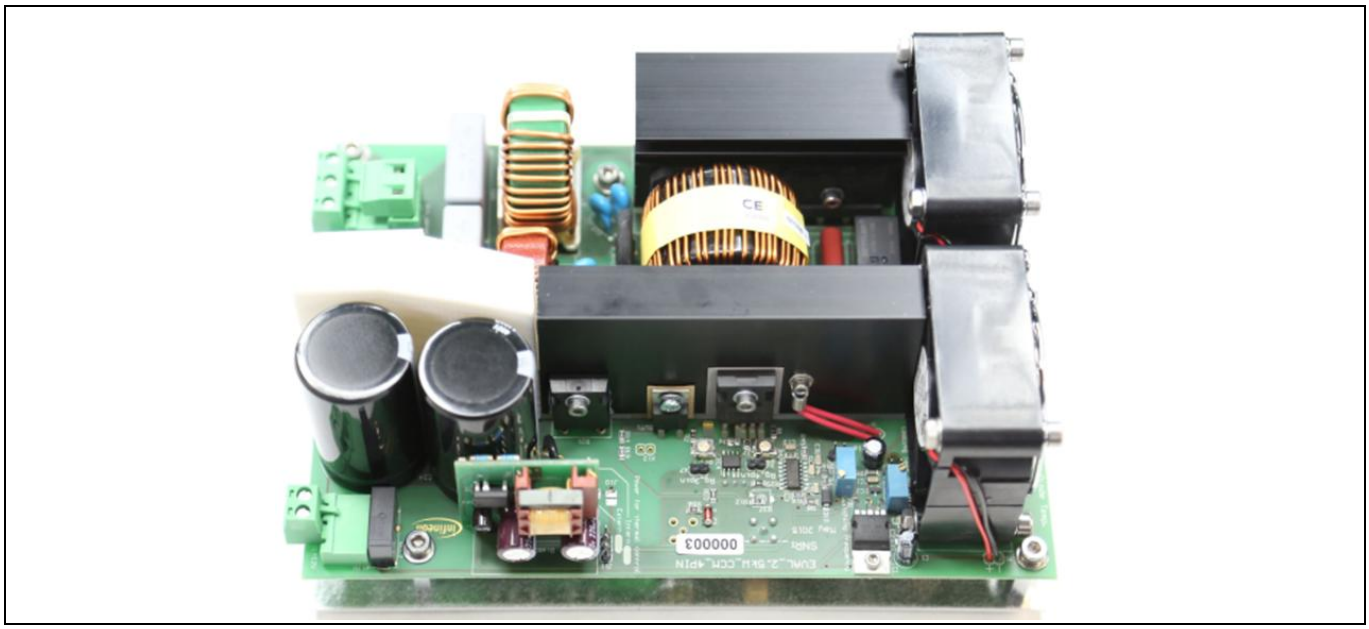


Figure 42 EVAL_2.5kW_CCM_4PIN evaluation board

The 2.5 kW evaluation board is an excellent example of a complete Infineon solution, and includes a PFC controller, MOSFET driver and SiC diode, enabling evaluation of the 4-pin functionality and its advantages for efficiency and signal quality. The layout of the board is intended to allow easy access to the different devices and to add measurement probes to areas of interest. The evaluation board is fitted with double connectors for the power line input and 400 V output to allow sense techniques for precise efficiency measurements.

For more detailed information about the evaluation board please review www.infineon.com/C7-600V.

Description	Specification
Low-line	90 V AC, 500/1250 W
High-line	230 V AC, 500/2500 W
PFC choke	600 µH
Shunt	5/10 mΩ
Frequency	65 kHz
Used parts	**IPDD60R190G7 and IDDD04G65C6** **IPDD60R050G7 and IDDD20G65C6**
Accuracy	0.1 percent
Board dimensions L x W x H [mm]	200 x 140 x 70

Figure 43 EVAL_2.5kW_CCM_4PIN evaluation board specification

The original design of this evaluation board is fitted with a TO-247 MOSFET. To use the DDPAK G7 and SiC diode devices in this evaluation board, some modifications with daughter boards are required.

The special daughter board shown in Figure 44 is designed to fit into the pin arrangement of the main PFC evaluation board.

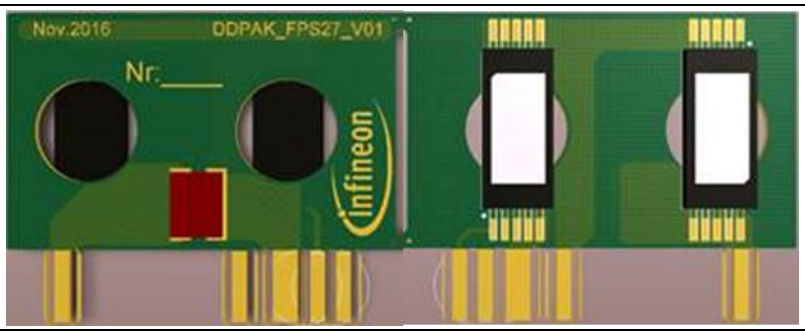


Figure 44 Daughter boards/cards for the DDPAK MOSFET and diode (front and back view)

On the DDPAK daughter card, the diode, the MOSFET and a capacitor are assembled. Thermal conductive paste must be added to the packages through the holes (openings in the PCB back for connection of the fasteners). The DDPAKs are fixed through these holes with two plastic screws. For thermal sensing two thermocouples can be connected to the back of the DDPAK package and read out via a data logger unit.

A bolt makes it possible to adjust the pressure that fixes the parts to the PFC board's heatsink. To ensure the right isolation between the heatsink and DDPAK, insulating foil must be added. Depending on the temperature of the foil, its behavior can vary.

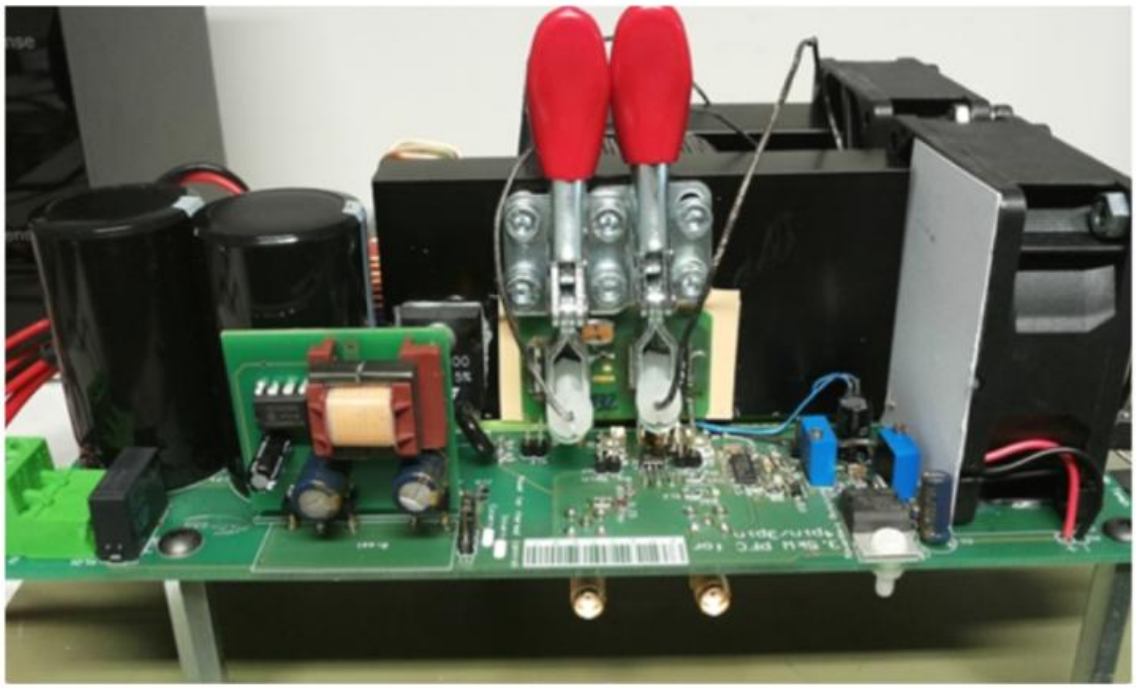


Figure 45 EVAL_2.5kW_CCM_4PIN evaluation board equipped with DDPAK daughter card

As can be seen in Figure 45, the evaluation board is also equipped with a big heatsink in the back, where different scenarios (cooling with fan/airflow; pre-heating of heatsink to given temperature) of different ambient conditions can be simulated.

As already shown in comparison with the thermal foils, two different tests have been performed.

Efficiency and thermal measurement with the smallest and the largest chip possible in the DDPAK package mean the 50 mΩ and the 190 mΩ chip.

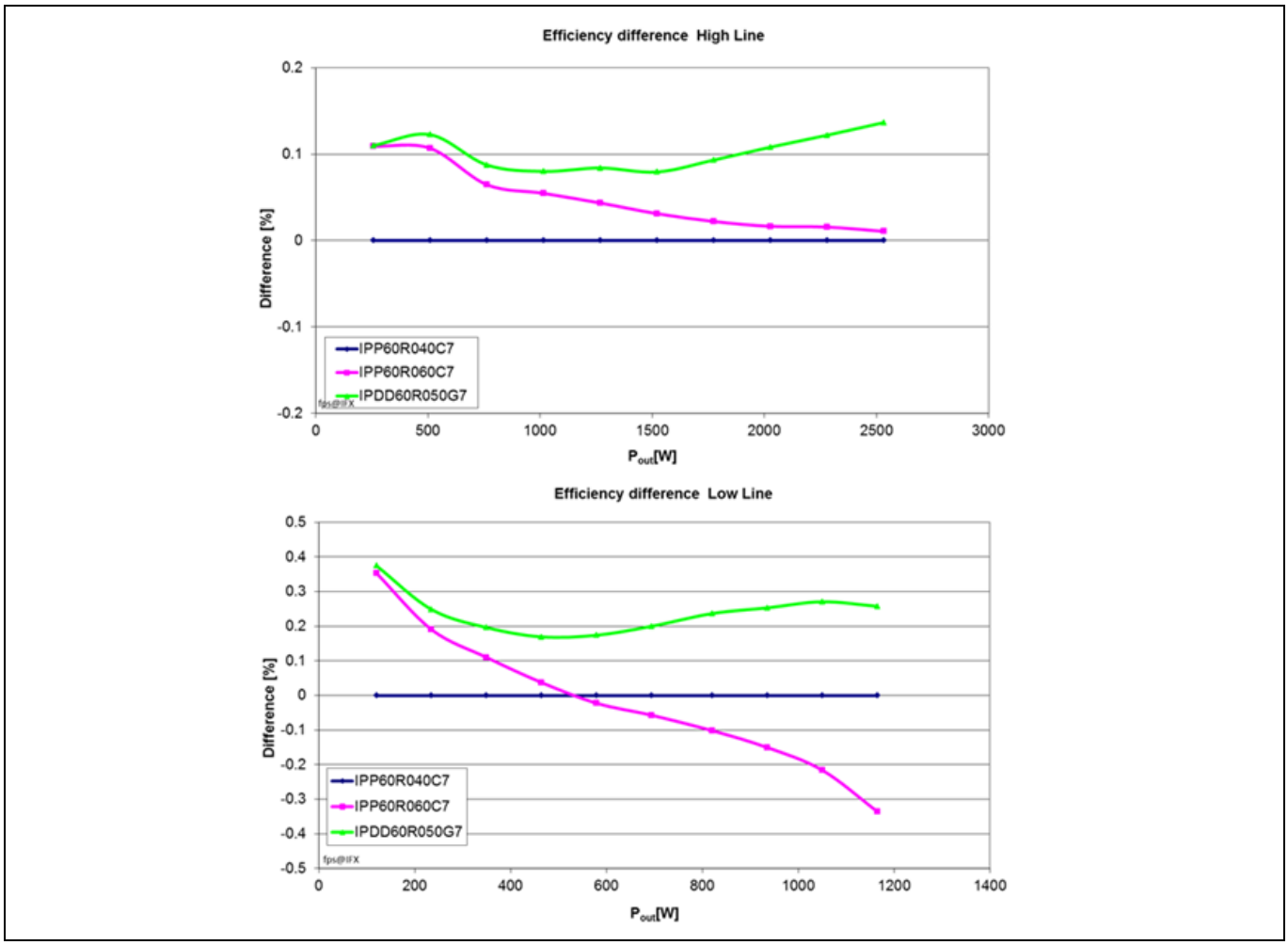


Figure 46 Efficiency measurement of the DDPAK MOSFET (IPDD60R050G7, 90/230 V AC, 65 kHz, R_G, ext. 10 Ω)

In Figure 46, the two differential charts with 230 V AC_{in} (above) and with 90 V AC_{in} (below) can be seen.

Since Infineon does not have the same $R_{DS(on)}$ in the DDPAK and TO-220 available, two comparable $R_{DS(on)}$s in TO-220 are presented (40 mΩ and 60 mΩ).

On the left side, the difference in efficiency is in the range of 0.1 percent, so within the tolerance level of the measurement itself. On the right side (where the low-line is applied) the strength of the 4-pin approach is more evident at the full-load point where the current is at its maximum. The clear signal quality on the gate helps to reduce overall losses inside the MOSFET, giving best efficiency at the full-load point.

The same test was performed in Figure 47 with the highest possible $R_{DS(on)}$ in DDPAK from our latest portfolio. Results are expected to be the same, proven during several lab tests.

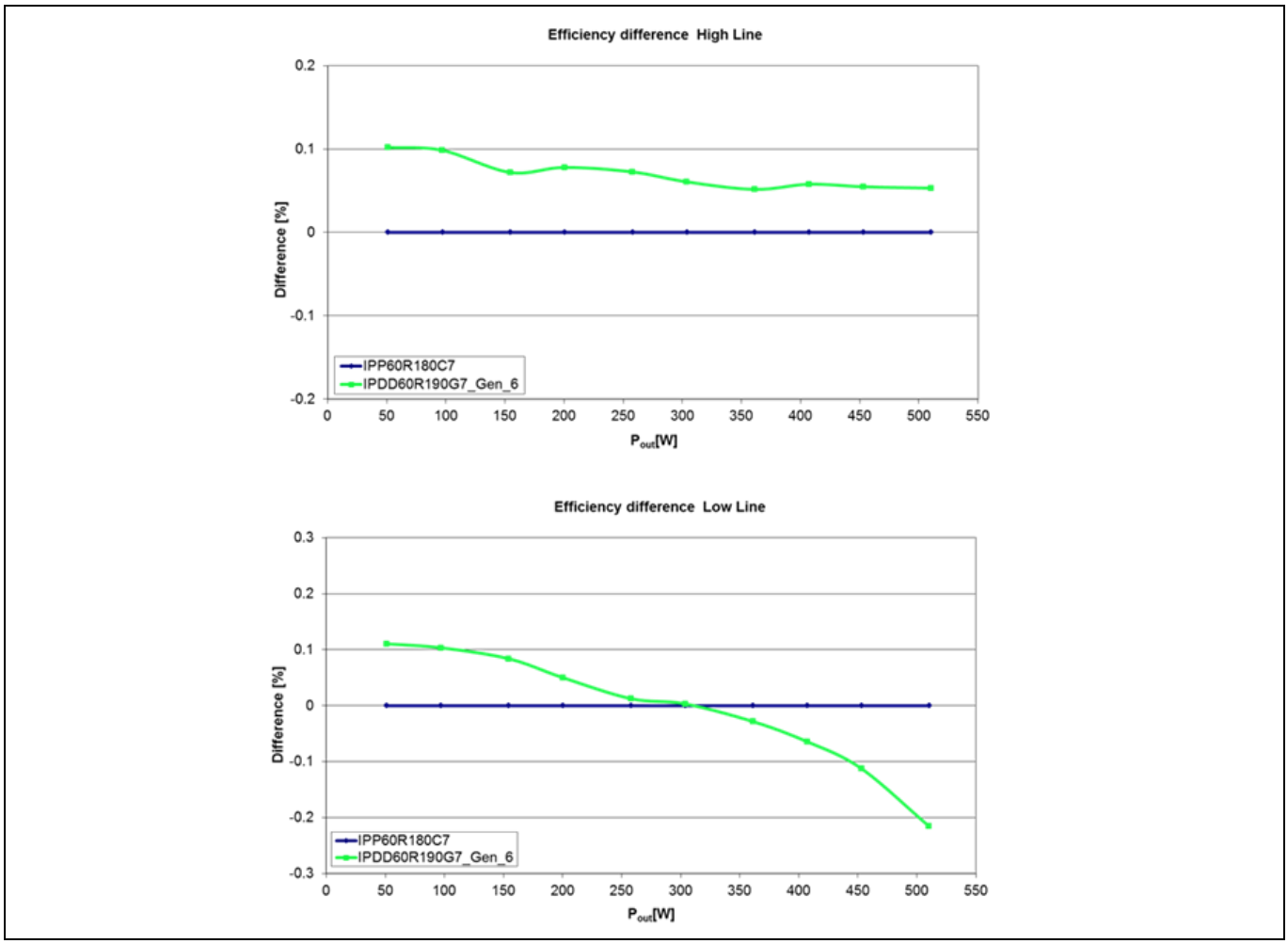


Figure 47 Efficiency measurement of the DDPAK MOSFET (IPDD60R190G7, 90/230 V AC, 65 kHz, R_G, ext. 10 Ω)

The results of the DDPAK G7 190 mΩ show at high-line a slight increase in performance in the range of 0.1 percent in efficiency, which translates to an appropriate thermal behavior in the system itself.

Looking at the lower chart where the low-line measurement is shown you will see a drop in efficiency at the full-load point (at 500 W) due to the worse $R_{DS(on)}$ of the DDPAK G7 190 mΩ compared to the IPP60R180C7 (10 mΩ of difference) device.

At the end, for changing from leaded to SMD packages a lot of effort is needed to come to the same or better performance without investing in and applying new thermal concepts.

But in the end these efforts will reduce total manufacturing costs, enabling a new level of power density, which is powerfully illustrated in the next chapter.

A laboratory test can only be an indication that the latest technologies (G7 + G6) in combination with an innovative package will bring various benefits in the application, but for exactly this reason the 1600 W Infineon Titanium server power supply was developed: a new SMD solution, bringing the strength of innovative new packages to reality, surpassing all state-of-the-art requirements and bringing power density to a new level.

5.2 1600 W Infineon Titanium server power supply

For details on 1600 W Titanium server power supply, see AN_1712_PL52_1802_095809.

Description	Specification
Input	176 – 265 V_{AC}
Output	12.2 V / 132 A Output
Efficiency Standard	Titanium Efficiency > 96 % at 50 % Load
EMI Class	Class B
Total harmonic distortion	<10 %, from 20 % load
Robustness	PLD compliant
Power Density	1U form factor ~55W/in³
Used parts	IPDD60R050G7 IPDD60R150G7 IDDD08G65C6
Board dimension L x W x H [mm]	193x70x44

Figure 48 1600 W Infineon server PSU specification

Targeting a server power supply, the specifications are listed in Figure 48. The DDPAK approach enables in this specific case a power density of around 55 W per cubic inch with Titanium efficiency standard.

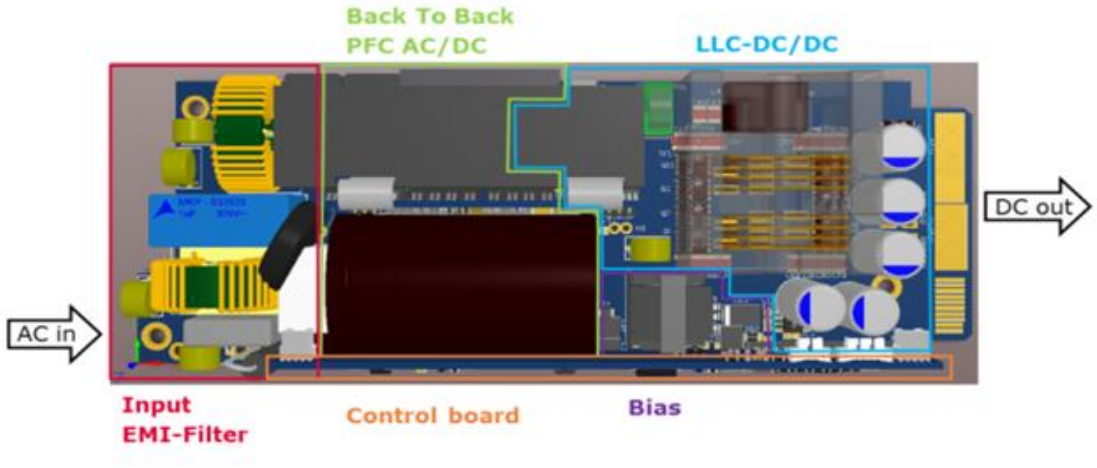


Figure 49 1600 W Infineon server PSU layout

In Figure 49, the main parts/sections are shown. The layout is defined via four sections: the input filter, the AC-DC part, the control and bias board, and the DC-DC stage.

In Figure 50, the top view of the board is visible, showing on the right-hand side the power board with soldered DDPAK devices.

A new option for integration

Application results

As is typical for server power supplies, a forced air-cooling via the fan on the upper left-hand side is guaranteed.

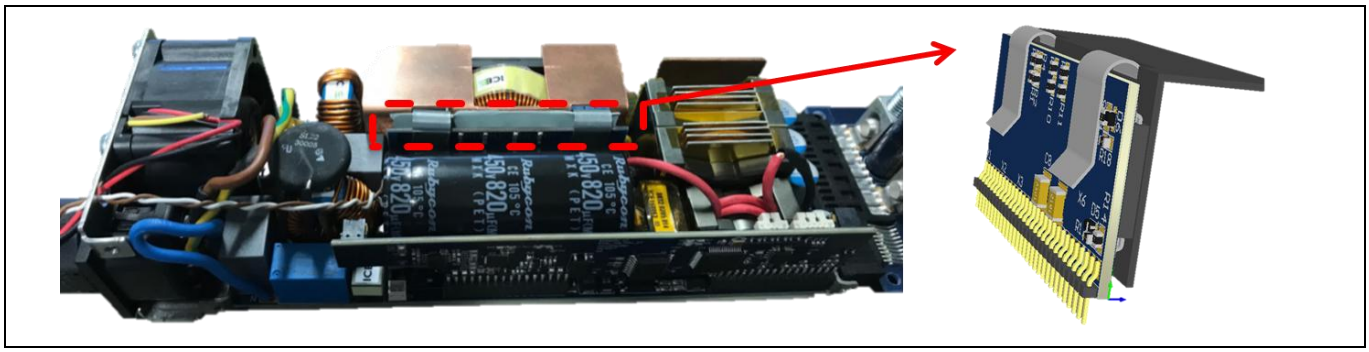


Figure 50 1600 W Infineon server PSU daughter card (PFC + LLC)

On the daughter card a full PFC plus half-bridge LLC stage is realized, giving an output power of maximum 1600 W at 230 V AC_{in}.

In Figure 51, the Titanium efficiency standard is shown by the dotted line giving a requirement point to be fulfilled at 10 percent, 20 percent, 50 percent and 100 percent load.

The Infineon 1600 W PSU version even exceeds this standard at the light-load and full-load points, reaching the standard at the 50 percent load point.

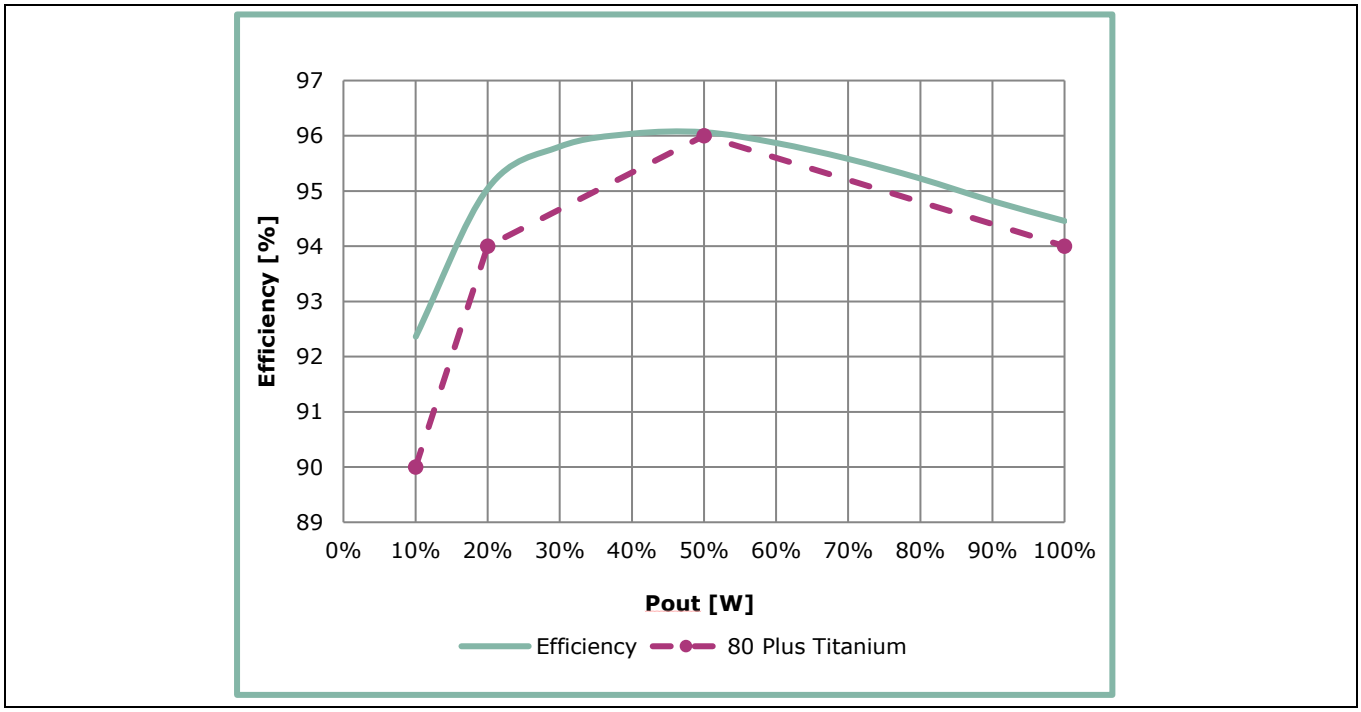


Figure 51 Efficiency measurement (at 230 V AC_{in})

For more details on several efficiency standards, see: https://de.wikipedia.org/wiki/80_PLUS.

Further important parameters are the Power Factor (PF) and the overall current distortion, shown in Figure 52.

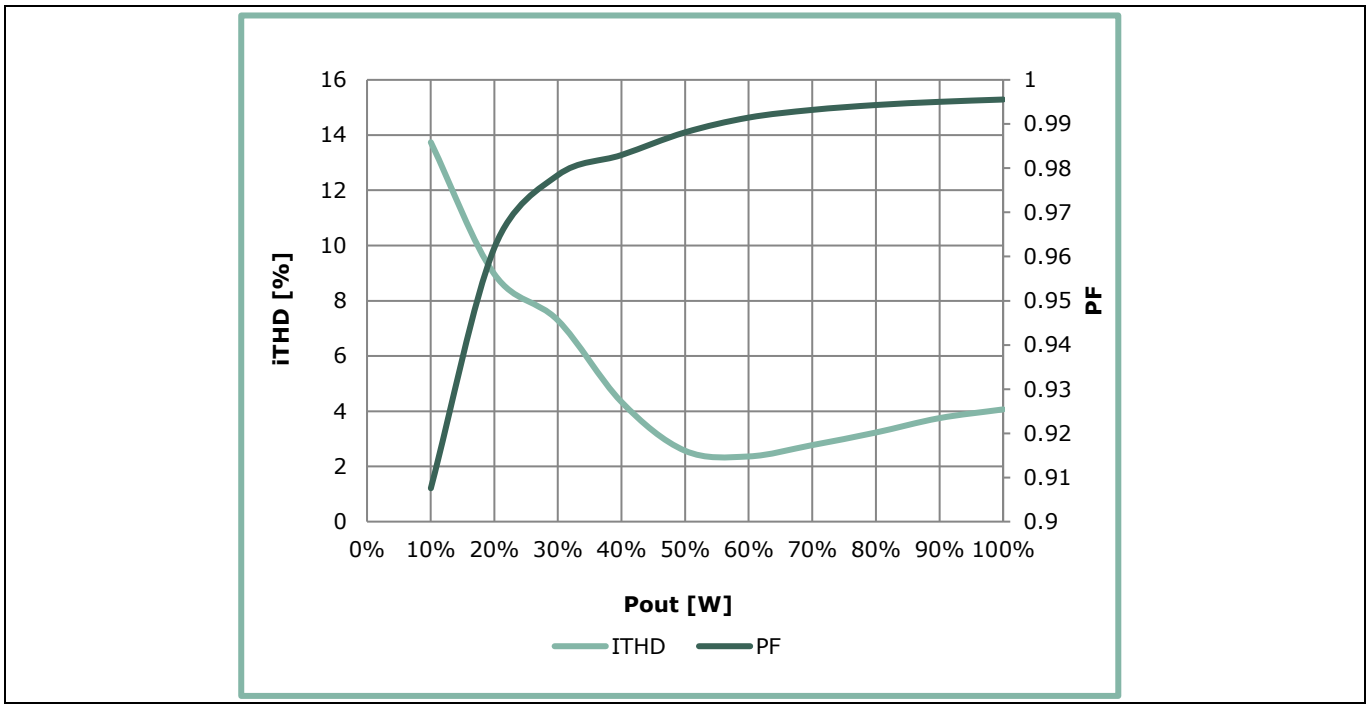


Figure 52 Current distortion and power factor (at 230 V AC_{in})

An electrical system supply powers loads by getting current and voltage from the mains. DC current is delivered to the board at the fundamental frequency. Only fundamental frequency current can provide real power.

Since this has a real effect on power consumption the 1600 W PSU can stay below 10 percent of total harmonic distortion on current (iTHD) over a quite wide load range (20 to 100 percent), going even lower than 5 percent iTHD in at the 40 percent to 100 percent load points.

In electrical engineering, the power factor of an AC electrical power system is defined as the ratio of the real power flowing to the load to the apparent power in the circuit. A PF of less than one means that the voltage and current waveforms are not in phase, and a good power supply is designed to be as close as possible to this value.

As can be seen in Figure 52, the PF of the PSU stays from 50 percent to 100 percent load over 0.99 PF, which is a quite remarkable value.

5.3 Application summary

With the top-side cooling approach of the DDPAK, whether on the CoolMOS™ or CoolSiC™ side, a lot of benefits have been demonstrated. In a nutshell, the following points are the most important:

- A new level of power density can be achieved with the top-side cooling approach of the DDPAK package
- Selection of the thermal interface has a significant influence on thermal performance
- The top-side of the DDPAK package allows heatsinks to be soldered on top of the package
- The eight pins of the package act like springs and reduce stress between the component and PCB (TCOB)
- Highest quality and reliability are ensured by several internal investigations

6 Portfolio

To summarize, the combined portfolio of the 600 V CoolMOS™ G7 and the latest 650 V CoolSiC™ G6 Schottky diode can be seen in Figure 53.

$R_{DS(ON)}$ [mΩ] Max.	CoolMOS™ G7	Amp [A]	CoolSiC™ Gen 6
190	IPDD60R190G7	4	IDDD04G65C6
150	IPDD60R150G7	6	IDDD06G65C6
125	IPDD60R125G7	8	IDDD08G65C6
102	IPDD60R102G7	10	IDDD10G65C6
80	IPDD60R080G7	12	IDDD12G65C6
50	IPDD60R050G7	16	IDDD16G65C6
		20	IDDD20G65C6



Figure 53 Combined portfolio of the 600 V CoolMOS™ G7 and 650 V CoolSiC™ G6 in the DDPAK

7 Summary

Summing up all the technical and commercial aspects described in this application note, the 600 V CoolMOS™ G7 and 650 V CoolSiC™ G6 Schottky diode in the DDPAK are shaping the market and support the trend to move from THD packages to SMD-based SMPS designs.

SMD packages support fast-switching and help to reduce the parasitic inductance associated with long leaded packages such as the common TO-220 package. In today's SMD-based designs thermal management remains a limiting factor. The innovative top-side cooling concept of the DDPAK allows thermal decoupling of the PCB and the semiconductor. Customers can use this feature to:

- Increase the power density of their designs by driving the MOSFET to higher output levels
- Improve the robustness of the design by reducing the board temperature, which leads to longer system lifetimes
- Achieve low parasitic switching due to the SMD approach and Kelvin source gate-driver connection giving boost in full-load efficiency at the highest power levels

As the DDPAK is fitted with Infineon's highly efficient MOSFET technology, the 600 V CoolMOS™ G7 and the latest 650 V CoolSiC™ G6, it supports top-side cooled system solutions for PFC as well as high-end MOSFET solutions for soft-switching topologies (e.g. LLC). The features of the 600 V CoolMOS™ G7 and 650 V CoolSiC™ G6 technologies together with the improved oscillation behavior thanks to the 4-pin Kelvin source configuration of the DDPAK enable customers achieve the highest efficiency levels.

In addition, the DDPAK exceeds the industry's quality requirements. It survives many more than 2000 TCOB cycles, is MSL1 compliant and totally lead free, and supports reduction of the TCO by reducing the manufacturing costs on the customers' side.

Also, Infineon will soon provide a further optimized power package solution with area-enhanced top-side cooling called QDPAK.

8 Related resources

- Silicon carbide CoolSiC™ MOSFETs
- Developer community

References

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[6] Infineon Technologies AG: *3 kW dual-phase LLC demo board application note*; Available online

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