Optimizing CoolMOS™ CE based power supplies to meet EMI requirements

About this document

Scope and purpose

Improving efficiency is a key consideration for AC-DC switch mode power supply (SMPS), charger and adapter designers. Chargers and adapters are in widespread usage due to the large increase in portable electronics and the efficiency and hence thermal performance need constant improvement for product differentiation and overall cost reduction. The switch in these SMPS is usually a MOSFET therefore, the lower the on state resistance $R_{DS(ON)}$ the better the efficiency. This MOSFET can be a standard planar MOSFET or superjunction MOSFET. With the same $R_{DS(ON)}$ and voltage rating, superjunction MOSFETs have lower intrinsic capacitance when compared to a standard planar MOSFET. Thus, the superjunction MOSFET switches faster than a standard MOSFET. Hence, the fast-switching SJ MOSFET needs special attention during EMI (Electromagnetic Interference) compliance testing.

In this application note we will discuss the impact of components and parasitics involved with the switching MOSFET and modify their parametric values to observe the effect on the EMI signature. A few practical cases are discussed where the above techniques are implemented successfully using CoolMOS™ CE MOSFET.

Intended audience

SMPS designers interested in moving from standard MOSFET to SJ based CoolMOS™ CE MOSFETs in order to improve the efficiency performance of their designs.

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1 Typical switching MOSFET related noise sources in a flyback based AC-DC charger and adapter SMPS

The MOSFET related di/dt and dv/dt in typical power supply stages are explained in the following sections. As shown in Figure 1, the drain net is the "noisy" high dv/dt net. Generally, when designing a flyback circuit, reducing the area of this net as much as possible will help. The MOSFET should be placed as close as possible to the pin of the transformer. Since I = C*dv/dt and dv/dt is unavoidable, reducing C will reduce the noise currents without slowing the switching speed or reducing the efficiency of the converter or generating more heat that has to be dissipated. The capacitance of a net is proportional to its area, by reducing a net's area and its capacitance to the outside world will be reduced as well.

The dv/dt challenges usually drive currents through capacitive coupling, however "di/dt" is a different issue. These fast changing currents and associated harmonics generate coupled noise voltages elsewhere, resulting in EMI. Additionally, "di/dt" can often couple through magnetic fields, since electric currents generate magnetic fields. The primary switching currents impact EMI and EMC as these are very fast changing di/dt events. The flyback circuit has several fast changing currents to be concerned about.

Of the three loops shown in Figure 1, the one causing problems most often is the output current loop. This loop's area should be minimized as much as possible in order to minimize rapidly changing magnetic fields. All the currents shown should have their loop area minimized, but for the purposes of this application note the focus will be on the primary current.

There are also transformer parasitic capacitances in a flyback design. Effective shielding and proper use of Y capacitors which limit the loop area alongside proper PCB design minimize the effects of these parasitics.

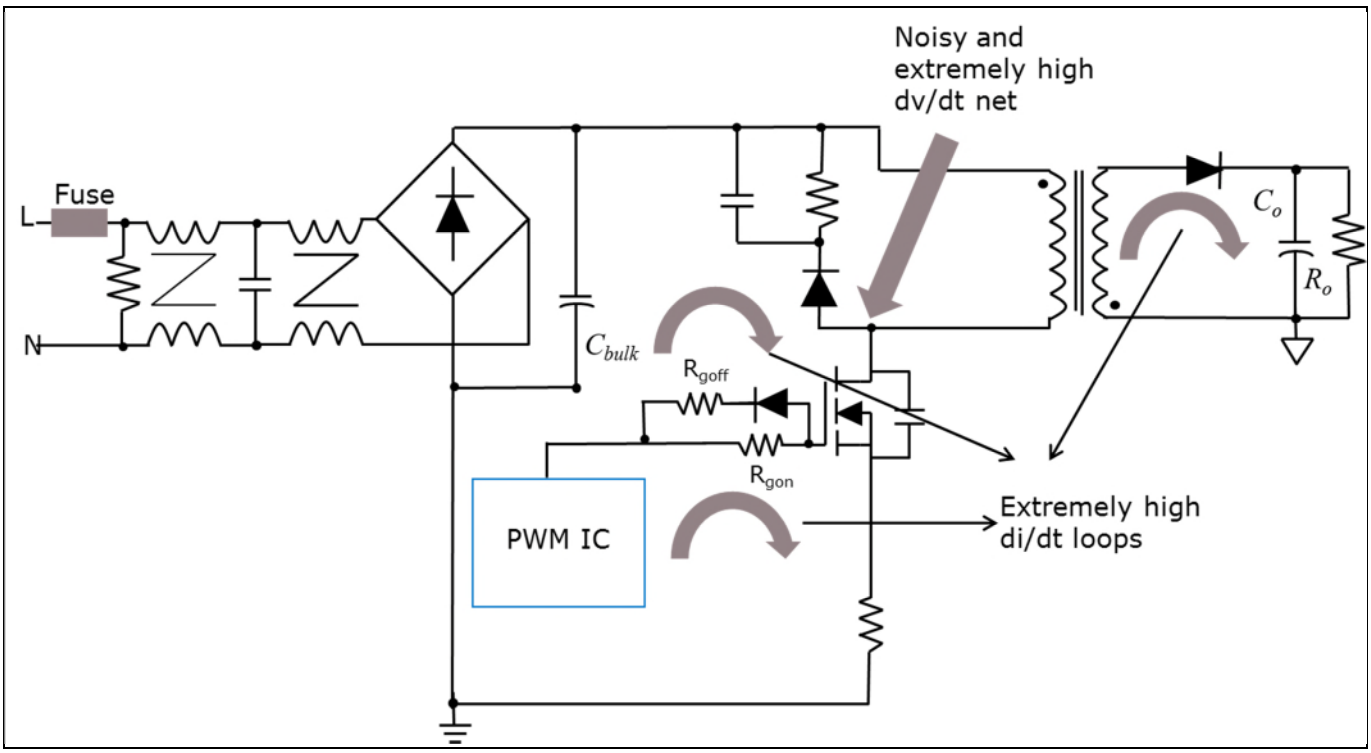


Figure 1 Typical flyback power supply and its dv/dt net, di/dt loops

To drive the MOSFET, separate turn-on and turn-off gate resistors are preferably used as shown in Figure 1. The series connected fast recovery diode is used to keep the gate resistance during turn-off lower than the gate resistance during turn-on. This is needed as the turn-off delay time is often longer than the turn-on delay time

for some of the power devices. It can also help to prevent a capacitive turn-on via the Miller capacitance. This also helps adjust the turn-on and turn-off behavior individually. Increasing R_{goff} leads to an increase in turn-off time, so the inductive peak overvoltage during turn-off will diminish. Increasing R_{gon} leads to an increase in turn-on time, effectively slowing the MOSFET switching speed. The reverse peak current of the free-wheeling diode will diminish. Turn-off time impacts efficiency and turn–on time impacts EMI performance. Therefore, the best compromise between efficiency and EMI has to be achieved by having a higher R_{gon} and lower R_{goff}. CoolMOS™ CE devices have R_g integrated into the device as shown in Figure 2.

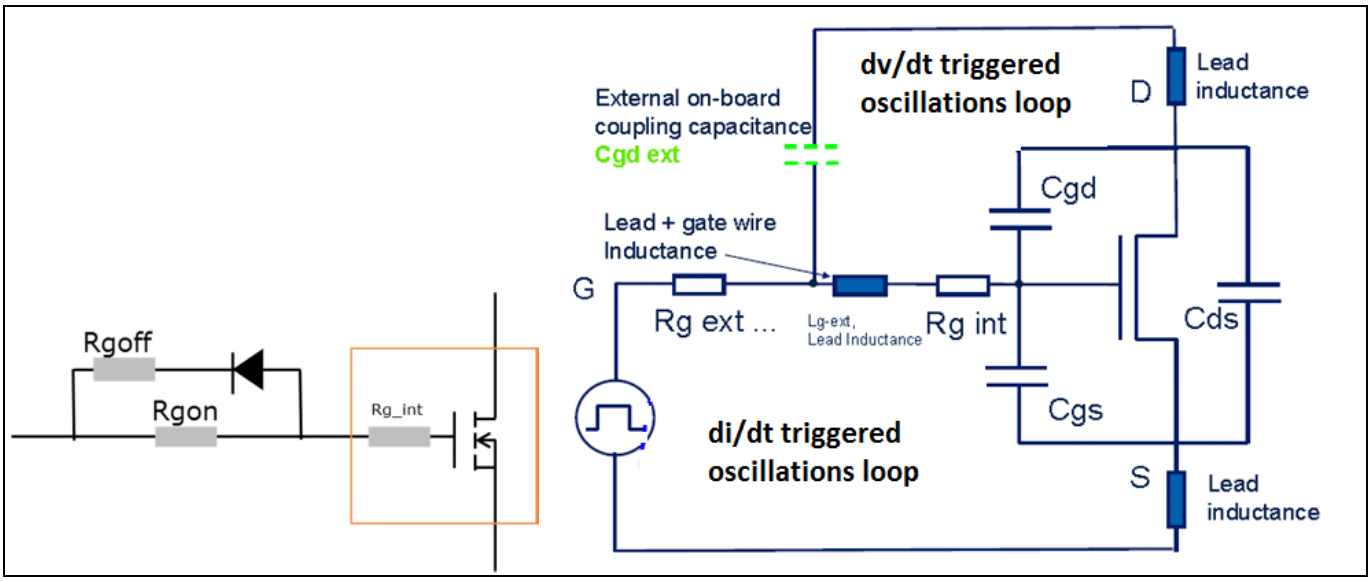


Figure 2 **Integrated R_g in CoolMOS™ CE and its used to limit dv/dt (red loop) and di/dt (blue loop) triggered oscillations.**

R_g affects both the dv/dt and di/dt of the MOSFET.

$dv/dt = V_{gs} / (R_g * C_{gd})$

di/dt = VL / L, where VL is the oscillation voltage added to the gate voltage V_{gs}

This internal R_g suppresses any oscillations that are caused by the external parasitics. Hence, with MOSFETs that have an internal R_g (such as the CoolMOS™ CE) it is safe to add external capacitance between the gate to drain (R_g_ext) and gate to source (C_{gs}_ext).

2 Reducing dv/dt and di/dt in CoolMOS™ CE

We discussed the basic concept of MOSFET dv/dt and di/dt in the previous section and have seen the typical nets and loops associated with these transients. Figure 3 shows the flyback power supply with different parasitics throughout the circuit.

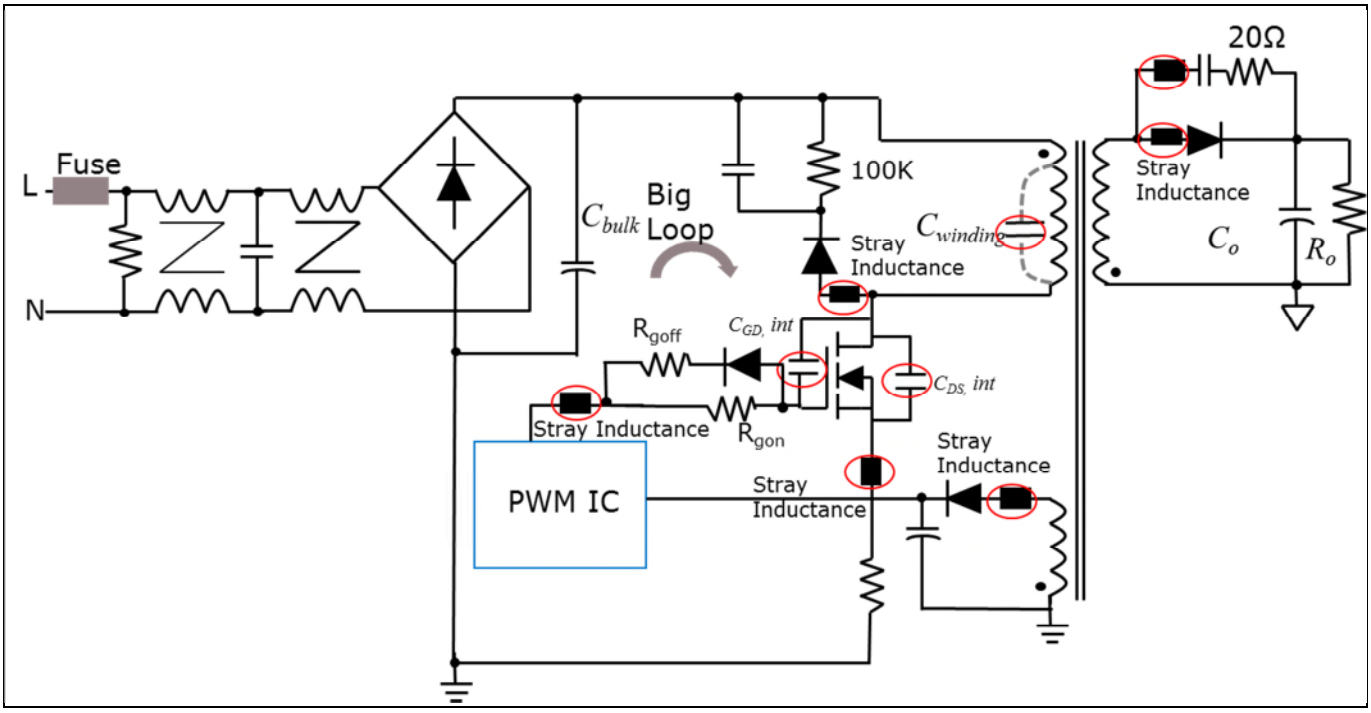


Figure 3 Flyback power supply and associated parasitics

The various parasitics include stray inductances at the drain and source of the MOSFET as well as stray inductance in the gate driving stage, stray inductances at the transformer output, output diode and the snubber stage. Stray inductance that is generally a few nanohenries in value often leads to large voltage overshoots based on the di/dt in the loop. Similarly, the stray capacitances that include the MOSFET internal parasitics (including output capacitance and transfer capacitances) and the transformer winding capacitances that cause currents due to the dv/dt present at that net. Hence, the interaction of these noise currents and voltages lead to EMI.

2.1 Reducing MOSFET di/dt

From the previous figure, the various di/dt sections which are present in the MOSFET drive stage cause the following effects

1. Noise voltage due to stray inductance at the gate
2. Noise voltage due to stray inductance at the source
3. Noise voltage due to stray inductance at the drain
4. Noise voltage due to big loop in the primary stage

If not already done by the optimal PCB layout, we start with reducing the PCB loop area around the primary switching node. This can be done by adding a high frequency, high voltage DC capacitor (preferably a ceramic

type) to reduce the effective loop area and the separate the high frequency and low frequency sections. This is shown as the CBP in Figure 4.

To slow the di/dt an extra, known inductance is added in the circuit. As this known inductance is in series with the stray inductance, the total value is always in the range of the added inductance which is known to the designer. A ferrite bead is a passive device that filters high frequency noise energy over a broad frequency range. It becomes resistive over its intended frequency range and dissipates the noise energy in the form of heat.

However, improper use of ferrite beads in system design can lead to some detrimental issues. Some examples are unwanted resonance due to combining the bead with a decoupling capacitor for low-pass filtering and the effect of dc bias current dependency that degrades the EMI suppression capability of the bead. With proper understanding and consideration of the ferrite bead's behavior, these issues can be avoided.

L_{bead}, the bead inductance is calculated by the following equation:

L_{bead} = XL / 2 x pi x f

From a typical ferrite bead datasheet, the region where the bead is most inductive gives the frequency f, for example f = 30 MHz, then the XL reactance at 30 MHz is found to be 233 Ω.

The above equation gives an inductance value (L_{bead}) of 1.2 µH for the typical ferrite bead. Most ferrite beads used in SMPS are in the range of 1.2 µH to 2.2 µH.

The parasitic capacitance and the DC resistance of the bead should be verified from the device datasheet so that the capacitive mode of operation and DC losses are minimized. Applying ferrite beads correctly can be an effective and inexpensive way to reduce high frequency noise and switching transients.

Thus, a properly selected ferrite bead can be placed at the di/dt transient sections of the MOSFET as shown in Figure 4. The di/dt of reverse recovery of the rectifier in the output and aux power circuit is controlled by switching on the primary side of the MOSFET. Hence, placing a bead at these points also helps reduce the EMI caused due to di/dt effects.

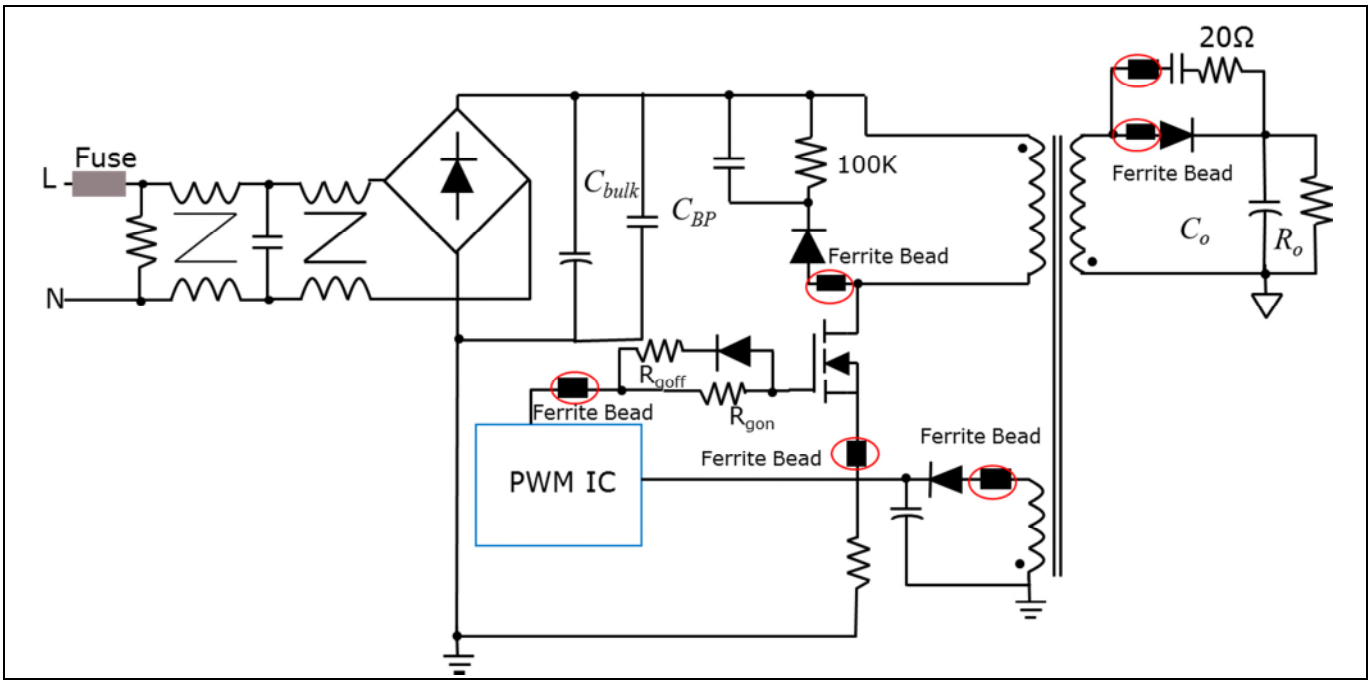


Figure 4 MOSFET di/dt reduction techniques

2.2 Reducing MOSFET dv/dt

A typical MOSFET turn-on and turn-off has been analyzed in many papers and some examples can be found in the reference section of this application note. A MOSFET can be modelled as shown in Figure 5. Our area of interest is the dv/dt feature of the MOSFET and the parasitics that impact this.

$dv/dt = V_{gsth} / (R_g * C_{gd})$

Hence, the lower the R_g and C_{gd}, the higher the dv/dt

$C_{oss} = C_{gd} + C_{ds}$

Hence, the lower the C_{oss}, the higher the dv/dt

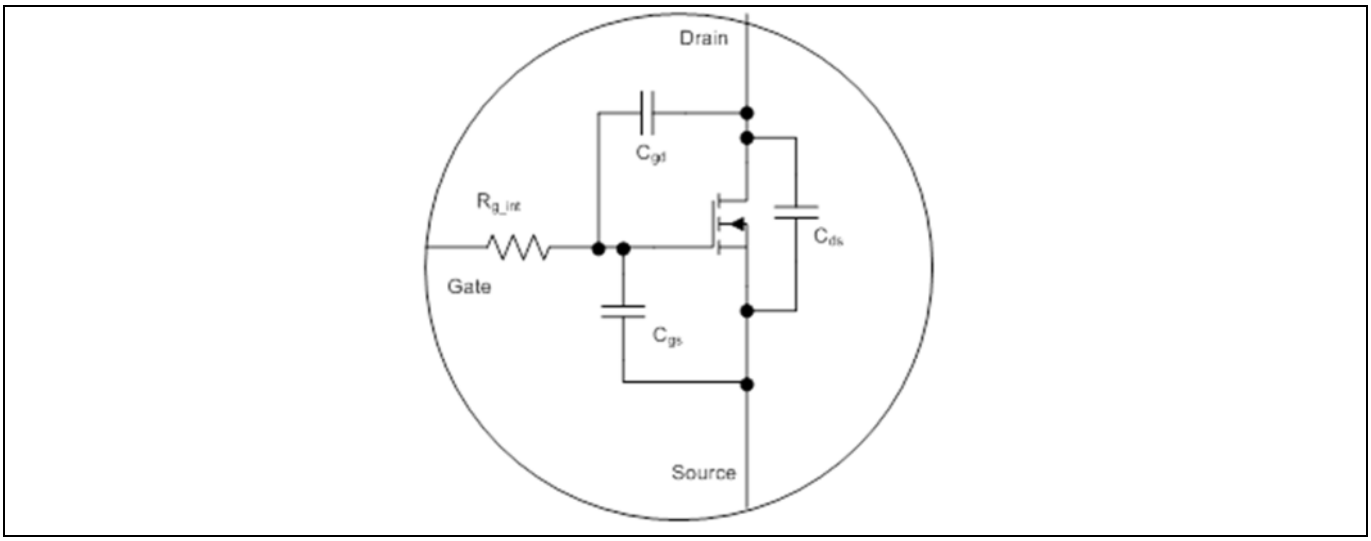


Figure 5 Typical MOSFET model

From above, we can clearly see the four parameters that can be modified to reduce dv/dt. They are:

Increasing C_{ds}

Increasing C_{gd}

Increasing R_g

Increasing C_{gs}

Higher C_{ds} reduces the dv/dt and reduces the V_{DS} overshoot.

Higher C_{gd} essentially increases the duration that the MOSFET stays in the Miller plateau and hence slows the dv/dt. This leads to increased switching losses thereby reducing the efficiency and increasing the temperature of the MOSFET.

The radiated noise of a quasi-resonant flyback converter mainly depends on the resonant capacitor, which is the C_{ds} of the MOSFET. Standard MOSFETs have a large C_{ds} and hence a slower dv/dt. The large C_{ds} also helps in meeting the radiated EMI. The efficiency of the quasi-resonant converter is higher with the non-ZVS condition and small C_{ds} as MOSFETs with a lower breakdown voltage and low on-resistance can be used. Therefore, if a small resonant capacitor (C_{ds}) is used considering the radiated noise; high efficiency can be achieved with the non-ZVS condition and a smaller resonant capacitor C_{gd}. Hence there is a tradeoff between meeting the radiated EMI requirement and meeting efficiency targets.

Hence, whenever the internal parasitics (C_{gd} and C_{ds}) of the MOSFET are low, it may become necessary to use an external C_{gd} and C_{ds} to ensure a reduced dv/dt. The external capacitors are in the range of 10 pF to 100 pF and give the designer a fixed value for these parasitic capacitances to design with. Standard MOSFETs have larger internal C_{gd} and C_{ds} capacitances as seen in their datasheets. Hence, when they are replaced by CoolMOS™ CE, external C_{ds} and C_{gd} are needed to slow the fast switching SJ MOSFET.

An external C_{gs} capacitor can also be added at the gate, but this option is rarely used as increasing the gate resistor R_g is relatively simpler.

As discussed in the earlier part of this application note, it is preferred to have different set of R_g values in the turn-on and turn-off conditions of the MOSFET. To reduce switch-off losses, a lower value of $R_{g,off}$ is required. To reduce turn-on voltage spikes, a higher value of $R_{g,on}$ is required. The internal R_g inside the MOSFET is needed to ensure smooth turn-on and turn-off behavior by internally damping the oscillations due to poor PCB layout. CoolMOS™ CE has an integrated R_g that calls for careful selection of the external $R_{g,on}$ and $R_{g,off}$ (which should include the internal R_g values based on the Rdson used).

A higher R_g value not only degrades the MOSFET's working conditions by increasing the temperature and switching losses, it also degrades application efficiency and working conditions by fully modifying the switching behavior of the device. A higher R_g heavily affects the driver/PWM controller, requiring it to sustain a higher temperature, as well as dissipating more power to charge the MOSFET input capacitance. It is also potentially produces cross conduction that may cause system disruption due to static dv/dt. The techniques for reducing dv/dt are summarized in Figure 6.

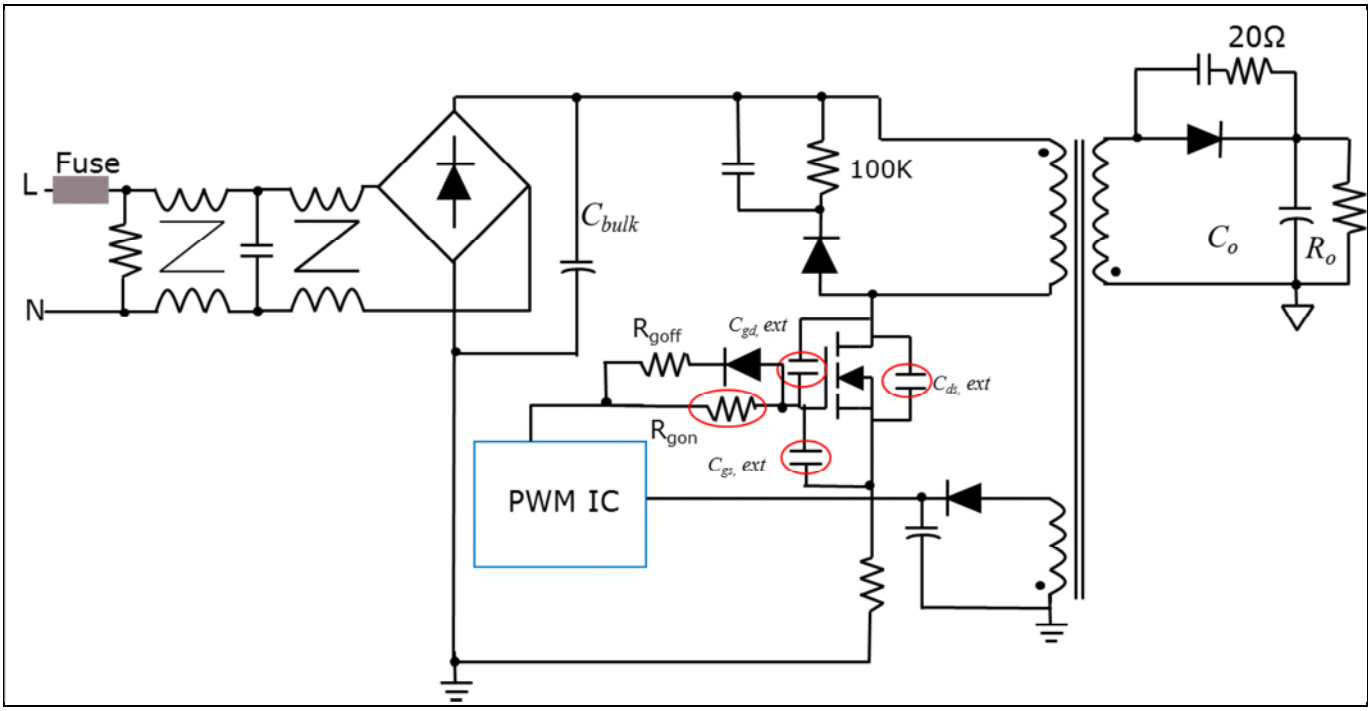


Figure 6 MOSFET dv/dt reduction techniques – adding external capacitors and increasing R_g

3 Reading EMI measurement plots

The typical conducted and radiated EMI limit lines are shown in Figures 7 and 8.

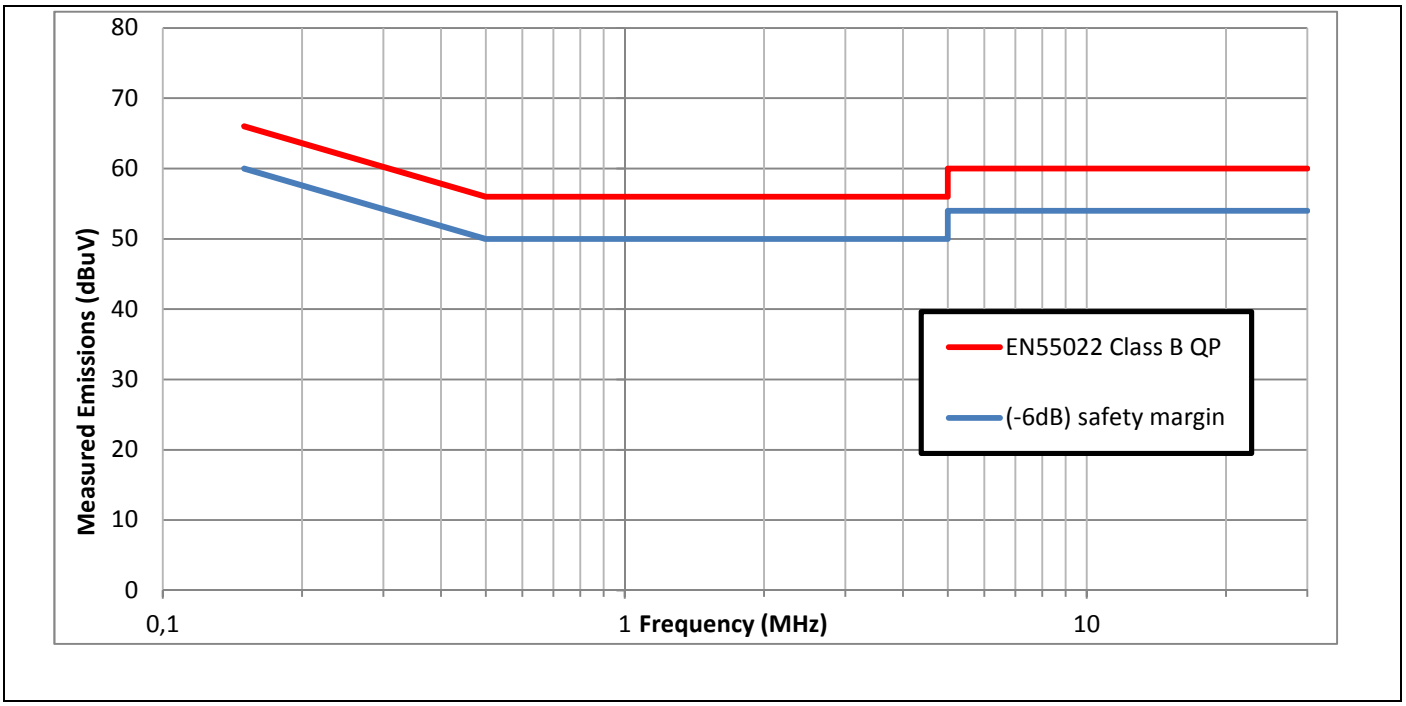


Figure 7 Conducted emission test limits – 150 kHz to 30 MHz

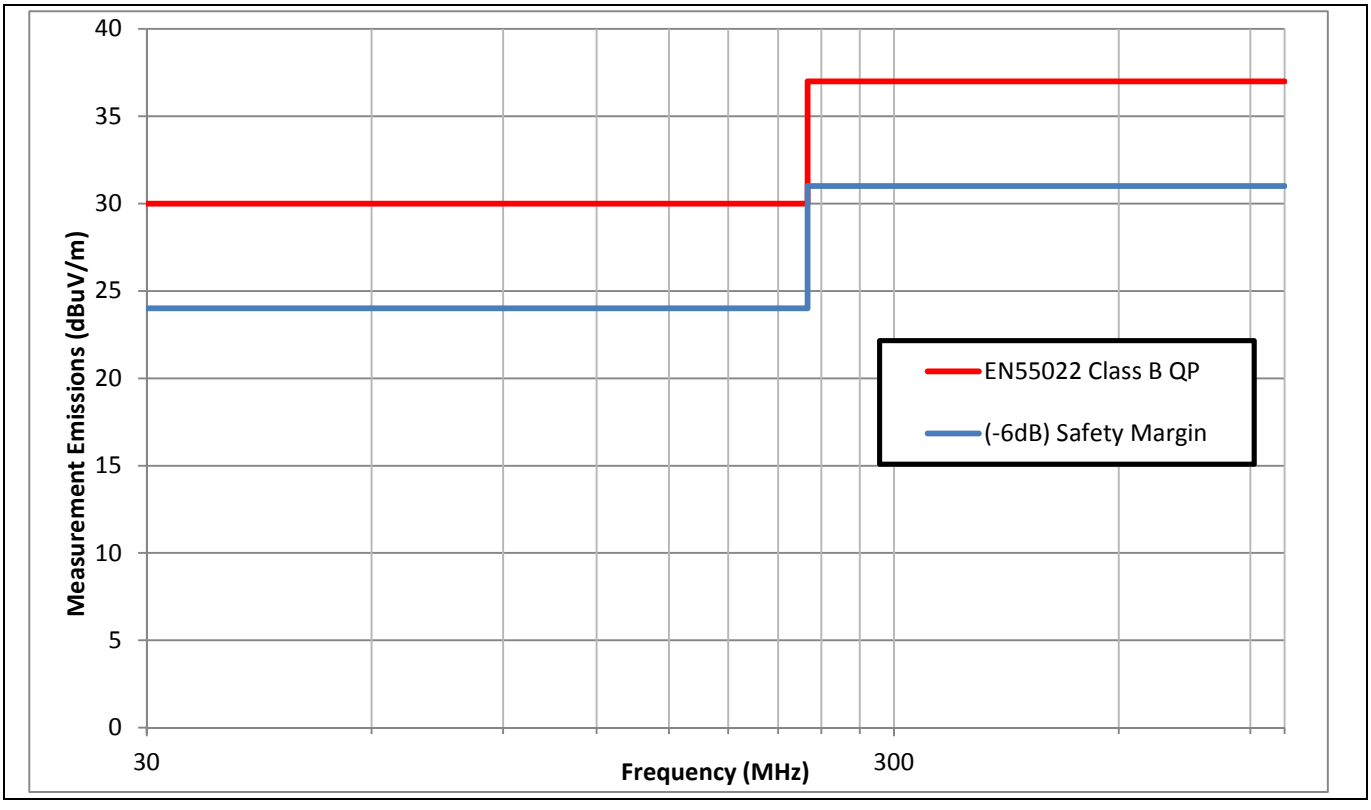


Figure 8 Radiated emission test limits – 30 MHz to 1 GHz

Based on the detector used in the spectrum analyzer, average, quasi-peak (QP) or peak measurements can be obtained. Peak detection will always give the highest reading, followed by QP and then average readings. Therefore, to perform EMI scans quickly most engineers prefer peak detection and then compare the results against QP limits. It this condition is met, then in effect additional headroom (safety margin) is achieved. QP detection should only be performed when the peak detection test (with QP limits applied) marginally fails.

Typically, a -6 dB safety margin is desired to account for measurement inaccuracy, board to board variations etc. Usually, if the QP limits are met the average limits (using average detection and average limits) are also met. At frequencies below approximately 5 MHz, the noise currents tend to be predominantly differential mode, whereas at frequencies above 5 MHz the noise currents tend to be predominantly common mode. At frequencies above 20 MHz, the conducted noise is attributed to inductive pickup, which can be the radiation from the input or output cables.

Meeting conducted emission specifications does not necessarily confirm that the radiated emission specification would be met, whereas meeting the radiated emission specification in most cases leads to meeting the conducted emission specifications as well. Hence, in order to save time, designers often tend to first check the radiated emissions. In the next section of the application note, various before and after EMI results are shown. Using the techniques of MOSFET di/dt and dv/dt reduction, CoolMOS™ CE can successfully meet EMI requirements. We also apply the lessons learnt in the previous sections of the application note and develop a quick-fix table which helps CoolMOS™ CE meet EMI test requirements.

4 Practical measurement results from various test cases

We will now look at implementing the lessons learnt in the above sections of this application note within three different, but typical, uses of CoolMOS™ CE.

1. Optimizing an AC-DC SMPS originally optimized for standard MOSFET – here CoolMOS™ CE is replacing a standard MOSFET.
2. Optimizing an AC-DC SMPS originally optimized for a SJ MOSFET – here CoolMOS™ CE is replacing a different technology SJ MOSFET .
3. Optimizing an AC-DC SMPS originally optimized for CoolMOS™ CE – here the SMPS design was started with CoolMOS™ CE.

4.1 Optimizing an AC-DC SMPS originally optimized for standard MOSFET – CoolMOS™ CE is replacing a standard MOSFET

As efficiency improvement is one of the key goals for an AC-DC adapter designer. Therefore, a SJ MOSFET is always a first choice as the switching MOSFET. Due to cost constraints designers may be forced to use a standard MOSFET. The price attractiveness and multiple package options with various $R_{DS(ON)}$ choices in the CoolMOS™ CE portfolio make it a preferred option for designers who are considering replacing the standard MOSFETs in their designs.

The circuit under consideration is shown in Figure 9:

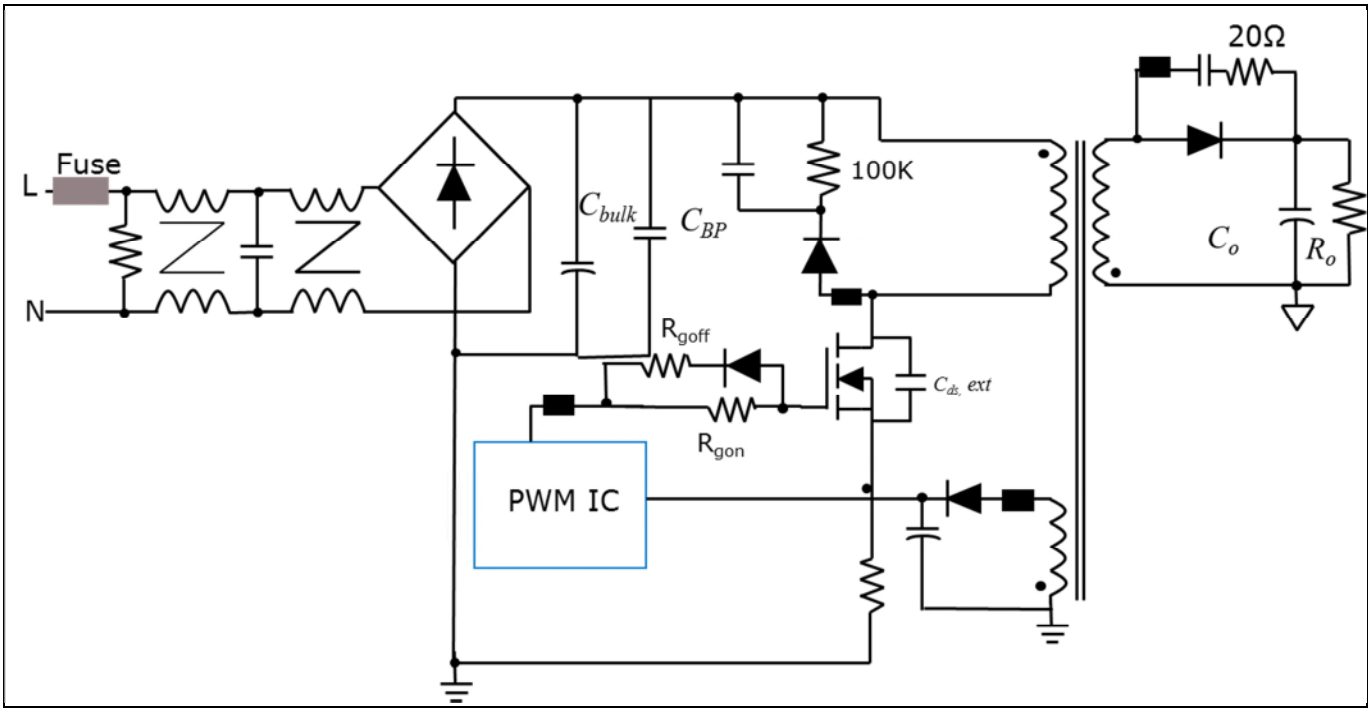


Figure 9 Typical flyback power supply – 30 W to 65 W output power

We looked at a few adapters with different power levels from 30 W to 65 W available off the shelf from various vendors. In all these products some dv/dt and di/dt reduction techniques were already implemented as summarized in Figure 15. The typical approach followed when replacing a standard MOSFET with CoolMOS™ CE is shown in Figure 10.

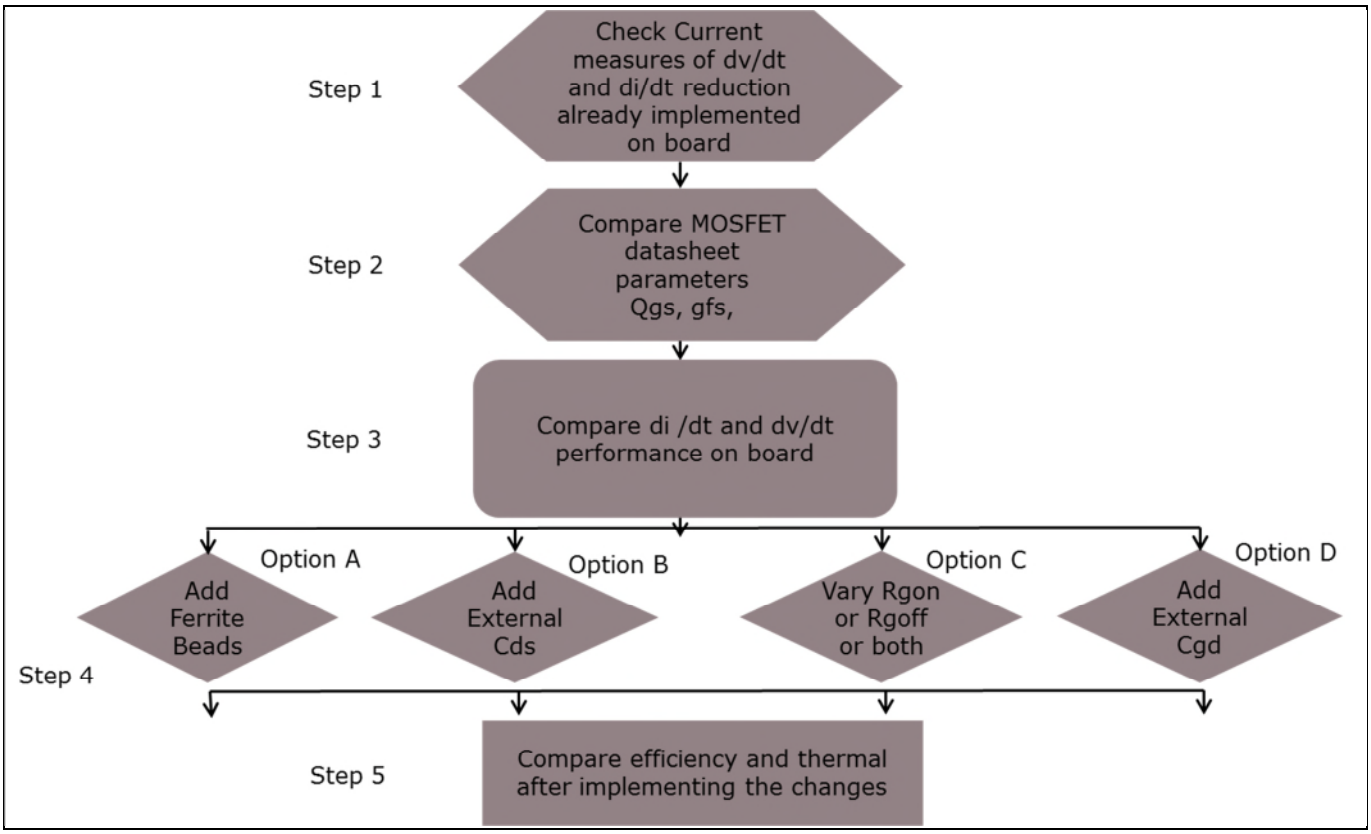


Figure 10 **Flowchart for replacing standard MOSFET with CoolMOS™ CE**

The steps shown in the flowchart above are explained in detail below:

Step 1: Check existing approaches for di/dt and dv/dt reduction by visual inspection of the SMPS PCB or by reviewing the schematics.

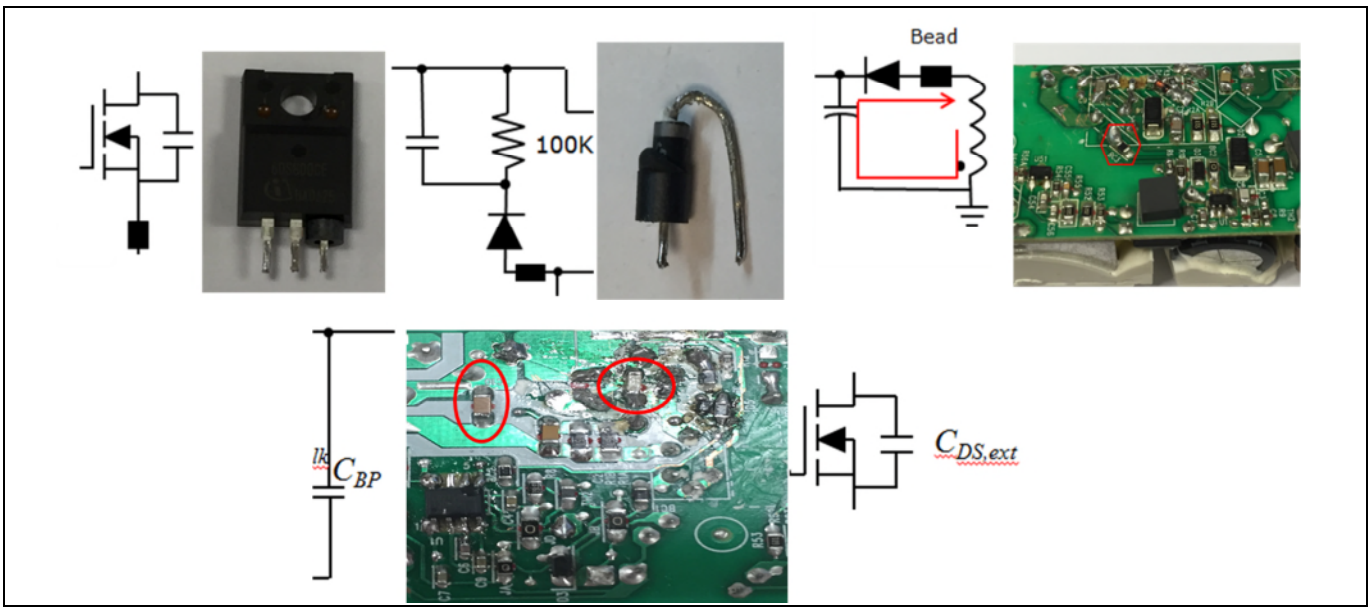


Figure 11 **Visual inspection of various di/dt and dv/dt measures approaches in an AC-DC SMPS – (A) beads for di/dt reduction at the MOSFET source, primary snubber diode (B) high frequency bypass capacitor CBP and external C_{ds}**

Step 2: Compare datasheet parameters to ensure the differences between the standard MOSFET and CoolMOS™ CE are identified and modifications required can be estimated as shown in Figure 19.

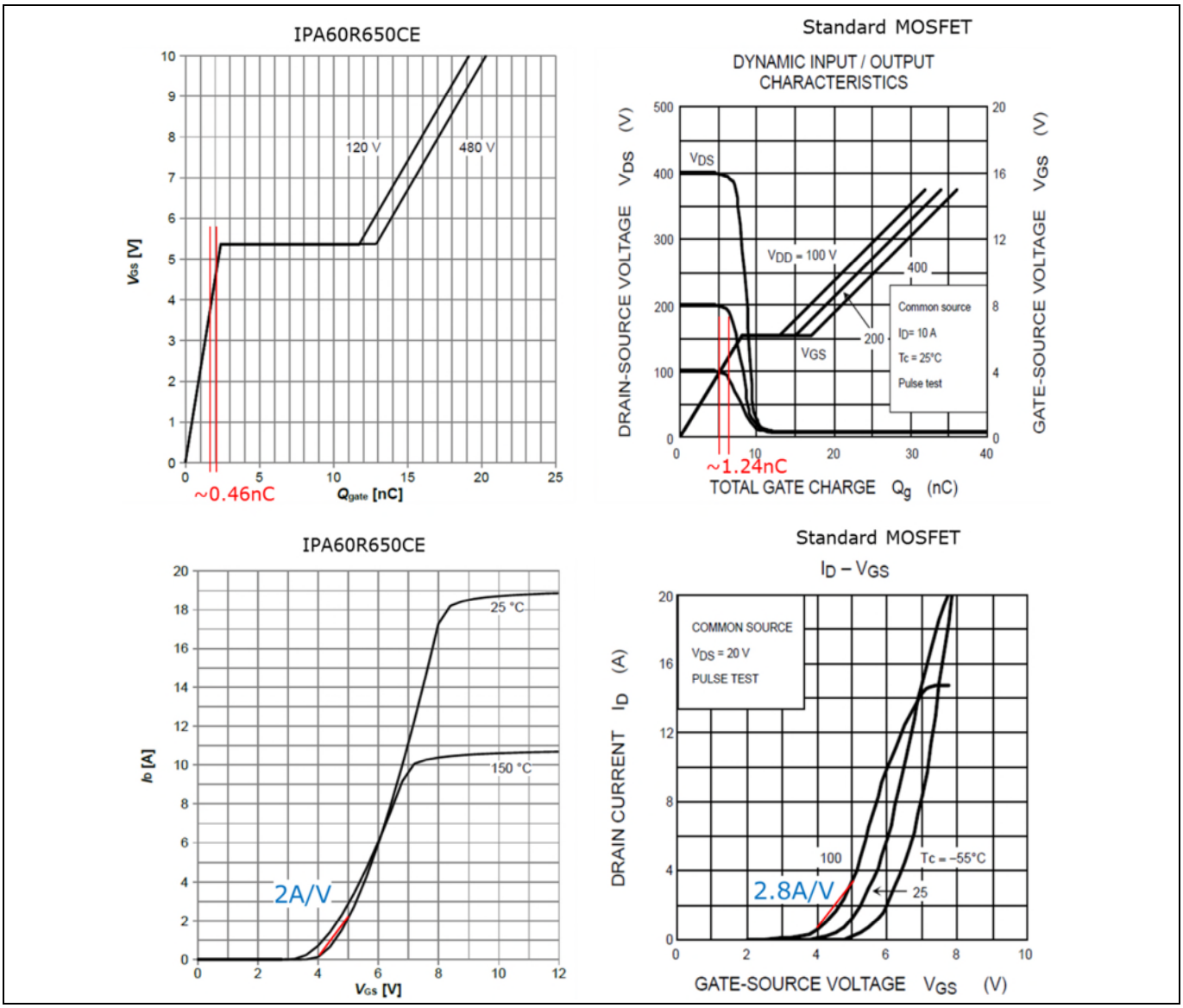


Figure 12 **CoolMOS™ CE and Standard MOSFET datasheet comparison. (A) Q_{gs} to determine the charging time of V_{GS}. (B) gfs determine the $R_{ds(on)}$ changing rate vs V_{GS}**

Based on the above comparison: From Q_{gs} and g_{fs} curves determine di/dt of the devices

$$\frac{di}{dt} = \frac{g_{fs} \times \Delta V}{\frac{Q_{gs}}{I_{driving}}} = \frac{g_{fs} \times \Delta V}{\frac{Q_{gs} \times R_{g,on}}{V_{driving}}}$$

For CoolMOS™ CE

$$Q_{gs} = 0.46nC \ @VGS = 4\ V \rightarrow 5\ V$$

Assume $V_{driving}$ = 5 V, $R_{g,on}$ = 200 Ω

$I_{driving}$ = 5/200 =25 mA, $t_{driving}$ = 18.4 ns

g_{fs} =2 A/V $@VGS = 4\ V \rightarrow 5\ V$

di/dt of MOSFET @$VGS = 4\ V \rightarrow 5\ V$

di/dt (CoolMOS™ CE) =2 A/18.4 ns= 108 A/us

For standard MOSFET:

$$Q_{gs} = 1.24nC\ @VGS = 4\ V \rightarrow 5\ V$$

Assume $V_{driving}$ = 5 V, $R_{g,on}$ = 200 Ω

$I_{driving}$ = 5/200 = 25 mA, $t_{driving}$ = 49.6 ns

g_{fs} = 2.8 A/V@$VGS = 4\ V \rightarrow 5\ V$

di/dt of MOSFET @$VGS = 4\ V \rightarrow 5\ V$

di/dt (standard MOSFET) =2.8 A/49.6 ns=56.4 A/µs

Hence from the datasheet comparison:

1. g_{fs} of 650CE is 70% of Standard MOSFET

2. Q_{gs} of 650CE is 37% of Standard MOSFET

To maintain the same di/dt of MOSFET SW ON

$$R_{g,on(CE)} = \frac{\frac{g_{fs,CE}}{Q_{gs,CE}}}{\frac{g_{fs}}{Q_{gs}}} R_{g,on,original}$$

$R_{g,on}$ of 650CE is 189% of standard MOSFET to have similar di/dt as MOSFET switching ON.

Step 3 and step 4: Compare switching waveforms to get an estimate of the di/dt and reconfirm our previous finding that higher $R_{g,on}$ is required to suppress the di/dt of CoolMOS™ CE. Also compare the dv/dt to check the parasitic capacitance effects. See Figure 20 for di/dt suppression using $R_{g,on}$.

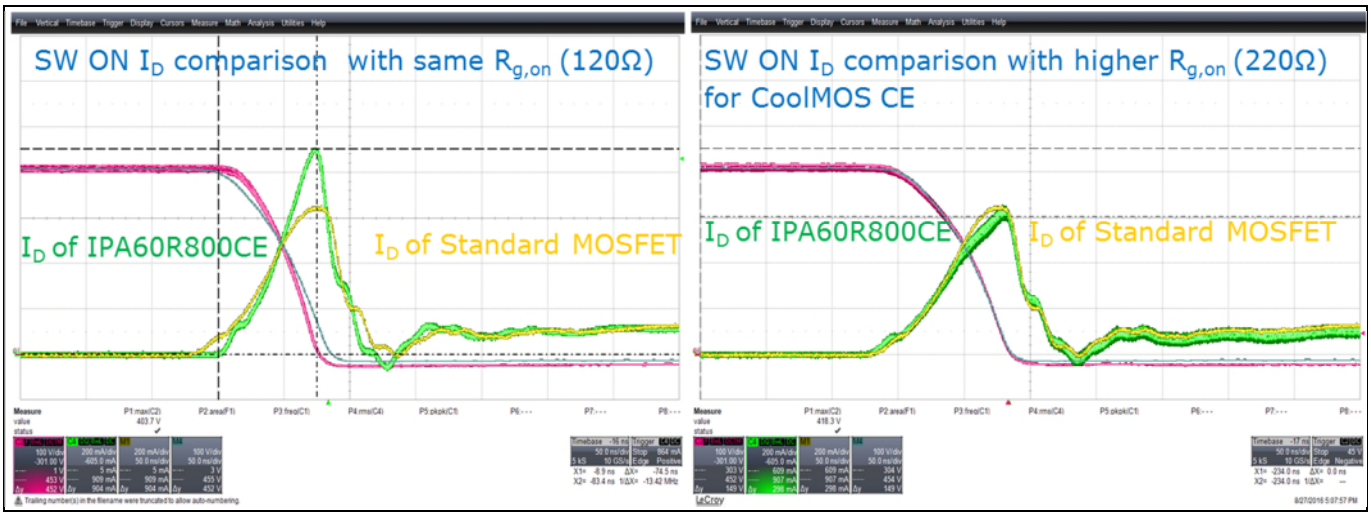


Figure 13 di/dt suppression with higher $R_{g,on}$ for CoolMOS™ CE. With higher $R_{g,on}$ di/dt of both the standard MOSFET and CoolMOS™ CE are similar

This higher $R_{g,on}$ also suppresses the voltage spike on the secondary synchronous MOSFETs (if used) when the primary CoolMOS™ CE turns-on.

The side effect of increasing $R_{g,on}$ is an increase in the switching losses as shown in Figure 14 below.

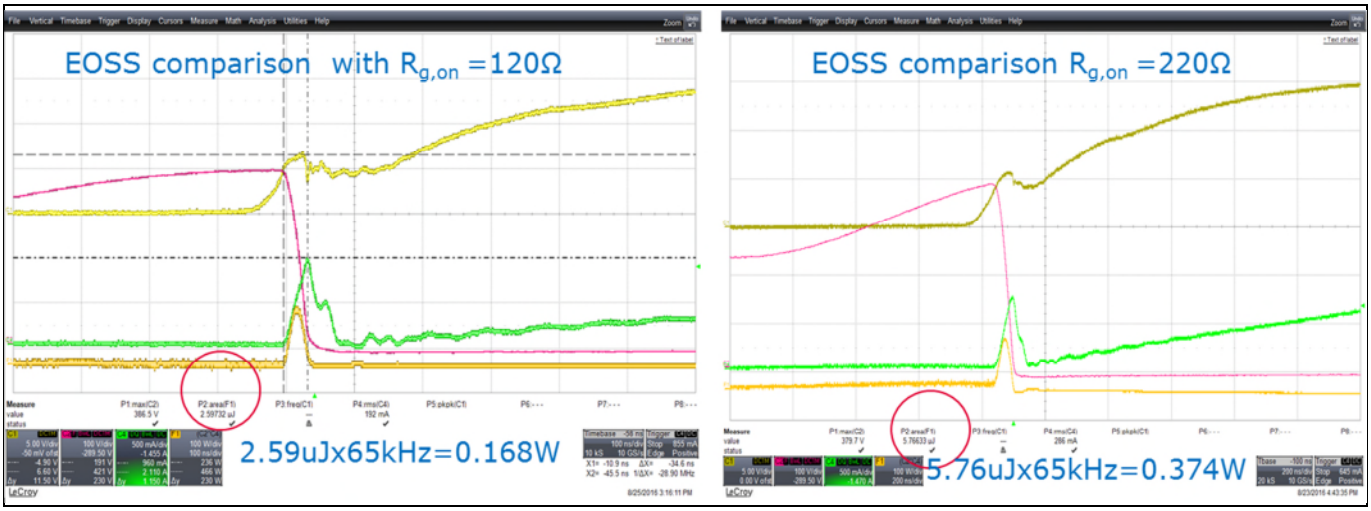


Figure 14 **CoolMOS™ CE E_{oss} comparisons between two $R_{g,on}$ selected based upon di/dt suppression to meet standard MOSFET di/dt. Switching losses double with doubling $R_{g,on}$**

CoolMOS™ CE has high di/dt and dv/dt switching off behaviour under the same condition when compared to a standard MOSFET. This can be seen in Figure 15. An external C_{ds} is required to match the device turn-off performance.

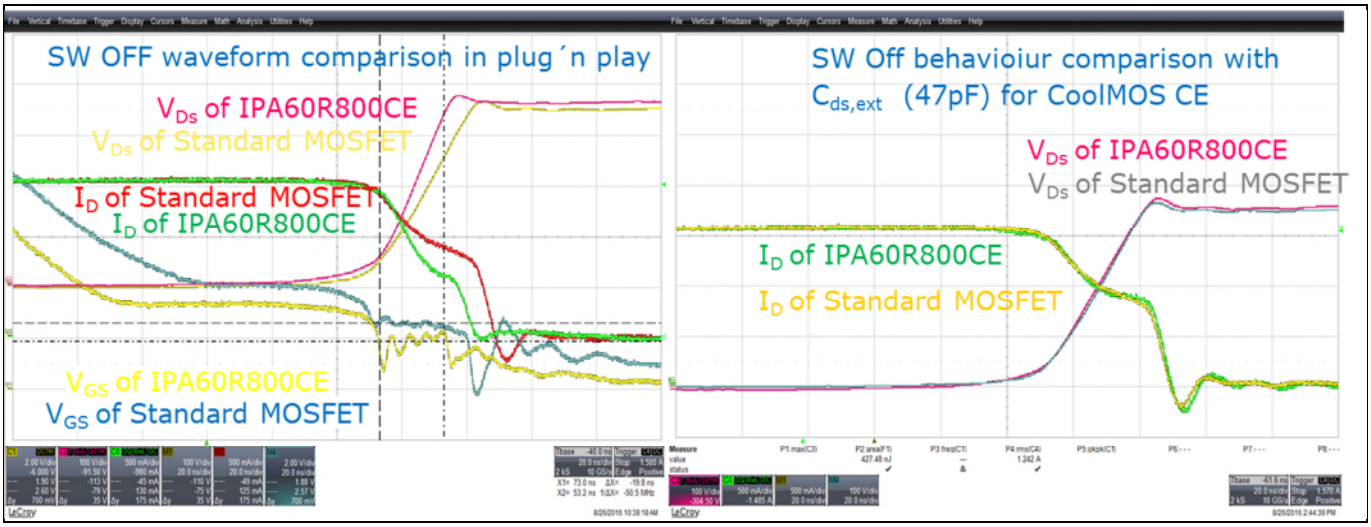


Figure 15 **CoolMOS™ CE switch-off (SW Off) behavior in plug and play and with an external C_{ds} (47 pF) required to match the switching behavior of the standard MOSFET.**

The switching loss comparison between CoolMOS™ CE and a standard MOSFET in plug and play is as shown in Figure 15 and with the external C_{ds} of 47 pF is shown in Figure 16. It can be seen that CoolMOS™ CE switching losses increase due to the addition of an external C_{ds}.

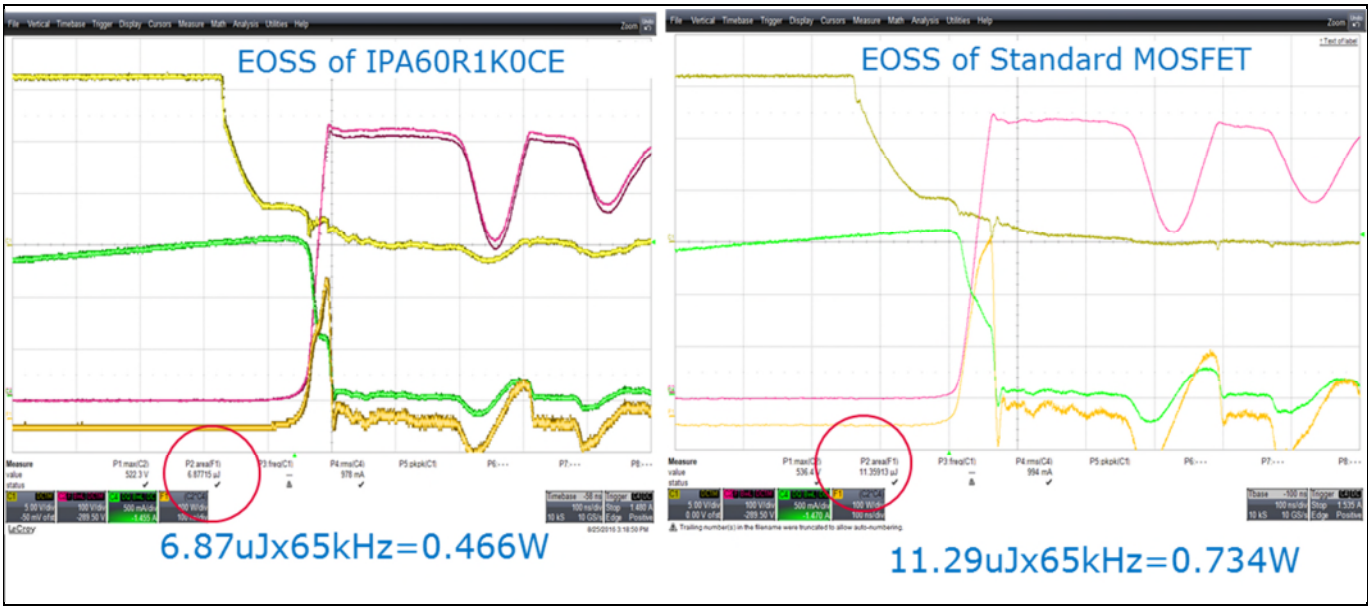


Figure 16 CoolMOS™ CE shows lower switching losses in plug and play

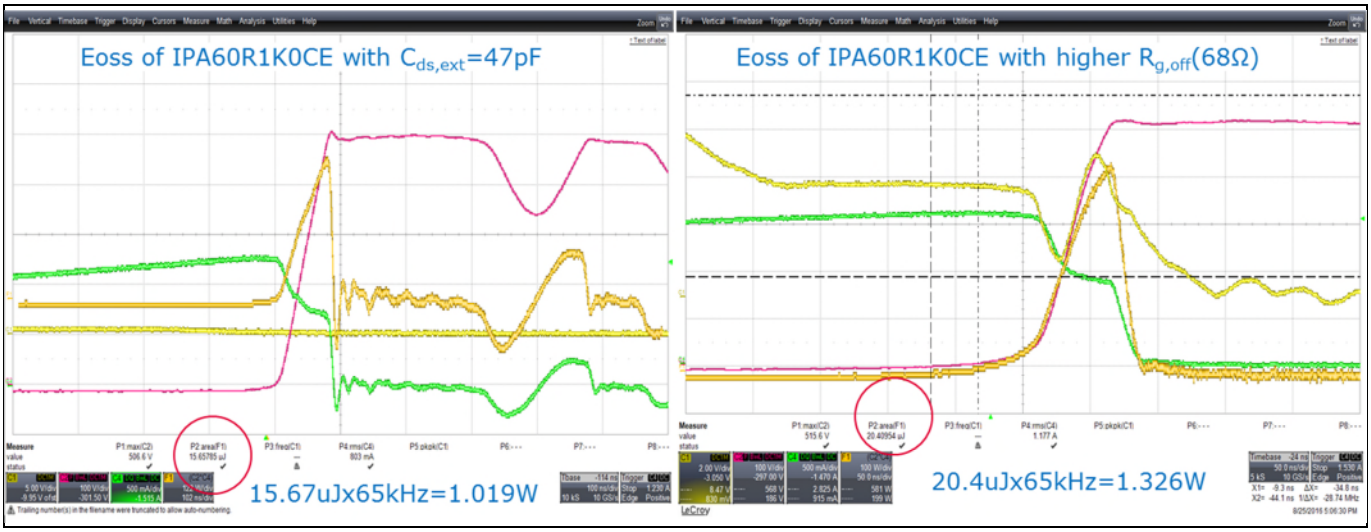


Figure 17 CoolMOS™ CE switching losses are increased by adding an external C_{ds} of 27 pF and increasing $R_{g,off}$ to 68 Ω which were needed to meet EMI performance at a similar level to a standard MOSFET.

Step 5: With all the necessary modifications performed by comparing the device datasheets and on board performance by comparing switching waveforms, CoolMOS™ CE was successfully meeting the EMI requirements at a level similar to standard MOSFET. As a final step it is advised to compare efficiency and thermal performance to ensure required performance.

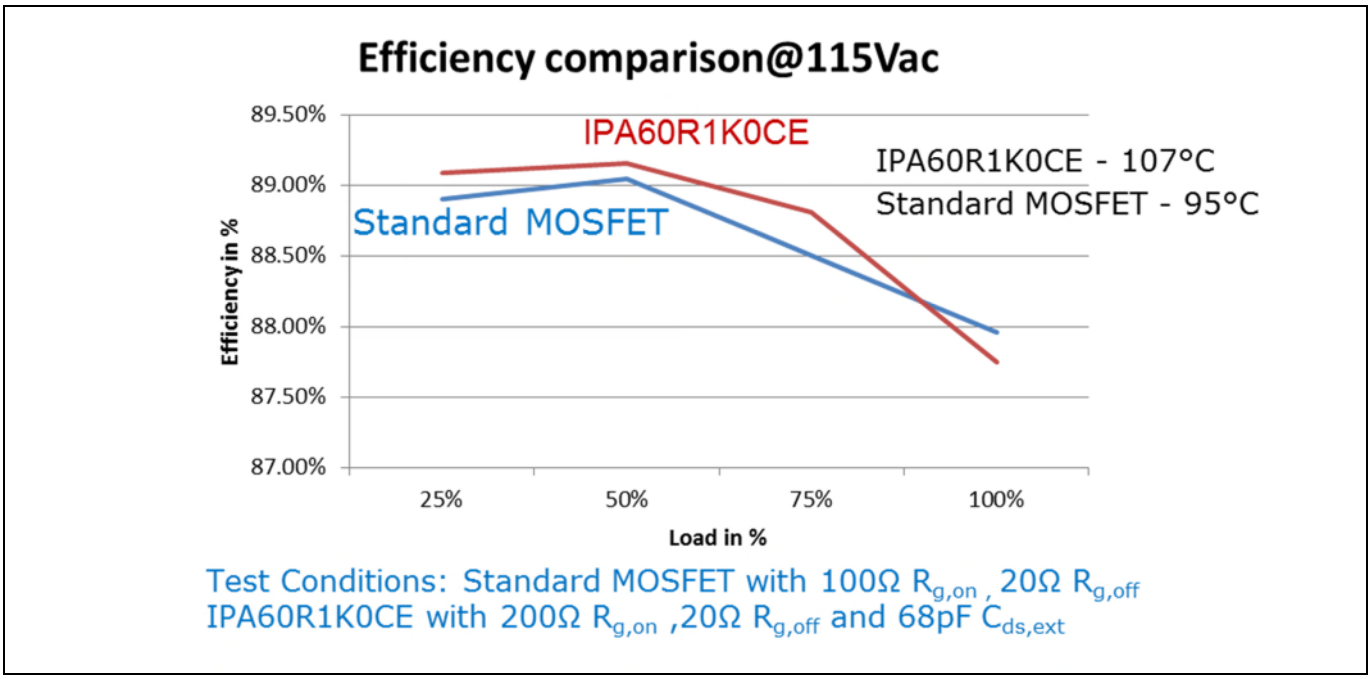
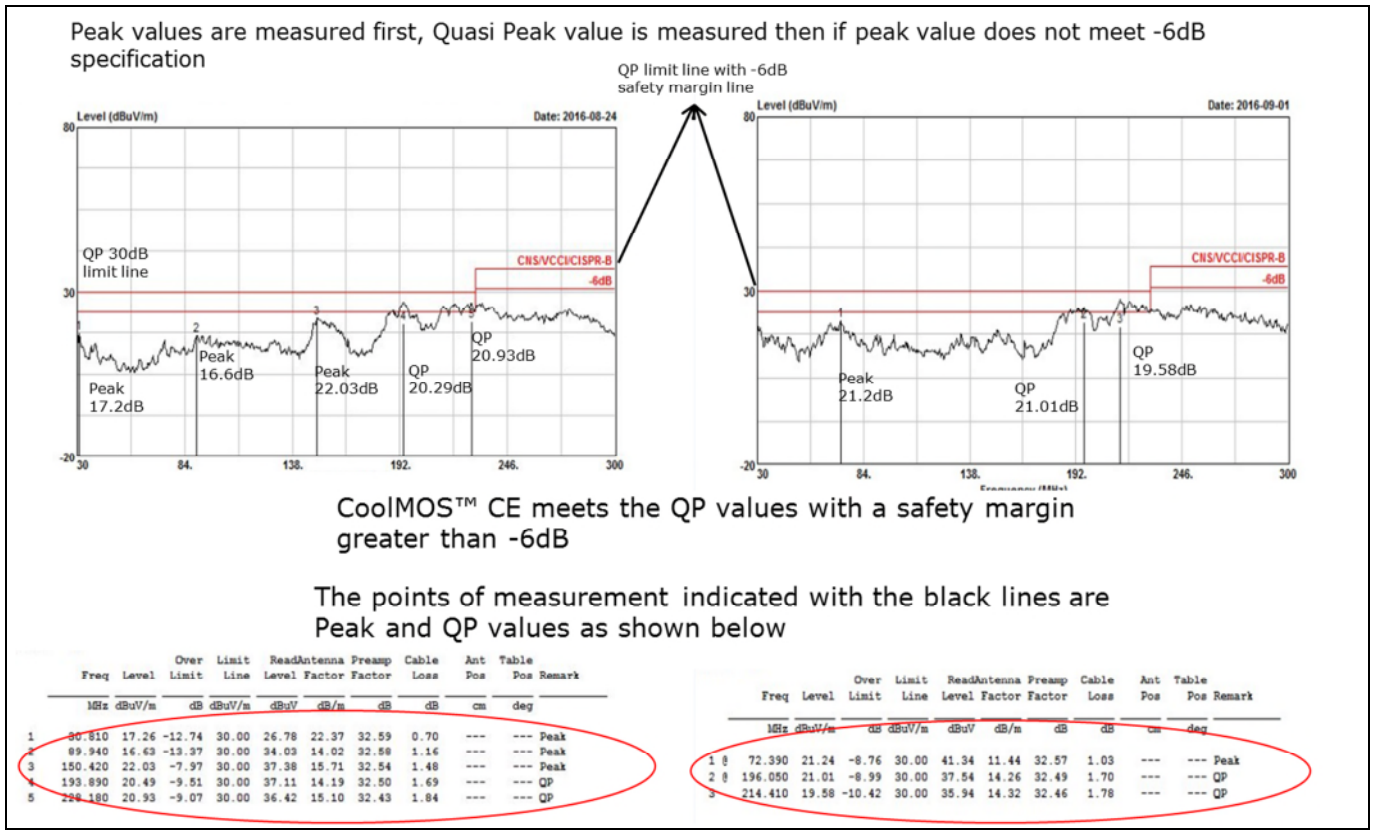


Figure 18 **In a 45 W adapter application, it can be seen that CoolMOS™ CE efficiency performance is better than with a standard MOSFET even with the additional measures of a higher $R_{g,on}$ and an external C_{ds} needed to meet EMI requirements. The thermal performance is lower due to the forced higher switching losses in the device. This is below the acceptable thermal limit of 110°C and hence CoolMOS™ CE was successfully qualified. The difference in full load efficiency is due to the lower $R_{ds,on}$ of the standard MOSFET.**

EMI comparison results are as shown in figure 19



	Freq	Level	Over Limit	Limit Line	ReadAntenna Level	Antenna Factor	Preamp Factor	Cable Loss	Ant Pos	Table Pos	Remark
	MHz	dBuV/m	dB	dBuV/m	dBuV	dB/m	dB	dB	cm	deg	
1	30.810	17.26	-12.74	30.00	26.78	22.37	32.59	0.70	---	---	Peak
2	89.940	16.63	-13.37	30.00	34.03	14.02	32.58	1.16	---	---	Peak
3	150.420	22.03	-7.97	30.00	37.38	15.71	32.54	1.48	---	---	Peak
4	193.890	20.49	-9.51	30.00	37.11	14.19	32.50	1.69	---	---	QP
5	228.180	20.93	-9.07	30.00	36.42	15.10	32.43	1.84	---	---	QP

	Freq	Level	Over Limit	Limit Line	ReadAntenna Level	Antenna Factor	Preamp Factor	Cable Loss	Ant Pos	Table Pos	Remark
	MHz	dBuV/m	dB	dBuV/m	dBuV	dB/m	dB	dB	cm	deg	
1 @	72.390	21.24	-8.76	30.00	41.34	11.44	32.57	1.03	---	---	Peak
2 @	196.050	21.01	-8.99	30.00	37.54	14.26	32.49	1.70	---	---	QP
3	214.410	19.58	-10.42	30.00	35.94	14.32	32.46	1.78	---	---	QP

Figure 19 **IPA60R1K0CE CoolMOS™ CE successfully meets the EMI requirements of a 45 W adapter with >6 dB safety margin**

A summary table is shown in Figure 28 for the various power supplies tested. This table is adapted to similar steps from 1 to 5 as discussed above. At all power levels CoolMOS™ CE successfully met the EMI requirements with a reduction of di/dt and dv/dt similar to standard MOSFET performance.

Adapter	Output Power		65W	65W	65W	45W	27W	65W	30W
Original with Standard MOSFET		Rg,on	150Ω+bead	300+10Ω	270+100Ω	100+20Ω	(100+0)Ω	200+0Ω	100+15Ω
		Rg,off	Bead	100Ω	100Ω	20Ω	0Ω	0Ω	15Ω
		Cds	33pF	100pF	NC	NC	47pF	NC	NC
	Snubber for Primary MOSFET	C	1nF	2.2nF	3.3nF	12nF	2.2nF	10nF	1nF
		R	300kΩ	86kΩ	102kΩ	102kΩ	102kΩ	102kΩ	470kΩ
		D	-	-	Yes	Yes	Yes	-	-
		Bead Core	Yes	-	-	-	-	-	-
	Snubber for Output Rectifier	C	1nF	1nF	330pF	1nF	1nF	1nF	1nF
		R	10Ω	47Ω	47Ω	20Ω	7.5Ω	10Ω	27Ω
		Bead Core	None	Yes	Yes	None	Yes	-	-
CoolMOS™ CE series of similar Rdson and Voltage class of Standard MOSFET		Rg,on	150Ω+bead	400+10Ω	270+100Ω	200+20Ω	(240+0)Ω	200+0Ω	100+15Ω
		Rg,off	150Ω+bead	100Ω	100Ω	20Ω	0Ω	0Ω	15Ω
		Cds	100pF	100pF	100pF	47pF	100pF	100pF	47pF
	Snubber for Primary MOSFET	C	1nF	2.2nF	3.3nF	12nF	2.2nF	10nF	1nF
		R	300kΩ	86kΩ	102kΩ	102kΩ	102kΩ	102kΩ	470kΩ
		D	-	YES	YES	Yes	-	-	-
		Bead Core	Yes	None	None	-	-	-	-
	Snubber for Output Rectifier	C	1nF	1nF	330pF	1nF	1nF	1nF	1nF
		R	10Ω	47Ω	47Ω	20Ω	7.5Ω	10Ω	27Ω
		Bead Core	None	None	Yes	None	Yes	-	-

Option A:adding beads
Option B: Adding external Cds
Option C: Increasing Rg

A B C C B C B C B B B

Figure 20 IPA60R1K0CE CoolMOS™ CE successfully meets the EMI requirements in standard off the shelf adapters with 30 W to 65 W output power

4.2 Optimizing an AC-DC SMPS originally optimized for superjunction MOSFET – CoolMOS™ CE is replacing a superjunction MOSFET with different technology

Very often the efficiency provided by SJ MOSFETs is significantly higher, and in designs where cost constraints overtake the performance criteria there is an option to look at higher $R_{DS(ON)}$ variants.

Here we will look at a design where Infineon´s IPI65R600C6 was replaced by an IPI70R950CE in a 25 W charger application.

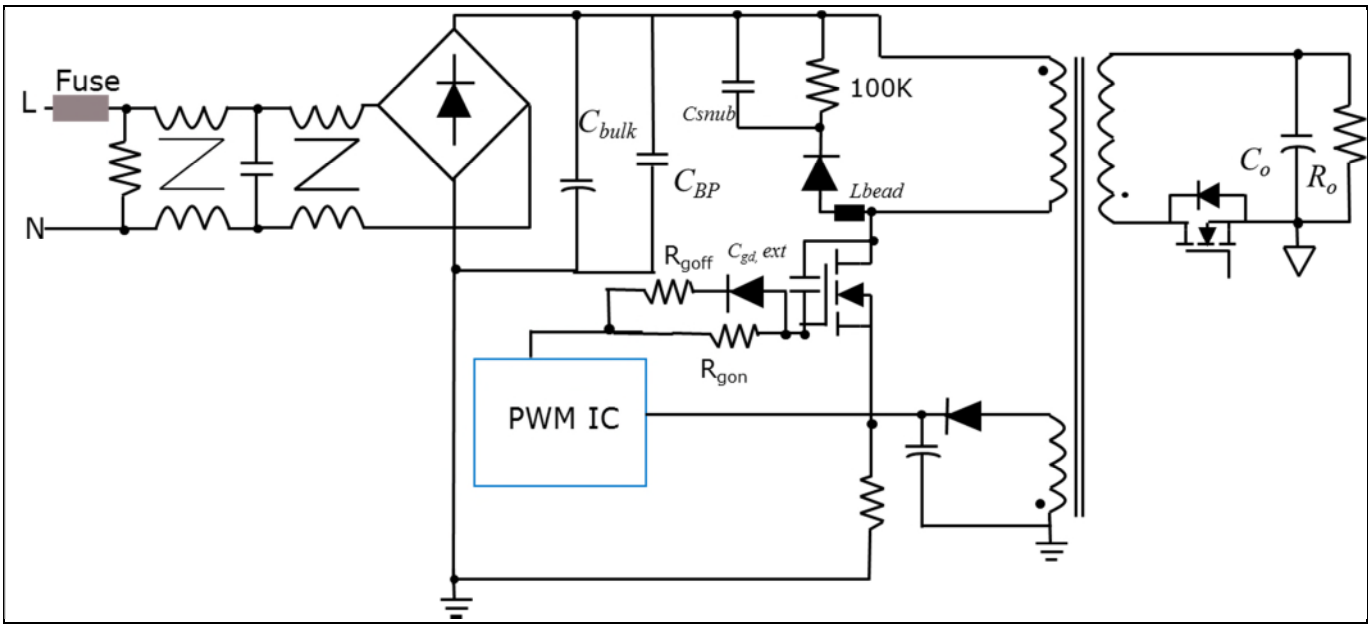


Figure 21 Typical 25 W AC-DC charger SMPS

We will follow a similar flowchart approach to the one we used in the previous example - with few changes. As the aim of moving to a higher $R_{ds,on}$ is to reduce efficiency, we focus mainly on the EMI aspect here.

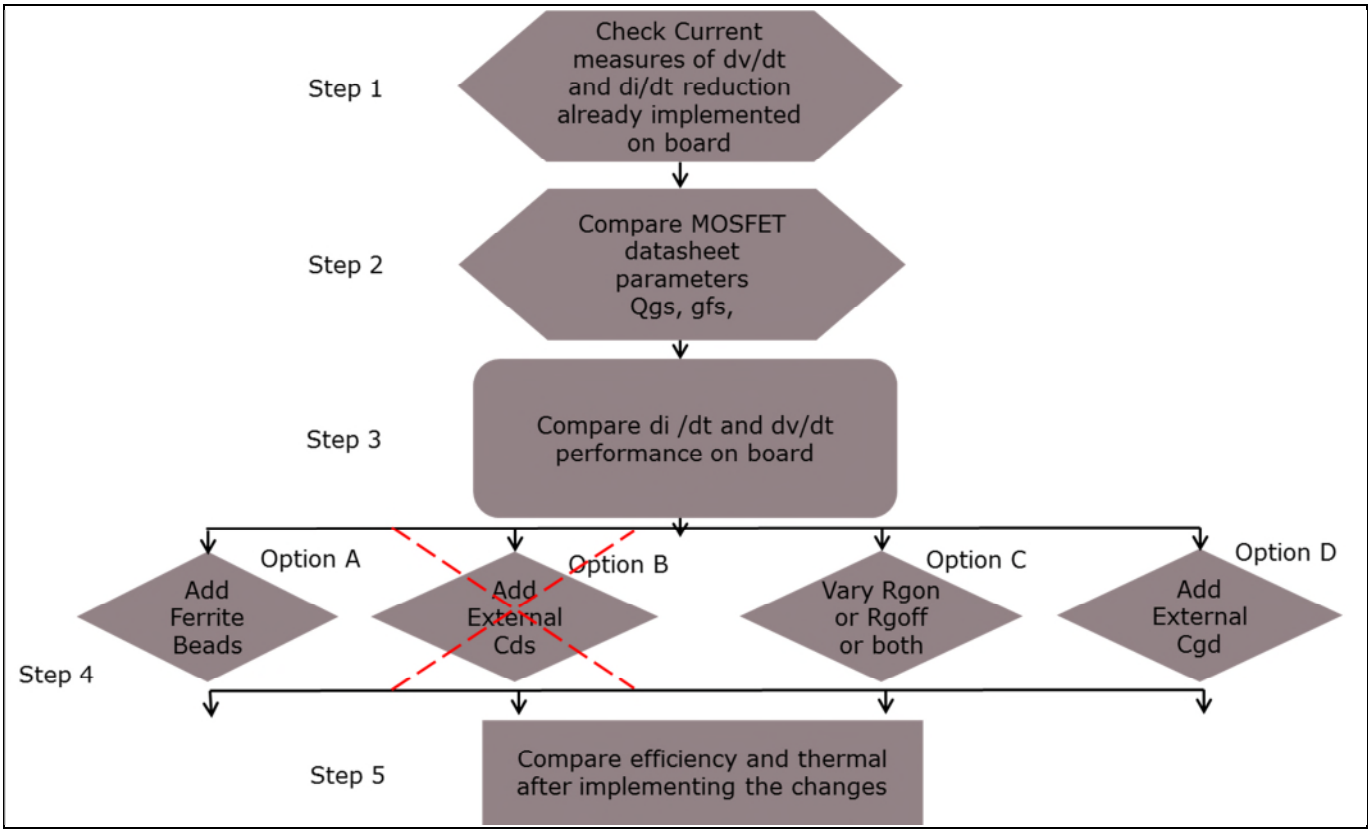


Figure 22 Flowchart for replacing SJ

The option of adding C_{ds} is not considered for EMI reduction. If the drain to source voltage spike becomes too large, then we will use an external C_{ds}. For meeting the EMI requirements we will rely on R_g and an external C_{gd}.

Step 1: Check current approaches on the PCB. Unlike the previous example, the 25 W charger board did not used ferrite beads to reduce di/dt.

Step 2: Compare device datasheets.

A closer look at the device datasheets showed one key difference apart from the higher $R_{ds,on}$ as shown in Figure 23.

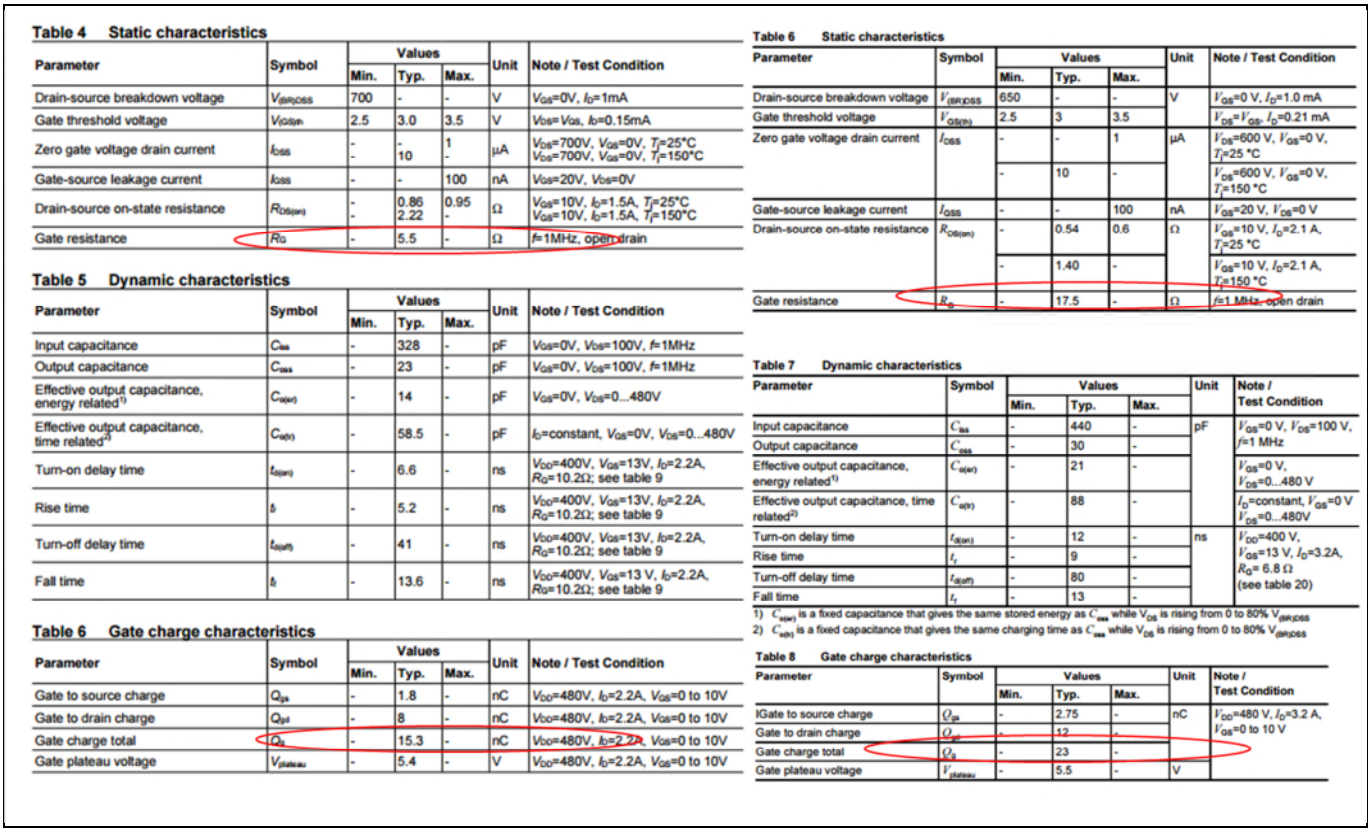


Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	700	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{GS(th)}$	2.5	3.0	3.5	V	V_{DS}= V_{GS}, I_D=0.15mA
Zero gate voltage drain current	I_{DSS}	- -	- 10	1 -	µA	V_{DS}=700V, V_{GS}=0V, T_j=25°C V_{DS}=700V, V_{GS}=0V, T_j=150°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.86 2.22	0.95 -	Ω	V_{GS}=10V, I_D=1.5A, T_j=25°C V_{GS}=10V, I_D=1.5A, T_j=150°C
Gate resistance	R_G	-	5.5	-	Ω	f=1MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	328	-	pF	V_{GS}=0V, V_{DS}=100V, f=1MHz
Output capacitance	C_{oss}	-	23	-	pF	V_{GS}=0V, V_{DS}=100V, f=1MHz
Effective output capacitance, energy related[1]	$C_{o(er)}$	-	14	-	pF	V_{GS}=0V, V_{DS}=0...480V
Effective output capacitance, time related[2]	$C_{o(tr)}$	-	58.5	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...480V
Turn-on delay time	$t_{d(on)}$	-	6.6	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=2.2A, R_G=10.2Ω; see table 9
Rise time	t_r	-	5.2	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=2.2A, R_G=10.2Ω; see table 9
Turn-off delay time	$t_{d(off)}$	-	41	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=2.2A, R_G=10.2Ω; see table 9
Fall time	t_f	-	13.6	-	ns	V_{DD}=400V, V_{GS}=13 V, I_D=2.2A, R_G=10.2Ω; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	1.8	-	nC	V_{DD}=480V, I_D=2.2A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	8	-	nC	V_{DD}=480V, I_D=2.2A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	15.3	-	nC	V_{DD}=480V, I_D=2.2A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	V_{DD}=480V, I_D=2.2A, V_{GS}=0 to 10V

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	V_{GS}=0 V, I_D=1.0 mA
Gate threshold voltage	$V_{GS(th)}$	2.5	3	3.5		V_{DS}=V_{GS}, I_D=0.21 mA
Zero gate voltage drain current	I_{DSS}	-	-	1	µA	V_{DS}=600 V, V_{GS}=0 V, T_j=25 °C
		-	10	-		V_{DS}=600 V, V_{GS}=0 V, T_j=150 °C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	0.54	0.6	Ω	V_{GS}=10 V, I_D=2.1 A, T_j=25 °C
		-	1.40	-		V_{GS}=10 V, I_D=2.1 A, T_j=150 °C
Gate resistance	R_G	-	17.5	-	Ω	f=1 MHz, open drain

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	440	-	pF	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz
Output capacitance	C_{oss}	-	30	-		
Effective output capacitance, energy related[1]	$C_{o(er)}$	-	21	-		V_{GS}=0 V, V_{DS}=0...480 V
Effective output capacitance, time related[2]	$C_{o(tr)}$	-	88	-		I_D=constant, V_{GS}=0 V V_{DS}=0...480V
Turn-on delay time	$t_{d(on)}$	-	12	-	ns	V_{DD}=400 V, V_{GS}=13 V, I_D=3.2A, R_G= 6.8 Ω (see table 20)
Rise time	t_r	-	9	-		
Turn-off delay time	$t_{d(off)}$	-	80	-		
Fall time	t_f	-	13	-		

1) $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$
2) $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

Table 8 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
IGate to source charge	Q_{gs}	-	2.75	-	nC	V_{DD}=480 V, I_D=3.2 A, V_{GS}=0 to 10 V
Gate to drain charge	Q_{gd}	-	12	-		
Gate charge total	Q_g	-	23	-		
Gate plateau voltage	$V_{plateau}$	-	5.5	-	V	

Figure 23 The integrated R_g and Q_g of the IPI70R950CE are much lower compared to the IPI65R600C6. Hence, the IPI70R950CE will switch much faster

Step 3: Adding external C_{ds}, C_{gd} and increasing R_g will significantly reduce the efficiency due to the higher $R_{ds,on}$ device under consideration. These options are viable choices between similar $R_{ds,on}$ MOSFETs. Hence it was decided to optimize the EMI by adding a bead (Lbead) and modifying the primary snubber capacitor (Csnub) value to keep the efficiency impact low.

Step 4 and Step 5: Verification.

Figure 24 shows the plug and play results for IPI70R950CE vs. IPI65R600C6.

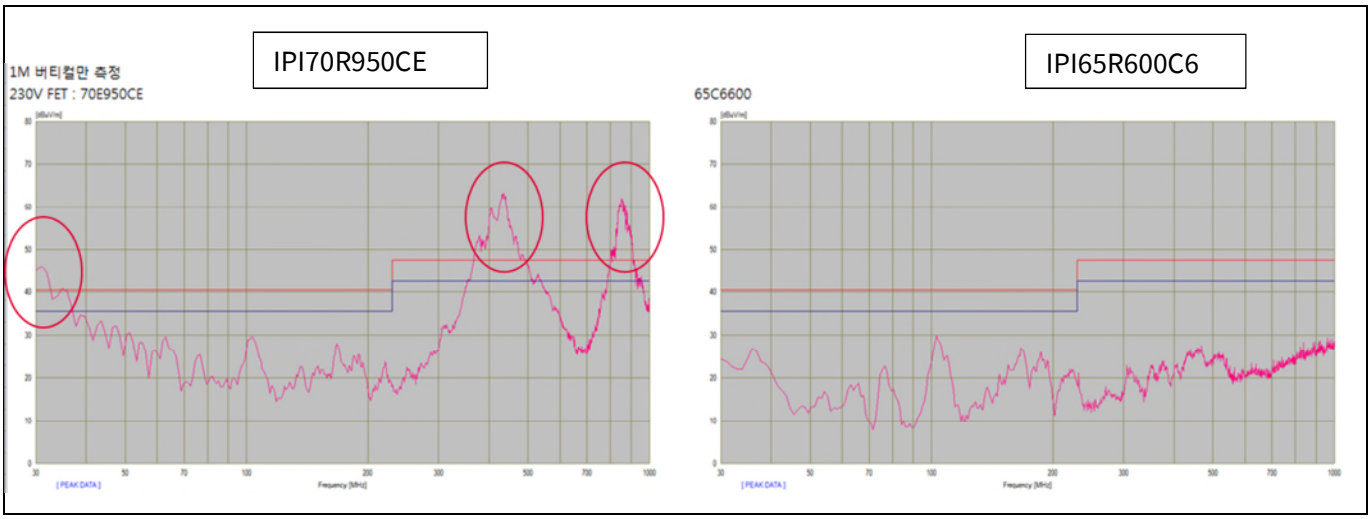


Figure 24 **IPI70R950CE clearly violated the radiated EMI limits by a large margin when compared to the IPI65R600C6 that meets the EMI requirement with sufficient margin.**

As seen in Figure 25, with the addition of a 2.2 uH bead and increasing the snubber capacitance to 45 pF, the EMI goals were successfully met with CoolMOS™ CE.

The snubber capacitance of 82 pF provided a larger safety margin, but the efficiency drop due to this higher capacitance was not acceptable. Hence the trade-off between efficiency and safety margin requires using 47 pF as the snubber capacitance.

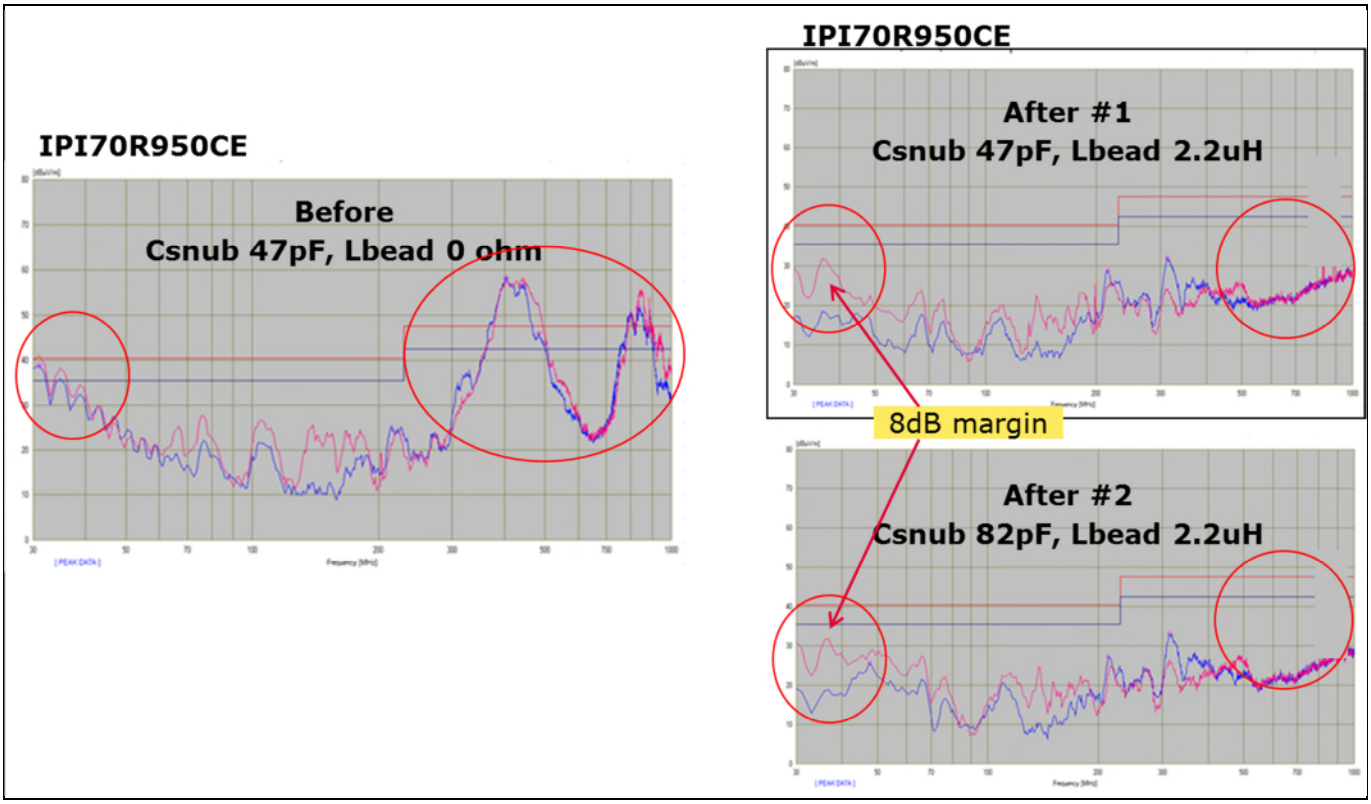


Figure 25 **IPI70R950CE CoolMOS™ CE successfully meeting EMI requirements by adding a bead (L_{bead} as shown in Figure 21) in the drain of the MOSFET and increasing the snubber capacitance (C_{snub} as shown in Figure 21)**

4.3 Optimizing an AC-DC SMPS originally optimized for CoolMOS™ CE – the SMPS design was started with CoolMOS™ CE

Ideally, it is always preferred to start an optimized AC-DC design with CoolMOS™ CE. When the device parameters are considered during the design stage itself and the appropriate EMI filters, PCB layout, transformer design are made, the efficiency benefits of SJ based CoolMOS™ CE are obvious.

The flow chart for designing with CoolMOS™ CE is as shown below:

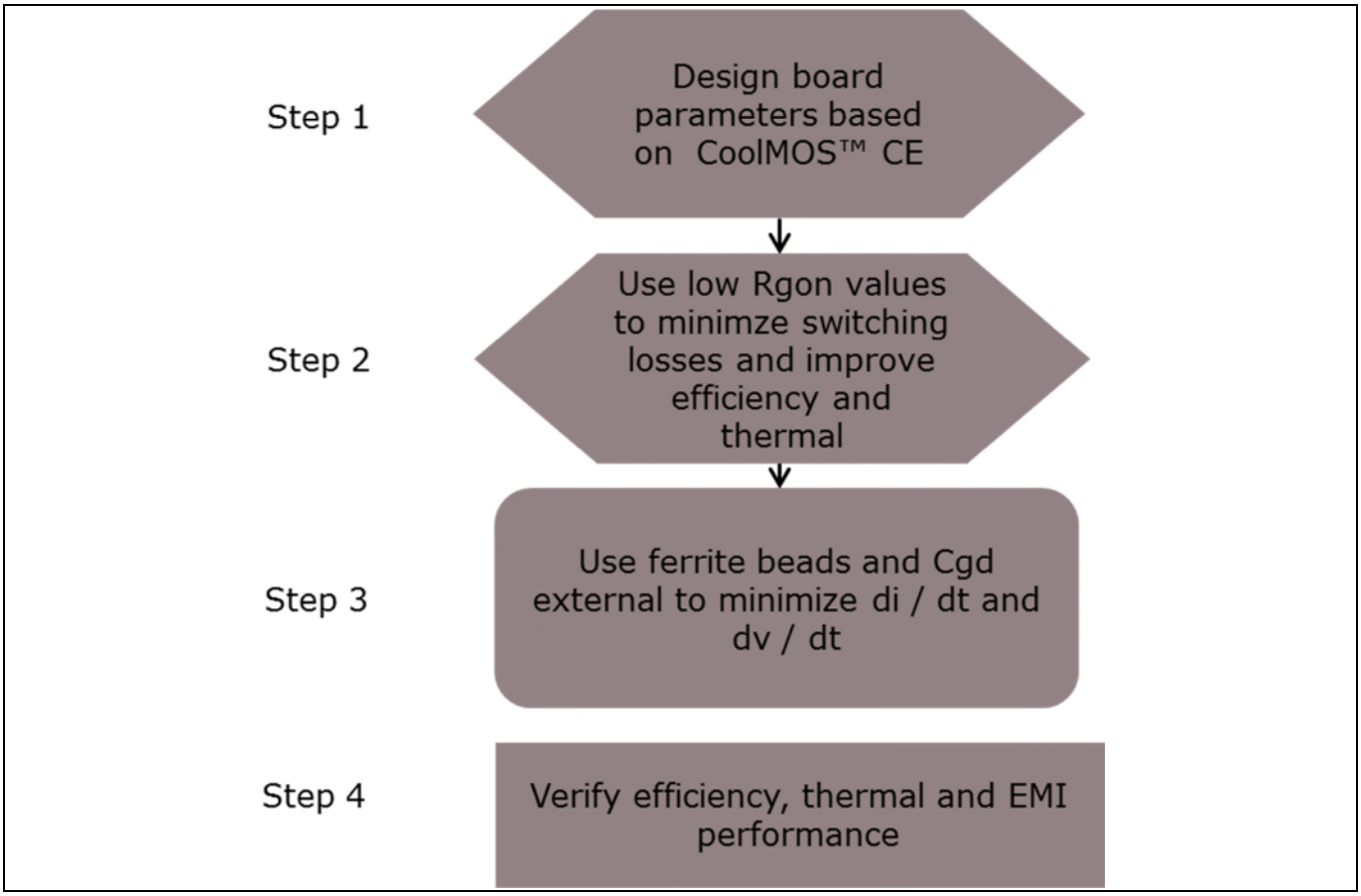


Figure 26 Designing with CoolMOS™ CE

A 110 W LED driver demo board is available to test the IPD60R460CE. The design guidelines are available at http://www.infineon.com/dgdl/Infineon-ICL5101-AN-v02_02EN.pdf?fileId=5546d462503812bb015046008b145ff7

The conducted and radiated EMI measurement results are shown in figure 27.

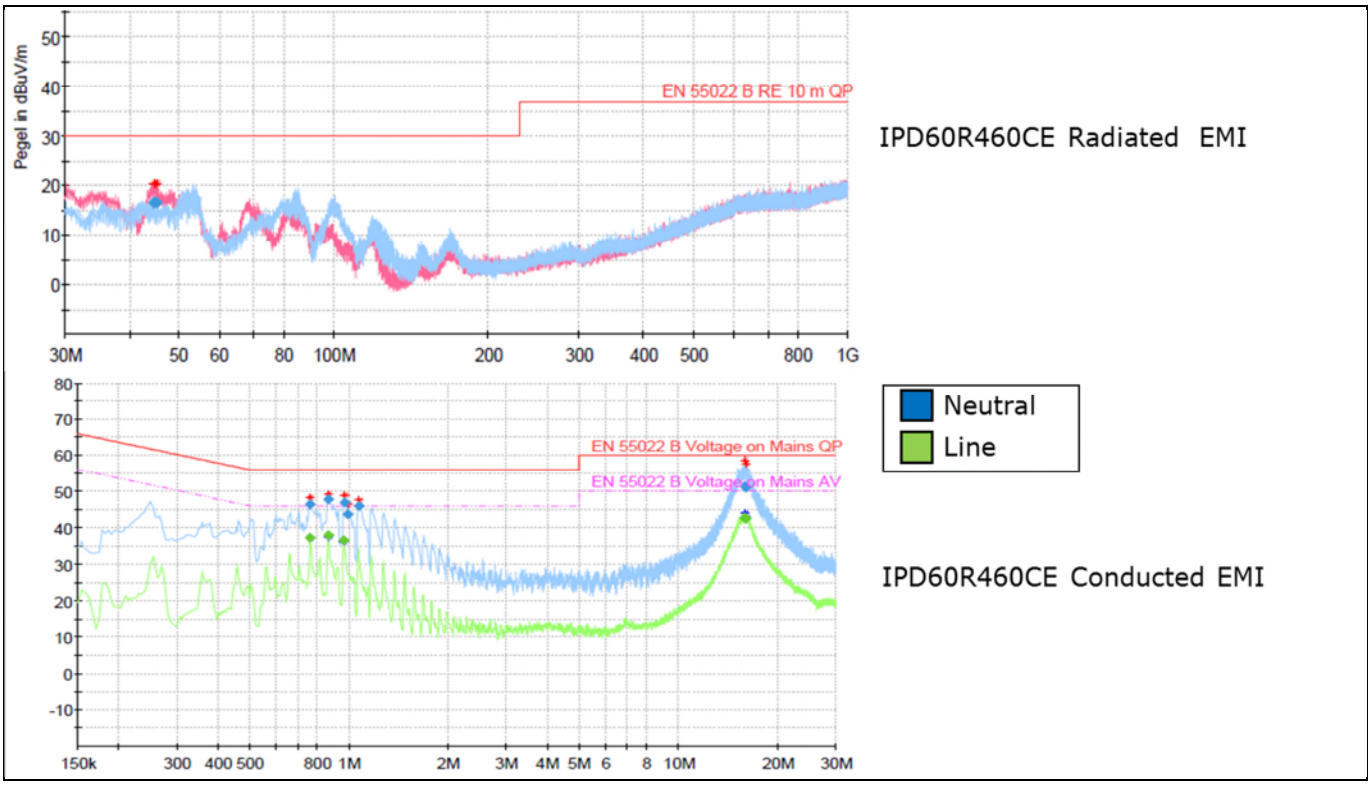


Figure 27 CoolMOS™ CE successfully meets QP conducted and radiated EMI requirements with sufficient margin and high efficiency (>90%) when the 110 W demo board is optimized for CoolMOS™ CE from the beginning of the design

5 Summary for reducing EMI when using CoolMOS™ CE

The overall summary for reducing the di/dt and dv/dt of a fast switching CoolMOS™ CE when replacing a standard MOSFET is as shown in Figure 28.

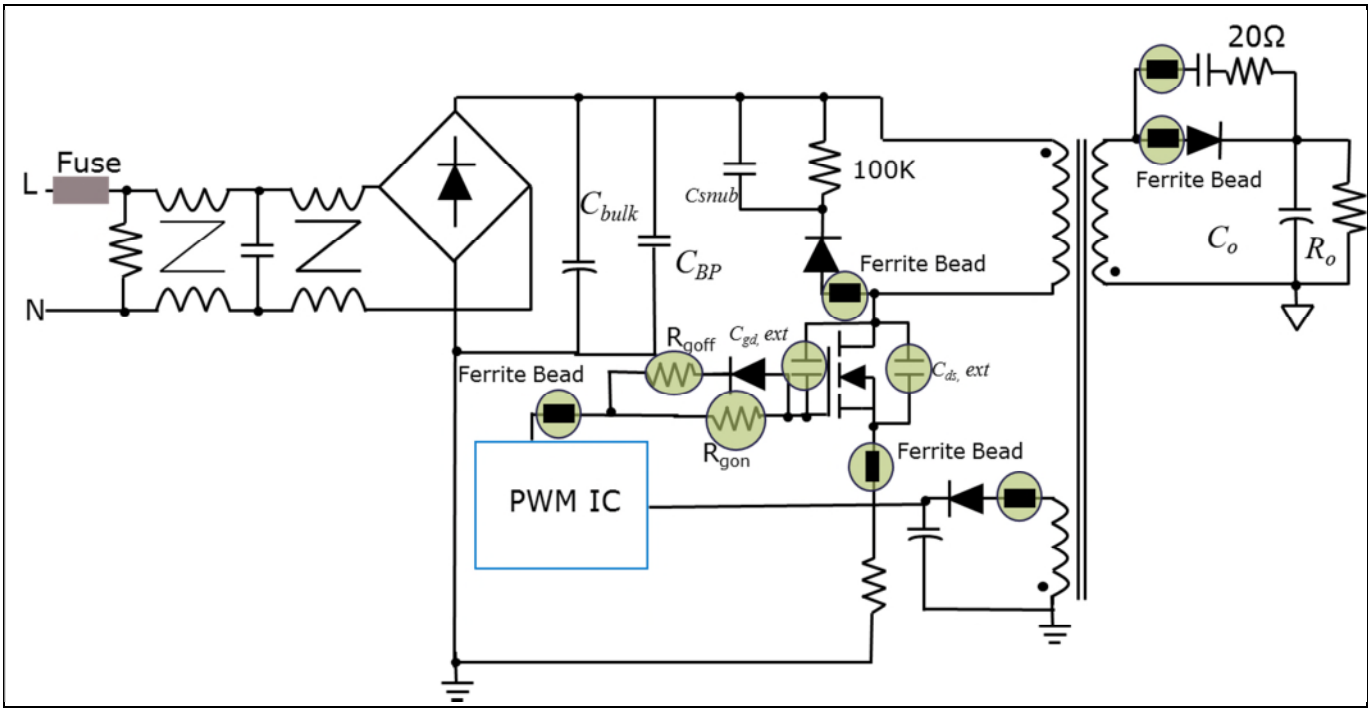


Figure 28 Summary of di/dt and dv/dt reduction techniques with CoolMOS™ CE

The preferred order of choice and its impact on efficiency and temperature rise is shown in the table below:

Options	Parameters	Typical values	Overall efficiency	Topology preference	MOSFET thermal	Cost
Option A	Adding Ferrite Beads	1.2 uH to 4.7 uH	Remains same	Fixed frequency and QR flyback	Remains same	+0.01 USD each
Option B	Adding External C_{ds}	Max. 100 pF	Reduces by ~0.1%	Fixed frequency and QR flyback	Increases by ~2°C	+0.005 USD
Option C	Adding External C_{gd}	Max. 22 pF	Reduces by ~0.2%	Fixed frequency and QR flyback	Increases by ~5°C	+0.005 USD
Option D	Increase $R_{g,on}$	10 Ω max* 250 Ω max**	Reduces by ~0.5%	QR flyback	Increases by ~10°C	0

This application note was mainly focused on MOSFET-related parameter modifications. However, a system approach can also be implemented to reduce EMI. This may not be directly related to MOSFET modifications but will help reduce EMI. A few systems-related modifications are discussed in the next section.

6 System related EMI optimization

6.1 Option A: layout practices for reducing di/dt and dv/dt in flyback power supplies

Optimal PCB layout also plays a key role in meeting EMI requirements. Care should be taken to reduce all of the di/dt loops. Connections must be made via the shortest possible route. Switching loop areas as shown in figures 1, 2 and 3 should be kept to a minimum. Reduce the unintended antennas in circuit boards such as:

1. Long traces - keep the trace as short as possible.
2. Vias – use shielded vias.
3. Component leads and pins – reduce stray inductances with short leads.
4. Placement of decoupling capacitors between power and ground where voltage fluctuations are determined to exist.
5. Power planes should be backed off from the edges of the PCB.
6. Avoid traces cut within ground or power planes, which can create an unintended aperture.
7. Avoid loop antennas that encompass any route in which both forward and return currents are on a well defined conducting path.

6.2 Option B: heat sink grounding to input bulk capacitor return rather than chassis ground

Ground the heat sink to PCB ground / input bulk capacitor return to reduce common mode noise and radiated noise.

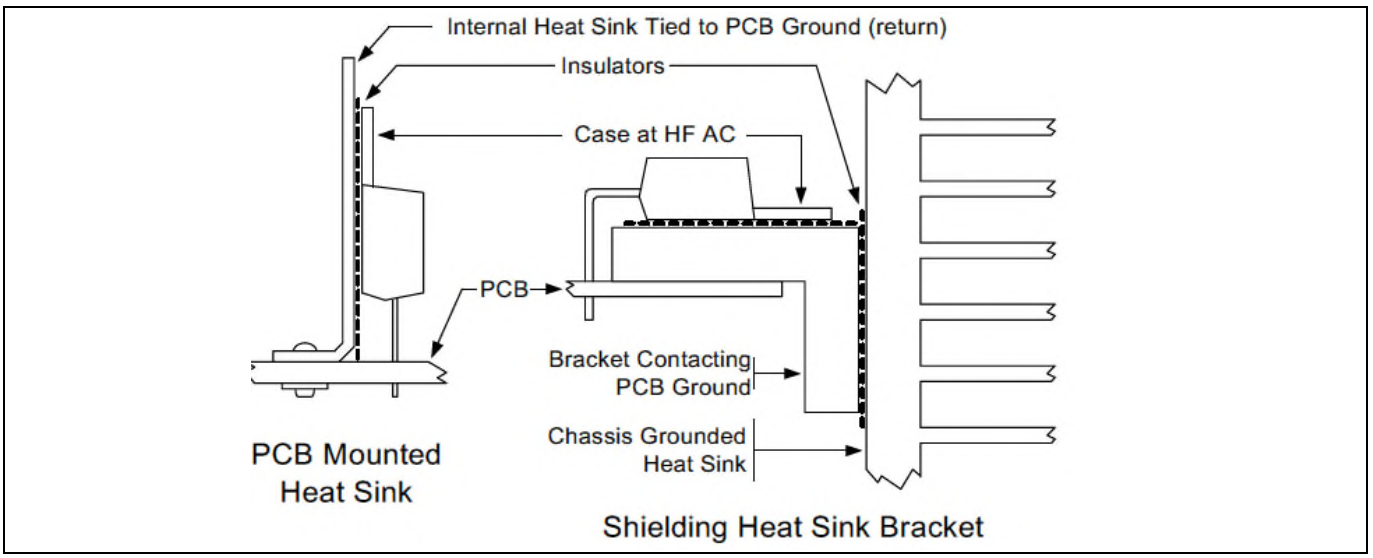


Figure 29 Two heat sink arrangements that divert capacitively coupled noise to circuit common rather than chassis ground

6.3 Option C: Y capacitors

Apart from having the parasitic winding capacitance in a flyback transformer as shown in Figure 3, practical transformers also have some stray capacitance between the primary and secondary windings. This capacitance interacts with the switching operation of the converter. As there is no other connection between input and output this will result in a high frequency voltage between the input and output. The cables from the power supply are now acting as an antenna, transmitting the high frequency generated by the switching process.

To suppress the high frequency common mode, it is necessary to put capacitors between the input and output side of the power supply with a capacitance substantially higher than the capacitance in the flyback transformer. This effectively shorts out the high frequency and prevents it escaping from the power supply.

When designing a class 2 (unearthed) power supply such as a charger, there is no alternative but to connect these capacitors to the input "live" and/or "neutral". However, short circuit failure of these capacitors would be a serious issue. In a class 1 power supply such as the adapter, failure of the capacitor between the mains supply and mains earth would mean a short to earth, (equivalent to a failure of "basic" insulation). In a class 2 PSU a failure of the capacitor is much worse, it would mean a direct and serious safety hazard to the user (equivalent to a failure of "double" or "reinforced" insulation). To prevent hazards to the user, the capacitors must be designed so that short circuit failure is very unlikely.

Hence, special capacitors are needed for the purpose of isolating noise voltage due to transformer parasitic capacitances. These capacitors are known as "Y capacitors" (X capacitors on the other hand are used between mains live and mains neutral). There are two main subtypes of "Y capacitor", "Y1" and "Y2" (with Y1 being the higher rated type). In general Y1 capacitors are used in chargers and Y2 capacitors are used in adapters.

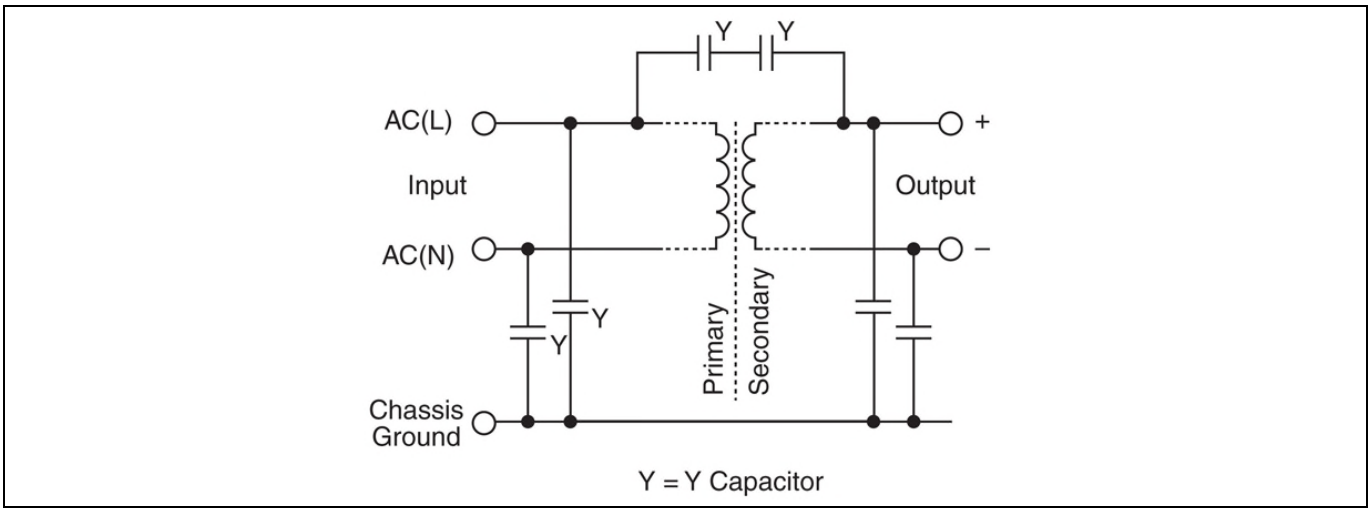


Figure 30 Using Y capacitors to limit noise due to transformer parasitic capacitance

6.4 Option D: transformer shielding

Transformers are designed with a Faraday shield or copper foil between the primary and secondary windings. These shields are connected to the primary and secondary grounds to ensure noise voltages are safely returned to the respective grounds. More information can be obtained from application notes 3 and 4 in the reference section.

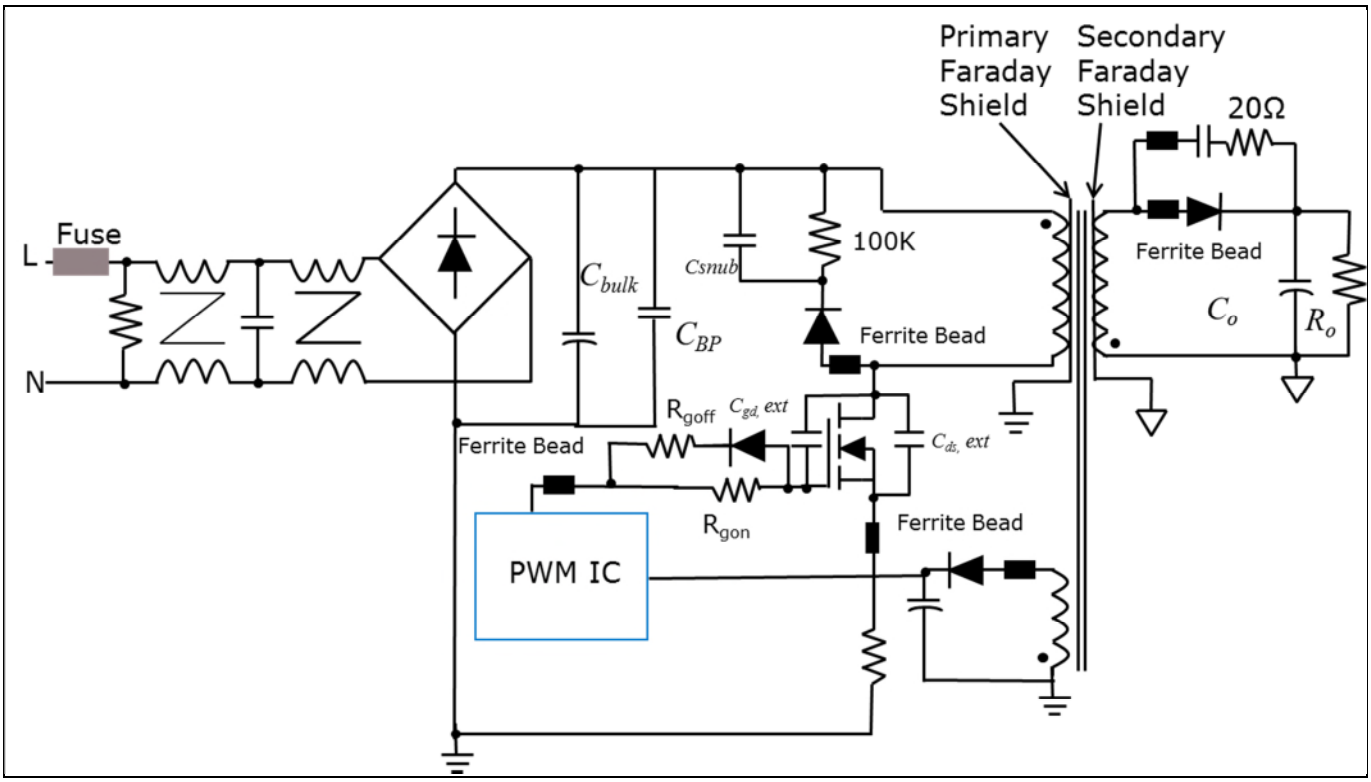


Figure 31 **Transformer shielding to minimize noise coupling due to parasitic capacitances between primary and secondary**

6.5 Option E: variable frequency PWM controller with frequency modulation

Apart from the techniques discussed above in this application note, for flyback converters that are controlled by a square wave with a constant frequency and duty cycle (D), the conventional technique to reduce EMI consists of using passive filters. This has limitations: size, weight, design complexity, efficiency, cost, etc. Modern variable-frequency (VF) EMI reduction techniques are available to overcome the problems faced in filter-solutions. The interleaving technique is used to equally share the total power to be delivered, the general idea in VF spread spectrum signaling is shown in Figure 33. Although the spectrum distribution is different between Figures 33(a) and (b), the total energy is the same in both cases, although the peak level has reduced in Figure 33(b). Switching frequency modulation (SFM) is an effective method to reduce EMI in SMPS. This technique is based on the original spread-spectrum clock generation (SSCG) techniques. Using SFM, there is a tradeoff between the amplitude reduction of the EMI harmonics and the generation of a set of additional sideband harmonics with a smaller amplitude.

The PWM spread spectrum control principle of an SMPS is described below:

f = fs + Δf, where fs is the reference frequency of the PWM switch; Δf is the additional spread spectrum signal frequency, which is changing frequency according the time-domain characteristics of the spread spectrum signal.

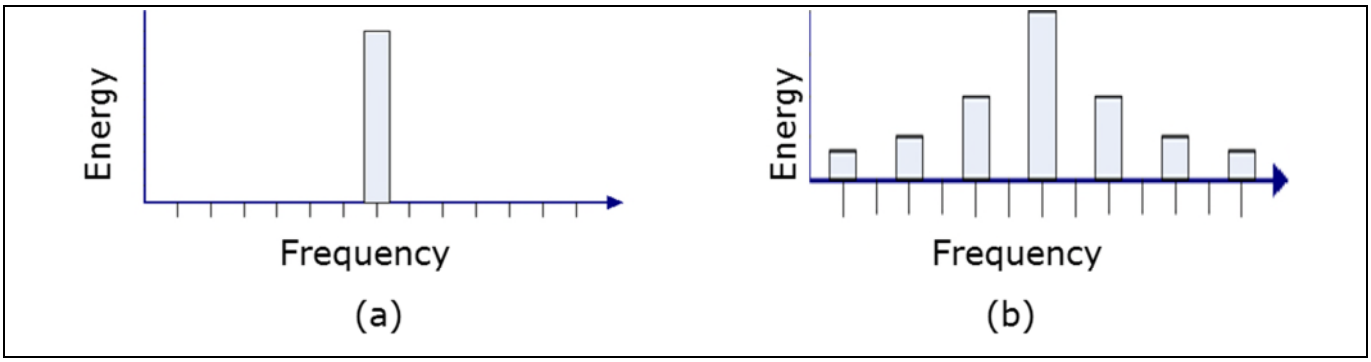


Figure 32 Spread spectrum frequency generation using variable frequency PWM controllers

The advantage of this non-linear control design approach is the simplicity of the circuit: even basic SMPS control circuits from many IC manufacturers can be used with only a few additional passive components. The main drawback of this approach is that the designer must carefully study the circuit performance at all load conditions and parameter variations to ensure the spread spectrum operation and overall system stability in all cases.

Infineon has many PWM controllers such as the ICE3XSO3 which employ such frequency modulation techniques to reduce EMI at the controller level.

7 Conclusion

When replacing standard or SJ MOSFETs with the new CoolMOS™ CE MOSFET, either for improving efficiency or for cost optimization, care should be taken with respect to the switching parameters of the CoolMOS™ CE MOSFET. The difference in switching characteristics is highlighted in the EMI testing and often the techniques discussed in this application note are required to safely meet the EMI requirements. The big gain in efficiency and thermal performance when using a CoolMOS™ CE device are often reduced by the need for bigger safety margins in EMI due to the modifications of surrounding components used to drive the CoolMOS™ CE as discussed in this application note. It is for the power supply designer to find the optimal tradeoff and effectively reap the benefits of CoolMOS™ CE.

Apart from reducing the di/dt and dv/dt of the CoolMOS™ CE, the designer can also look at a system solution approach of optimizing the PCB layout, using Y capacitors with correct grounding, shielding the switching transformer with correct grounding, grounding the heat sink and using a PWM controller with variable frequency including frequency modulation options.

Meeting the EMI requirements with a system solution approach tends to increase the charger and adapter efficiency when CoolMOS™ CE is used.

Thanks to Gary Chang (Infineon Taiwan) and Tommy Lee (Infineon Korea) for their valuable contribution to the measurement section of this application note and for EMI verification on typical application boards using CoolMOS™ CE.

8 References

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3. Transformer construction techniques
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4. Meeting EMI-EFT requirements on a system level
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Revision History

Major changes since the last revision

Page or Reference	Description of change

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