950 V CoolMOS™ P7

Infineon's first 950 V CoolMOS™ MOSFET developed for low-power applications

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About this document

Scope and purpose

Infineon is introducing its first 950 V HV MOSFET (Metal Oxide Semiconductor Field Effect Transistor) solution, developed and produced on 300 mm production for low-power applications. The 950 V CoolMOS™ P7 offers a competitively priced solution for industrial and consumer applications like chargers and adapters, industrial SMPS, and lighting in the power range from 10 W to 150 W. These power converters are typically based on flyback topologies. The 950 V CoolMOS™ P7 is no longer a multipurpose MOSFET from Infineon Technologies; it is a tailored technology for flyback and PFC applications. It is not recommended to be used in any half-bridge or full-bridge configuration in which a hard commutation on a conducting body diode can occur.

The portfolio includes frequently used packages which offer a direct replacement of existing MOSFETs, enabling improved performance in comparison to any other technology targeting this low-power market. The 950 V CoolMOS™ P7 is able to fit into several low-power packages, such as SOT-223, with the lowest $R_{DS(on)}$ available on the market.

This application note provides an explanation of the new CoolMOS™ technology. The goal of this application note is to describe technical and technological benefits of the 950 V CoolMOS™ P7. Additionally, it shows a comparison between old technologies and the main competitor products. Furthermore, it will present evaluations of internal and external customer designs to demonstrate the performance that can be achieved with the 950 V CoolMOS™ P7 with respect to thermal aspects, efficiency and electromagnetic interference behavior.

The 950 V CoolMOS™ P7 is the right solution for all the main challenges faced by designers of low-power applications, keeping Bill of Materials (BOM) costs low while not sacrificing technical specifications and meeting safety requirements.

Intended audience

Switched mode power supply design engineers.

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1 Target applications

As already described, the 950 V CoolMOS™ P7 is a tailored technology for flyback topologies and Power Factor Correction (PFC). This chapter will introduce the main target market, which is applications from 10 W to 150 W. The difference between charger and adapter is the output voltage. Chargers typically operate at between 5 V and 12 V output voltage, and adapters use around 19 V. All these applications typically use flyback topologies. There are three main flyback structures that have the highest market share. First the Continuous Current Mode (CCM) flyback, second fixed-frequency DCM flyback, and finally QR flyback, which will be introduced in the next section. In addition the snubberless flyback will also be described.

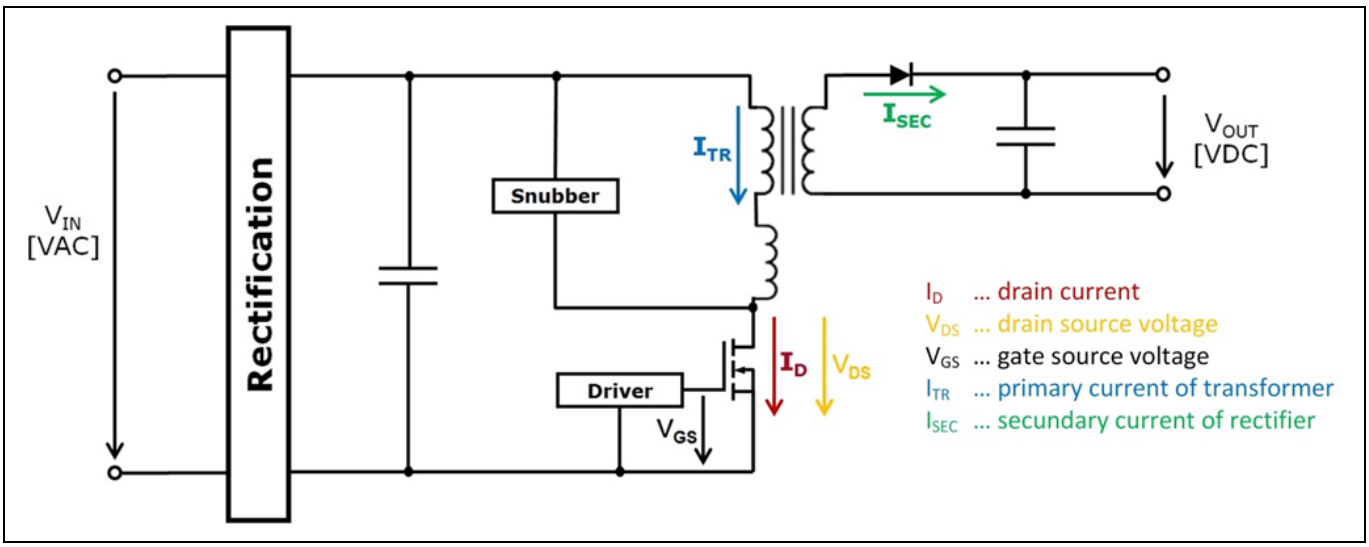


Figure 1 Flyback – simplified schematic

1.1 CCM flyback (fixed frequency)

A CCM flyback is a fixed-frequency flyback and is typically used for adapters in the higher power range, above 45 W. In this flyback the current through the main transformer (I_{TR}) never reaches 0 A in steady-state operation, as shown in Figure 2. This leads to a fully hard-switching topology, where the E_{oss} (energy stored in output capacitance at a certain voltage) behavior of the 950 V CoolMOS™ P7 can show its best performance. Fixed-frequency controllers are typically three to four times cheaper than Quasi Resonant (QR) controllers. In order to regulate the output voltage the duty cycle will change depending on the output load. It needs to be considered that a CCM flyback can also operate in DCM in light-load operation, depending on the value of the primary windings and the inductance of the main transformer. In Figure 2 the principle of operation and simplified waveforms are represented.

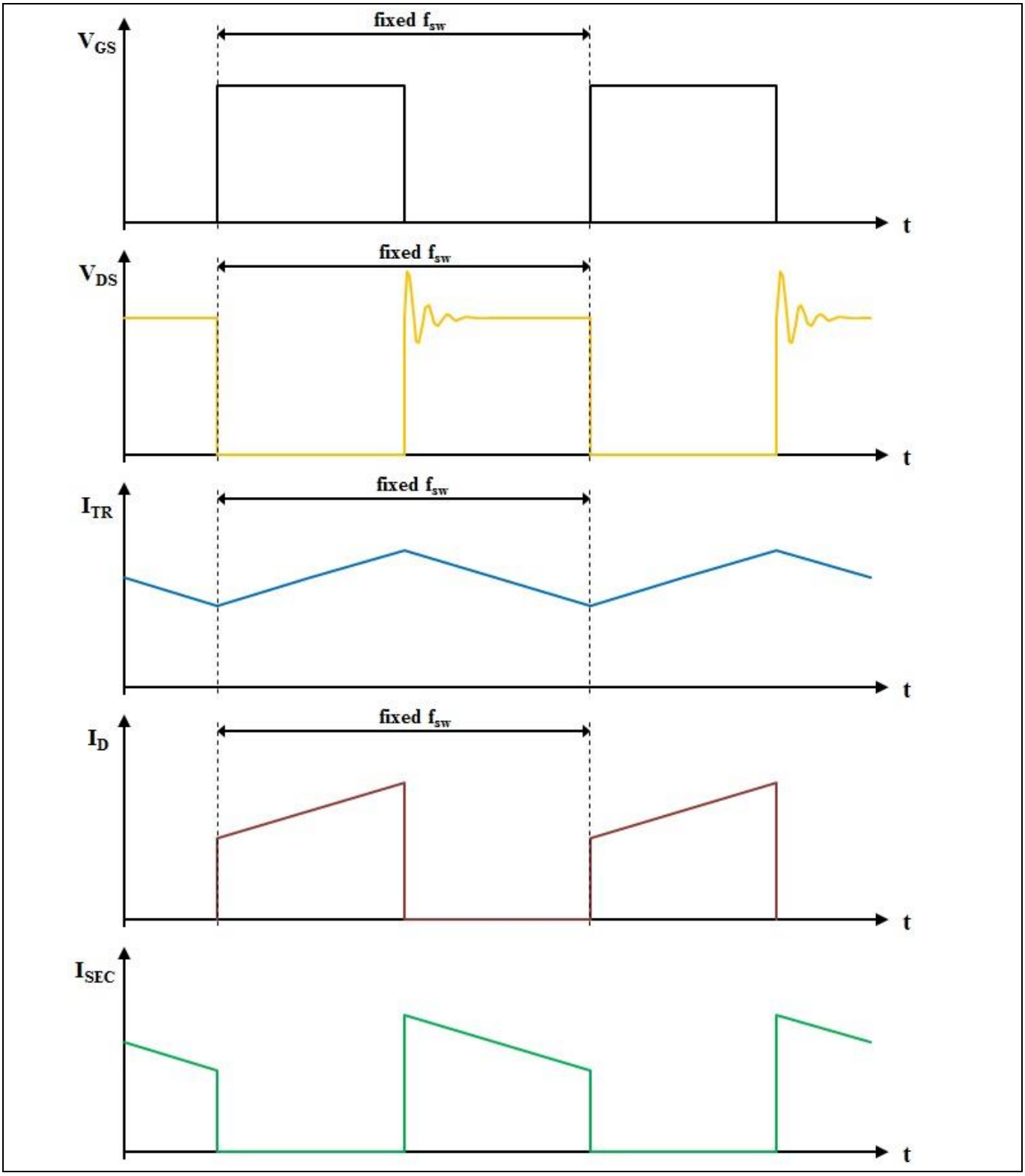


Figure 2 CCM flyback – principle of operation

1.2 DCM flyback (fixed frequency)

As already mentioned the DCM flyback is typically used at lower output loads. In a standard DCM flyback the output is also regulated by the duty cycle. This set-up is now not often used due to new efficiency standards. Also second sourcing is not always easy to achieve, as the E_{oss} losses from a MOSFET contribute significantly to

the overall efficiency and are different for all MOSFETs available on the market. Figure 3 shows the principle of operation and simplified waveforms.

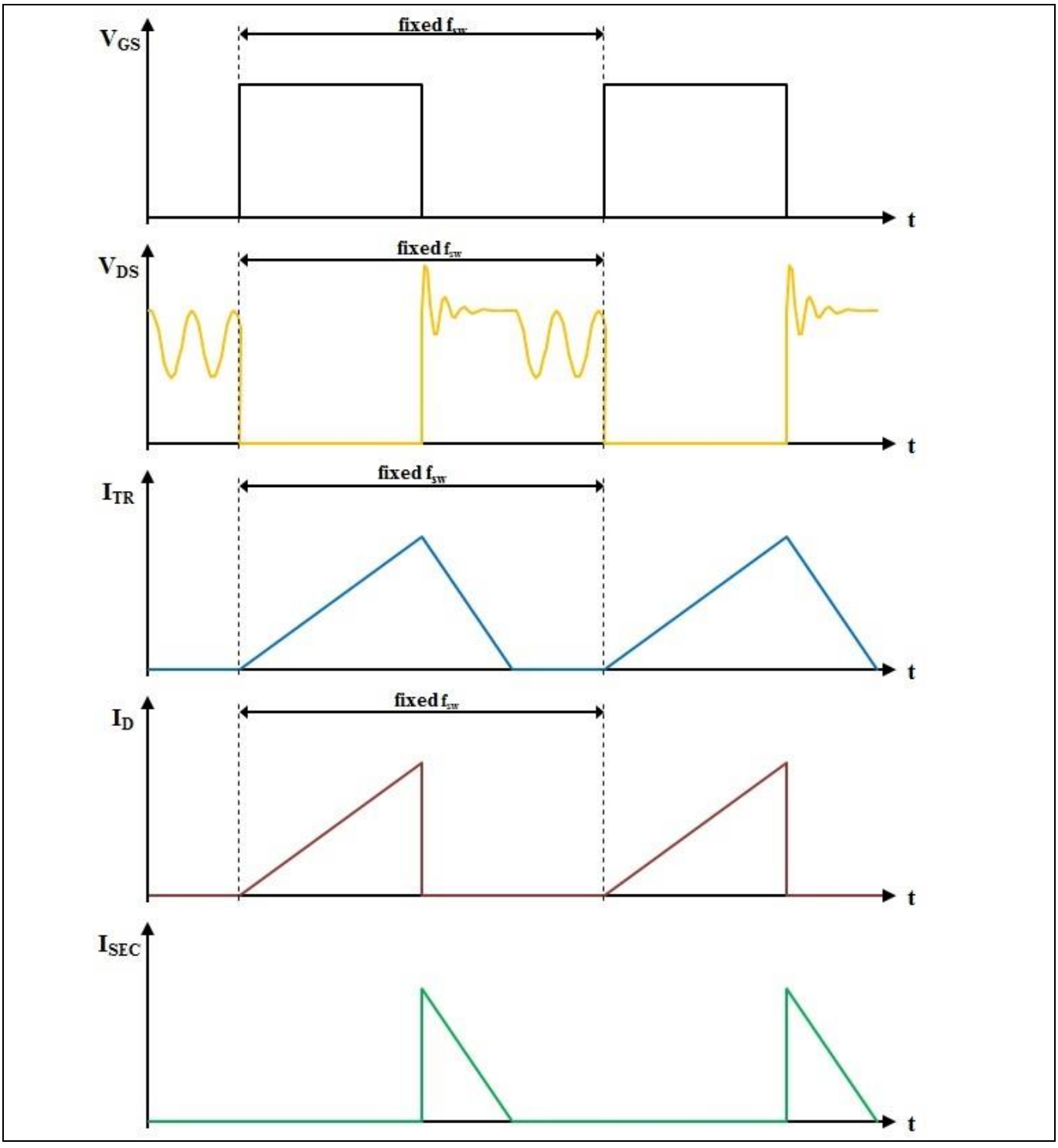


Figure 3 DCM flyback – principle of operation

1.3 QR flyback (variable frequency)

QR flyback topologies are the most used topologies for low-power charges. They offer better performance due to lower switching losses. A QR flyback can only operate in DCM, because it switches the MOSFET on during the oscillation phase of drain node capacitance and transformer main inductance when the current through the

main transformer is 0 A. The difference between a standard DCM flyback and QR operation is that the MOSFET is able to turn on at minimum drain source voltage (V_{DS}), which reduces the E_{oss} losses. This behavior is called valley switching and can be seen in Figure 4.

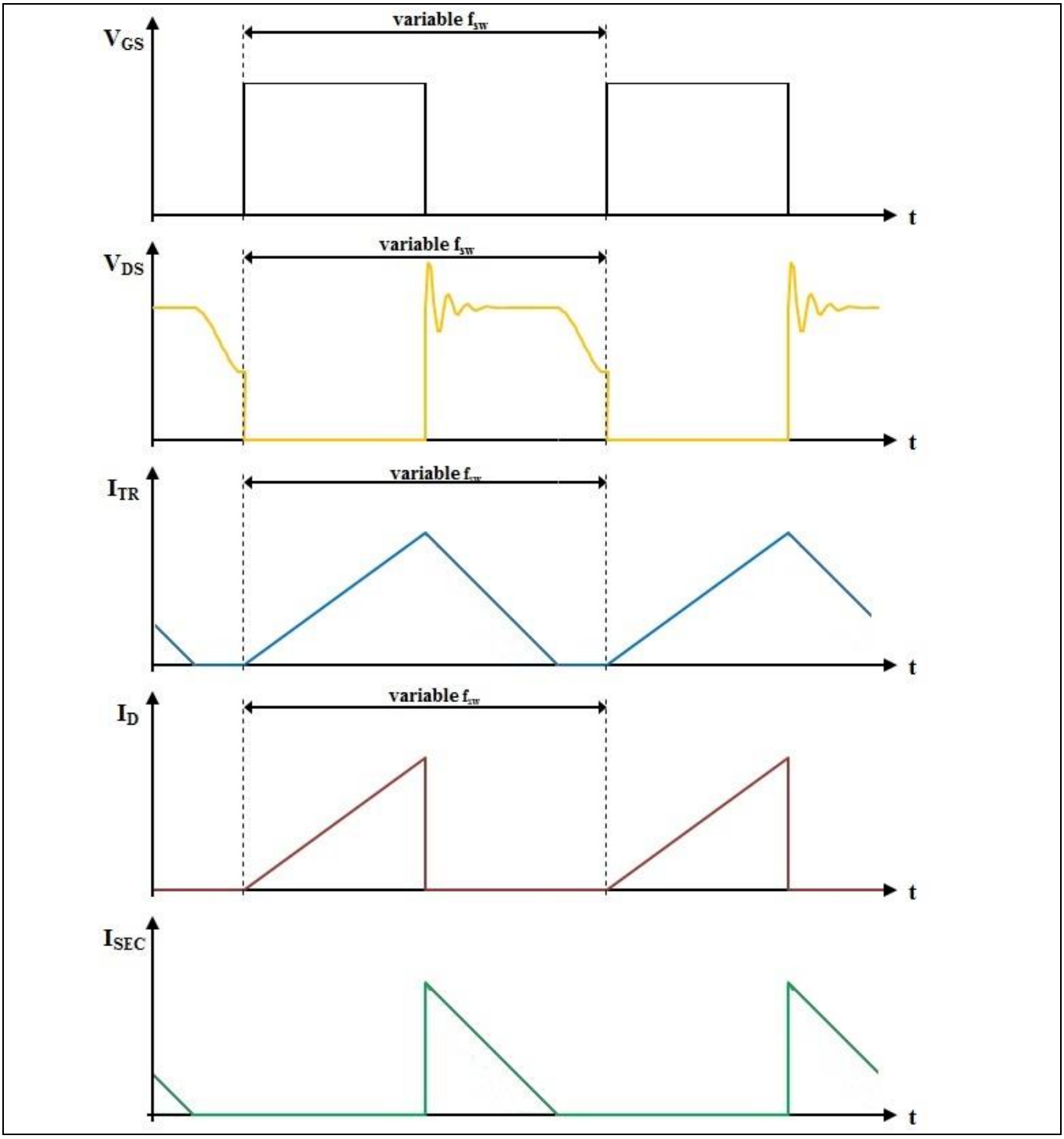


Figure 4 QR flyback – principle of operation

Typically at very light loads the MOSFET turns on later, while at heavy loads the MOSFET turns on in the first valley. As described, the V_{DS} oscillation is given by the capacitance value on the drain node and is influenced by the output capacitance of the MOSFET (C_{oss}). In this case the switching frequency can be influenced by MOSFET selection.

At the moment there are also other flyback solutions available, like zero voltage switching (ZVS) flyback or active clamp flyback, but these solutions are not part of this application note. The 950 V CoolMOS™ P7 is not meant to be used in half-bridge or full-bridge configuration where a hard commutation of a conducting body diode can occur due to the lower ruggedness of the body diode itself. More details can be found in the corresponding datasheet of the products.

1.4 Snubberless (QR) flyback

The new 950 V variant of the CoolMOS™ P7 enables a more efficient standard flyback without RCD snubber.

By removing the snubber network and switching to a snubberless design, the overall system efficiency can be improved. Switching losses and snubber losses play a large role in the losses of this supply due to the HV operation. In addition to improving the system efficiency, the snubberless flyback converter also reduces the necessary PCB area and removes the cost of the RCD network.

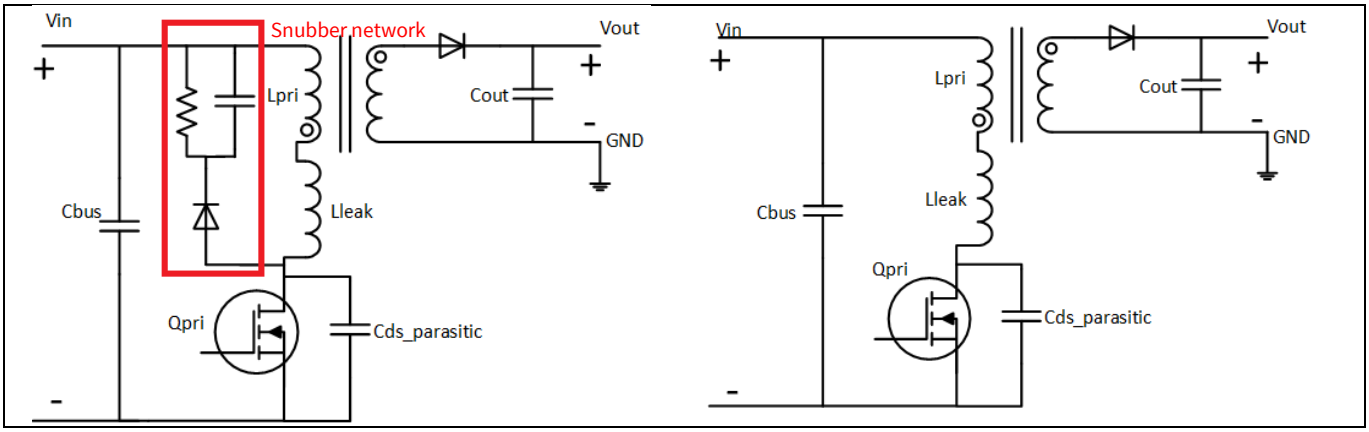


Figure 5 The typical RCD (in red) snubber vs snubberless configuration

The losses of the system are reduced in a snubberless design (Figure 5) due to removing two key loss mechanisms.

The first is that the RCD network charges up to the reflected voltage every switching cycle regardless of the system load. The leakage inductance energy also increases this voltage, leading to further losses across the snubber resistor.

The second loss mechanism comes from the additional capacitance added to the switching node from the RCD network, as well as needing to charge the capacitance across the RCD diode junction. These loss mechanisms are eliminated by removing the RCD snubber network.

To keep the MOSFET V_{DS} from getting too high, an additional drain source capacitance is added across the drain node of the MOSFET. This leads to a higher C_{DS} switching loss when compared to the design with a snubber network, as shown above in red. The energy that is stored in the transformer leakage inductance gets dissipated in the high-frequency copper loss of the transformer rather than in the RCD network.

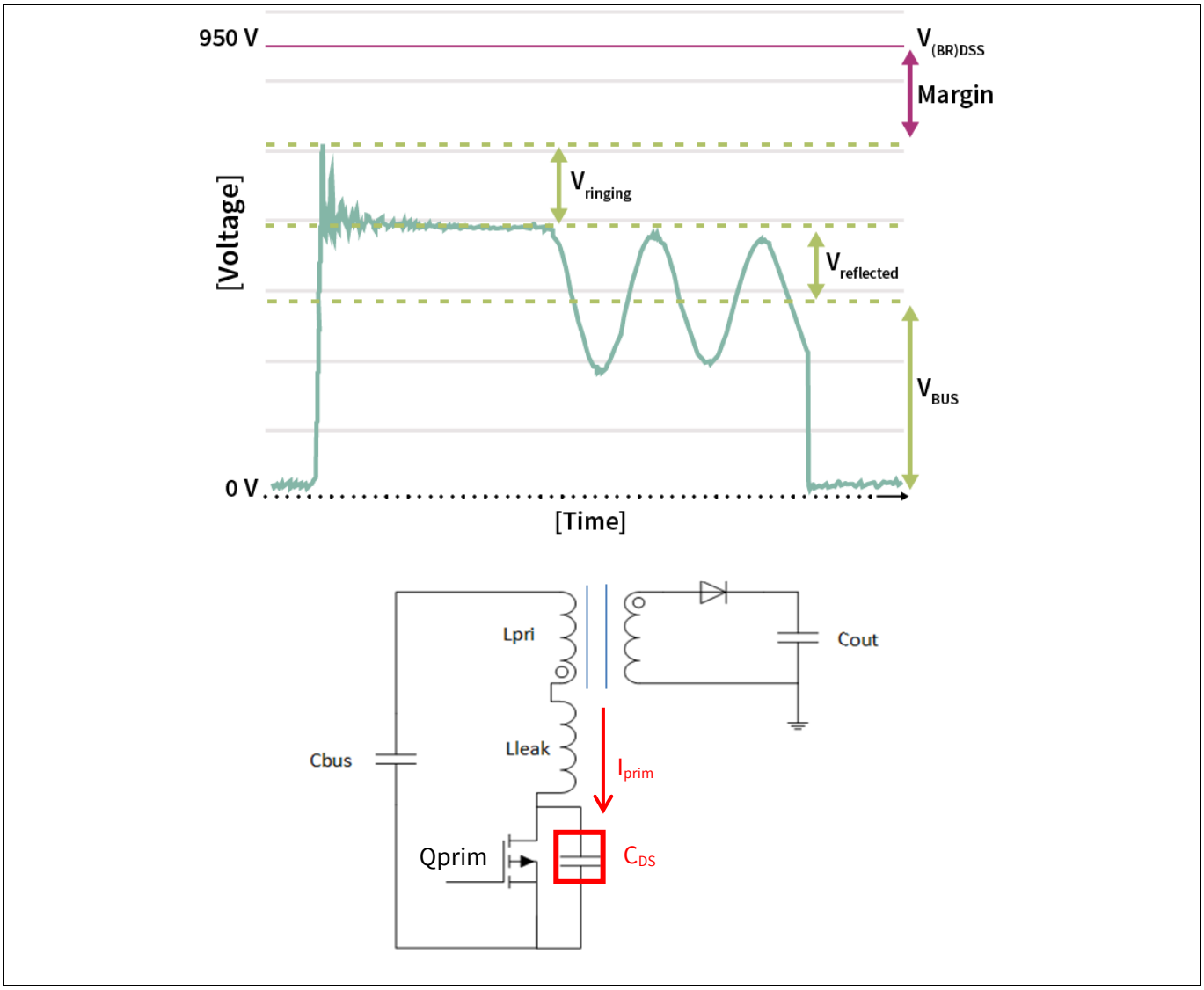


Figure 6 The MOSFET V_{DS} margin needs consideration for snubberless operation

In designing a snubberless flyback converter, it is critical to make sure the $V_{(BR)DSS}$ of the MOSFET is not exceeded. The V_{DS} of a MOSFET consists of three main sections, as shown in Figure 6. The V_{DS} is the total of the bus voltage (V_{bus}), the reflected voltage ($V_{reflected}$) and the ringing voltage ($V_{ringing}$). The ringing voltage of the MOSFET is the only portion that is affected in the transition from an RCD snubber to a snubberless design. To understand how to remove the snubber, the mechanism behind the drain source ringing needs to be understood.

When the MOSFET is turned on in a flyback converter, the current through the primary side of the transformer begins to ramp. When the MOSFET turns off this energy gets transferred to the secondary of the flyback converter. Not all this energy gets transferred to the secondary, and the leakage inductance is the energy that cannot couple to the secondary. This energy then transfers to the total output capacitance of the MOSFET, which consists of the MOSFET C_{DS}, transformer parasitic capacitance, trace capacitance and any other capacitance on the drain node. An LC ringing occurs with the period set by the C_{DS} total and the $L_{leakage}$. To control the peak voltage of the drain source ringing an external capacitance can be added in parallel to the drain source of the MOSFET. Furthermore, cold start-up sequences must be considered. As a recommendation,

a minimum of 10 percent margin should be kept from the drain source breakdown voltage with worst-case component tolerances.

2 Technology parameters

This chapter is going to describe the technological parameters that influence the behavior in the target applications. Additionally it is worth mentioning that the 950 V CoolMOS™ P7 offers an ESD protection diode which gives at least class 1C in the human body model for all $R_{DS(on)}$ classes, and offers class 2 for all products with the $R_{DS(on)}$ of 2 Ω or smaller.

2.1 Q_g – gate charge

The gate charge influences the driving losses, which could significantly influence the efficiency during light-load operation or increased switching frequency.

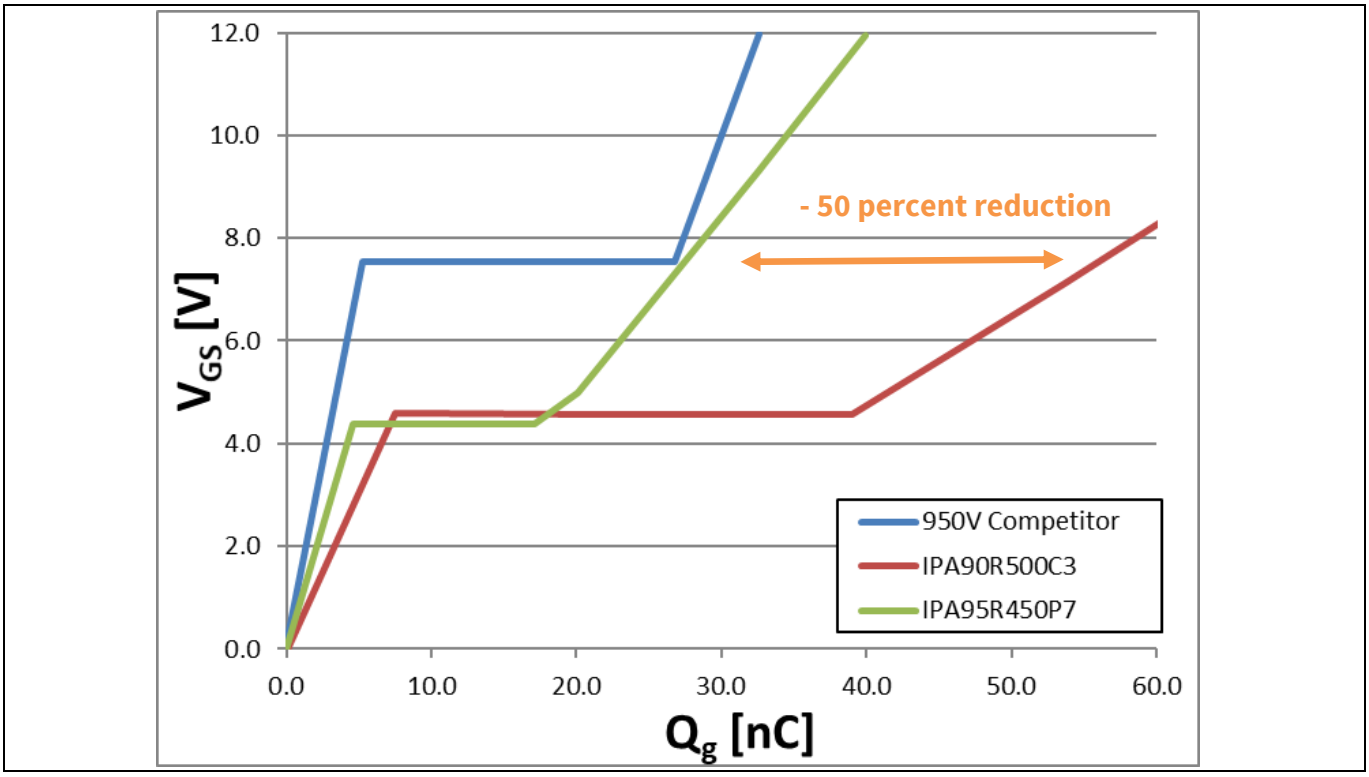


Figure 7 Gate charge of 500 mΩ equivalent devices

As can be seen in Figure 7, the 950 V CoolMOS™ P7 shows the lowest Q_g (over 50 percent reduction already at 8 V driving voltage) in comparison to all former Infineon technologies, and good performance in comparison to its main competitor.

With this behavior the 950 V CoolMOS™ P7 can enable higher switching frequencies (more than 100 kHz), which can be beneficial in reducing the magnetic components of the design, leading to smaller form factors or higher power density. It can be clearly seen that the driving losses are reduced in comparison to the former C3 technology, nearly closing the gap between Infineon's long-established and leading technology and its competitors' latest products.

2.2 $R_{DS(on)}$ – temperature dependency of on-state resistance

Also in the lower-power market the conduction losses have a huge influence on the efficiency and the thermal behavior of the overall system, especially at lower input voltages like 90 V AC or 110 V AC. In this case the 950 V CoolMOS™ P7 can offer excellent value; the MOSFET structure offers the lowest $R_{DS(on)}$ change driven by increasing junction temperature. The following diagram shows this behavior.

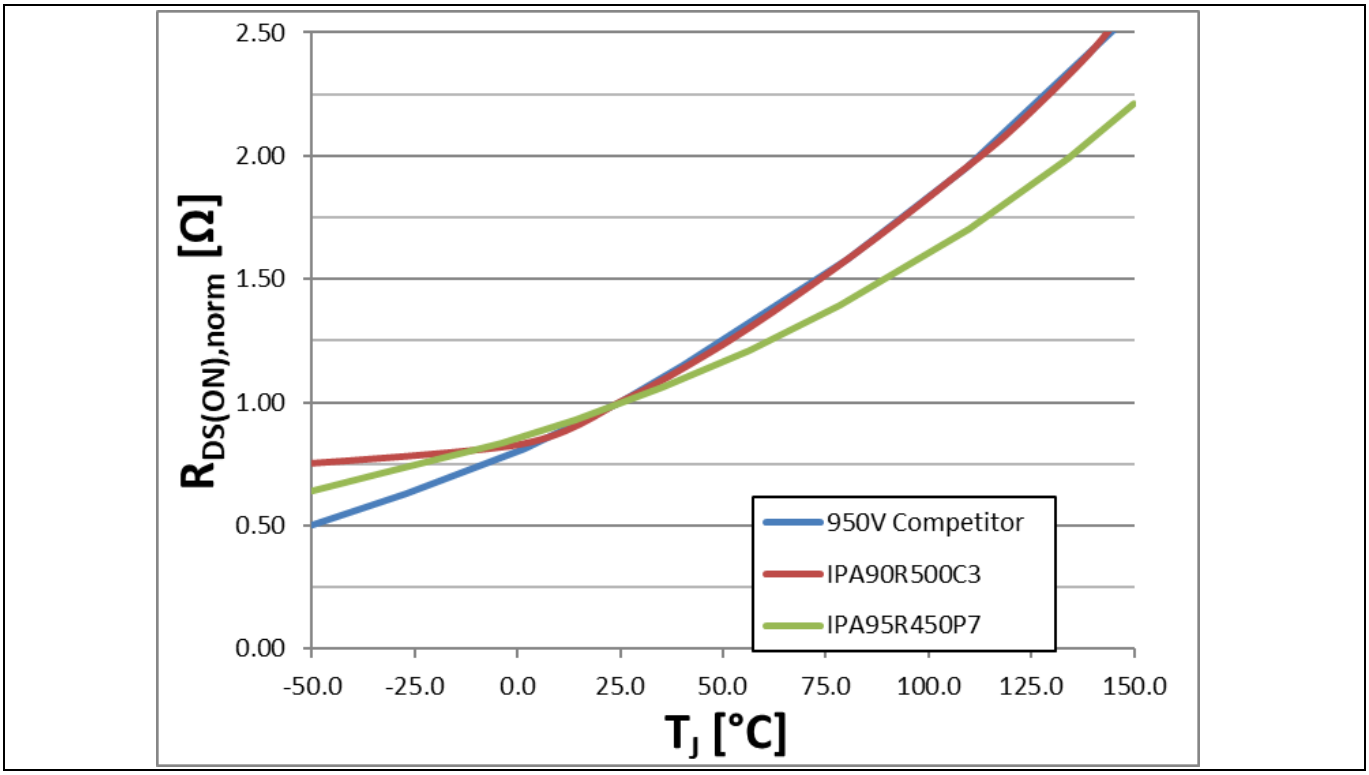


Figure 8 $R_{DS(on)}$ behavior over-junction temperature

At 100°C junction temperature the 950 V CoolMOS™ P7 shows around 15 percent lower maximum $R_{DS(on)}$ compared to Infineon's CoolMOS™ C3 family. In several adapter applications, the junction temperature limit is set by customer default to 80°C, and even there the benefit will be visible in the end application (~ 10 percent lower).

This key parameter results in the reduction of the conduction losses of the MOSFET in any available design.

2.3 E_{oss} – energy stored in output capacitance

The E_{oss} is one of the main losses during turn-on of the MOSFET. This is the energy which translates into losses during turn-on at a certain V_{DS} voltage. In QR flyback converters there are no E_{on} losses as there is no overlap between I_D and V_{DS} as the current through the main transformer is 0 A. Nevertheless additional losses are generated inside the MOSFET at every turn-on and turn-off based on the amount of energy stored in the internal capacitances.

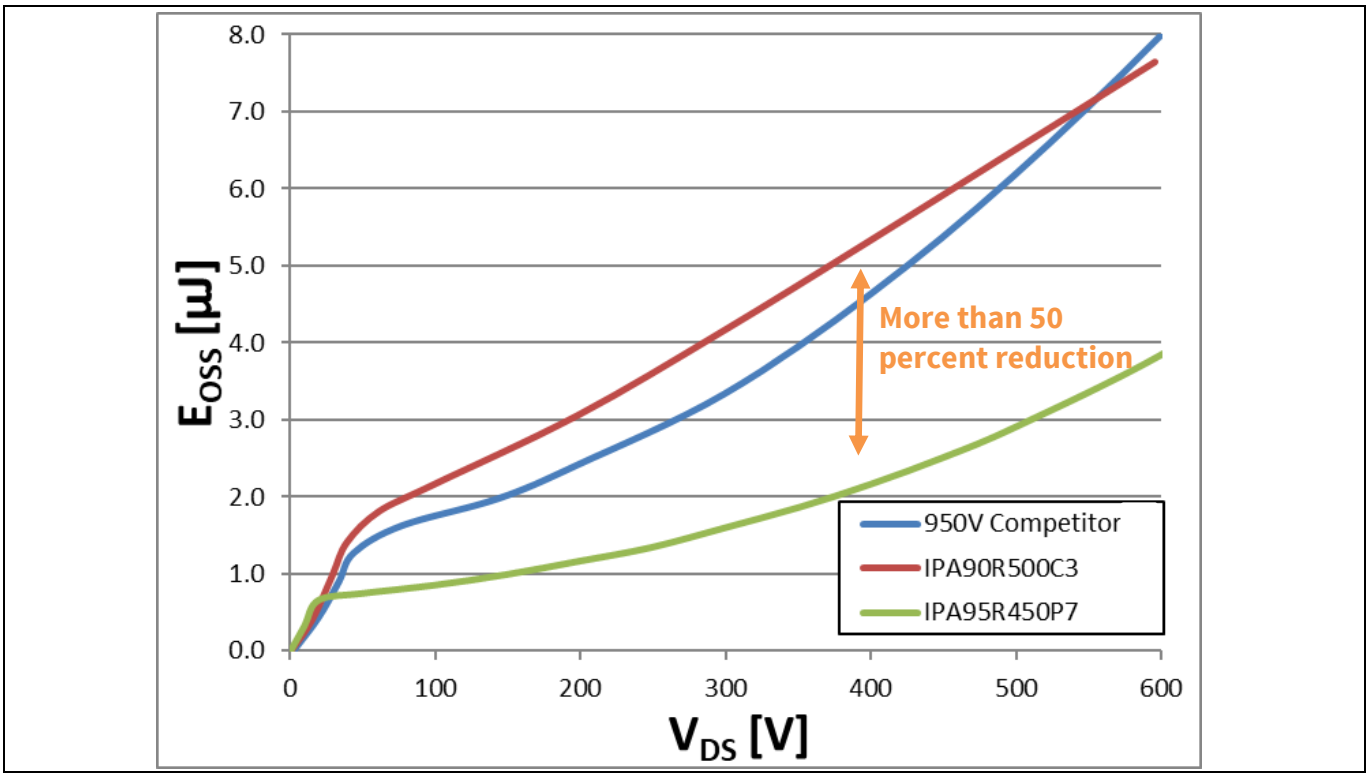


Figure 9 E_{oss} comparison of ~ 500 mΩ devices

The diagram in Figure 9 shows that the 950 V CoolMOS™ P7 offers the lowest E_{oss}, starting from 50 V V_{DS}. At 400 V the difference to former C3 technology is more than 50 percent, which is a big step from one generation to the next.

Typically it is not possible to have a real ZVS turn-on of the MOSFET, as there would be the need to significantly increase the reflected voltage from the secondary side to the primary side. This would also increase the bulk voltage and the V_{DS} peak during turn-off. Therefore turn-on V_{DS} at low-line is typically between 50 V and 100 V, and at high-line 200 V to 300 V, resulting in around 50 percent lower turn-on losses than the main competitors and more than 60 percent lower than the older C3 technology.

As these additional losses are present at every turn-on, the 950 V CoolMOS™ P7 also offers the possibility of higher switching frequencies with the same possibilities as already described in the gate charge section of this chapter.

2.4 Q_{oss} – charge stored in output capacitance

It has already been shown that the valley switching is typically above 50 V V_{DS}, and in order to also have the charge related to this value the Q_{oss} is represented.

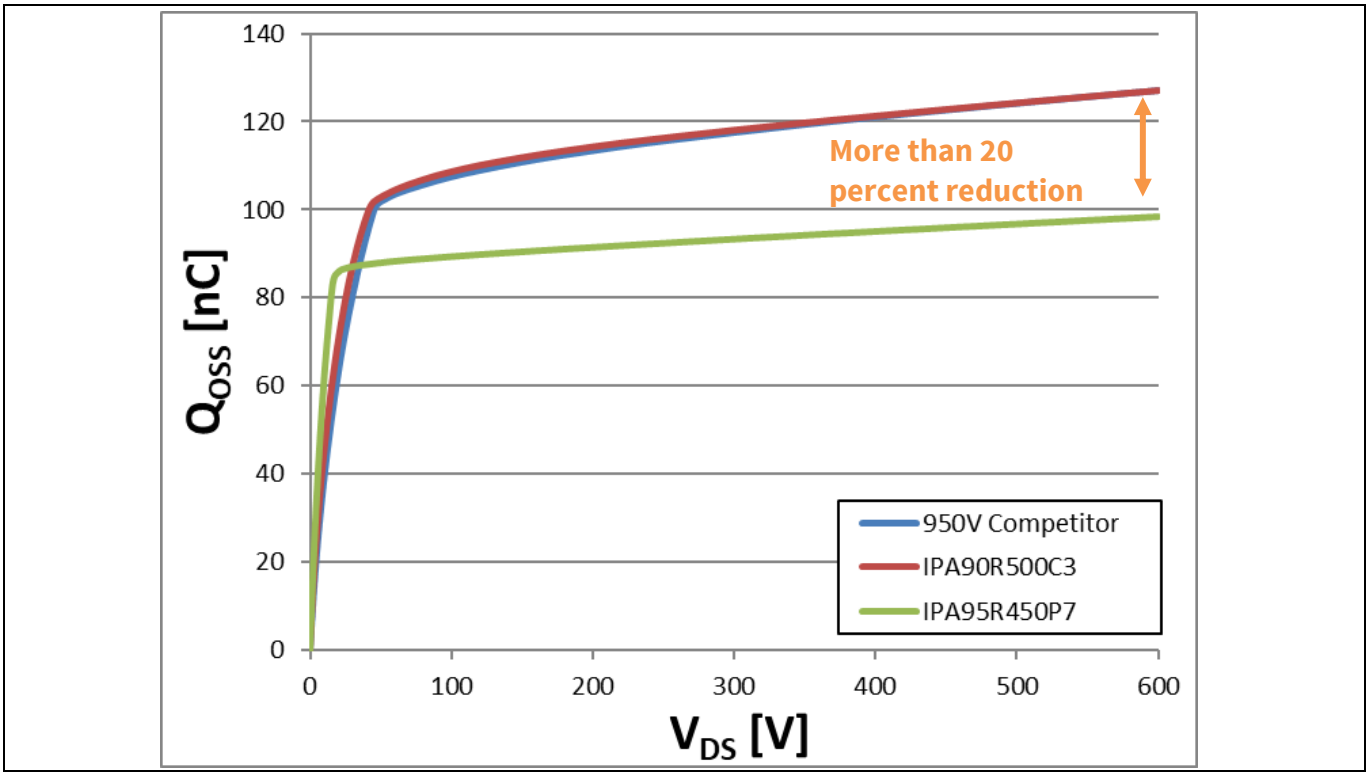


Figure 10 Q_{oss} comparison of 450 mΩ and 500 mΩ devices

The Q_{oss} between 50 V and 600 V for the 950 V CoolMOS™ P7 is reduced compared to previous technologies. This reduced Q_{oss} charge helps to reduce the amount of recirculating current which is required in ZVS applications. This helps to reduce passive losses and increase the light load efficiency of designs.

2.5 Transfer characteristics

Around 95 percent of all flyback converters use peak current control. This means that the controller is sending the turn-off signal to the gate driver at a certain current value running through primary inductance of the main transformer and the MOSFET. There is a well-known failure mode in charger and adapter applications when the gate source voltage drops, for example during burst mode operation, and the MOSFET is not able to carry enough current to reach the peak current. In this case the MOSFET operates in the linear region and the MOSFET does not turn off, resulting in destruction of the application. Here the 950 V CoolMOS™ P7 can offer a very narrow $V_{GS(th)}$ (gate source threshold voltage) window from 2.5 V to 3.5 V with a typical value of 3 V.

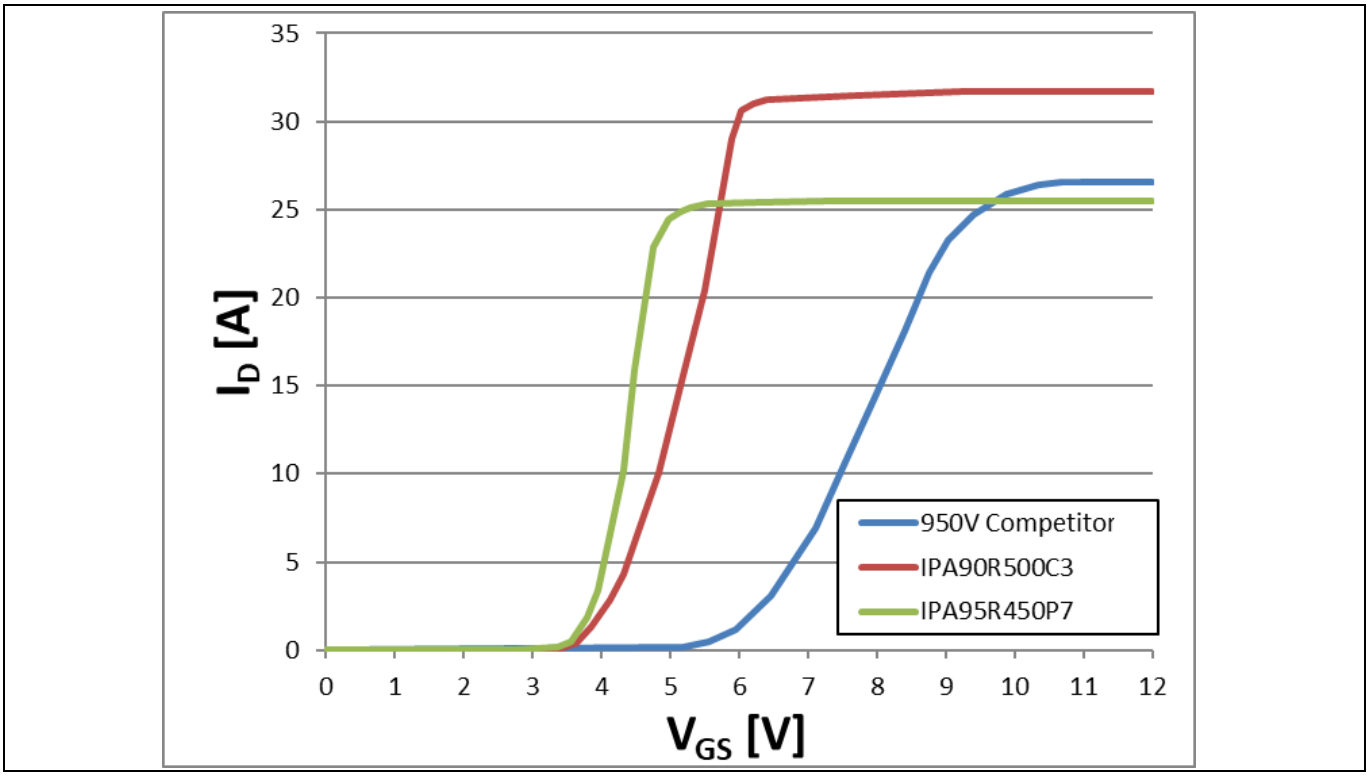


Figure 11 Transfer characteristics comparison of 450 mΩ and 500 mΩ devices at 25°C

The 950 V CoolMOS™ P7 shows the best-in-class trans-conductance behavior (in comparison to the main competitor) thanks to the market-unmatched current capability at low gate source voltage. This leads to the possibility of reducing the gate source voltage intentionally in order to minimize the overall driving losses and the possibility of satisfying new no-load operation requirements.

2.6 Avalanche

2.6.1 Introduction and avalanche operation mechanism

The general recommendation is to stay on the V_{DS} below $V_{BR(DSS)}$ (breakdown voltage) rating of the product represented in all datasheets. As market analysis has shown, 80 percent de-rating is used in all charger and adapter applications during standard operation, and this is allowed to rise to 100 percent during transients. This leads to the assumption that avalanche is not present in the applications mentioned. Nevertheless there are also surge tests done on customer applications during the qualification, which only represents a pass/fail test, where the MOSFET is not allowed to be the root cause of a failure. In this case it is hard to verify whether the MOSFET is driven into avalanche operation or not. A snubber network should always be used to limit the V_{DS} over-shoot and should be dimensioned so that the snubber is active before the $V_{BR(DSS)}$ of the MOSFET is reached. This can be seen in Figure 12.

The avalanche operation in a flyback can only be driven by the leakage inductance of the transformer, which is typically in the range of 1 to 2 percent of the main transformer primary inductance. Based on this there are much lower energies and inductance values as in previous MOSFET datasheets (older technologies like the C3).

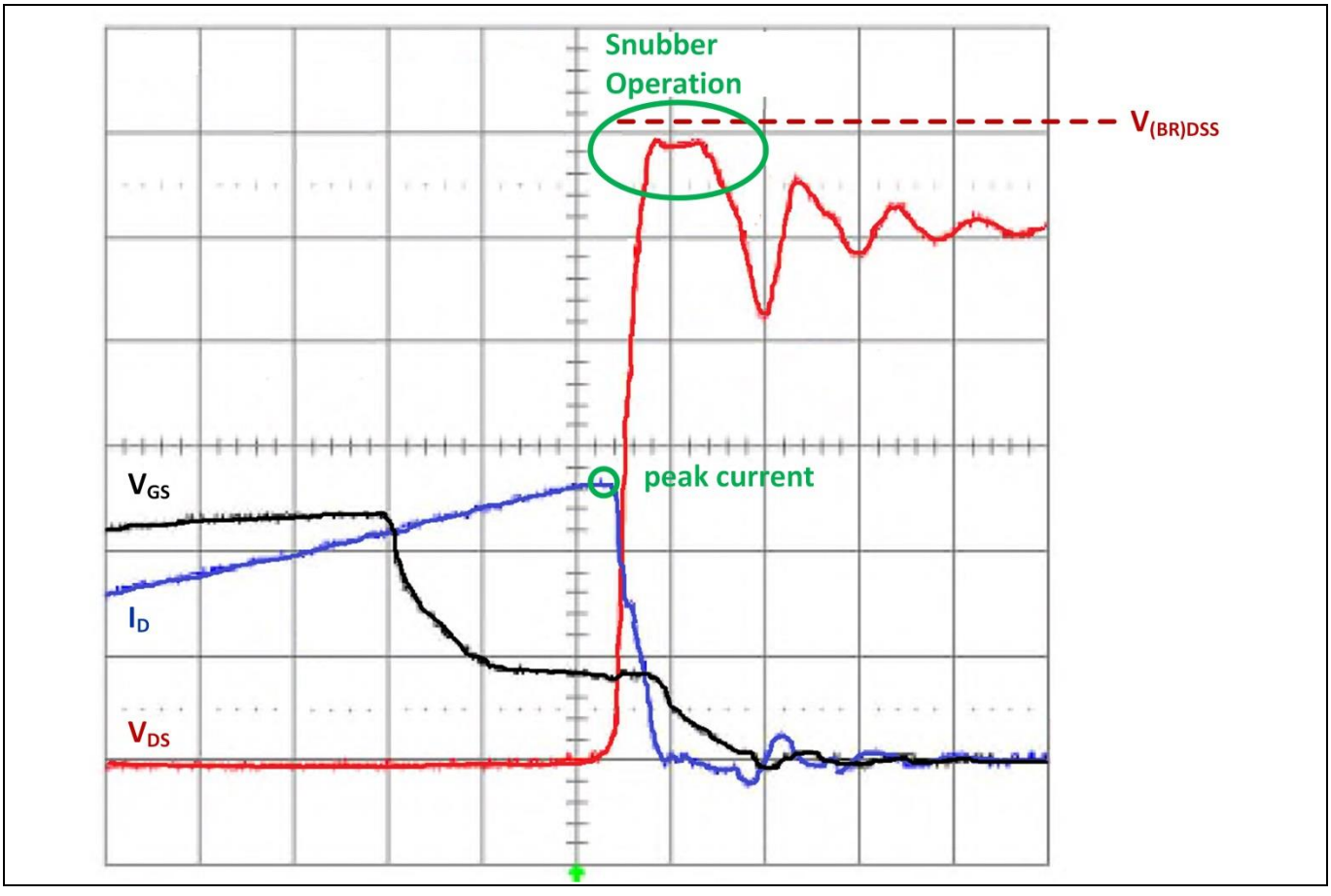


Figure 12 Flyback converter turns off avalanche operation

For more information, please see our previously published material:

- Key Facts about Avalanche (Link)
- Power MOSFET Avalanche Design Guidelines (Link)

As already discussed in other publications, an avalanche energy destruction with high energy and high inductance values is not representative of any low power SMPS application. Therefore Infineon adopts the avalanche conditions in all new datasheets of new technologies to meet the application design environment. The 950 V CoolMOS™ P7 introduces the current destruction mechanism ratings in all its datasheets. The current itself during the avalanche is limited by the peak current control and can therefore be controlled quite easily.

As an example, below is an extract from a 950 V CoolMOS™ P7 datasheet where the application-relevant/near-avalanche current is shown.

In addition to the standard ratings E_{AS} and E_{AR} shown in the datasheet this I_{AS} provides the customer with more information on real application conditions where the leakage inductance is quite small (much less than 1 mH).

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Application (Flyback) relevant avalanche current, single pulse[3)]	I_{AS}	-	7.0	-	A	measured with standard leakage inductance of transformer of 10µH

Figure 13 Application-relevant typical avalanche current (e.g. IPD95R450P7)

From feedback we have seen that these parameters are helpful for our customers, so we specified the I_{AS} as a typical value in all our 950 V CoolMOS™ P7 datasheets.

It can be seen in the last column in Figure 13 (“Note/Test Condition”) that in our internal tests a leakage inductance of 10 µH was chosen through all our $R_{DS(ON)}$s.

Connecting the I_{AS} datasheet value to a real application is explained as follows:

- Infineon XDPL8218 demo board equipped with 950 V CoolMOS™ P7 MOSFET
- Input 90 V AC to 305 V AC; output 40 W
- MOSFET used: IPN95R1k2P7
- More details in Infineon application note (ER_1803_PL21_1804_055653)



Figure 14 Infineon XDPL8218 40 W reference design board

Some detailed application parameters for the evaluation and calculation of the single-pulse avalanche capability are needed to give a first indication of whether the usage setting correlates to the MOSFET specification:

- R_{sense} (sense resistor): 0.2 Ω
- Peak current limit voltage: 0.304 V
- Leakage inductance of transformer: 4.5 µH
- Primary inductance of transformer: 544 µH

First of all you have to check your datasheet values for E_{AS}/E_{AR}/I_{AS} of the corresponding MOSFET.

Avalanche energy, single pulse	E_{AS}	-	-	11	mJ	I_D=0.7A; V_{DD}=50V; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.14	mJ	I_D=0.7A; V_{DD}=50V; see table 10

Figure 15 E_{AS} and E_{AR} datasheet value of IPN95R1k2P7

Application (Flyback) relevant avalanche current, single pulse[3)]	I_{AS}	-	3.0	-	A	measured with standard leakage inductance of transformer of 10µH

Figure 16 $I_{AS,typ}$ datasheet value of IPN95R1k2P7

Then you have to ensure that the peak current is not going to exceed the allowable (single-pulse) avalanche current of the MOSFET set via the controller's peak current control. In the equation below you can see that the peak current control will get active in the range of 1.6 A (+/- some tolerances) but is still 50 percent ahead of the typical value stated in the datasheet (Figure 16).

$$I_{PK} = I_{AS} = \frac{Peak\ current\ voltage}{R_{sense}} = \frac{0.304}{0.2} 1.52A < 3\ A$$

As a next step, make sure the leakage energy will not avalanche the MOSFET. All results can be calculated with the following formula:

$$E_{avalanche} = \frac{1}{2} \cdot L \cdot I^2$$

Filled up with the application data:

$$E_{avalanche} = \frac{1}{2} * 4.5\mu H * 1.52A^2$$
$$E_{avalanche} = 5.19\mu J < 140\mu J$$

As can be seen in the equation above, there is enough headroom in comparison to the datasheet values (Figure 15Figure 16).

As an optional checkpoint you can look at an extreme edge. The primary inductance itself should not avalanche the MOSFET at all.

This would imply a very large surge event and shows that even under an extreme condition (also repetitive) the MOSFET is still more robust than necessary (Figure 15).

$$E_{avalanche} = \frac{1}{2} * 544\mu H * 1.52A^2$$
$$E_{avalanche} = 0.628mJ < 11mJ$$

In summary a step-by-step approach is required to be sure a single surge event or an abnormal condition will not avalanche your MOSFET, which is not recommended and can lead to immediate failures or later field returns.

With this configuration it was possible to achieve a surge robustness of more than 2 kV. More examples will follow on the next page.

In order to see if the 950 V CoolMOS™ P7 is ready for surge qualification we have tested several internal demo boards and end customer designs and applied surge qualification directly to customer designs. The following table represents the results of this market test until design failure during surge qualification.

Table 1 Surge verification tests done (internal and end-customer applications)

Customer applications	L- N surge voltage	Fail	Note
20 W LED driver	2 kV	Fuse	No MOSFET destruction
40 W LED driver design	2.5 kV	Fuse, X-cap	No MOSFET destruction
40 W IFX adapter design	3 kV	Fuse	No MOSFET destruction
45 W IFX LED driver design	2.5 kV	X-cap fail	No MOSFET destruction
55 W LED driver	2 kV	Fuse, bridge rectifier diode	No MOSFET destruction

As can be seen in Table 1, all surge tests show the 950 V CoolMOS™ P7 surviving the surge event. But looking at an old design, optimized for C3, a failure on the MOSFET can happen. All our investigations, not only internal, have shown that in most of the cases the input filter design was not checked or adopted.

Generally it is best to stay below datasheet ratings in terms of energy and current destruction mode, and design/set an appropriate peak current control to prevent avalanche operation of the MOSFET. Most critical applications are single-stage flyback configurations, where the energy storage is done in the secondary side (e.g. lighting applications). In most charger and adapter designs, the energy storage is done with a huge bulk cap at the primary side and controllers with peak current control to reduce the amount of energy transferred to the switch during a surge event.

With the 950 V CoolMOS™ P7, a new topology is coming to the market. Especially with the use of the snubberless flyback, where no limiting snubber network is preventing the MOSFET going into avalanche operation mode, these effects should be a particular focus for every designer. Even in this topology it is important to design according to datasheet values (with de-ratings) and well-designed/adapted input filters to the needs of a new technology variant of our P7 family.

2.6.2 Avalanche destruction modes

As mentioned in the previous chapter, the needs of an application close to avalanche value became more important in lighting applications, where the energy storage is done on the secondary side and where the leakage inductance of the transformer is quite small.

Due to further technology improvements one of the critical parameters of the MOSFET was the avalanche rating in the datasheet. A direct comparison between the competition and Infineon was becoming difficult because the same conditions were not universally applied.

Therefore an Infineon internal test platform was designed to fulfill this need and to give customers additional information directly in the datasheet, coming closer to the application conditions (e.g. transformer leakage).

It should be made clear that this parameter "$I_{AS,typ}$" (Figure 16) is a typical value and was tested and evaluated during a laboratory test. As an indication for a designer, this should already provide a suggestion of what the

MOSFET can handle. Evaluations and calculations in customer designs still have to be performed and cross-checked. All other parameters should not be violated during normal and abnormal operation of MOSFETs (e.g. the SOA diagram during a surge event – and don't forget to de-rate in terms of cold temperatures -> V_{BRDSS})

Avalanche energy, single pulse	E_{AS}	-	-	29	mJ	I_D=1.8A; V_{DD}=50V; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.36	mJ	I_D=1.8A; V_{DD}=50V; see table 10
Application (Flyback) relevant avalanche current, single pulse[3)]	I_{AS}	-	7.0	-	A	measured with standard leakage inductance of transformer of 10µH

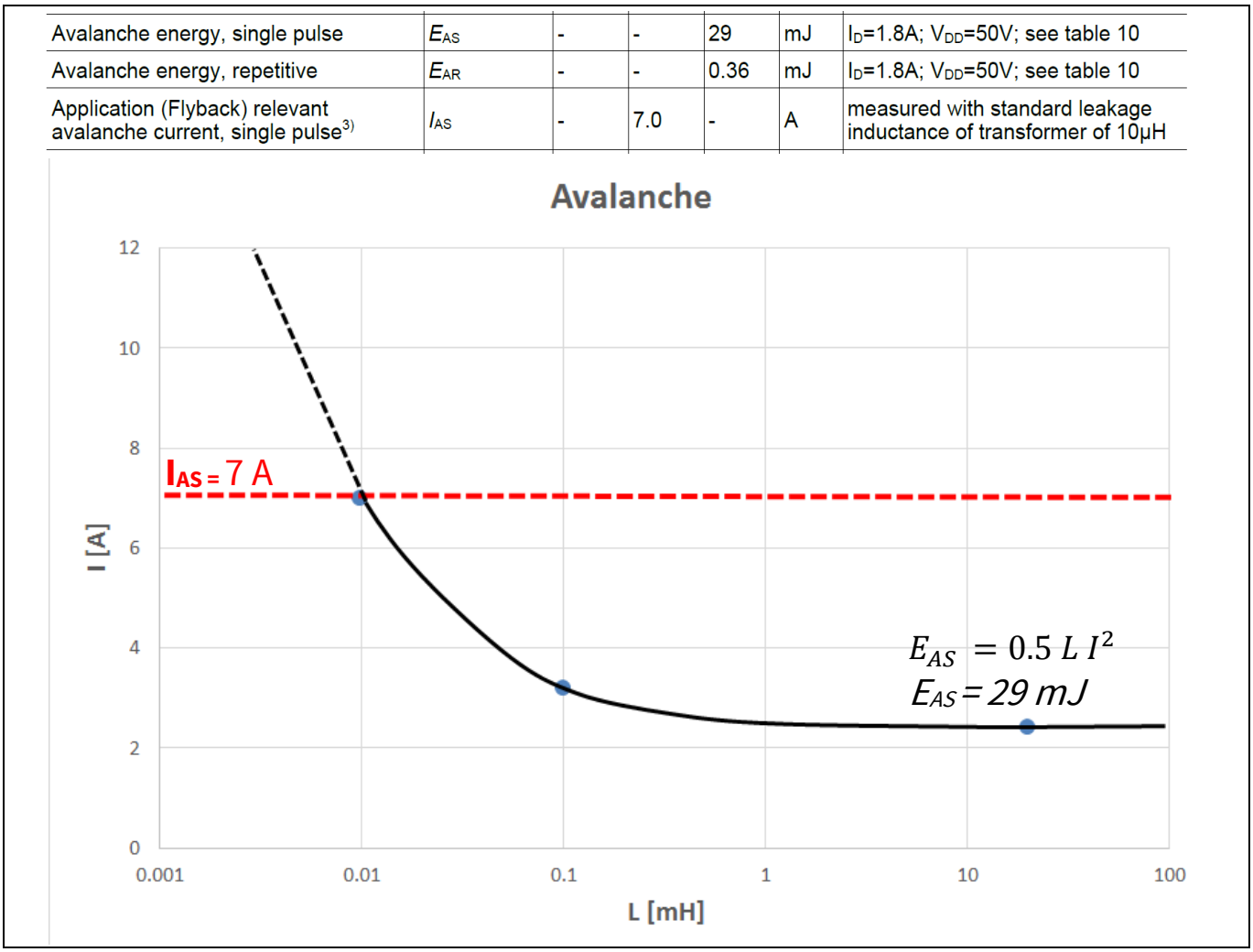


Figure 17 Correlation between avalanche current and inductor value (IPx95R450P7)

In the MOSFET avalanche there are two key destruction modes that must be avoided. The first is the energy mode of destruction and the second is the current mode of destruction.

When avalanching occurs in the MOSFET the device behaves like a Zener diode that is conducting. There is a fixed breakdown voltage across the device and a current begins to flow through the device. The losses in the MOSFET are the total current multiplied by the breakdown voltage of the device. These losses end up heating the chip, and if the chip temperature exceeds 150°C then the device can be destroyed due to overheating. This is the thermal mode of destruction. The actual rate of energy transfer into the MOSFET will change depending on the inductance that is being used, as a larger current will heat the device more quickly to this failing temperature, and there is less time to dissipate the heat. A datasheet value is provided for this condition as the E_{AS} value. This value is measured with a particular test inductance and will vary depending on the MOSFET chip starting temperature and the rate of energy transfer into the MOSFET.

As the inductor providing the avalanche energy gets smaller the current required to get the same amount of energy gets higher. Eventually the current mode of destruction of the device will be the limiting factor. There are several causes of this current mode of destruction and it needs to be characterized for the particular device.

For the 950 V CoolMOS™ P7 this current limit is provided as the I_{AS} value, which is tested with a 10 µH test inductance. In a peak current mode controlled flyback this destruction can be avoided by ensuring that the peak current mode limit is set below this threshold. This will ensure that if the leakage ringing of the V_{DS} exceeds the breakdown voltage of the device, the current transferring into the device is below this destruction limit.

3 Benchmarking of 950 V CooMOS™ P7 in low-power designs

As already anticipated in the target applications the 950 V CoolMOS™ P7 is tailored for low-power applications that are using flyback topologies, and PFCs. In order not to limit the possible usage of the latest Infineon technology, some internal and external evaluation/demo boards as well as boards from the open market have been tested.

This chapter will show the performance benefits of the 950 V CoolMOS™ P7 in comparison to the main competitor in this market.

3.1 6 W bias supply

A variant of our well-known auxiliary power supply was developed. This power supply was already available in an 800 V version.

Now, with the snubberless approach and the 950 V CoolMOS™ P7 (IPU95R3k7P7) on board, the auxiliary power supply again comes with a performance increase compared to the former versions, and the 950 V CoolMOS™ P7 demonstrates the lowest temperatures and the highest efficiency.

On all our demo boards, where an auxiliary power supply is needed, from now on the latest version will be implemented. To increase the efficiency of older demo boards, the new version is pin-to-pin compatible, so can easily be replaced. For more details and the dedicated application note, please check the support material page, where efficiency and temperature measurements in comparison to several former versions/variants are also shown.



Parameter	Value
Input voltage	120-440 V_{DC}
Output voltage	12 V_{DC}
Output current	0.5 A
Output power	6 W
Efficiency	85.2 %
Dimension	31x35x15 [mm]

Figure 18 6 W bias supply and specification

Typically all designers of switching applications are interested in the mold compound temperature at full load, the efficiency at 75 percent, 50 percent and 25 percent load points, and the average efficiency. The following diagram represents the relative efficiency comparison over the output power. For reference the IPU95R3K7P7 is used.

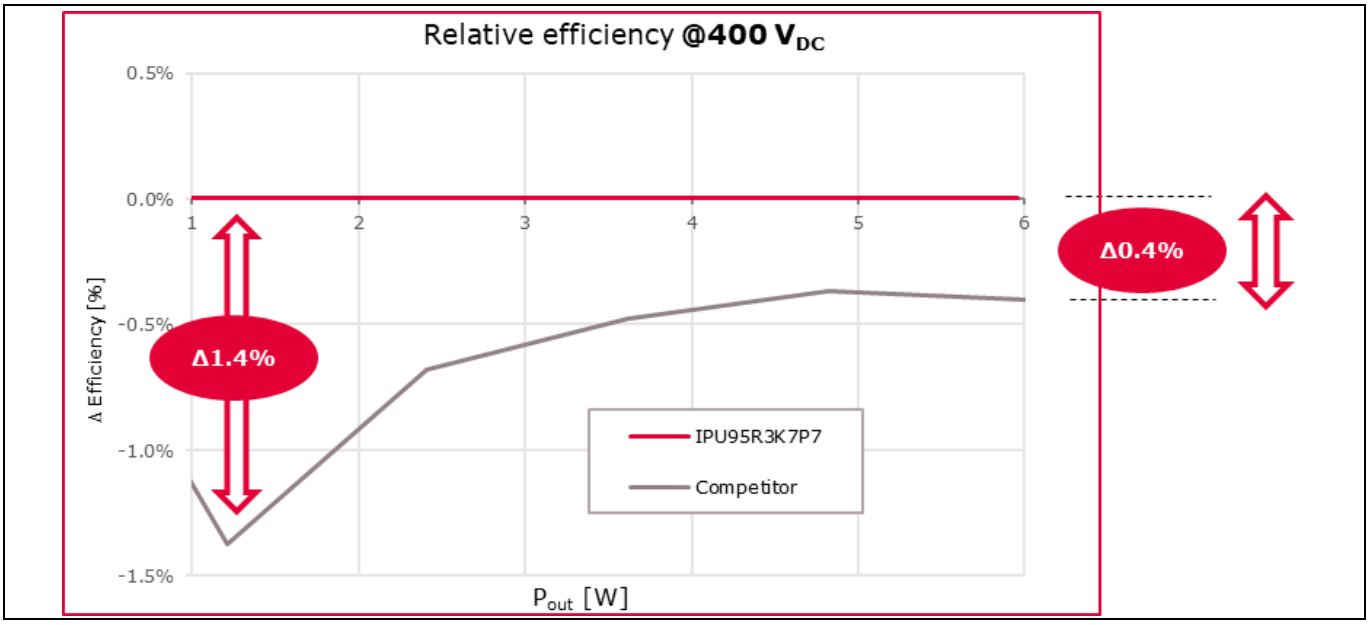


Figure 19 Relative efficiency chart – 6 W bias supply

Figure 19 shows that an efficiency gain of about 0.4 percent up to more than 1 percent can be realized in a direct 1:1 comparison with the main competitor.

But it's not only the relative efficiency that is of interest for the designer; in Figure 20 the temperature graph shows a nearly 5°C lower MOSFET mold compound temperature. In terms of lifetime this is not a negligible value at all, and also reduces the total temperature in a closed environment.

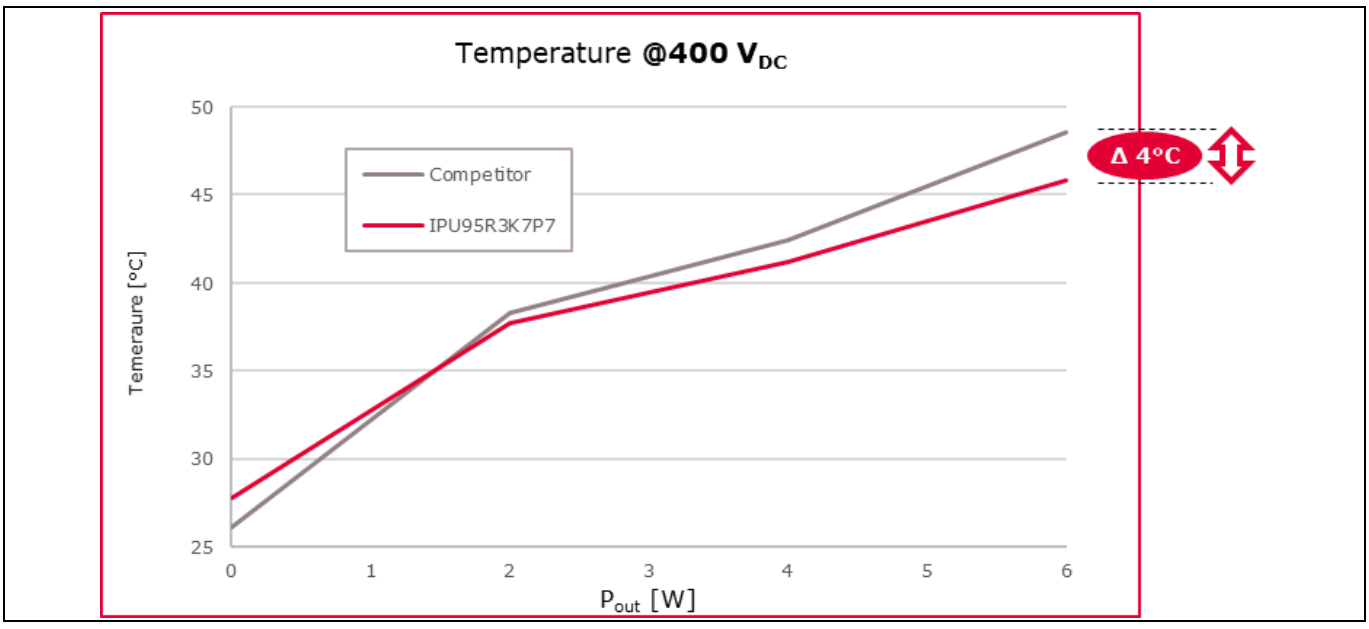


Figure 20 Temperature over output power chart – 6 W bias supply

3.2 20 W LED driver from the open market

As another example, a customer application from the open market was chosen. A 20 W LED driver with wide range input and a standard peak efficiency around 80 percent run through our internal evaluation, giving an indication at an early stage of usage in a “real” customer application.

These measurements show efficiency and thermal behavior in a 1:1 comparison; nevertheless every customer has its own release criteria in terms of EMI and surge. This has to be proven finally on the customer side, because our end customers are selling the final product where they have also to cover tolerances from other components (which can also influence the MOSFET’s behavior).

However, showing customers the following results will convince them much more than showing a demo board measurement.



Parameter	Value
Input voltage	110-240 V_{AC}
Output voltage	0-22 V_{DC}
Output current	900 mA
Output power	20 W
Efficiency	81.8%
Dimension	108x52x22 [mm]

Figure 21 20 W LED driver with specification

With the new 950 V CoolMOS™ P7 the efficiency gain at the full-load point with high line (230 V AC) input voltage was in the range of 0.4 percent compared to the closest and main competitor.

This impressive increase also convinced our customers to change over now to our latest technology, also increasing the safety margin in terms of breakdown voltage (also C3 900V was in use).

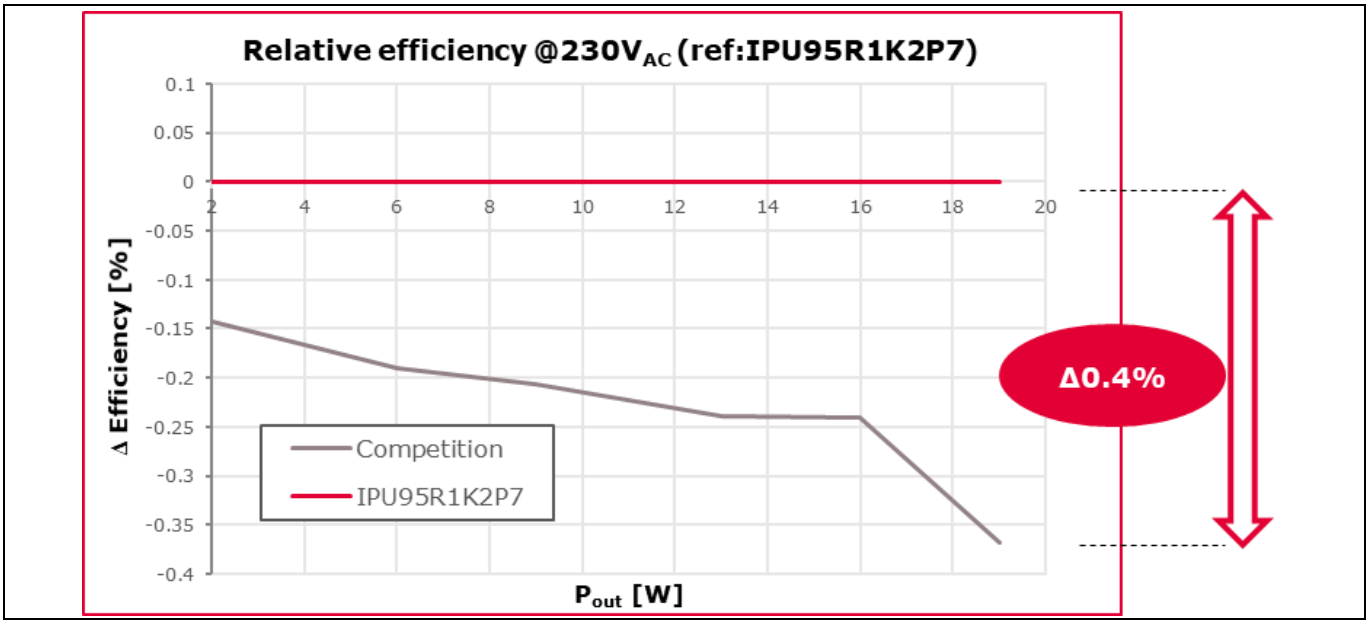


Figure 22 Relative efficiency chart – 20 W LED driver

But it's not only the efficiency that plays a role in smaller form factor applications; temperature is also a consideration (Figure 23). The reduction here is nearly 10°C, which shows the strength of the 950 V CoolMOS™ P7.

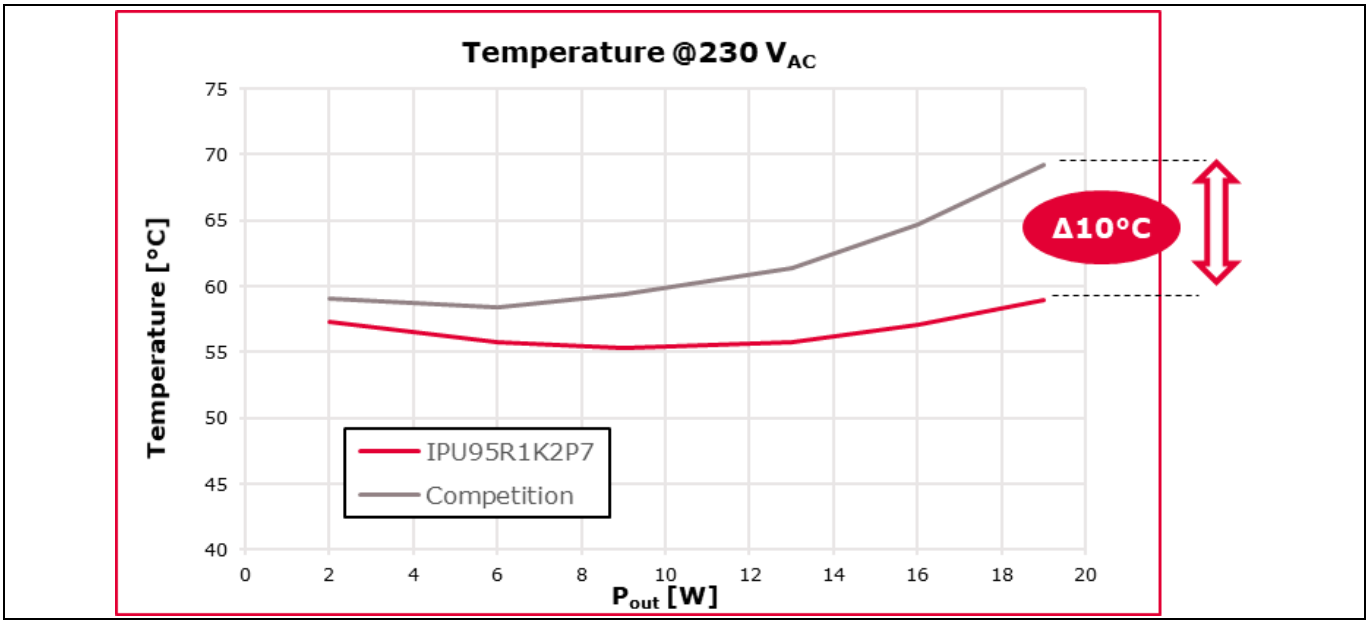


Figure 23 Temperature over output power chart – 20 W LED driver

3.3 40 W Infineon snubberless flyback demo board

The introduction of the 800 V CoolMOS™ P7 brought a modular platform for the promotion and evaluation of new MOSFET generations. The original 45 W adapter demo board was intended to be a form, fit and function test platform for charger and adapter applications. This platform was also chosen this time to give our customers the ability to test the 950 V CoolMOS™ P7's performance as well the snubberless flyback option.

This 40 W snubberless flyback board can be ordered via ISAR, the details of which are at the end of this application note.

To summarize, it's a wide input range flyback design, targeting adapter solutions for notebooks with 19 V DC output for illustration.



Parameter	Value
Input voltage	90-265 V_{AC}
Output voltage	19 V_{DC}
Output current	2 A
Output power	40 W
Efficiency	88.1%
Dimension	100x37x25 [mm]

Figure 24 40 W snubberless flyback adapter demo board with specification

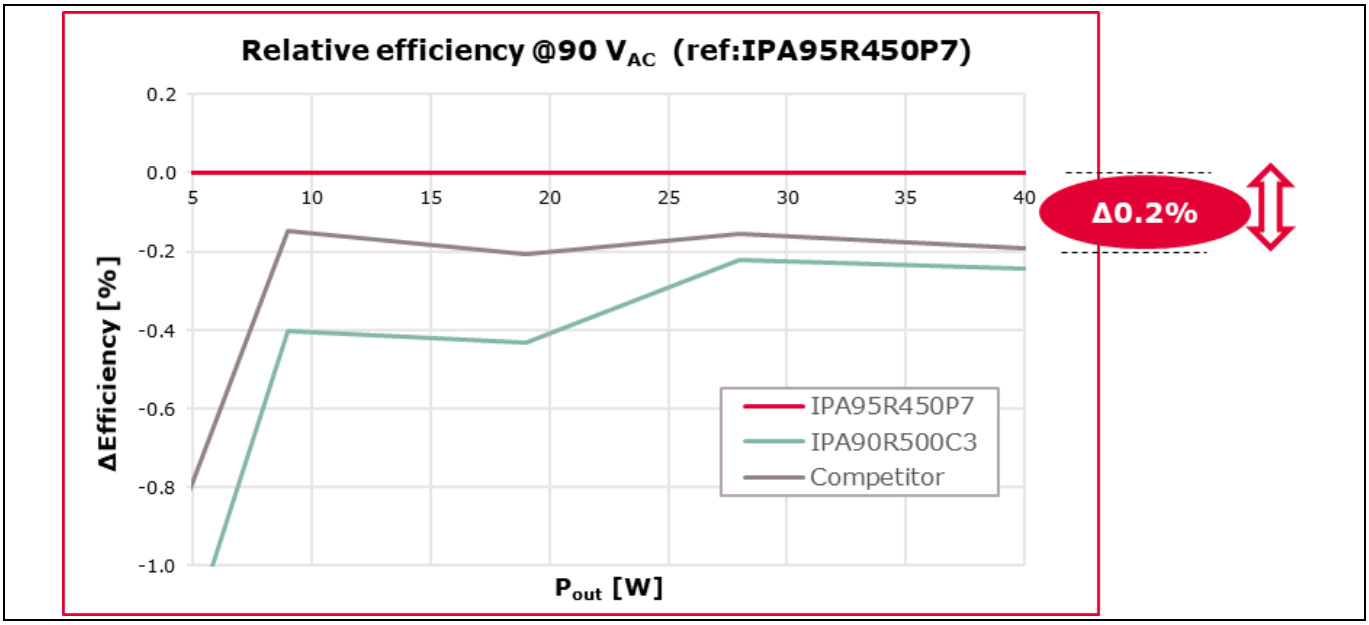


Figure 25 Relative efficiency chart – 40 W snubberless adapter demo board

In the chart in Figure 25 it's obvious that an efficiency difference in the range 0.2 percent at full load is outperforming the competitor part.

Another interesting package variant tested is the SOT-223. Due to the large copper area around the drain pad and the pin-to-pin compatibility of DPAK and SOT-223 it was possible to reach the same performance in the application. So this is quite impressive, and shows a further reduction in cost for our customers.

In Figure 26 below you can see that at the lowest input voltage the new Infineon device stays at least 5°C cooler at the full load point.

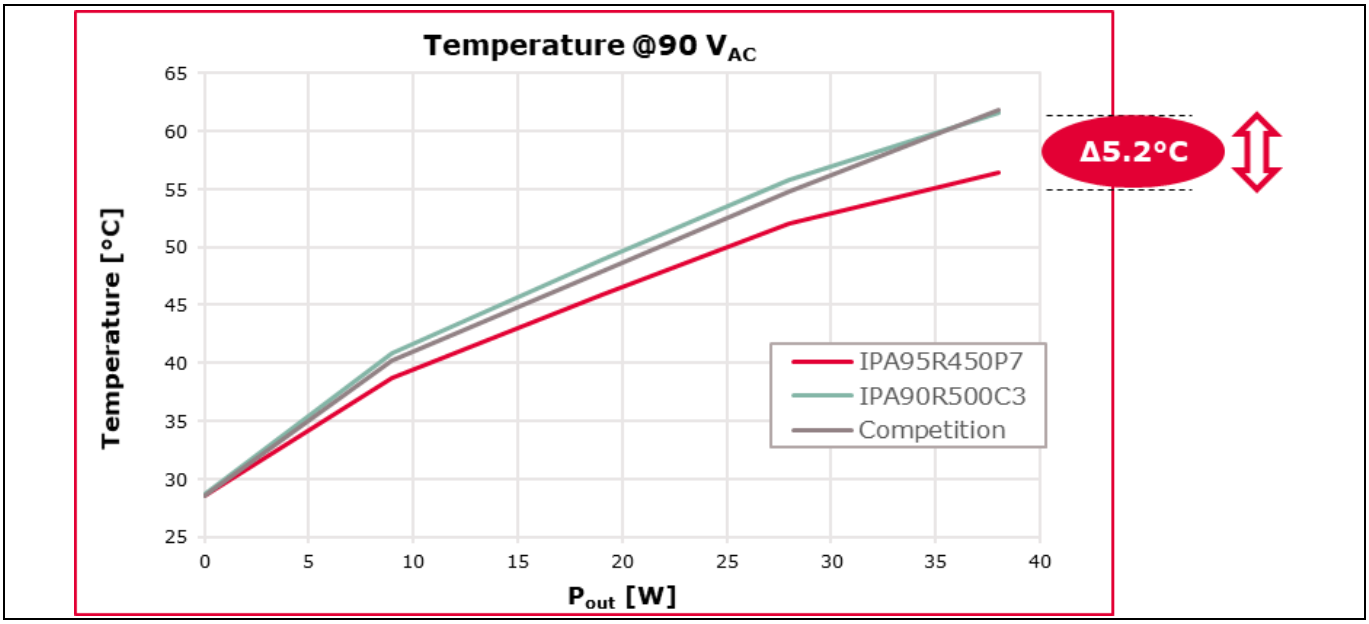


Figure 26 Temperature over output power chart – 40 W snubberless adapter demo board

The customer must plan the usage of a SOT-223 in advance if they want to have a similar performance. If the copper area around the drain pad is only the minimum DPAK footprint, the thermal performance of SOT-223 is

worse in a 1:1 $R_{DS(on)}$ comparison on its minimal footprint, but can be overcome as shown in the 40 W example in Figure 24. There the drain pad copper area was already adapted (increased) in the first design phase. You can find more details on the application in a dedicated application note and in several SOT-223 presentations.

3.4 60 W flyback board from competition

A last application we want to show is a 60 W wide input range flyback board from one of our competitors. Detailed specifications can be seen in the parameter table below.



Parameter	Value
Input voltage	90-227 V_{AC}
Output voltage	52 V_{DC}
Output current	Up to 1.2 A
Output power	60 W
Efficiency	89.7%
Dimension	165x50 [mm]

Figure 27 60 W flyback board

Involving not only internal but also external boards – including competitor promotion boards – in our tests was a decision made due to the fact that often a board is designed precisely for one MOSFET technology only. It should be mentioned that in the case of a direct replacement the customer might find the overall performance acceptable, as not all customers seek the same balance between cost and performance.

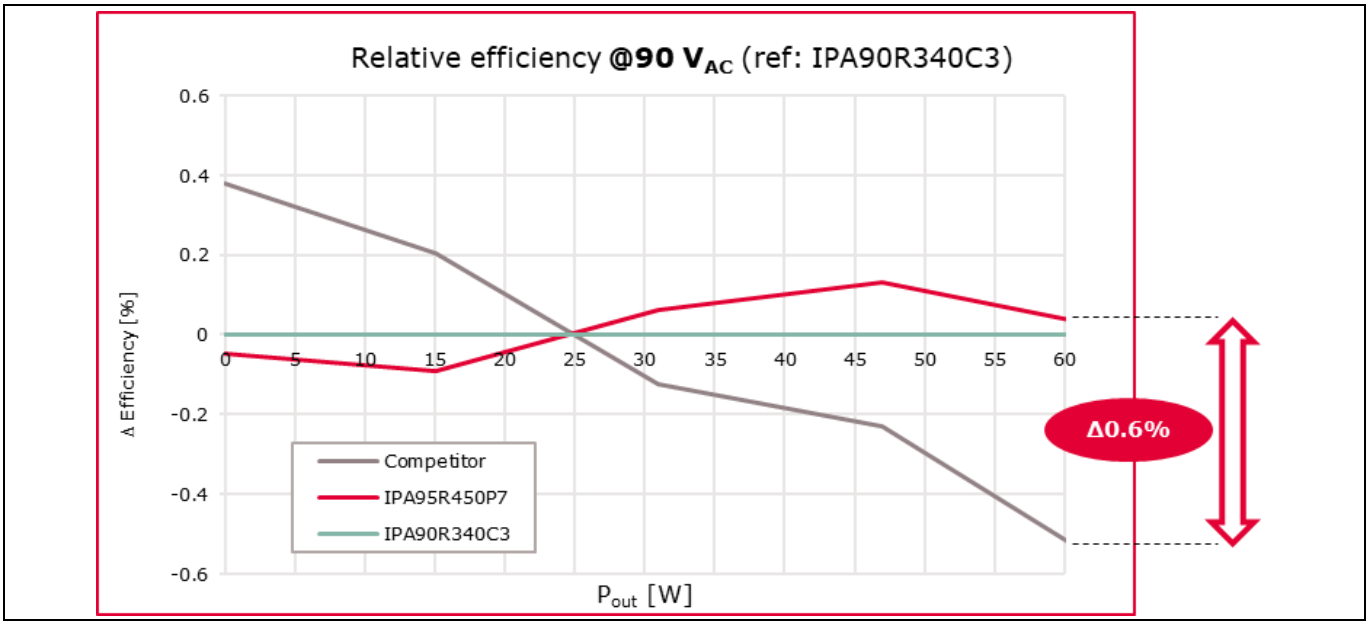


Figure 28 Relative efficiency chart – 60 W flyback board

If you look now at the lower graph above, at the 60 W full-load point, the efficiency difference from our main 500 mΩ competitor is in the range of 0.6 percent. It has to be taken into account that the 950 V CoolMOS™ P7 has a much smaller chip inside and also is 50 mΩ lower in $R_{DS(on),max}$. Even reaching such a performance is quite difficult and for sure, the $R_{DS(ON)}$ typical, the lower integrated R_g and $R_{DS(ON)}$ hot performance (Figure 8) helps here a lot.

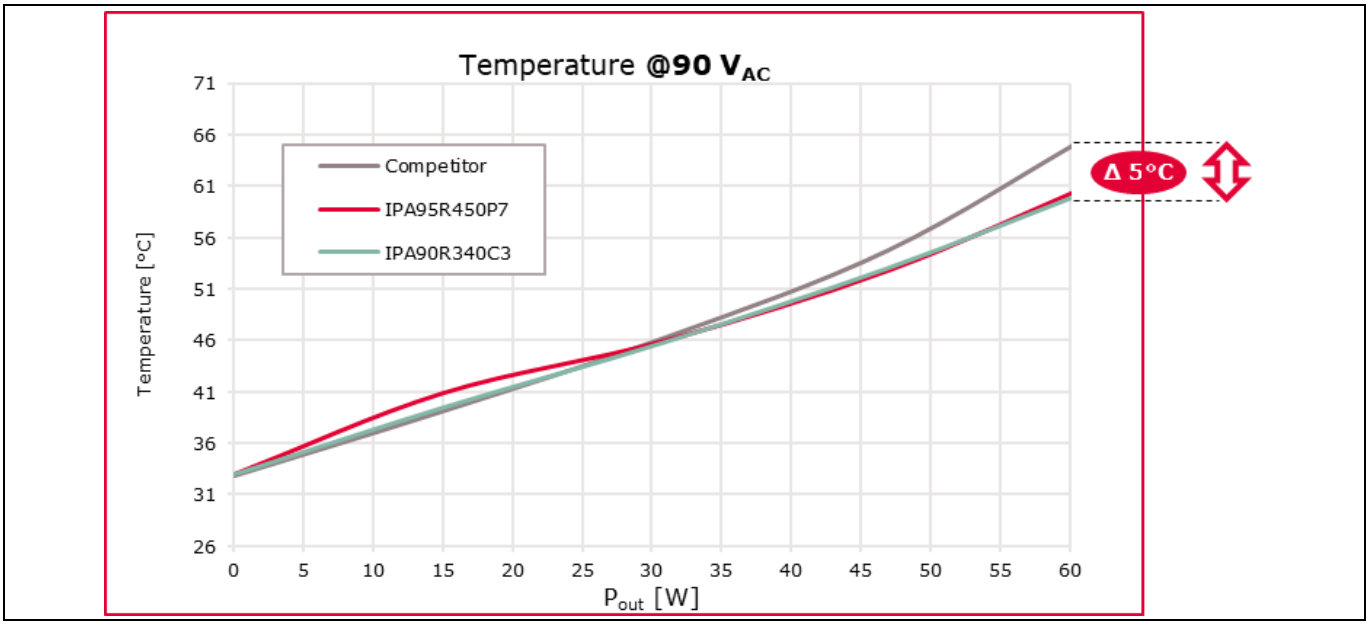


Figure 29 Temperature over output power chart – 60 W flyback board

In Figure 29 the temperature vs output power graph is shown. At 90 V AC, the lowest possible input voltage, the current for the MOSFET is the highest. But at the full-load point, P7 remains 5°C lower (Figure 29).

4 Portfolio

The 950 V CoolMOS™ P7 provides an optimized portfolio with respect to $R_{DS(on)}$ classes and offers the most relevant packages for low-power application.

All main target applications are covered, including lighting, chargers and adapters, smart metering, industrial SMPS and auxiliary power supply applications.

Portfolio 950 V P7 SJ MOSFET

Industrial Grade

ESD Class (HBM)	RDS(ON) [mΩ]	TO220FP	IPAK LL	DPAK	SOT223
1C	3700		IPU95R3K7P7		IPN95R3K7P7
2	2000		IPU95R2K0P7	IPD95R2K0P7	IPN95R2K0P7
	1200	IPA95R1K2P7	IPU95R1K2P7	IPD95R1K2P7	IPN95R1K2P7
	750	IPA95R750P7	IPU95R750P7	IPD95R750P7	
	450	IPA95R450P7	IPU95R450P7	IPD95R450P7	



Figure 30 950 V CoolMOS™ P7 portfolio

In addition to traditional packages, Infineon also offers the full portfolio as bare die.

Already well known in the P7 family is the integrated Zener diode, protecting the gate structure up to a level of 2-4 kV. It can be seen in the table to the lower right, the HBM class 2 can be guaranteed up to 2 Ohm, the 3.7 Ohm parts come with class 1C.

Furthermore Infineon is the sole supplier of SOT-223, enabling and supporting customers with smaller designs and ensuring lower BOM costs.

On the market, we see one important competitor where we can offer now a much lower $R_{DS(ON}$ in DPAK enabling possible change in terms of package selection. Our lowest $R_{DS(ON}$ in C3 technology was 1.2 Ohm, now we are able to put a 450 mOhm chip in the DPAK package, which results in markets best in class $R_{DS(ON}$ in this SMD package.

The customer benefit is obvious. You can design an application much smaller, thinner and more efficient, even when coming from leaded packages like TO-220 to an SMD solution. A further benefit is lower production cost due to machine assembly with the wave soldering process.

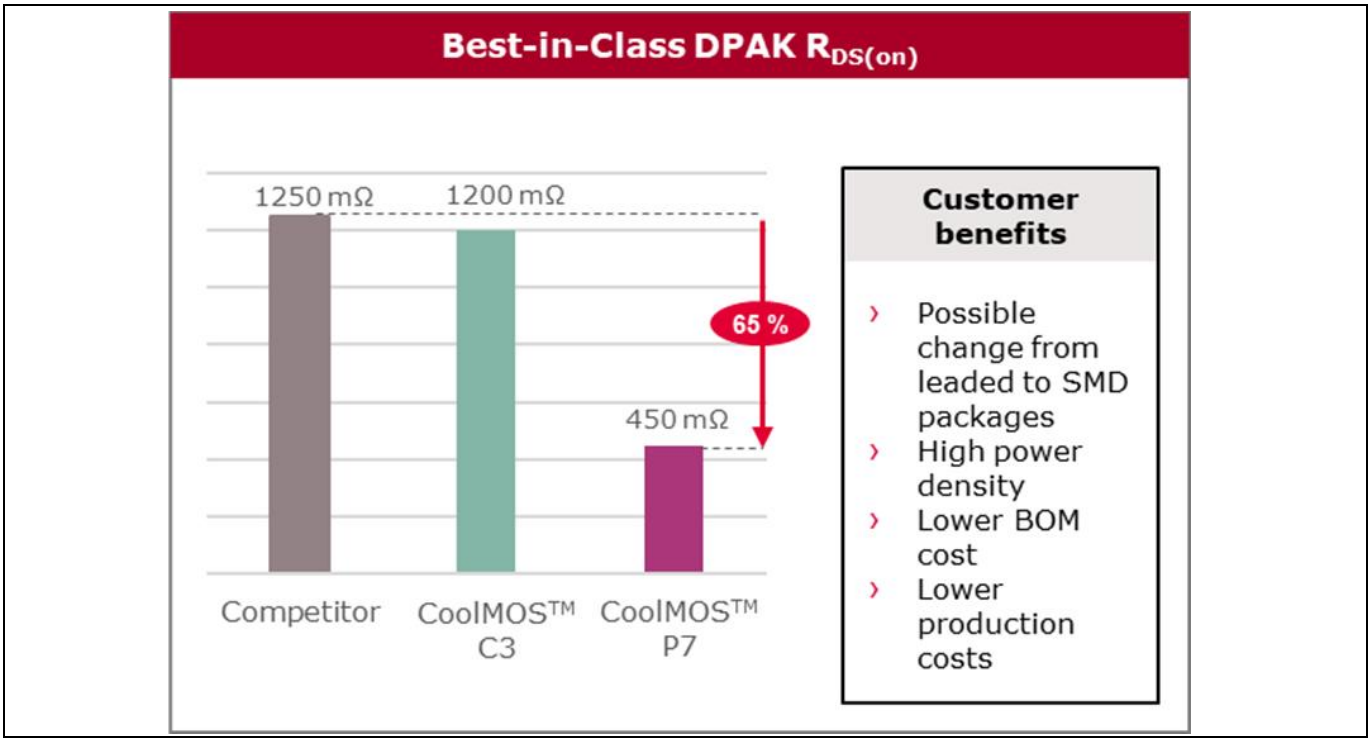


Figure 31 Best in class $R_{DS(ON)}$ for DPAK

Before the final chapter, which includes some design recommendations and rules, please note that there is a lot of additional material (demo boards, simulation model, etc.) for the 950 V CoolMOS™ P7 available at www.infineon.com/p7.

5 Design considerations

This final chapter will describe the most relevant design considerations when deciding to use the latest 950 V Infineon technology.

5.1 Paralleling of MOSFETs

These applications typically do not use paralleled MOSFETs; nevertheless in order to parallel MOSFETs a gate bead is always recommended and depends on the parasitics of the PCB itself.

5.2 Source impedance (source bead)

Source impedances are used in order to slow down the di/dt on the drain path, resulting in a lower drain source over-voltage peak.

Nevertheless, this also induces a voltage drop during turn-on and turn-off that can lead to oscillations in the gate drive loop. This influences the general EMI behavior and could also lead to destruction of any MOSFET if this voltage oscillation drives the gate source voltage over +30 V or under -30 V.

Therefore a source bead is not recommended to limit a possible over-voltage peak from drain to source. For more details and practical examples to optimize the EMI behavior of the MOSFET in the application, please also see the Infineon application note from the former CE series (Link). All optimization steps shown can also be used for our latest P7 technologies.

5.3 Target applications

The 950 V CoolMOS™ P7 is not allowed to be used in half-bridge or full-bridge configurations, or any other topology where a hard commutation on a conducting body diode can appear.

It’s tested and proven that in PFC and flyback topologies the latest generation has found its perfect fit.

6 Support material

Dedicated support material, not only for the 950 V CoolMOS™ P7, but also for the full P7 series, can be found at: www.infineon.com/p7

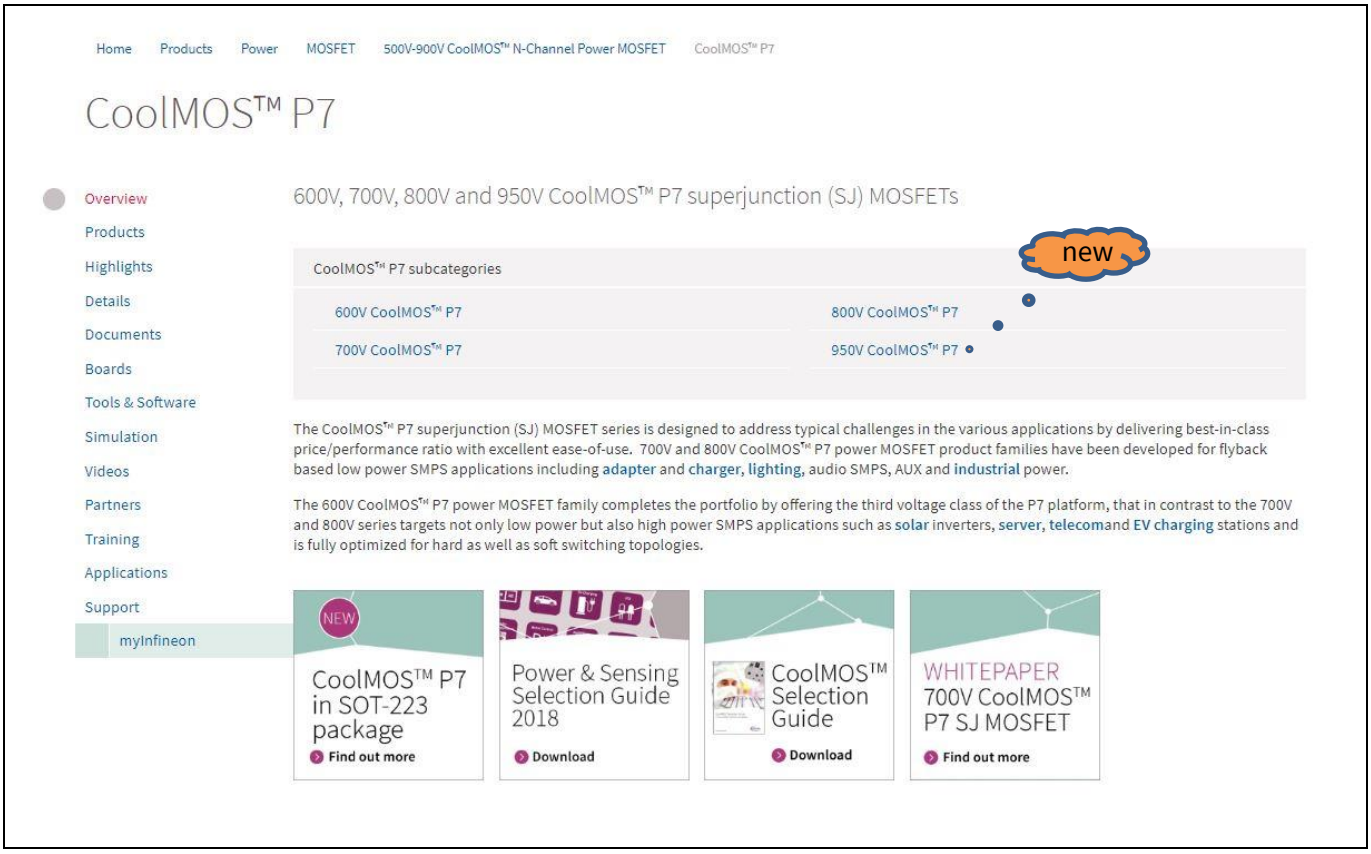


Figure 32 Dedicated P7 support material web page

In the “boards” chapter two dedicated boards equipped with 950 V CoolMOS™ P7 MOSFETs can be found and ordered via the Infineon internal order system or as an external partner/customer via the online purchasing system.



Figure 33 Support material – 950 V CoolMOS™ P7

Revision history

Document version	Date of release	Description of changes
v 1.0	27.07.2018	Final

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