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CoolMOS™ C7 650V Switch in a Kelvin Source Configuration

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1 Introduction

With new generations of power switches becoming faster and faster, the effect of the parasitic elements of package and board limit more and more the overall system performance. In many applications the switching losses are significantly increased by the negative feedback caused by the parasitic inductance in the source lead of the power switch. An effective measure to overcome this problem is to provide an additional connection to the source (Kelvin connection), that is used as a reference potential for the gate driving voltage, thereby eliminating the effect of voltage drops over the source inductance (Fig. 1). The achievable efficiency improvement, resulting mainly from faster switching transients, can in fact be significant. This is demonstrated by both simulations and measurements for CoolMOS™ C7, Infineon's latest generation of superjunction power transistors. Moreover, the very clean gate-to-source driving voltage signal enables the user to easily stay compliant with gate voltage limitations. As a drawback, however, the gate driving circuitry has to deal with considerable voltage spikes with respect to ground. The potential difficulties arising from that can be overcome by utilizing a dedicated gate driver IC, which isolates the output from the input by means of an integrated coreless transformer.

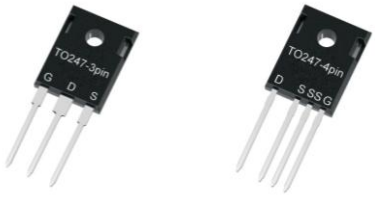
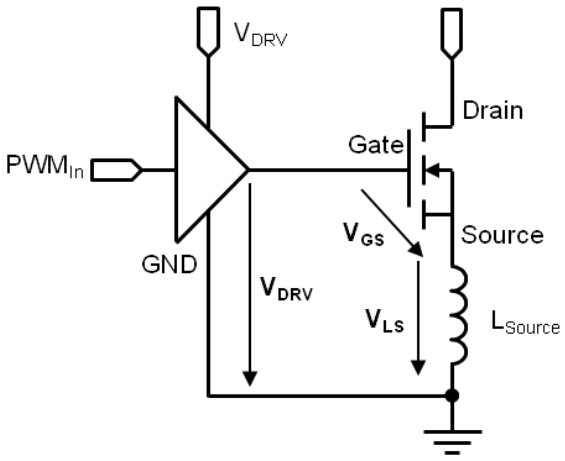


Fig. 1 TO-247 package and TO-247 4pin package with Kelvin source connection (source sense (SS))

2 System aspects

The ever-increasing demands on efficiency and/or compactness of power systems have led to impressive results in the development of power switches. The latest generation superjunction MOSFETs [1, 2] and new technologies utilizing wide bandgap semiconductors including Silicon Carbide or Gallium Nitride, are able to switch several hundreds of volts and several tens of amperes within a few nanoseconds. But to benefit from this potential, an appropriate system environment is crucial.



In common gate drive arrangements the fast current transient causes a voltage drop V_{LS} across the parasitic inductance of the source of the switching transistor that counteracts the driving voltage. By considering the induced source voltage to be given by V_{LS} = L * di/dt, it can be easily seen, that the typical parasitic inductances of package and PCB in the range of a few nH limit the achievable current slope. This may lead to slowing down the switching transient and increasing the associated energy loss [3].

$$V_{GS} = V_{DRV} - V_{LS} = V_{DRV} - L\frac{di}{dt}$$

Fig. 2 Standard gate drive schematic with parasitic source inductance in gate drive loop

The best method to eliminate this effect is obviously to not include the source inductance in the gate driving loop. This is achieved by providing an additional connection to the transistor source (4pin package) that serves as the reference potential for the driver. Fig. 3 depicts this concept for a classic PFC boost stage. The complete output stage of the gate driver is floating with respect to the power ground (or the switching node in high-side applications) by the voltage drop across the source inductance, and the negative feedback can be completely avoided.

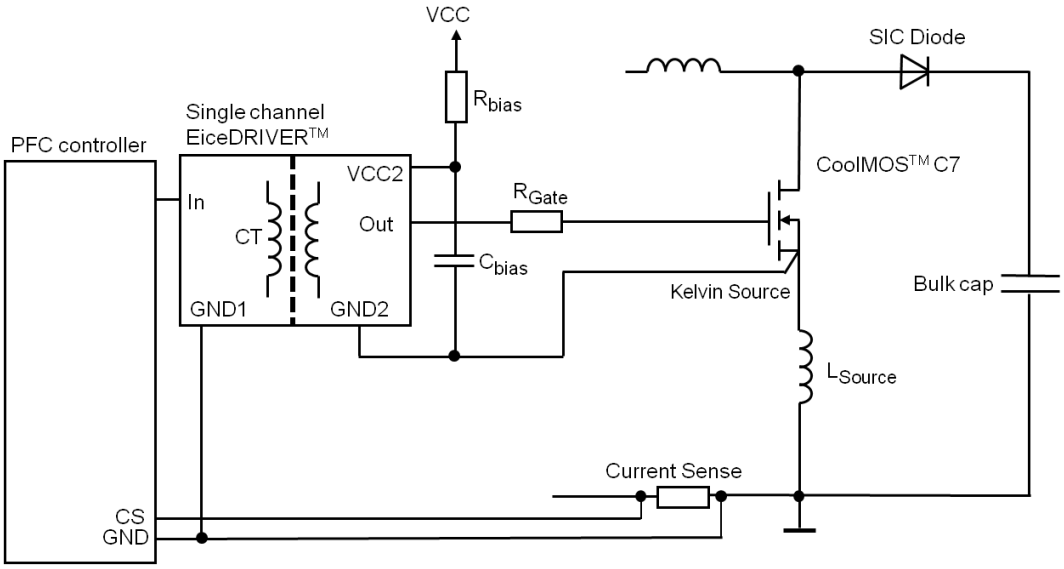


Fig. 3 Block diagram of PFC for 4pin configuration with coreless transformer driving

Same schematic is also possible with standard driver fitted by a signal RC input filter.

2.1 Layout example with standard TO-247

In a customer layout it is often difficult to connect the source pin very close to the package due to some geometrical constrains as seen in Fig. 4. This results in high source inductance values and therefore high voltage drops at each switching and reduction of the efficiency for high current operation.

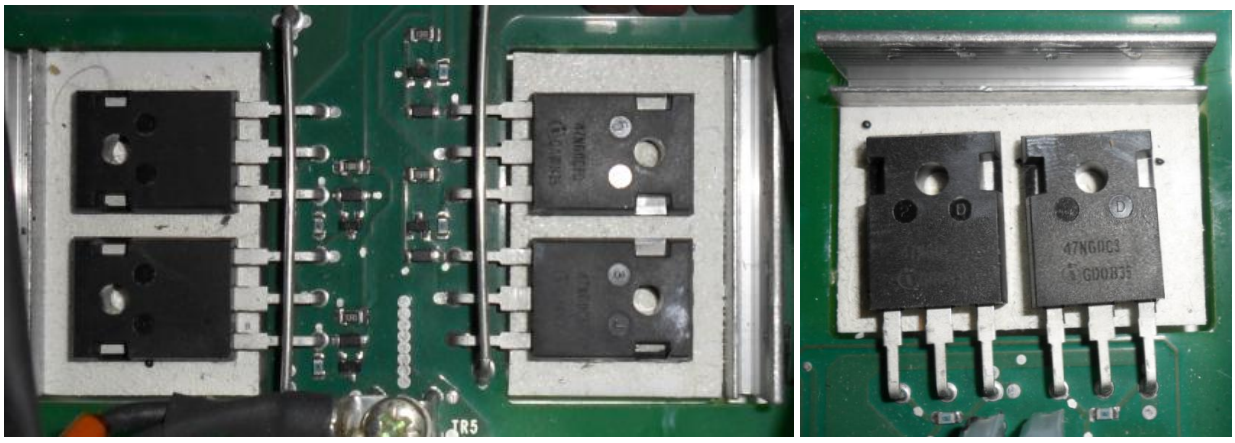


Fig. 4 Commercial layout reference with high source inductance

With the new TO-247 4pin package such placement would have both good cooling possibilities and low source feedback to the gate driving circuit.

3 Driver requirements

However, it should be clear that the effects associated with a “floating” driver output stage require very careful investigation. In a monolithic driver IC realized in a conventional junction isolated wafer process, the observed voltage peaks in the range of +/- 20V (or even higher) can be critical in terms of latch-up sensitivity and may require costly design and layout measures. On the other hand, dielectrically isolated processes suffer from significantly higher cost and poorer thermal behavior.

This is why it was decided to use a gate driver in a 2-chip MCM approach, that utilizes Infineon’s “Coreless Transformer” (CT) technology to isolate the ground-referenced input circuitry from the output driving stage (such an isolation is required to drive high-side switches in high-voltage applications). CT utilizes on-chip coupled inductors realized in the existing metal layers to transmit the gate drive signals from the input to the output stage with isolation provided by a thick inter-metal oxide. This approach offers high speed and very good common-mode transient immunity, which is crucial when taking into account the very fast voltage transients apparent when driving high-side switches. The Infineon EiceDRIVER™ family offers a wide range of CT based gate drivers supporting these requirements. Future products will also be available in cost efficient, compact packages.

3.1 RC definition for the driver supply

This paragraph will help to define the values for the RC network shown in Fig. 3 for the power supply to the driver. To choose the values we first need to know the Gatecharge of the driven CoolMOS^{TM}.

For taking the **IPZ65R019C7**, the latest CoolMOS^{TM} technology from Infineon as reference to calculate the dimensioning for the highest Gatecharge type, we find in the datasheet the total Gatecharge Q_g=215nC. Considering that the total charging energy has to be delivered by the capacitor directly together with the equation Q=C*U we find that the voltage change at the capacitor to charge or discharge the gate is calculated as $dU_c=Q_g/C_{bias}$.

An acceptable voltage change at a single switching cycle of about dU_C=400mV is reasonable. Putting this into the equation we derive $\mathbf{C_{bias}=2*}Q_g/dU_c$=2*215nC/400mV**=**1.07µF. In order to compensate the displacing energy from the source inductance seen as a ground bouncing voltage peak at turn on and turn off transient it is necessary to increase this value according to the switched current in L_{source} and the switching speed di/dt. As a rule of thumb one would take the value 10times higher and use **10µF** instead.

For a simplified definition of the decoupling resistor R_{bias} the maximum allowed displacement current will be considered. In addition to this it also has to be considered, that the consumed power for the Gatecharge has to be delivered through this resistor.

First let’s do the simplified calculation for the maximum value in order to deliver the Gatecharge power through the R_{bias}. We take the equation $P_{Gate}=2*0.5*Q_g*U_G*f$. This means for the **IPZ65R019C7** operating at 100kHz and 12V_{cc} drive gate drive losses of P_{Gate}=2*0.5*215nC*12V*100kHz=0.258W. Out of this we derive that the average charging current for the C_{bias} has at least to be $I_{bias}=I_G=P_{Gate}/U_G$= 258mW/11.8V=22mA. To follow the pragmatic approach one can choose 40mA. Therefore the resulting decoupling resistor R_{bias} would be $\mathbf{R_{bias}}$= dU_C/I_{bias}=400mW/40mA=**10Ω.**

Considering as cross check this R_{bias}=10Ω for a peak voltage spike on the L_{source} during switching transient of 20V we derive a displacement current up to 2A for some fraction of a nanosecond, which therefore is a reasonable and acceptable value.

4 Simulation results

The achievable improvement is clearly demonstrated by the simulation results depicted in Fig. 5 and Fig. 6. Here for a CoolMOS™ C7 transistor with an $R_{DS(on)}$ of 45mΩ the "on" and "off" switching losses E_{on} and E_{off} are calculated as a function of hard-commutated current for several different package source inductance values. The main contribution to these losses is caused by the current/voltage overlap in the power transistor during the switching transients. The dissipated energy always increases with the switched current and E_{on} dominates.

If the finite current slope due to the parasitic source inductance determines the duration of this transient, the losses over current increase more than linearly, as would approximately be the case with zero source inductance. The di/dt limit is approximately: $di/dt<(U_g-V_{th})/L_S$ (does not depend on R_g).

From Fig. 5, the Kelvin connection method reduces the turn on switching losses at 30A, a typical maximum current in a PFC application, to 70µJ; i.e. by a factor of 2 and 4 compared with a source inductance of 2.5 and 5nH, respectively. The reduction of switching losses can also be seen in Fig. 6 however at much lower absolute energy values. The current level where the source inductance is starting to take an important role is seen in the range of 15A for the 45mΩ CoolMOS™ C7 transistor.

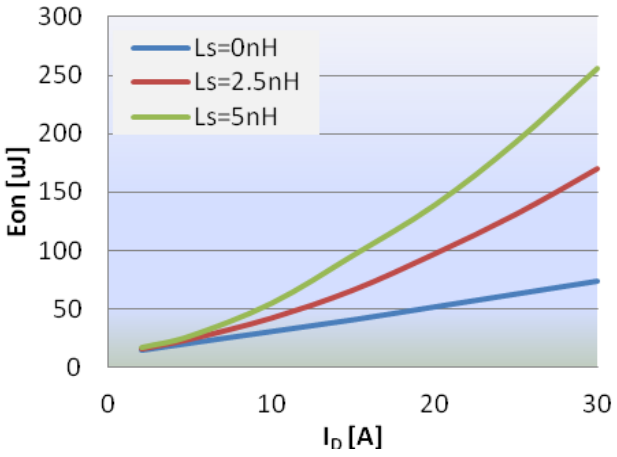


Fig. 5 Simulated turn on (E_{on}) switching energy versus switched current for different values of the parasitic source inductance

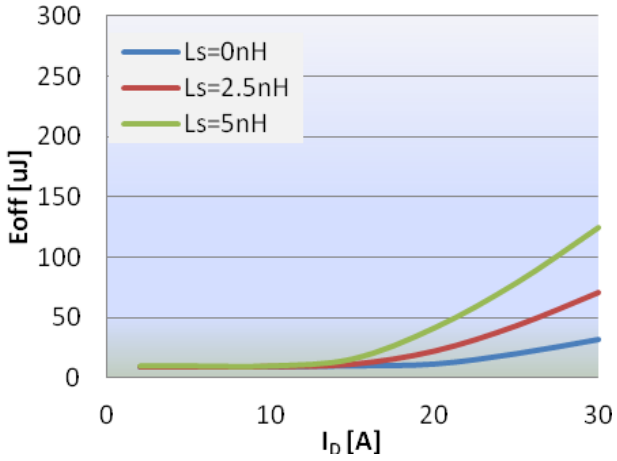


Fig. 6 Simulated turn off (E_{off}) switching energy versus switched current for different values of the parasitic source inductance

5 Measurement results

To verify the validity of the concept and the simulation results, a classical 1200W PFC stage according to Fig. 3 has been realized utilizing a 45mΩ CoolMOS™ C7 switch in both TO-247 packages together with a 12A SiC diode. Measurement results of the switching energy are given in Fig. 7. Here E_{on} has been measured in 3 and 4pin configuration for different values of parasitic source inductance, defined by the pin length between package and PCB (0 and 5mm, resp.). The measured values coincide quite well with the simulation, if we assume an effective source inductance of about 2 and 4nH, respectively. It should be pointed out, that in the 4pin configuration the results are identical, regardless of package pin length.

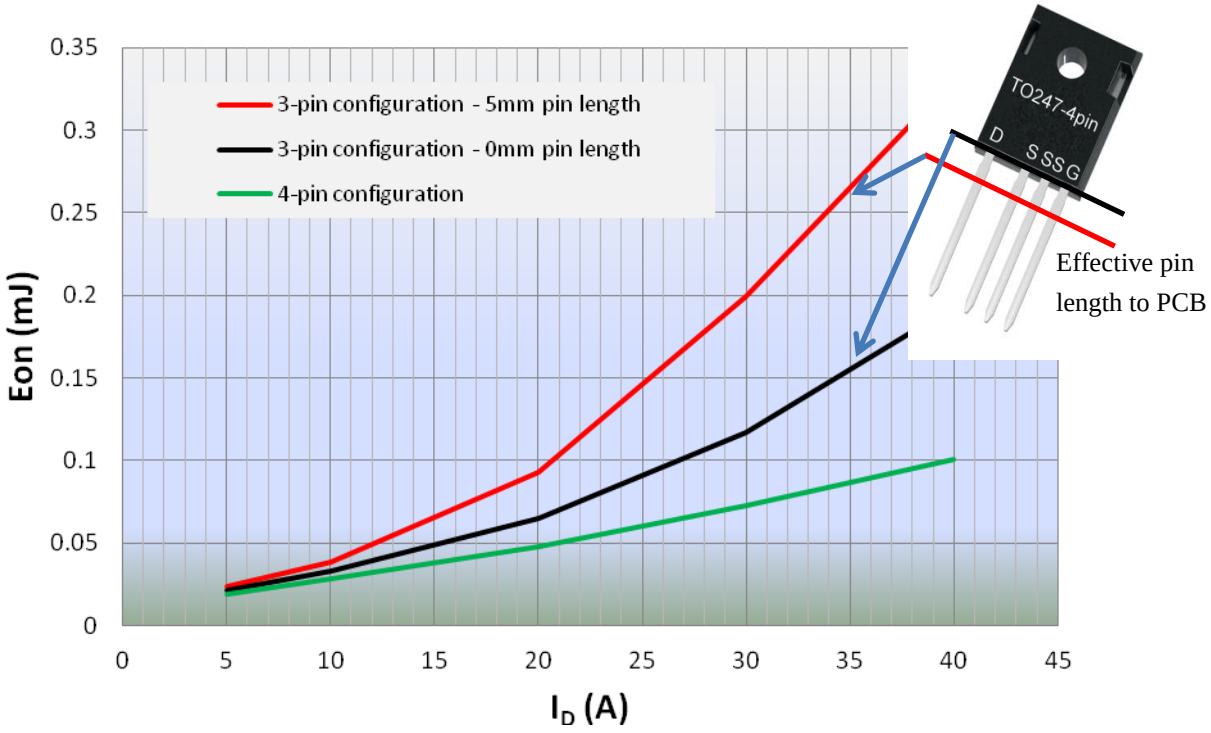


Fig. 7 Measured turn on switching energies versus switched current for different configurations

The difference with the 3pin configuration seen here in the Fig. 7 is caused by the inductance of the bond wire inside the package itself, which can only be excluded from the drain current path by the 4pin package, since this package has its separate wire for the source sense inside the package.

This is further illustrated by the voltage and current waveforms depicted in Fig. 8 and Fig. 9. With 5mm pin length a significant prolongation of the switching transient takes place for the standard configuration (Fig. 9) due to the reduced current slope.

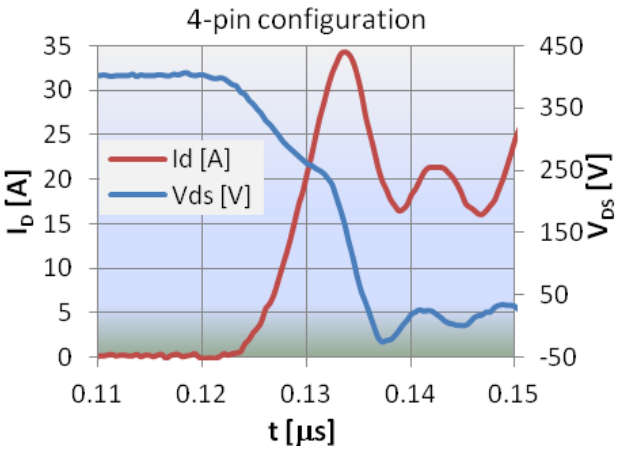


Fig. 8 Voltage and current waveforms at I_D=20A and R_G=10Ω with Kelvin source connection configuration (5mm pin length)

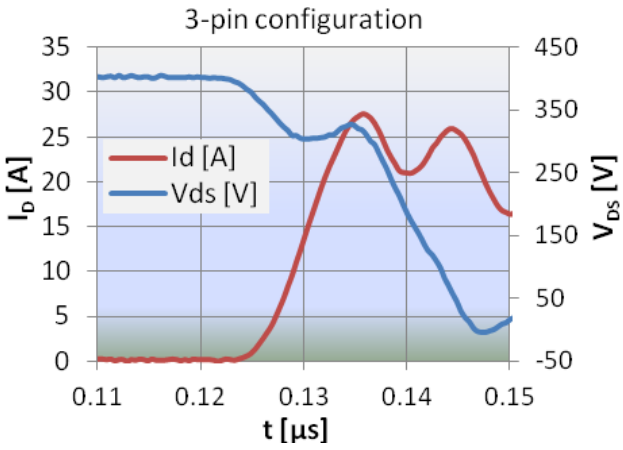


Fig. 9 Voltage and current waveforms at I_D=20A and R_G=10Ω without Kelvin source connection configuration (5mm pin length)

Finally the overall efficiency of the PFC has been measured. From the results in Fig. 10 we can conclude, that the switching loss reduction enabled by the source sense concept results in a remarkable performance improvement. As expected, the efficiency benefits increase for higher currents (i.e power ratings).

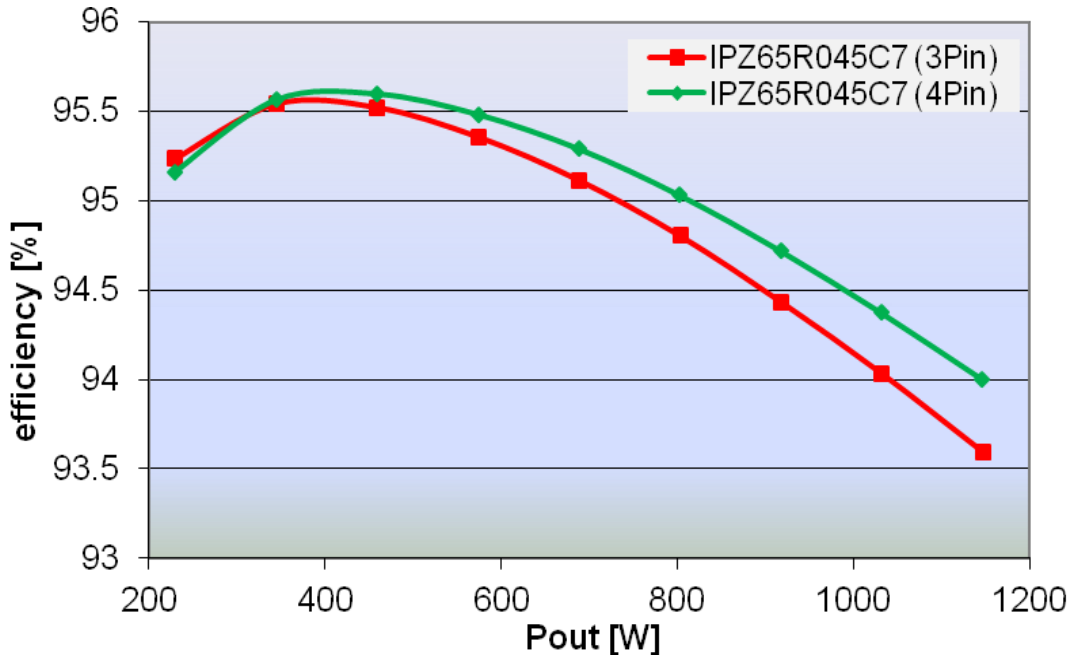


Fig. 10 PFC efficiency comparison between 3pin and 4pin configuration for 90Vac (PFC CCM, RG=10Ω, IDH16G65C5 @100kHz; 5mm pin length)

6 Conclusion

The impact of the parasitic source inductance on efficiency was discussed in this application note, and it was shown that for high power applications with requirements for high efficiency, the new 4pin package is needed. This was shown in theory, by simulation and by physical measurement in a reference PFC testing platform.

7 References

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[3] Y. Xiao, H. Shah, T. P. Chow and R. J. Gutmann, “Analytical Modeling and Experimantal Verification of Interconnect Parasitic Inductance on MOSFET Switching Characteristics”, APEC 2004, Dig. Tech. Papers