

900 V CoolMOS™ C3 MOSFET

New 900 V class for superjunction devices and a new horizon for SMPS and renewable energy applications

About this document

Scope and purpose

This document explains the design principles, characteristics, and application benefits of Infineon's CoolMOS™ 900 V superjunction MOSFET technology. It provides guidance for achieving high efficiency and reliability in power conversion systems across various topologies and voltage ranges.

Intended audience

The intended audiences for this document are power electronics engineers, circuit designers, and technical professionals working on SMPS, renewable energy systems, and high-voltage applications.

Keypoints

- Introduces Infineon's CoolMOS™ 900 V superjunction MOSFET technology, designed for high-efficiency power conversion
- Explains the superjunction principle, overcoming the "silicon limit" for reduced on-resistance and improved switching performance
- Highlights device characteristics: ultra-low conduction and switching losses, low gate charge, and best-in-class figure-of-merit. Also, details target applications: SMPS, ATX power supplies, LCD TV flyback converters, renewable energy (solar), lighting, and auxiliary power supplies in 3-phase systems
- Provides circuit design recommendations for layout, dv/dt control, and minimizing parasitic capacitance
- Includes comparative performance data and product portfolio overview

About this product family

Product family

Infineon's CoolMOS™ is a high-voltage N-channel silicon power MOSFET that is designed to provide excellent thermal performance, lowest switching and conduction power losses, and optimal $R_{DS(on)}$ for increased system efficiency, supporting a range of application from low power levels to high power levels.

Target applications

- [Consumer electronics](#)
- [Industrial applications](#)
- [Home appliances](#)
- [Server](#)
- [Telecom](#)
- [Renewables](#)

900 V CoolMOS™ C3 MOSFET

New 900 V class for superjunction devices and a new horizon for SMPS and renewable energy applications

Table of contents

Table of contents

About this document.....	1
About this product family	1
Table of contents	2
1 Introduction	3
1.1 The superjunction principle.....	4
2 Device characteristics	6
3 Target applications CoolMOS™ 900 V	9
3.1 Wide range designs (90...270 Vac) with their typical 400 V _{DC} bulk voltage	9
3.2 Replacement of IGBTs by CoolMOS™ 900 V Series	12
3.3 Lighting applications.....	13
3.4 Auxiliary power supplies in 3-phase systems.....	13
4 Product portfolio	14
5 Circuit design and layout recommendations	15
5.1 Control dv/dt and di/dt by proper selection of gate resistor.....	15
5.2 Minimize parasitic gate-drain board capacitance	15
5.3 Locate gate drivers and gate turn-off components as close as possible to the gate	17
5.4 Use symmetrical layout for paralleling MOSFETs, and good Isolation of gate drive between FETs..	17
5.5 Summary	17
6 Related resources	18
References.....	19
Revision history.....	20
Disclaimer.....	21

900 V CoolMOS™ C3 MOSFET

New 900 V class for superjunction devices and a new horizon for SMPS and renewable energy applications

Introduction

1 Introduction

Infineon introduces a new 900 V voltage class of energy-saving CoolMOS™ power MOSFETs for high efficiency switch-mode power supply and renewable energy applications.

CoolMOS™ 900 V offers extremely low static and dynamic losses, which is the signature of super junction MOSFET technology where the “silicon limit” is overcome. The square-law dependency between on-resistance and blocking voltage in conventional MOSFETs is amended by new CoolMOS™ 900 V, resulting in an industry-best on-state resistance per package type being four times or even lower if compared to conventional 900 V MOSFETs: 0.12 Ohm in TO247, 0.34 Ohm in TO220, and 1.2 Ohm in DPAK packages. A figure-of-merit (FOM) on-resistance times gate charge ($R_{DS(on)} \cdot Q_g$) as low as $34 \Omega \cdot nC$ is reached, which translates into extremely low conduction, driving and switching losses.

Samples are available now and the complete product spectrum will be filled up during 2008.

Target applications for CoolMOS™ 900 V are ATX power supplies, solar converters, Quasi-Resonant Flyback designs for LCD TV, active frontend 3-phase-systems and other designs, where high blocking voltage, low conduction and switching losses combined with low gate charge are necessary.

Table 1 gives a quick overview of available CoolMOS™ series today.

Table 1 CoolMOS™ series at a glance

	Market entry	Voltage class [V]	Special characteristic	V _{gs,th} [V]	G _{fs} [S]	Internal R _g [Ω]
CoolMOS™ S5	1998	600	Low $R_{DS(on)}$, Switching speed close to standard MOSFETs	4.5	Low	High
CoolMOS™ C3	2001	500/600/	Fast switching speed	3	High	Low
–	–	650/800	symmetrical rise/fall time at V _{GS} =10 V	–	–	–
CoolMOS™ CFD	2004	600	Fast body diode, $Q_{rr} 1/10^{th}$ of C3 series	4	High	Low
CoolMOS™ CP	2005	500/600	Ultra-low $R_{DS(on)}$, ultra-low Q_g , very fast switching speed	3	High	Low
CoolMOS™ C3	2008	900	low $R_{DS(on)}$, low Q_g , fast switching speed	3	High	Low

900 V CoolMOS™ C3 MOSFET

New 900 V class for superjunction devices and a new horizon for SMPS and renewable energy applications

Introduction

1.1 The superjunction principle

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs and designed according to the superjunction (SJ) principle [1], which in turn is based on the RESURF [2] ideas being successfully used for decades in lateral power MOSFETs. Conventional power MOSFETs suffer from the limitation of the so-called “silicon limit” [3], which means that doubling the voltage blocking capability typically leads to an increase in the on-state resistance by a factor of five. The “silicon limit” is shown in Figure 1, where the area-specific on-state resistance of state-of-the-art standard MOSFETs are indicated. SJ technology may lower the on-state resistance of a power MOSFET virtually towards zero. The basic idea is to allow the current to flow from top to bottom of the MOSFET in a very high doped vertically arranged regions. In other words, a lot more charge is available for current conduction compared to a standard MOSFET structure. In the blocking state of the SJ MOSFET, the charge is counterbalanced by exactly the same amount of charge of the opposite type. The two charges are separated locally in the device by a very refined technology, and the resulting structure shows a laterally stacked fine-pitched pattern of alternately arranged p- and n-areas, see Figure 2. The finer the pitch can be made, the lower the on-state resistance of the device will be.

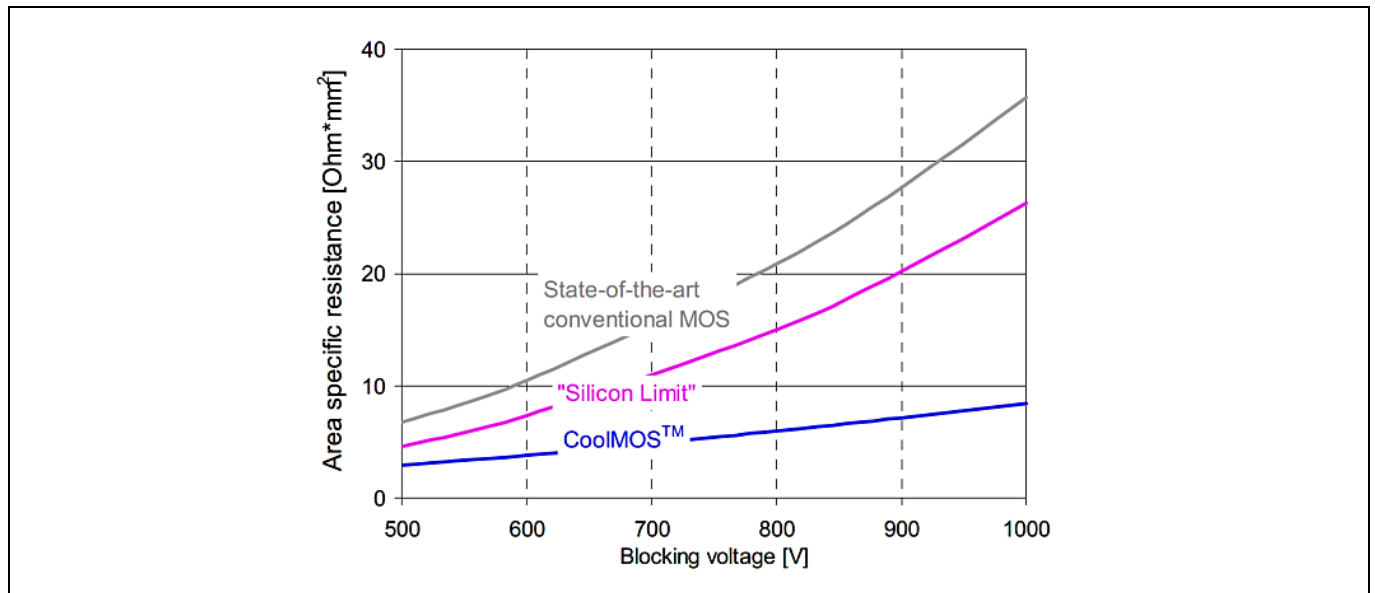


Figure 1 Area-specific on-resistance vs. breakdown voltage comparison of standard MOSFET and CoolMOS™ technology

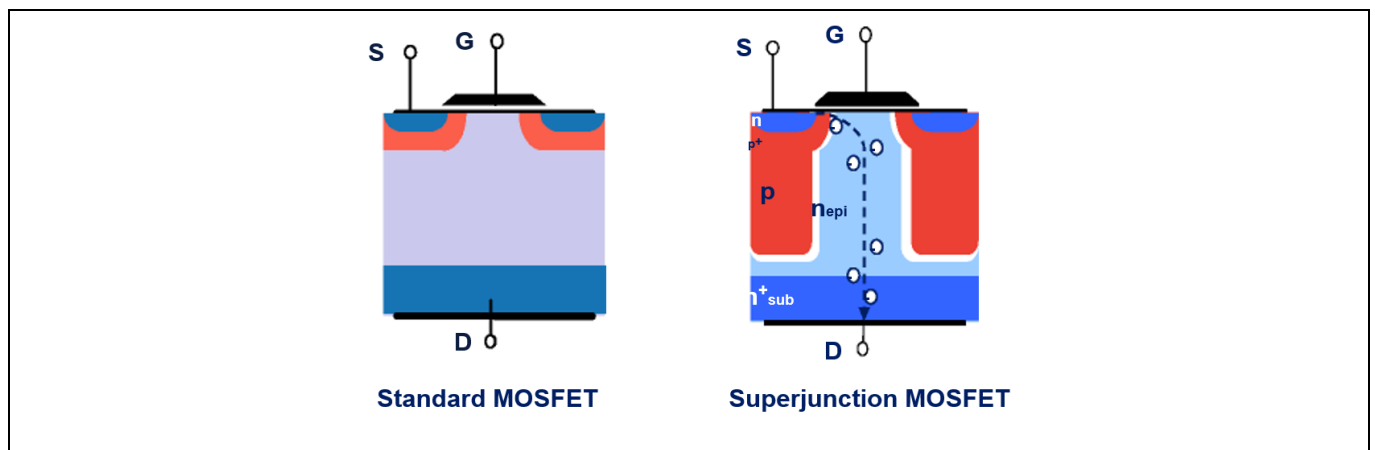


Figure 2 Schematic cross-section of a standard power MOSFET vs. a superjunction MOSFET

900 V CoolMOS™ C3 MOSFET

New 900 V class for superjunction devices and a new horizon for SMPS and renewable energy applications



Introduction

Another signature of SJ technology is the extremely fast switching speed. The turn off behavior of an SJ MOSFET is not characterized by the relatively slow voltage driven vertical expansion of the space charge layer, but by a sudden nearly intrinsic depletion of the laterally stacked p-n structure. This unique behavior makes the device very fast. The neutralization of these depletion layers is done via the MOS controlled turn-on of the load current for the n-areas and via a voltage driven drift current for the p-areas. SJ devices therefore reach theoretical rise and fall times in the range of a few nanoseconds.

Figure 3 shows a comparison of $R_{DS(on),max}$ between today's most advanced available MOSFETs.

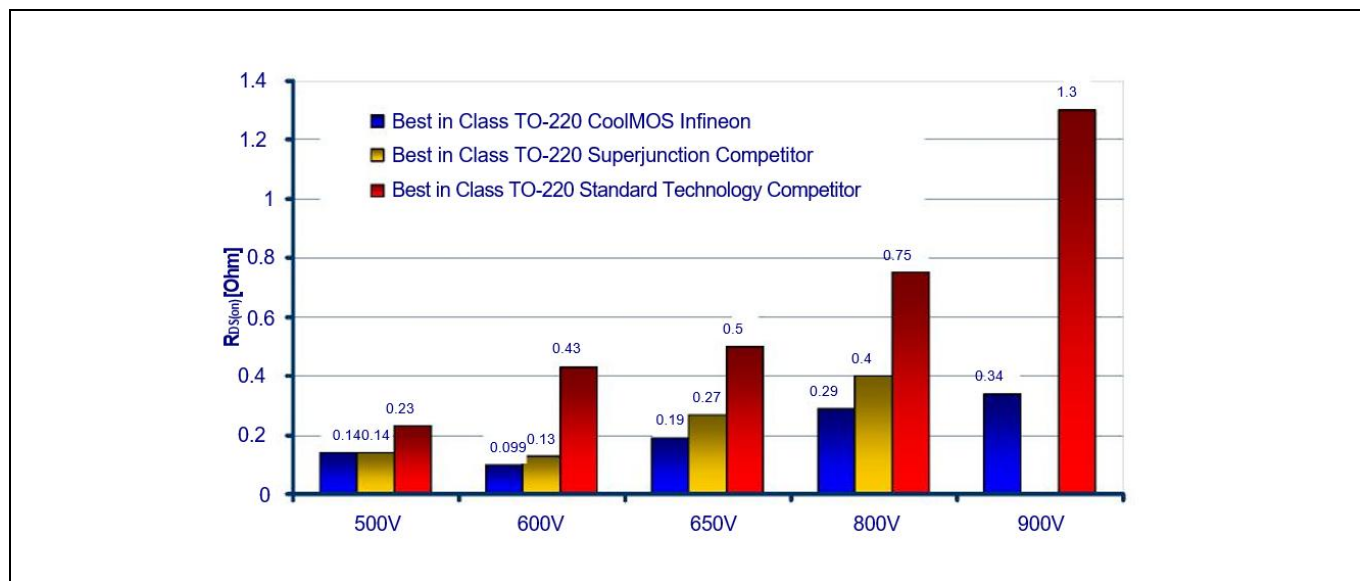


Figure 3 Comparison of $R_{DS(on),max}$ for most advanced MOSFETs in TO220 package available in the market

900 V CoolMOS™ C3 MOSFET

New 900 V class for superjunction devices and a new horizon for SMPS and renewable energy applications

Device characteristics

2 Device characteristics

CoolMOS™ 900 V is the next step towards THE IDEAL HIGH VOLTAGE SWITCH with key features:

- Very low conduction and switching losses
- Lowest on-state-resistance per package at 900 V blocking capability
- Ultra-low gate charge and lowest figure-of-merit $R_{DS(on)} \times Q_g$

Which gives the application benefits:

- Extremely reduced heat generation
- Reduced system size and weight
- Very low gate drive power facilitating the use of low-cost ICs and gate drivers
- Reduced overall system cost

The most interesting circuit design aspect is that the more-than-square-law dependency of the area-specific on-resistance ($R_{DS(on)} \times A$) on the breakdown voltage in case of standard MOSFETs has been amended and a close to linear proportionality has been achieved:

$$R_{DS(on)} \cdot A \propto (V_{Br})^n \quad n = \begin{cases} 2,4...2,6 & \text{Standard MOS} \\ 1,3 & \text{Cool MOS}^{\text{TM}} \end{cases}$$

It follows from this that the on-state losses P_{stat} present in the switch when transferring a particular power are:

$$P_{stat} \propto I_{sw,eff}^2 \cdot R_{DS(on)} \propto P_{out}^2 \cdot V_{Br}^{n-2}$$

Therefore, while losses increase with the operating voltage when using a standard MOSFET (proportional to $V^{0,4...0,6}$), they are reduced using CoolMOS™ transistors, proportionally to $V^{-0,7}$.

CoolMOS™ 900 V series has the world's lowest area-specific $R_{DS(on)}$ for 900 V MOSFETs as shown [Figure 4](#), which results in lowest $R_{DS(on)}$ per package type. 120 mΩ in TO247 and 340 mΩ in TO220 result in low conduction losses and high current handling capability. Continuous drain currents up to 36 A and pulse currents up to 96 A are possible (CoolMOS™ 900 V 120 mΩ). A comparison of available $R_{DS(on)}$ -values in DPAK, TO220, and TO247 are given in [Figure 4](#).

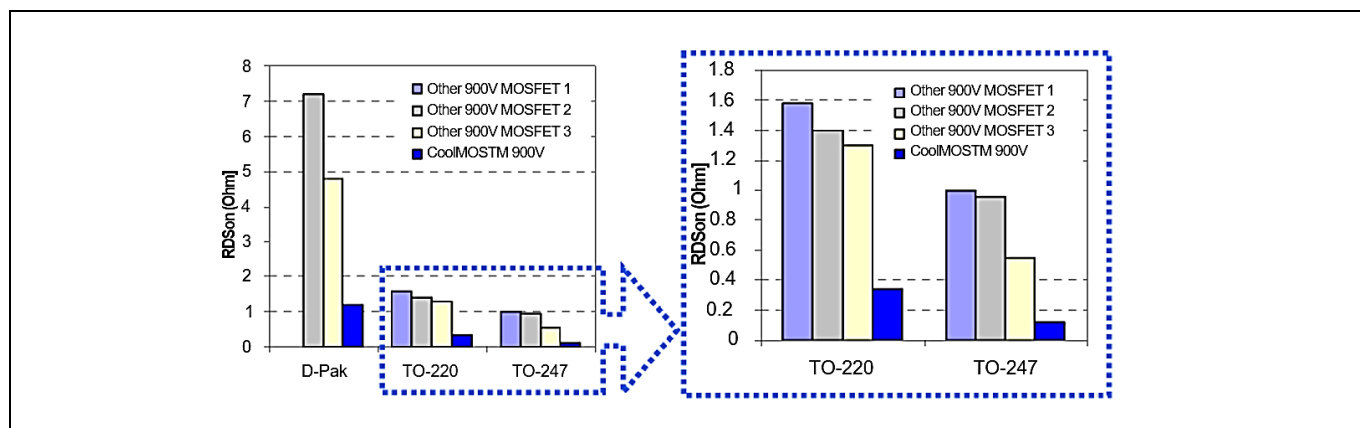


Figure 4 Comparison of $R_{DS(on),max}$ for best-in-class 900 V devices (right: zoom-in TO220/TO247)

900 V CoolMOS™ C3 MOSFET

New 900 V class for superjunction devices and a new horizon for SMPS and renewable energy applications

Device characteristics

The CoolMOS™ 900 V cuts down the achievable $R_{DS(on)}$ in both packages by nearly a factor of four. By introducing our new CoolMOS™ 900 V technology, we also establish a reduction of the total gate charge. The new technology reduces the total gate charge Q_g for similar $R_{DS(on)}$ types by 25% (Figure 5) and offers the lowest FOM ($R_{DS(on)} \times Q_g$) in this voltage class. The FOM, on the one hand, a measure of the conduction losses attributed to the switch, on the other hand, it correlates with Q_g , a parameter related to the energy the driver circuit must offer to turn the switch on and off. A very low FOM, therefore, indicates low conduction losses, easy driving, and low switching losses.

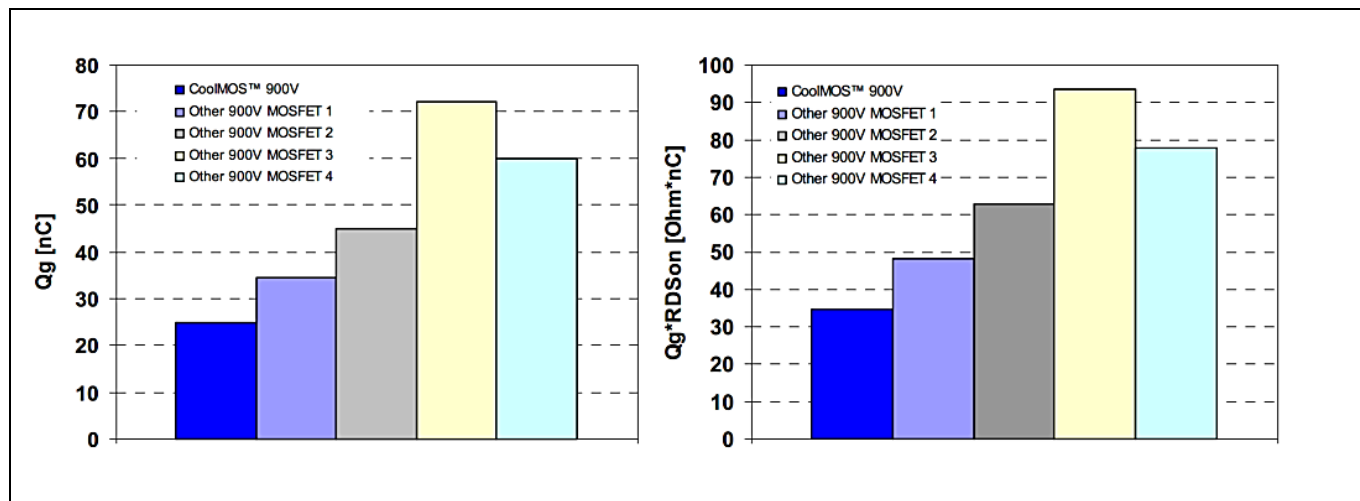


Figure 5 Gate charge Q_g and figure-of-merit ($R_{DS(on)} \times Q_g$) values for 900 V devices with nearly same $R_{DS(on)}$ of 1.3 Ω - 1.4 Ω

Not only has the new technology achieved breakthrough at reduced $R_{DS(on)}$ values, but new benchmarks have also been set for the device capacitances. A second effect to be considered in the switching losses is the energy being stored in the output capacitance. This energy E_{oss} (Figure 6) is transferred into heat during hard switched turn-on. Due to the strongly nonlinear voltage dependence of the output capacitance, the 900 V CoolMOS™ compensation devices offer a very good performance if switched to more than 150 V (marked in Figure 6).

Energy stored in the output capacitance of the MOSFETs is reduced by a factor of two or more at working voltage.

900 V CoolMOS™ C3 MOSFET

New 900 V class for superjunction devices and a new horizon for SMPS and renewable energy applications

Device characteristics

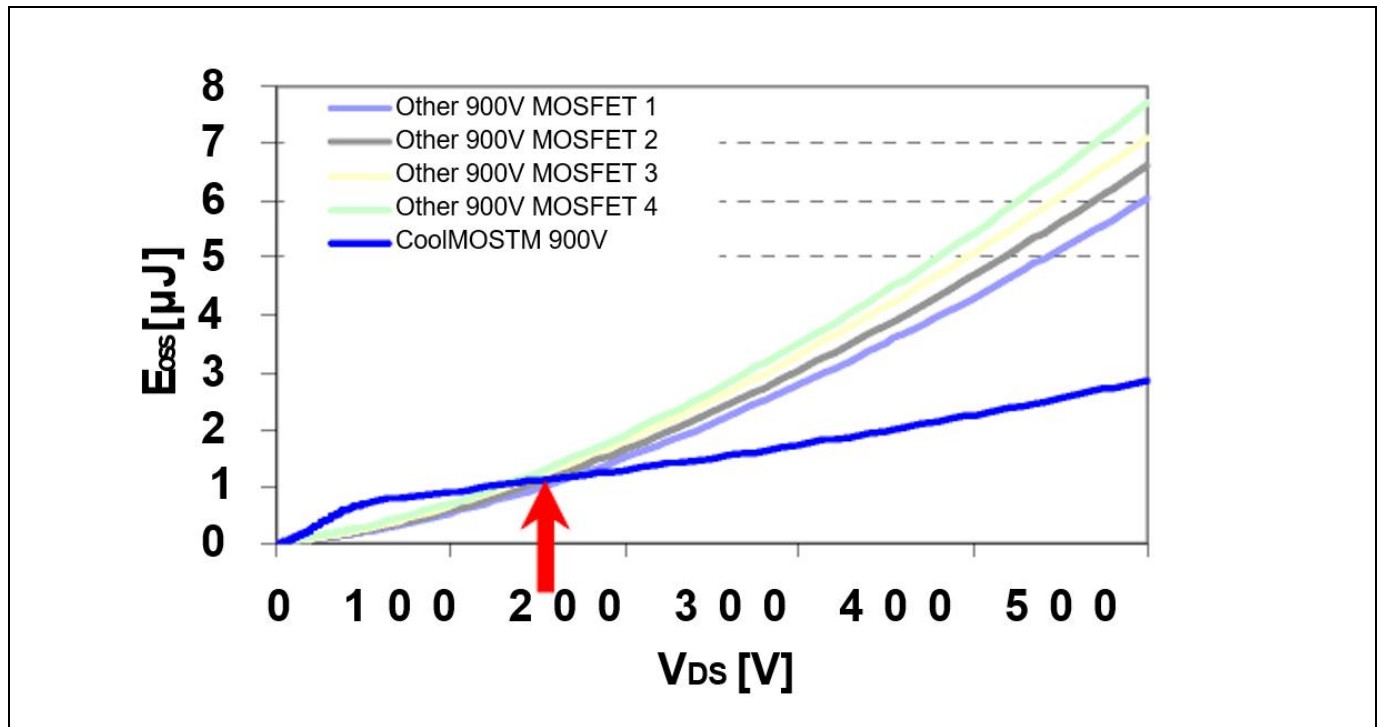


Figure 6 E_{oss} values for different 900 V MOSFETs

900 V CoolMOS™ C3 MOSFET

New 900 V class for superjunction devices and a new horizon for SMPS and renewable energy applications

Target applications CoolMOS™ 900 V

3 Target applications CoolMOS™ 900 V

The new CoolMOS™ 900 V series offer more design flexibility and pushes the existing limits towards higher power without significant disadvantages. Designers of power units benefit from the high blocking voltage, low $R_{DS(on)}$, and low Gate charge of the new CoolMOS™ 900 V. Some examples are explained in the following paragraphs.

3.1 Wide range designs (90...270 Vac) with their typical 400 V_{dc} bulk voltage

Designs for standard grid voltages can benefit from higher blocking voltage. Depending on the application, the efficiency can be increased and/or design can be simplified without additional costs or other disadvantages.

Example 1: 500 W Single Transistor Forward (STF) Converter used in ATX power supplies

Major benefits with CoolMOS™ 900 V:

- 500 W output power achievable with STF
- Compared to TTF:
 - Higher efficiency (+0.7% with BiC TO220)
 - Lower cost and part count
 - Easier design (no high side control)

The output power benchmark for STF converters can be increased by using CoolMOS™ 900 V. Up to 500 W is achievable with a single MOSFET with increased performance and lower costs compared to standard Two-Transistor-Forward (TTF) with 200 mΩ 500 V/600 V MOSFETs. Figure 7 shows the schematics of both topologies. In the STF we have only one transistor compared to the two transistors and the pulse transformer in a TTF.

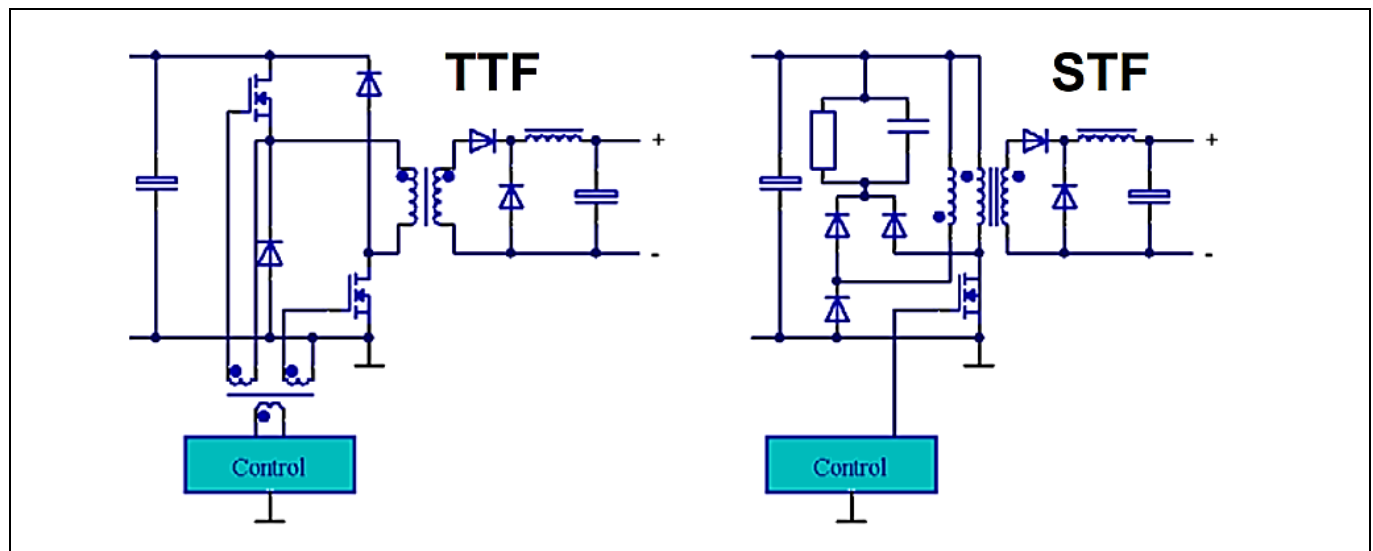


Figure 7 ATX power supplies (secondary side schematic being simplified)

Changing the topology from TTF to STF not only simplifies the design and adds layout benefits but also avoids the disadvantages (like the need for high-side-switching) of TTF.

Table 2 shows a comparison of the primary side losses of TTF and STF. The working frequency is 100 kHz.

900 V CoolMOS™ C3 MOSFET

New 900 V class for superjunction devices and a new horizon for SMPS and renewable energy applications

Target applications CoolMOS™ 900 V

Table 2 Losses comparison: Two-Transistor-Forward Converter vs. Single-Transistor-Forward Converter

Losses	TTF with 200 mΩ/600 V	STF with 500 mΩ/900 V	STF with 340 mΩ/900 V
Conduction	6.5 W	8.1 W	5.5 W
Output capacitance	2.8 W	1.0 W	2.1 W
Switching	7.3 W	4.7 W	4.7 W
Demagnetizing winding	–	0.5 W	0.5 W
Total losses	16.6 W	14.3 W	12.8 W

Despite the higher $R_{DS(on)}$ of the CoolMOS™ 900 V, it is possible to design a STF with a higher efficiency than a TTF with 200 mΩ 600 V MOSFETs. This is due to the higher dynamic losses in TTF, because, in every cycle, two transistors must be switched compared to only one transistor in STF.

Indeed, the transformer in STF needs an additional demagnetizing winding which causes a small amount of losses which do not exist in TTF topology. But with careful design (bifilar winding), these losses can be very low and do not influence the result significantly.

Cost optimized designs use the 500 mΩ CoolMOS™ 900 V with slightly increased efficiency (compared to TTF with 200 mΩ MOSFETs) and reducing losses up to 0.7% is possible by using the 340 mΩ CoolMOS™ 900 V.

Example 2: 200W Quasi-Resonant Flyback converters for LCD-TV

Major benefits with CoolMOS™ 900 V:

- More than 200 W of output power achievable with Quasi-Resonant Flyback
- Improved EMI behavior due to true zero-voltage switching
- Higher efficiency (+0.7% compared to 600 V or 650 V parts, 0.2% compared to 800 V parts)
- Lower voltage stress on secondary diodes or synchronous rectifiers

Modern LCD-TV requires output power up to 200 W with high efficiency of the power supply together with low costs. The best topology for these requirements is the Quasi-Resonant Flyback Converter (QR-FB) and its disadvantages (like the high peak voltage on primary switch) are easy to handle with CoolMOS™ 900 V.

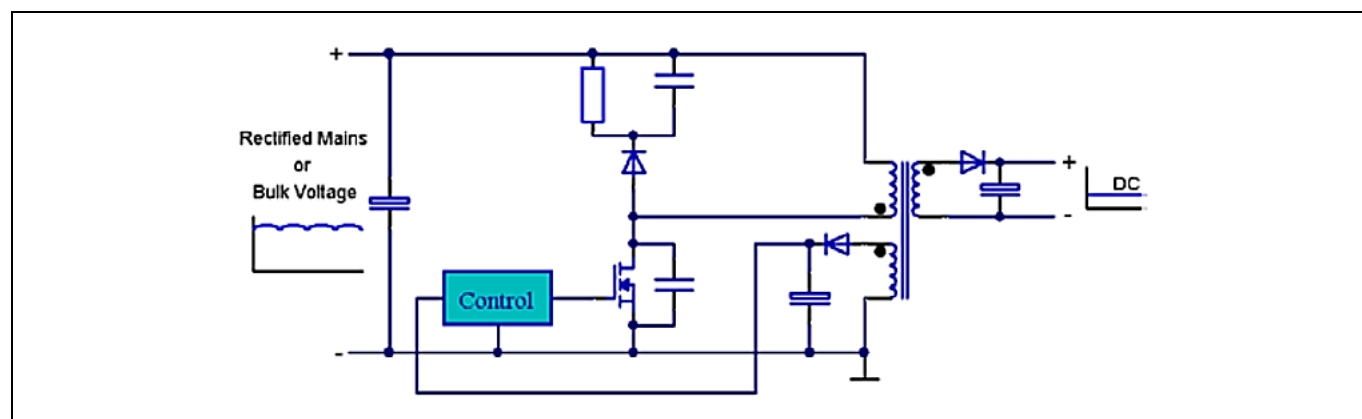


Figure 8 Quasi-Resonant Flyback Converter for LCD-TV (schematic simplified on secondary)

MOSFETs with high blocking voltage allow optimized transformer design resulting in reduced semiconductor losses and reduced voltage stress on secondary diode or synchronous rectifier.

900 V CoolMOS™ C3 MOSFET

New 900 V class for superjunction devices and a new horizon for SMPS and renewable energy applications

Target applications CoolMOS™ 900 V

Efficiency improvement of 0.2% compared to available 800 V parts and even 0.7% compared to the standard 650 V parts is possible using CoolMOS™ 900V.

Table 3 shows the results of a 200 W/24 V Quasi-Resonant Flyback design realized with 650 V, 800 V, and 900 V MOSFETs, respectively, at a switching frequency of 100 kHz.

Table 3 200 W/24 V Quasi-Resonant Flyback with different types of MOSFETs

	650 V 500 mC CoolMOS™	800 V 500 mC CoolMOS™	900 V 500 mC CoolMOS™	Benefit by using CoolMOS™ 900 V
Duty Cycle at $V_{in,min}$ and max load	18%	27%	32%	Longer DC due to higher reflected voltage
Peak current	4.8 A	3.1 A	2.7 A	Reduced peak current
Conduction losses	1.35 W	0.90 W	0.76 W	Reduced conduction loss
Turn-on-losses	0.17 W	0.09 W	0	True zero-voltage switching. Improved EMI behavior
Turn-off-losses	1.4 W	0.9 W	0.8 W	Reduced turn-off loss due to lower peak current
Voltage stress on secondary side diode	91 V	57 V	48 V	Reduced voltage stress on sec. side diode or sync.rec MOSFET
Total losses	6.6 W	5.6 W	5.2 W	
Efficiency loss	3.31%	2.80%	2.61%	Significant loss reduction. 0.7% vs. 650 V 0.2% vs. 800 V

900 V CoolMOS™ C3 MOSFET

New 900 V class for superjunction devices and a new horizon for SMPS and renewable energy applications

Target applications CoolMOS™ 900 V

3.2 Replacement of IGBTs by CoolMOS™ 900 V Series

Using a MOSFET with its Ohmic forward characteristic, allows a significant reduction of conduction losses below the power dissipation of IGBTs, where conduction losses cannot fall below the on-set voltage times load current.

PFC and PWM stages are possible to up to 750 V bulk voltage using CoolMOS™ 900 V without diminishing safety margin.

Example 3: Renewable energy applications/solar converters

Major benefits with CoolMOS™ 900 V:

- More panels in series possible - lower copper losses in wiring
- Higher overall efficiency
- No Overvoltage Protection (OVP) necessary
- Smaller magnetic components due to higher switching frequency

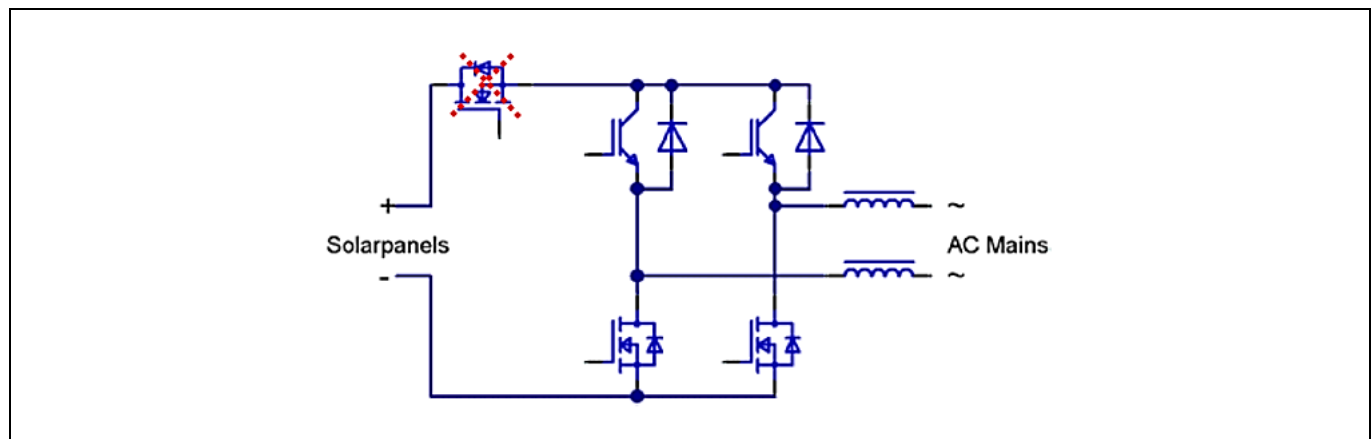


Figure 9 Typical DC/AC solar converter (with overvoltage protection)

Renewable energy applications such as photovoltaic converters show very high efficiency requirements due to system amortization via payback of electricity fed back into the public network.

The use of MOSFETs instead of IGBTs enhances the efficiency especially in the mid-range of output power - as being characteristic especially for many days in central and northern Europe – by avoiding the characteristic onset voltage of the IGBT. The clear disadvantage of the MOSFET, its limited blocking voltage range and its more-than-square-law between $R_{DS(on)}$ and BV_{DSS} is amended by the new MOS generation CoolMOS™ 900 V. This new product family allows to build converters with an enlarged input voltage range coming, thus, closer to the upper limit of 1000 V as defined by the IEC 60364 for solar modules. Putting more panels in series instead of paralleling significantly reduces cabling losses, efforts, and costs. The cabling losses alone can be cut by a factor of 2 when changing from 600 V to 900 V voltage class.

Another factor in photovoltaic systems is the size and cost of magnetic components. Offering a device with improved $R_{DS(on)} \times Q_g$ and $R_{DS(on)} \times E_{oss}$ performance allows an increase of switching frequency without suffering from the penalty of increased losses. Therefore, reduction of system size is possible without losing energy efficiency.

3.3 Lighting applications

Using SEPIC topology as PFC converter eliminates high inrush current and improve surge current capability. With CoolMOS™ 900 V, the necessary higher blocking voltage compared to standard PFC boost topology can be handled.

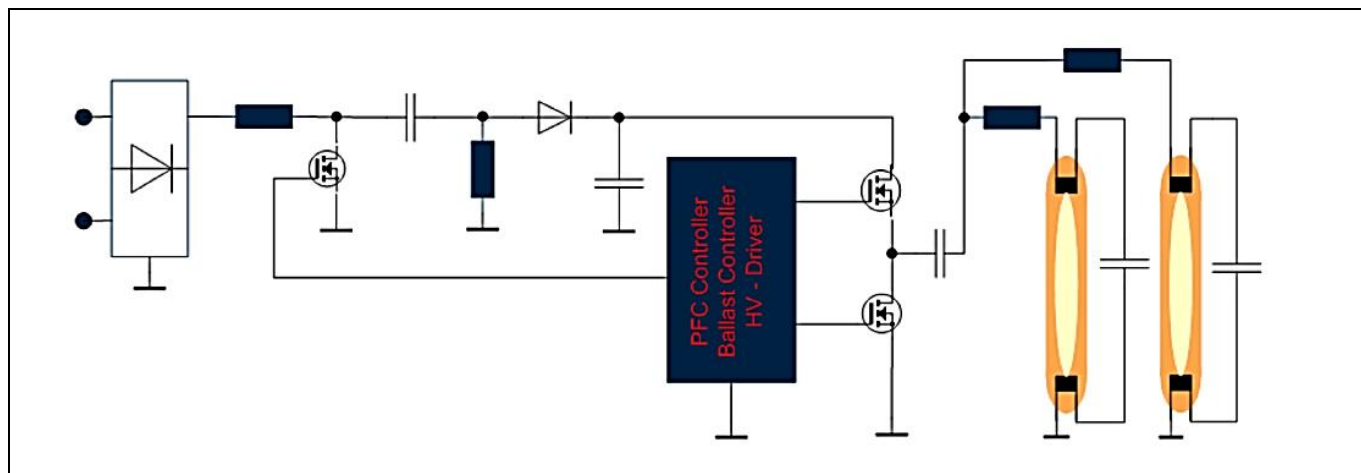


Figure 10 Lamp ballast with SEPIC preconverter

Additionally, the 3-phase-supply of Lamp ballasts for street lighting and greenhouses requires a higher voltage capability than is offered with 600 V or 800 V MOSFETs, and lower on-resistance than what is offered with conventional 900 V MOSFETs.

Ballasts for Flat Fluorescent Lamps require switches with higher voltage capability due to the favored single-switch resonant topology.

3.4 Auxiliary power supplies in 3-phase systems

Using a 3-phase grid, the blocking voltage of the MOSFETs in auxiliary power supplies needs to be higher than 800 V. With CoolMOS™ 900 V Flyback converters for higher output power levels are easy to design, thanks to low conduction, switching, and driving losses.

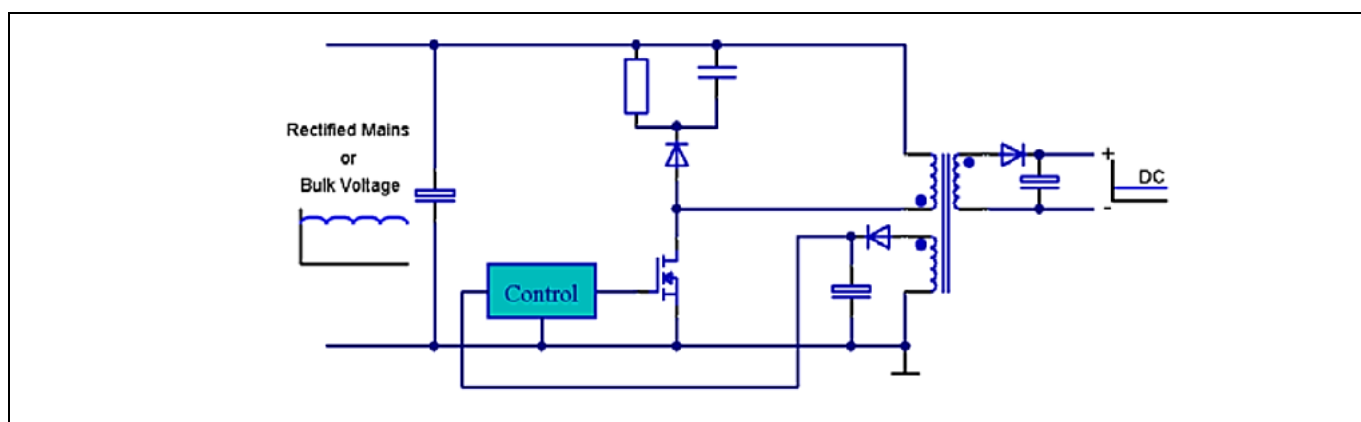


Figure 11 Flyback Converter for auxiliary power supplies

900 V CoolMOS™ C3 MOSFET

New 900 V class for superjunction devices and a new horizon for SMPS and renewable energy applications

Product portfolio

4 Product portfolio

CoolMOS™ 900 V portfolio is shown in Figure 12.

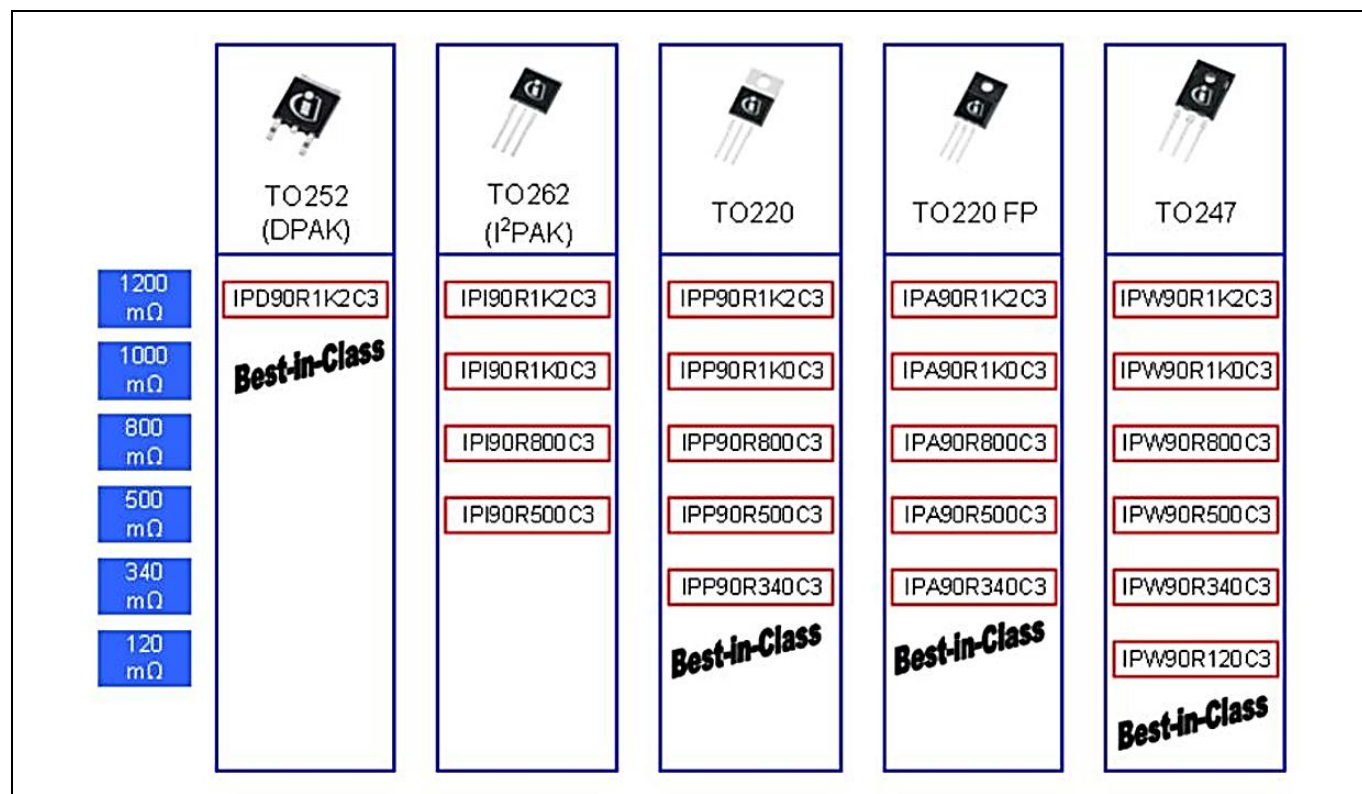


Figure 12 CoolMOS™ 900 V Products

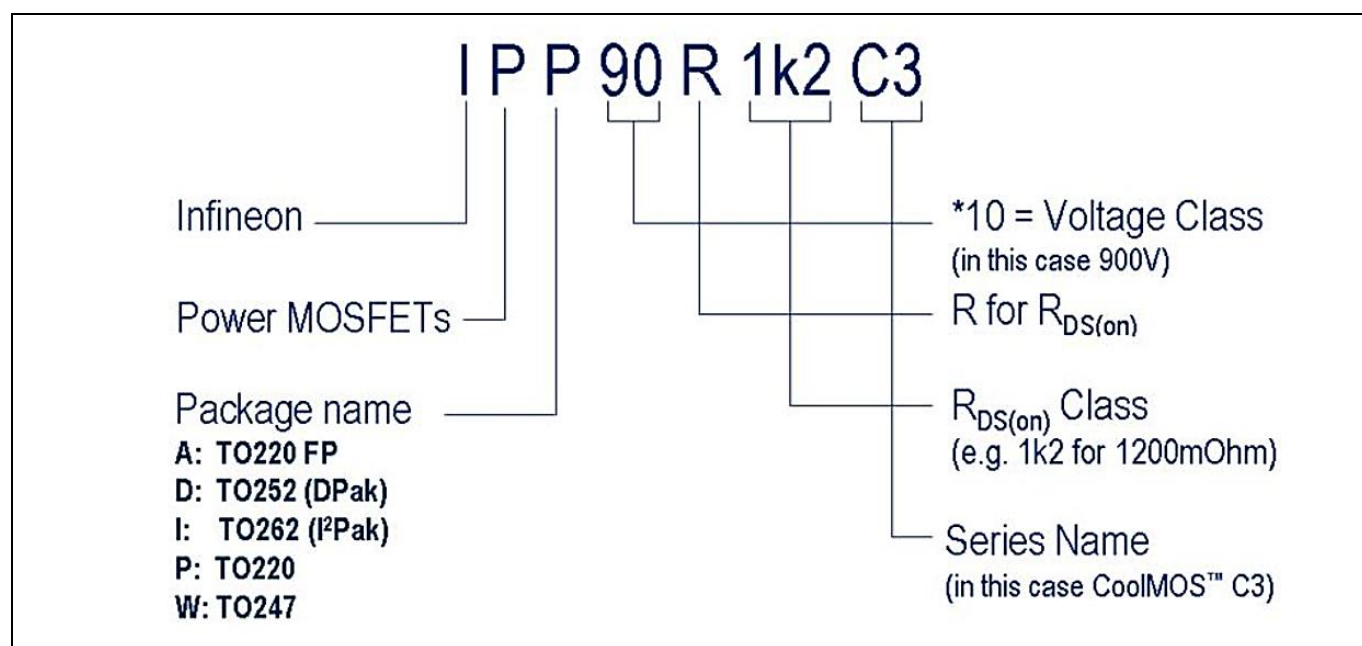


Figure 13 Naming system for CoolMOS™ Products

5 Circuit design and layout recommendations

There are a number of recommendations to make with respect to circuit design and layout practices which will ensure a combination of high performance and reliability. They can be recommended as if “in order of importance”, but realistically all are important, both in contribution towards circuit stability, reliability as well as the overall efficiency and performance. They are not very different from the recommendations made for introducing MOSFETs compared to bipolar transistors, or CoolMOS™ compared to standard MOSFETs; it is simply a matter of the degree of care required.

5.1 Control dv/dt and di/dt by proper selection of gate resistor

In order to exert full R_g control on the device maximum turn-off dv/dt we recommend the following procedure:

1. Check for highest peak current in the application
2. Choose R_g accordingly, not to exceed 50 V/ns (maximum rating in datasheet)
3. At normal operation condition, quasi ZVS condition can be expected which gives best efficiency results

5.2 Minimize parasitic gate-drain board capacitance

Particularly, care must be spent on the coupling capacitances between gate and drain traces on the PCB. As fast switching MOSFETs are capable to reach extremely high dv/dt values, any coupling of the voltage rise at the drain into the gate circuit may disturb proper device control via the gate electrode. As the CoolMOS™ series reaches extremely low values of the internal C_{gd} capacitance (C_{rss}) in the datasheet), we recommend keeping layout coupling capacitances below the internal capacitance of the device to exert full device control via the gate circuit. [Figure 14](#) shows a good example, where the gate and drain traces are either perpendicular to each other or go into different directions with virtually no overlap or paralleling to each other. A “bad” layout example is shown as reference to the good layout in [Figure 15](#).

If possible, use source foils or ground-plane to shield the gate from the drain connection.

900 V CoolMOS™ C3 MOSFET

New 900 V class for superjunction devices and a new horizon for SMPS and renewable energy applications

Circuit design and layout recommendations

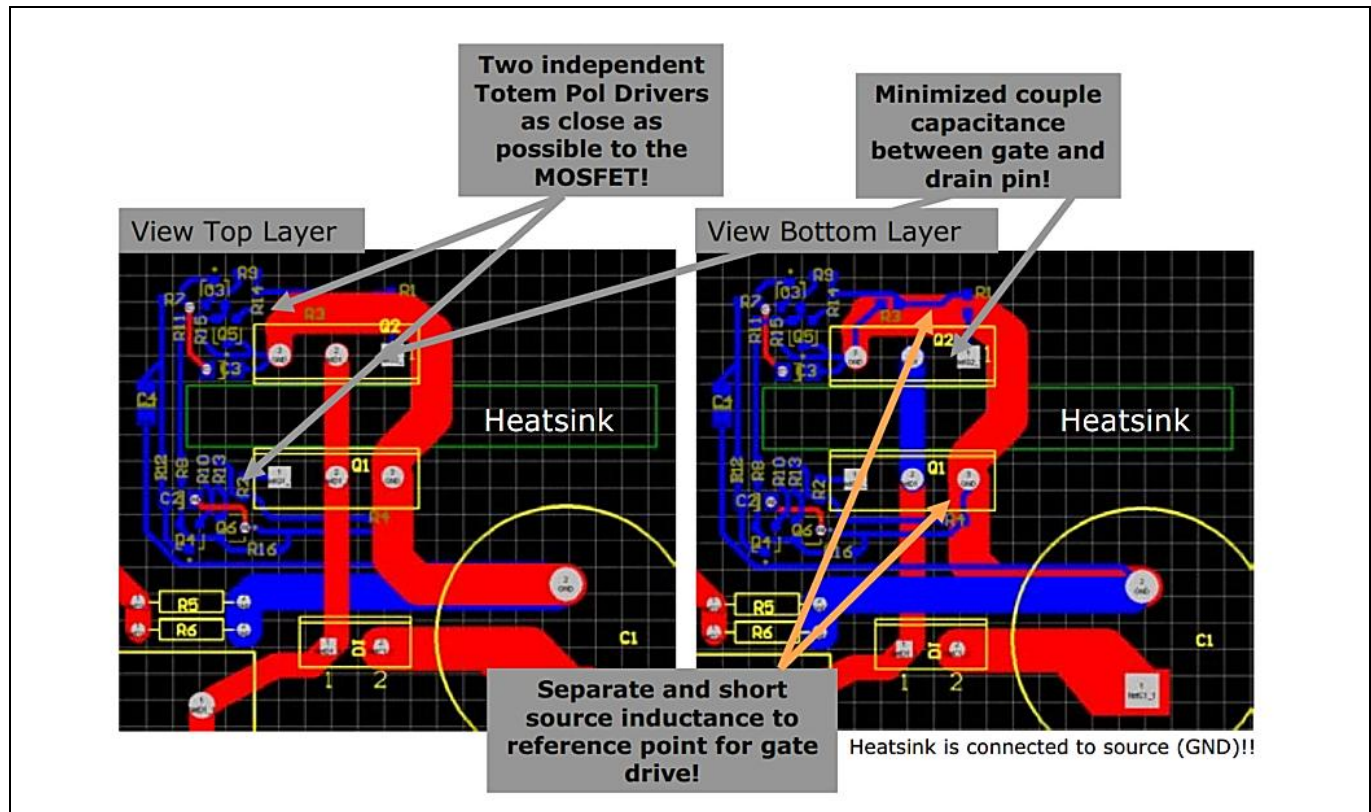


Figure 14 Good layout example ensuring clean waveforms when designing in CoolMOS™

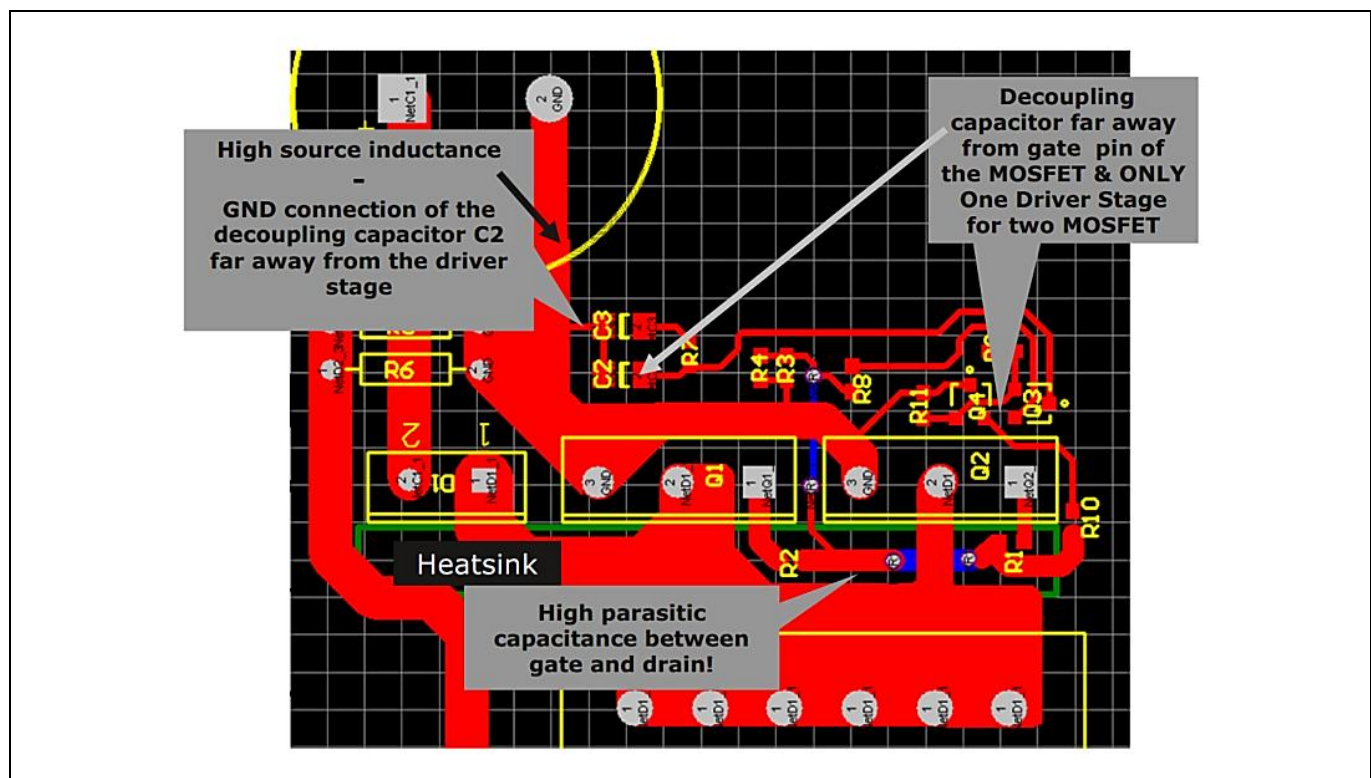


Figure 15 Bad layout example

5.3 Locate gate drivers and gate turn-off components as close as possible to the gate

Always locate the gate drive as close as possible to the driven MOSFET and the gate resistor in close proximity of the gate pin. This prevents it from acting as an antenna for capacitively coupled signals. The controller/IC driver should be capable of providing a strong “low” level drive with voltage as close to ground as possible. MOS or bipolar/MOS composite output stages work well in this regard due to low output saturation voltages. While some drivers may appear to have sufficient margin under static or “DC” conditions, factors such as ground bounce, source inductance drop, and so on can quickly eliminate the operating margin needed to ensure the device remains in the “off” mode.

5.4 Use symmetrical layout for paralleling MOSFETs, and good Isolation of gate drive between FETs

We recommend the use of multi-channel gate drivers in order to have separate channels for each MOSFET. Physical layout should be as symmetrical as possible, with the low impedance driver located as close as possible to the MOSFETs and on a symmetric axis.

5.5 Summary

To summarize, below recommendations are important when designing in CoolMOS™ 900 V to reach highest efficiency with clean waveforms and low EMI stress.

- Control dv/dt and di/dt by proper selection of gate resistor
- Minimize parasitic gate-drain capacitance on board
- Locate gate drivers and gate turn-off components as close as possible to the gate
- Use symmetrical layout for paralleling

900 V CoolMOS™ C3 MOSFET

New 900 V class for superjunction devices and a new horizon for SMPS and renewable energy applications

Related resources

6 Related resources

- [800 V and 900 V CoolMOS™ C3](#)
- [Developer Community](#)

References

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900 V CoolMOS™ C3 MOSFET

New 900 V class for superjunction devices and a new horizon for SMPS and renewable energy applications

Revision history

Revision history

Document revision	Date	Description of changes
V 1.0	–	Initial release
V 1.1	2008-04-03	Modified chapter 3.2
V 1.2	2008-05-13	Disclaimer and Figure 9 actual
V 1.3	2008-05	–
V 1.4	2026-02-02	Lifecycle review: Updated to the latest template and branding update

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