PFC demoboard - system solution

High power density 800 W 130 kHz Platinum server design

Application Note

About this document

Scope and purpose

This document presents the design methodology and results of an 800 W 130 kHz Platinum Server Power Factor Correction (PFC) Continuous Conduction Mode (CCM) Boost Converter, based on:

- 600 V CoolMOS™ C7 Super Junction MOSFET and 650V CoolSiC™ Schottky Diode Generation 5
- 2EDN7524F Non Isolated Gate Driver (EiceDRIVER™)
- ICE3PCS01G PFC controller
- XMC1300 & XMC1400 microcontroller
- ICE2QR4780Z flyback controller

Intended audience

This document is intended for design engineers who want to verify the performance of the latest 600 V CoolMOS™ C7 MOSFET technology working at 130 kHz in a CCM PFC boost converter along with EiceDRIVER™ ICs and 650V CoolSiC™ Schottky Diode Generation 5 using analog and digital control.

Table of contents

1 Introduction 4
1.1 Topology 4
1.2 PFC modes of operation 4

2 Power stage design 7
2.1 EMI filter 7
2.2 Rectifier bridge 7
2.3 PFC choke 8
2.3.1 600 V CoolMOS™ C7 9
2.3.2 Fast dual channel 5 A low side gate driver 10
2.3.3 SiC G5 Diode 10
2.4 Output capacitor 11
2.5 Heat sink design and cooling fan 11
2.6 Specification: input, output, efficiency, power factor 11
2.6.1 Input requirements 11
2.6.2 Output requirements 12

3 ICE3PCS01G PFC controller 13
3.1 Soft start 14
3.2 Switching frequency 14
3.3 Protection features 15
3.3.1 Open loop protection 15
3.3.2 Peak current limit 15
3.3.3 IC supply under voltage lock out 15
3.3.4 DC-link voltage monitor and enable function 15

4 XMC™ digital PFC control implementation 16
4.1 Regulation algorithms 16
4.1.1 Voltage control loop 16
4.1.2 Current control loop 18
4.1.3 Other functionalities 25
4.1.4 Limits and protection 26
4.2 XMC™ implementation 26
4.2.1 Software implementation 26
4.2.2 Hardware usage and configuration 28
4.2.3 PFC state machine 30
4.2.4 Interrupt usage and tasks distribution 31
4.2.5 Software header file 35
4.2.6 Guide to adapt the software to a new design 37
4.2.7 Signaling and protection 38
4.3 Firmware downloading and debugging 39

5 ICE2QR4780Z controllers for auxiliary converter 40
5.1 Input and output requirements 40
5.2 Flyback transformer 40
5.3 Switching frequency 41

6 Experimental results 42

6.1 ICE3PCS01G IC control 42
6.1.1 Efficiency at low and high Line 42
6.1.2 Standby power consumption 44
6.1.3 Efficiency versus semiconductor stress 45
6.1.4 Load steps 46
6.1.5 Conducted EMI measurements 47
6.1.6 Start up 48
6.2 XMC1300 / XMC1400 digital control 49
6.2.1 Power factor, efficiency and input current THD 49
6.2.2 Load steps 52
6.2.3 Start up 53
6.2.4 AC line drop-out 54
6.2.5 Performance of the demoboard at very light load with digital control 55

7 Demoboard 56
7.1 Powerboard 56
7.1.1 Schematics 56
7.1.2 PCB layout 58
7.1.3 Bill of material 60
7.2 ICE3PCS01G daughter board 62
7.2.1 Schematics 62
7.2.2 PCB layout 64
7.2.3 Bill of material 65
7.3 XMC1300 daughter board 67
7.3.1 Schematics 67
7.3.2 PCB Layout 67
7.3.3 Bill of Material 69

8 Useful material and links 71

9 References 72

1 Introduction

Power Factor Correction (PFC) shapes the input current of the power supply to synchronize with the mains voltage, in order to maximize the real power drawn from the mains. In a perfect PFC circuit, the input current follows the input voltage just like a pure resistor, without any input current harmonics or phase shift.

This document is intended to demonstrate the design and practical results of an 800 W 130 kHz Platinum Server PFC demoboard based on Infineon Technologies devices including power semiconductors, non-isolated gate drivers, analog and digital controllers for the PFC converter as well as a flyback controller for the auxiliary supply.

1.1 Topology

Although active PFC can be achieved by several topologies, the boost converter (Figure 1) is the most popular topology used in server PFC applications, for the following reasons:

- The line voltage varies from zero to some peak value typically 375 V_{PK}; hence, a step up converter is needed to deliver a DC bus voltage of 380 V_{DC} or more. For that reason, the buck converter is eliminated, and the buck-boost converter has high switch voltage stress (V_{in}+V_o), therefore it is also not the popular one.
- The boost converter has the filter inductor on the input side, which provides a smooth continuous input current waveform as opposed to the discontinuous input current of the buck or buck-boost topology. The continuous input current is much easier to filter, which is a major advantage of this design as any additional filtering needed on the converter input will increase the cost and reduce the power factor due to capacitive loading of the line.

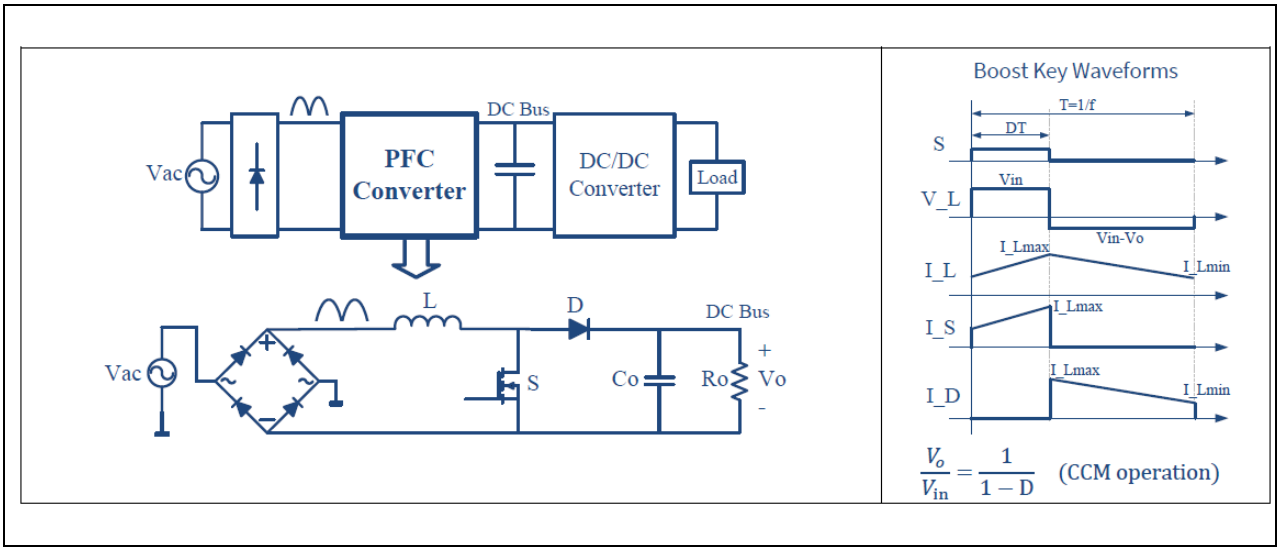


Figure 1 Structure and key waveforms of a boost converter

1.2 PFC modes of operation

The boost converter can operate in three modes: continuous conduction mode (CCM), discontinuous conduction mode (DCM), and critical conduction mode (CrCM). Figure 2 shows modeled waveforms to illustrate the inductor and input currents in the three operating modes, for exactly the same voltage and power conditions.

By comparing DCM to the other modes, DCM operation seems simpler than CrCM, since it may operate in constant frequency operation; however DCM has the disadvantage that it has the highest peak current when compared to CrCM and also to CCM, without any performance advantage when compared to CrCM.

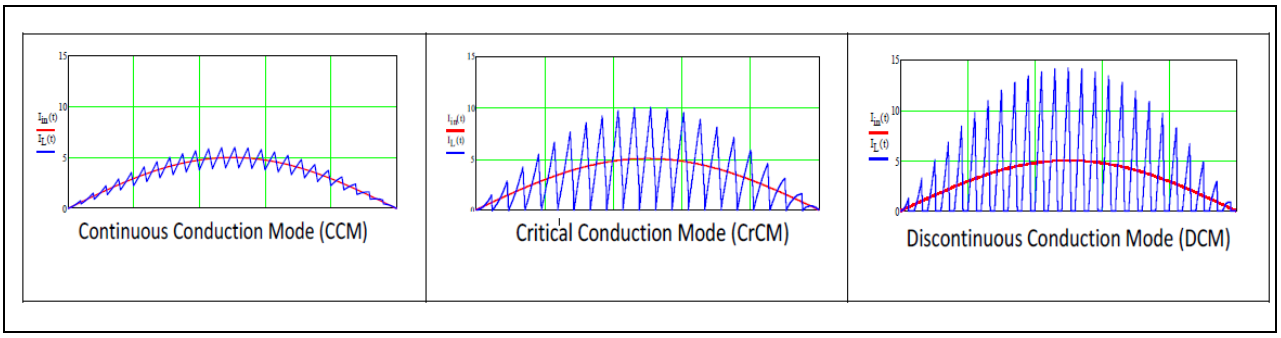


Figure 2 PFC Inductor and input line current waveforms in the three different operating modes

CrCM may be considered to be a special case of CCM, where the operation is controlled to remain at the boundary between CCM and DCM. CrCM normally uses constant on-time control; the line voltage is changing across the 50/60 Hz line cycle, the reset time for the boost inductor is varying and the operating frequency will also change in order to maintain the boundary mode operation. CrCM requires the controller to sense the inductor current zero crossing in order to trigger the start of the next switching cycle.

For fix switching frequency operation, the input voltage and power output of the PFC will determinate the operation mode, in this way we may have:

- Complete half AC cycle in CCM operation mode
- Complete half AC cycle in DCM operation mode
- DCM and CCM operation modes during half AC cycle

The boundaries between such operation modes can be calculated theoretically, an example is shown in Figure 3:

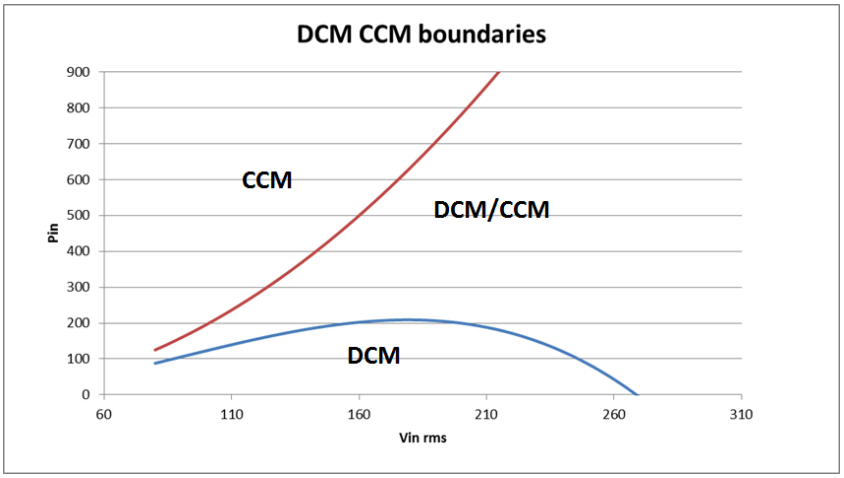


Figure 3 Operation mode boundaries

The control mode of the PFC topology explained in this document is focused on the constant switching frequency operation control mode, due to its advantage of simplified input filter, as well as solve the

different operation modes with the XMC™ digital controller to maximize the performance of the whole system. The proposed concept and implementation will cover DCM and CCM operation mode, therefore we can say that the algorithm supports multimode operation.

2 Power stage design

2.1 EMI filter

The EMI filter is implemented as a two-stage filter, which provides sufficient attenuation for both differential mode (DM) and common mode (CM) noise.

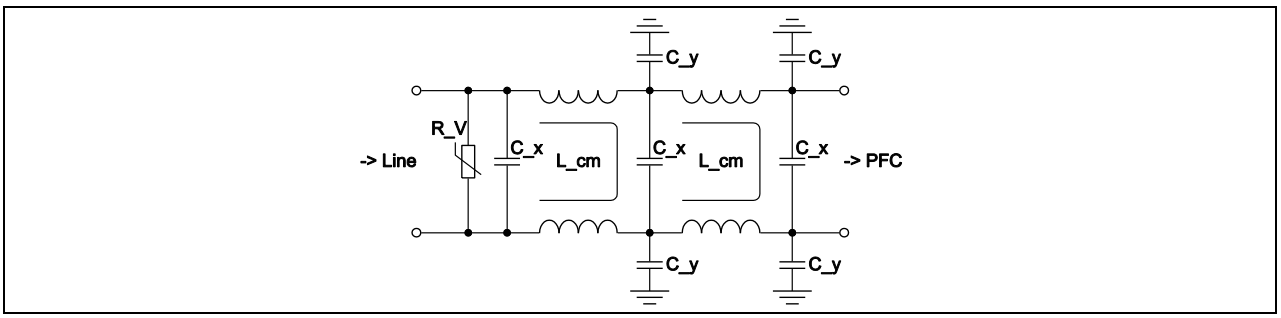


Figure 4 Two-stage filter structure

The two high current common mode chokes L_cm are based on high permeability toroid ferrite cores. The first CM choke is 2 x 26 Turns / 2 x 4,76 mH and the second one is 2 x 28 Turns / 2 x 5,7 mH. The relatively high number of turns causes a considerable amount of stray inductance, which ensures sufficient differential mode attenuation.

2.2 Rectifier bridge

The rectifier bridge is designed for the worst case: maximum output power and minimum input voltage. To calculate the input current, an efficiency of 94% (at V_{in} = 90 V_{AC}) is applied.

Maximum RMS value of the input current:

$$I_{INrms} = \frac{P_{OUTmax}}{\eta V_{INrms}} = \frac{800W}{0{,}94 \cdot 90V} = 9{,}46A$$ Equation 2-1

Maximum RMS value of the diode current:

$$I_{Drms} = \frac{I_{INrms}}{2} = 4{,}73A$$ Equation 2-2

Maximum average value of the diode current:

$$I_{Davg} = \frac{\sqrt{2} I_{INrms}}{\pi} = 4{,}26A$$ Equation 2-3

Due to the calculated mean and effective current values, the rectifier type LVB2560 with very low forward voltage drop was selected. This 800 V device has sufficient voltage reserve with V_{in} = 265 V. The smaller size types GBU and KBU are only available for currents up to 10A. For the following formula, r_D was extracted from the characteristic curve of the data sheet (T_A = 100 °C).

Conduction losses of a rectifier diode:

$$P_D = I_{Davg} \cdot V_D + (I_{Drms})^2 \cdot r_D = 4{,}26A \cdot 0{,}5V + (4{,}73A)^2 \cdot 0{,}016\Omega = 2{,}49W \qquad \text{Equation 2-4}$$

Total losses of the rectifier:

$$P_{REC} = 4P_D = 4 \cdot 2{,}49W = 9{,}96W \qquad \text{Equation 2-5}$$

2.3 PFC choke

The PFC choke design is based on a toroidal high performance powder core.

Toroidal chokes have a large surface area and allow a good balance, minimizing core and winding losses, and achieving a homogeneous heat distribution without hot spots. Hence they are suitable for systems which are targeting the highest power density with forced air cooling. Very small choke sizes are feasible.

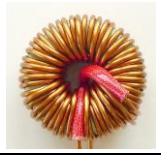


Figure 5 Photograph of PFC choke

The core material chosen was Chang Sung Corporation's (CSC) HIGH FLUX, which has an excellent DC bias and good core loss behavior. The part number is CH270060. The outer diameter of the core is 27mm.

The winding was implemented using enameled copper wire AWG 16 (1,25 mm diameter). The winding covers approximately 1,5 layers, meaning that there is one layer on the outer diameter, while inside there is a double layer structure. This arrangement allows a good copper fill factor, while still having good AC characteristics, and is a preferred fill form factor for high power toroidal inductors.

There are 60 turns, taking advantage of the high allowable DC bias. The resulting small signal bias inductance is 270 µH. The effective inductance with current bias is determined by the core material B-H characteristics and illustrated as follows:

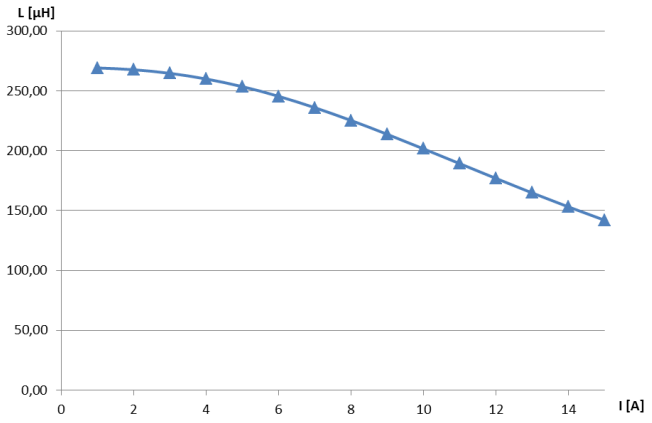


Figure 6 DC-Bias dependency of inductance

The effective inductance together with the switching frequency of 130 kHz, produce a relatively low current ripple, which supports the whole system performance. The peak and RMS currents for the semiconductors and filter components are minimized. The low ripple design achieves low core losses, which is important for light load performance of the system.

Table 1 Choke losses @800 W/130 kHz (calculation results of magnetic design software)

V_{in_ac} [V]	P_{core} [W]	P_{wi} [W]	P_{tot} [W]
90	1,2	4,5	5,7
115	1,5	2,9	4,4
230	1,5	0,9	2,4

Infineon Semiconductors

2.3.1 600 V CoolMOS™ C7

The 600 V CoolMOS™ C7 series of devices offers a ~50% reduction in turn-off losses compared to the CoolMOS™ CP, offering a GaN-like level of performance in PFC, TTF and other hard-switching topologies. The CoolMOS™ C7 delivers an area-specific on resistance ($R_{DS(ON)}$*A) of just 1Ω per mm², extending Infineon's portfolio of products with lowest $R_{DS(ON)}$ per package to support customer efforts to further increase power density.

The 600 V CoolMOS™ C7 series features ultra-low switching losses and targets high power SMPS applications such as server, telecom, solar and industrial applications requiring high efficiency and a reduced Bill of Materials (BoM) and low total cost of ownership (TCO).

Applications driven by efficiency and Total Cost of Ownership, such as hyper-scale data centers and telecom base stations benefit from the switching loss reduction offered by CoolMOS™ C7. Efficiency gains of 0.3% to 0.7% in PFC and 0.1% in LLC topologies can be achieved, leading to significant TCO benefits. In the case of a 2.5 kW server PSU, for example, using 600 V C7 MOSFETs can result in energy cost reductions of ~10% for PSU energy loss.

In BoM and cost driven designs such as enterprise servers, the 600 V CoolMOS™ C7 devices offer a cost reduction in magnetics. Due to the significantly lower gate charge and output capacitance, the C7 can be operated at double the normal switching frequencies with only a marginal loss in efficiency. This allows the size of magnetic components to be minimized, lowering the overall BoM cost. For example, doubling the switching frequency from 65 kHz to 130 kHz may reduce the magnetic component cost by as much as 30%.

2.3.1.1 Design implementation

Based on the analysis of several current server PSUs and customer feedback, it is a common practice to implement two MOSFETs in parallel in the classic PFC topology for improving thermal performance during both normal and critical operating conditions like AC line drop out. As a result, this demoboard is designed to use and test two 180 mΩ TO-220 MOSFETs working in parallel. This also has the advantage of lowering the net source inductance, and helps avoid source inductance related increases in switching losses which occur above 5 A in a single package, by splitting the current load at low line between two packages.

2.3.2 Fast dual channel 5 A low side gate driver

2.3.2.1 Introduction

The 2EDN7524 is a non-inverting fast dual-channel driver for low-side switches. Two true rail-to-rail output stages with very low output impedance and high current capability are chosen to ensure highest flexibility and cover a wide variety of applications.

All inputs are compatible with LVTTL signal levels. The threshold voltages (with a typical hysteresis of 1 V) are kept constant over the supply voltage range.

Since the 2EDN7524 is particularly aimed at fast-switching applications, signal delays and rise/fall times have been minimized. Special effort has been made toward minimizing delay differences between the 2 channels to very low values (typically 1 ns).

The 2EDN7524 driver used in this demoboard comes in a standard PG-DSO-8 package.

2.3.2.2 Driver outputs

The two rail-to-rail output stages realized with complementary MOS transistors are able to provide a typical 5 A of sourcing and sinking current. The on-resistance is very low with a typical value below 0.7 Ω for the sourcing p-MOS and 0.5 Ω for the sinking n-MOS transistor. The use of a p-channel sourcing transistor is crucial for achieving real rail-to-rail behavior and not suffering from the source follower's voltage drop.

Gate drive outputs are held active low in case of floating inputs (ENx, Inx) or during startup or power down once UVLO is not exceeded.

2.3.2.3 Under Voltage Lockout (UVLO)

The Under-Voltage Lockout (UVLO) function ensures that the output can be switched to its' high level only if the supply voltage exceeds the UVLO threshold voltage. Therefore, it can be guaranteed that the switch transistor is not operated if the driving voltage is too low to completely switch it on, so avoiding excessive power dissipation.

The default UVLO level is set to a typical value of 4.2 V or 8 V (with some hysteresis). A UVLO of 4.2 V is normally used for low voltage and TTL based MOSFETs. For higher level, like high voltage super junction MOSFETS, an minimum active voltage of 8 V is used.

2.3.3 SiC G5 Diode

Selection of the boost diode is a major design decision in a CCM boost converter, because the diode is hard commutated at a high current, and the reverse recovery can cause significant power loss, as well as noise and current spikes. Reverse recovery can be a bottleneck for high switching frequency and high power density power supplies. Additionally, at low line, the available diode conduction duty cycle is quite low, and the forward current quite high in proportion to the average current. For that reason, the first criteria for selecting a diode in a CCM boost circuit are fast recovery with low reverse recovery charge, followed by V_f operating capability at high forward current.

Since SiC Schottky diodes have a capacitive charge, Q_c, rather than reverse recovery charge, Q_{rr} their switching loss and recovery time are much lower than a Silicon ultrafast diode leading to an enhanced performance. Moreover, SiC diodes allow higher switching frequency designs, hence, higher power density converters are achieved. The capacitive charge for SiC diodes are not only low, but also independent of di/dt, current level, and temperature; which is different from Silicon diodes that have strong dependency on these conditions.

The recommended diode for CCM boost applications is the 650 V CoolSiC™ Schottky Diode Generation 5, which include Infineon's leading edge technologies, such as diffusion soldering process and wafer thinning technology. The result is a new family of products showing improved efficiency over all load conditions, resulting from the improved thermal characteristics. Note that even with the high surge current capability of SiC diode Schottky diode, it is still preferred to use a bulk pre-charge diode. This is a low frequency standard diode with high I^2t rating to support pre-charging the bulk capacitor to the peak of the AC line voltage; this is a high initial surge current stress (which should be limited by a series NTC) that is best avoided for the HF boost rectifier diode.

In this demo board, a 6 A IDH06G65C5 diode is used.

2.4 Output capacitor

Possible over-voltages require the selection of a 450 V (low impedance) type capacitor. The minimum capacitance is defined by the minimum hold up time and the minimum allowable DC-link voltage of the system or the maximum allowable voltage from the 2x line frequency AC ripple current:

- t_{hu} = 10 ms
- V_{bmin} = 320 V

$$C_b = \frac{2 * P_{out} * t_{hu}}{V_b^2 - V_{bmin}^2} = 381\ \mu F \qquad \text{Equation 2-6}$$

The chosen type is a 470 µF RUBYCON 450 V XH470MEFCSN30X50 capacitor.

2.5 Heat sink design and cooling fan

Heat sinks for the rectifier and power semiconductors are made of a 1 mm copper plate.
Fan speed control operation depends on the board/heatsink temperature. There are two speed levels, the fan operates with low speed at 57°C and increases to high speed above 79°C.

2.6 Specification: Input, Output, Efficiency, Power factor

2.6.1 Input requirements

Table 2 Input requirements

Parameter	Value
Input voltage range, V_{in_range}	90 V_{AC} – 265 V_{AC}
Nominal Input Voltage, V_{in}	230 V_{AC}
AC Line Frequency range, f_{AC}	47 – 64 Hz
Max peak Input current, I_{in_max}	10 ARMS @ V_{in} = 90 V_{AC} , P_{out_max} = 800 W , Max load
Turn on input voltage, V_{in_on}	80 V_{AC} – 87 V_{AC}, Ramping up
Turn off input voltage, V_{in_off}	75 V_{AC} – 85 V_{AC}, Ramping down
Power Factor , PF	Shall be greater than 0.95 from 20% rated load and above
Hold up time	10 ms after last AC zero point @ P_{out_max} = 800 W, V_{out_min} = 320 V_{DC}
Total Harmonic Distortion, THD	<15% from 10% load @ high line, for class A equipment

2.6.2 Output requirements

Table 3 Output requirements

Parameter	Parameter
Nominal output Voltage, V_{out}	380 V_{DC}
Maximum Output Power, Pout	800 W
Peak Output Power, Pout_max	1 kW
Maximum Output Current, Iout_max	2,1 A
Output Voltage ripple	Max 20 Vpk-pk @ V_{out}, I_{out}
Output OV threshold maximum	450 V_{DC}
Output OV threshold minimum	420 V_{DC}

3 ICE3PCS01G PFC controller

The ICE3PCS01G is a 14pin controller IC for power factor correction circuits. It is suitable for wide range line input applications from 85 to 265 V_{AC} with overall efficiency above 97%. The IC supports the converters in boost topology and operates in continuous conduction mode (CCM) with average current control by regulating D_{off}, without the need for input voltage sensing except for brown out detection.

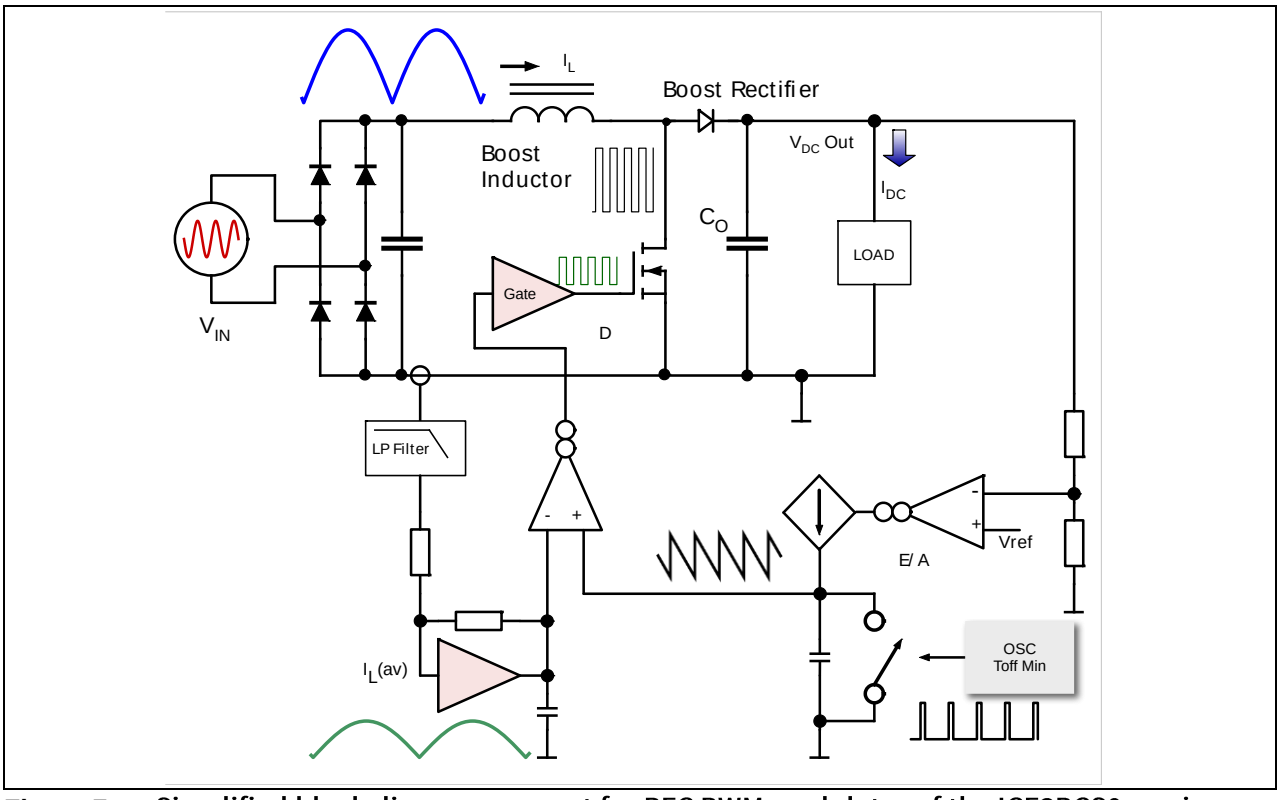


Figure 7 Simplified block diagram concept for PFC PWM modulator of the ICE3PCS0x series

The IC operates with a cascaded control; the inner current loop and the outer voltage loop. The inner current loop of the IC controls the sinusoidal profile for the average input current. It uses the dependency of the PWM duty cycle on the line input voltage to determine the corresponding input current. This means the average input current follows the input voltage as long as the device operates in CCM. Under light load conditions, depending on the choke inductance, the system may enter into discontinuous conduction mode (DCM) resulting in higher harmonics but still meeting the Class D requirement of IEC 1000-3-2 (EN 61000-3-2). The current sense amplifier filters and amplifies the ISENSE signal and provides a current loop bandwidth control via the ICAP pin for external compensation capacitor.

The outer voltage loop of the IC regulates the output bulk voltage and is realized digitally within the IC, using a delta-sigma converter operating at about 3.4 kHz to digitize the voltage feedback signal. Depending on the load condition, the PID signal is converted to an appropriate low frequency voltage that controls the amplitude of the current loop by means of a variable voltage ramp generated at the switching clock frequency, which is also sent to the PWM comparator. The current charging the ramp generator is a function of the error amplifier feedback level, plus some nonlinear block signal processing.

The digital PID has some unique features that give it some regulation advantages when compared with conventional OTA amplifiers, while still realizing low harmonic distortion and high power factor.

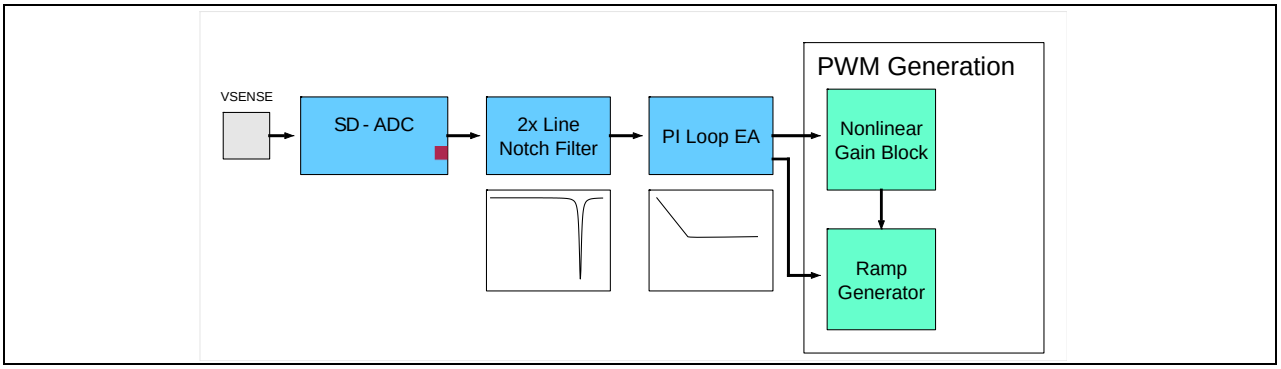


Figure 8 Digital error amplifier system concept, with 2x line frequency notch filter

The self calibrating 2x line frequency notch filter greatly reduces the distortion effects from feedback of the bulk capacitor ripple, while allowing somewhat higher gain, which translates to better load step transient response.

The IC is equipped with various protection features to ensure safe operation for the system and the device.

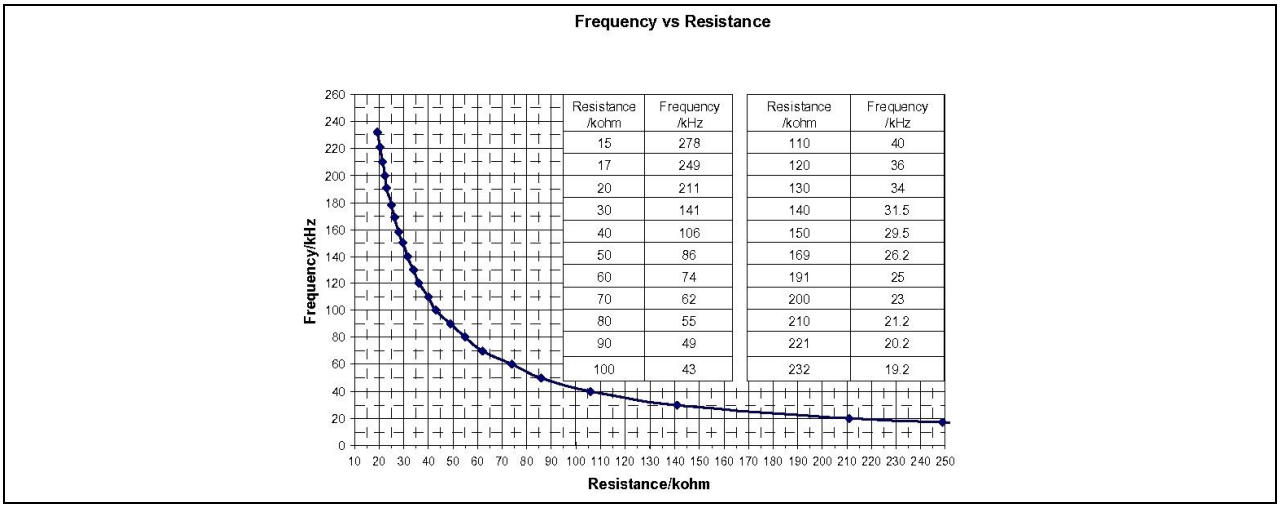
3.1 Soft start

During power up when V_{OUT} is less than 96% of the rated level, the internal voltage loop output increases from the initial voltage under the soft-start control. This results in a controlled linear increase of the input current from 0A. This helps to reduce the current stress in power components.

Once V_{OUT} has reached 96% of the rated level, the soft-start control is released to achieve good regulation and dynamic response and the VB_OK pin is raised to 5V indicating that the PFC output voltage is in the normal range.

3.2 Switching frequency

The switching frequency of the PFC converter can be set with an external resistor R_{FREQ} attached between the FREQ pin and SGND. The voltage on the FREQ pin is typically 1 V. The corresponding capacitor for the oscillator is integrated in the device and the R_{FREQ}/frequency is given in Figure 9. The recommended operating frequency range is from 21 kHz to 250 kHz. In the case of this demoboard, a R_{FREQ} of 33 kΩ at pin FREQ will set a switching frequency f_{SW} of around 134 kHz (typ).



Resistance /kohm	Frequency /kHz	Resistance /kohm	Frequency /kHz
15	278	110	40
17	249	120	36
20	211	130	34
30	141	140	31.5
40	106	150	29.5
50	86	169	26.2
60	74	191	25
70	62	200	23
80	55	210	21.2
90	49	221	20.2
100	43	232	19.2

Figure 9 Frequency setting in the ICE3PCS01G IC

3.3 Protection features

3.3.1 Open loop protection

Open loop protection is available for this IC to safe-guard the output and is implemented using a comparator with a threshold of 0.5 V. Whenever the voltage at the VSENSE pin falls below 0.5 V, or equivalently V_{OUT} falls below 20% of its rated value, it indicates an open loop condition (i.e. VSENSE pin not connected). In this case, most of the blocks within the IC will be shutdown. Normally the bulk pre-charge diode will charge the bulk capacitance to a value higher than this, so this voltage range will occur.

3.3.2 Peak current limit

The IC provides a cycle by cycle peak current limitation (PCL). It is active when the voltage at pin ISENSE reaches -0.2 V. This voltage is amplified by a factor of -5 and connected to comparator with a reference voltage of 1.0 V. A de-glitcher with 200 ns after the comparator improves noise immunity for the activation of this protection. In other words, the current sense resistor should be designed to be lower than the -0.2 V PCL for normal operation.

3.3.3 IC supply under voltage lock out

When the supply voltage V_{CC} is below the under voltage lockout threshold $V_{CC,UVLO}$, (typically 11 V), the IC is turned off and the gate drive is pulled low internally to maintain the off state. The current consumption is reduced to only 1.4 mA.

3.3.4 DC-link voltage monitor and enable function

The IC monitors the bulk voltage status through the VSENSE pin and outputs a TTL signal to enable the PWM IC or control the inrush relay. During soft-start once the bulk voltage is higher than 95% of the rated value, pin VB_OK is raised to a high level. The threshold to trigger the low level is determined by the externally adjustable voltage on the VBTHL pin.

When the VBTHL pin is pulled lower than 0.5V, most functional blocks are turned off and the IC enters into standby mode for low power consumption. When the disable signal is released the IC recovers via a soft-start.

4 XMC™ digital PFC control implementation

The XMC1300 & XMC1400 are part of the XMC™ microcontroller family from Infineon Technologies. This family of microcontrollers based on ARM™ Cortex™–M0 cores is designed for real time critical applications. The control of power supplies is a strong focus for XMC™ microcontrollers where users can benefit from features such as analog comparators, PWM timers, co-processors or high precision analog to digital converters.

This section describes how to use an XMC™ microcontroller to implement a digital PFC controller. Some of the XMC1300 & XMC1400 features are listed here:

- 12 bit ADC, 1 MSample/sec. Flexible sequencing of conversions including synchronization
- Clock frequency is 32/48 MHz, nevertheless, key peripherals can run at double the CPU frequency, like PWM timers or MATH Co-Processors, to accelerate calculations or improve PWM resolution.
- Fast analog comparators for protections such as overcurrent protection.
- Co-Processor that can run in parallel to the main core (Cortex-M0). In this particular case will help executing faster divisions (17 clock cycles)
- Flexible timing scheme due to CCU timers. These timers allow synchronization of PWM patterns and accurate generation of ADC triggers.
- Interconnection matrix to route different internal signals from one peripheral to another. As an example, the timers can connect to an ADC to signify the exact point in time when a signal must be sampled, or a comparator output can be connected to a PWM timer. This can be used to make sure that whenever the comparator trips, the PWM stops.

Serial communication protocols are supported including UART, I2C, SPI. These are used for GUI or possible communication with the secondary stage of a full power supply.

4.1 Regulation algorithms

The output of the proposed PFC is regulated in voltage; therefore a voltage feedback and the corresponding regulation loop is needed to keep regulated DC output voltage.

Due to the nature of the proposed topology, the output will contain a considerable ripple added to the DC output voltage which depends on the load conditions, implying that special care for output voltage sensing needs to be considered.

On other hand, it is required to keep an input current waveform that follows, in a proportional manner, the input voltage to keep good power factor and low Total Harmonic Distortion.

To solve the previously mentioned challenges a feedback loop will be used, with a voltage loop controlling an inner current loop.

4.1.1 Voltage control loop

Based on the load model shown in Figure 10, If a small variation at the output voltage is assumed (normally the case when a big output capacitor is used), the system can be seen as a current source feeding the output capacitor and the PFC load can be represented as a current sinking source taking energy from the output capacitor.

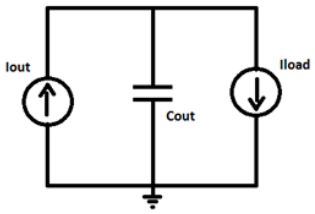


Figure 10 Simplified PFC plant

The resulting voltage loop with its inner current block is shown below.

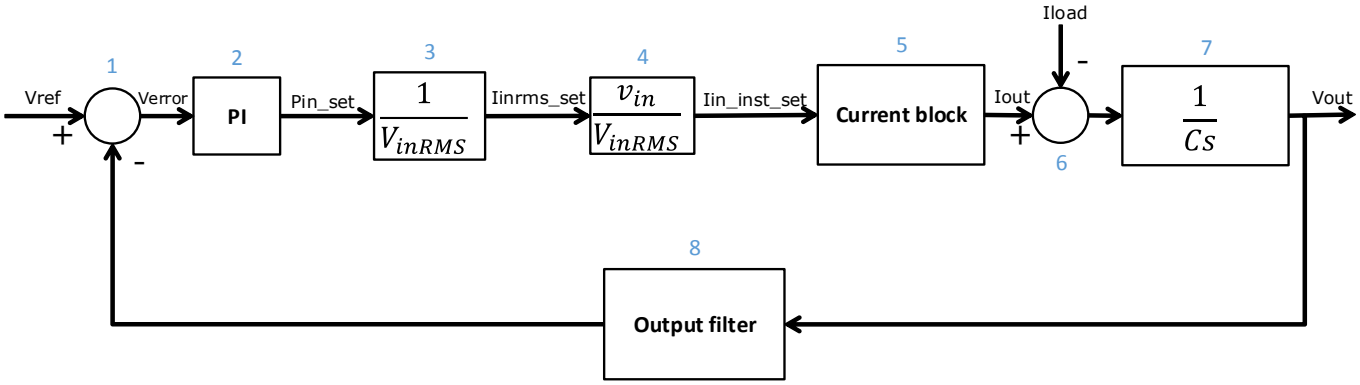


Figure 11 Voltage loop block diagram

The different blocks of the voltage loop are described in Table 4.

Table 4 Voltage loop blocks

Block number	description
1	Subtraction to calculate the error from the reference voltage
2	PI regulator
3	Input current RMS calculation
4	Current shaping according to input voltage
5	Current block, ensure that input current follow the instantaneous given value
6	Total current flowing into the output capacitor
7	Output capacitor model
8	Filter used to extract the DC value from the output voltage

From Figure 11, it is possible to give units to the *P* and *I* part of our *PI* regulator:

- **P** will be measured in Watts/volt.
- **I** will be measured Watts/(volts × sec)

Special attention must be paid at the output voltage filter, since a low pass filter would add a delay into the system that may result into instable loop or slow regulation. To avoid such issue an optional notch filter and a non-lineal filter are suggested.

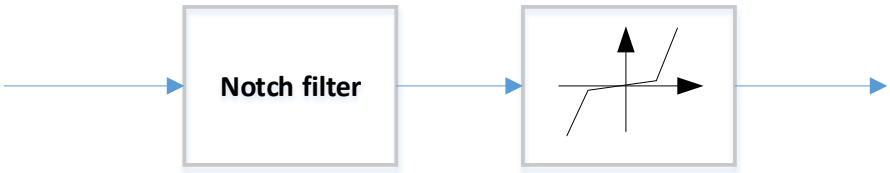


Figure 12 Output filter

The notch filter rejects the major frequency of the output voltage (100Hz or 120Hz); a selection is done during start up depending of the line frequency.

The non-lineal filter ensures a smooth response for small drifts of the output voltage but increase its response when the output drift is too high to ensure a good response during load or line transients.

4.1.2 Current control loop

The current loop will ensure that a given current is taken from the line independent of the input voltage; such current is commanded by the outer voltage loop. As can be seen in Figure 3, the conduction mode results into CCM mode, DCM mode and/or a mix mode which changes along the half AC cycle.

To find out the operation mode boundary a closer look at the inductor current shape is required. The border between CCM and DCM occurs when the lower value of the current hits zero at the end of the off phase, in other words, the peak to peak current is double than the average current.

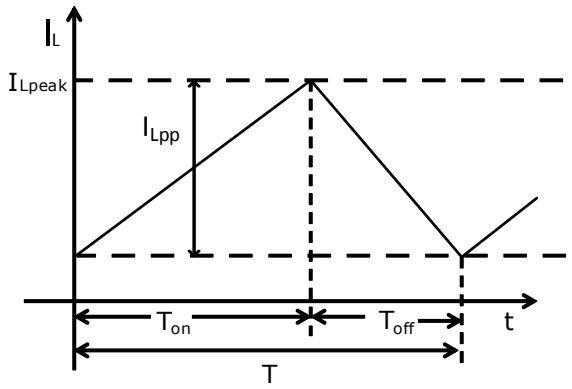


Figure 13 Inductor current shape during CCM operation

Assuming the switching frequency is higher than the line frequency, it can be stated that the base duty cycle in CCM (D_{Bccm}) is:

$$V_{in}T_{on} = (V_{out} - V_{in})T_{off} \quad \text{Equation 4-1}$$

$$D_{Bccm} = 1 - \frac{V_{in}}{V_{out}} \quad \text{Equation 4-2}$$

From Figure 13 it can be stated that the inductor peak to peak current is:

$$I_{Lpp} = \frac{V_{in}}{L} T_{on}$$ Equation 4-3

The condition to have DCM is that $I_{lpp}>2I_{set}$, where I_{set} is the desired average current. Considering the previous equation the condition for DCM is:

$$V_{in} D_{Bccm} > 2\frac{L}{T} I_{set}$$ Equation 4-4

The previous equation can be used to evaluate when exactly the DCM operation occurs either during a complete or partial half cycle.

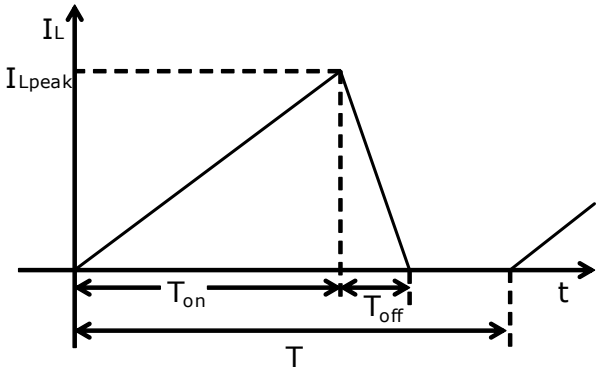


Figure 14 Inductor current shape during DCM operation

During DCM operation the base duty cycle required comes from the Equation 0

$$I_{Lpeak} = \frac{V_{in} T_{on}}{L} = 2I_{set} \frac{T}{T_{on}+T_{off}}$$ Equation 4-5

$$D_{Bdcm} = \sqrt{\frac{2LI_{set} D_{Base}}{TV_{in}}}$$ Equation 4-6

Looking at the gains in CCM and steady state for DCM, two different equations can be obtained:

For CCM:

$$\frac{\hat{\imath}}{\hat{d}} = \frac{V_{out}}{sL}$$ Equation 4-7

For DCM:

$$\frac{dI}{dD} = \frac{V_{in} T D_{Bdcm}}{L D_{Bccm}}$$ Equation 4-8

The gains shown for CCM and DCM are different and normally there is an abrupt change of them at the boundary.

In Figure 15 we can see the operation mode for the next conditions (considering no losses):

- Switching frequency: 128 kHz
- Inductance value: 270 µH
- V_{AC} RMS: 230 V
- Input current: 1 A
- Output voltage: 380 V

Figure 16 shows the change of the gain due to the different operation modes for the same conditions.

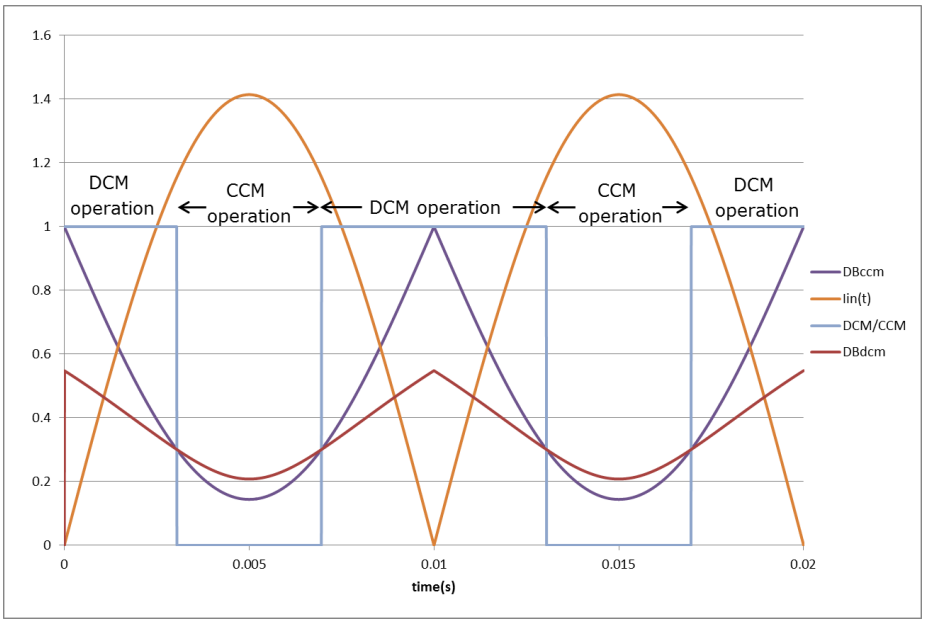


Figure 15 Operation mode over half AC cycle

Figure 15 shows the CCM base duty cycle (D_{Bccm}) previously calculated, as well as the required duty cycle required for DCM operation. From this analysis, it can be clearly stated that a pure CCM algorithm would not ensure good current shape under all conditions.

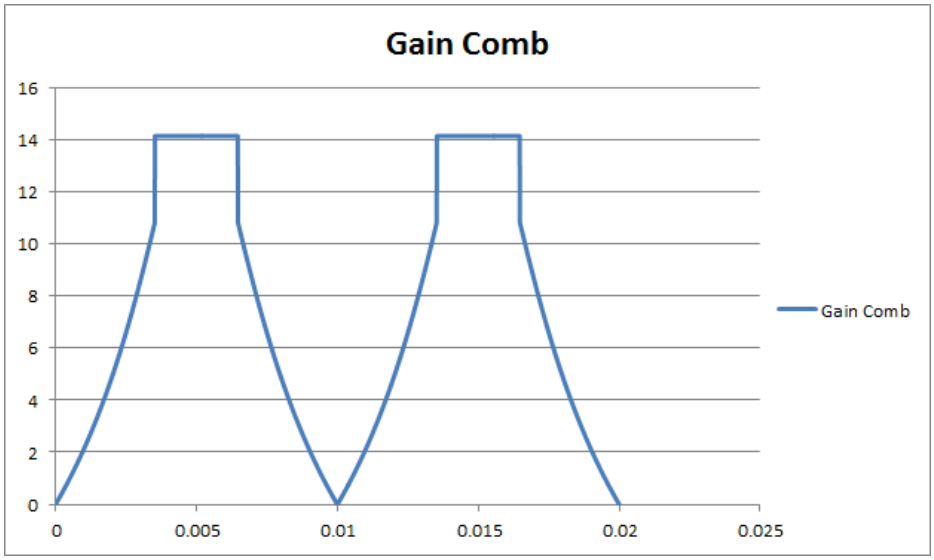


Figure 16 Plant gain over one AC cycle

The change of the operation mode and the required duty cycle as well as the system transfer function gain need to be consider in the regulator to achieve the best performance.

A feed-forward of the required duty cycle is given as a base to the regulator, in such way that the offset to be corrected by the regulator is much less.

On the other hand, the proportional part of the regulator is changed inversely proportional to the gain of the system transfer function in order to linearized the system and ensuring the best performance and stability in all cases and thus avoid the need to trim the regulator coefficients depending of the line and load conditions. This intelligent algorithm allows easy code porting and adaptation to new designs.

Additional aspects to consider are:

- Distinguish when CCM or DCM mode is present
- In DCM it is necessary to calculate the real average current compare to the measured current.
- Change the proportional part of the **PI** according to the plant DCM or CCM.

Since the gain of the plant in DCM is normally lower and in some cases much lower than the gain in CCM, the proportional part of the ***PI*** has to be higher for DCM than CCM. Not correcting such change in gain provokes the risk of having CCM operation with the required compensator gain of DCM which would result in a current overshoot and/or oscillations. Therefore, the appropriate measures have to be taken into account to avoid such situation. As a result, three factors are considered:

- The assumed operation mode is the one which gives the minimum duty cycle.
- The used CCM base duty cycle is multiplied by a constant less than 1 to ensure an early entry to and late exit from CCM mode.
- The compensator gain used for CCM (lower than DCM gain) is used in DCM close to the boundaries.

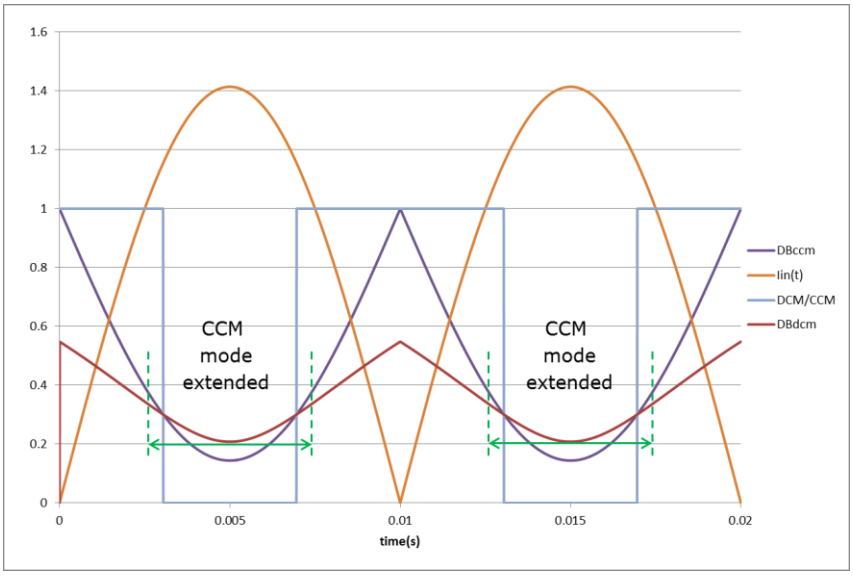


Figure 17 Controller proportional gain change

Particularly, the gain is changed when the DCM base duty cycle is bellow CCM base duty cycle plus a given delta.

The correction of the measured average current respect to the sampled one is a function of the base duty cycle for DCM and CCM as shown in Equation 4-0.

$$I_{avg} = I_{sam} \frac{D_{Bdcm}}{D_{Bccm}} \qquad \text{Equation 4-0}$$

Considering all that has been mentioned above, the algorithm can be summarized as shown in Figure 18:

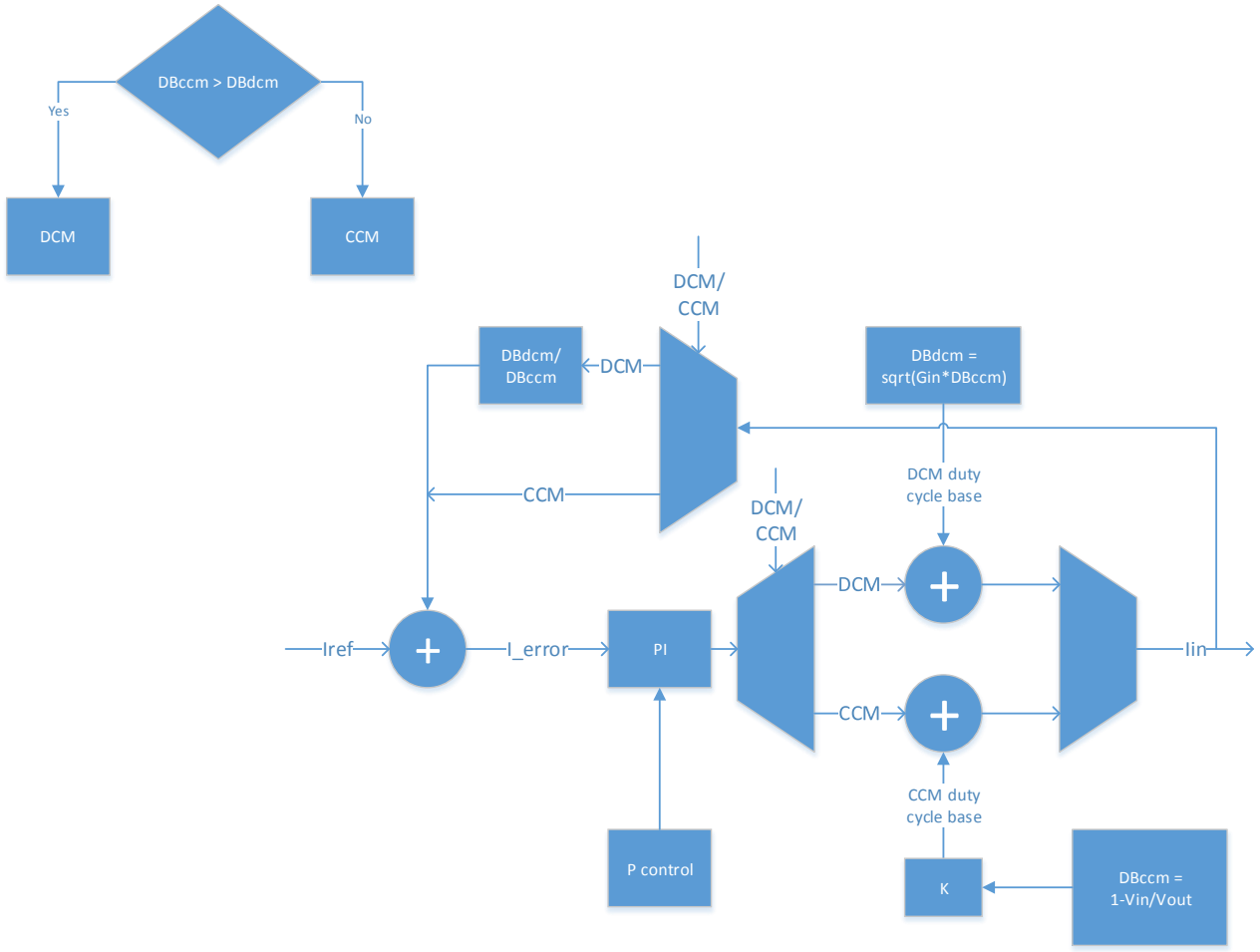


Figure 18 Current loop block diagram

4.1.2.1 Practical improvements to the current loop

The performance in terms of the Total Harmonic Distortion (THD) of the input current could be further improved by enforcing certain operation mode under certain load and line conditions. For example, when only a small portion of the half AC wave requires DCM operation, it is better to use only the CCM algorithm because it will result in a smoother current shape. Please be aware that this has not been is not implemented in the current version of the digital control in the demoboard.

4.1.2.2 Additional considerations for the current loop

Different effects need to be taken into account to ensure a full performance of the system.

- Compensator´s proportional part adjustment
- MOSFET output capacitor effect, C_{oss}

The compensator´s proportional part is adjusted upon the operation mode as explained in section 4.1.2, and additionally, the compensator´s gain for every mode includes the inverse of the plant gain multiplied by a constant in order to linearize the plant behavior, as expressed in Equation 4-10 and Equation 4-11.

For CCM:

$$P = k_{ccm}\frac{L}{TV_{out}}$$ Equation 4-10

For DCM:

$$P = k_{dcm}\frac{LD_{Bccm}}{V_{in}TD_{Bdcm}}$$ Equation 4-11

Additionally, the variation of the inductance with the current has to be taken into account by decreasing the compensator proportional part as the input current increases, as shown in Figure 6. Correcting such variations will avoid oscillations of the input current when its value is too high. The compensation is done assuming a lineal decrease of the inductance with respect to the current.

The second effect to be corrected is the influence of the MOSFET output capacitor. As shown in Figure 19, the current in the inductance (yellow) continue flowing while the output MOSFET capacitance is being charged (blue V_{DS}) even if the gate driver is already off (red).

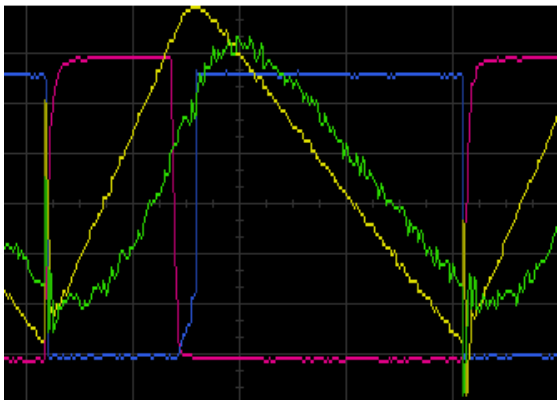


Figure 19 C_{oss} **effect on the inductance current**

Such effect is visible in the input current shape around the zero crossing for high RMS input current values, under such conditions the duty cycle is almost one and the resulting effect leads to “concatenated-like” pulses until the input current is high enough to bring the V_{DS} up.

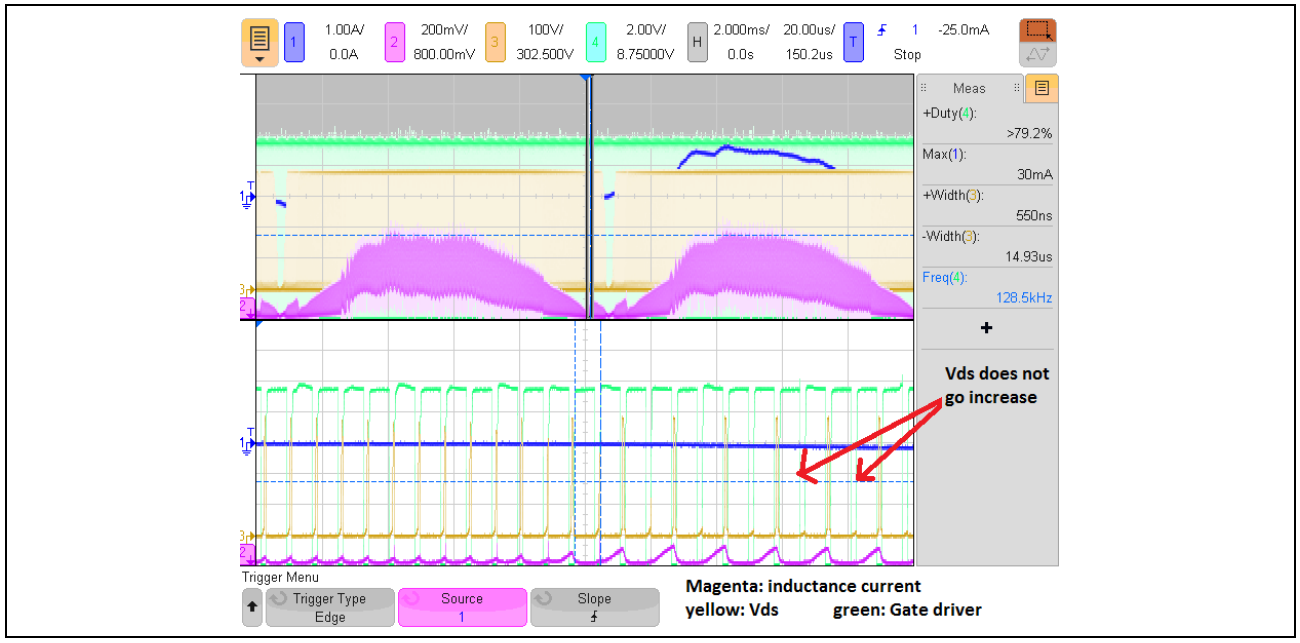


Figure 20 C_{oss} **effect on the inductance current**

Such correction improves the current shape during zero crossing of the input voltage for high load low line operation, allowing value of total harmonic distortion below 2%.

4.1.3 Other functionalities

4.1.3.1 Pseudo PLL and RMS calculation

One of the basic variables required for the regulation loops is the input voltage RMS value. To allow a fast reaction, it is desired to have the value update as soon as possible. Take an example of a line transient where an increase of input voltage does not result into a decrease of the input current. The energy transferred may increase significantly.

Although the feedforward used in the current loop for the duty base calculation helps, a pseudo PLL synchronized with the input voltage zero crossing has been implemented. At every voltage zero crossing, the average value of the input voltage for the last half AC cycle will be measured. Assuming a perfect rectified sine wave the RMS value is extracted by multiplying the average by a given factor: 1.11 (RMS value/average value).

The PLL has an additional functionality such as a counter to measure the input voltage frequency, which is used to determine the notch filter to be used (100 Hz rejection or 120 Hz rejection) in case it is not bypassed.

4.1.3.2 Start up phase

The start up phase is the time taken to bring the output voltage into its regulation point. In order to allow a smooth start up, a programmable ramp can be configured in the software that will result in a progressive increase of the reference voltage. Such approach helps the user to avoid overshoots and excessive current to charge the output capacitor.

4.1.4 Limits and protection

Several limits and protection features have been implemented to ensure the safe operation of the whole system; they can be divided into hardware protections and software limits and protections.

4.1.4.1 Hardware protections

There are two hardware protections implemented with comparators that will deactivate the gate driver in case these are triggered:

- Output overvoltage protection: the comparator is fed with a constant voltage (limit) and the output voltage scaled for comparison.
- Inductor overcurrent protection: the comparator is fed with a constant voltage (limit) and the input current sensed for comparison.

4.1.4.2 Software limits and protections

While the application is running, several limits are applied to avoid stress of the components (limits will not trigger a shutdown):

- Instantaneous input current: limits the value of the requested instantaneous current set point for the current loop
- Instantaneous input power: limits the value of the **PI** output in the voltage loop which represents the transferred power.
- Instantaneous input conductance: limits the value of the set input conductance value (I_{RMS}/V_{RMS}).
- Output voltage limit: If the output voltage is over this limit, the requested input power of the system is set to 0.
- Duty cycle minimum and maximum values
- Absolute value of the delta duty cycle: limits the change of the duty cycle per update.

Additionally several protections are implemented by software, which leads to a system shut down:

- Output voltage protection: If the measured output voltage is over a given protection, threshold then a shutdown will be triggered.
- Input current protection: If the measured input current value is over a given protection, threshold then a shutdown will be triggered. Particularly this protection can be separately defined for output voltage ramp up and tracking.
- Overload: if the system detects that the average output voltage falls below a given value then this protection will be triggered.

4.2 XMC™ implementation

In the next sections, the implementation carried out on the XMC1300 and XMC1400 from software and hardware point of view is discussed.

4.2.1 Software implementation

The software has been structured in different layers in order to preserve modularity and easy hardware access as follows:

- The lowest level is the hardware access, i.e. hardware registers definition.
- On top of it, XMC™ lib is used, such library implements APIs (Application Programming Interface) that simplify the interface to the peripherals.
- Dave 4 APPs are used only during initialization and helps the user to easy assign pins and initialize the peripherals, i.e.: V_{in} pin, ADC sampling time, ADC sampling order, etc.
- On the top, the initialization functions and control loop are found, which are of most interest for the final user.

Such structure with the different layers is clearly depicted in the following Figure 21.

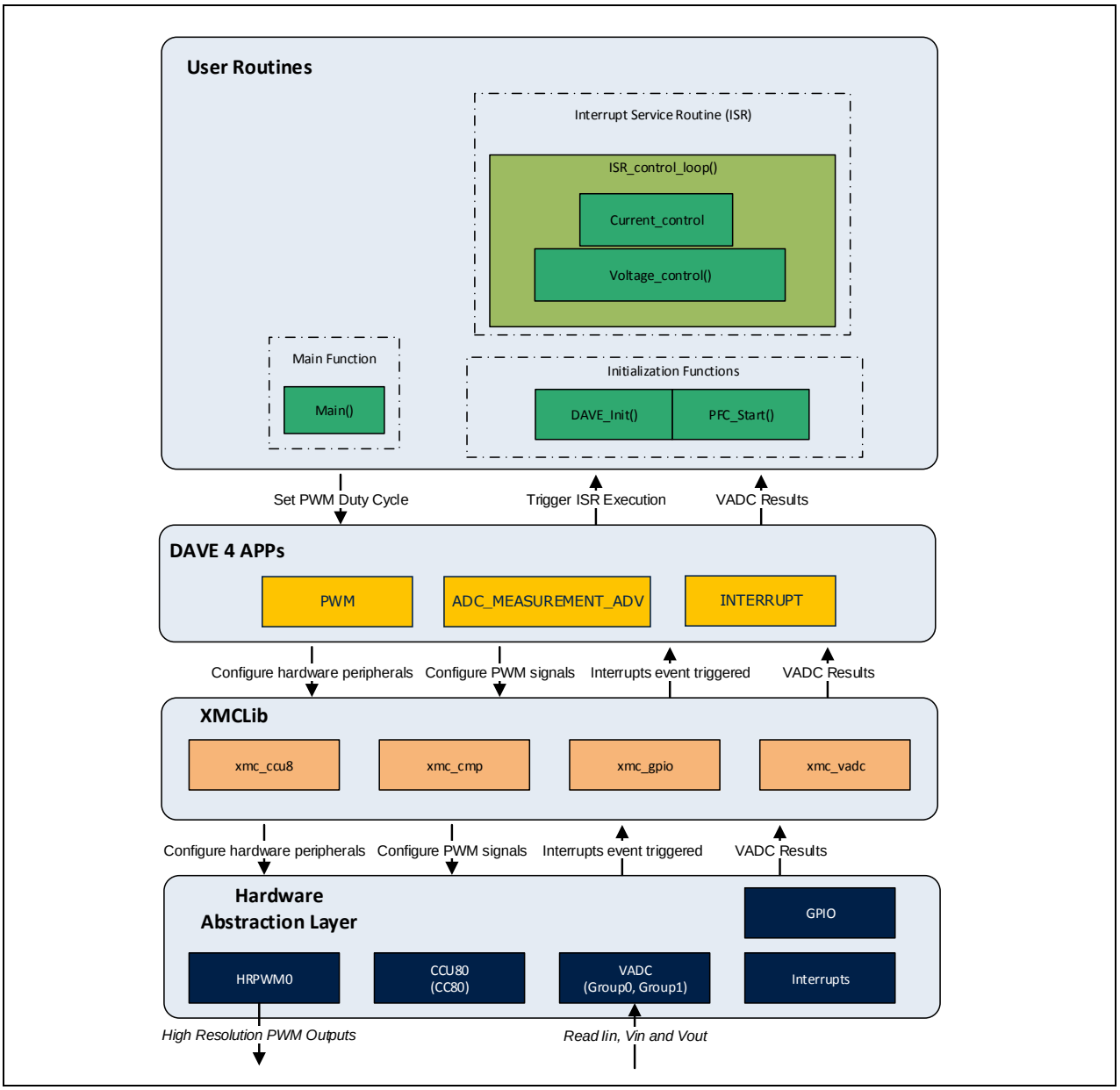


Figure 21 Software layer overview

4.2.2 Hardware usage and configuration

The implemented software on the digital control daughter card uses the next peripherals:

- Two comparators
- One Capture and Compare Unit (CCU4)
- Three ADC channels: V_{in}, I_{in} and V_{out}
- Division unit (part of MATH coprocessor)

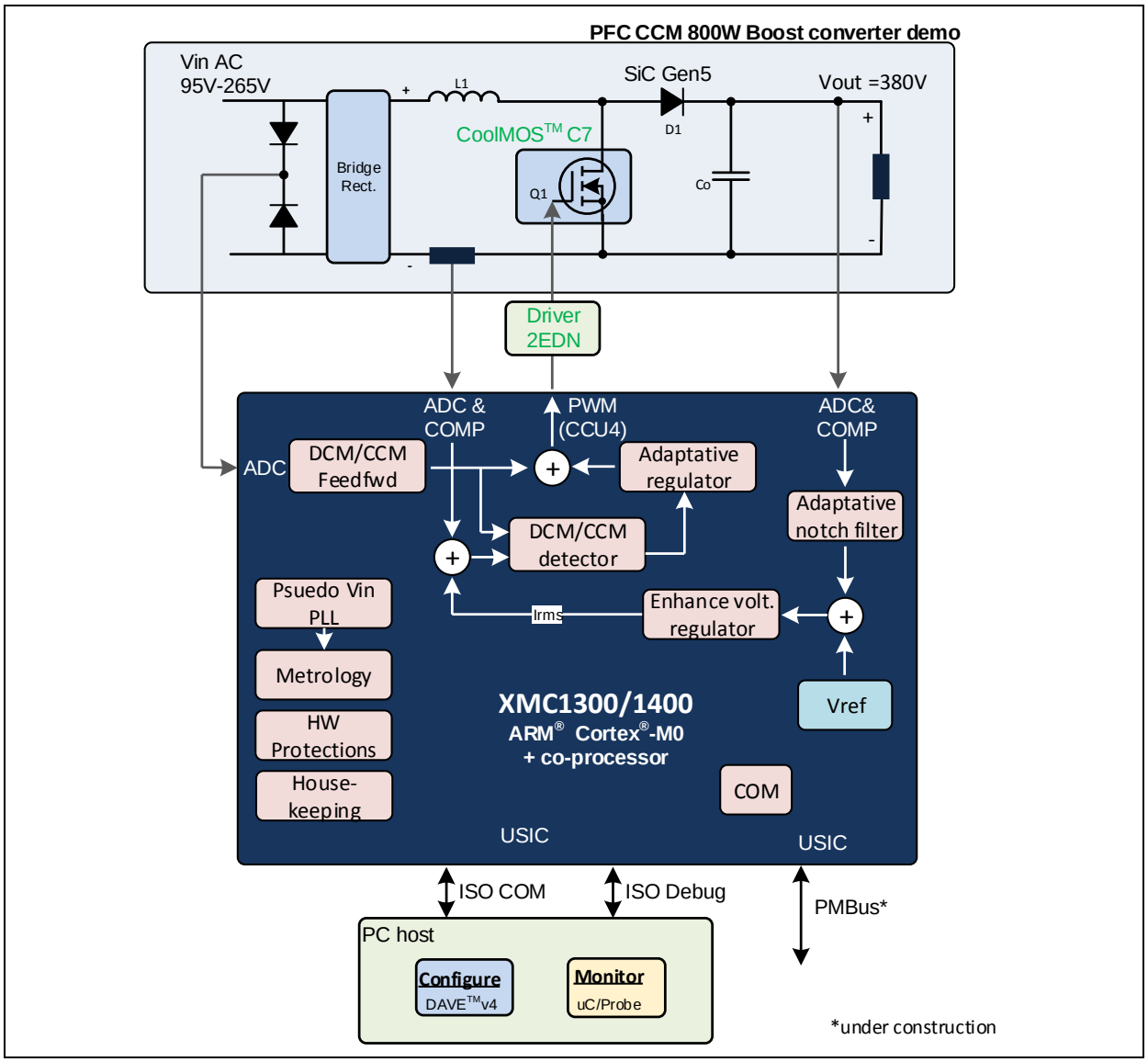


Figure 22 Interface between PFC hardware and XMC™

As can be seen in Figure 22, the two comparators are used for hardware overvoltage and overcurrent protection leading to a switch off of the gate driver when triggered. The software can check if such protection has been triggered by checking the status of the TRAP functionality.

The CCU4 unit is used for three purposes:

- Generate the PWM for the gate driver.
- Trigger the corresponding ADC conversions synchronized with PWM.
- Trigger the interrupt for the control loops.
-

The CCU4 slide 0 timer is configured in center aligned mode with a compare value that will modulate the gate driver output.

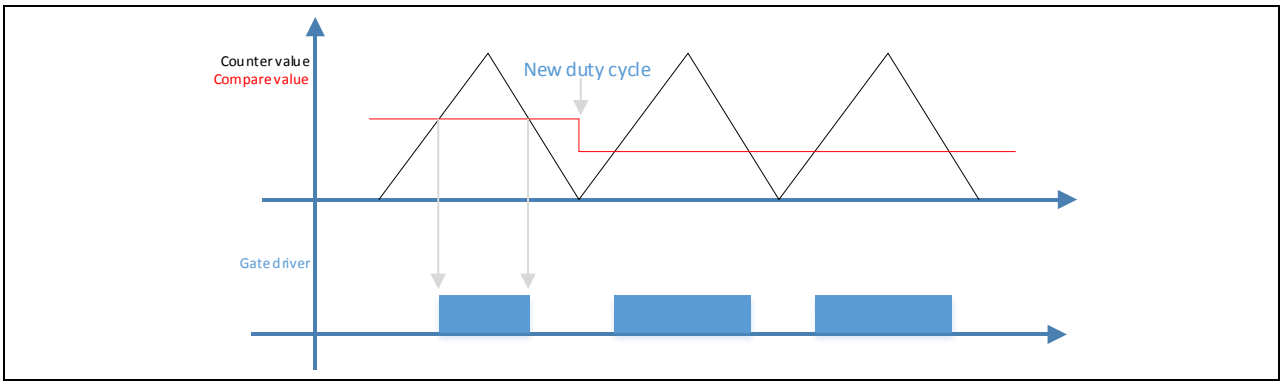


Figure 23 Gate driver modulation with CCU

The CCU4 slide 3 timer is used to trigger an interrupt periodically and synchronized with the switching frequency. Particularly, the interrupt is generated every 4 switching cycles, this is a value that will determinate how often the control loop is executed and will influence in a great manner the CPU usage and the regulation speed.

4.2.2.1 ADC configuration

It is very important to synchronize the ADC conversions with the switching frequency to ensure that conversions do not happen while the MOSFET is switching, that will minimize the possible noise couple on the target signal.

There are three signals to be converted:

- Input voltage
- Output voltage
- Inductance current

The trigger for the conversion is done by a zero match of the CCU40 as shown in Figure 24.

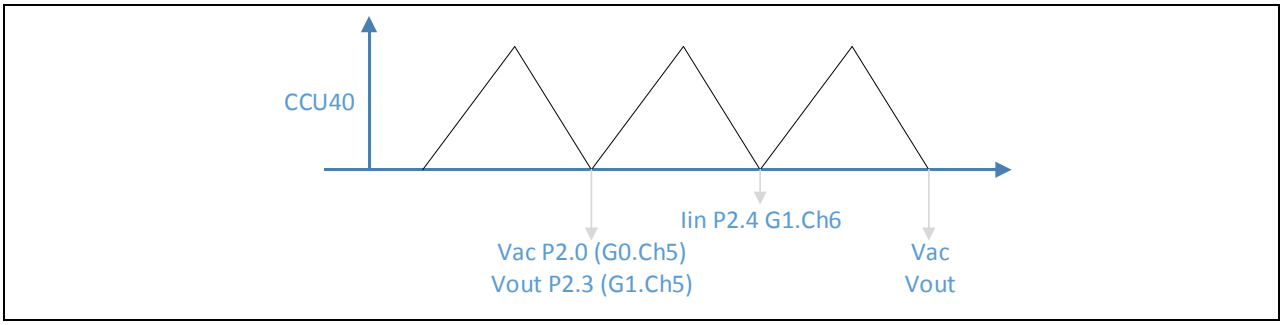


Figure 24 ADC configuration

The protections using comparators, the PWM generation and ADC conversions are handle in the peripherals autonomously without intervention of the CPU.

Another important hardware configuration is the CPU and peripheral clock. In the implementation the CPU clock is running at 32 MHz while the peripheral clock runs at 64 MHz which allows good resolution for the PWM.

4.2.3 PFC state machine

The PFC track its status with a state machine, the initial staus is “IDLE”.

Upon a call to the ***SW API PFC_Start()*** the status changes to “Start request”, as soon as the voltage is over the brown-in threshold the status changes to “soft start” and the gate driver starts sending pulses to bring the output voltage to its target, during this time an extra current is required to charge the output capacitor.

Once the output voltage reference reaches its target the status is changed to “tracking”.

The status may change to ***IDLE*** by calling the ***API PFC_Stop(idle)*** in case it needs to be switch off by software. Any protection feature will stop the PFC and change its status to the detected failure to report the error.

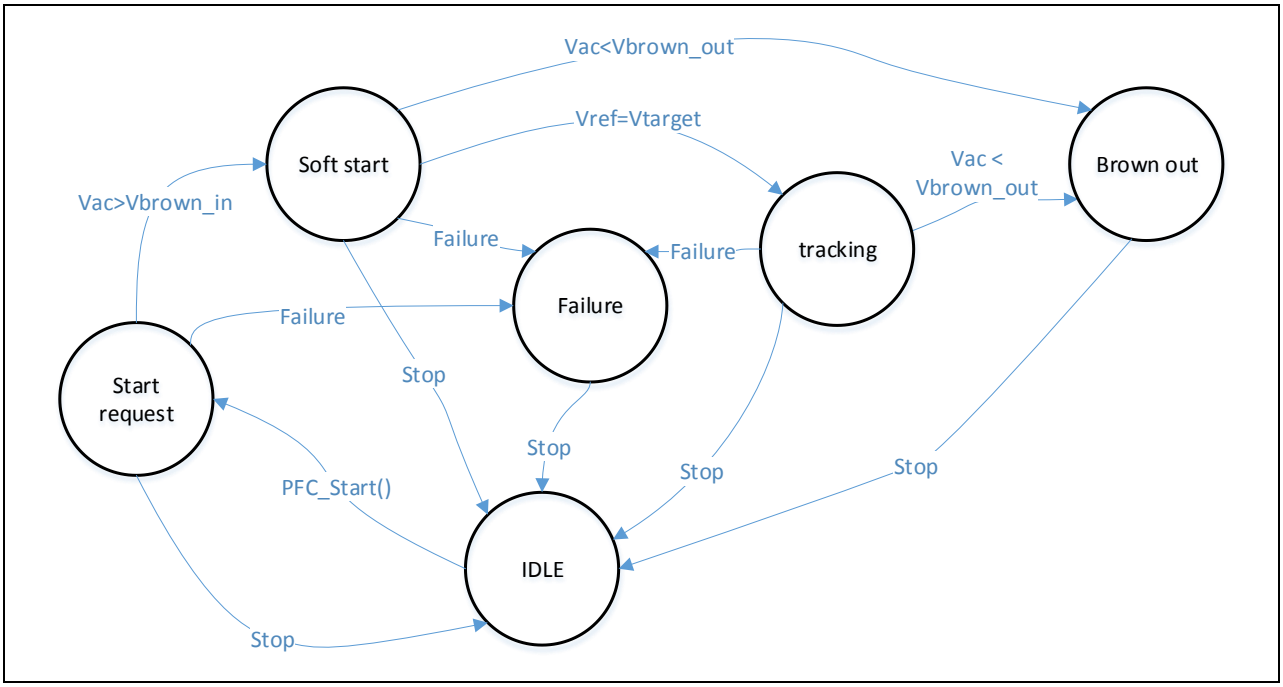


Figure 25 PFC state machine

4.2.4 Interrupt usage and tasks distribution

There are several different tasks which need to be carried out, all of them related to PFC regulation algorithms, limits and protections which are part of the module layer, most of them need to be executed in regular basics, and those are:

- @ 32 kHz
  - Current loop
- @ 4 kHz
  - Voltage loop
  - Pseudo PLL
  - Update DCM base duty cycle 1
  - Notch filter
  - Non-linear gain for voltage loop
  - Protections flags checks and other functionality
  - Update DCM base duty cycle 2

There is a single interrupt which handles all the tasks described above, such interrupt is triggered every fourth switching cycle, that means at 32 kHz. The current loop is executed every time the interrupt is triggered, the rest of the tasks are executed one out of eight times the interrupt is called, meaning with 4 kHz frequency.

Slot seven is not used.

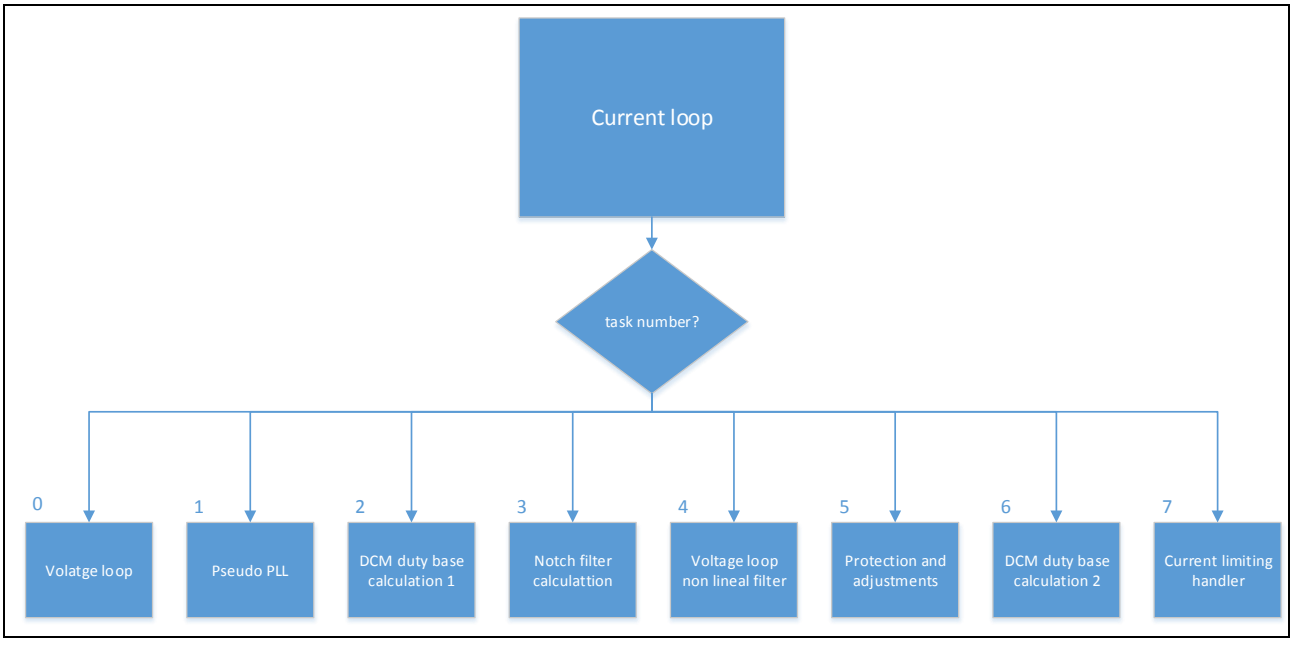


Figure 26 Software tasks distribution

This kind of tasks distribution will ensure a synchronized and time controlled response together with an even distribution of the CPU load.

4.2.4.1 Current loop

The function of the current loop is to ensure that input current follows the reference given by the voltage loop. It is executed when the PFC status is in tracking or soft start only. Inside the control loop a software check for the current protection is done. During the start phase a special case can happen, the input voltage can be bigger than output voltage due to the diode bridge voltage drop (i.e. at the peak of the sine wave), during such time a minimum duty cycle is applied until the output voltage is bigger than the input voltage.

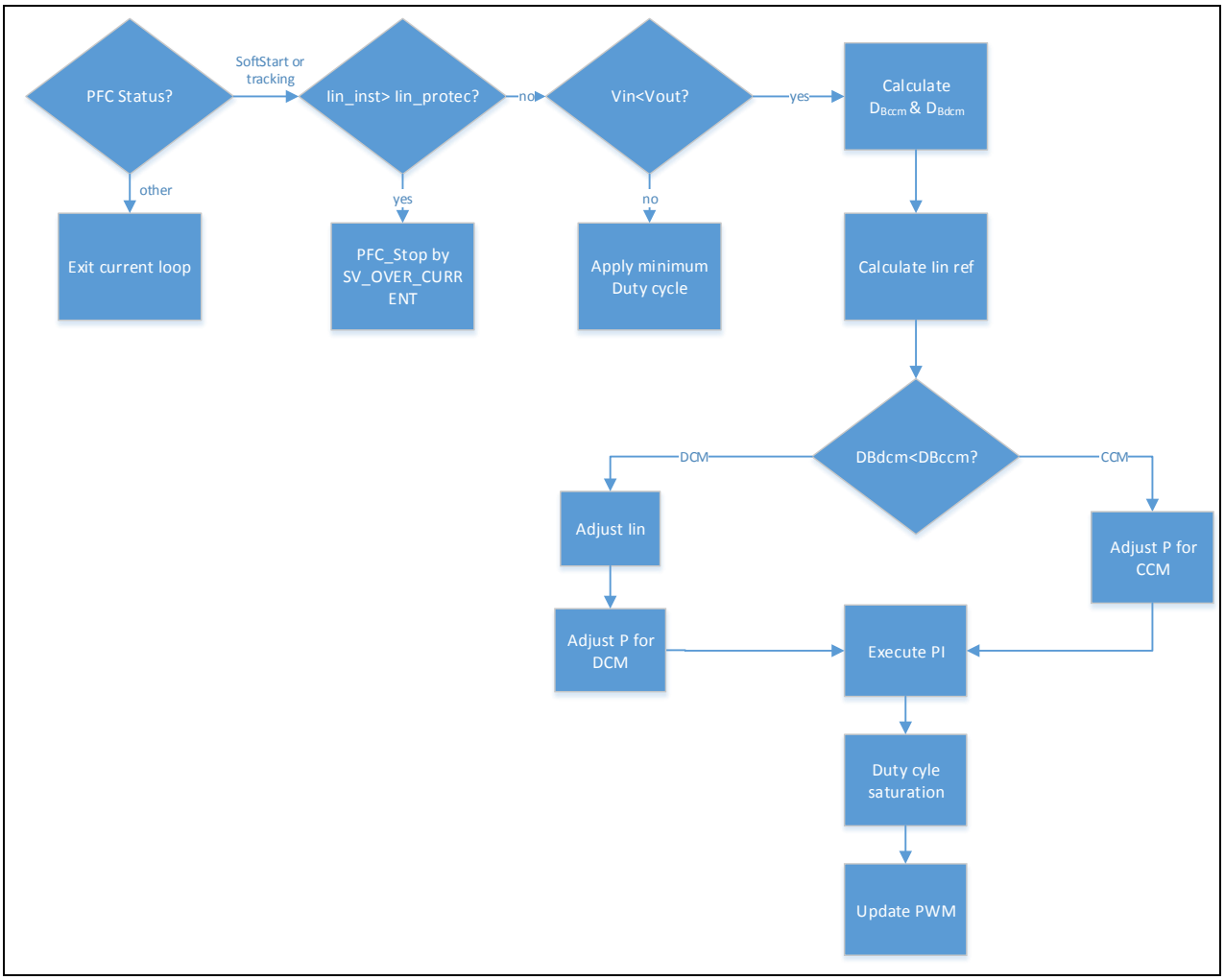


Figure 27 Current loop block diagram

4.2.4.2 Voltage loop

The voltage loop will take care of the setting of the required instantaneous current as a reference for the current loop.

Due to the fact that the output capacitor value used is high in order to keep low ripple and the corresponding hold time, the nature of the voltage loop in a PFC is slow. Therefore, the execution frequency of the control loop is chosen to be 4 kHz.

Special care has to be taken into account during start up to allow a smooth voltage ramp the reference is slowly incremented from the current value of the output voltage at the time the request to start is done until the desired output voltage target.

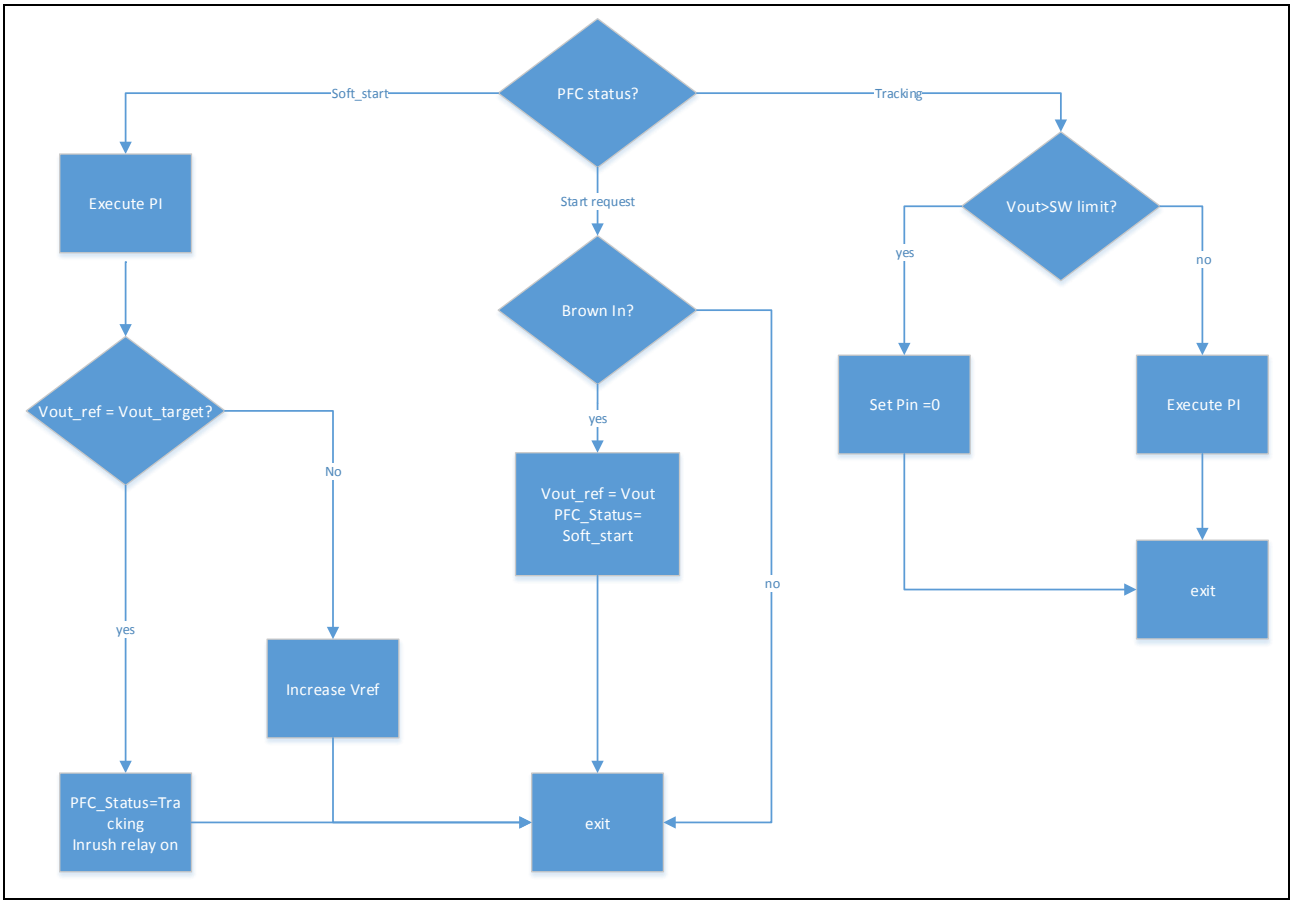


Figure 28 Voltage loop block diagram

4.2.4.3 Pseudo PLL

The pseudo PLL implements a detection of the zero voltage crossing at the input voltage in software, since XMC™ only sees a rectified value of V_{AC}, it is needed to detect when the voltage is at its lower value.

To carry out such task, three values of the input voltage are kept, as depicted in Figure 29. A zero crossing is detected when the middle sample is lower than the two adjacents and below a give value (in our case 25V) which depends on the sampling frequency and maximum V_{AC} RMS

Every time a zero crossing is detected the average value of the input voltage and its frequency are calculated, the RMS is extracted by multiplying the average value by a factor (RMS value/average value ~ 1.11).

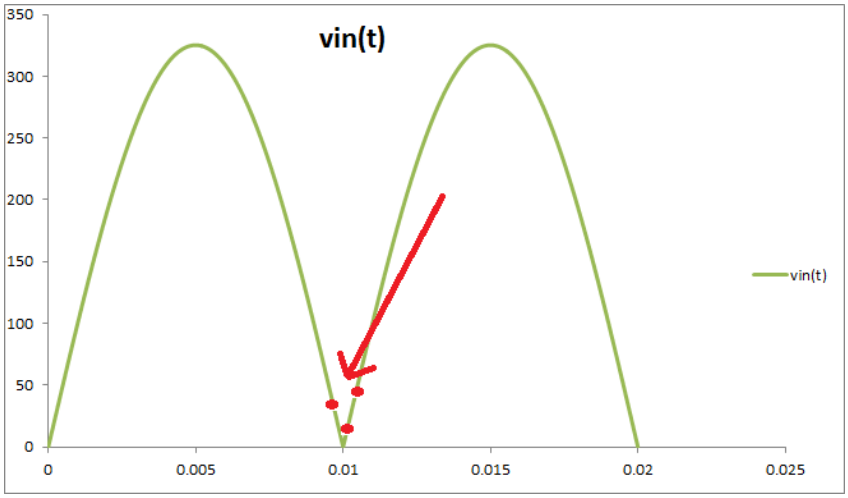


Figure 29 Rectified AC wave

4.2.4.4 Voltage loop non-lineal gain

The non-linear filter just increases the proportional part of the *PI* voltage loop regulator linearly when the output voltage exceeds certain value.

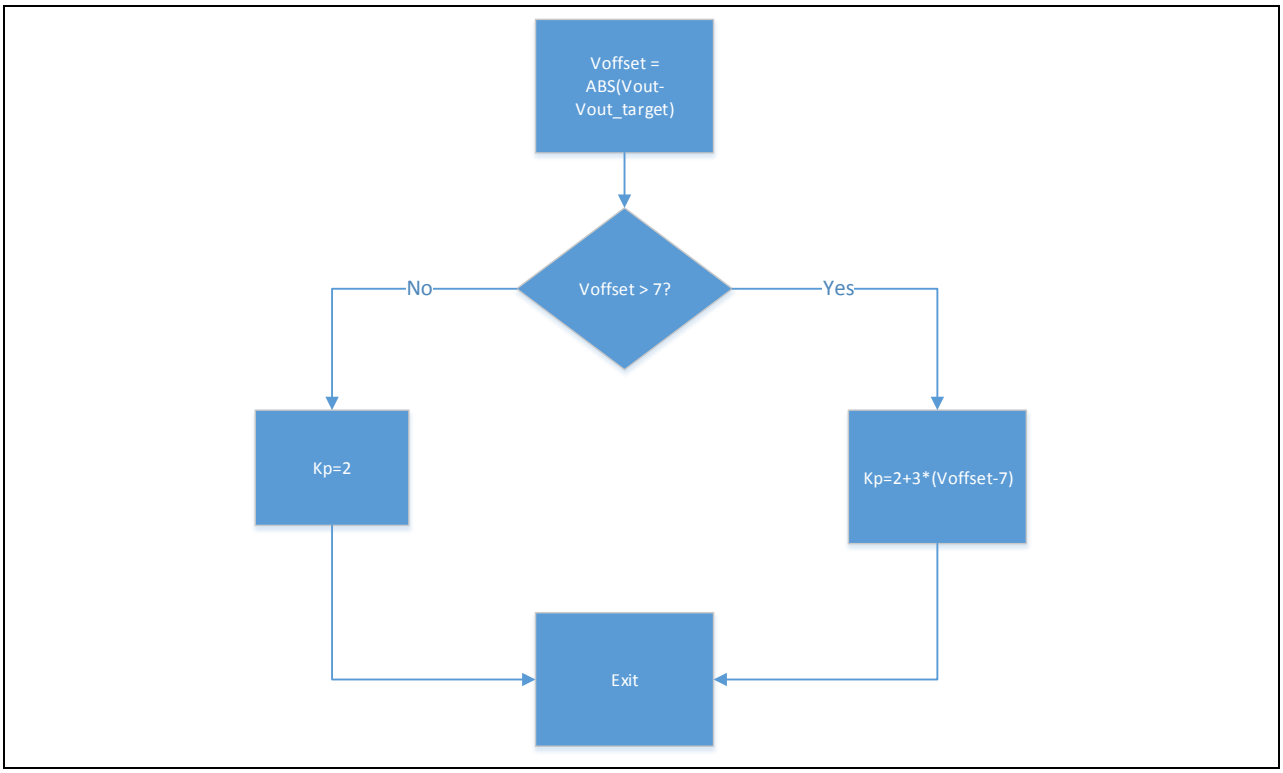


Figure 30 Non-linear gain for output voltage

4.2.4.5 Protections and adjustments

When critical protections are detected by hardware then the gate driver is switched off (e.g. output OVP and inductance OCP). If a hardware protection happens a flag is raised to inform the software.

The software regularly checks, task 5 in Figure 26, whether any software protection has occurred or any flag from hardware protections is active. If so, then the MOSFET is switched off and the status is changed accordingly.

In this section of the software the next protections are checked:

- Hardware:
  - Output OVP
  - Inductor OCP
- Software:
  - Over temperature pin
  - Brown out
  - SW output OVP (average voltage over given threshold)
  - SW overload (output voltage average below given threshold)

In this same section of the software, an adjustment of the ***PI*** current loop gain used in CCM is done in order to correct the dependency with the output voltage to compensate for the plant variations, Equation 4-10.

4.2.5 Software header file

Not only is the major reason to use a digital controller for easy integration of communications in power conversion applications but also because the software can be adapted and customized to specific hardware.

In the software development, it is intended to keep a generic approach without fine tuning specific points to enable an easy porting of the code to a new system.

Nevertheless, certain values need to be change depending of the hardware.

The header file is split in the next sections:

- Hardware parameters
- PFC parameters
- Limits and protections
- Correction factors
- Others

4.2.5.1 Hardware parameters

Here the following parameters are stated:

- Input voltage divider: AC input voltage divider ratio.
- Output voltage divider: DC output voltage divider ratio.
- Input current divider: Input current to voltage ratio.
- Inductance @ 0 A: inductance value in µH @ 0 A.
- Inductance derating: represent the inductance value decrease with current in µH/A.

- MOSFET effective output capacitance, time related $C_{o(tr):}$ approximate MOSFET $Co_{(tr)}$ value in pF (this value can be adjusted to increase I_{THD} performance)

4.2.5.2 PFC parameters

In this section, the following parameters are stated:

- PFC switching frequency
- Brown In
- Brown Out
- Target output voltage
- In-rush relay switch on delay: in number of cycles from first gate pulse
- Output voltage ramp up slope in V/sec
- Voltage loop regulator parameters:
  - Kp in Watts/V
  - Ki in Watts/(V × sec)
  - Non lineal filter threshold offset
  - Non lineal filter Kp factor
  - VOUT_OFFSET_MAX: limit the maximum Kp used
- Notch filter enable/disable switch
- Current loop Kp factor
- Current loop Ki
- Input RMS voltage sample average: useful adjust reaction time to brown out

4.2.5.3 Limits and protections

Here the following parameters with pre-defined set values are stated:

- Software instantaneous input current protection: 25 A
- Software instantaneous input current limit: 17 A
- Software input current RMS limit: 17 A
- Software output voltage limit: 410 V
- Software output voltage OVP: 430 V
- Software input conductance limit (Irms/Vrms): 0.35 A/V
- Software overload voltage threshold: 0 V, not active
- Software power limit: 1300 W
- Maximum Soft Start time: 600 AC half cycles
- Maximum delta duty cycle: 0.06
- Maximum duty cycle: 0.97
- Minimum duty cycle: 0
- Hardware cycle by cycle input current limit: 19.94 A
- Hardware input over current protection: 24.24 A
- Hardware output voltage protection: 450 V
- Hardware over temperature protection: 90°C

- Any triggered protection will lead to a latch of the system. A GUI based on uC-Probe is available to read the status and metering values of the PFC.

4.2.5.4 Correction factors

Several system offsets are adjusted here:

- Input current sense offset: partially correct current sense offset due to filtering.
- *GD ON_OFF* delay correction: correct delays in the gate driver.
- Duty base correction factor.
- Brown In correction: may correct hardware imprecisions.
- Duty cycle delta DCM/CCM gain: apply CCM compensator gain when D_{Bccm} < (D_{Bdcm} + this value) to ensure that DCM gain is not applied while CCM mode occurs.

4.2.6 Guide to adapt the software to a new design

Adapting the software to a new board requires changes on the header file, besides of the hardware resources assignment in case different pins are used. In this section, some points that may need special care when modifying the header file are analysed.

A set of parameters that needs to be adapted in any case are those related to the board, i.e. hardware parameters.

From the hardware parameters, there is one which needs to be trimmed for I_{THD} improvement at high input current values: ***MOSFET_CO_TR_pF***. Its value is highly linked with the MOSFET output capacitance time related parameter, this value will help to improve I_{THD} at zero crossing as explain in 4.1.2.2.

PFC_INDUCTANCE_DERATING_uH_A could be increased if oscillations are observed at the top of the sine wave; this will decrease the compensator gain with increasing current values.

Another important factor to avoid DCM operation while system is in CCM is ***DUTY_BASE_CORR_FACTOR***; such factor as well ensures the right base duty cycle for CCM, (theoretically 1). Such factor defines the threshold used by the software to apply DCM duty base and the change of gain for the compensator proportional part.

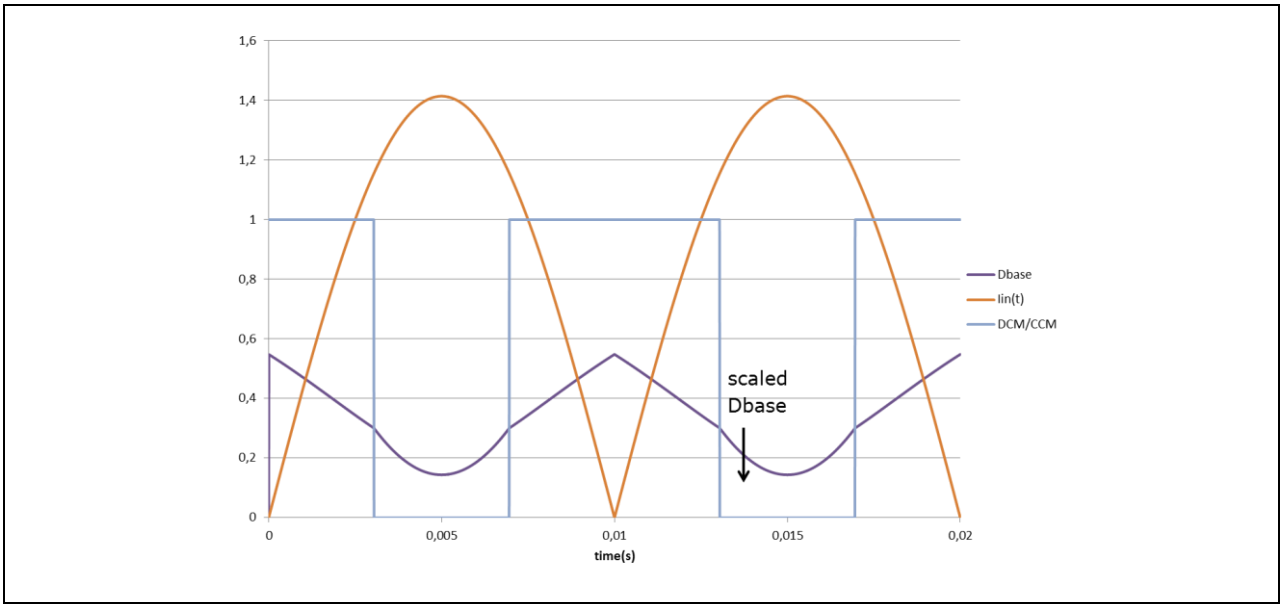


Figure 31 Duty base correction factor effect

By decreasing the correction factor, the crossing point between DCM and CCM will be closer to the zero crossings and so enlarging a bit the CCM duty cycle base and gain.

The last parameter that needs particular attention in order to ensure that a DCM gain of the compensator is not used during CCM operation is: ***DCYCLE_DELTA_CCM_DCM_GAIN***, as explained in Figure 17, if oscillations are observed during the transition from DCM to CCM this parameters should be increased or the inductance value should be corrected.

Overall parameters to trim the current loop ***PI*** are:

- ***CURRENT_LOOP_Kp_FACTOR_CCM***: defines the gain factor for CCM operation mode
- ***CURRENT_LOOP_Kp_FACTOR_DCM***: defines the gain factor for DCM operation mode (only integer values are allowed)
- ***CURRENT_LOOP_Ki***: integrative part for the current loop.
- ***V_LIMIT_I_PI_GAIN***: this value limits the maximum gain of the compensator during DCM by adding a constant value to V_{in} in Equation 0.
- The Brown out reaction time and filtering of possible voltage drops can be adjusted with the number of samples used in the cumulative moving average filter for V_{in} RMS: ***VIN_RMS_AVG_FACTOR***, the bigger the factor the slower the reaction time will be.
- ***N_CYCLES_SKIP_ILOOP***: Determines how many switching cycles will be between the updates of the current loop. Executing the current loop too often may lead to saturation of the CPU, therefore a 32 kHz update rate is advised.

4.2.7 Signaling and protection

Three LEDs on the control board display operating conditions and errors:

- The orange LED indicates a brown out condition. LED turns on when brown out happened (V_{in}<80 V), and turns off when brown in happened (V_{in}>86 V).
- The green LED indicates the presence of V_{out} at the output. The LED turns on after the soft start phase once V_{out} is greater than 376 V and turns off when the system stops due to brown out or failure.
- The red LED indicates over-current or overvoltage protection.

As a reference, the programmed system settings are:

- Output voltage: 380 V
- Brown in: 86 V
- Brown out: 80 V
- Switching frequency: 128 KHz
- NTC relay switch on: after 10 half AC cycles
- Start up voltage ramp: 420 V/s

4.3 Firmware downloading and debugging

The firmware implementation with all digital control features explained in the previous section was downloaded and debugged using Infineon Technologies Debug Probe XMC™ Link.

XMC™ Link is an isolated debug probe for all XMC™ microcontrollers. The debug probe is based on SEGGER J-Link debug firmware, which enables use with DAVE™ and all major third-party compiler/IDEs within the wide ARM® ecosystem.

The main features are:

- 1 kV DC isolation
- Debug protocols
  - JTAG
  - Infineon's Single Pin Debug (SPD)
  - Serial Wire Debug (SWD)
  - Serial Wire Output (SWO)
- Virtual COM port support
- 10-pin Cortex® debug connector
- 8-pin XMC™ MCU debug connector
- 2.5 V to 5.5 V target voltage operation

Please refer to Section 8 for further information about this debug probe.

5 ICE2QR4780Z controllers for auxiliary converter

5.1 Input and output requirements

The voltages needed to supply the control circuitry and the fan is provided by the dedicated flyback DC-DC converter ICE2QR4780Z, which is assembled on the power board. The DC-link voltage supplies such converter.

Table 5 Input / Output requirements

Parameter	Value
Input voltage range, V_{in_range}	125 V_{DC} – 450 V_{DC}
Nominal output voltage, V_{aux_pri}	12 V_{DC} +/-10%
Nominal output voltage, V_{aux_sec}	12 V_{DC} +/-10%
Maximum output Power, P_{out}	6 W

5.2 Flyback transformer

The transformer design is based on a gapped ferrite core EE 16/8/5 with a horizontal arranged bobbin. The total air gap is 0,2 mm. The selected core material is TDK N87 or equivalent.

The turns ratio was chosen to be 184:15:15, resulting in 150 V (approximately) reflected primary transformer voltage.

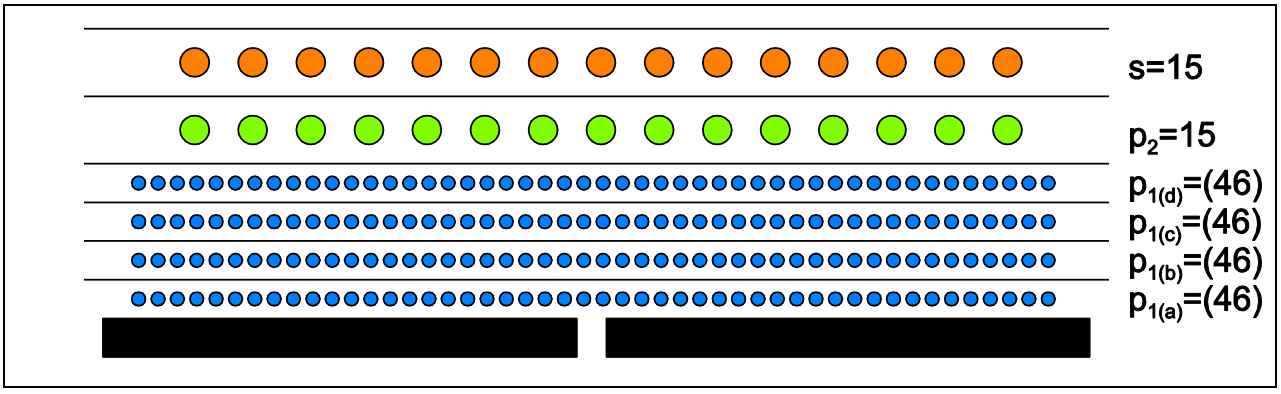


Figure 32 Winding arrangement

The secondary winding (S) has safety insulation from primary side, which is implemented using triple insulated wire. The other windings are made of standard enameled wire. The high voltage primary winding (P1) is split in to 4 layers.

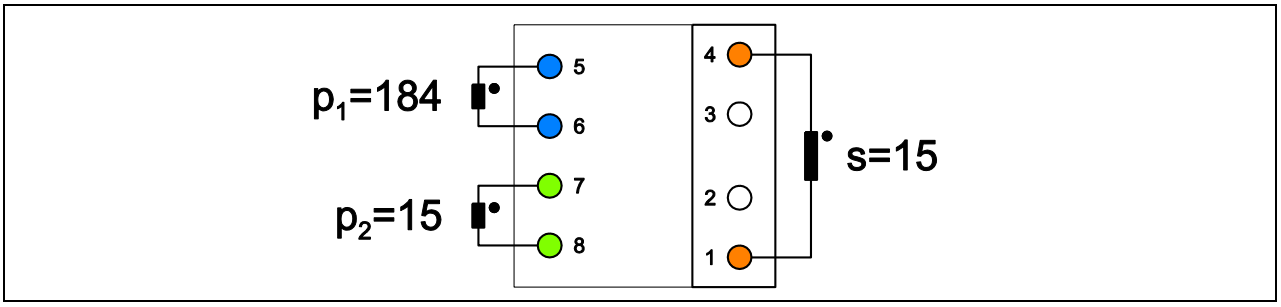
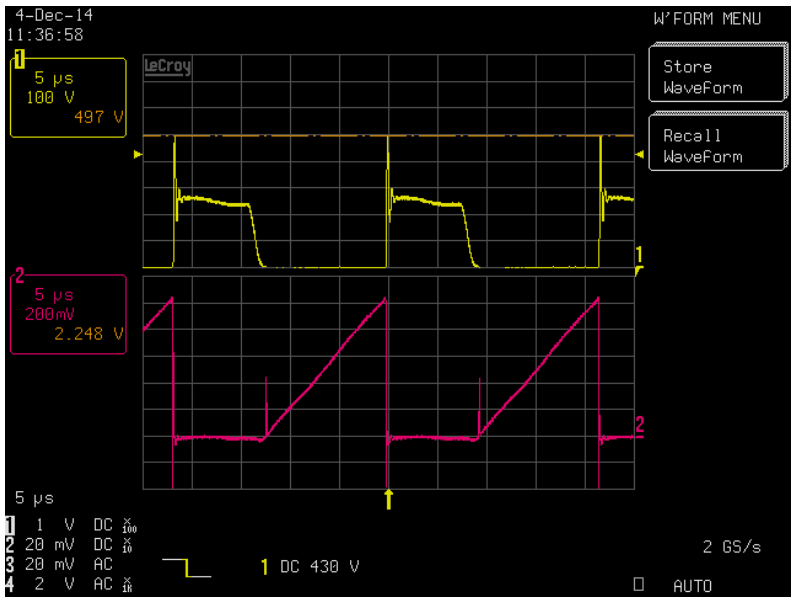


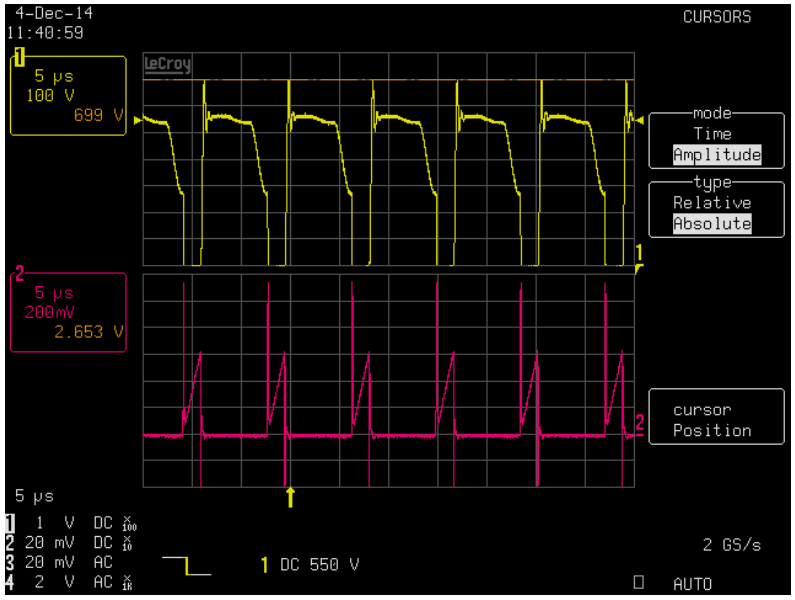
Figure 33 Pin arrangement, top view

5.3 Switching frequency

The ICE2QR4780Z is a Quasi-Resonant PWM Controller with integrated 800 V CoolMOS™. The switching frequency depends on load power and input voltage and is between 40 kHz and 130 kHz.



- V_{in}=100 V_{DC}
- CH1-Drain-Source Voltage
- CH2-Shuntvoltage (R3,9Ω)



- V_{in}=400 V_{DC}
- CH1-Drain-Source Voltage
- CH2-Shuntvoltage (R3,9Ω)

Figure 34 Characteristics of auxiliary power supply

6 Experimental results

6.1 ICE3PCS01G IC control

6.1.1 Efficiency at low and high Line

Efficiency measurements were carried out with a “WT330” Yokogawa digital power meter. Losses of the EMI-Filter are included. The fan was supplied from an external voltage source.

Table 6 Efficiency measurements

P_{load} [%]	V_{in}[V]	I_{in}[A]	P_{in}[W]	V_{out}[V]	I_{out}[A]	P_{out}[W]	η[%]	PF	iTHD (%)
10	115,14	0,7184	81,69	379,88	0,2015	76,56	93,72	0,987	7,20
20	115,07	1,4388	164,91	379,89	0,4124	156,67	95,00	0,996	5,37
30	115,05	2,1575	247,82	379,89	0,6244	237,19	95,71	0,998	3,44
40	115,03	2,8761	330,4	379,89	0,8352	317,3	96,04	0,999	2,92
50	115	3,6025	413,9	379,89	1,0474	397,8	96,11	0,999	3,21
60	114,97	4,3337	497,8	379,9	1,2593	478,4	96,10	0,999	2,97
70	114,93	5,0706	582,4	379,88	1,4719	559,1	96,00	0,999	2,59
80	114,91	5,7611	661,6	379,9	1,6696	634,2	95,86	0,999	2,64
90	114,88	6,505	747	379,89	1,881	714,6	95,66	1,000	2,49
100	114,87	7,257	833	379,89	2,094	795,3	95,47	0,999	2,92
10	230,87	0,4057	80,2	380,03	0,1998	75,9	94,64	0,857	12,83
20	230,85	0,7345	162,3	380	0,4122	156,6	96,49	0,957	10,66
30	230,84	1,0822	244,7	380,01	0,625	237,5	97,06	0,979	6,85
40	230,83	1,4293	326,3	380	0,8373	318,1	97,49	0,989	3,21
50	230,81	1,7851	408,7	379,96	1,05	398,9	97,60	0,992	2,42
60	230,78	2,1398	490,8	379,96	1,2619	479,4	97,68	0,994	2,82
70	230,76	2,4935	572,7	379,95	1,4741	560	97,78	0,995	2,62
80	230,74	2,8249	649,3	379,95	1,6717	635,1	97,81	0,996	2,34
90	230,72	3,1799	731,2	379,94	1,8833	715,4	97,84	0,997	2,56
100	230,7	3,5366	813,3	379,93	2,0954	796	97,87	0,997	2,94

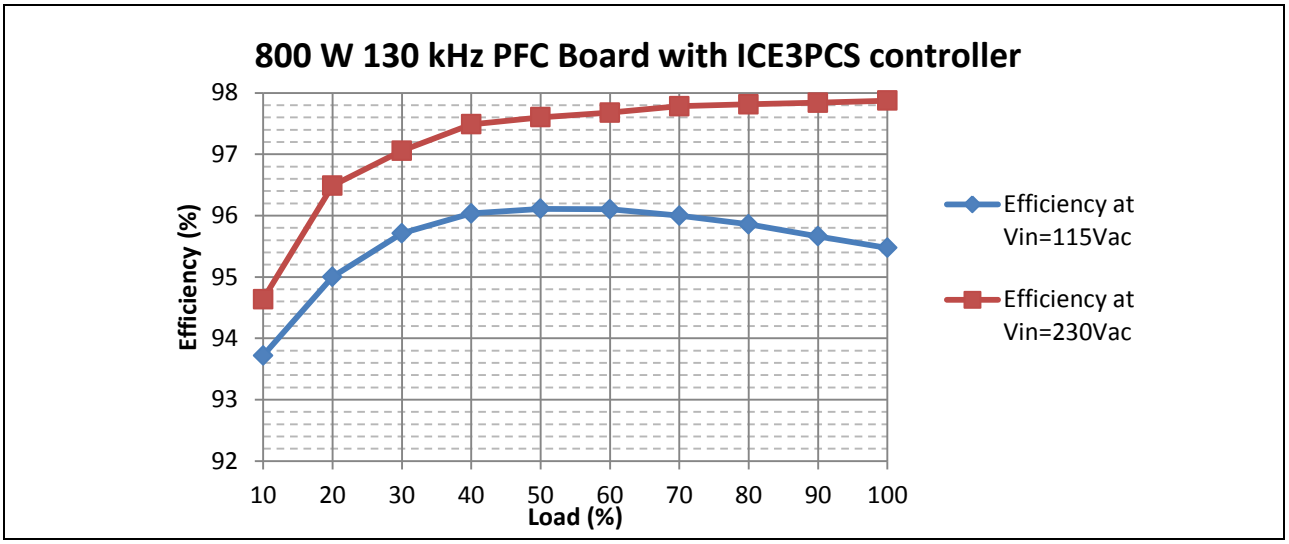


Figure 35 High line and low line efficiency with 2x IPP60R180C7 @ f_s = 130 kHz, R_{gate_on} = 15 Ω, R_{gate_off} = 39 Ω

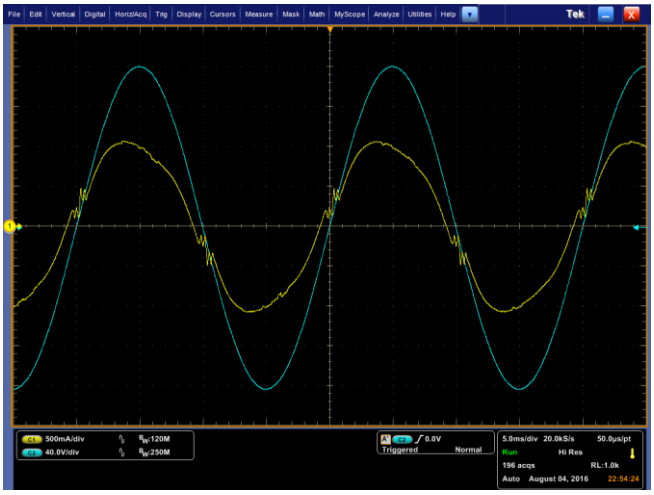


Figure 36 Input current distortion and PF for P_{OUT}=80 W at V_{IN}=115 V_{AC} with analog control

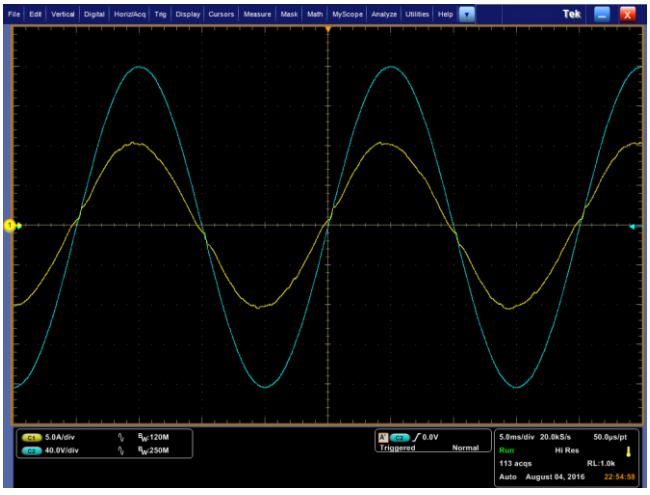


Figure 37 Input current distortion and PF for P_{OUT}=800 W at V_{IN}=115 V_{AC} with analog control

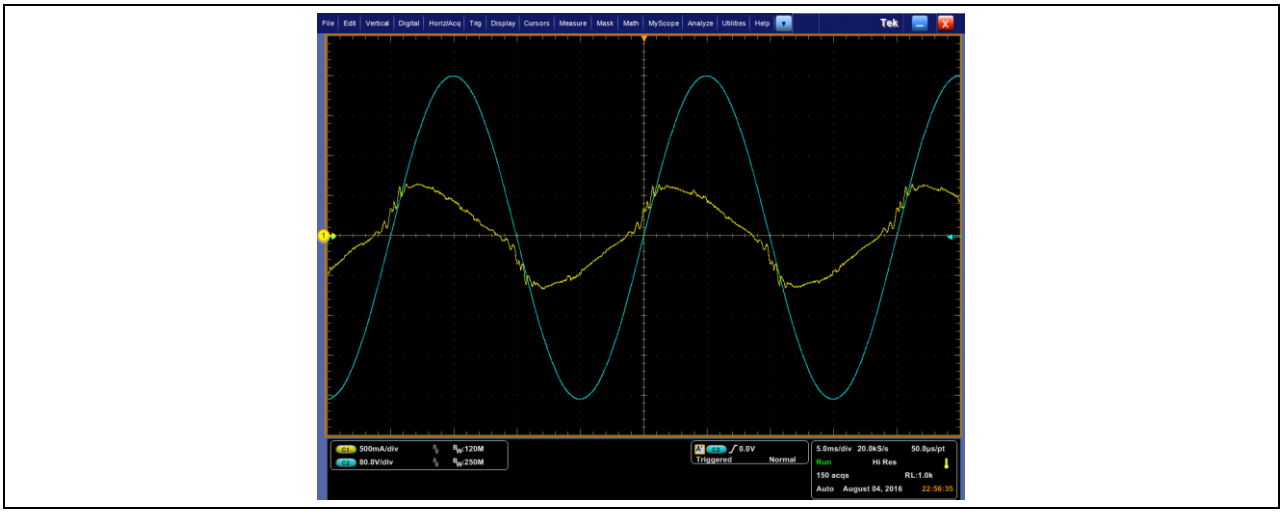


Figure 38 Input current distortion and PF for P_{OUT}=80 W at V_{IN}=230 V_{AC} with analog control

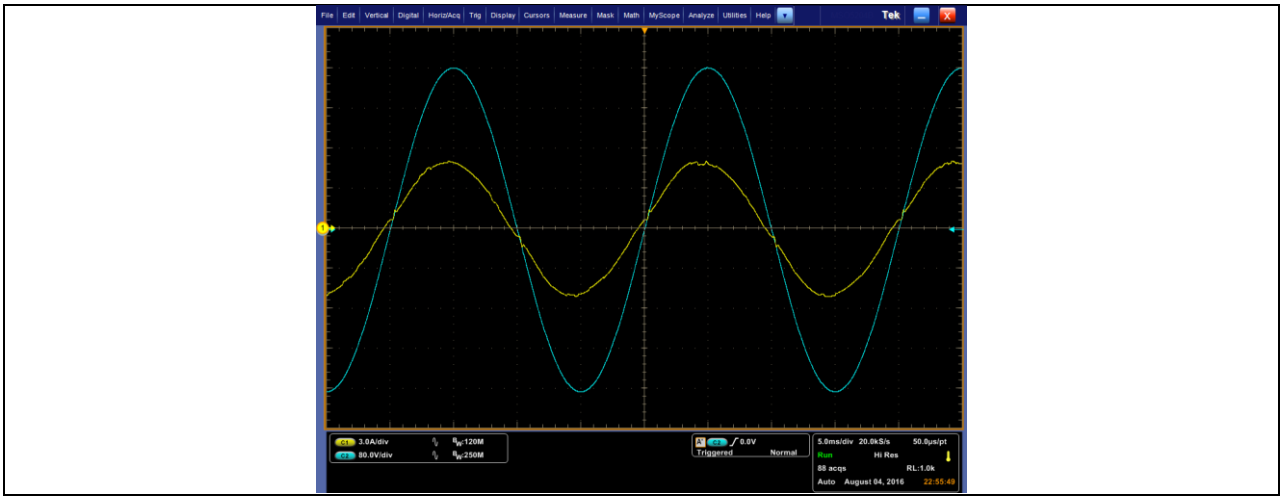


Figure 39 Input current distortion and PF for P_{OUT}=800 W at V_{IN}=230 V_{AC} with analog control

6.1.2 Standby power consumption

Measurements done with a “WT330” Yokogawa digital power meter showed the following results for standby power consumption of the demoboard at no load:

Table 7 Standby power consumption at no load

V_{IN} = 230 V_{AC}	V_{IN} = 115 V_{AC}
I_{IN} < 200 mA_{RMS}	I_{IN} < 100 mA_{RMS}
P_{OUT} < 1 W	P_{OUT} < 1W

6.1.3 Efficiency versus semiconductor stress

During the design process, there is always a trade-off between achieving high efficiency and semiconductor stress if the derating guidelines of the IPC 9592 standard are to be fulfilled. This stress depends on drain current, drain to source voltage, stray inductances of the package itself and PCB as well as the switching speed (di/dt). Depending on the requirements of the application, the designer can select the proper value of turn on and turn off gate resistors to achieve certain efficiency at a certain stress on the MOSFET.

The design for this board is very conservative in the sense that the turn off resistors for each of the MOSFETs have been chosen to be 39 Ω in order to keep the drain to source voltage below the 80% of the corresponding derating factor even at V_{IN} = 90 V_{AC} as well as to keep the ringing at the gate very low. What it worth to notice here is that even with such “big” turn off resistor values, the performance of the 600 V CoolMOS™ C7 device in the PFC demoboard is remarkable in such a way that from 20% of the load upwards the overall efficiency is >95% at V_{IN}=115 V_{AC} and >96% at V_{IN}=230 V_{AC}. Such efficiency performance is sufficient to meet the 80PLUS Platinum standard for redundant and non-redundant power supplies.

Key to the following two figures

- CH 2 (blue): Drain to Source Voltage (70 V/div)
- CH 3 (magenta): Gate to Source Voltage (5 V/div)



Figure 40 Turn off waveforms during turn off when V_{IN}=115 V_{AC} at P_{out}=800 W.

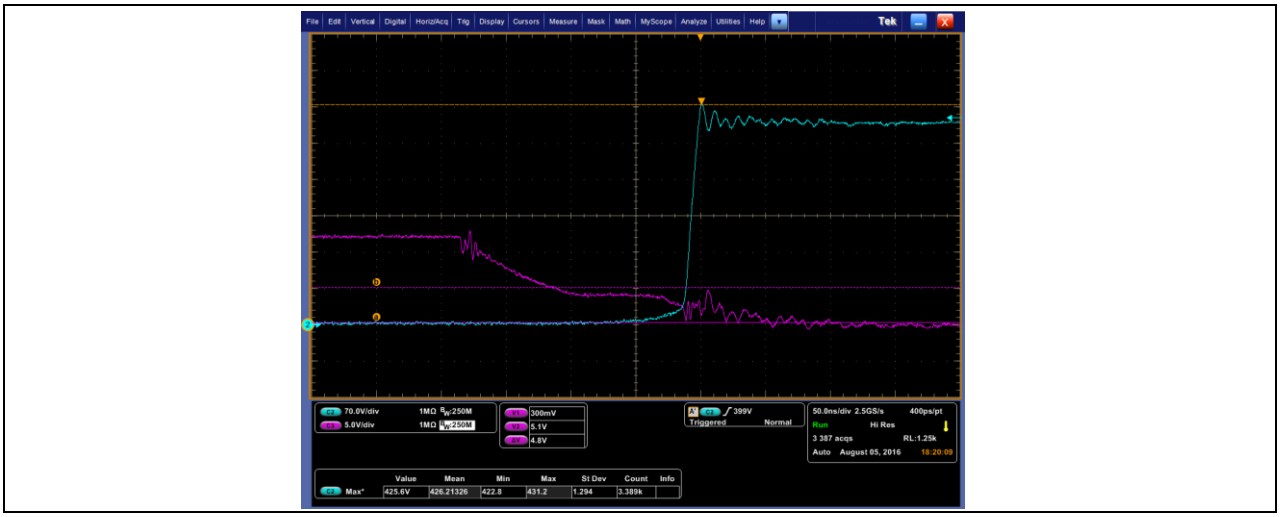


Figure 41 Turn off waveforms during turn off when V_{IN}=230 V_{AC} at P_{out}=800 W.

6.1.4 Load steps

- Channel 1 (yellow): Load current
- Channel 2 (green): PFC output voltage (with an offset of 350 V)

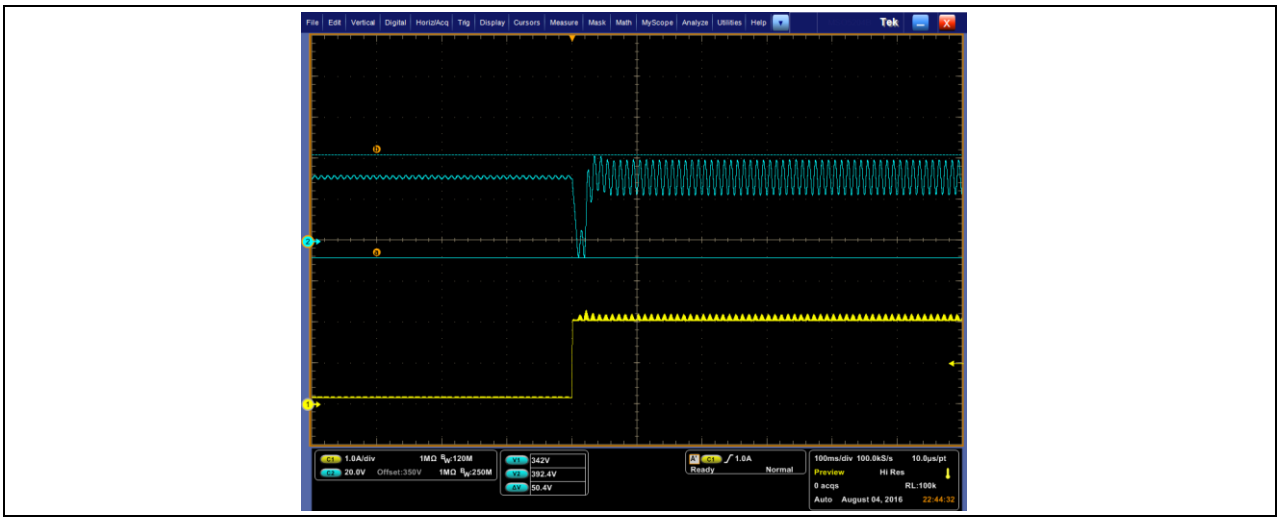


Figure 42 Load step: 10% ➔ 100% at V_{in}=115 VAC

The figure above illustrates the response of the voltage control loop during a load step from 10% of the load to full load with a voltage undershoot down to 342 V_{DC}.

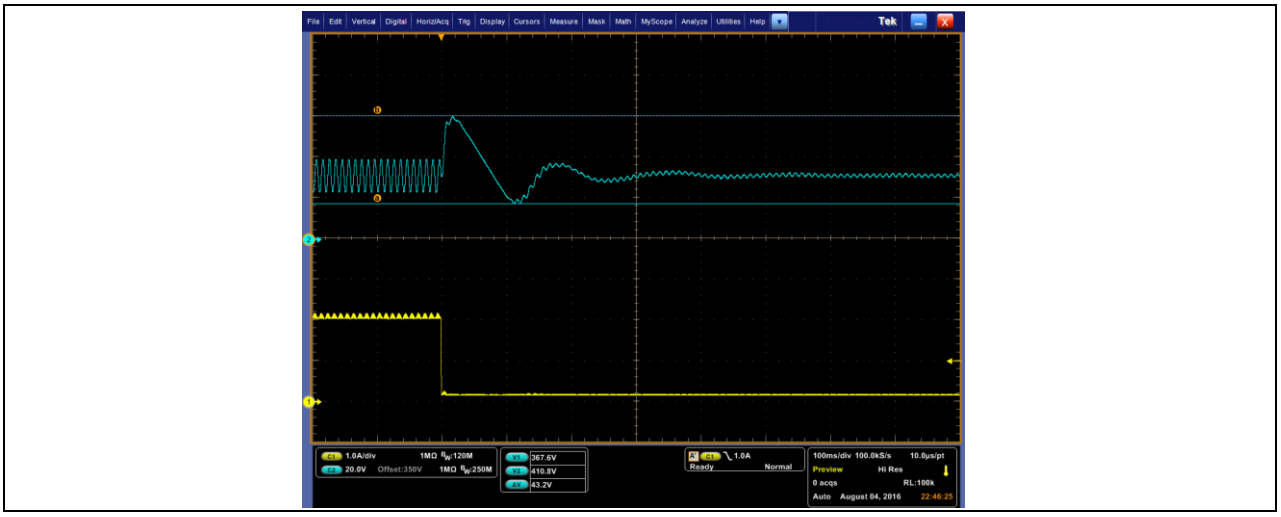


Figure 43 Load step: 100% ➔ 10% at V_{in}=115 VAC

The figure above illustrates the response of the voltage control loop during a load step from full load to 10% of the load with a voltage overshoot up to 410 V_{DC}.

6.1.5 Conducted EMI measurements

EMI is a very important quality factor for a power supply. The EMI has to consider the whole SMPS and is split into radiated and conducted EMI. For the evaluation PFC board it is most important to investigate on the conducted EMI-behavior since it is the input stage of any SMPS below a certain power range.

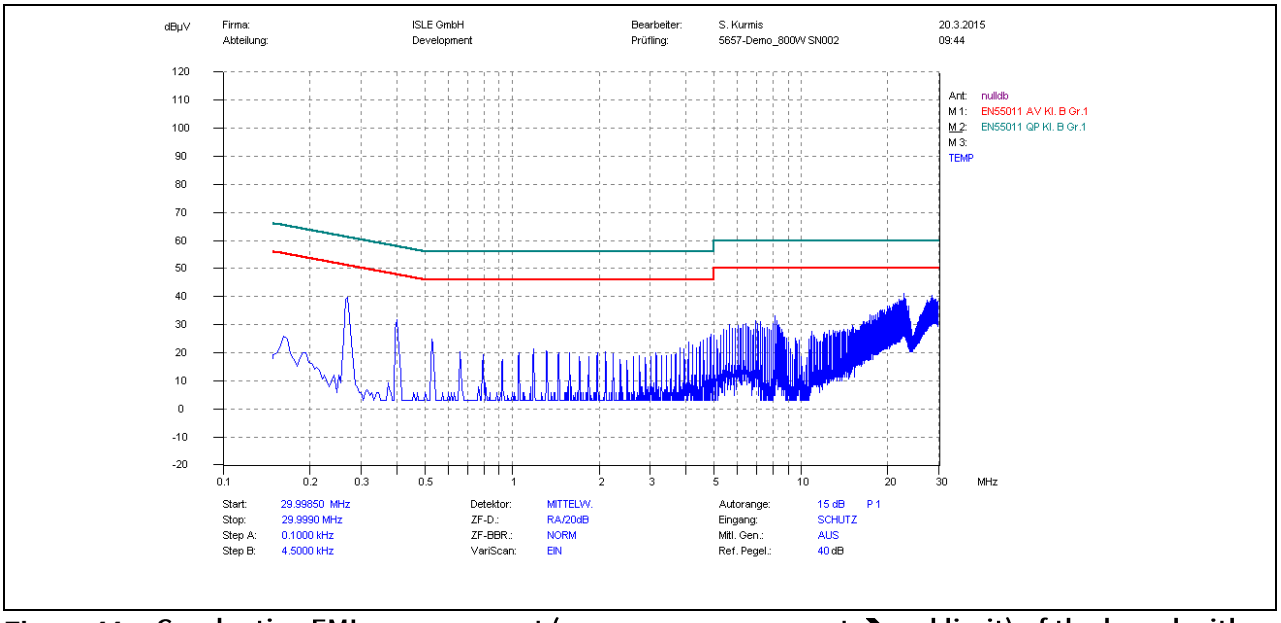


Figure 44 Conductive EMI measurement (average measurement ➔ red limit) of the board with resistive load (800 W) and input voltage of 230 V_{AC}

6.1.6 Start up

The PFC demoboard has a circuitry to limit the turn-on inrush current on the first half cycle to around 35 A_{peak}. After turning-on the system, the auxiliary supply will provide a stable voltage of 12 V. Once all circuits are powered and the input voltage is higher than the brown out threshold the PFC starts operating. The NTC-Limiter is then bypassed by the relay as long as the input current is greater than 0.2 A_{rms}; this precise moment can be clearly identified in Figure 46 and Figure 47 when the output voltage starts to ramp up.

This timing is different for the low-line and the high-line situations. For further information please refer to Infineon Technologies AN-PS0052 “Design Guide for Boost Type CCM PFC with ICE3PCS0xG” Ch. 2.14)

Key to the following two figures

- Channel 1 (yellow): Input current
- Channel 2 (blue): PFC output voltage
- Channel 3 (magenta): 12 V_{DC} from the auxiliary supply

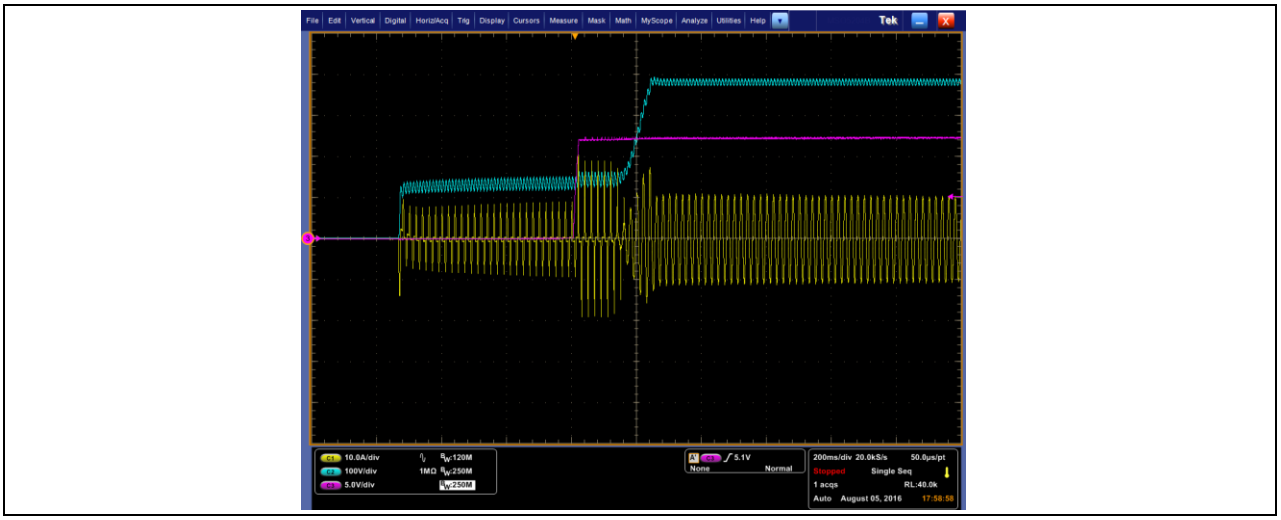


Figure 45 Start-up at V_{in}=115 V_{AC}

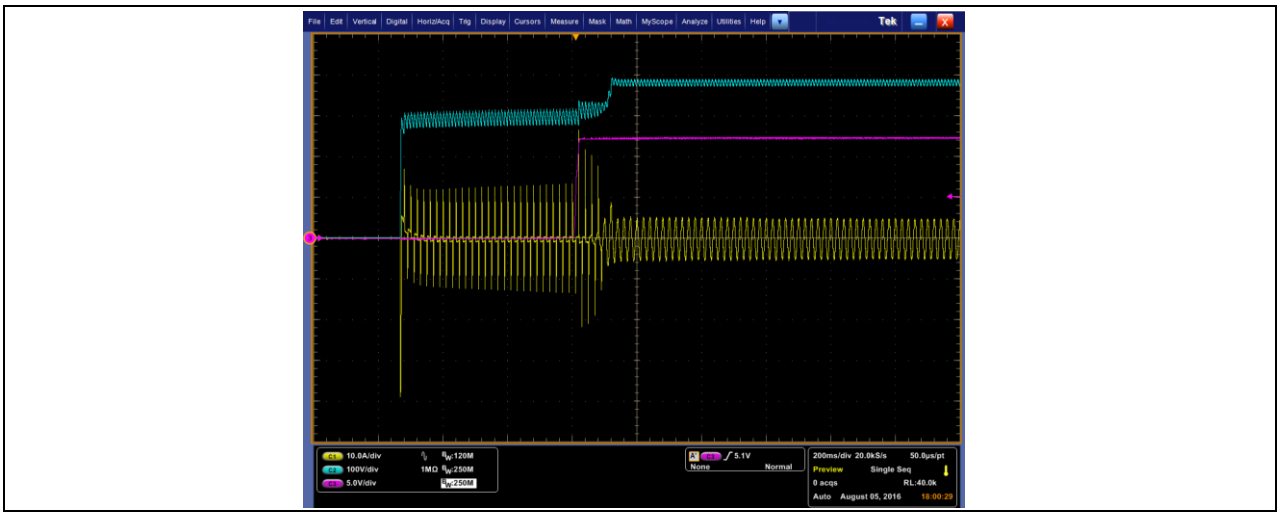


Figure 46 Start-up at V_{in}=230 V_{AC}

6.2 XMC1300 / XMC1400 digital control

6.2.1 Power factor, efficiency and input current THD

Efficiency measurements were carried out with a “WT330” Yokogawa power meter. Losses from the EMI-filter are included. The fan was supplied from an external voltage source.

Table 8 Efficiency Measurements

P_{LOAD} [%]	V_{in} [V]	I_{in} [A]	P_{in} [W]	V_{out} [V]	I_{out} [A]	P_{out} [W]	η [%]	PF	iTHD (%) XMC1300	iTHD (%) XMC1400
10	115,15	0,71	81,45	380,01	0,20	76,45	93,86	0,9909	5,32	6,02
20	115,1	1,43	164,56	380,09	0,41	156,46	95,08	0,9975	3,73	3,32
30	115,08	2,15	247,54	380,08	0,62	237,07	95,77	0,9994	1,96	1,92
40	115,05	2,87	330,4	380,09	0,84	317,4	96,07	0,9997	1,61	1,85
50	115,03	3,60	413,9	380,14	1,05	398	96,16	0,9998	1,56	1,44
60	115	4,33	498	380,15	1,26	478,5	96,08	0,9999	1,38	1,42
70	114,97	5,07	582,5	380,16	1,47	559,3	96,02	0,9999	1,24	1,31
80	114,95	5,76	661,9	380,17	1,67	634,5	95,86	0,9999	1,15	1,32
90	114,91	6,50	747,3	380,19	1,88	714,8	95,65	0,9999	1,11	1,31
100	114,88	7,26	833,6	380,22	2,09	795,6	95,44	0,9999	1,05	1,32
10	230,83	0,40	79,6	380,03	0,20	75,66	95,05	0,8644	9,80	7,85
20	230,83	0,73	161,79	380,02	0,41	156,21	96,55	0,9589	7,65	5,31
30	230,82	1,08	244,12	380,05	0,62	237,21	97,17	0,9788	7,25	4,90
40	230,81	1,43	326,06	380,06	0,84	317,84	97,48	0,9890	4,84	4,03
50	230,8	1,78	408,16	380,03	1,05	398,58	97,65	0,9917	4,44	2,91
60	230,79	2,14	490,12	380,05	1,26	479,16	97,76	0,9941	4,20	2,66
70	230,78	2,49	572,28	380,1	1,47	559,8	97,82	0,9962	3,22	2,07
80	230,77	2,82	648,7	380,1	1,67	634,7	97,84	0,9975	2,55	1,78
90	230,77	3,17	730,6	380,1	1,88	715	97,86	0,9982	2,40	1,64
100	230,76	3,53	812,8	380,14	2,09	795,5	97,87	0,9986	2,10	1,45

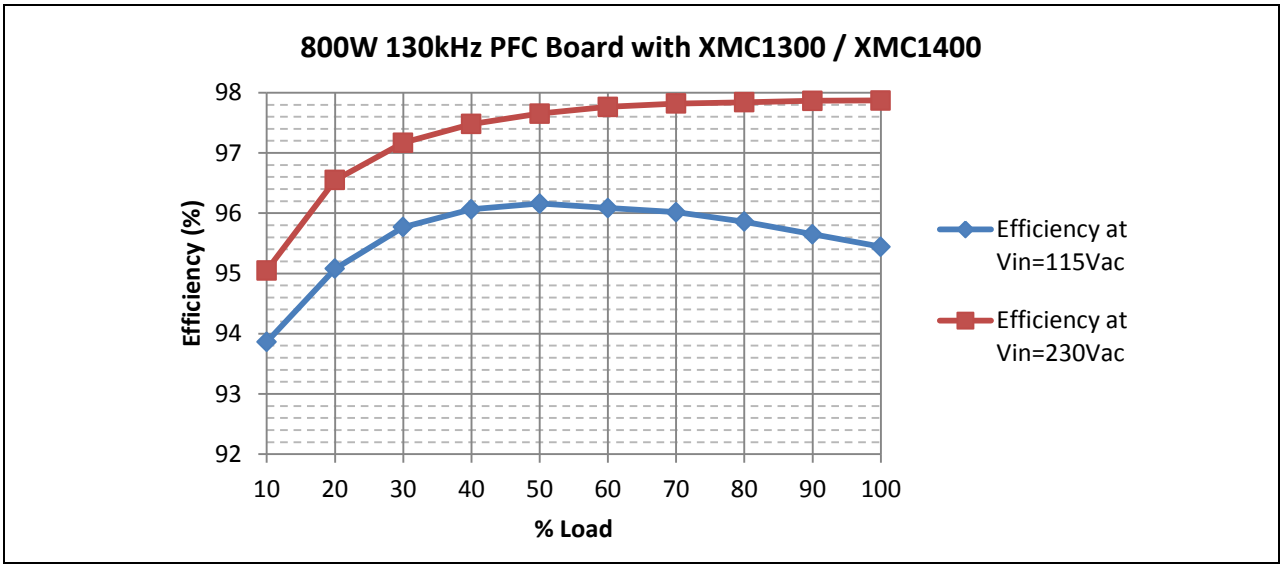


Figure 47 High line and low line efficiency with 2x IPP60R180C7 @ f_s = 130 kHz, R_{gate_on} = 15 Ω, R_{gate_off} = 39 Ω.

Key to the following two figures:

- Channel 1 (yellow): Input current
- Channel 2 (blue): Input voltage

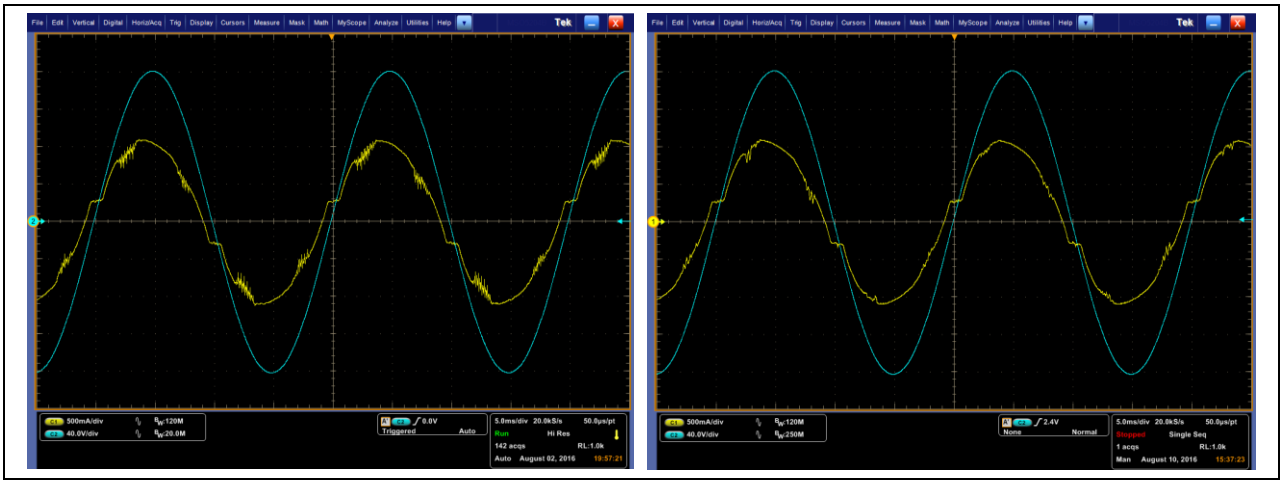


Figure 48 Input current distortion and PF for P_{OUT} = 80 W at V_{IN} = 115 V_{AC} with XCM1300 (left) and XMC1400 (right)

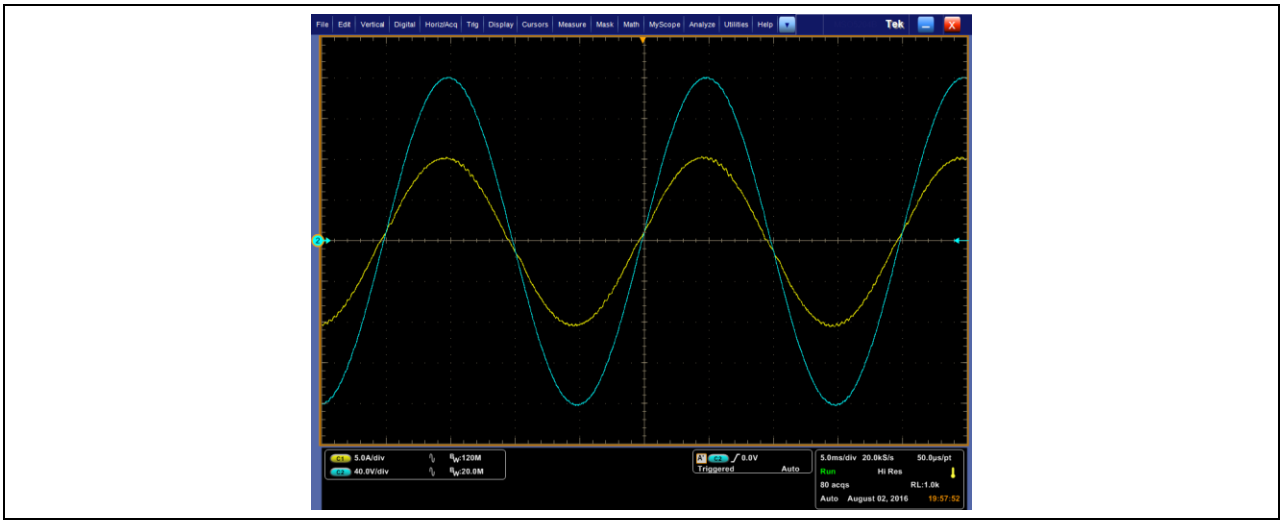


Figure 49 Input current distortion and PF for P_{OUT} = 800 W at V_{IN} = 115 V_{AC} with digital control

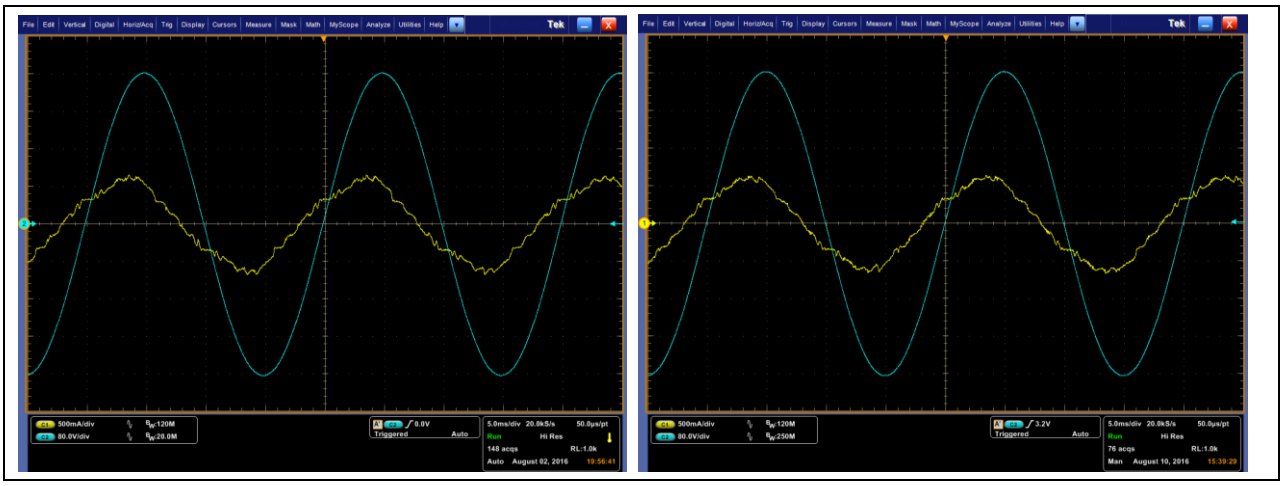


Figure 50 Input current distortion and PF for P_{OUT} = 80 W at V_{IN} = 230 V_{AC} with XMC1300 (left) and XMC1400 (right)

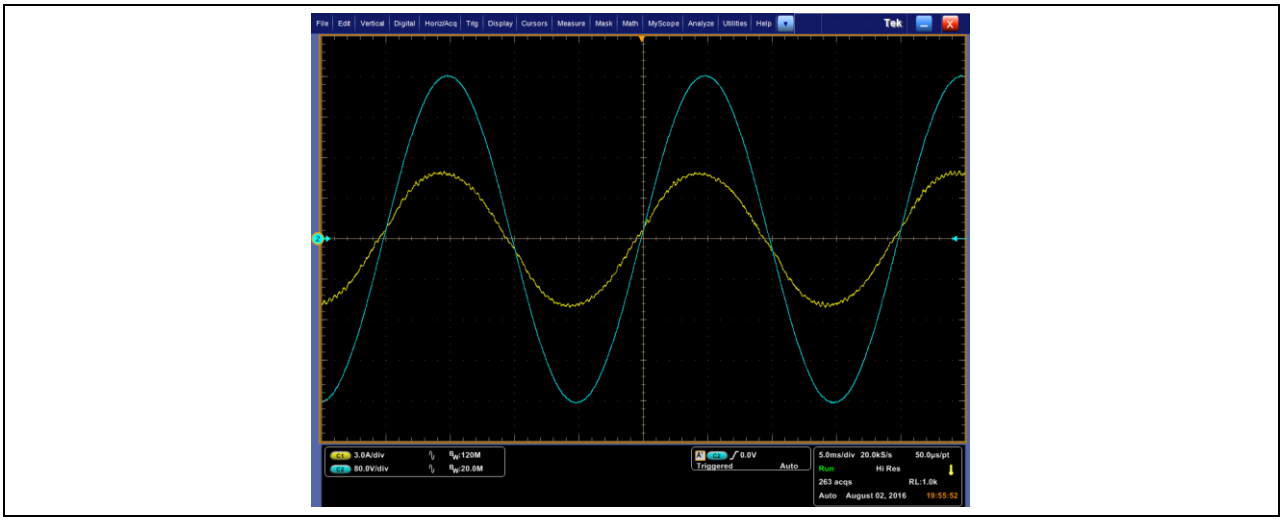


Figure 51 Input current distortion and PF for P_{OUT} = 800 W at V_{IN} = 230 V_{AC} with digital control

6.2.2 Load steps

Key to the following two figures:

- Channel 1 (yellow): output current (1 A/div)
- Channel 2 (blue): output voltage (20 V/div) with 350 V_{DC} offset

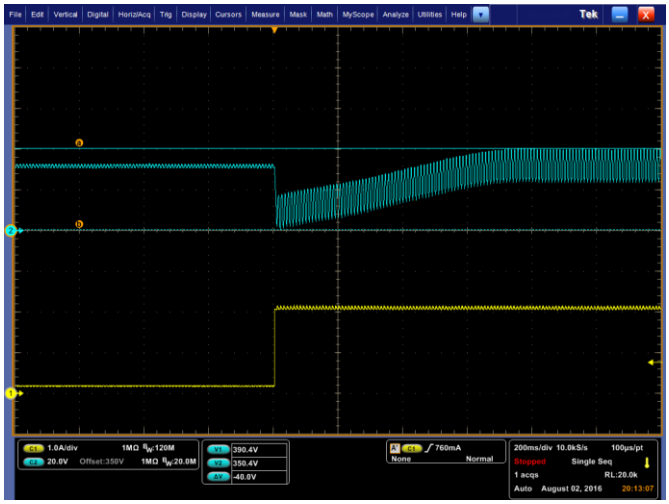


Figure 52 Load step: 10% ➔100% at V_{IN} = 115 V_{AC}

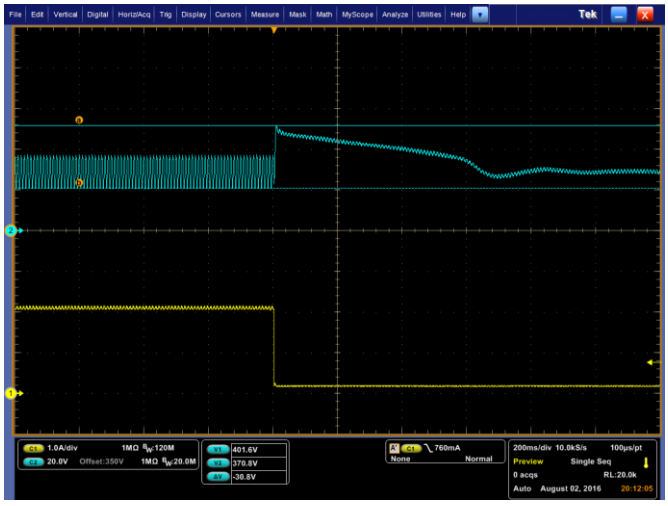


Figure 53 Load step : 100% ➔10% at V_{IN} = 115 V_{AC}

The behavior of the output voltage on abrupt load changes is shown in Figures 52 and 53.

It can be seen that the voltage control ensures an undershoot of about 30 V and a settling time of 700 ms back to the nominal output voltage in case of the 10% to 100% step load full load is present as shown in Figure 52.

In case of the 100% to 10% load jump the voltage overshoot is kept in the range of 21 V as can be seen in Figure 53.

6.2.3 Start up

Key to the following figures:

- Channel 1 (yellow): Input current (10 A/ div)
- Channel 2 (blue): PFC Output voltage (100 V/ div)
- Channel 3 (magenta): 12 V from auxiliary supply

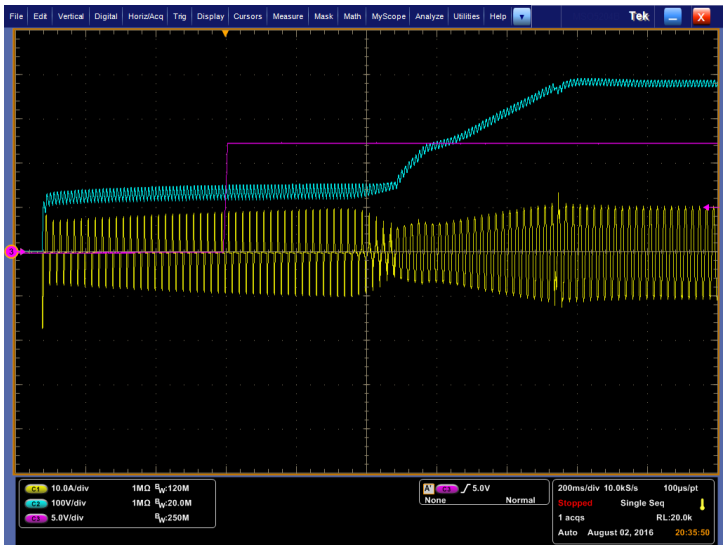


Figure 54 Start-up for P_{OUT} = 800W at V_{IN} = 115 V_{AC}

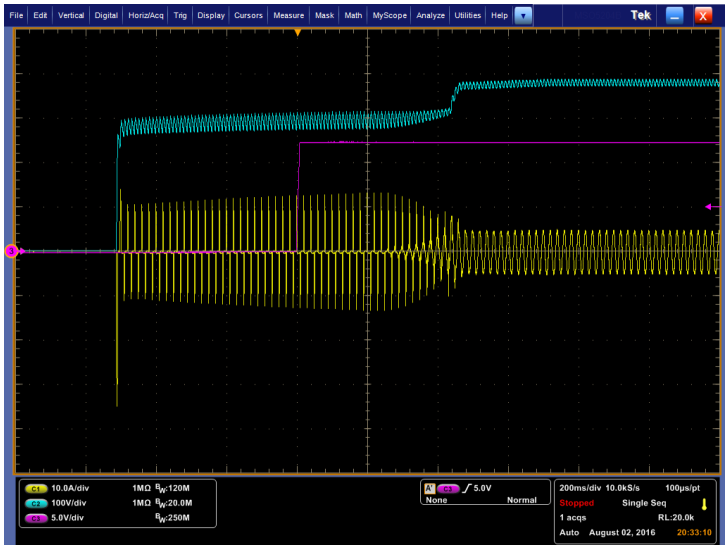


Figure 55 Start-up for P_{OUT} = 800W at V_{IN} = 230 V_{AC}

The software state “Start Request” is entered after initialization of the microcontroller. A ramp with a final value of V_{out_REF} = 380 V_{DC} is set as output voltage reference and boost operation starts from the rectified input voltages 163 V (115 V_{AC}) or 325 V (230 V_{AC}), respectively.

6.2.4 AC line drop-out

Key to the following figures:

- Channel 1 (yellow): Input current (10 A/ div)
- Channel 2 (blue): Output voltage (100 V/ div)

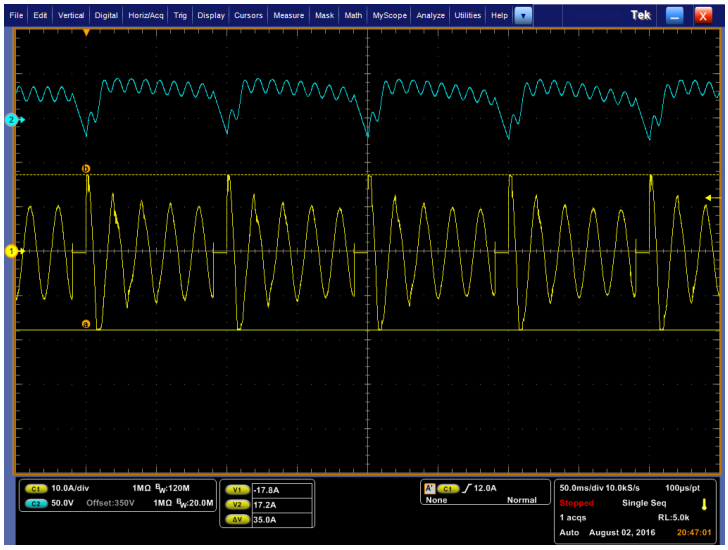


Figure 56 Response of the digital control during five consecutive AC line drop out events for P_{OUT} = 800 W at V_{IN} = 115 V_{AC}



Figure 57 Response of the digital control during five consecutive AC line drop out events for P_{OUT} = 800 W at V_{IN} = 230 V_{AC}

The previous two figures show the robustness of the software to keep running the PFC operation during and after five AC line drop out events at full load. At any input voltage or phase angle triggering event, the transients seen on the input current are within the limits specified in Section 4.2.5.3

6.2.5 Performance of the demoboard at very light load with digital control

A multimode control algorithm has been implemented to ensure best performance at light load and/or high input voltage (i.e. for load demands lower than 10% of rated power only DCM operation is required).

The implemented XMC™ software recognizes the required operation mode in a fast way and applies the algorithm accordingly. This is required because the operation mode can change over half AC cycle or due to load jump.

The two different used algorithms, DCM and CCM, focus on providing the right feedfoward duty cycle and linearize the system transfer function by modifying the gain of the controller inversely proportional to the PFC system transfer function.

With this advance control method the PFC demoboard achieves a Total Harmonic Distortion lower than below 10% at input voltages of 115V and 230V from 5% to 100% of the rated power.

It is also worth to mention that the performance of the XMC1400 microcontroller on the PFC demoboard in terms of Total Harmonic Distortion is better compared to the XMC1300 one, as can be read in Table 8 as well as seen in Figure 48 and Figure 50. For further information about the XMC1400 daughter board, please contact your local Field Application Engineer from Infineon Technologies.

Even though the differential mode capacitors in the EMI filter at very light load add a phase shift, which is not corrected by the controller, the THD and PF achieved are outstanding.

7 Demoboard

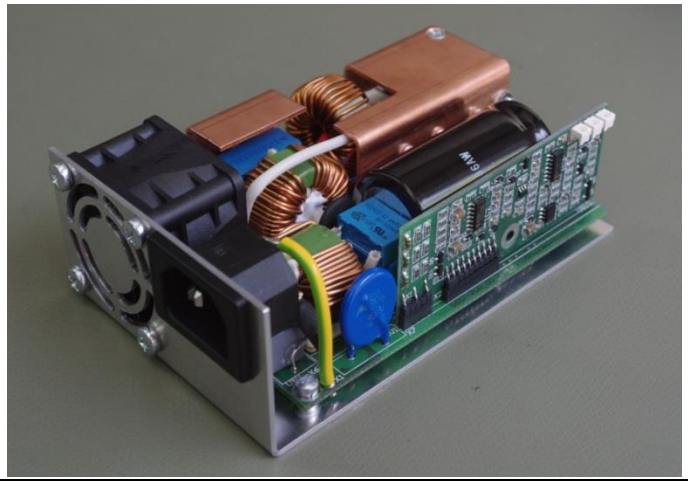


Figure 58 800 W PFC board

7.1 Powerboard

7.1.1 Schematics

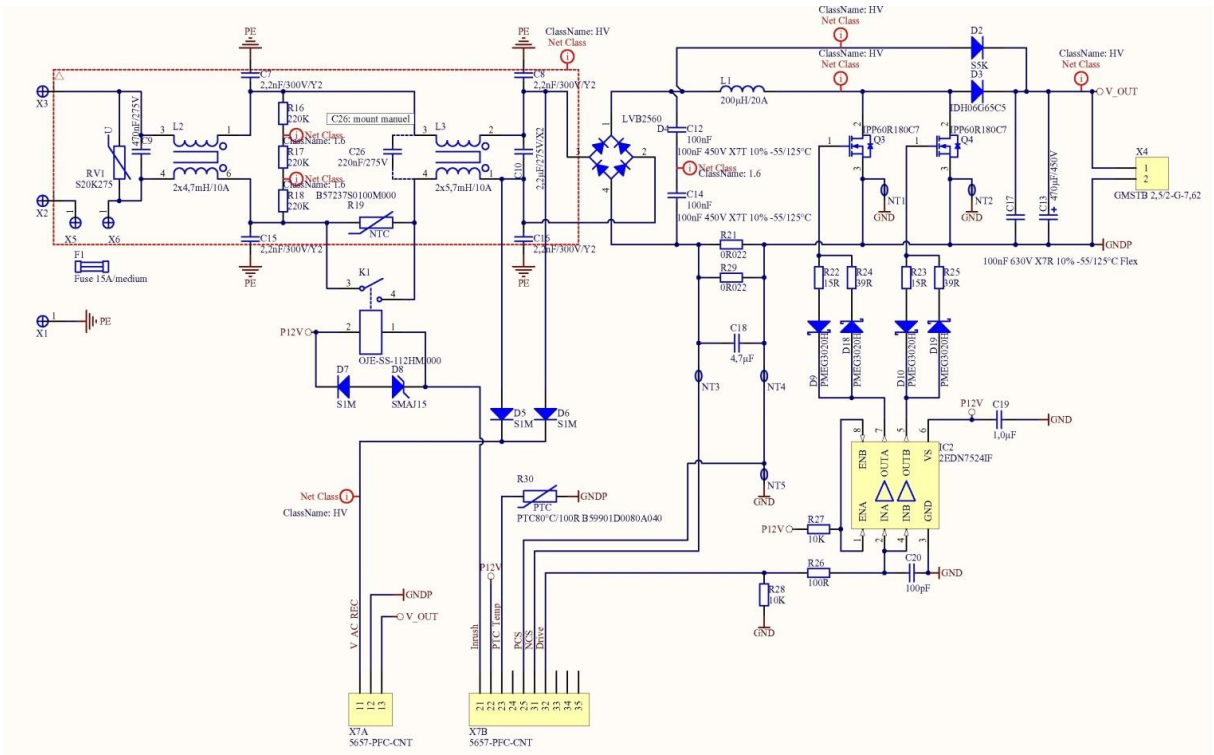


Figure 59 Schematic of power stage

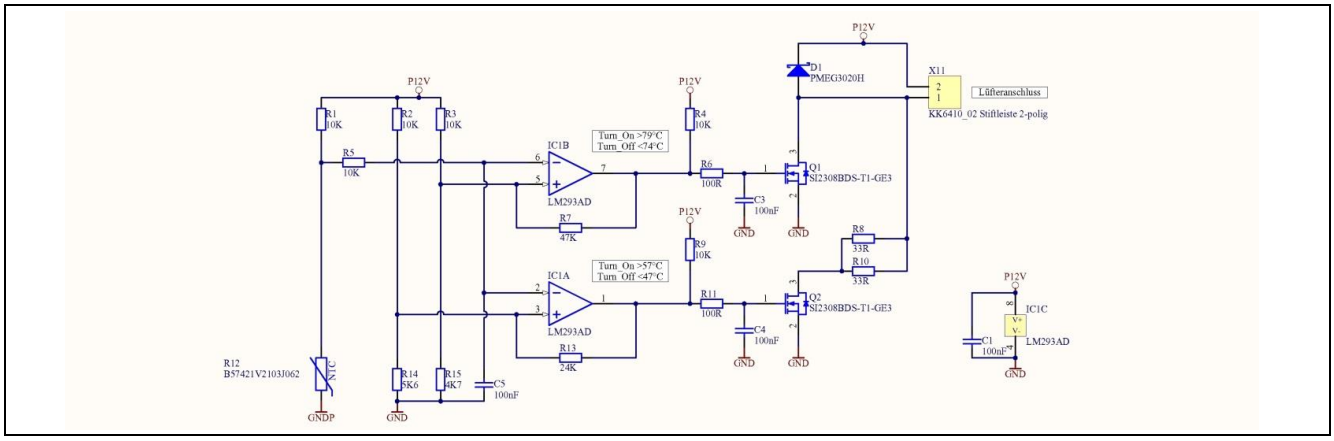


Figure 60 Schematic of fan control

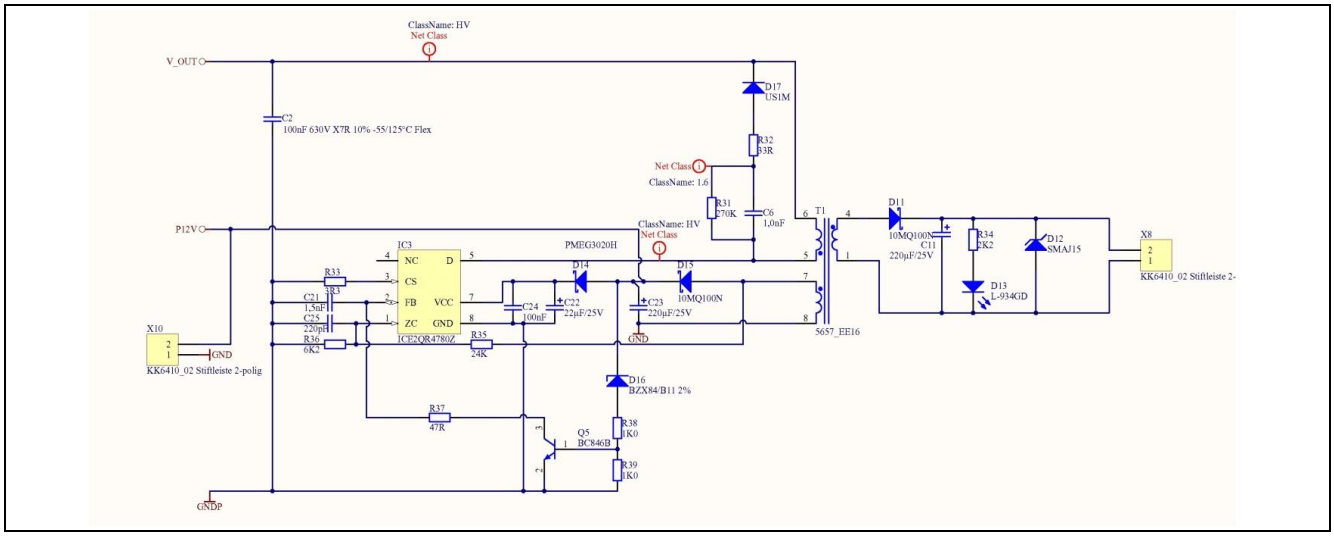


Figure 61 Schematic of auxiliary supply

7.1.2 PCB layout

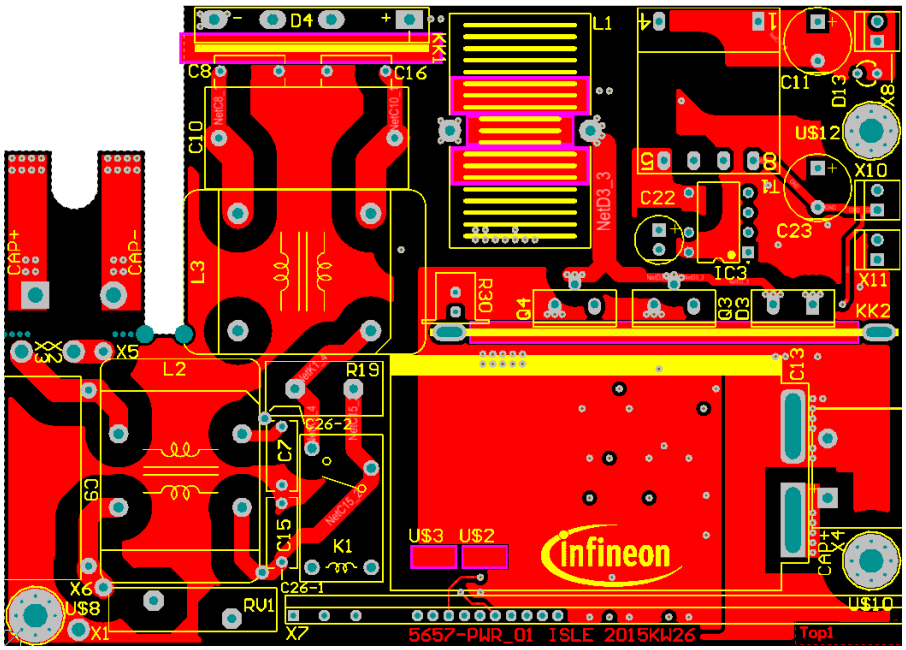


Figure 62 View of PCB top layer

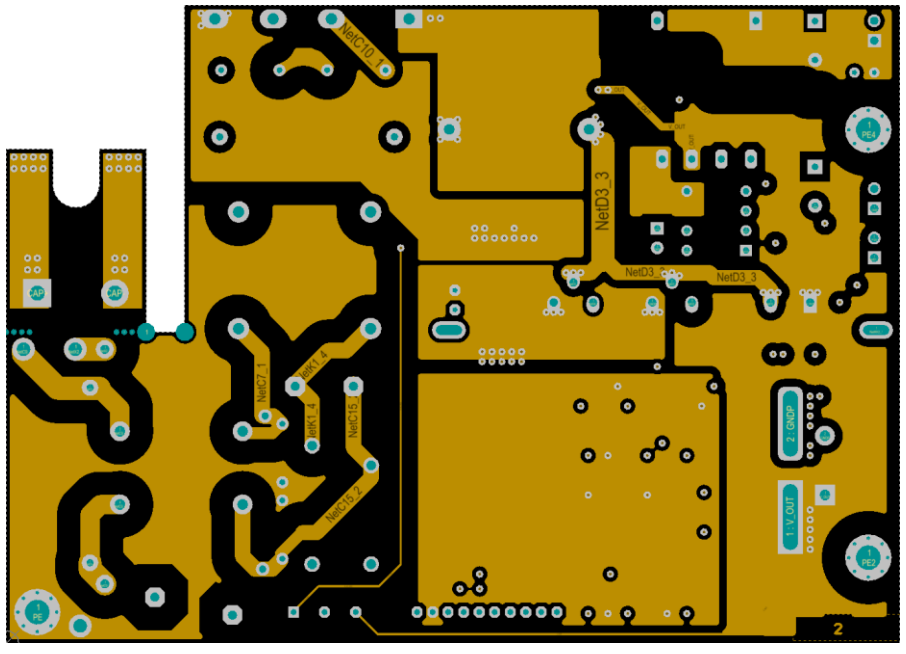


Figure 63 View of PCB Inner 1 layer

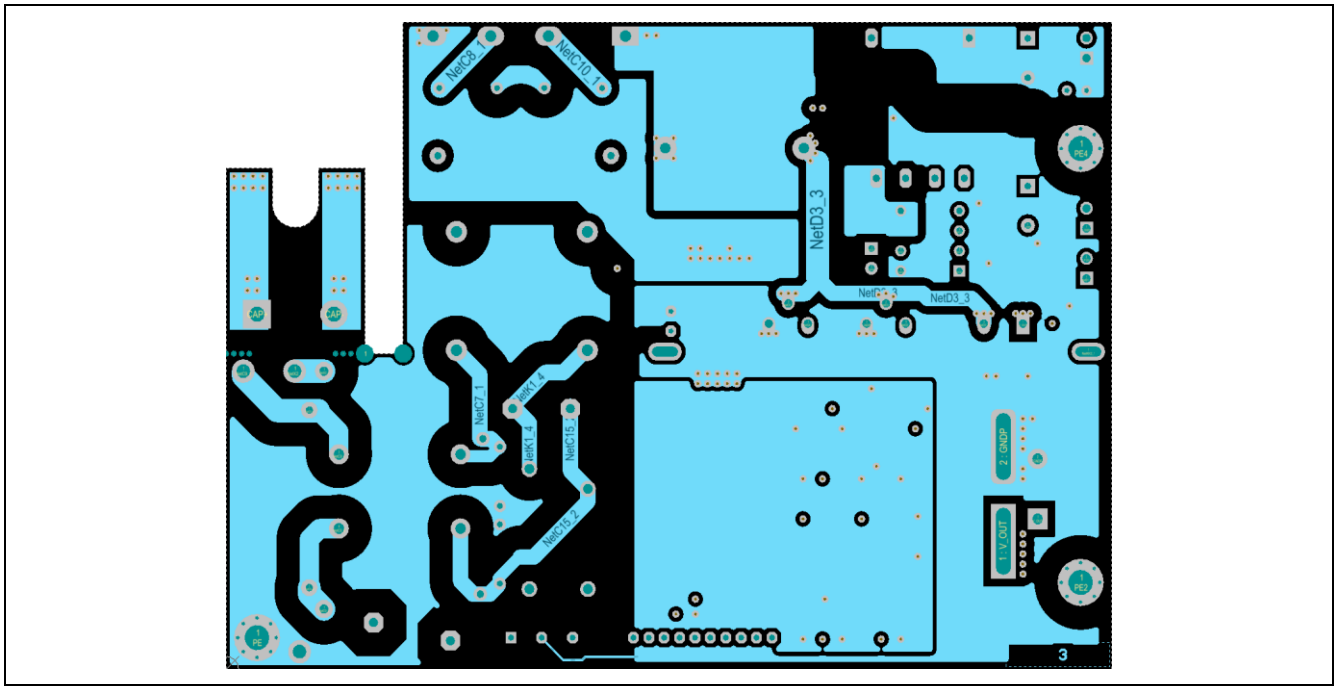


Figure 64 View of PCB inner 2 layer

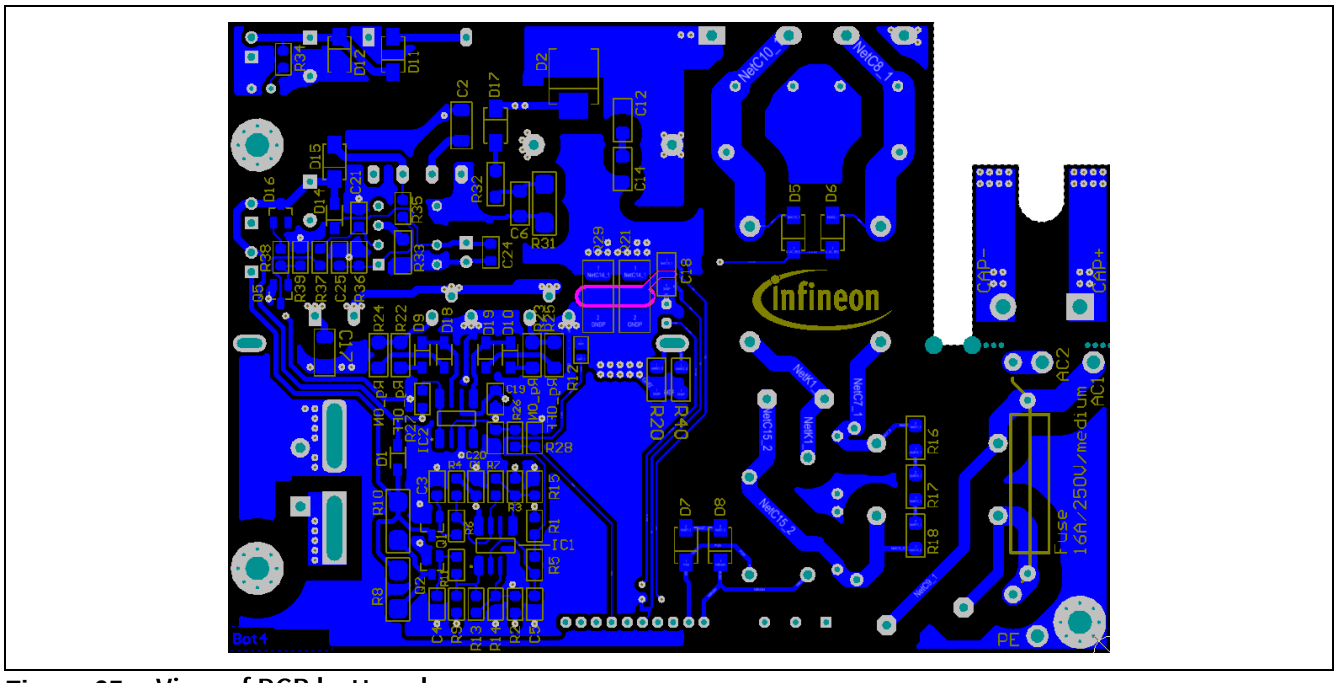


Figure 65 View of PCB bottom layer

7.1.3 Bill of Material

Table 9 BOM of power board

Quantity	Comment	Description	Footprint	Designator
1	220 nF/275 V	220 nF 275 V X2		C26
1	5657-PFC-CNT		5657-CNT_Con2	X7
1	Fuse 15 A/medium	15 A Fuse		F1
1	B57237S0100M000	NTC Inrush 10R 3300 K 3,7 A 17 mW/K	B57237-Sxxx	R19
1	PTC80°C/100 R B59901D0080A040	PTC	B59901-Mxxx	R30
1	1,0 µF	1,0 µF 25 V X7R 10% -55/125°C	CAPC2012M	C19
1	100 pF	100 pF 50 V C0G 5% -55/125°C	CAPC2012M	C20
1	220 pF	220 pF 50 V C0G 5% -55/125°C	CAPC2012M	C25
1	1,5 nF	1,5 nF 50 V X7R 10% -55/125°C	CAPC2012M	C21
5	100 nF	100 nF 50 V X7R 5% -55/125°C	CAPC2012M	C1, C3, C4, C5, C24
1	4,7 µF	4,7 µF 25 V X7R 10%	CAPC3216m	C18
2	100 nF	100 nF 450 V X7T 10% -55/125°C	CAPC3216M	C12, C14
1	1,0 nF	1,0 nF 630 V C0G 5%	CAPC3216M	C6
1	100 nF/630 V	100 nF 630 V X7R 10% -55/85°C	CAPC4520M	C2
1	470 µF/450 V	120 µF 450 V 105°C	CAPPA10-30x50R	C13
1	22 µF/25 V	22 µF 25 V	CAPPR2.5-6.3x11	C22
2	220 µF/25 V	220 µF 25 V	CAPPR5-8.7x12	C11, C23
4	2,2 nF/300 V/Y2		CAPR7.5-9X4	C7, C8, C15, C16
1	2,2 µF/305 V	2,2 µF 305 V X2	CAPR22.5-11X26X20	C10
1	470 nF/275V	470 nF 275V X2	CAPR22.5-11X26X20	C9
1	ICE2QR4780Z	PWM Controller Current Mode QR	DIP-8_-6	IC3
1	GMSTB 2,5/2-G-7,62	Phoenix	GMSTBA2,5/2-G-7,62	X4

1	5657_EE16	EF16 Bias Supply	Hartu_E16-8-P2P3	T1
1	2x5,7 mH/10 A	5657 Common Mode Choke	IFX_L-2875053801(L3)	L3
1	2x4,7 mH/10 A	5657 Common Mode Choke	IFX_L-2875070500(L2)	L2
3	KK6410_02 Plug connector 2-pins	Molex	KK6410_2	X8, X10, X11
1	5657-KK_GL	Heatsink	KK_GL	KK1
1	5657-KK_TO220	Heatsink	KK_TO220	KK2
1	L-934GD	LED Low Current green	LED_5MM	D13
1	200 µH/20 A	5657 PFC Choke	PFC_CHOKE-SK	L1
1	LVB2560	Diode Bridge 600 V 25 A	REC-GSIB-5S	D4
1	47R		RESC2012M	R37
3	100R		RESC2012M	R6, R11, R26
2	1K0		RESC2012M	R38, R39
1	2K2		RESC2012M	R34
1	4K7		RESC2012M	R15
1	5K6		RESC2012M	R14
1	6K2		RESC2012M	R36
8	10K		RESC2012M	R1, R2, R3, R4, R5, R9, R27, R28
2	24K		RESC2012M	R13, R35
1	47K		RESC2012M	R7
1	B57421V2103J062	NTC 10K 4000K	RESC2012N	R12
2	22R		RESC3216M	R22, R23
2	39R		RESC3216M	R24, R25
3	220K		RESC3216M	R16, R17, R18
2	0R022	0R022 2512 RESC6330 TK75	RESC6332M	R21, R29
1	3R9		RESMELF3614M	R33
1	33R		RESMELF3614M	R32
2	33R		RESMELF5822M	R8, R10
1	270K		RESMELF5822M	R31
1	OJE-SS-112HM,000	Relay SPST-NO	RLY_TE-OJE	K1
1	S20K275	Varistor 275 V 1 W	S20K275	RV1
2	SMAJ15	Diode Supressor	SMA_M	D8, D12
2	10MQ100N	Diode Schottky	SMA_M	D11, D15
3	S1M	Rectifier diode	SMA_M	D5, D6, D7

1	US1M	Diode Ultra Fast 1000 V	SMA_M	D17
1	S5K	Rectifier diode	SMC_M	D2
4	PMEG3020H	Diode Schottky 30 V 2 A	SOD123M	D1, D9, D10, D14
1	LM293AD	Comparator	SOIC127P600-8M	IC1
1	2EDN7524IF	Low Side Dual MOSFET Driver, non-inverting	SOIC127P600-8M	IC2
1	BC846B	NPN Transistor	SOT23-3M	Q5
1	BZX84/B11 2%	Diode Zener	SOT23-3M	D16
2	SI2308BDS-T1-GE3	MOSFET N-Channel	SOT23-3M	Q1, Q2
2	IPP65R180C7	MOSFET N-Channel	TO220-AB_HV	Q3, Q4
1	IDH06G65C5	Diode Schottky 650 V	TO220-AC	D3

7.2 ICE3PCS01G daughter board

7.2.1 Schematics

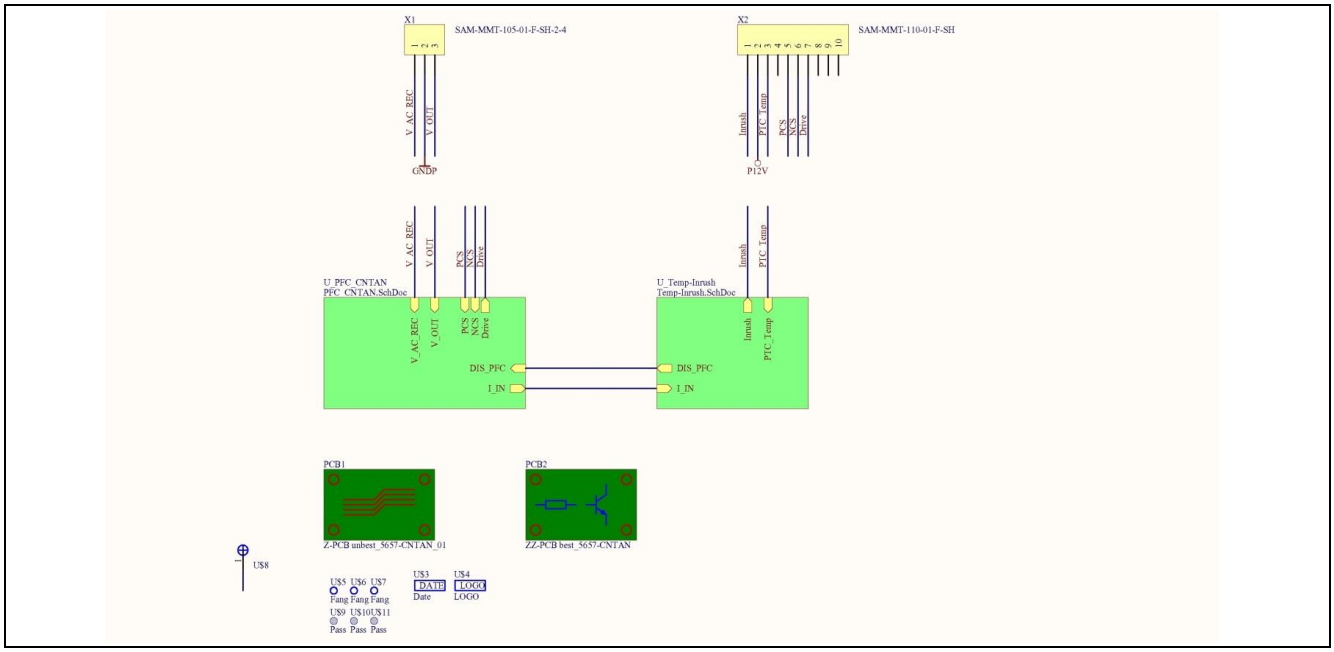


Figure 66 Schematic of connector

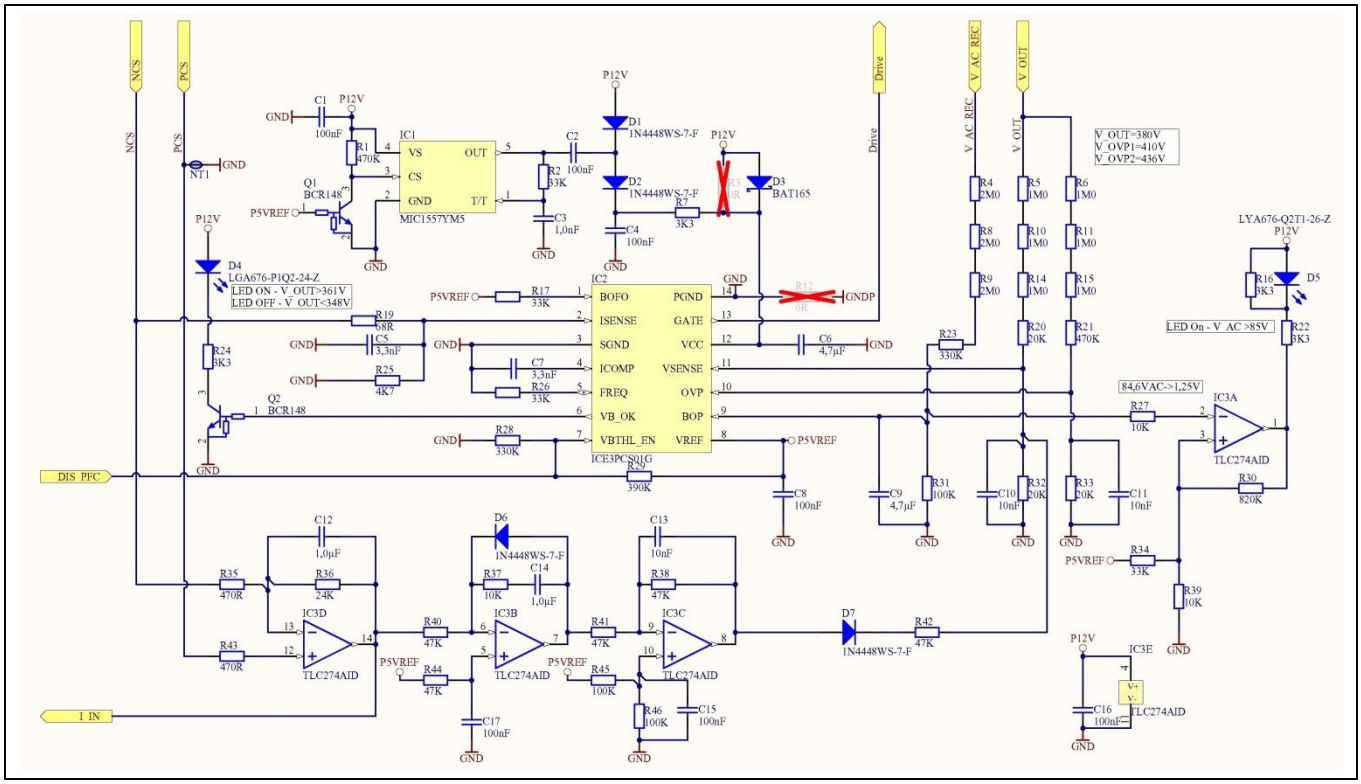


Figure 67 Schematic of PFC control

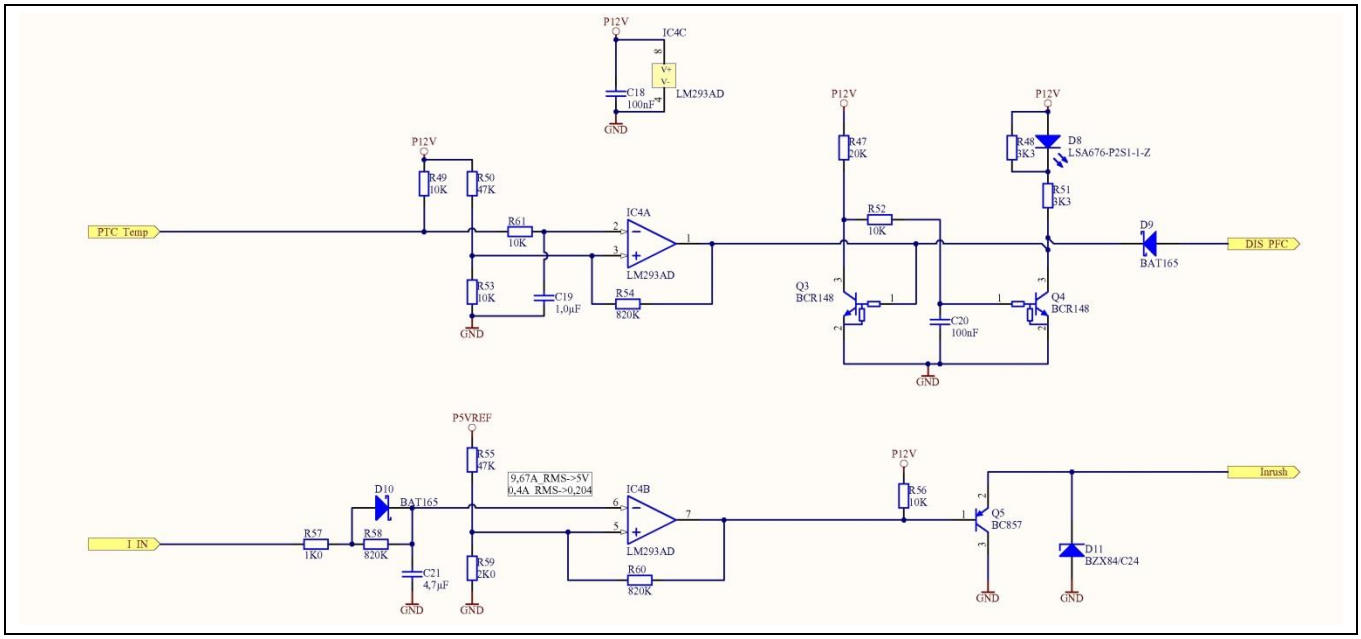


Figure 68 Schematic of temperature monitoring and inrush relay control

7.2.2 PCB Layout

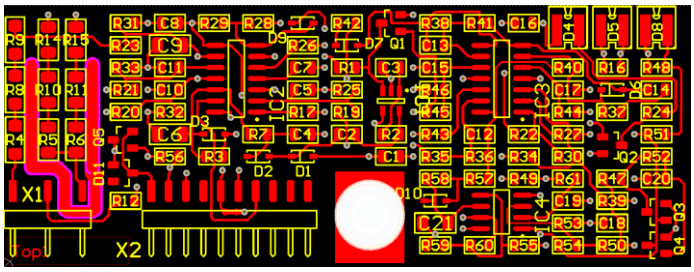


Figure 69 View of analog control PCB top layer

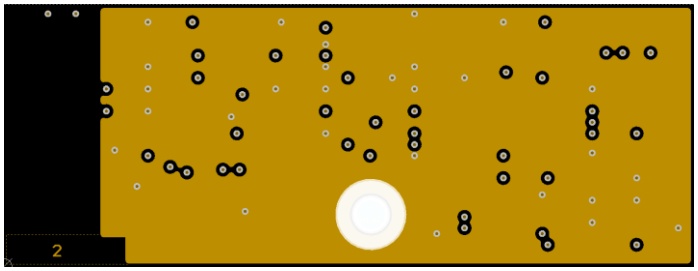


Figure 70 View of analog control PCB inner 1 layer

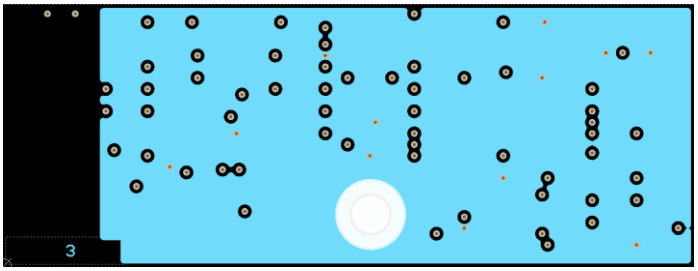


Figure 71 View of analog control PCB inner 2 layer

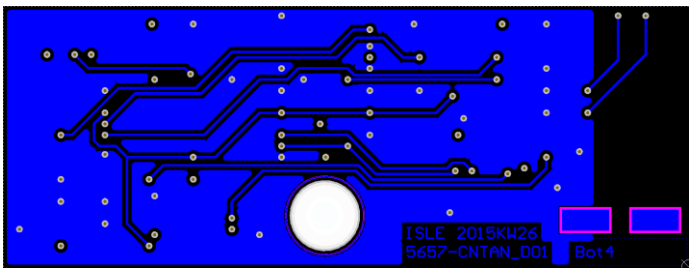


Figure 72 View of analog control PCB bottom layer

7.2.3 Bill of material

Table 10 BoM of control board

Quantity	Comment	Description	Footprint	Designator
3	1,0µF	1,0µF 25V X7R 10% -55/125°C	CAPC2012N	C12, C14, C19
1	1,0nF	1,0nF 50V C0G 5% -55/125°C	CAPC2012N	C3
2	3,3nF	3,3nF 50V X7R 10% -55/125°C	CAPC2012N	C5, C7
3	10nF	10nF 50V X7R 5% -55/125°C	CAPC2012N	C10, C11, C13
9	100nF	100nF 50V X7R 5% -55/125°C	CAPC2012N	C1, C2, C4, C8, C15, C16, C17, C18, C20
3	4,7µF	4,7µF 25V X7R 10%	CAPC3216N	C6, C9, C21
1	LSA676-P2S1-1-Z	LED Hyper Bright Super-Red	LED_LxA670	D8
1	LGA676-P1Q2-24-Z	LED Hyper Bright green	LED_LxA670	D4
1	LYA676-Q2T1-26-Z	LED Low Current yellow	LED_LxA670	D5
1	68R		RESC2012N	R19
2	470R		RESC2012N	R35, R43
2	1K0		RESC2012N	R57, R59
6	3K3		RESC2012N	R7, R16, R22, R24, R48, R51
1	4K7		RESC2012N	R25
7	10K		RESC2012N	R27, R37, R39, R52, R53, R56, R61
4	20K		RESC2012N	R20, R32, R33, R47
1	24K		RESC2012N	R36
4	33K		RESC2012N	R2, R17, R26, R34
8	47K		RESC2012N	R38, R40, R41, R42, R44, R49, R50, R55
3	100K		RESC2012N	R31, R45, R46
2	330K		RESC2012N	R23, R28
1	390K		RESC2012N	R29
2	470K		RESC2012N	R1, R21
4	820K		RESC2012N	R30, R54, R58,

				R60
6	1M0		RESC3216N	R5, R6, R10, R11, R14, R15
3	2M0		RESMELF3614N	R4, R8, R9
1	SAM-MMT-105-01-X-SH-2-4		SAM-MMT-105-01-X-SH-2-3	X1
1	SAM-MMT-110-01-X-SH		SAM-MMT-110-01-X-SH	X2
3	BAT165	Diode Schottky	SOD323	D3, D9, D10
4	1N4448WS-7-F	Diode Fast Switching	SOD323	D1, D2, D6, D7
1	LM293AD	Comparator	SOIC127P600-8N	IC4
1	TLC274AID	Operational Amplifier	SOIC127P600-14N	IC3
1	ICE3PCS01G	PFC Controller Continuous Conduction Mode	SOIC127P600-14N	IC2
1	BC857	pnp Transistor	SOT23-3N	Q5
4	BCR148	npn Transistor	SOT23-3N	Q1, Q2, Q3, Q4
1	BZX84/C24	Diode Zener	SOT23-3N	D11
1	MIC1557YM5	Timer	SOT23-5N	IC1

7.3 XMC1300 daughter board

7.3.1 Schematics

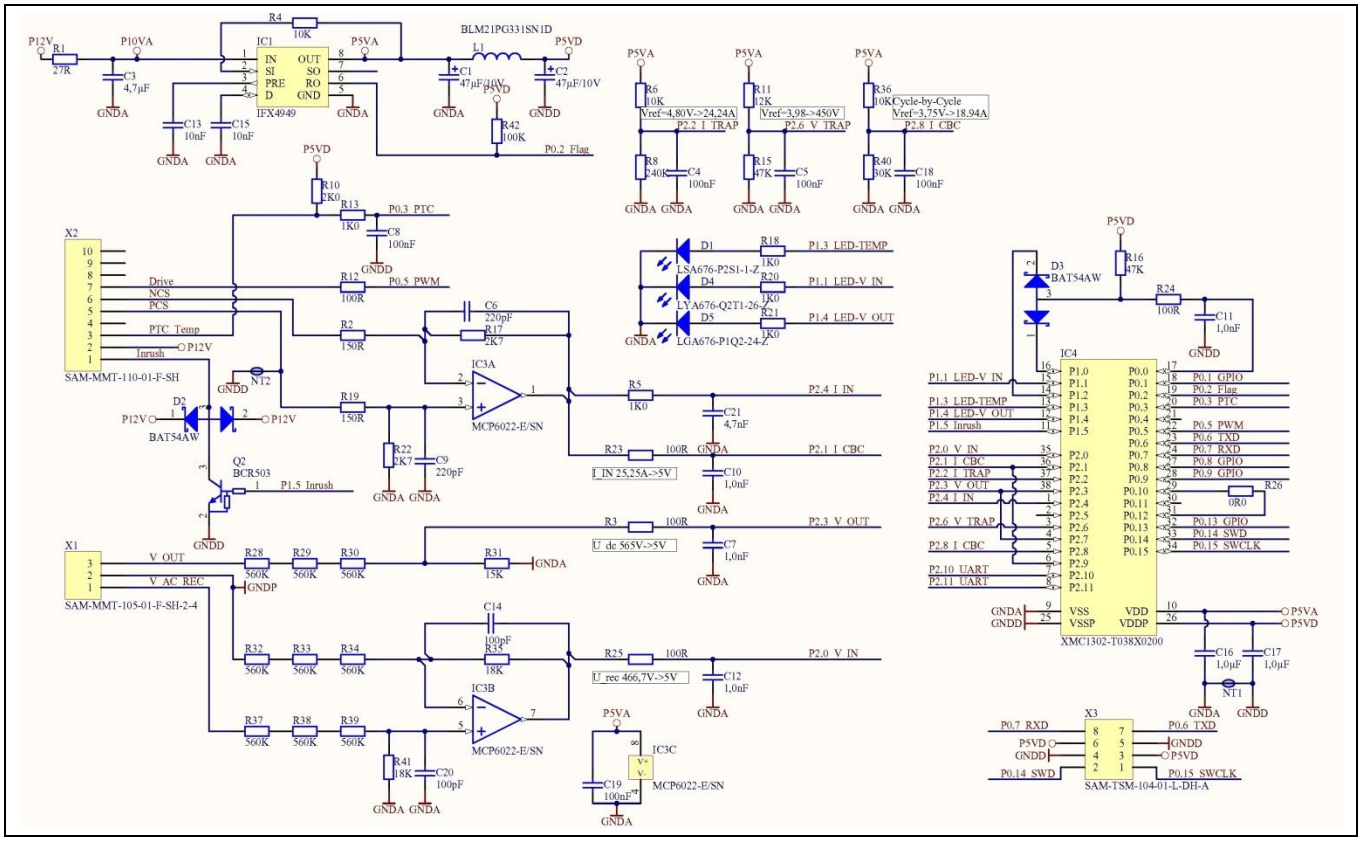


Figure 73 Schematic of DPFC control

7.3.2 PCB Layout

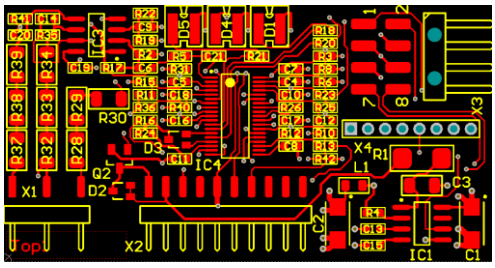


Figure 74 View of DPFC-PCB top layer

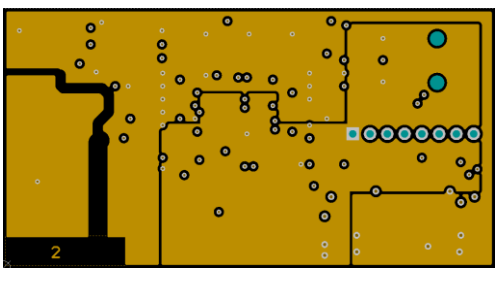


Figure 75 View of DPFC-PCB inner 1 layer

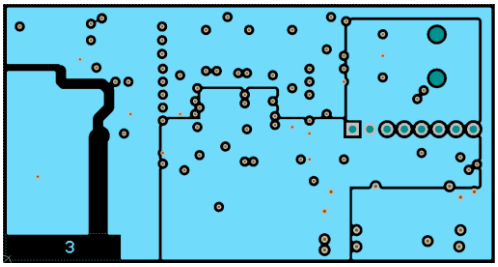


Figure 76 View of DPFC-PCB inner 2 layer

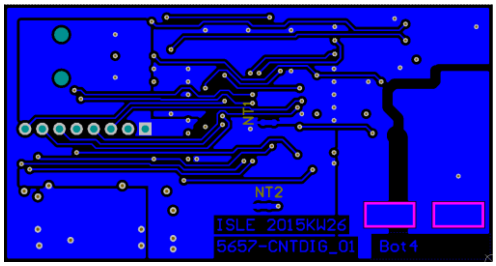


Figure 77 View of DPFC-PCB bottom layer

7.3.3 Bill of Material

Table 11 BoM of DPFC control board

Quantity	Comment	Description	Footprint	Designator
2	1,0 µF	1,0 µF 16 V X7R 10% -55/125°C	CAPC1608N	C16, C17
2	10n F	10 nF 50 V X7R 10% -55/125°C	CAPC1608N	C13, C15
5	100 nF	100 nF 50 V X7R 10% -55/125°C	CAPC1608N	C4, C5, C8, C18, C19
2	100 pF	100 pF 50 V C0G 5% -55/125°C	CAPC1608N	C14, C20
4	1,0 nF	1,0 nF 50 V C0G 5% -55/125°C	CAPC1608N	C7, C10, C11, C12
2	220 pF	220 pF 50 V X7R 10% -55/125°C	CAPC1608N	C6, C9
1	4,7 nF	4,7 nF 50 V X7R 10% -55/125°C	CAPC1608N	C21
1	4,7 µF	4,7 µF 25 V X7R 10%	CAPC3216N	C3
2	47µF/10V	47 µF 10 V 125°C	CAPMP4726X20N	C1, C2
1	BLM21PG331SN1D	Ferrite bead 330Ohm, 1,5 AA	INDP2012N	L1
1	LSA676-P2S1-1-Z	LED Hyper Bright super-red	LED_LxA670	D1
1	LGA676-P1Q2-24-Z	LED Hyper Bright green	LED_LxA670	D5
1	LYA676-Q2T1-26-Z	LED Low Current yellow	LED_LxA670	D4
5	100R		RESC1608N	R3, R12, R23, R24, R25
2	150R		RESC1608N	R2, R19
5	1K0		RESC1608N	R5, R13, R18, R20, R21
2	2K7		RESC1608N	R17, R22
3	10K		RESC1608N	R4, R6, R36
1	12K		RESC1608N	R11
1	15K		RESC1608N	R31
2	18K		RESC1608N	R35, R41
2	47K		RESC1608N	R15, R16
1	100K		RESC1608N	R42
1	30K		RESC1608N	R40
1	0R0		RESC1608N	R26
1	240K		RESC1608N	R8
9	560K		RESC3216N	R28, R29, R30, R32, R33, R34, R37, R38, R39
1	27R		RESMELF5822N	R1
1	SAM-MMT-105-01-F-SH-2-4	pin-header 2mm 5-poles SMT Pin 2 and 4 removed	SAM-MMT-105-01-X-SH-2-3	X1
1	SAM-MMT-110-01-F-SH	pin-header 2mm 10 poles SMT	SAM-MMT-110-01-X-SH	X2

1	SAM-TSM-104-01-L-DH-A	pin-header 2x4 SMT	SAM-TSM-104-01-X-DHA-Revers	X3
1	MCP6022-E/SN	Operational Amplifier	SOIC127P600-8N	IC3
1	IFX4949	Voltage Regulator	SOIC127P600-8N	IC1
1	XMC1302-T038X0200 B-Step	Microcontroller	SOP50P640-38N	IC4
1	BCR503	npn Transistor digital	SOT23-3N	Q2
2	BAT54AW	Diode Schottky	SOT323N	D2, D3

8 Useful material and links

- 600 V CoolMOS™ C7 webpage
  www.infineon.com/600V-C7

- Product brief 600 V CoolMOS™ C7
  http://www.infineon.com/dgdl/Infineon-Product_Brief_600V_CoolMOS_C7-PB-v01_00-EN.pdf?fileId=5546d4624cb7f111014d664a241c4aa1

- 650 VCoolSiC™ Schottky diode generation 5 webpage
  http://www.infineon.com/sic-gen5

- Product brief 650 VCoolSiC™ Schottky Diode generation 5
  http://www.infineon.com/dgdl/Infineon+-+Product+Brief+-+Silicon+Carbide+-+Schottky+Diodes+-+650V+thinQ%21+Generation+5.pdf?fileId=db3a3043399628450139b06e16a721d0

- 2EDN7524F non isolated gate driver (EiceDRIVER™) webpage
  www.infineon.com/2EDN

- Product brief 2EDN7524F non isolated gate driver (EiceDRIVER™)
  http://www.infineon.com/dgdl/Infineon-Product+Brief+2EDN+MOSFET+EiceDRIVER+Family-PB-v01_00-EN.pdf?fileId=5546d4624cb7f111014d668a5a004c12

- ICE3PCS01G PFC controller webpage
  http://www.infineon.com/cms/en/product/channel.html?channel=ff80808112ab681d0112ab6a716f0504

- XMC1300 microcontroller webpage
  http://www.infineon.com/cms/en/product/evaluation-boards/KIT_XMC13_BOOT_001/productType.html?productType=db3a30443ba77cfd013baec9c4b30ca8

- ICE2QR4780Z flyback controller product webpage
  http://www.infineon.com/cms/en/product/power/supply-voltage-regulator/ac-dc-integrated-power-stage-coolset-tm/quasi-resonant-coolset-tm/ICE2QR4780Z/productType.html?productType=db3a30432a7fedfc012ab2458b0c36ff

- KIT_XMC_LINK_SEGGER_V1 isolated debug probe webpage
  http://www.infineon.com/cms/en/product/productType.html?productType=5546d462501ee6fd015023aeb65733b3#ispnTab1

9 References

[1] Huliehel, F.A.; Lee, F.C.; Cho, B.H., "Small-signal modeling of the single-phase boost high power factor converter with constant frequency control," *Power Electronics Specialists Conference, 1992. PESC '92 Record., 23rd Annual IEEE* , vol., no., pp.475,482 vol.1, 29 Jun-3 Jul 1992

[2] M. Xie, “Digital Control for Power Factor Correction”, Virginia Polytechnic Institute and State University, 2003

[3] XMC™ APPs and XMC™ Lib, from Infineon Homepage > Microcontroller > Development Tools, Software and Kits > DAVE™ – Free Development Platform for Code Generation > All new 2015 DAVE™ – Beta-Version 4:
http://www.infineon.com/cms/de/product/microcontroller/development-tools-software-and-kits/dave-tm-%E2%80%93-free-development-platform-for-code-generation/dave-tm-version-4/channel.html?channel=5546d46149b40f65014a0a403bfb0922

[4] Van de Sype, David M.; De Gusseme, K.; Van den Bossche, A.P.M.; Melkebeek, J.A., "Duty-ratio feedforward for digitally controlled boost PFC converters," in *Industrial Electronics, IEEE Transactions on* , vol.52, no.1, pp.108-115, Feb. 2005

Revision History

Major changes since the last revision

Page or Reference	Description of change
--	First Release

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