600 W Half Bridge LLC Evaluation Board with 600 V CoolMOS™ C7

About this document

Scope and purpose

The present 600 W Half Bridge LLC evaluation board is a great example of a full Infineon solution, including high voltage and low voltage power devices, controllers, and drivers to demonstrate the most flexible and effective way to design the high voltage DC/DC stage of a server PSU fulfilling the 80PLUS® Titanium Standard.

Furthermore, the reader will get additional information on how the 600 V CoolMOS™ C7 behaves in this LLC board and what benefits will be achieved.

Intended audience

This document is intended for design engineers who want to improve their high voltage power conversion applications.

Keypoints

- Describes a complete design workflow for a 600 W half-bridge LLC converter, covering topology behavior, resonant tank calculation, and ZVS considerations
- Explains implementation choices for magnetics, resonant components, synchronous rectification, and control strategies aligned with 80PLUS® Titanium efficiency requirements
- Demonstrates practical design trade-offs including inductance factor selection, transformer thermal limits, burst-mode behavior, and hard-commutation mitigation
- Summarizes board-level integration aspects, including layout, schematics, and test procedures relevant for validating high-efficiency server PSU HV DC-DC stages

About this product family

Product family

Infineon's CoolMOS™ is a high-voltage N-channel silicon power MOSFET that is designed to provide excellent thermal performance, lowest switching and conduction power losses, and optimal $R_{DS(on)}$ for increased system efficiency, supporting a range of application from low power levels to high power levels:

Target applications

- Consumer electronics
- Industrial applications
- Home appliances
- Server
- Telecom
- Renewables

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1 Introduction

The opportunity to significantly reduce the size of power converters by increasing the switching frequency created by the MOSFET technology has recently focused topology development and optimization on the reduction of switching losses of the semiconductor devices, which are perceived as the major obstacle to maximizing the switching frequency of PWM converters.

This has triggered studies on the resonant power conversion, which allows minimizing the switching losses through the achievement of zero-voltage (ZVS) or zero-current (ZCS) switching behavior.

An important example of resonant power conversion is provided by the LLC topology, which can address the requirements of high efficiency and power density through the achievement of a true zero voltage switching. Finally, its bill of material is significantly reduced compared to the other very popular soft-switching topology, the phase shift full bridge. These arguments bring the LLC resonant converter more in usage in the server/telecom market.

This document will describe an analog controlled 600 W Half Bridge (HB) LLC converter designed using Infineon products. Order information for ISAR: EVAL_600W_12V_LLC_C7

2 HB LLC converter design considerations

In the present chapter, the most relevant design decisions are explained and documented with related calculations.

2.1 Principle of operation

The principle schematic of a Half Bridge LLC converter is shown in the Figure 1. C_r, L_r, and L_m represent the so called "resonant tank": together with the main transformer, they are the key components in the LLC design. The primary Half Bridge and the secondary synchronous rectification are the other two stages to be defined.

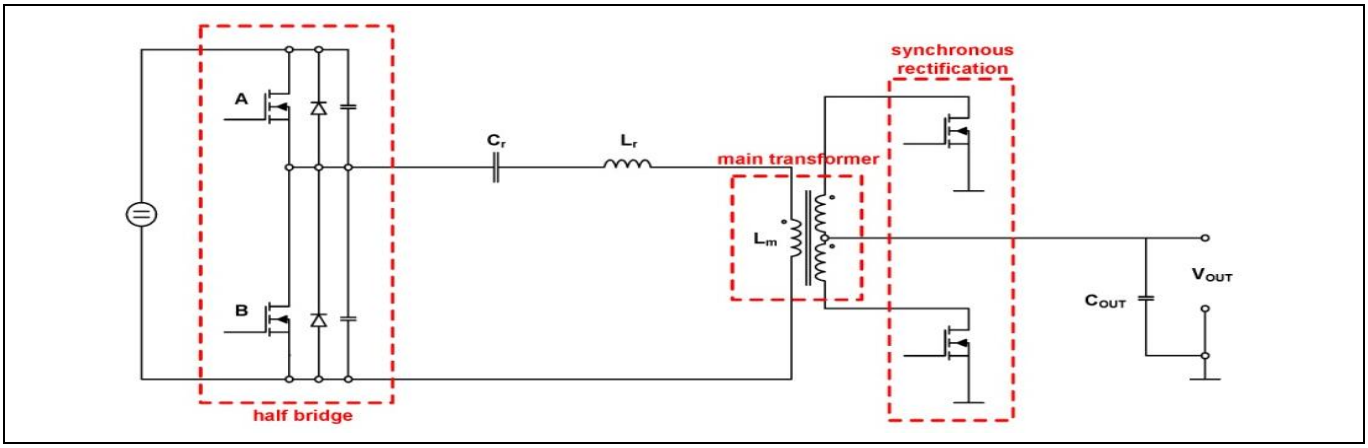


Figure 1 Principle schematic of a Half Bridge LLC converter

The LLC is a resonant converter, that means it operates with frequency modulation, instead of the pulse width modulation (PWM), traditional approach to power conversion.

Starting point in a resonant converter design is the definition of an energy transfer function, which can be seen as a voltage gain function, a mathematical relationship between input and output voltages of the converter. Trying to get this function in an "exact" way involves several nonlinear circuital behaviors governed by complex equations. However, under the assumption that the LLC operates in the vicinity of the series resonant frequency, important simplifications can be introduced.

In fact, under this assumption, the current circulating in the resonant tank can be considered purely sinusoidal, ignoring all higher order harmonics: this is the so called First Harmonic Approximation Method (FHA), which is the most common approach to the design of an LLC converter.
In the FHA, the voltage gain is calculated with reference to the following equivalent resonant circuit, as shown in Figure 2.

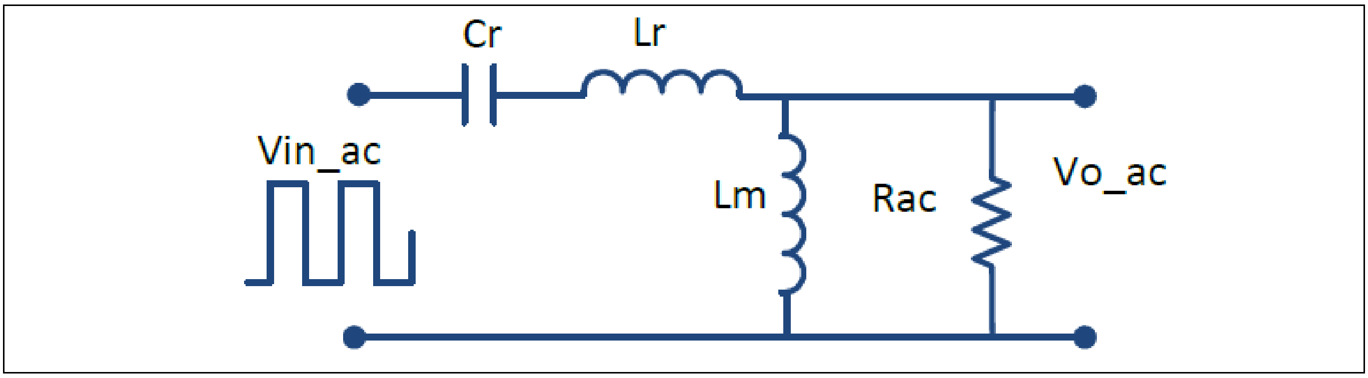


Figure 2 First Harmonic Approximation equivalent resonant circuit

The mathematical expression of the gain K is:

$$K(Q,m,Fx) = \left| \frac{Vo\_ac(s)}{Vin\_ac(s)} \right| = \frac{Fx^2(m-1)}{\sqrt{(m \cdot Fx^2 - 1)^2 + Fx^2 \cdot (Fx^2 - 1)^2 \cdot (m-1)^2 \cdot Q^2}} \tag{1}$$

where:

$$m = \frac{Lr + Lm}{Lr}; \quad fr = \frac{1}{\sqrt{Lr \cdot Cr}}; \quad Fx = \frac{fs}{fr}; \quad Rac = \frac{8}{\pi^2} \cdot \frac{Np^2}{Ns^2} \cdot Ro; \quad Q = \frac{\sqrt{Lr/Cr}}{Rac}; \tag{2}$$

So, the resonant tank gain K can be plotted in function of the normalized switching frequency f_x for different values of the quality factor Q and any single value of the inductance factor m.

In this chapter, a design procedure for selecting the main LLC parameters is presented, with the goal to achieve the best performance while fulfilling the input and output regulation requirements.

At same time, zero voltage switching operation of the primary half bridge MOSFETs must be ensured, to get full benefits out of the soft-switching behavior, especially at light load.

2.2 Input design data

In Table 1, an overview of the major design parameter is displayed.

Table 1 Design parameters

Description	Minimum	Nominal	Maximum
Input voltage	350 V_{DC}	380 V_{DC}	410 V_{DC}
Output voltage	11.9 V_{DC}	12 V_{DC}	12.1 V_{DC}
Output power	–	–	600 W
Efficiency at 50% P_{max}	97.5%	–	–
Switching frequency	90 kHz	150 kHz	250 kHz
Dynamic output voltage regulation (0-90% load step)	–	–	Maximum overshoot = 0.1 V Maximum undershoot = 0.3 V
V_{out_ripple}	–	–	150 mV_{pk-pk}

From the Table 1, the first important design parameters can be derived:

Main transformer turn ratio:

$$n = \frac{Np}{Ns} = \frac{Vin\_nom}{2 \cdot Vout\_nom} \approx 16 \tag{3}$$

Minimum needed Gain:

$$K_{\min}(Q,m,Fx) = \frac{n \cdot Vo\_\min}{Vin\_\max / 2} \approx 0.95 \tag{4}$$

Maximum needed Gain:

$$K_{max}(Q, m, Fx) = \frac{n \cdot Vo\_max}{Vin\_min / 2} \approx 1.08 \tag{5}$$

2.3 Selection of the inductance factor 'm'

The inductance factor (Equation 2) has an important impact on the converter operation. Lower values of 'm' achieve higher boost gain and narrower range of the frequency modulation, that means more flexible control and regulation, which is valuable in applications with very wide input voltage range.

On the other hand, this means also smaller values of L_m which leads into significantly high magnetizing current circulating in the primary side: this current doesn't contribute to the power transferred, but mainly generates conduction losses on the primary side. In other words, there is a trade-off between flexible regulation and overall efficiency requirements, especially at light load.

In the case of our demo board, the main goal is to achieve high efficiency, so a relatively high inductance factor 'm' is selected. This is also because the input range is relatively narrow and, in any case, we rely on the bulk capacitor to meet specific hold up time requirements at the complete AC/DC SMPS level; therefore, in our design m≈12.

2.4 Gain curve

The resulting gain curves (Figure 3), for loads between 10% and 100% P_{max} are in the following plot:

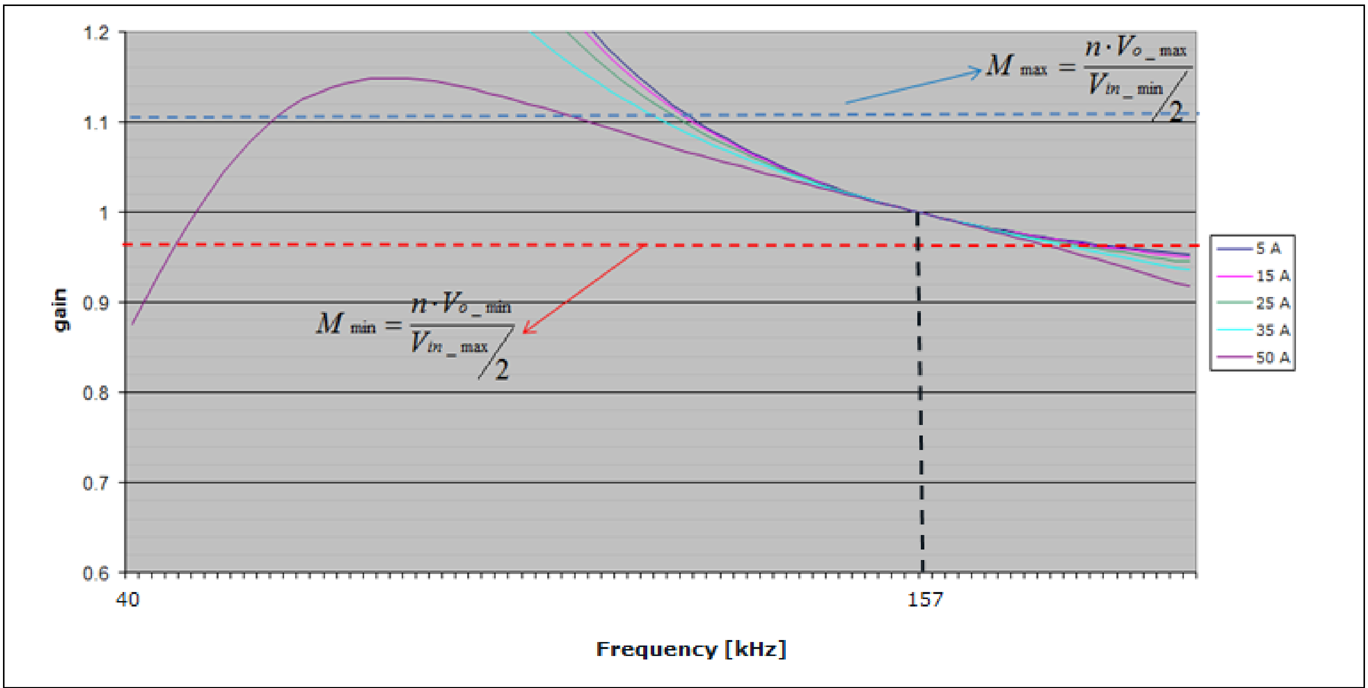


Figure 3 Gain curve

Both the M_{min} and M_{max} limits cross all the gain curves of our LLC converter, indicating that regulation is fully achieved within the specified ranges.

2.5 Resonant components calculation

Combining equations (1) and (2), we get a system where the unknown is L_r, C_r and L_m.

To solve it, the following values are set for the LLC converter:

$$n = \frac{Np}{Ns} = \frac{Vin\_nom}{2 \cdot Vout\_nom} \approx 16 \Rightarrow Np = 16; Ns = 1 \tag{6}$$

$$m = \frac{Lr + Lm}{Lr} \approx 12 \Rightarrow Lm = 195\mu H; Lr = 17\mu H \tag{7}$$

$$Cr = 66nF \tag{8}$$

$$fr = \frac{1}{2\pi \cdot \sqrt{Lr \cdot Cr}} \approx 150KHz \tag{9}$$

2.6 The ZVS behavior: energy and time considerations

ZVS calculations involve two kinds of analysis, the one in the energy domain and the other in the time domain. The goal is to have enough energy in the resonant tank able to discharge the output capacitance of the primary MOSFET, but also an appropriate dead time between the turn-off of each device and the corresponding turn-on of the one at the other side of the half bridge.

$C_{o(er)}$ is the C_{oss} energy related component of the used high voltage MOSFET, in our case CoolMOS™ IPP60R180C7.

Q_{oss} is the charge stored in C_{oss} at $V_{in(nom)}$=380 V_{DC}

2.6.1 Energy related equations

$$\mathrm{I}mag\_\min = \frac{2 \cdot \sqrt{2}}{\pi} \cdot \frac{n \cdot Vo}{2\pi \cdot fsw\_\max \cdot Lm} = 0.672A \tag{10}$$

$$Enres\_\min = \frac{1}{2} \cdot (Lm + Lr) \cdot I^2 mag\_\min = 95.1\mu J \tag{11}$$

$$Encap\_\max = \frac{1}{2} \cdot (2Co(er)) \cdot V^2 DS\_\max \approx 9\mu J \tag{12}$$

$$\Rightarrow Enres\_\min > Encap\_\max \tag{13}$$

2.6.2 Time related equation

It can be demonstrated that:

$$tdead = \frac{tecs}{2} + \frac{2 \cdot Qoss@\mathrm{V}_{\mathrm{in\_nom}}}{\mathrm{Im}, pk} = \frac{tecs}{2} + \frac{2 \cdot Co(tr)@\mathrm{V}_{\mathrm{in\_nom}} * \mathrm{V}_{\mathrm{in\_nom}}}{\mathrm{Im}, pk} \quad (14)$$

where t_{dead} is the dead time set between the conduction time of the two HB devices and t_{ecs} is the time when the channel of each MOSFET is still in conduction after turning it off (linear mode operation), which is the function of device parameters like $V_{gs(th)}$, $R_{g(tot)}$ and C_{gs}/C_{gd}.
Using that equation, together with the min and max values of the magnetizing current:

$$\mathrm{Im}\,ag\_\min = \frac{2 \cdot \sqrt{2}}{\pi} \cdot \frac{n \cdot Vo}{2\pi \cdot fsw\_\max \cdot Lm} = 0.672\ A \quad (10)$$

$$\mathrm{Im}\,ag\_\max = \frac{2 \cdot \sqrt{2}}{\pi} \cdot \frac{n \cdot Vo}{2\pi \cdot fsw\_\min \cdot Lm} = 1.66\ A \quad (11)$$

$$tdead, \min = \frac{tecs}{2} + \frac{2 \cdot Qoss, @400V}{\mathrm{Im}, ag, \max} \approx 130\ ns \quad (14)$$

$$tdead, \max = \frac{tecs}{2} + \frac{2 \cdot Qoss, @400V}{\mathrm{Im}\,ag, \min} \approx 311\ ns \quad (15)$$

2.7 The main transformer design

As explained in Section 2.6, the target efficiency of this design is fixed by the 80PLUS® Titanium Standard; that means fixing certain minimum requirements for the high voltage DC/DC stage at 10%, 20%, 50%, and 100% load conditions.

The most critical condition for the main transformer is full load, mainly due to thermal considerations. The selection of the core size and material is based on this condition, along with the power density (and therefore switching-frequency) target and the available airflow.

Keeping a margin in the design, the minimum efficiency requirement at full load is fixed for the Half Bridge LLC converter to 97%, which means our goal is to keep the total dissipated power in that condition below 18 W.
To guarantee a balanced spread of power and heating, a good rule in the design of the LLC Converter is to keep the total power dissipated on the main transformer below 1/6 of the total dissipated power, which means the maximum allowed power on it shall be below 3 W. This is our first important design input.

The maximum operating temperature is 55°C as in typical server applications. Due to transformer safety insulation approvals, the maximum operating temperature of the transformer must be lower than 110°C, therefore:

$$\Delta T_{trafo\_MAX} = (110 - 55)°C = 55°C \quad (16)$$

From (16) and (17), the maximum thermal resistance of the core shape can be easily derived:

$$R_{th\_trafo\_MAX} = \frac{\Delta T_{trafo\_MAX}}{P_{trafo\_MAX}} = \frac{55}{3} {}^{\circ}C/_{W} = 18.3 {}^{\circ}C/_{W} \quad (17)$$

So, our selected core shape must have thermal resistance lower than 18.3°C/W.
This requirement can be fulfilled with different choices: the preferred will allow maximizing the ratio between available winding area and effective volume, while remaining consistent with equation (18).
Also, considering the power density target (in the range of 20 W/inch^3), the most suitable selection is PQ 35/35, as shown in Figure 4.

The related coil form shows a minimum winding area of 1.58 cm^2 and a thermal resistance of 16.5°C/W, thus able to dissipate up to 3.33 W by keeping the ΔT_{MAX} <55°C.
Once verified that the thermal equations are fulfilled, we can proceed with the design of the primary and secondary windings and the core material selection with some important goals:

- Fitting the geometry/overall dimensions of the core
- Fulfilling the condition (16)
- Try to distribute the losses between the core and windings as evenly as possible: ideally a "fifty-fifty" split should be achieved at full load, but any percentage close to it would be acceptable

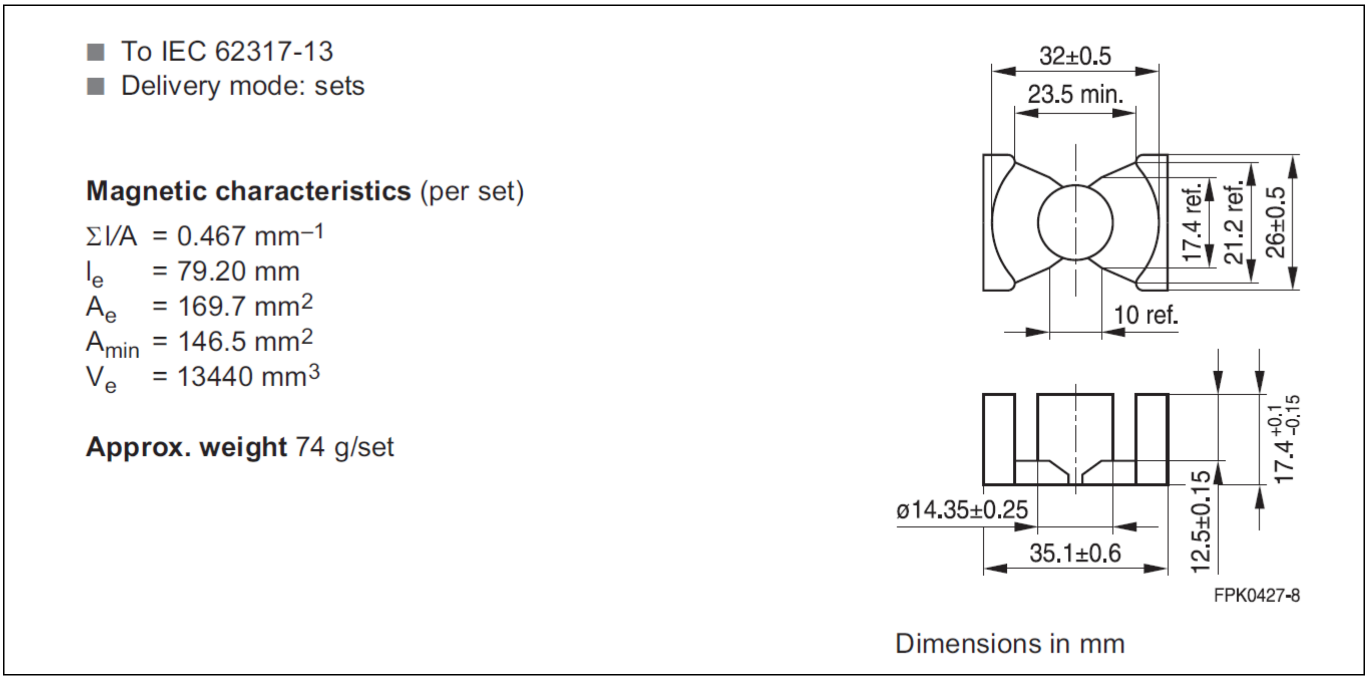


Figure 4 **TDK-Epcos PQ35/35 core**

The selected core material is the ferrite TDK PC95, showing a very interesting plot of core losses (PCV) versus flux density versus frequency (see Figure 5).

The final structure of the main transformer is shown in Figure 6 and was developed in cooperation with the partner company Kaschke Components GmbH, Göttingen, Germany. The primary winding is implemented in a "sandwich" technique using sixteen turns arranged in four layers of litz wire (45 strands, 0.1 mm diameter). This allows minimizing the AC losses caused by skin and proximity effect. The secondary is done using a 20 × 0.5 mm copper band.

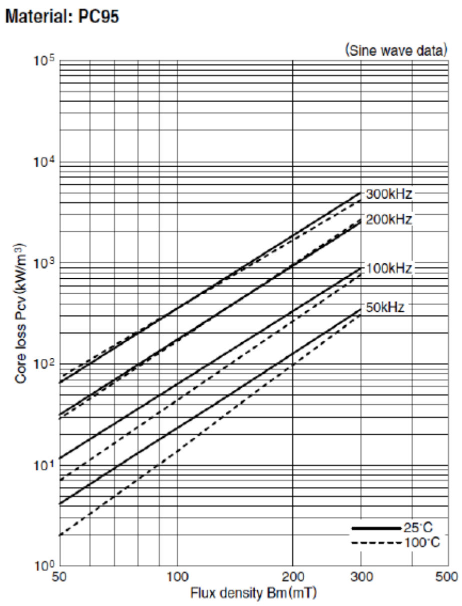


Figure 5 **Ferrite core material TDK PC95**

With this choice, at full-load condition, the total copper losses (primary + secondary, DC + AC components) are 1.1 W and the core losses are 1.8 W, resulting in a total loss of:

$$P_{trafo} = P_{copper} + P_{core} = 2.9W < P_{trafo\_MAX} \tag{18}$$

In other words, equation (18) fulfils the thermal equation (17).

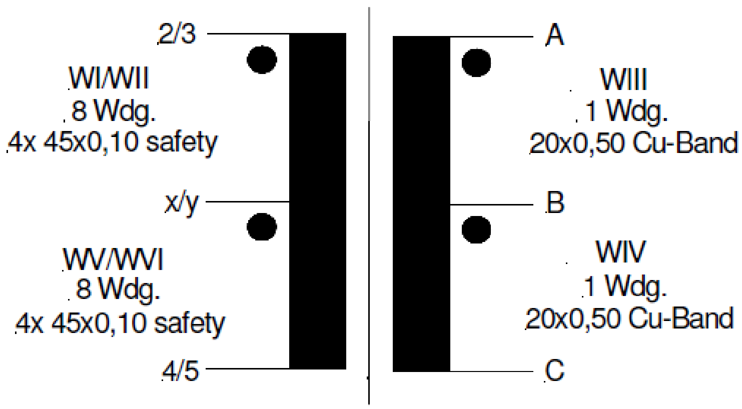


Figure 6 **Winding structure of the PQ 35/35 LLC transformer (Kaschke Components GmbH)**

An important transformer parameter involved in the LLC design is the primary or magnetizing inductance L_m, which, according to equation (7) must be 195 µH. This value is obtained with distributed airgap on the side legs of the PQ core: this construction is preferred since it minimizes the effect of the so called “fringing flux” which generates additional losses in the windings close to the inner limb.

2.8 The resonant choke design

In LLC designs with stringent power density requirements, the resonant choke is typically embedded in the transformer, in the sense that the leakage inductance is utilized for this purpose. This technique offers a significant advantage of saving space and eliminating the cost of an additional magnetic component. However, it also presents some drawbacks, such as difficulty of controlling the L_r value consistently in mass production.

In case of the present design, it has been decided to use an external L_r.This is due to the fact that the demo board is intended to be primarily used for test and benchmarking and therefore, high power density is not in the main focus: having the resonant inductance externally, allows to change the resonant tank in a more flexible way.

According to equation (7), the overall value of L_r shall be 17 µH, including the contribution of the transformer leakage inductance and the external resonant choke.

The external resonant choke is realized using a RM-12 core and a winding construction shown in Figure 7 and implemented by the partner company Kaschke Components GmbH, Göttingen, Germany.

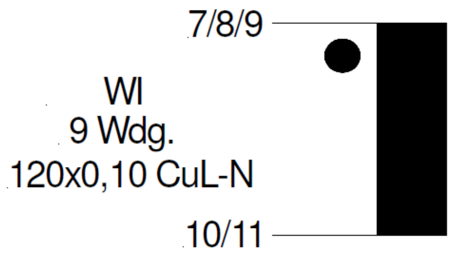


Figure 7 Winding structure of the RM 12 resonant choke (Kaschke Components GmbH)

2.9 The synchronous rectification stage

In applications that target high efficiency both at low and high loads, such as 80PLUS® Titanium- while often requiring high power densities, it is critical to select for the Synchronous Rectification Stage MOSFETs that combine multiple key characteristics.

First of all, these Sync Rec MOSFETs should exhibit very low $R_{DS(on)}$. Indeed, due to the low voltages observed on the secondary side of server power supplies, large currents flow through the Sync Rec MOSFETs. Moreover, compared with hard switching topologies such as ZVS PS FB (zero voltage switching phase-shifted full bridge), using LLC topology leads not only to increased peak currents for the Sync Rec MOSFETs, but also higher root-mean-square currents I_{RMS}.

Since the conduction losses $P_{cond,SR}$ of each Sync Rec MOSFET are defined by:

$$P_{cond\_SR} = R_{DS,on} \cdot (I_{RMS})^2 \tag{19}$$

These losses can only be mitigated through the use of a part with very low $R_{DS(on)}$.

Secondly, it is critical for these Sync Rec MOSFETs to exhibit low gate charges Q_g.

At lower loads, the switching losses of the Sync Rec MOSFETs predominate over the already mentioned conduction losses. In case of LLC topology, the main contributor of these switching losses is related to Q_g.

Most of the time, a driving voltage of 12 V is applied to Sync Rec MOSFETs. Although 12 V is not necessarily the optimized driving voltage for Sync Rec MOSFETs (as discussed below), this driving voltage is very popular in server PSUs because it is readily available and there is no need to derive it from another voltage rail. Therefore,

we chose to follow this trend for this demo board by driving the Sync Rec MOSFETs with 12 V.
This requirement for low Q_g puts an extra-strain on MOSFET manufacturers, especially considering that Sync Rec MOSFETs need to exhibit at the same time a very low $R_{DS(on)}$. Such a feat was however possible due to the new Infineon OptiMOS™ 40 V generation, whose gate charges have been significantly reduced in comparison with the previous generation.

Thirdly, the paralleled Sync Rec MOSFETs should turn on almost simultaneously. This can be achieved by tightening the threshold voltage range $V_{GS(th)}$. In the case of the new OptiMOS™ 40 V generation, its datasheet guarantees a very narrow $V_{GS(th)}$ range, with minimum and maximum values equal to 1.2 V and 2.0 V, respectively.

Finally, the MOSFET package is critical for a variety of reasons. The package should exhibit low parasitic inductances in order to confine its contribution to the V_{DS} overshoot to a strict minimum. This is even more critical in server applications using LLC topology due to the limited headroom for the V_{DS} overshoot between the transformer secondary voltage (25 V) and the 90% derating (36 V_{max}) or even 80% derating (32 V_{max}) applied to the V_{DS} of the Sync Rec MOSFETs. Moreover, due to the conflicting requirements for high power density and high current capability, the package should combine a minimum footprint with good power dissipation.

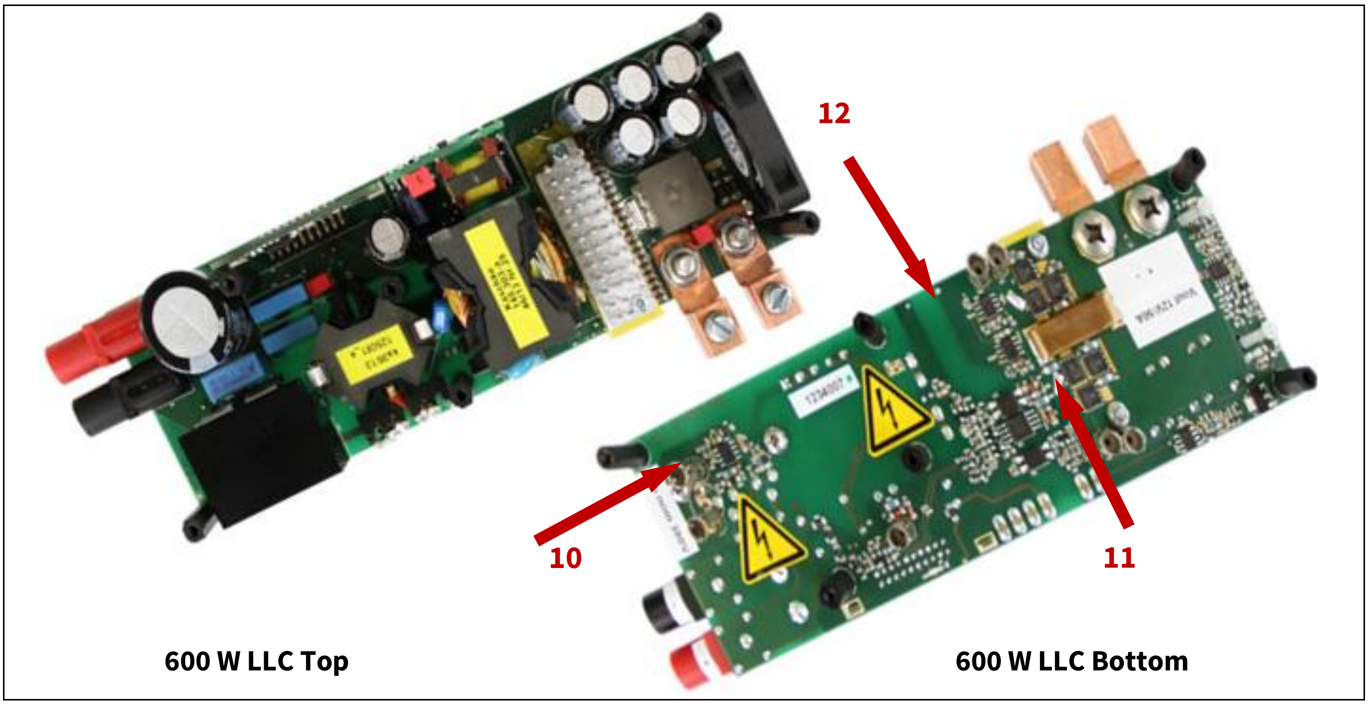
Because of the high current densities arising at the source pins, which can lead to electro-migration and thereafter, destruction of the Sync Rec MOSFETs, the package should provide an enlarged source connection. While the first two sub-items are tackled by standard SuperSO8 packages, it is the addition of source fused leads implemented in the new Infineon OptiMOS™ 40 V generation that reduces the high current densities mentioned above.

3 Board description

3.1 General overview

Figure 8 is the top view, bottom view and the assembly of 600 W Half Bridge LLC evaluation board. Key components are:

(1) heat sink with the assembly of primary side switches CoolMOS™ IPP60R180C7
(2) Resonant capacitor
(3) LLC analog controller ICE2HS01G
(4) Resonant inductor
(5) Main DC-DC transformer
(6) PCB assembly of the auxiliary circuit with bias QR Flyback controller ICE2QR2280Z
(7) Heat sink assembly for cooling the synchronous rectifier
(8) Output capacitor
(9) Output inductor
(10) Half Bridge MOSFET gate driver 2EDL05N06PF
(11) Synchronous rectifier OptiMOS™ BSC010N04LS
(12) Advanced dual-channel Gate Drive 2EDN7524F



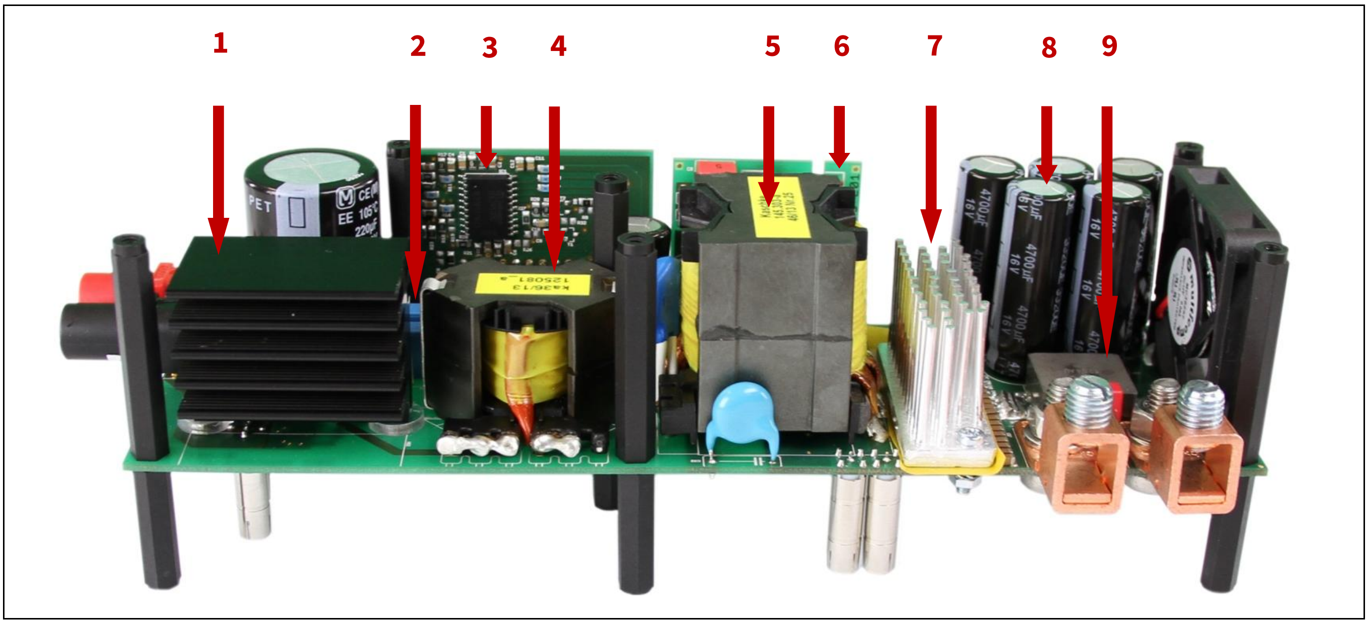


Figure 8 IFX 600W LLC Evaluation Board

3.2 Infineon BOM

This HB LLC 600 W demonstration board is a full Infineon solution, meeting the highest efficiency standard 80PLUS® Titanium using the following parts:

3.2.1 Primary HV MOSFETs CoolMOS™ IPP60R180C7

The 600 V CoolMOS™ C7 is the next step of Silicon improvement based on the 650 V CoolMOS™ C7. It stays with the strategy to increase switching performance in order to enable highest efficiency in any kind of target applications as for boost topologies like PFC's (power factor correction) and high voltage DC/DC stages like LLC's (DC/DC stage with resonant tank in order to maintain zero voltage switching). Although the 600 V CoolMOS™ offers very fast switching, it also kept the ease-of-use level (how easy to control the switch) of the 650 V C7 "parent technology". Therefore, the 600 V CoolMOS™ C7 is an optimized device for highest efficiency SMPS (switched mode power supply). The 600 V C7 represents the new standard of SJ MOSFET.

In LLC application, converter is in resonant operation with guaranteed ZVS even at a very light load condition. Switching loss caused by E_{oss} during turn-on can be considered negligible in this topology. With this consideration, CoolMOS™ C7 family of parts offers superior price/performance ratio with low FOMs (R_{on}*Q_g and R_{on}*Q_{OSS}), which means that MOSFET switching transitions can happen in a shorter dead time period. This will result in a lower turn-off loss pushing further efficiency. The following are the additional features and benefits of CoolMOS™ C7 making it suitable and advantageous for resonant switching topologies like LLC:

- Suitable for hard and soft switching (PFC and high-performance LLC)
- Increased MOSFET dv/dt ruggedness to 120 V/ns
- Increased efficiency due to best-in-class FOM $R_{DS(on)}$*E_{oss} and $R_{DS(on)}$*Q_g
- Best-in-class $R_{DS(on)}$/package
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)

3.2.2 LLC analog controller ICE2HS01G

ICE2HS01G is Infineon's 2nd generation Half Bridge LLC controller designed especially for high efficiency Half Bridge or Full Bridge LLC resonant converter with synchronous rectification (SR) control for the secondary side. With its new driving techniques, the synchronous rectification can be realized for LLC converter operated with secondary switching current in both CCM and DCM conditions. No special synchronous rectification controller IC is needed at the secondary side. The maximum switching frequency is supported up to 1 MHz. Apart from the patented SR driving techniques, this IC provides very flexible design and integrates full protection functions as well. It is adjustable for maximum/minimum switching frequency, soft-start time, frequency, dead time between primary switches, turn-on, and turn-off delay for secondary SR MOSFETs. The integrated protections include input voltage brownout, primary three-levels overcurrent, secondary overload protection and no-load regulation. It also includes a burst mode function which offers an operation with low quiescent current maintaining high efficiency at low output load while keeping output ripple voltage low.

3.2.3 Half Bridge Gate Drive 2EDL05N06PF

2EDL05N06PF is one of the drivers from Infineon's 2EDL EiceDRIVER™ Compact 600V Half Bridge gate driver IC family with monolithic integrated low-ohmic and ultrafast bootstrap diode. Its level-shift SOI technology supports higher efficiency and smaller form factors of applications. Based on the used SOI-technology, there is an excellent ruggedness on transient voltages. No parasitic thyristor structures are present in the device. Hence, no parasitic latch-up may occur at all temperature and voltage conditions. The two independent driver outputs are controlled on the low side using two different CMOS signals. LSTTL compatible signals, down up to 3.3 V logic. The device includes an undervoltage detection unit with hysteresis characteristic which are optimised either for IGBT or MOSFET. 2EDL05N06PF (DSO-8) and 2EDL05N06PJ (DSO-14) are driver ICs with undervoltage-lockout for MOSFETs. These two parts are recommended for server/telecom, low-voltage drives, e-bike, battery charger, and Half Bridge based switch mode power supply topologies.

- Individual control circuits for both outputs
- Filtered detection of undervoltage supply
- All inputs clamped by diodes
- Offline gate clamping function
- Asymmetric undervoltage lockout thresholds for high side and low side
- Insensitivity of the bridge output to negative transient voltages up to -50 V given by SOI-technology
- Ultra-fast bootstrap diode

3.2.4 Advanced dual-channel Gate Driver 2EDN7524F

The Fast Dual Channel 5 A Low-Side Gate Driver is an advanced dual-channel driver optimized for driving both Standard and Superjunction MOSFETs, as well as GaN Power devices, in all applications in which they are commonly used. The input signals are TTL compatible (CMOS 3.3 V) with an input voltage range from 3 V to +20 V. The ability to operate with -10 V_{DC} at the input pins protects the device against ground bounce conditions. Each of the two outputs is able to sink and source a 5 A current utilizing a true rail-to-rail stage, that ensures very low impedances of 0.7 Ω up to the positive and 0.55 Ω down to the negative rail respectively. Very low channel to channel delay matching, typically 1 ns, enables the double source and sink capability of 10 A by paralleling both channels. Different logic input/output configurations guarantee high flexibility in all applications, such as with two paralleled switches in a boost configuration (see Figure 9). The gate driver is available in the three package options: A standard PG-DSO-8, a thin PG-WSON-8-1, and PG-TSSOP-8-1 (minimized DSO 8 package).

Main Features

- Industry-Standard Pinout
- Two independent low-side gate drivers
- 5 A peak sink/source output driver at V_{DD} = 12 V
- –10 V_{DC} negative input capability against GND-bouncing
- Enhanced operating robustness due to high reverse current capability
- True low-impedance rail-to-rail output (0.7 Ω and 0.55 Ω)
- Very low propagation delay (19 ns)
- Typical 1 ns channel to channel delay matching
- Wide input and output voltage range up to 20 V
- Active low output driver even on low power or disabled driver
- High flexibility through different logic input configurations (LVTTL and CMOS 3.3 V)
- PG-DSO-8, PG-WSON-8-1 and PG-TSSOP-8-1 Package
- Extended operation from -40 °C to 150 °C (junction temperature)
- Particularly well-suited for driving standard, superjunction MOSFETs, IGBTs or GaN power devices

Typical applications

- SMPS
- DC/DC converters
- Motor control
- Solar power, industrial applications

3.2.5 Bias QR Flyback controller ICE2QR2280Z

ICE2QRxxxx is a second generation quasi-resonant PWM CoolSET™ with power MOSFET and startup cell in a single package optimized for off-line power supply applications such as LCD TV, notebook adapter, and auxiliary/housekeeping converter in SMPS. The digital frequency reduction with decreasing load enables a quasi-resonant operation till very low load. As a result, the system average efficiency is significantly improved compared to conventional solutions. The active burst mode operation enables ultra-low power consumption at standby mode operation and low output voltage ripple. The numerous protection functions give full protection of the power supply system in failure situations. Main features of ICE2QR2280Z which make it suitable as an auxiliary converter of this LLC demonstration board are:

- High voltage (650 V/800 V) avalanche rugged CoolMOS™ with startup cell
- Quasi-resonant operation
- Load dependent digital frequency reduction
- Active burst mode for light load operation
- Built-in high voltage startup cell
- Built-in digital soft start
- Cycle-by-cycle peak current limitation with built-in leading edge blanking time
- Foldback Point Correction with digitalized sensing and control circuits
- V_{CC} undervoltage and overvoltage protection with auto restart mode
- Overload/open loop protection with auto restart mode

- Built-in overtemperature protection with auto restart mode
- Adjustable output overvoltage protection with latch mode
- Short-winding protection with latch mode
- Maximum on time limitation
- Maximum switching period limitation

3.2.6 Synchronous Rectification MOSFETs OptiMOS™ BSC010N04LS

For the synchronous rectification stage, the selected device is OptiMOS™ BSC010N04LS, from the latest OptiMOS™ 40 V family. SR is in fact naturally the best choice in high efficiency designs of low output voltage and high output current LLC, as in our case. In applications that target high efficiency both at light and heavy loads – such as 80PLUS® Titanium- while often requiring high power densities, it is critical to select SR MOSFETs that combine the following key characteristics:

- Very low $R_{DS(on)}$: OptiMOS™ BSC010N04LS provides the industry's first 1 mΩ 40 V product in SuperSO8 package
- Low gate charge Q_g, which is important to minimize driving losses, with benefits on light load efficiency
- Very tight $V_{GS(th)}$ range: In case of paralleling, this allows the MOSFETs to turn on almost simultaneously Selected OptiMOS™ offer very close minimum and maximum of $V_{GS(th)}$, respectively 1.2 V and 2 V
- Monolithically integrated Schottky like diode, to minimize the conduction losses on it
- Package: OptiMOS™ BSC010N04LS in SuperSO8 with source fused leads can address all the typical crucial requirements for a suitable SR MOSFET package:
  - Minimizing parasitic inductances
  - Combining compact footprint with good power dissipation
  - Enlarged source connection to minimize electro-migration occurrence

3.3 Board schematics

3.3.1 Mainboard schematic

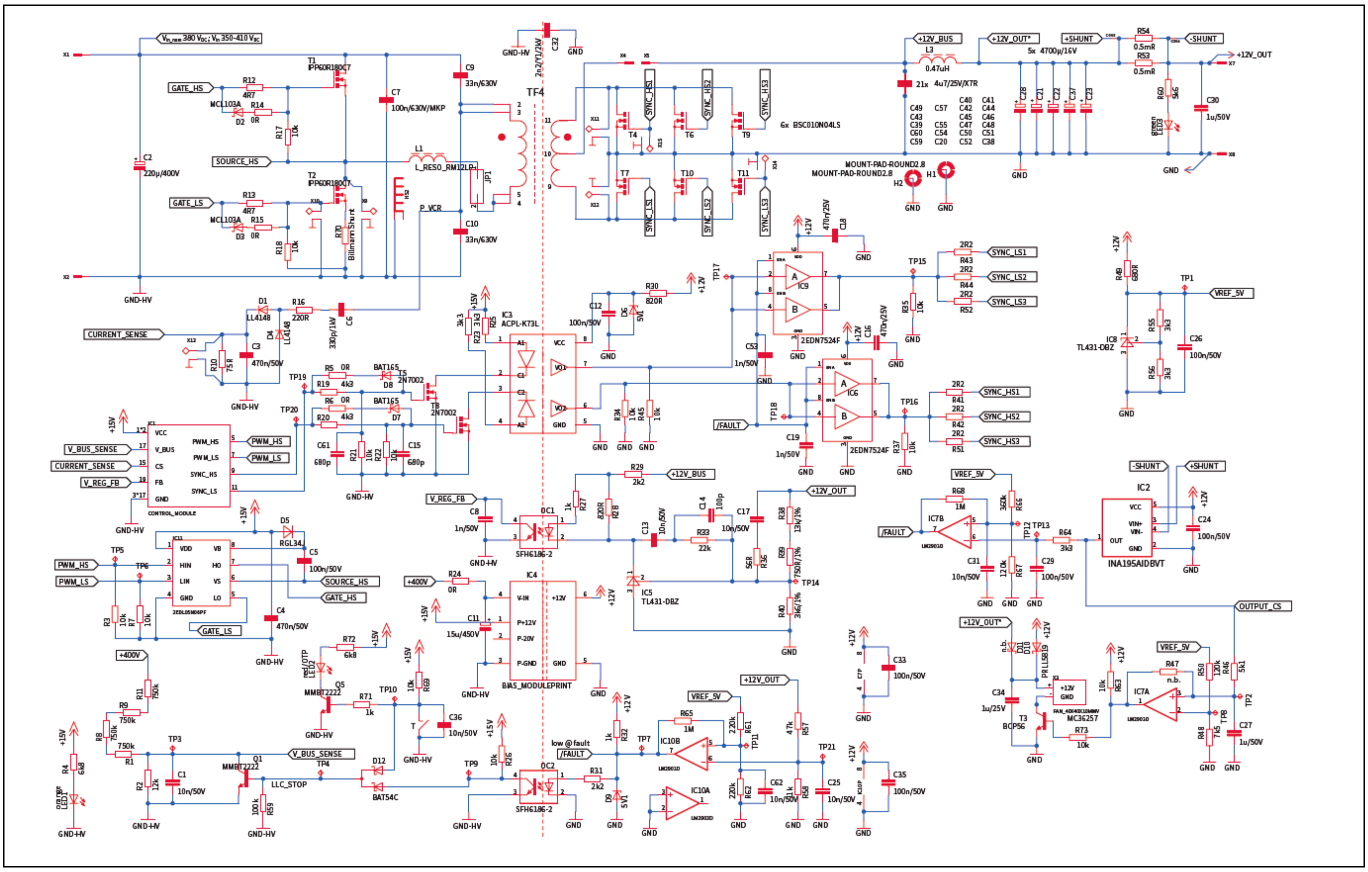


Figure 9 Mainboard schematic

3.3.2 Control board schematic

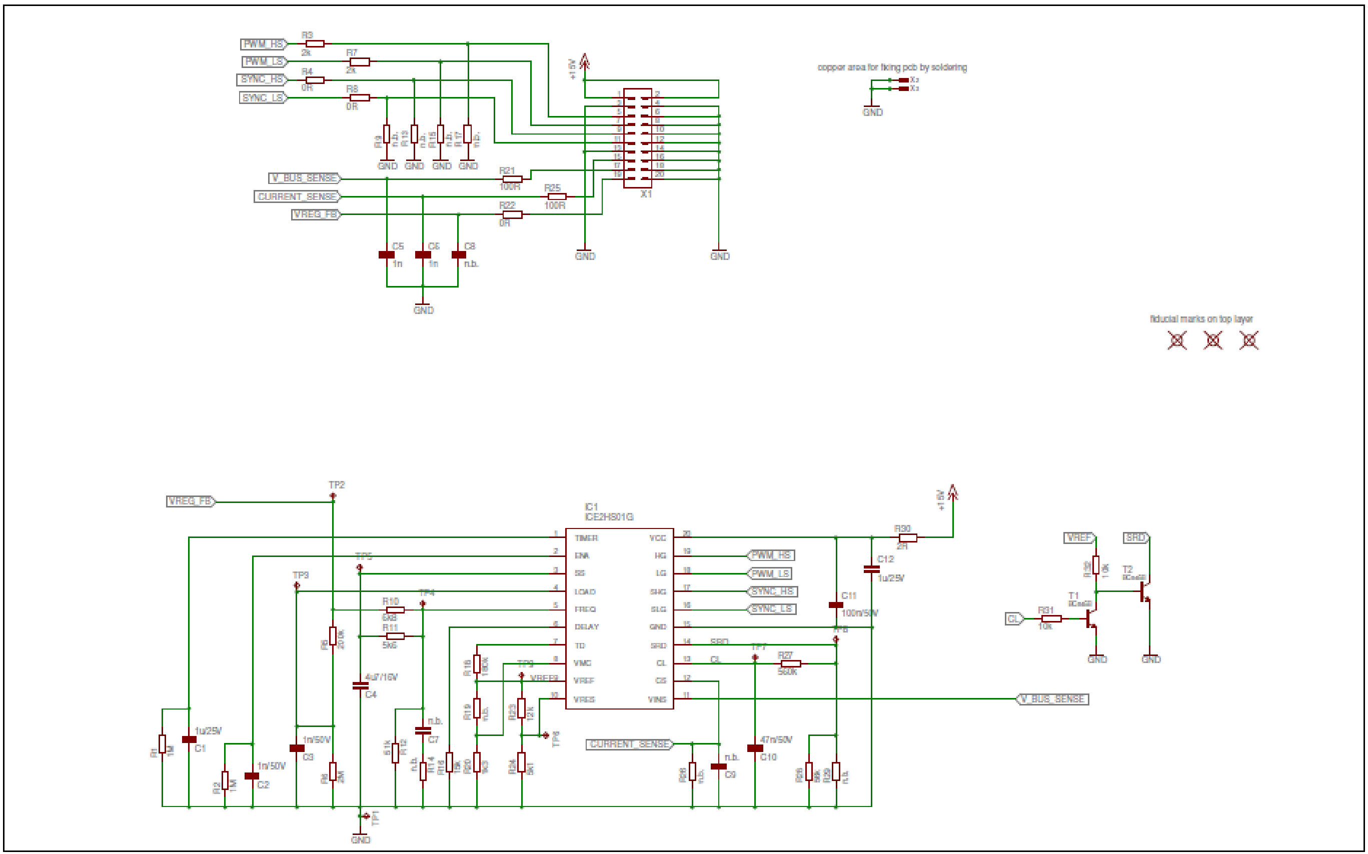


Figure 10 Control board schematic

3.3.3 Bias board schematic

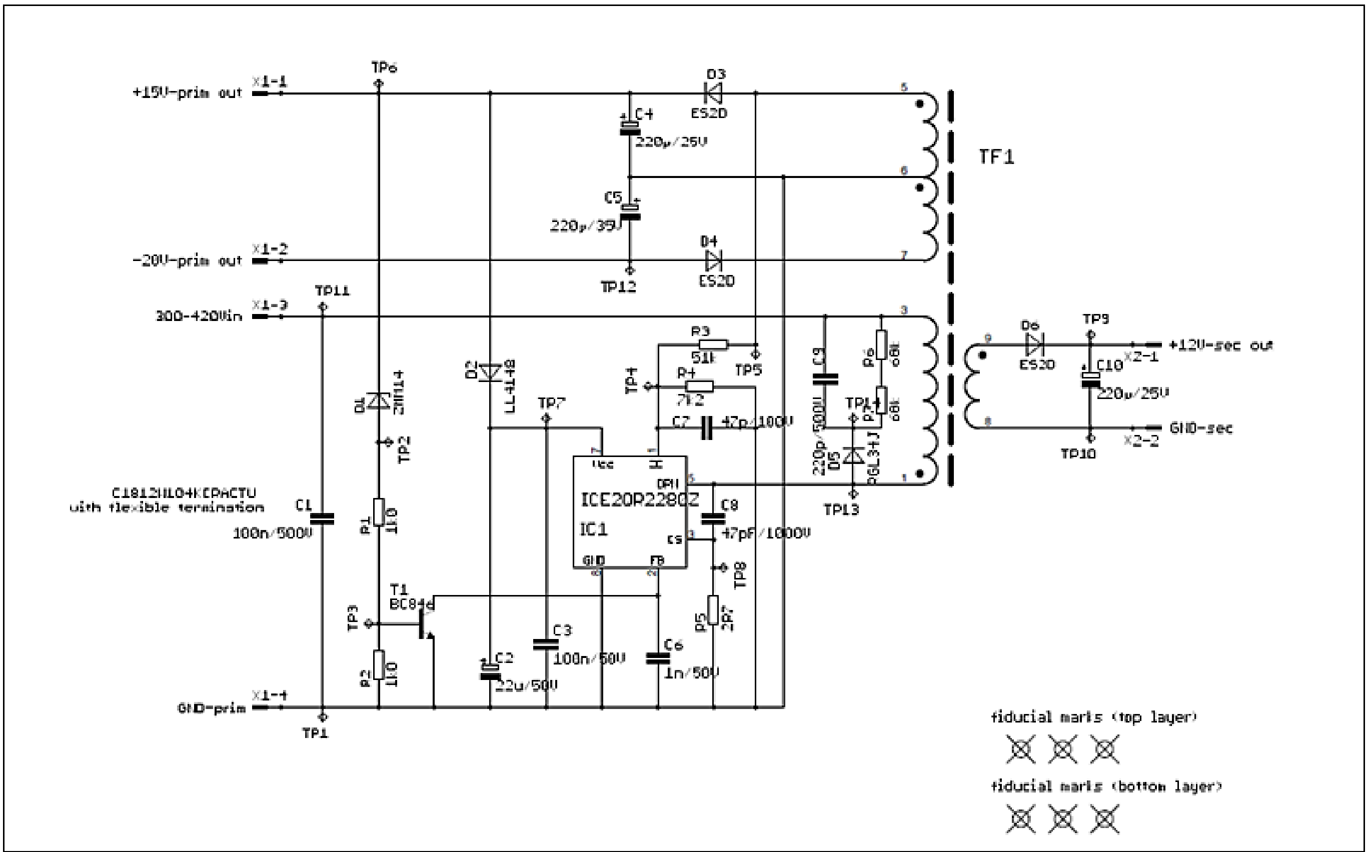


Figure 11 Bias board schematic

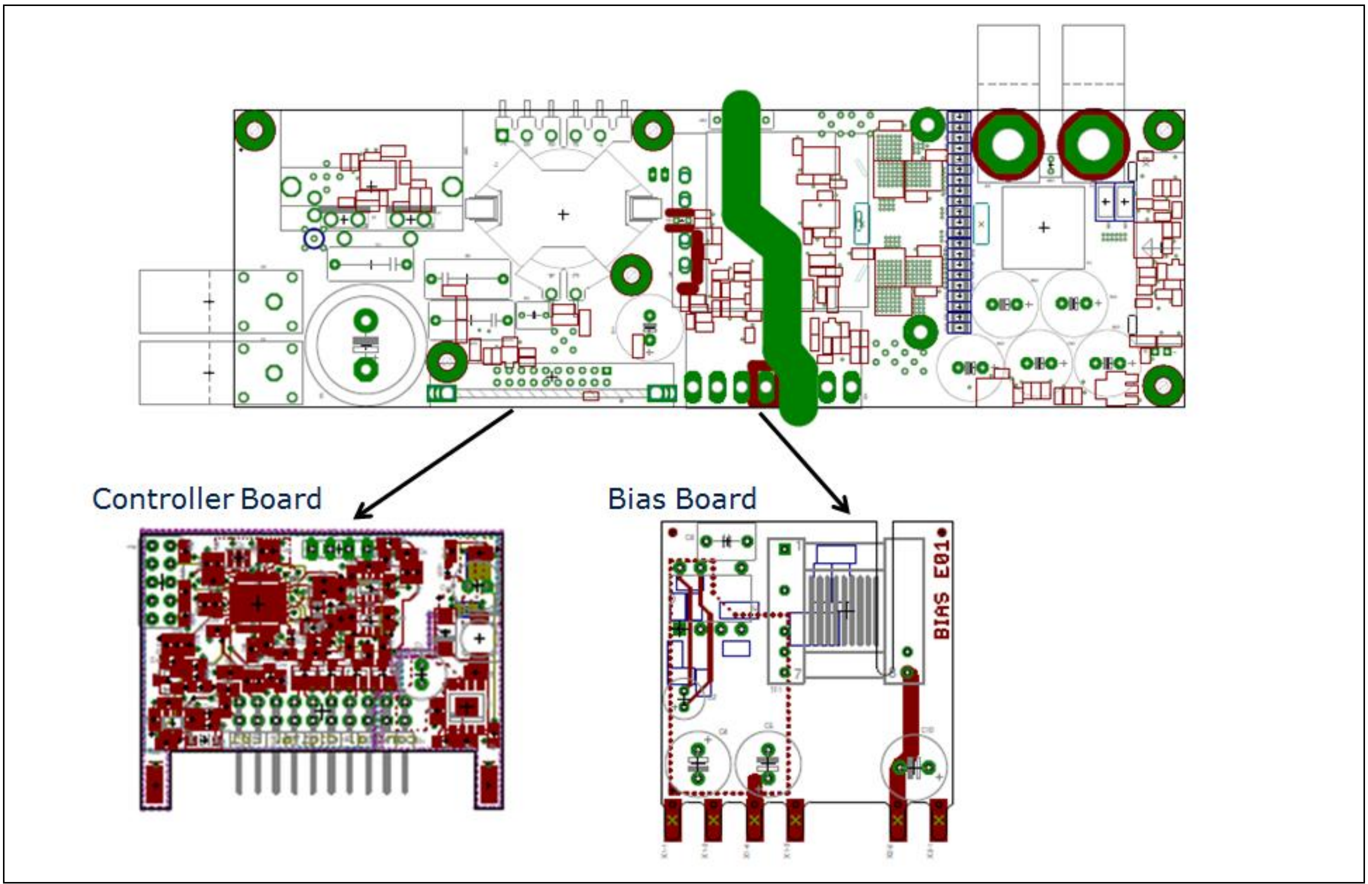


Figure 12 Mainboard PCB with control board and bias board

4 Typical characteristics with 600 V CoolMOS™ C7

4.1 Critical LLC operation - hard commutation

In LLC converter, hard commutation of the body diode normally only occurs during the startup, burst mode, overload, and short circuit condition. These conditions can be minimized if not avoided in the design using an analog controller with proper selection of resonant components and proper setting of the minimum and maximum operating frequency. Hard commutation happens in LLC during the commutation period of the body diode. During this time, resonant inductor current is flowing through body diode of the MOSFET creating ZVS condition upon the turn-on of the MOSFET. When the current cannot change its direction prior to the turn-on of the other MOSFET, more charges will remain in the P-N junction of that MOSFET. When the other MOSFET turns on, a large shoot-through current will flow due to the reverse-recovery current of the body diode. This results to a high reverse recovery peak current I_{RRM} and high reverse recovery dv/dt which sometimes could result in a MOSFET breakdown.

In this 600 W LLC analog controlled demonstration board, only the burst mode condition has the tendency of undergoing hard commutation. In Figure 13, hard commutation at burst mode is minimal that IPP60R180C7 was able to withstand without any problem.

Figure 13 Hard commutation during burst mode operation, V_{DS_pk} , $V_{GS\_max/min}$ and I_{RMM}

The voltage spike on the gate V_{GS} and drain V_{DS} can be influenced by varying both turn-on and turn-off gate resistors up to 10 Ω, without affecting the efficiency, due to the switching behavior of the C7 technology.

Due to the carefully designed control loop on this 600 W analog LLC demonstration board, no hard commutation is observed during start-up or short-circuit conditions.

4.2 Full ZVS area

Nearly full ZVS is achieved on the entire output load range as shown in Figure 14.

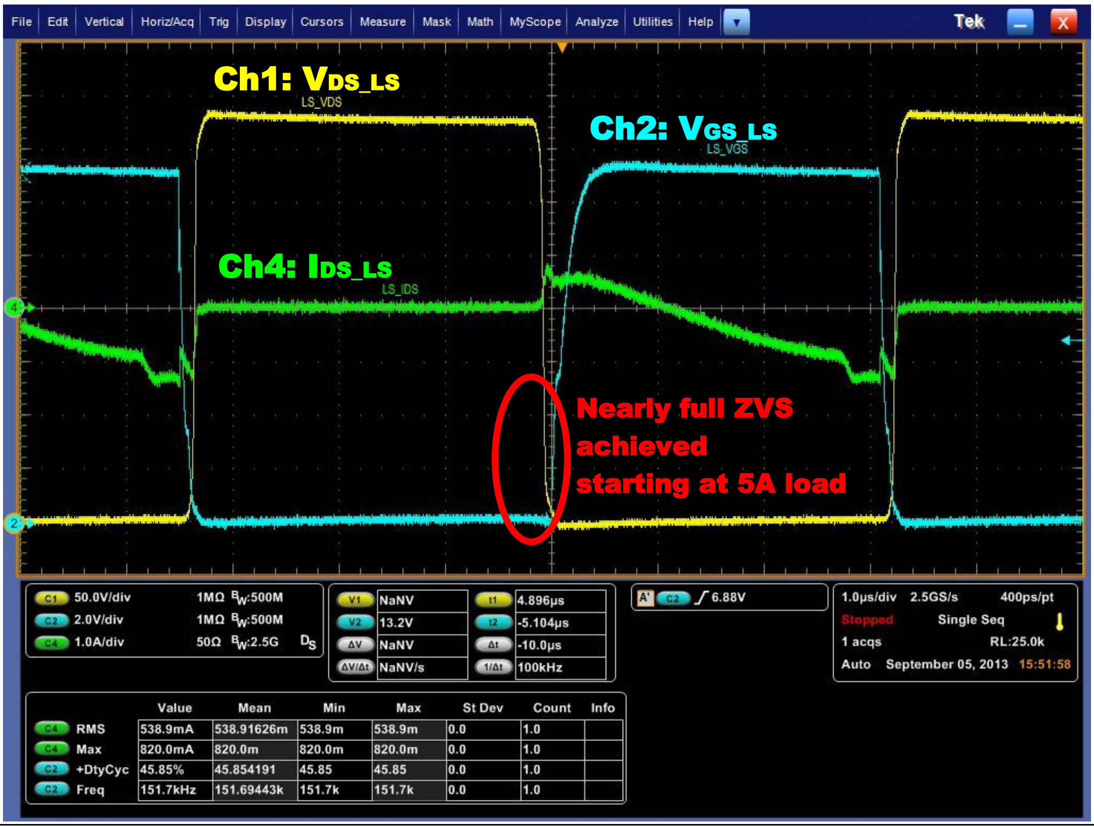


Figure 14 Nearly full zero voltage switching (ZVS) starting at 5 A load

4.3 Burst-mode operation

At no load or a very light load condition, LLC controller provides frequency approaching its maximum setting. In this condition, to still achieve full ZVS, magnetizing current should be high enough to discharge the output capacitances. Due to magnetizing current limitations, switching losses, especially turn-off losses, are relatively high if the devices continue to switch at the highest frequency. To overcome this phenomenon, burst-mode function is enabled and implemented. This results in effective lower switching losses and driving losses because of the low burst frequency. Additionally, this helps to achieve regulation even at no load condition. In Figure 15, one can see the waveform of burst-mode operation at no-load and/or very light load condition.

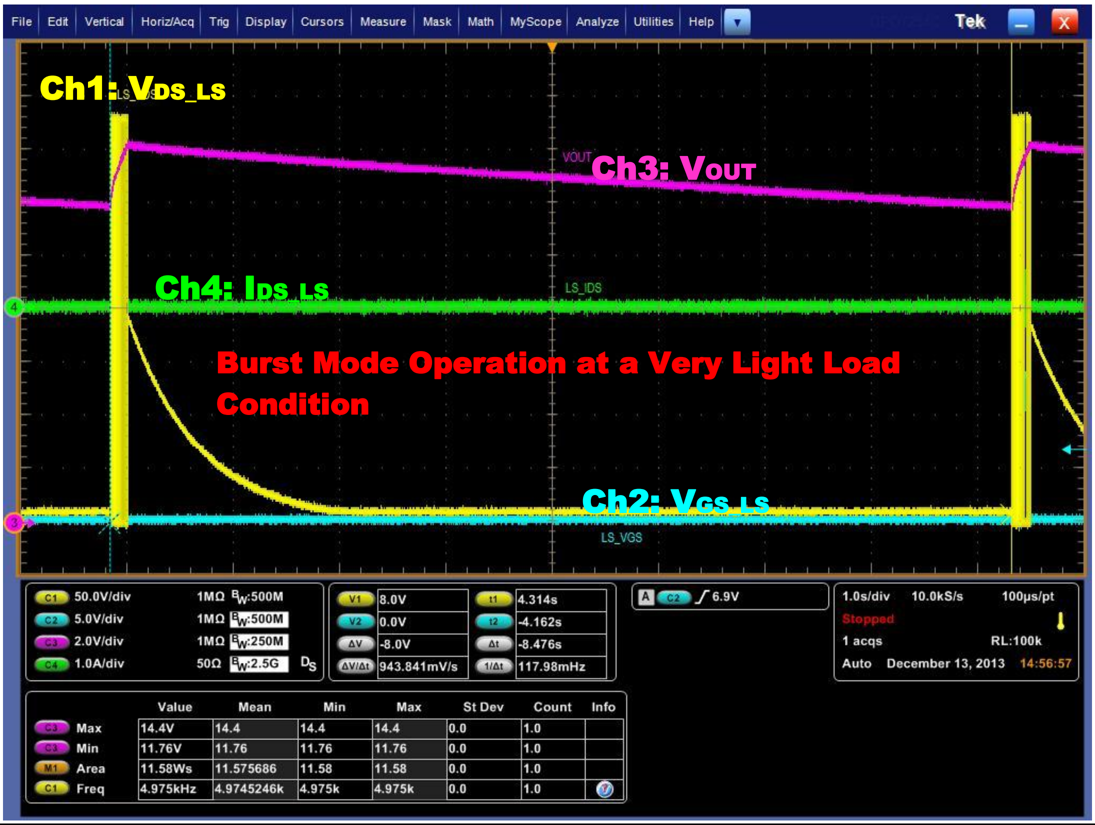


Figure 15 Burst-mode operation at no-load and/or very light load condition

4.4 Efficiency plot

Figure 16 shows the efficiency plot, measured in the 600 W LLC evaluation board with reference to the 80PLUS® Titanium Efficiency Standard (applied to the only HV DC/DC stage). At the most important point (50% load), this LLC board offers 0.3 % margin compared to the Titanium Efficiency Line.

The efficiency plot has been measured without including the bias and the fan absorption.

In fact, in typical single-output power supply (often used in rack mount servers and blade server applications) the fans are sized not only to remove heat from the power supply but also the heat from the system. For this reason, also to facilitate the system designer's use of different cooling strategies for the system, the power consumed by the fan is not included for efficiency calculations. If the power supply has an internal fan, then the manufacturer gives provision to supply external power to the fan during the power supply efficiency testing.

In our concept, we intentionally focus the application note on the LLC design independently from the design of the auxiliary bias, which can be more or less efficient according to the topology chosen for the auxiliary converter and the target of light load efficiency.

Our 600 W LLC is able to fulfill with enough margins the 80+ Titanium Standard requirements for the HV DC-DC stage.

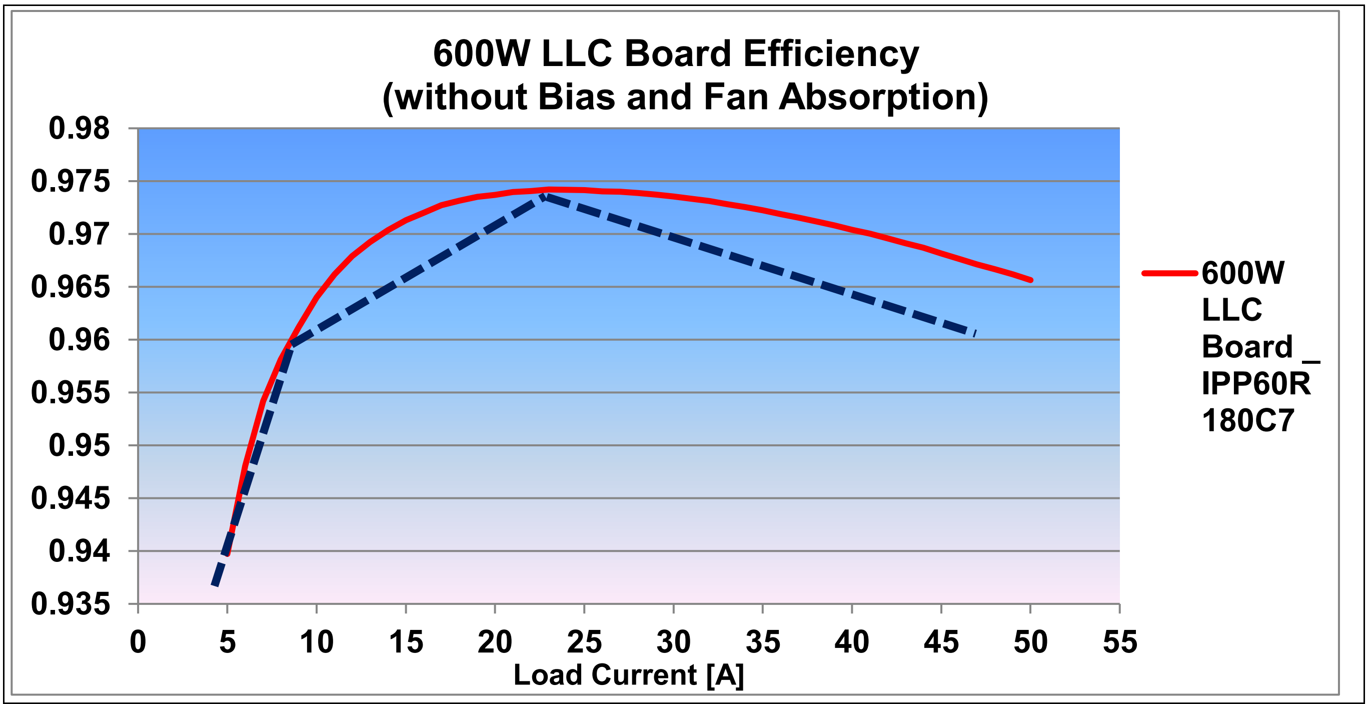


Figure 16 IFX 600 W LLC demonstration board efficiency vs Titanium Standard Efficiency

5 Test/powerup procedure

Table 2 Test/powerup procedure

Test	Test procedure	Condition
1. Auxiliary Circuit Turn-On	Apply 30 V_{DC} on the input	V_{in}: ~30 V_{DC}
		Orange LED will light up
2. LLC Converter Turn-On	Apply 350 V_{DC}. Converter will give V_{out} = 12 V_{DC}	V_{in}: 350 V_{DC}
		V_{out}:12 V
3. Operational switching frequency	Using voltage probe, monitor switching frequency at the following test conditions:	V_{in}:380 V_{DC}
		V_{out}:12 V
	At 5 A Output Load 10%Load - ~ 155 kHz*	**I_{out}: 5 A**
	At 25 A Output Load 50%Load - ~ 142 kHz*	**I_{out}: 25 A**
	At 50 A Output Load 100%Load - ~ 132 kHz*	**I_{out}: 50 A**
	*(*measure frequency at "Pri_LS_VGS"- connector)*	
	[* +/-10 kHz]	
4. Fan enable	Switch the load from 50 A to 5 A. Increase the output load current from 11-14 A, fan should turn on	V_{in} =380 V_{DC}
		I_{out}= 5 A
		ÞFan is off
		V_{in} =380 V_{DC}
		I_{out}= 11-14 A
		ÞFan is on
5. Switch off Input Start-up at no load	Switch off the input	V_{in}= 0 V_{DC}
		I_{out}= 0 A
	Switch at 380 V_{DC} on **no load output**. Operation should be in burst mode	V_{in} =380 V_{DC}
		I_{out} = 0 A
		V_{out} = 11,5 – 12,5
6. Switch off Input; Start-up at full load	Switch off the Input	**V_{in}= 0 V_{DC}**
		I_{out}= 0A
	Apply 380 V_{DC} with full load at 50 A output. V_{out} is in between 11.8 V_{DC} – 12.2 V_{DC}* *(*measure on the board-connector)*	V_{in} =380 V_{DC}
		V_{out}: 11,8 – 12,3 V_{DC}
		I_{out} = 50 A
7. Running no load -> output short-circuit	Switch off load from 380 V_{DC} **50 A** to 380 V_{DC} **0 A**	V_{in} =380 V_{DC}
		(after short-circuit) **V_{out} = 0 V_{DC}**

Test/powerup procedure

Test	Test procedure	Condition
	Short-circuit the load using the short-circuit function of the e-load. **Converter should latch**	**I_{out} = 0 A**
8. Switch off input and remove short-circuit	Switch off the input	**V_{in}= 0 V_{DC}**
9. Running full load -> overcurrent protection	Remove short-circuit function on the load	I_{out}= 0 A
	Apply 380 V_{DC} 50 A with full load output. Increase the current on the output 1 A each step until the converter goes into protection starting from 50 A. OCP occurs between 55 A and 62 A	V_{in} = 380 V_{DC}
		I_{out} = 50 A
		OCP = between 55 A – 62 A
10. Running full load -> output short-circuit	Apply 380 V_{DC} 50 A with full load output. Short circuit the load using the short circuit functions of the load. Converter should latch	I_{out} = 0 A
		V_{in} = 380 V_{DC}
		I_{out} = 50 A
		(after short circuit) **V_{out} = 0 V_{DC}**
11. Switch off Input; startup -> output short-circuit	Switch off the Input.	V_{in} = 0 V_{DC}
		I_{out} = 0 A
	Apply 380 V_{DC} with output load short circuit. *Converter should be in hiccup/latch mode*	V_{in} = 380 V_{DC}
		I_{out} = short-circuit
		V_{out} = 0 V short-circuit (hiccup/latch)
12. Switch off input and remove short-circuit	Switch off the Input	V_{in} = 0 V_{DC}
	Remove short-circuit function on the load	I_{out} = 0 A
13. Dynamic loading	Apply 380 V_{DC}. Set the electronic load to dynamic loading mode with the following settings:	V_{in} = 380 V_{DC}
	CCDH1: I_{out} 5 A	**I_{out} = 5 A to 50 A** **V_{out} = 11,5 V_{DC} – 12,5 V_{DC}**
	CCDH2: I_{out} 50 A	
	Dwell time: 10 ms	
	Load slew rate: 1 A/µS	

6 Related resources

- Primary HV MOSFETs CoolMOS™ IPP60R180C7
- LLC Analog Controller ICE2HS01G
- Advanced Dual-Channel Gate Drive 2EDN7524F
- Bias QR Flyback Controller ICE2QR2280Z
- SR MOSFETs OptiMOS™ BSC010N04LS
- Main Transformer and Resonant Choke Ferrite Cores
- Half Bridge Gate Drive 2EDL05N06PF

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[6] Infineon Technologies AG: *600 V CoolMOS™ C7 Design Guide*; Available online

Revision history

Document revision	Date	Description of changes
V 1.0	–	Initial release
V 1.1	–	Update on layout and structure
V 1.2	–	Update to Section 3.2.4
V 1.3	2026-01-27	Lifecycle review: Updated to the latest template

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