800 W ZVS phase shift full bridge evaluation board

Using 600 V CoolMOS™ CFD7 and digital control by XMC4200

About this document

Scope and purpose

This document describes the design and performance of an 800 W ZVS phase shift full bridge (PSFB) evaluation board intended for use in the isolated high voltage (HV) DC-DC stage of a switched mode power supply (SMPS) for server and industrial applications.

This is a high-performance example with a complete Infineon solution, including HV and LV power MOSFETs, controllers and drivers, demonstrating a very effective way to design the HV DC-DC stage of a server or industrial SMPS fulfilling the highest standard of efficiency and reliability. The overall best-in-class performance is achieved thanks to a mix of proper control techniques and best-in class power device selection.

Key Infineon products used to achieve this performance level include:

- 600 V CoolMOS™ CFD7 superjunction (SJ) MOSFET IPA60R280CFD7
- Advanced dual-channel gate driver 2EDN7524F
- Syncrec MOSFETs OptiMOS™ 5 BSC026N08NS5
- XMC4200 microcontroller
- Bias converter flyback controller + switch CoolSET™ ICE3RBR4765JZ

Along with design information and documentation on the phase shift (PS) converter, the reader will receive additional information on how the 600 V CoolMOS™ CFD7 behaves in ZVS PSFB applications and the associated benefits, how the high-performance magnetics design can be approached, and insights into how to develop the ZVS PSFB in similar power ranges adapted to specific requirements.

Intended audience

This document is intended for design engineers who wish to evaluate high-performance topologies for high-power SMPS converters, and develop an understanding of the design process and how to apply the ZVS PSFB design methods to their own system applications.

Note: *General knowledge about the soft-switching converters principle of operation is required for proper comprehension of the concepts reported in this paper.*

Keypoints

- Demonstrates a complete design methodology for ZVS PSFB converters using 600 V CoolMOS™ CFD7
- Explains digital control implementation with XMC4200 supporting both voltage and peak current mode for flexible performance tuning
- Describes planar transformer and integrated inductor design enabling high power density and reduced magnetic losses
- Provides insights into adaptive dead-time and synchronous rectification schemes for optimized switching and reduced conduction losses

- Evaluates thermal, efficiency, and protection performance under real-world conditions for server and industrial SMPS applications

About this product family

Product family

Infineon's CoolMOS™ is a high-voltage N-channel silicon power MOSFET that is designed to provide excellent thermal performance, lowest switching and conduction power losses, and optimal RDS(on) for increased system efficiency, supporting a range of application from low power levels to high power levels such as:

Target applications

- Consumer electronics
- Industrial applications
- Home appliances
- Server
- Telecom
- Renewables

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1 Introduction

In today's AC-to-DC power supplies used in server and telecom base station applications, there is a growing need for high efficiency combined with high power density. The trade-off challenges for designing such a power converter are centered on the MOSFETs and magnetics used in these high-power designs. Soft-switching topologies provide the ability to switch at high frequencies, thereby reducing the size of the magnetics and also reducing the losses in the MOSFETs during switching transitions. The zero voltage switched (ZVS) phase-shift full bridge (PSFB) is one of the most common soft-switching topologies used in the applications listed above.

This application note predominantly discusses the benefits of the new 600 V CoolMOS™ CFD7 MOSFET in a ZVS PSFB topology. The 800 W ZVS PSFB evaluation board is based on IPA60R280CFD7, and the benefits of the CFD7 technology are clearly demonstrated here.

The highly innovative digital control scheme based on the XMC4200 helps to achieve very high efficiencies of more than 96% at half load and more than 93% efficiency at light load, targeting the HV DC-DC stage of an 80+ Platinum SMPS. Both peak current mode and voltage mode have been implemented and are available as possible options for the converter control. A Graphical User Interface (GUI) running under Windows has been designed in order to help the user in the interaction with the demo board simply using a PC/laptop through a serial communication (UART).

The innovative planar magnetic design and optimal layout enable a very compact form factor in the range of 40 W/inch^3 power density.

1.1 CoolMOS™ CFD7 feature sets

The critical MOSFET parameters required in a ZVS PSFB converter are:

- Gate charge Q_g
- Output capacitance C_{oss}
- Body-diode Q_{rr}, t_{rr} and I_{rrm}
- On-resistance $R_{DS(on)}$

A typical loss breakdown in a ZVS PSFB converter ([1], [4]) will show that one of the main losses in the converter is due to the primary switching MOSFETs. We can further break down these losses within the MOSFETs and conclude that a significant percentage of losses at light-load (10%) operation is due to the MOSFET driving. The driving losses are directly proportional to the MOSFET gate charge Q_g. IPA60R280CFD7 has the lowest Q_g as compared to competition parts of the similar $R_{DS(on)}$ class. The low Q_g also enables fast-switching. The conduction losses form a major percentage of losses within the MOSFET during full-load (100%) operation. They are directly proportional to the MOSFET on-resistance $R_{DS(on)}$. The CFD7 technology has one of the lowest $R_{DS(on)}$ per package available in the market, to enable high efficiency at full-load operation, without sacrificing any power density requirement. The benefits of reduction in Q_g and $R_{DS(on)}$ are directly visible in the efficiency improvements which are demonstrated towards the end of this application note.

Another critical parameter for efficiency improvement in a ZVS PSFB topology is the MOSFET E_{oss}, which is the energy stored in its output capacitance. Lower MOSFET E_{oss} helps in selecting a smaller resonant inductor, which is necessary for the resonant tank in the bridge.

Other than the light-load and full-efficiency benefits, the IPA60R280CFD7 also makes the body-diode rugged, which is essential in topologies like the ZVS PSFB.

1.2 CoolMOS™ CFD7 vs CoolMOS™ CFD2

In this paragraph the benefits of CoolMOS™ CFD7 are compared to the older CoolMOS™ CFD2 technology. The CFD2 is the well-proven predecessor of CFD7. The main features and benefits of CoolMOS™ CFD2 are documented in the application note “650 V CoolMOS™ CFD2” released by Infineon in February 2011 [2]. Figure 1a shows a quantitative comparison between IPA60R280CFD7 (green columns) and IPA60R310CFD2 (gray columns), which is provided to show the improvements gained from the new CoolMOS™ CFD7 technology. The most relevant differences between key parameters of the two technologies are shown with the corresponding impact on performance.

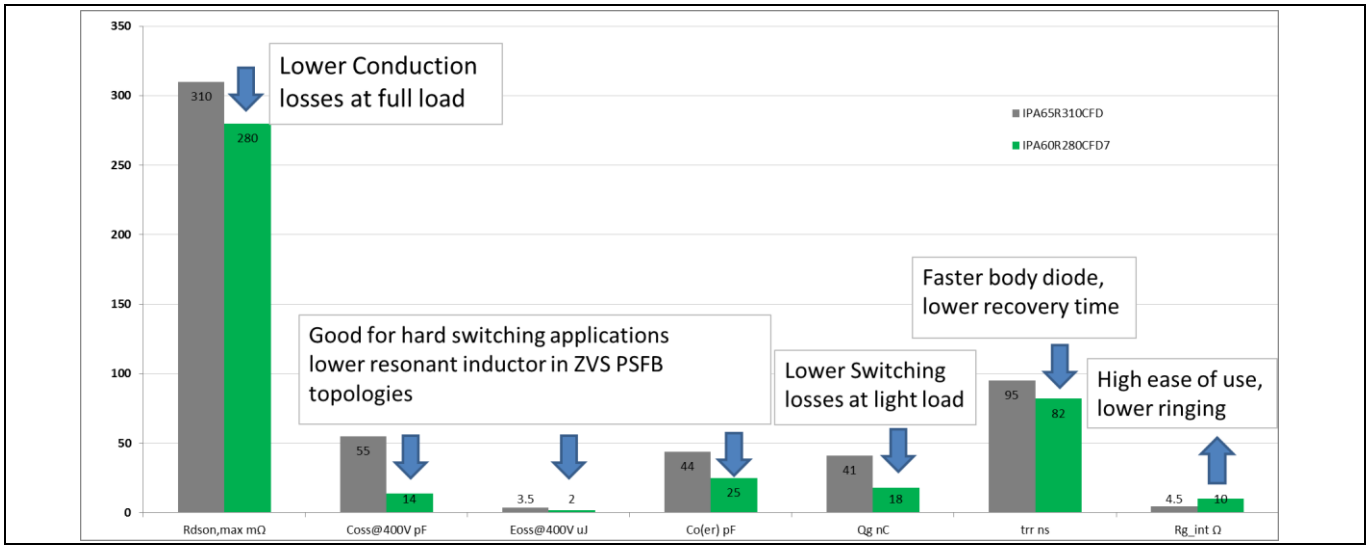

Figure 1 IPA60R280CFD7 vs. IPA65R310CFD key datasheet parameter comparison and key benefits

Trade-offs involving adjustments of delay times, dimensioning of the resonant inductance and impact of $R_{G(ext)}$ optimization of primary-secondary MOSFET delays will be explained in detail in this paper. General guidelines for a ZVS PS design methodology are available in the previous application note “ZVS PSFB CFD2 optimized design” released by Infineon in March 2013 [2]. In this application note, we focus on the innovative digital control and planar magnetic design.

The main focus of this application note is on the waveforms analysis in a “real” application board which has similar power densities as the best commercial variants available in the market. Digital control technique and the design tradeoffs involving the ZVS PS topology such as placement of the clamp diodes, current sensing and planar magnetic design are explained in details in the subsequent sections.

The measurement results are available in the last section of the application note. The high-efficiency benefits of IPA60R280CFD7 are compared with IPA65R310CFD and some relevant competitors.

2 Design concept

The demo board has been designed according to the typical requirements of the HV DC-DC stage of a server or industrial SMPS:

- Input voltage range: 350–410 V DC
- Nominal input voltage: 400 V DC
- Output voltage: 12 V±4%
- Max. output current/power: 67 A/800 W
- Efficiency: ≥ 93% at 20% load, ≥ 96% at 50% load, ≥ 96% at full load (target: 80+ Platinum)
- 1U form factor
- Power density: 40 W/inch^3
- f_{sw} = 100 KHz

2.1 ZVS PSFB converter

The ZVS PSFB is one of the most popular soft-switching topologies in use in HP SMPS applications. Introduced in the 1990s [5], it has immediately gained popularity within the power electronic designer community due to the relatively smooth way in which it minimizes switching losses even without fully resonant operation, thus avoiding all the pitfalls associated with the resonant approach.

There was trouble when this topology started being used only as a result of certain critical operating conditions, such as output short-circuit, especially starting from no-load operation. In fact some apparently inexplicable failures started happening around the world, mainly related to the unavoidable usage of the MOSFET intrinsic body-diode [6]. Nowadays these conditions are fully understood: the usage of appropriate control techniques, combined with the selection of proper HV MOSFETs in the full-bridge prevents any problems like those described above.

More precisely, the advent of CoolMOS™ technology, with a vertical structure based on the superjunction concept, has removed all the possible failure mechanisms linked to the parasitic bipolar transistor (BJT) ignition, one of the root causes of the initial troubles in this topology (see [7] for more details).

Moreover, it has been demonstrated that a MOSFET with a fast body-diode is intrinsically able to prevent any problem in those conditions (see [1] for more details).

The CoolMOS™ CFD7 technology provides a fast and rugged body-diode, suitable for this topology, as well as an excellent switching Figure of Merit (FOM), in order to allow reliable operation in high-performance converters.

2.1.1 Principle of operation

The ZVS PSFB topology principle of operation is already described in [1]. For the reader’s convenience, Figures 2 and 3 recap the fundamental steps.

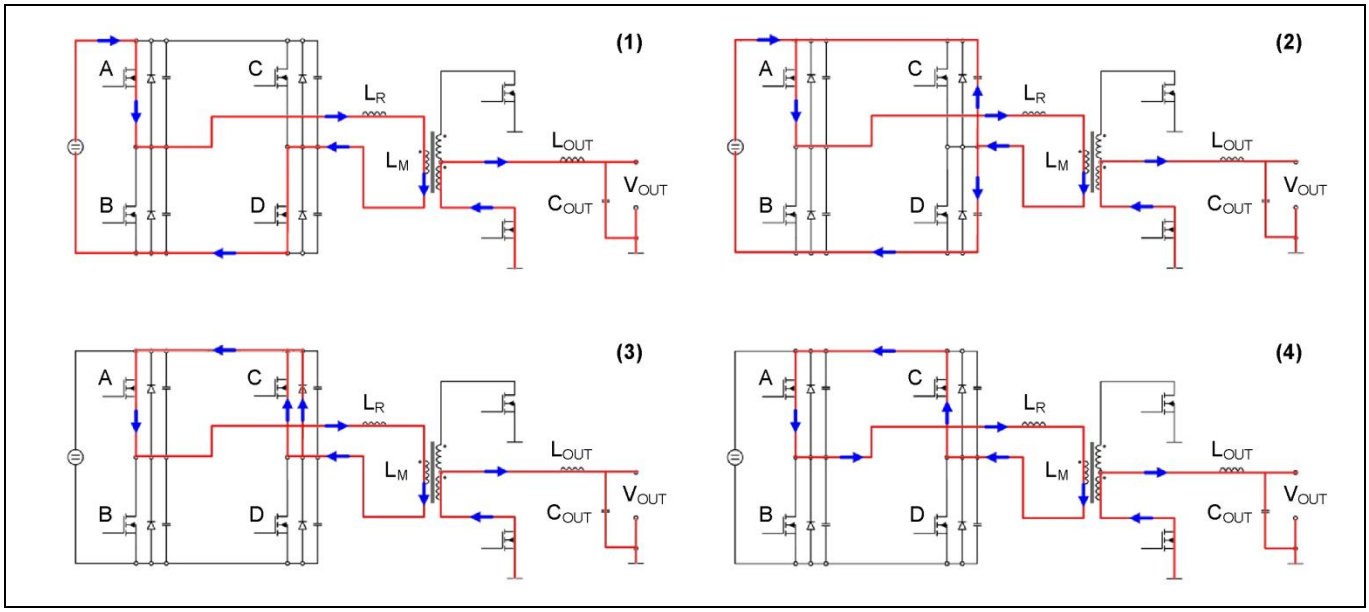

Figure 2 ZVS PSFB principle of operation: phases 1–4

1. Power transfer phase: MOSFETs A and D are turned on and the current flows as shown in the diagram. During this phase, the primary current is rising according to the value of the total primary inductance
2. The second phase is responsible for the zero-voltage switching of MOSFET C. In order to reach a zero-voltage turn-on, the energy stored in the resonant inductance is used to discharge the output capacitance of MOSFET C and charge the output capacitance of MOSFET D
3. After the output capacitance of MOSFET C is discharged, the current is commutating to the body-diode of MOSFET C
4. MOSFET C is actively turned on and the current is flowing through the channel and not through the body-diode anymore. This phase is also called the “freewheeling phase”

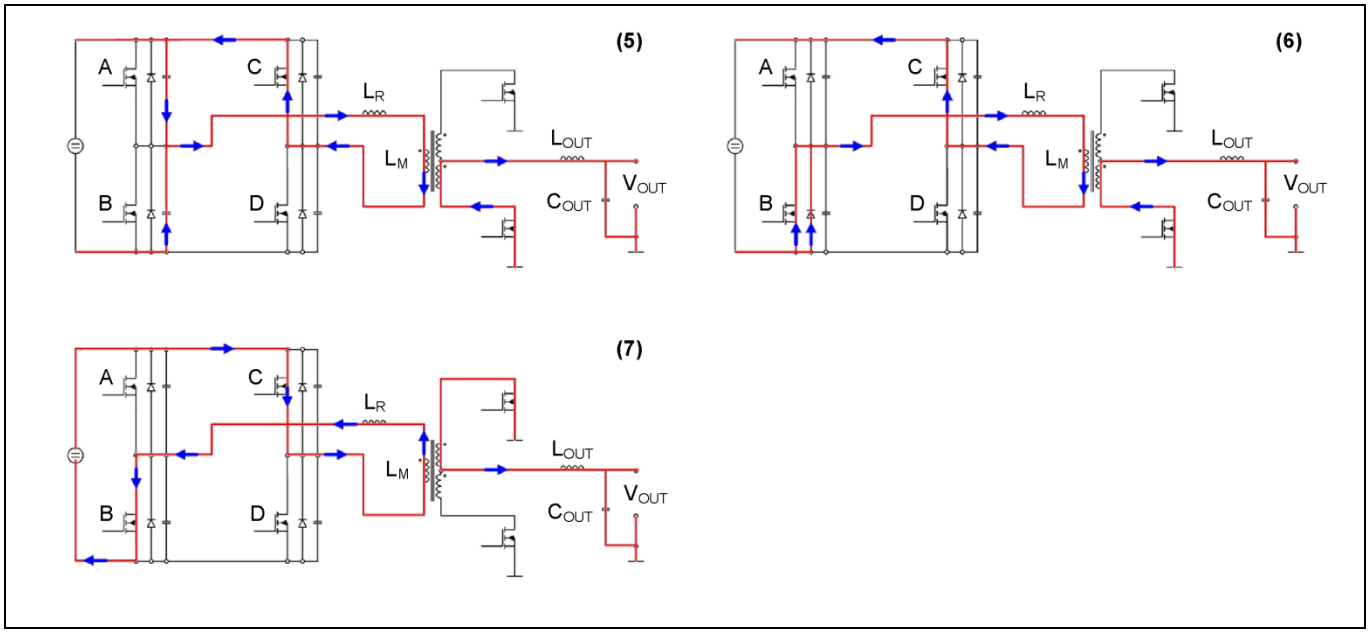

Figure 3 ZVS PSFB principle of operation: phases 5–7

5. In order to start a new power transfer phase MOSFET B is turned on. This phase is achieved in the same way as phase 2 by turning off MOSFET A. The output capacitance of MOSFET A is charged and the output capacitance of MOSFET B is discharged before actively switching on the MOSFET
6. The body-diode conduction time of MOSFET B, which is visible in this phase, should also be reduced to a minimum as in phase 3
7. MOSFET B is actively turned on, the current changes its direction and the next power transfer phase starts

Figure 4 shows the control signals applied to the four MOSFETs of the bridge.

(1) and (7) are power transfer phases, whose duration defines the total effective on-time (and thus the duty cycle), which is given by the overlapping conducting period of the MOSFET on the same diagonal (A–D and B–C). The time intervals (2)–(3) and (5)–(6) are also called dead times: they represent the time between the turn-off and turn-on of the MOSFETs on the same leg. They must be set long enough in order to achieve the Zero Voltage Switching (ZVS) turn-on.

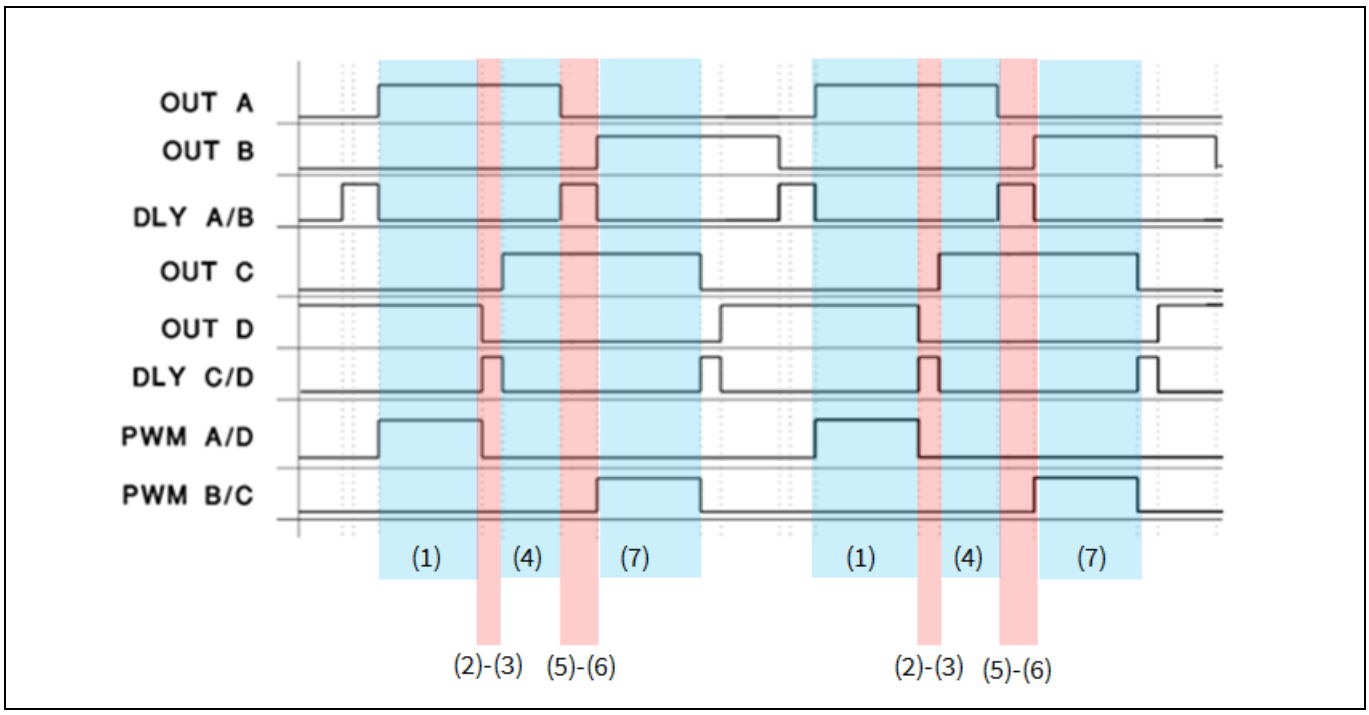

Figure 4 Control signals in the ZVS PSFB operation

It can be observed that the duration of these two times is not equal: the one applied to the C–D leg is lower compared to the one applied to the A–B leg. This is because C–D starts a ZVS transition after a power transfer phase, so with more resonant energy available compared to A–B, which starts the transition before the power transfer.

For this reason C–D is commonly called the “lagging leg” and A–B the “leading leg”.

Thus, assuming the same MOSFETs (C_{oss}) are used in the two legs, the time needed to discharge the output capacitance is obviously lower for the lagging leg compared to the leading leg.

Further and more detailed explanations of the ZVS PSFB topology operation and control, including the secondary synchronous rectification, are reported in section 4 of this document.

2.2 Planar transformer technique

The main transformer has been designed using a planar structure. This development has been carried out by Infineon in cooperation with the company Payton Planar Magnetics Ltd.

Planar technology is optimal for producing highly interleaved transformers. This high interleaving, if used correctly, can reduce leakage inductance and significantly reduce the proximity effect losses in the transformer.

As switching frequency increases, the need for reducing proximity effect losses becomes more important.

With its superior conduction cooling and highly repeatable results, planar technology is best suited to most high-efficiency high frequency transformer designs.

As with all technologies, it is imperative to use it accurately in order to maximize performance. That is why custom-made designs are a crucial part in any power supply design aiming at maximizing efficiency and reducing size. Only a tailored solution will unlock the full potential of any technology.

By combining the strength of planar technology, while maintaining wire-wound design, Payton Planar products strive to maximize efficiency and reduce size while meeting all of the power supply designer's requirements.

See [14] for more details about planar transformers in soft-switching DC-DC converters.

2.2.1 Concept

In the unique transformer design for the 800 W ZVS PSFB demo board a special multi-layer PCB has been used for the primary winding, with thick copper winding, and stamped copper lead frames for the secondary side. The special PCB design has been chosen to enable a high number of turns and at the same time meet the high insulation requirements. Using a PCB for winding also improves the reliability and repeatability of the winding.

Copper-stamped lead frames were used for the secondary side. The thick copper windings made it possible to handle the high currents on the secondary the side of the transformer typical of a server or industrial 12 V output SMPS.

In order to have a high interleaving count and improve proximity losses, the transformer has three separate unique PCB boards. Primary windings were sandwiched between the secondary lead frames, which helps to achieve very low proximity losses.

In order to reach the leakage inductance required to energize the ZVS behavior, without increasing proximity losses, an integrated inductor was designed on the top of the transformer. The integrated inductor has a magnetic flux in the opposite direction to the transformer magnetic flux, and in this way core losses can be reduced. This construction also saves on board space and height.

The inductor, as it cannot be interleaved having one winding, has been done with litz wire to improve its efficiency at high frequency. The inductor lead wires are connected through the transformer PCB. This connection combines two magnetic parts into one module with low losses and high leakage inductance value. This reduces the number of components, as the transformer and inductor can be considered as one module.

Figure 5 shows the concept, and the detailed spec of the transformer is available in section 3.3.1.

In conclusion, our planar concept is the best way to combine high power density, reduced AC and core losses, high current capability and very good reproducibility in mass production: all are important requirements in high-power high-performance SMPS for server and industrial applications.

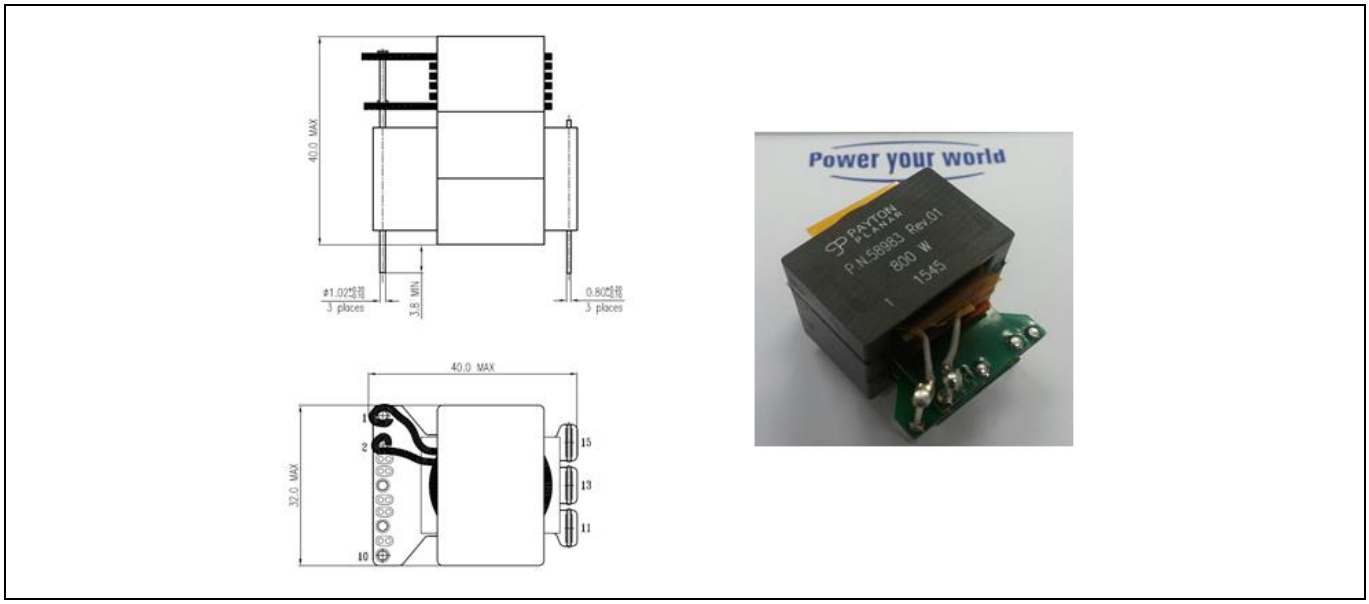

Figure 5 Main transformer: planar stacked structure

3 Board description

Figure 6 gives an overview of the demo board components.

It consists of a main power board (where the main transformer and all power components are assembled) and three daughter cards: the digital control, the synchronous rectification and the auxiliary converter cards, which can be easily identified below.

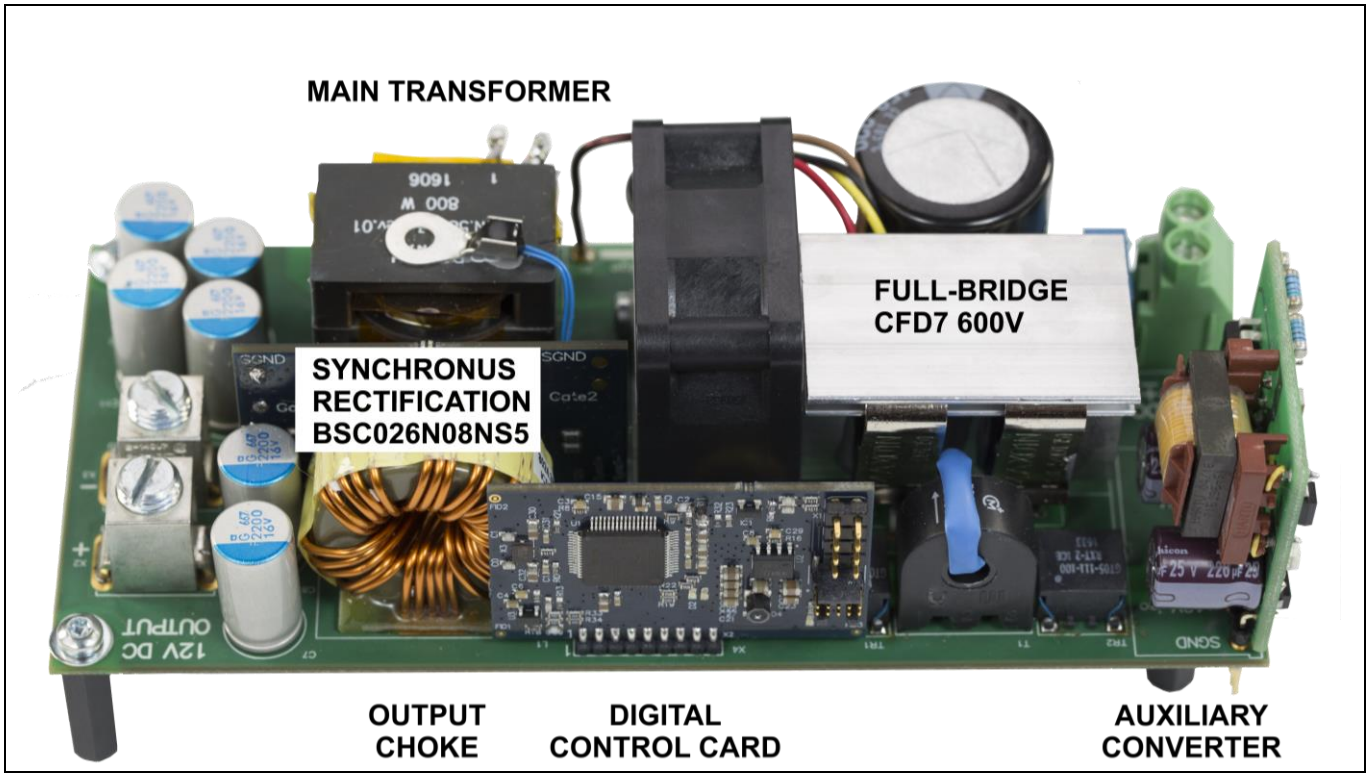

Figure 6 Board overview

3.1 Infineon components

3.1.1 Primary HV MOSFETs 600 V CoolMOS™ CFD7

CoolMOS™ is a revolutionary technology for HV power MOSFETs, designed according to the SJ principle and pioneered by Infineon Technologies. The latest CoolMOS™ CFD7 is the successor to the CoolMOS™ CFD2 series, and is an optimized platform tailored to target soft-switching applications such as PSFB (ZVS) and LLC. Resulting from reduced gate charge (Q_g), best-in-class reverse recovery charge (Q_{rr}) and improved turn-off behavior, CoolMOS™ CFD7 offers the highest efficiency in resonant topologies. As part of Infineon's fast body-diode portfolio, this new product series blends all the advantages of a fast-switching technology together with superior hard-commutation robustness, without sacrificing easy implementation in the design-in process. The CoolMOS™ CFD7 technology meets the highest efficiency and reliability standards and furthermore supports high power density solutions. Altogether, CoolMOS™ CFD7 makes resonant switching topologies more efficient, more reliable, lighter, and cooler.

Features

- Ultra-fast body-diode
- Low gate charge

- Best-in-class reverse recovery charge (Q_{rr})
- Improved MOSFET reverse diode dv/dt and di/dt ruggedness
- Lowest FOM $RDS_{(on)}$*Q_g and $RDS_{(on)}$*E_{oss}
- Best-in-class $RDS_{(on)}$ in SMD and THD packages
- Qualified for industrial-grade applications according to JEDEC (J-STD20 and JESD22)

Benefits

- Excellent hard-commutation ruggedness
- Highest reliability for resonant topologies
- Highest efficiency with outstanding ease-of-use/performance trade-off
- Enabling increased power density solutions

Applications

- Suitable for soft-switching topologies
- Optimized for PSFB (ZVS), and LLC stages in server, telecom, EV charging applications

3.1.2 Advanced dual-channel gate driver 2EDN7524

The fast dual-channel 5 A non-isolated gate driver is an advanced dual-channel driver optimized for driving both standard and SJ MOSFETs, as well as GaN power devices, in all applications in which they are commonly used. The input signals are Transistor-Transistor Logic (TTL) compatible with a high-voltage capability of up to 20 V and down to -5 V. The unique ability to handle -5 V DC at input pins protects the IC inputs against GND-bounce transients.

Each of the two outputs is able to sink and source up to 5 A current, utilizing a true rail-to-rail stage, which ensures very low impedances of 0.7 Ω up to the positive and 0.55 Ω down to the negative rail respectively. Very low channel-to-channel delay matching is implemented, typically 1 ns, which enables the double source and sink capability of 10 A by paralleling both channels.

Different logic input/output configurations guarantee high flexibility for all applications; e.g. with two parallel switches in a boost configuration. The gate driver is available in three package options: PG-DSO-8, PG-VDSON-8 and PG-TSDSO-8-X (size minimized DSO-8).

Main features

- Industry-standard pin-out
- Two independent low-side gate drivers
- 5 A peak sink/source output driver at V_{DD} = 12 V
- True low-impedance rail-to-rail output (0.7 Ω and 0.5 Ω)
- Enhanced operating robustness due to high reverse current capability
- -10 V DC negative input capability against GND-bouncing
- Very low propagation delay (19 ns)
- Typically 1 ns channel-to-channel delay matching
- Wide input and output voltage range up to 20 V
- Active low-output driver even on low power or disabled driver
- High flexibility through different logic input configurations
- PG-DSO-8, PG-VDSON-8 and TSSOP-8 packages

- Extended operation from -40°C to 150°C (junction temperature)
- Particularly well suited to driving standard MOSFETs, SJ MOSFETs, IGBTs, or GaN power transistors

3.1.3 Syncrec MOSFETs OptiMOS™ 5 BSC026N08NS5

OptiMOS™ 5 80 V, Infineon's latest generation of medium voltage power MOSFETs, are especially designed for synchronous rectification in telecom and server power supplies. In addition, these devices can also be utilized in other industrial applications such as solar, low voltage drives and adapters.

The OptiMOS™ 5 80 V MOSFETs yield designs with the lowest synchronous-rectification losses: the extremely low $R_{DS(ON)}$ allied with extremely low output (Q_{oss}), reverse recovery (Q_{rr}) and gate charges (Q_g) reduce not only conduction losses but also switching losses.

The OptiMOS™ 5 80 V SynchRec MOSFET low-output and reverse-recovery charges drain less energy from the input voltage source through the isolation transformer, increasing the converter efficiency. Moreover, these low charges also store less energy in the isolation transformer leakage inductance and in the primary-side resonant inductor, yielding not only an overshoot with low energy on the SynchRec MOSFET being blocked, but also low recirculated current through the primary-side inductor clamping diodes, which also contribute positively to the converter efficiency.

Finally, the OptiMOS™ 5 80 V MOSFET low gate charge alleviates the burden on the SynchRec driver circuitry, especially in high-power designs like this one, which employ many parallel SynchRec MOSFETs.

Summary of features

- Optimized for synchronous rectification
- Ideal for high switching frequency
- Optimized $C_{oss} \times R_{DS(on)}$ FOM

Benefits

- Highest system efficiency
- Reduced switching and conduction losses
- Less paralleling required
- Increased power density
- Low voltage overshoot

3.1.4 XMC4200

The XMC4200 combines Infineon's leading-edge peripheral set with an industry-standard ARM® Cortex®-M4F core.

The control of SMPS is a strong focus for XMC™ microcontrollers, where users can benefit from features such as smart analog comparators, high-resolution Pulse Width Modulation (PWM) timers and the ARM® Cortex®–M4F DSP instruction set, including floating-point or high-precision analog-to-digital converter.

As a key feature it offers a high-resolution PWM unit with a resolution of 150 ps. This unique peripheral makes it especially suitable for digital power conversion in applications such as solar inverters as well as SMPS and uninterruptible power supplies (UPS).

The XMC4200 is supported by Infineon's integrated development platform DAVE™, which includes an IDE, debugger and other tools to enable a fast, free-of-charge, and application-oriented software development.

Summary of XMC4200 key features

- ARM® Cortex®-M4F, 80 MHz, including single-cycle DSP MAC and Floating Point Unit (FPU)
- CPU frequency: 80 MHz
- High ambient temperature range: -40°C to 125°C
- Wide memory size options: up to 512 kB of flash and 80 kB of RAM
- HRPWM (High Resolution PWM) allowing PWM adjustment in steps of 150 ps
- 12-bit ADC, 2 MSample/sec. Flexible sequencing of conversions including synchronous conversion of different channels
- Fast and smart analog comparators offer protections such as overcurrent (OC) protection, including filtering, blanking, and clamping of the comparator output. A 10-bit DAC with a conversion rate of 30 MSamples/sec provides an internal reference for the comparators that can be configured to be a negative ramp for slope compensation purposes
- A flexible timing scheme due to capture and compare unit (CCU) timers and HRPWM. These timers allow the creation of almost any PWM pattern and accurately synchronize PWM signals with ADC measurements
- Interconnection matrix to route different internal signals from one peripheral to another. For example, the comparator output can connect to a PWM timer to indicate an OC protection event and immediately switch off the PWM output
- Communication protocols supported, including USB, UART, I^2C, SPI

3.1.4.1 CCU8-PWM generation

The CCU8 is a multi-purpose timer unit for signal monitoring/conditioning and pulse width modulation (PWM) signal generation. It is designed with repetitive structures with multiple timer slices that have the same base functionality. The internal modularity of the CCU8 translates into a software-friendly system for fast code development and portability between applications [8].

Each CCU8x has four 16-bit timer slices, CC8y (y = 3-0), which can be concatenated up to 64-bit.

A slice has:

- One timer
- Four capture registers
- One period register
- Two compare registers

Its numerous key features for a flexible PWM generation scheme make it the perfect peripheral for PWM generation in SMPS. Some features include:

- Each timer slice of the CCU8 can operate in center-aligned or edge-aligned mode
- Additional operation modes like single-shot, counting or dithering modes are also available
- Complementary PWM signal generation with dead time
- HW asymmetric PWM generation for multi-channel/multi-phase pattern generation with parallel updates
- Additional external controllable functions give another degree of PWM manipulation (e.g. timer gate, timer load, timer clear, etc.)
- HW TRAP generation
- Both the period and compare registers have shadow registers
- Each slice can work independently and in different modes, and still be synchronized to other CCU8 slices

Due to all these features the CCU8 timer slices are used to drive the PSFB 800 W. See Figure 7 for some examples of CCU8 usage.

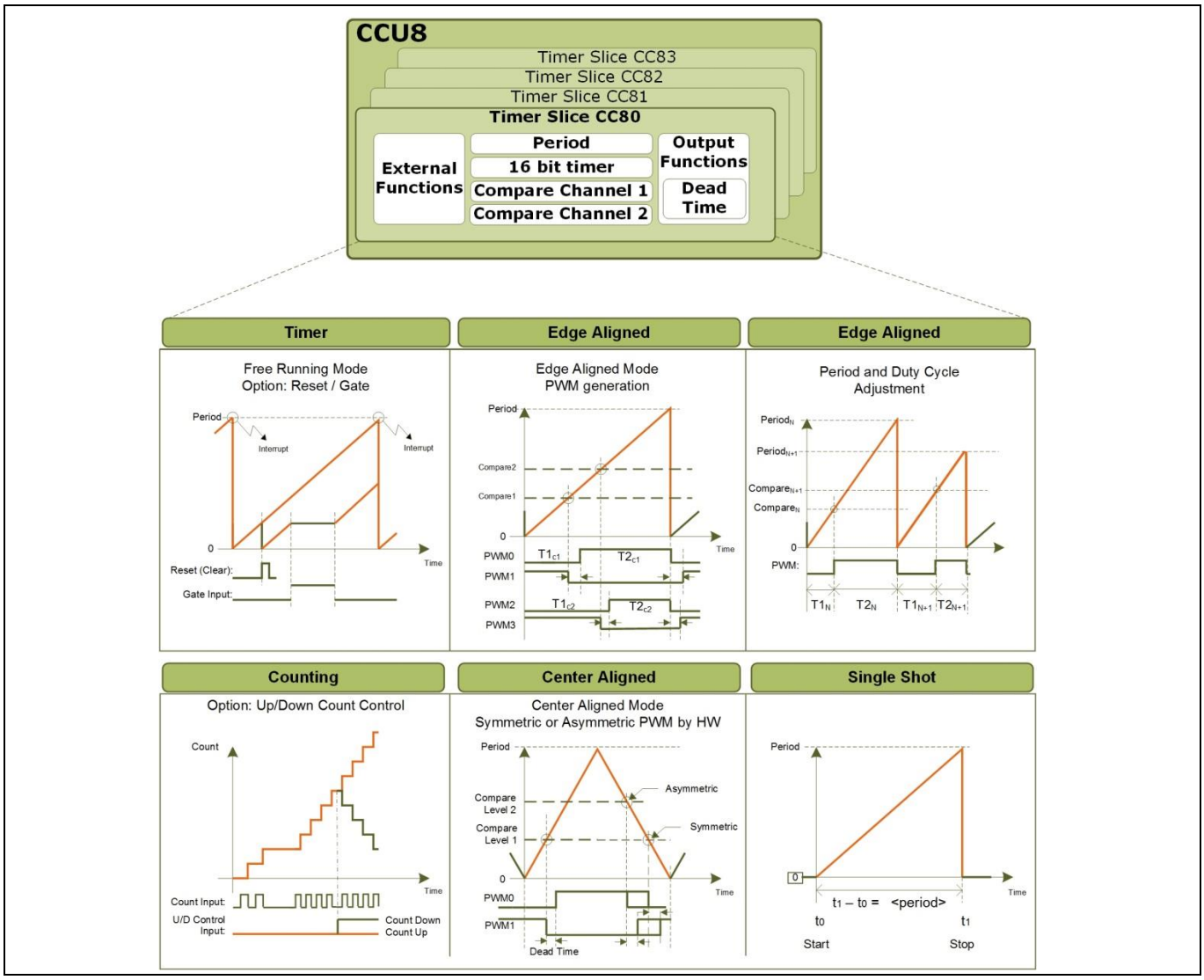

Figure 7 CCU8 flexible PWM generation scheme

3.1.4.2 HRPWM generation

The HRPWM generator (150 ps) is an essential module, for cutting-edge and optimized SMPS application development [8].

The XMC42xx devices offer high resolution channel (HRC) generation. The HRPWM is used together with CCU8 slices.

The enhanced PWM resolution is performed by means of an insertion that shortens or lengthens the original pulse width of the CCU8 slice output pulse in steps of 150 psec. It can offer a resolution of 10 bit up to 6 MHz PWM. A dynamic dead-time insertion feature is available in the HRPWM path.

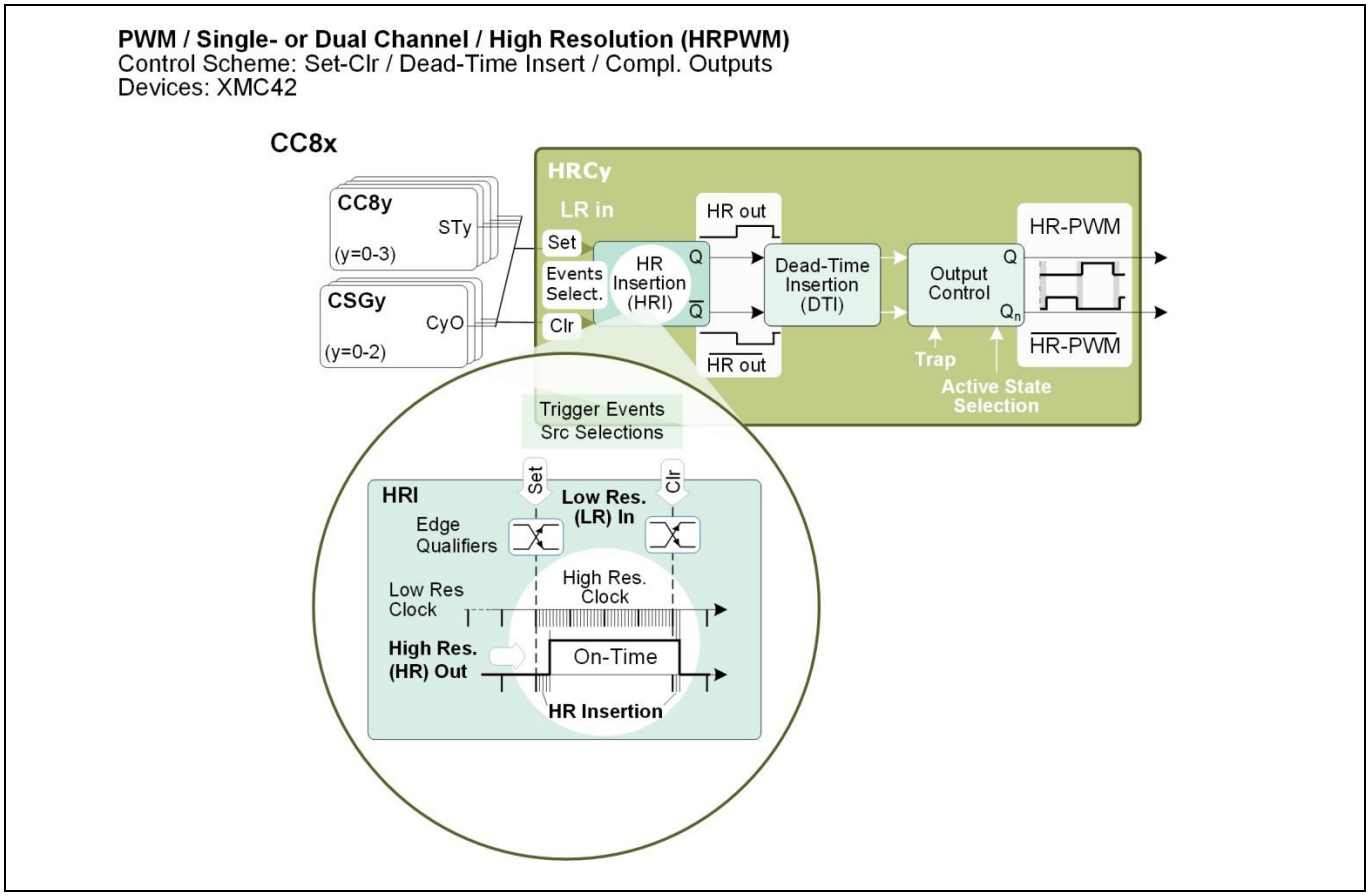

Figure 8 High-resolution channel

3.1.4.3 Voltage and current sensing-VADC

Input voltage, output voltage, and inductor current and all necessary signals to control a power converter can be monitored via versatile analog-to-digital converter (VADC) channels in XMC™ [8].

The functionalities of VADC that are useful for digital power control are as follows:

- Automatic scheduling of complex conversion sequences with priority for time-critical conversions
- Synchronous sampling of several analog signals
- Independent result registers, selectable for 8/10/12 bits, with 16 steps FIFO
- Sampling rates up to 2 MHz (up to 1 MHz for the XMC1000 family)
- FIR/IIR filter with selectable coefficients plus accumulation

The VADC module is intelligently connected to other peripherals, like PWM generation modules, in the MCU. This provides an accurate sampling point for real-time applications where the conversion of the analog signals must be done in a deterministic way.

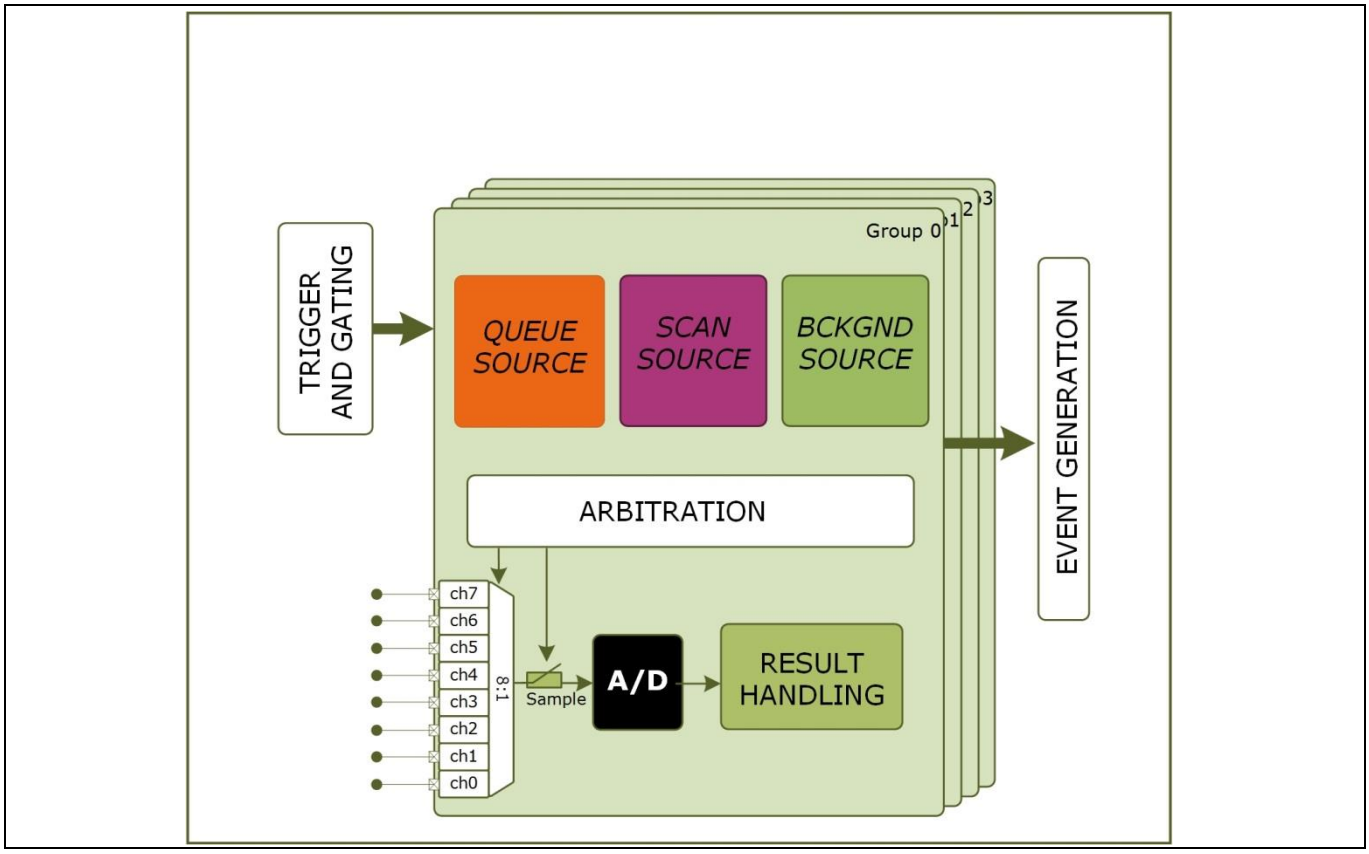

Figure 9 VADC schema

3.1.4.4 Comparator and slope generator (CSG) – XMC4200 MCU

With three high-speed comparators and hardware slope, it is possible to address several power-conversion topologies with reduced SW interaction. The CSG consists of essential interaction factors for several control techniques (see Figure 10); an analog high-speed comparator ~20 nsec that can be used to monitor:

- Coil current for current protection or peak current mode control (PCMC)
- Voltage outputs for protections
- Slope generator with high-speed DAC (~30 Msample/sec) that can be used to:
  - Reference control for the comparator
  - Insert a decrementing or incrementing ramp to the comparator for PCMC
- Filtering and blanking capabilities to avoid current commutation spikes to pass to the comparator

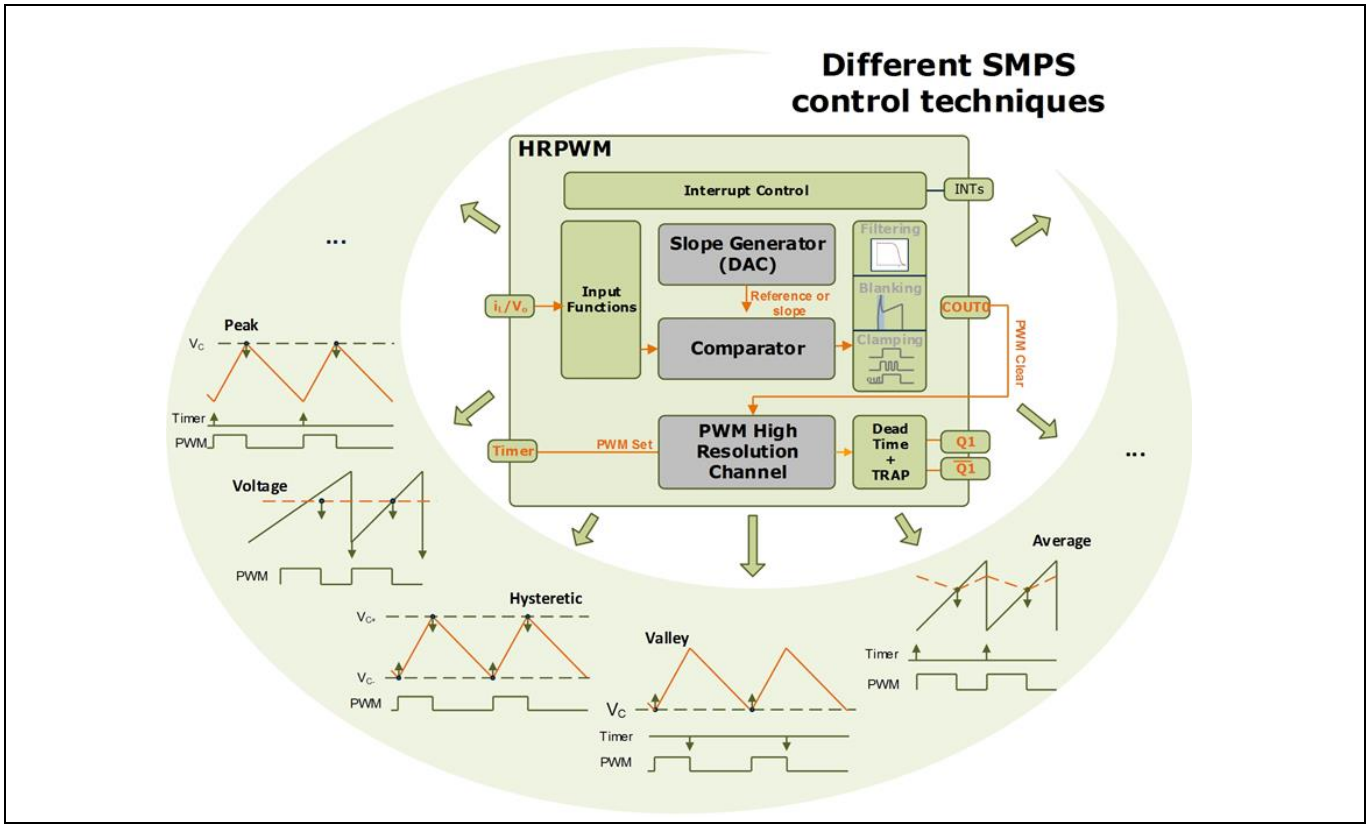

Figure 10 Using the CSG together with the HRC for implementing different SMPS control techniques

3.1.4.5 Event Request Unit (ERU)

The ERU module can be used to expand the point-to-point connections of the device: ports-to-peripherals, peripherals-to-peripherals, and ports-to-ports. It also offers configurable logic that allows the generation of triggers, pattern detection, and real-time signal monitoring [8].

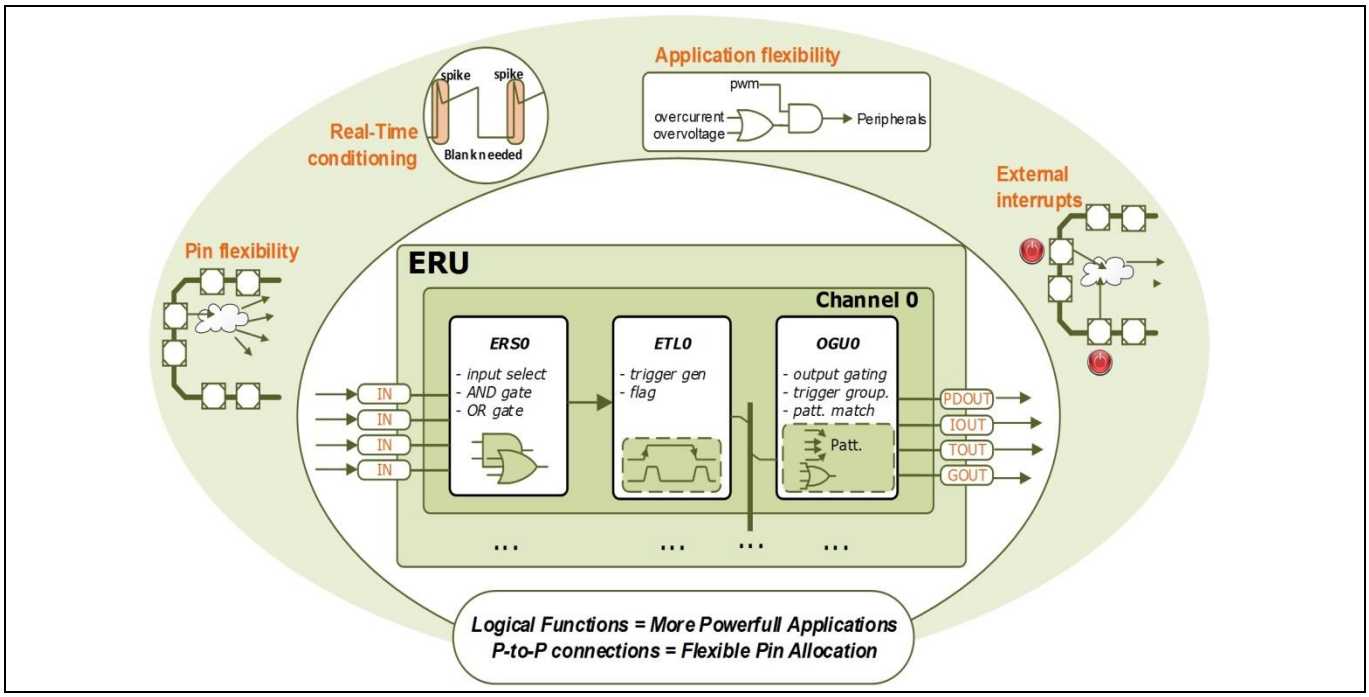

Figure 11 XMC™ peripheral interconnections through the ERU

3.1.5 Bias QR flyback controller ICE3RBR4765JZ

The ICE3RBR4765JZ belongs to the Infineon CoolSET™ range of off-line SMPS current mode controller ICs with integrated 650 V CoolMOS™ and start-up cell in a DIP-7 package. The outstanding performance includes BiCMOS technology, active burst mode, built-in frequency jitter, soft gate driving, propagation delay compensation, built-in soft-start time, built-in blanking time and extendable blanking time for over-load protection, and an external auto-restart enable feature.

Summary of features

- 650 V avalanche rugged CoolMOS™ with built-in start-up cell
- Active burst mode for lowest standby power
- Fast load-jump response in active burst mode
- 65 kHz internally fixed switching frequency
- Auto-restart protection mode for over-load, open-loop, V_{CC} undervoltage, overtemperature, and overvoltage
- Built-in soft-start
- Built-in blanking window with extendable blanking time for short-duration high current
- External auto-restart enable pin
- Max. duty cycle 75%
- Overall tolerance of current limiting < ±5%
- Internal PWM leading edge blanking
- BiCMOS technology providing wide VCC range
- Built-in frequency jitter and soft driving for low EMI

Benefits

- Lowest standby power requirements < 50 mW
- Low operating temperature down to -40°C
- Auto-restart protection for over-load, overtemperature, overvoltage
- Wide VCC range
- Soft driving for low EMI

Target applications

- Adapter, charger, Blu-ray player, DVD player, set-top box, digital photo frame, auxiliary power supply for server, PC, printer, TV, home theater/audio system, white goods, etc.

3.1.5.1 Upcoming new BIAS version with ICE5QSAG

The BIAS converter efficiency predominantly affects the light-load efficiency of the whole ZVS PSFB board. In order to further improve it, Infineon Technologies is going to introduce a new version of the auxiliary converter using the latest CoolSET™ ICE5QSAG controller and a 800 V CoolMOS™ P7 MOSFET IPU80R4K5P7. This converter will be used as a platform for the BIAS in all the new developed high-power demo boards and will be introduced in the next revision of the present 800 W ZVS PSFB. Updated documentation will be provided at the time of the new release.

3.2 Board schematics

3.2.1 Main converter

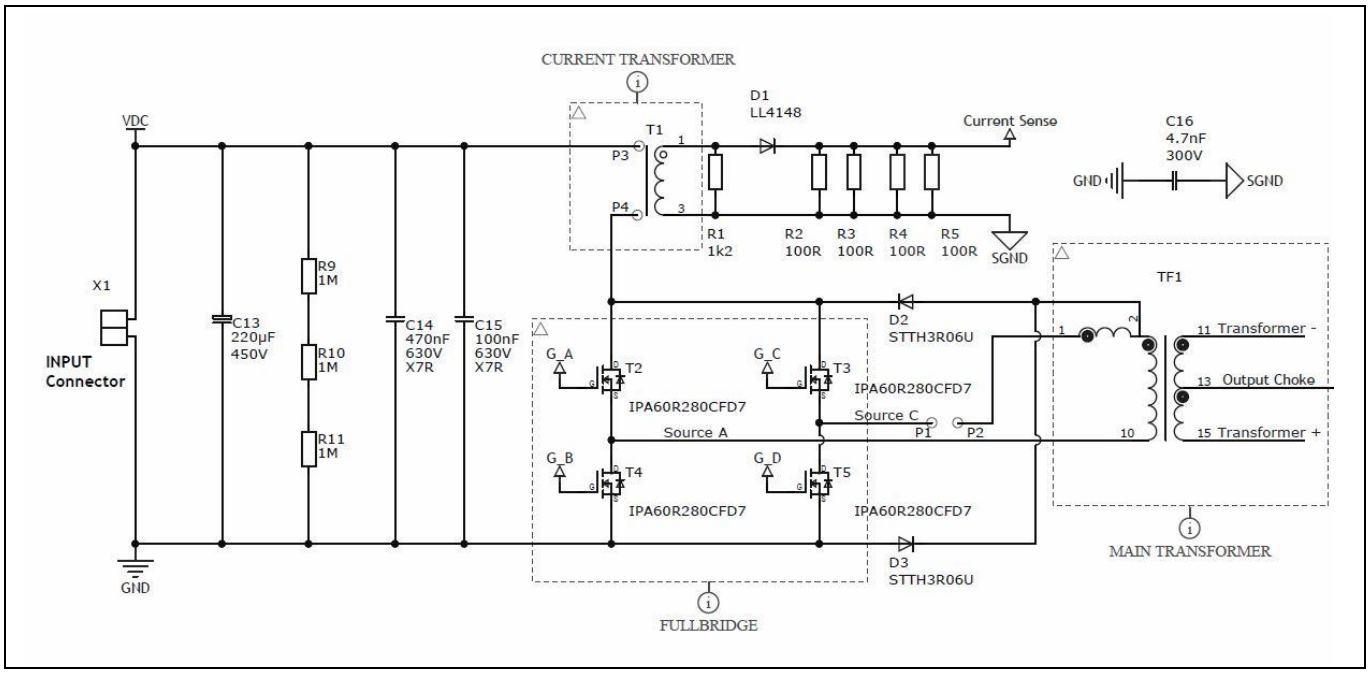

Figure 12 Primary side

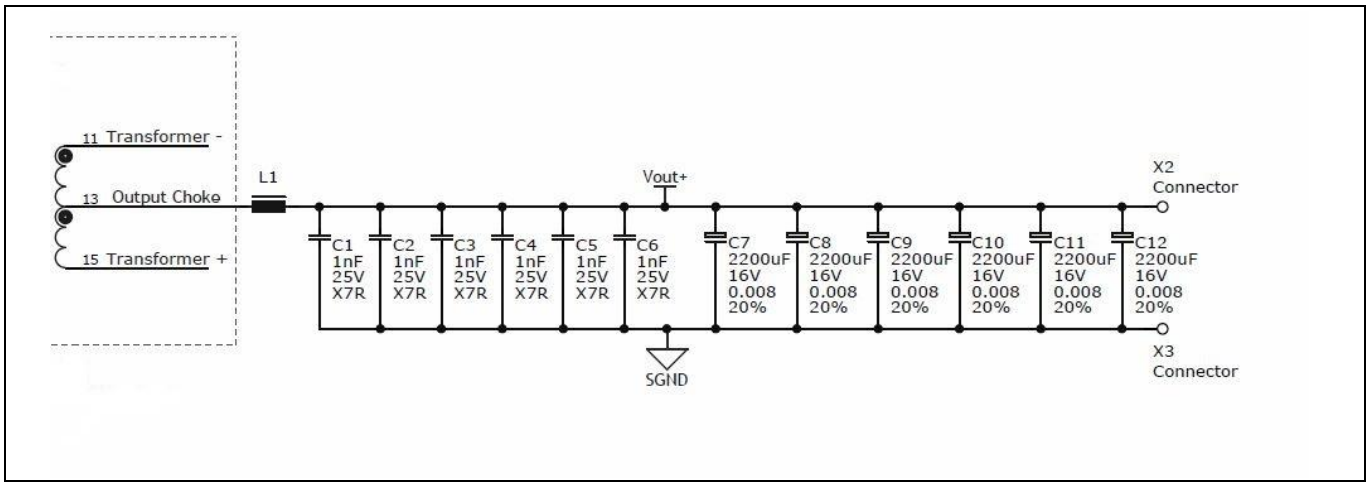

Figure 13 Secondary side

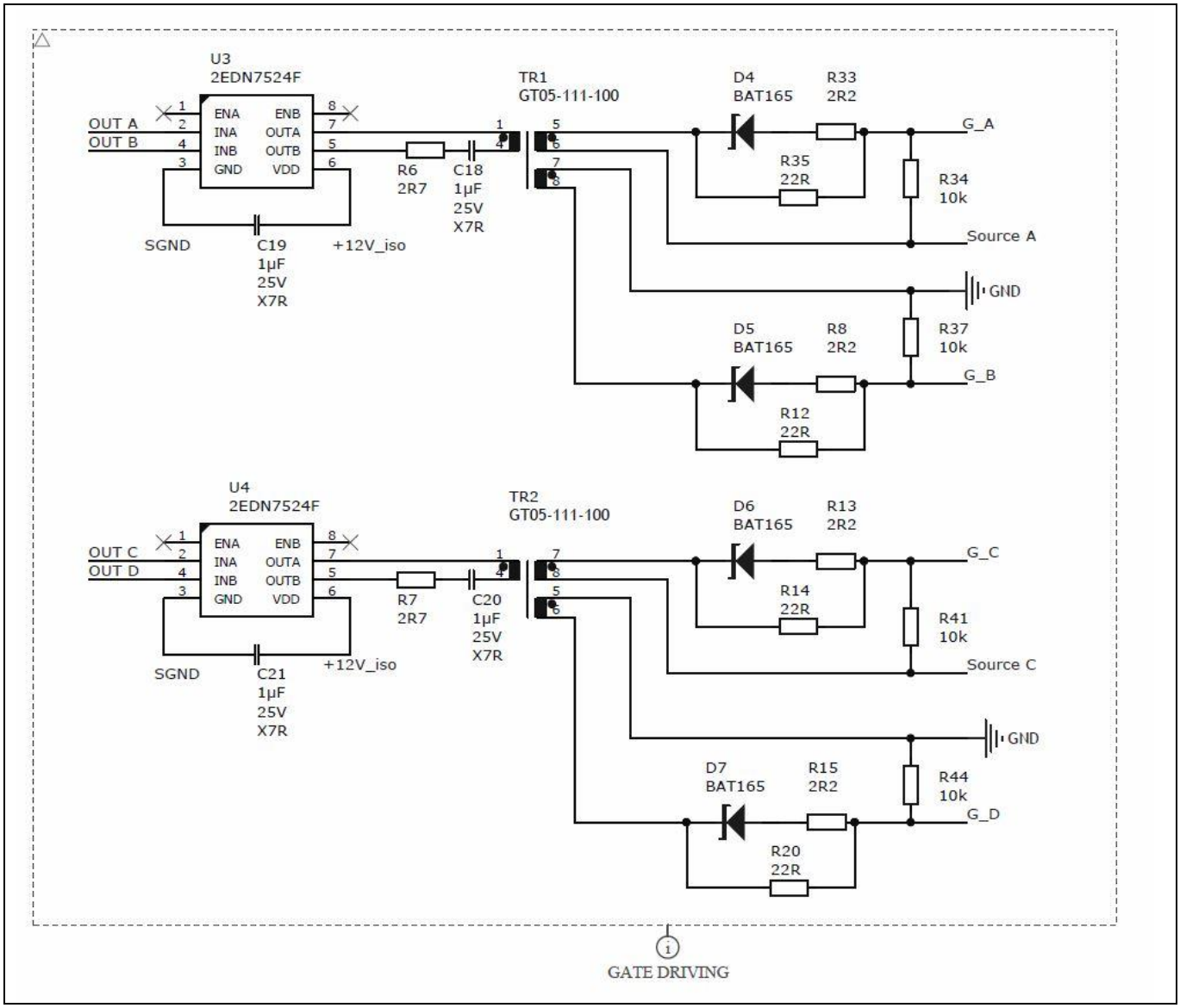

Figure 14 Gate driver

3.2.2 Synchronous rectification daughter card

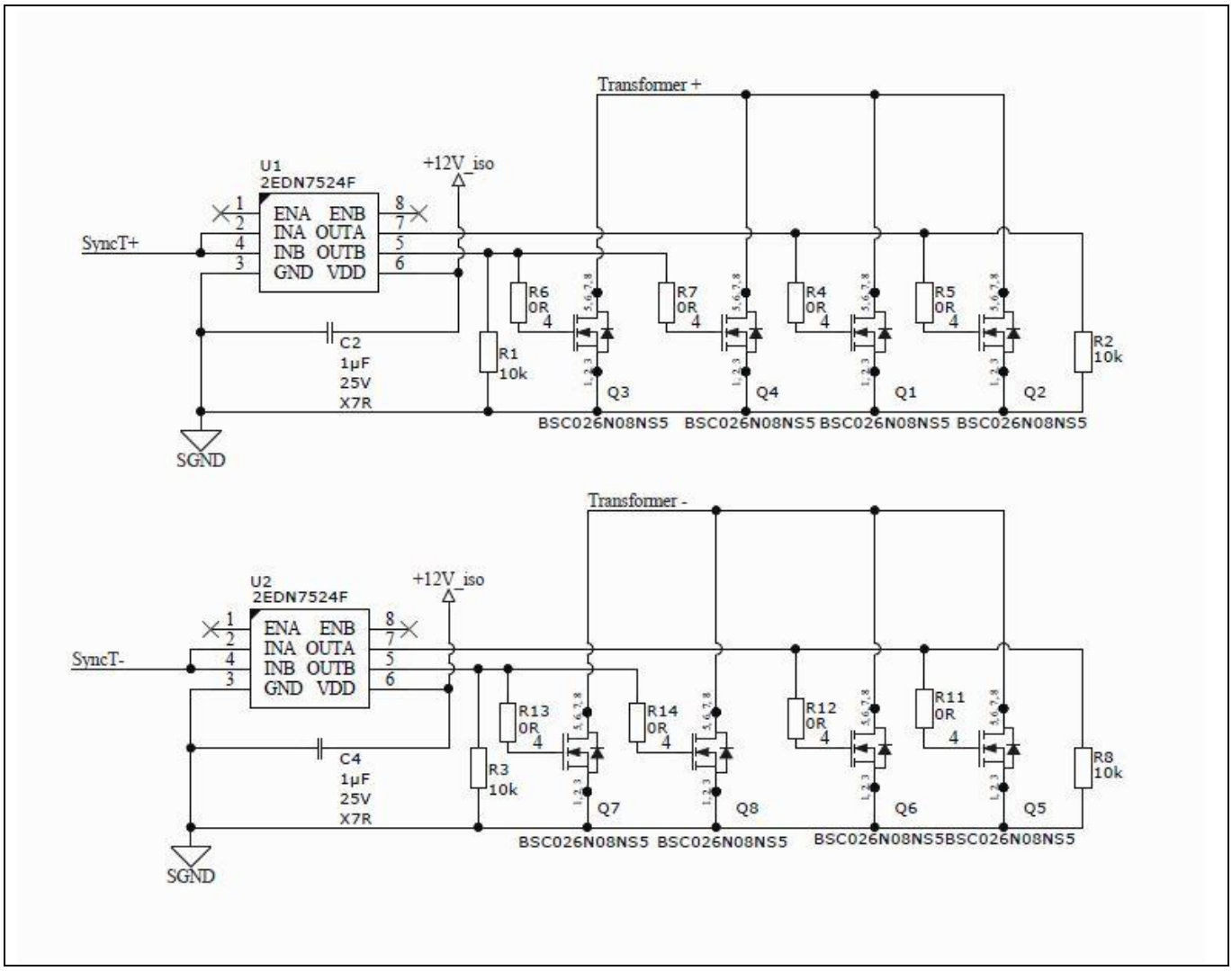

Figure 15 Synchronous rectification

3.2.3 Control board

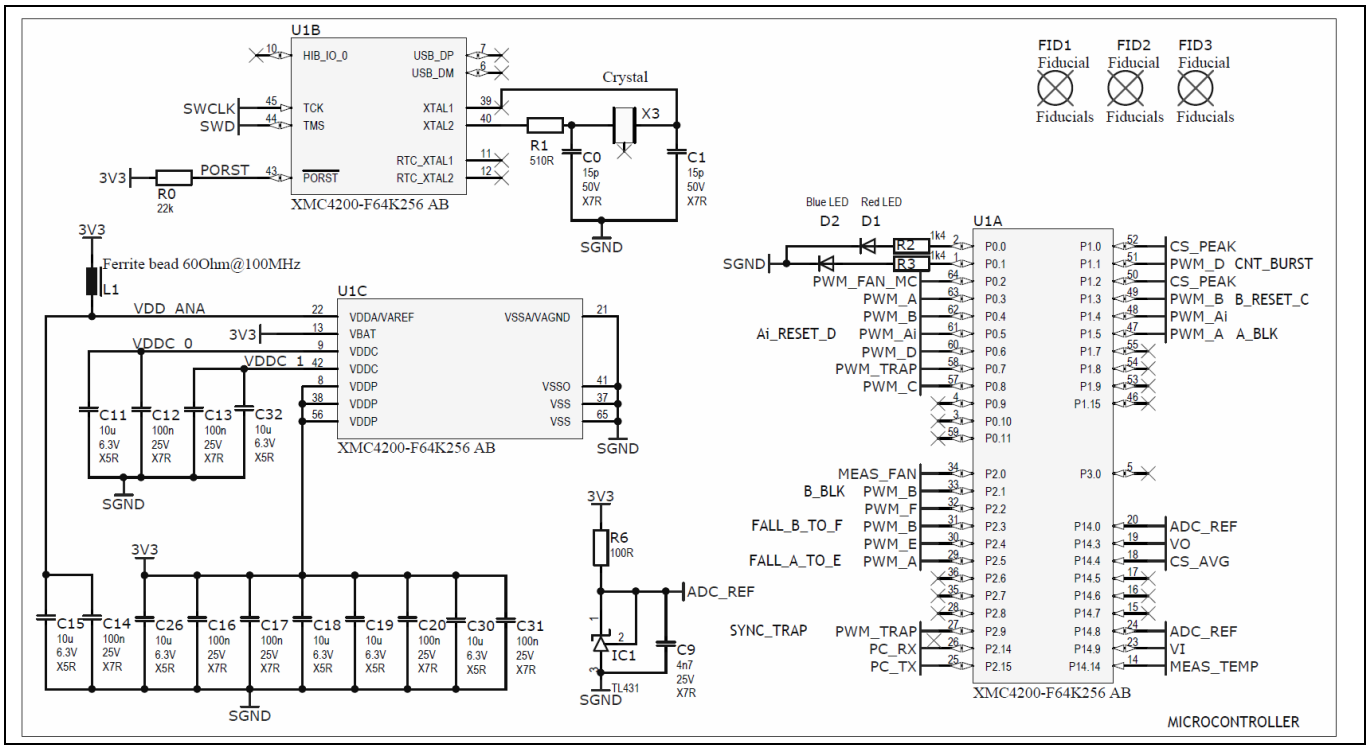

Figure 16 Microcontroller pin-out

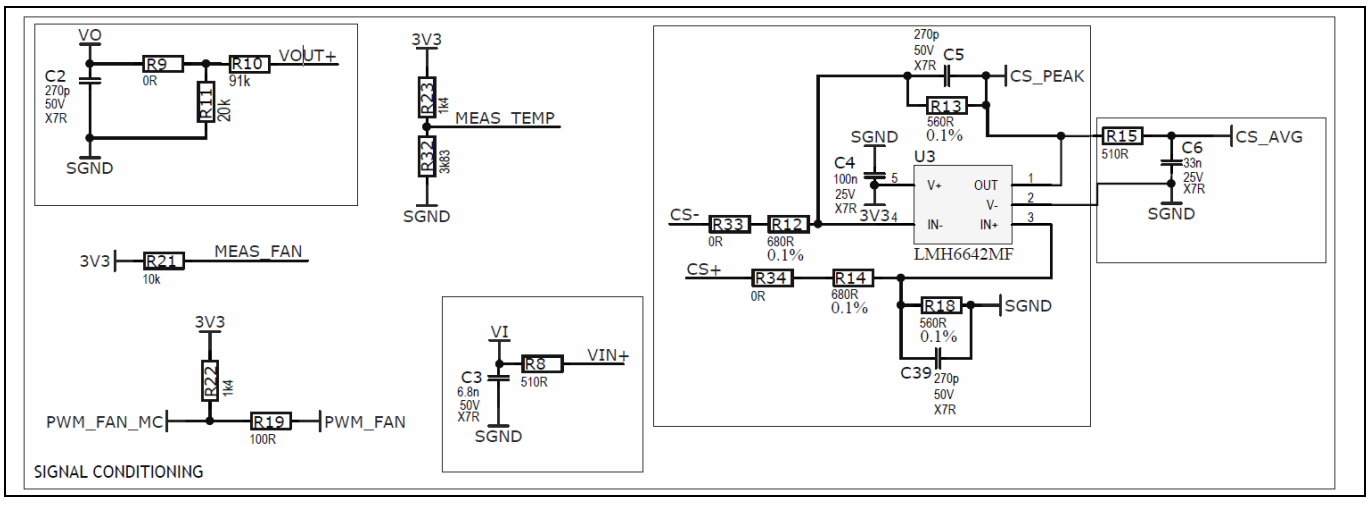

Figure 17 Signal conditioning of analog measurements (amplification and filtering)

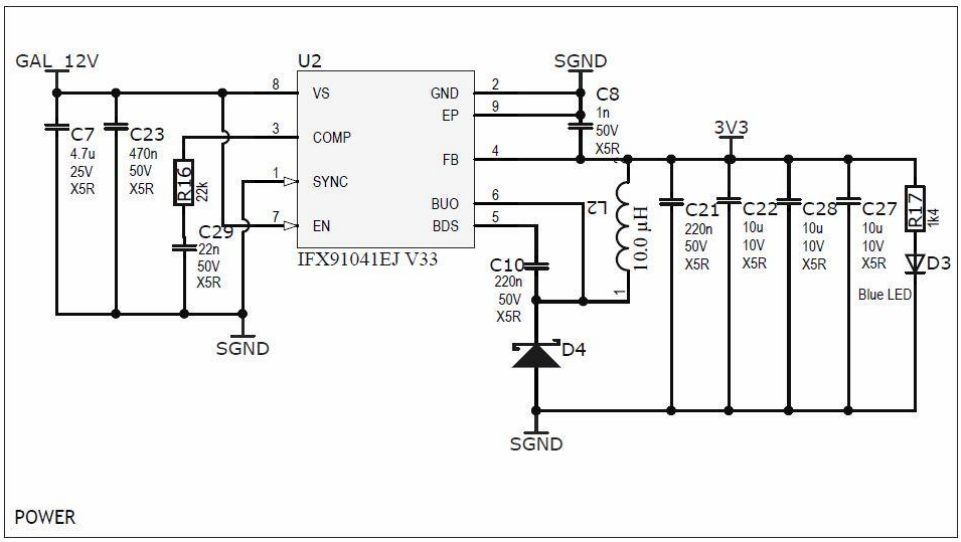

Figure 18 Supply of microcontroller and signal-conditioning circuitry

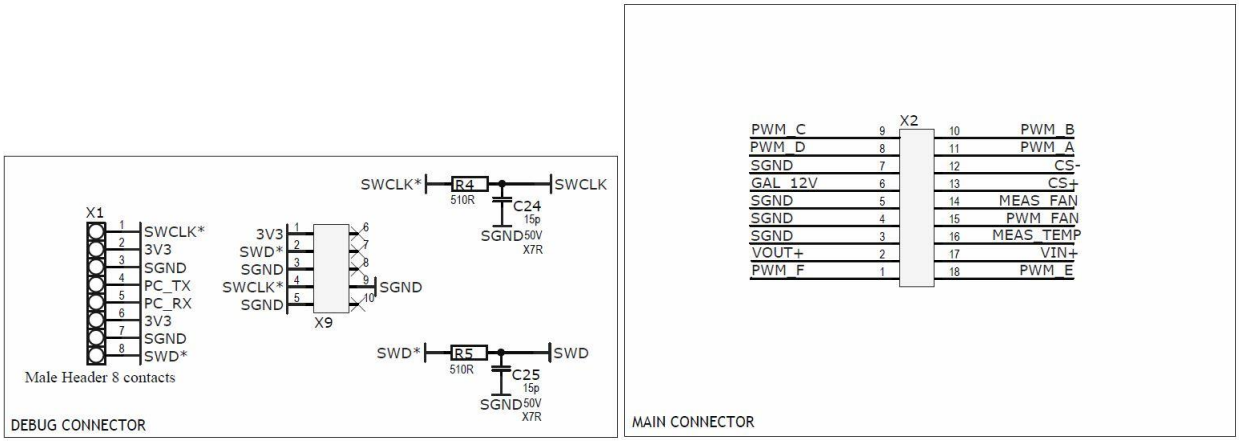

Figure 19 Control card connectors

3.2.4 Bias board (auxiliary converter)

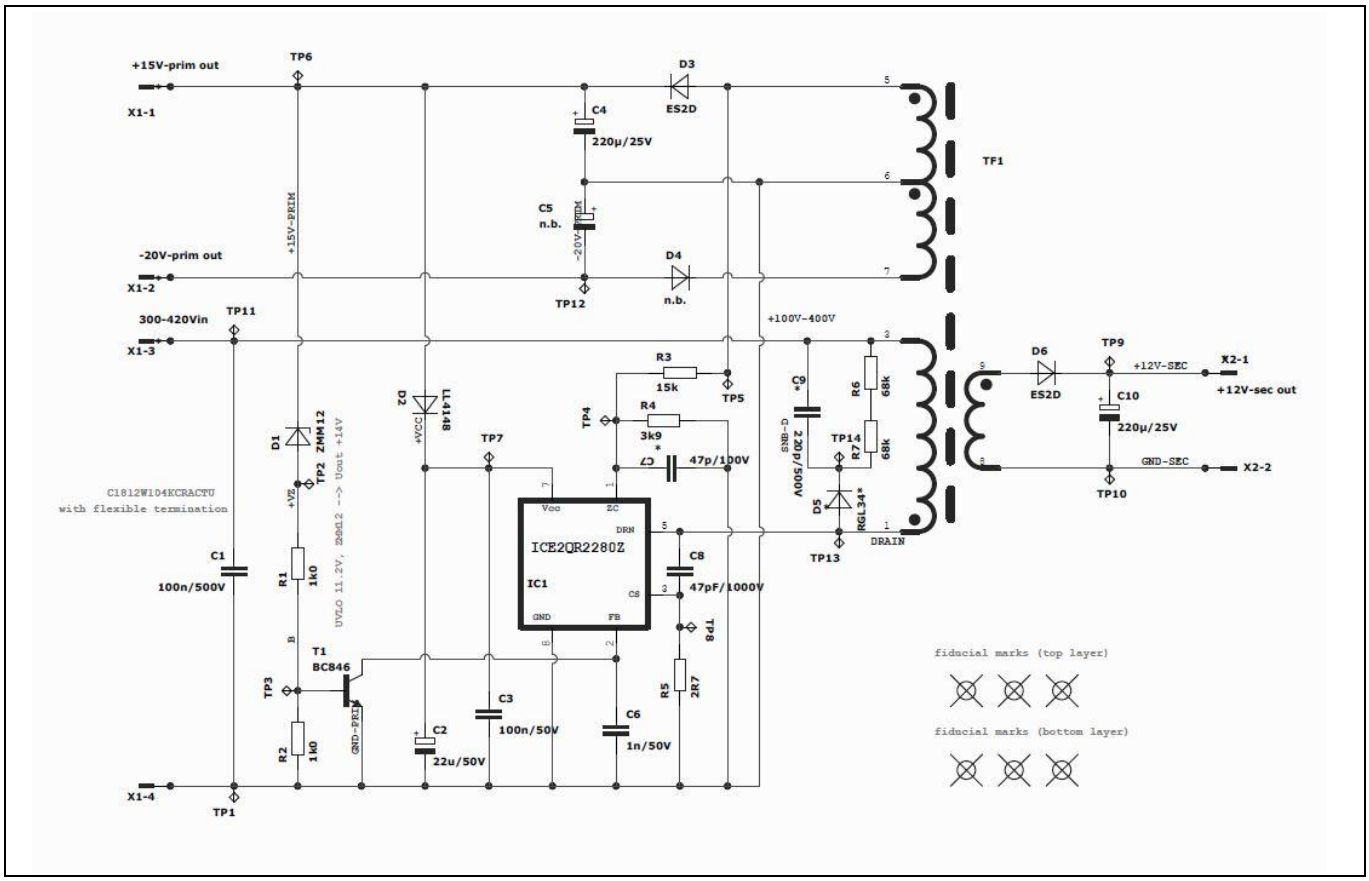

Figure 20 Bias schematic

3.3 Magnetic components

3.3.1 Main transformer

Electrical specifications at 25°C ±5°C:

Measurement	Terminal	Specification
Magnetizing inductance	2–10	2.1 mH +/- 20% @ 100 kHz, 0.5 Vrms
Leakage inductance	2–10 (11–15 shorted)	4.3 µH nominal @ 100 kHz, 0.5 Vrms
Inductor inductance	1–2	21 µH +/- 15% @ 100 kHz, 0.5 Vrms
DCR	1–10 11–15	280 mΩ max. 0.6 mΩ max.
TR	2–10:11–13 2–10:13–15	22 22
Hi-pot Hi-pot Hi-pot	Pri. to sec. Pri. to core Sec. to core	4.0 kV AC, 6 mm creepage 2.5 kV AC 0.5 kV DC

Mechanical and appearance

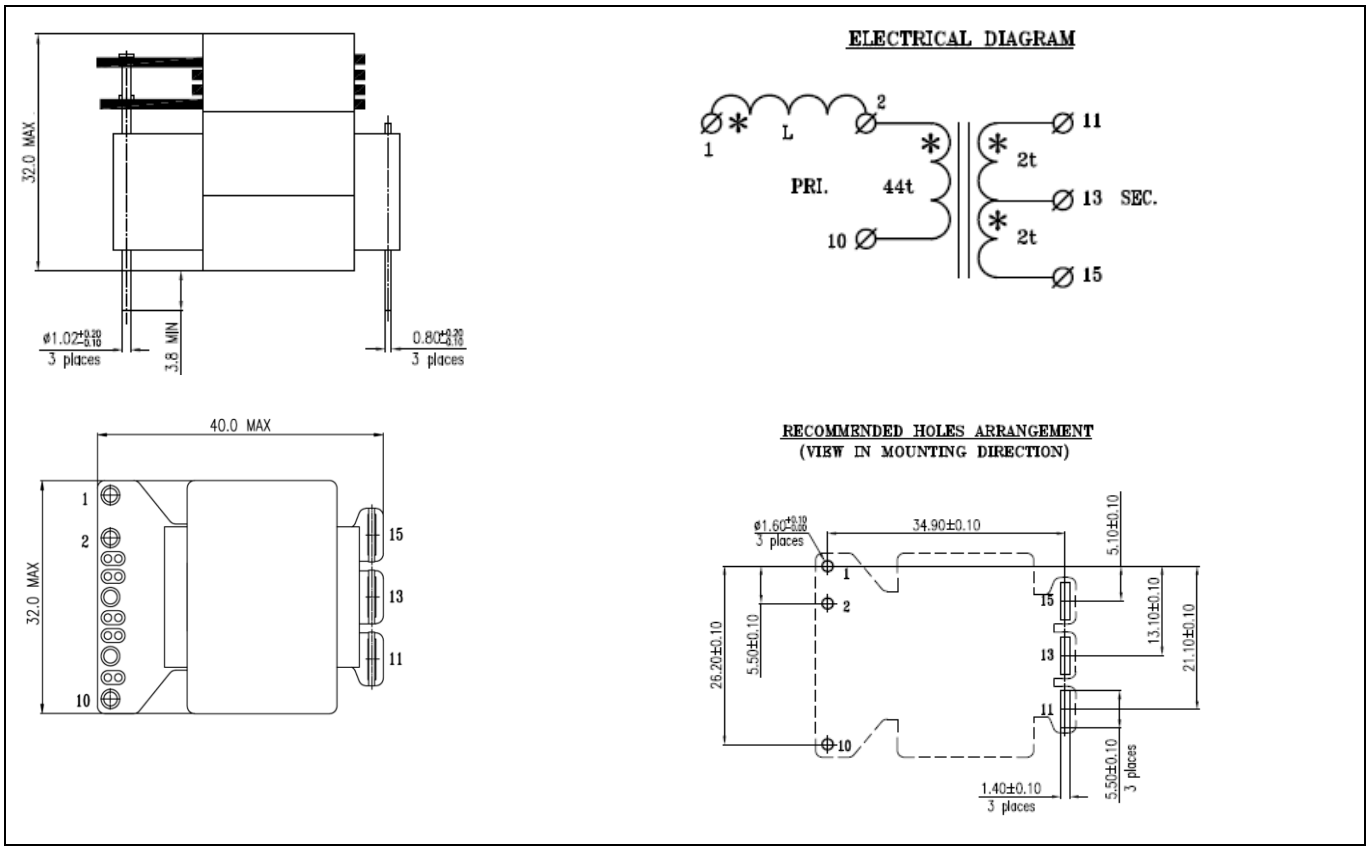

Figure 21 Mechanical and appearance: all dimensions are in mm

Module operational temperature range: -40˚C up to 130˚C, including module self-temperature rise.

Losses at full power (800 W): 11 W nominal magnetic module losses.

Losses breakdown: 3 W core losses, 8 W copper losses.

9.5 W losses on the transformer, 1.5 W on the leakage inductor.

The transformer has been developed by Infineon in cooperation with the company Payton Planar Magnetics Ltd – Israel

3.3.2 Output choke

Figure 22 Output choke specification sheet

The inductor is produced by Infineon's trusted partners in the development and manufacture of magnetic components:

- ICE Transformers s.r.l. – Loreto Aprutino (Pescara), ITALY
- Kaschke Components GmbH – Göttingen, GERMANY

3.3.3 Gate drive transformer

Part number	Turns ratio Drive: Gate	Drive ind. (µH, min.)	DCR (mΩ, max.)	Lkg ind. (nH, max.)	E-T prod (V-µs)	Hi-pot Drive: Gate	Hi-pot Gate: Gate
GT05-111-100	1:1:1	2000	1430:1300	470	100	3750 V AC	1.500 V DC

The gate drive transformer is a standard P/N produced by the company ICE Components, Inc.

3.3.4 Auxiliary transformer

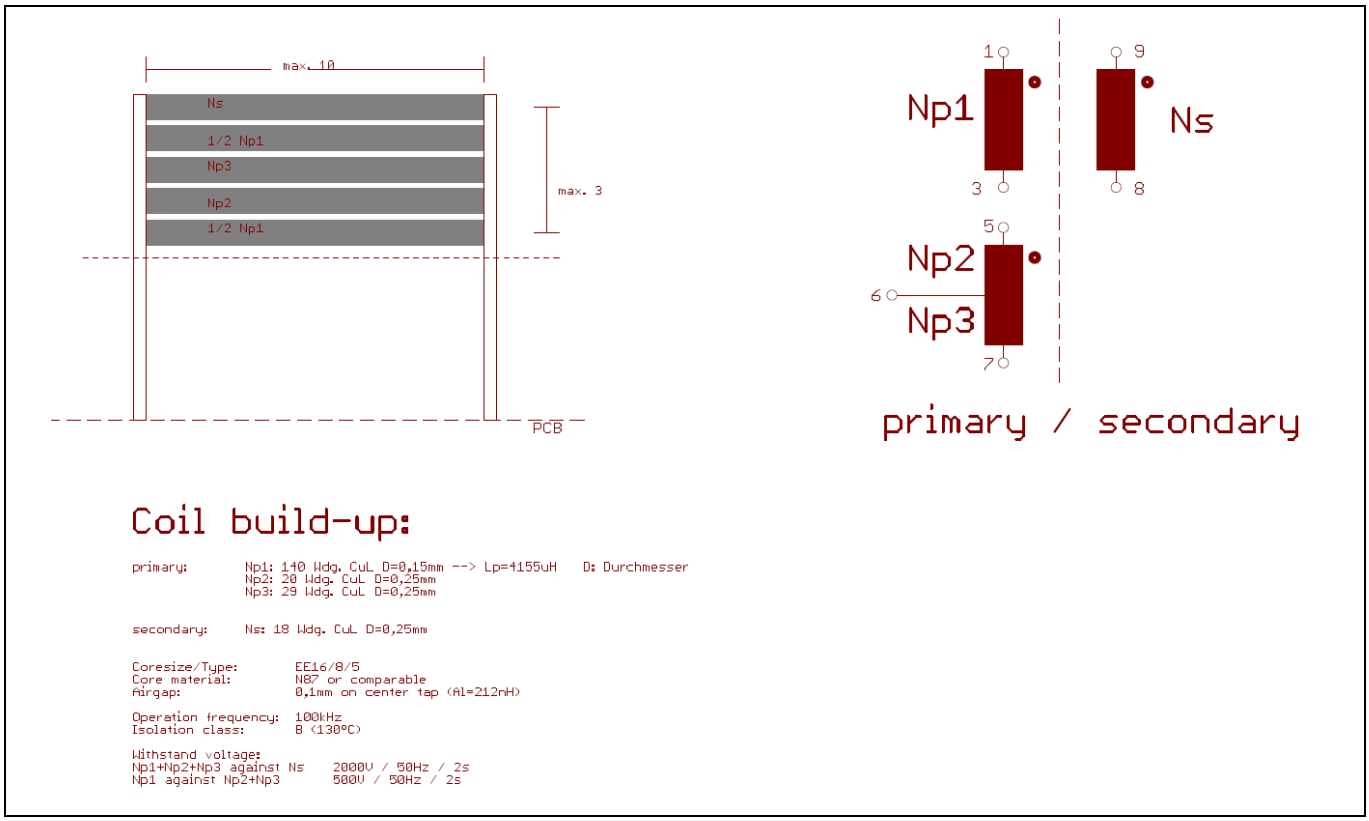

Figure 23 Flyback transformer

The transformer is produced by Infineon's trusted partners in the development and manufacture of magnetic components:

- ICE Transformers s.r.l. – Loreto Aprutino (Pescara), ITALY
- Kaschke Components GmbH – Göttingen, GERMANY

4 Digital control of PSFB

The control of the PSFB converter has been implemented using XMC4200, which is part of the XMC™ microcontroller family from Infineon Technologies. This family is based on an ARM® Cortex®-M4 core, and the main characteristics are summarized in 3.1.4. The following chapter will introduce the main features of the implemented digital control as well as the resources necessary for proper implementation.

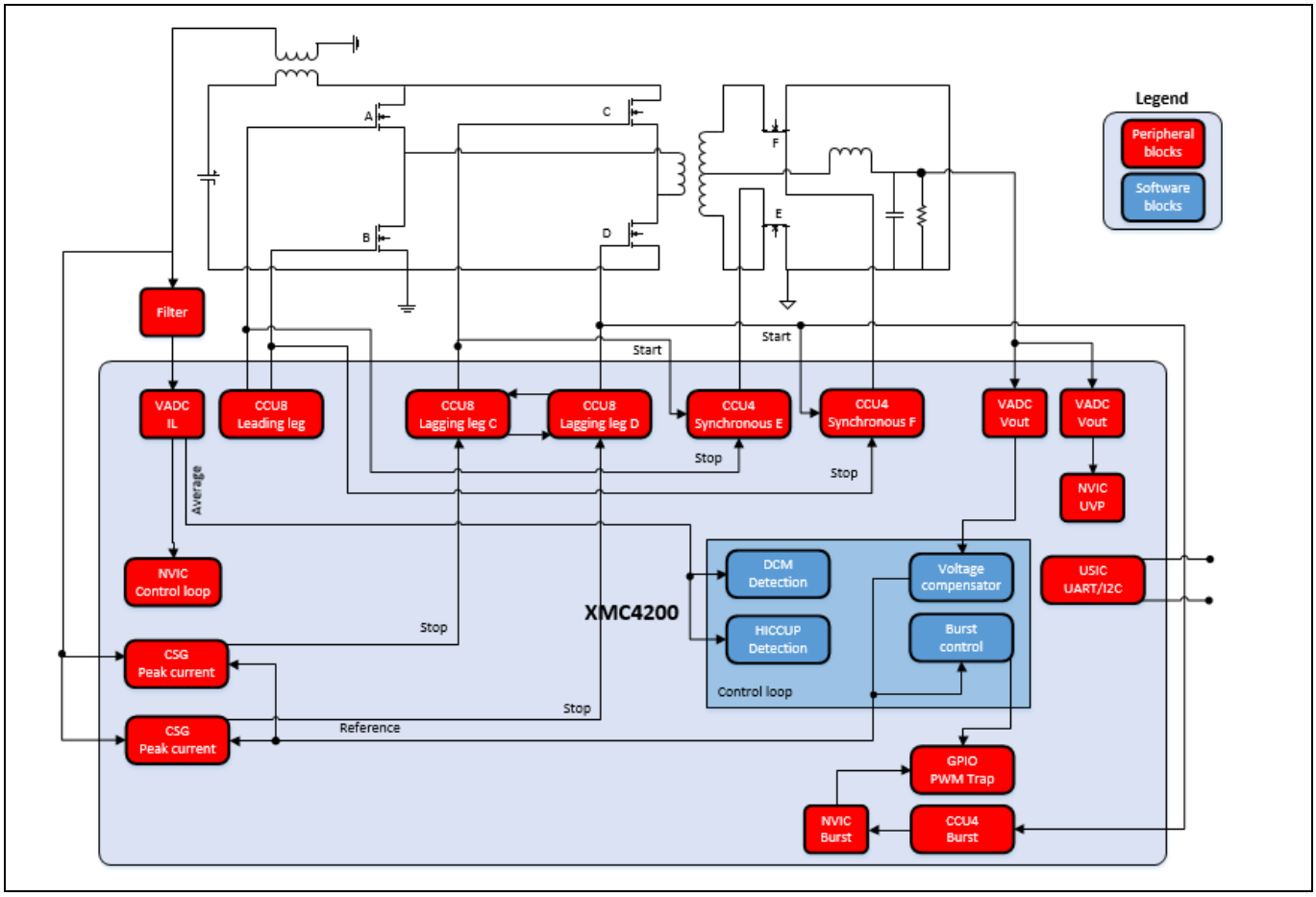

Figure 24 Simplified peak current mode control implementation blocks

The design, coding, documentation, testing and debugging process of digital control for the PSFB implementation with XMC4200 was supported by DAVE™ 4.1.2 and XMC™ low-level driver library (XMC™ Lib LLD).

DAVE™ 4.1.2 is a professional free-of-charge development platform for code generation provided by Infineon. Please note that XMC™ Lib and DAVE™ generated code can be used with other third-party tool chains.

There are two variants of control scheme differentiated by the PWM applied by the controller and, because of it, they have different dynamic behavior, as well as some advantages and disadvantages, which are addressed in the next sections.

- In voltage mode control (VMC) the phase shift between the driving signals of the bridge is the control variable (Figure 25). The phase shift or power transfer time is proportional to the output voltage error when compared to the internal reference
- In peak current mode control (PCMC) the peak current during a power transfer cycle is the control variable (Figure 24). The primary peak current of the transformer is proportional to the output voltage error when compared to the internal reference

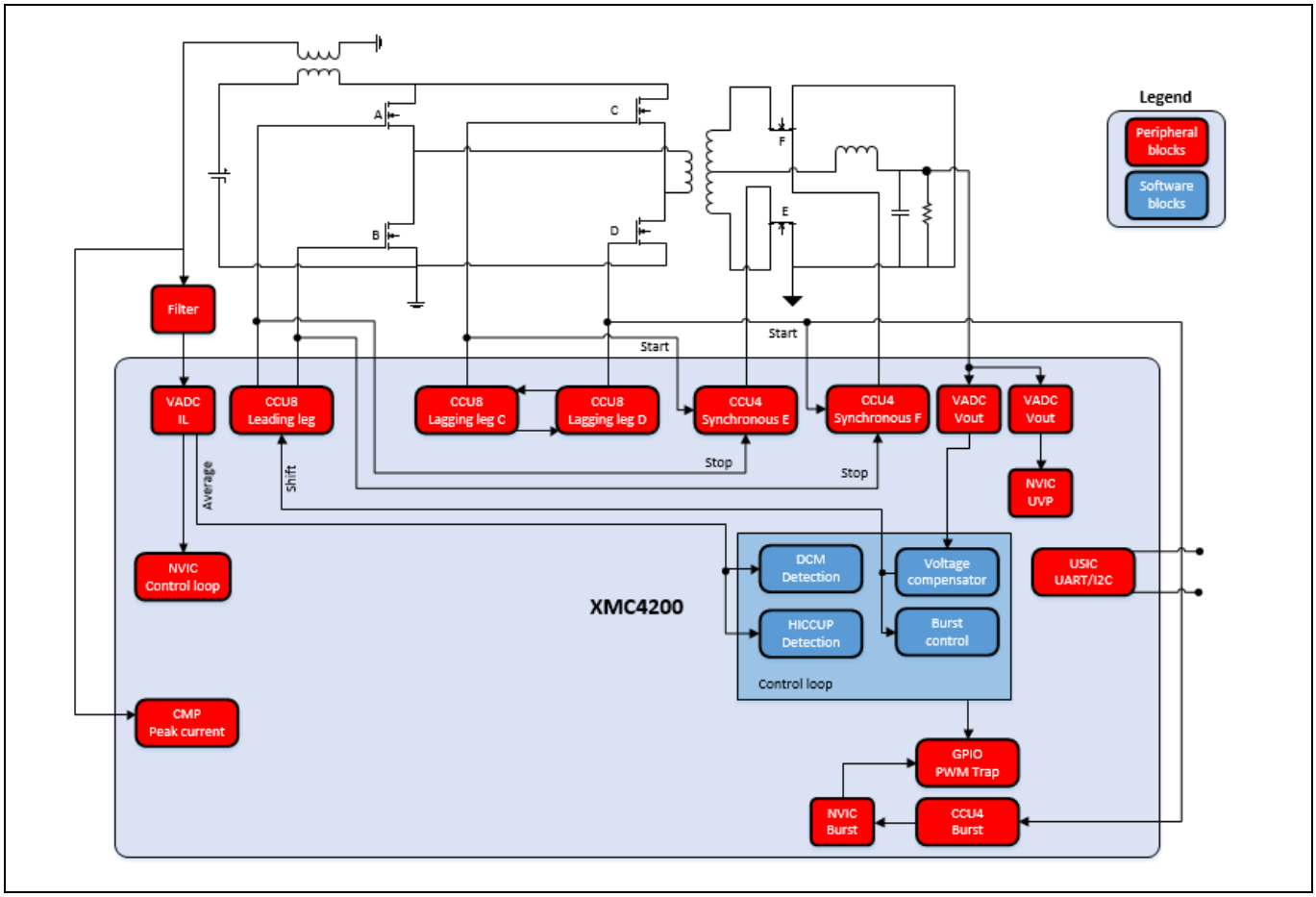

Figure 25 Simplified voltage mode control implementation blocks

Implementation of the control with XMC4200 allows the usage of both modulation schemes without external hardware adaptations.

PCMC is recommended for this application, as the advantages over VMC enable a design with better performance in terms of efficiency and reliability.

The control routines are executed at the switching frequency (100 kHz), together with the highest-priority software protections (some of them with redundant asynchronous mechanisms). The remaining CPU time is used by the background tasks (see Figure 26).

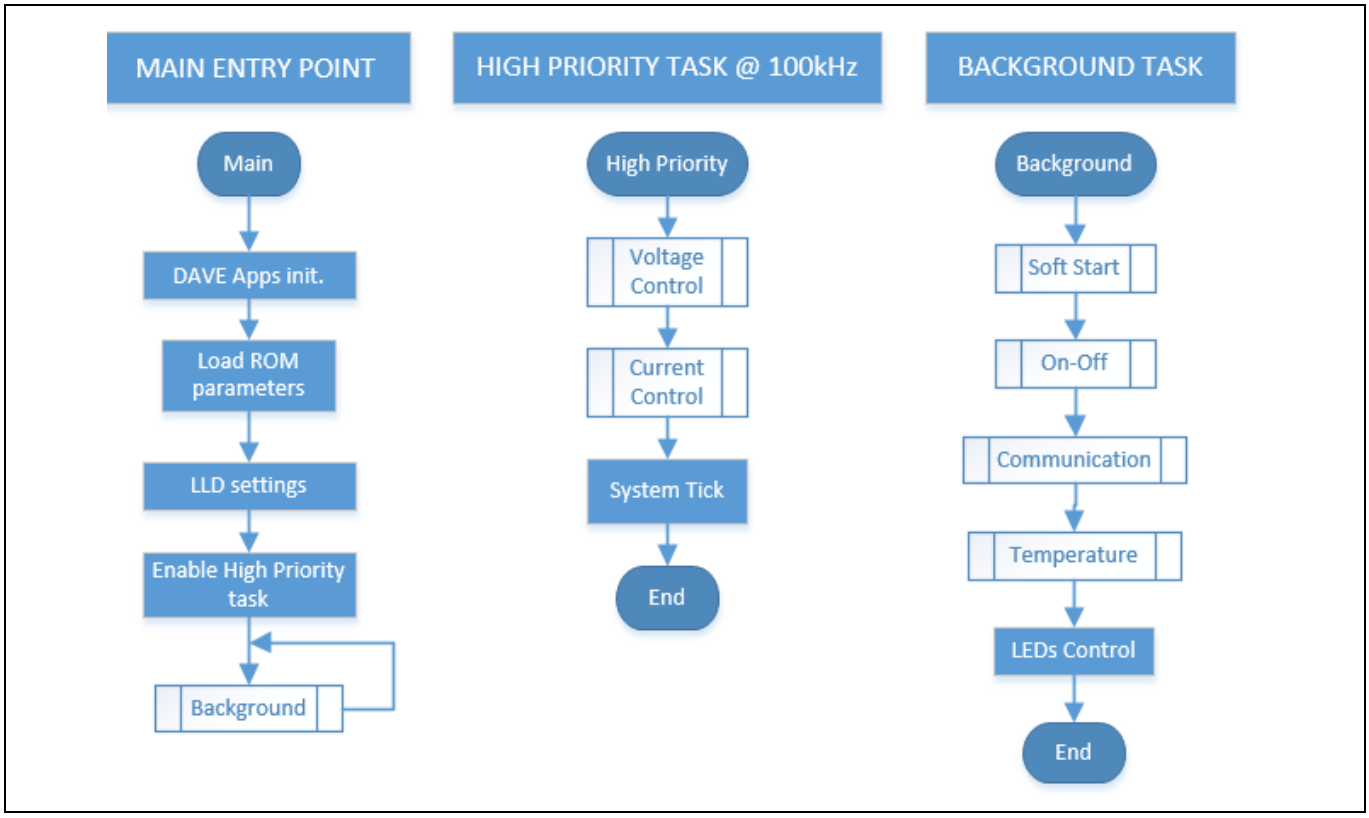

Figure 26 PSFB digital control with XMC42 main structure

Note: Hardware protections, enabled by the XMC42 peripherals, do not appear in the software flow diagrams. These redundant mechanisms provide faster reaction times to asynchronous events.

4.1 Voltage mode control (VMC)

In this mode, leading leg driving pulses (A and B in Figure 27) have a fixed frequency and fixed 50% duty, excluding required dead times.

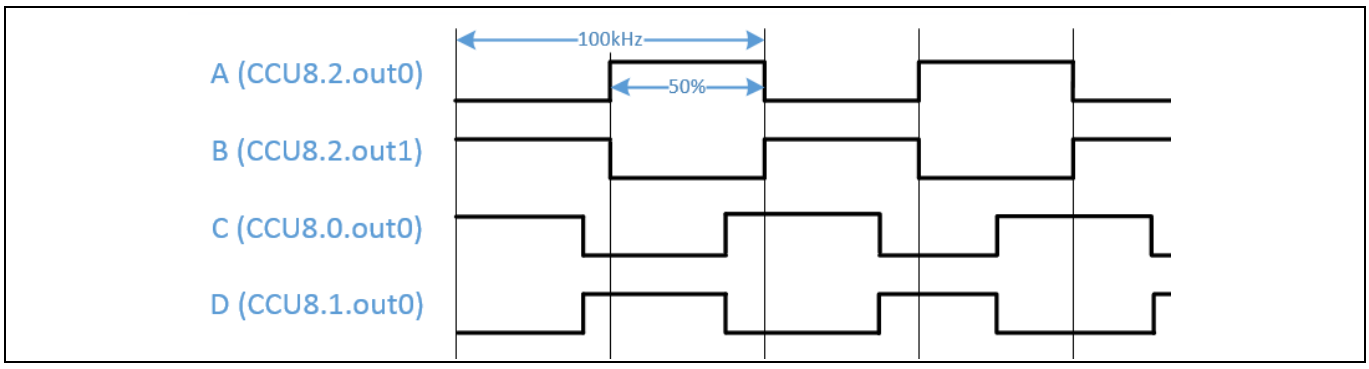

Figure 27 Fixed frequency and fixed 50% duty of the leading leg PWM

The lagging leg high side driving pulses (C in Figure 27) have fixed frequency and fixed 50% duty cycle like the leading leg. However, the low side pulse (D in Figure 27) will vary its period to adjust the phase shift between the legs.

In steady-state the pulses of D have also fixed frequency and fixed 50% duty. Only during a phase shift change, due to a transient, one of the pulses will have a different duration (Figure 28).

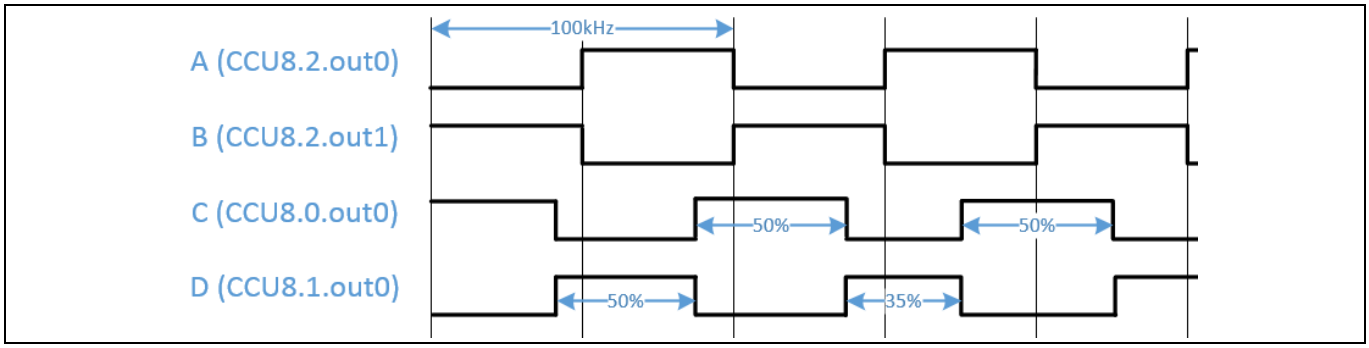

Figure 28 Duty variation of the D pulse modifies the phase shift between legs

VMC takes advantage of the HRPWM peripheral in XMC4200 for adjusting the phase shift between legs in steps down to 150 ps. This gives around 3 k resolution steps of regulation for the PSFB 800 W design (100 kHz switching frequency).

Note: Phase shift applied at 100% of load is approximately 3.66 µs and it becomes 3.30 µs at no load. The nominal regulation window is 0.36 µs.

Some advantages of VMC are:

- Simple modulation scheme and control implementation
- Easy-to-implement alternative synchronous modulation schemes
- HRPWM steps avoid possible limit cycles

Some disadvantages of VMC that could arise, depending on the application and design:

- Unbalance of the transformer magnetizing current could lead to saturation. Careful design of the magnetics or a capacitor in series with the primary side of the transformer avoids the problem
- The gain of the converter depends on the input voltage. Feedforward of the input voltage removes the dependency, which is easy to implement in a digital controller if the input voltage is measured

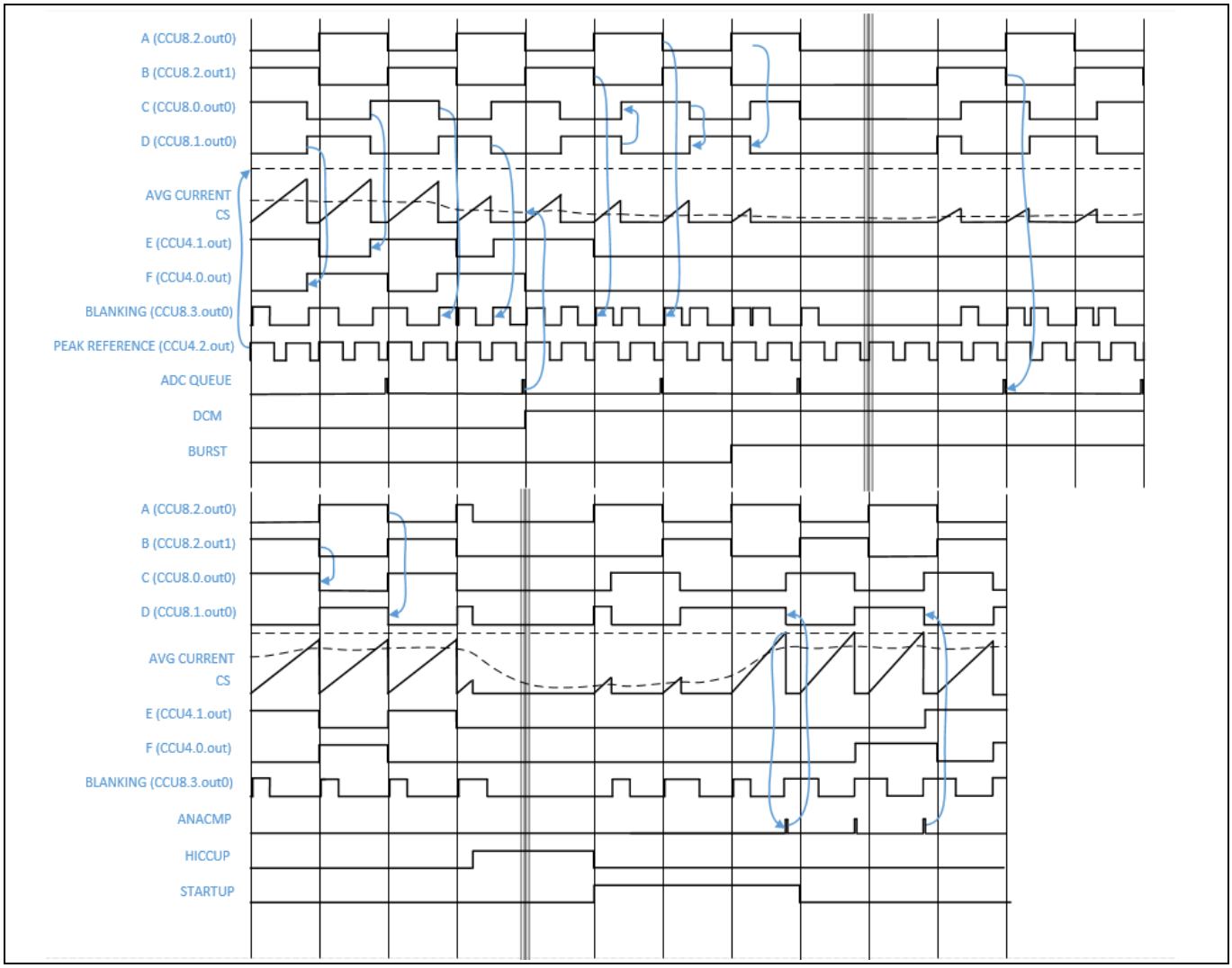

Figure 29 VMC implementation in XMC42

Figure 29 shows in more detail some signals and states of the controller in VMC. A blue arrow indicates a link between events. Compare with PCMC in Figure 35.

4.1.1 VMC small-signal model

Small-signal analysis of PSFB with VMC modulation can be found in the literature, or derived. The model here has been extracted from [8].

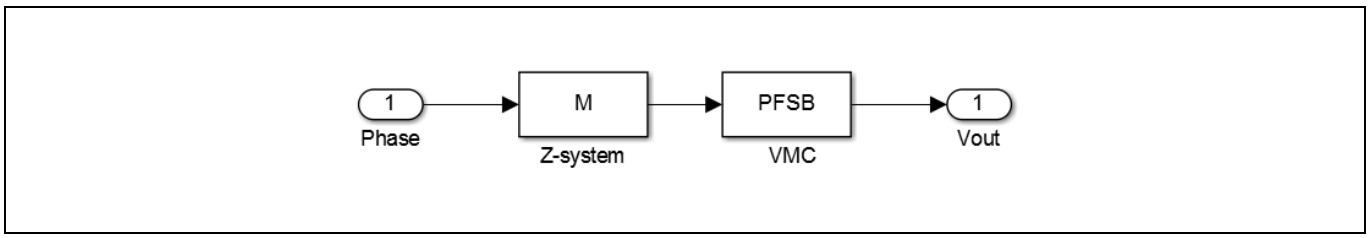

Figure 30 Modulation and converter open-loop path

Equivalent resistance of transformer:

$$Req = (2 * Llkg * fs) * n^2 \quad (1)$$

Where n is the turns ratio of the transformer, L_{lkg} is the leakage of the transformer plus the external resonant inductance, and f_s is the switching frequency.

$$R_1 = Req + \frac{Rc * Ro}{Rc + Ro} \quad (2)$$

Where R_c is the series resistance of the output capacitors and R_o is the resistive load of the converter.

$$R_2 = \mathrm{Ro} + \mathrm{Rc} \quad (3)$$

$$P_s = s^2 + \left(\left(1 + \frac{R_1}{\mathrm{Ro}}\right) * \frac{1}{\mathrm{Lo} * \mathrm{Co}}\right) + s * \left(\frac{R_1}{\mathrm{Lo}} + \frac{1}{\mathrm{Co} * \mathrm{Ro}}\right) \quad (4)$$

The transfer function of the transformer, primary duty to output voltage is G_{vd}.

$$G_{vd} = n * Ro * V_{in} * \frac{1 + Rc * Co * s}{Lo * Co * R_2 * P_s} \quad (5)$$

The gain of the PWM scheme is M (Figure 30).

$$M = \frac{uC_{clk}}{2 * f_s} \quad (6)$$

The gain and phase of the converter are influenced by the load and the input voltage, and the compensation network must be designed for the worst-case scenario (Figure 31). Here we consider only the variation in the load and keep the input voltage fixed at the nominal value.

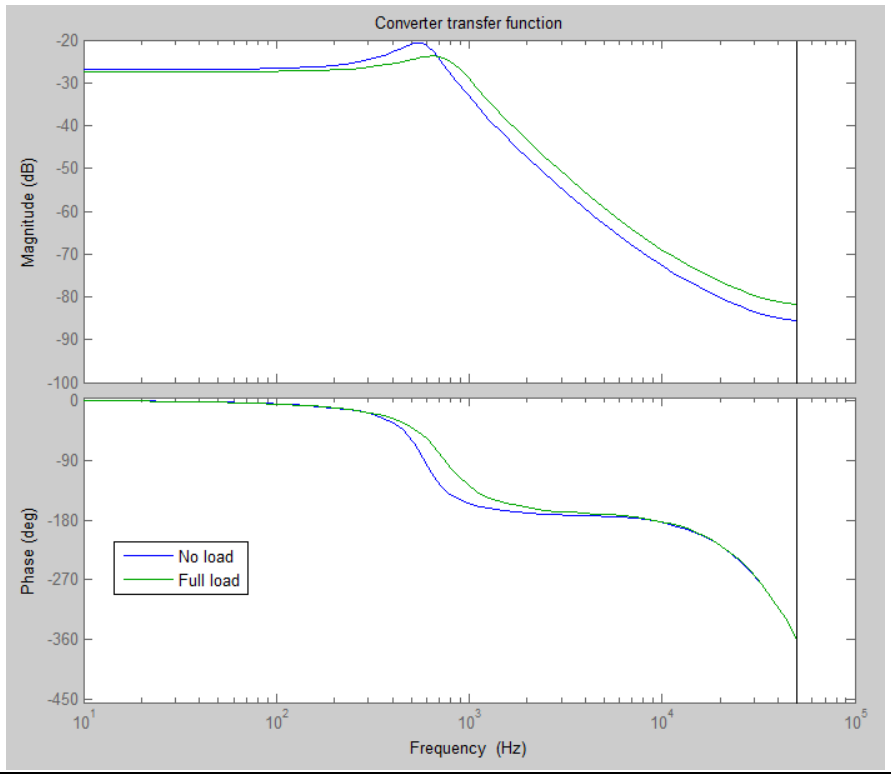

Figure 31 Open-loop frequency response of the PSFB 800 W converter under different load conditions, including modulation block

4.1.2 VMC discrete compensator

The system must be compensated for stability and dynamic performance. For this application only a voltage control loop is required (Figure 32).

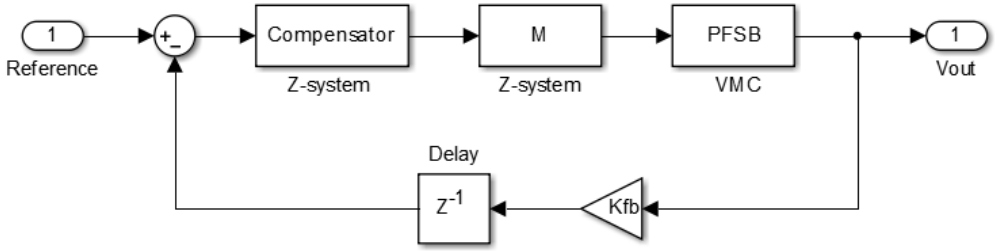

Figure 32 Closed-loop network for the PSFB converter and compensation

A two-pole and two-zero discrete compensator is designed and implemented to achieve a 10.3 dB gain and 54.6° phase margin (Figure 33).

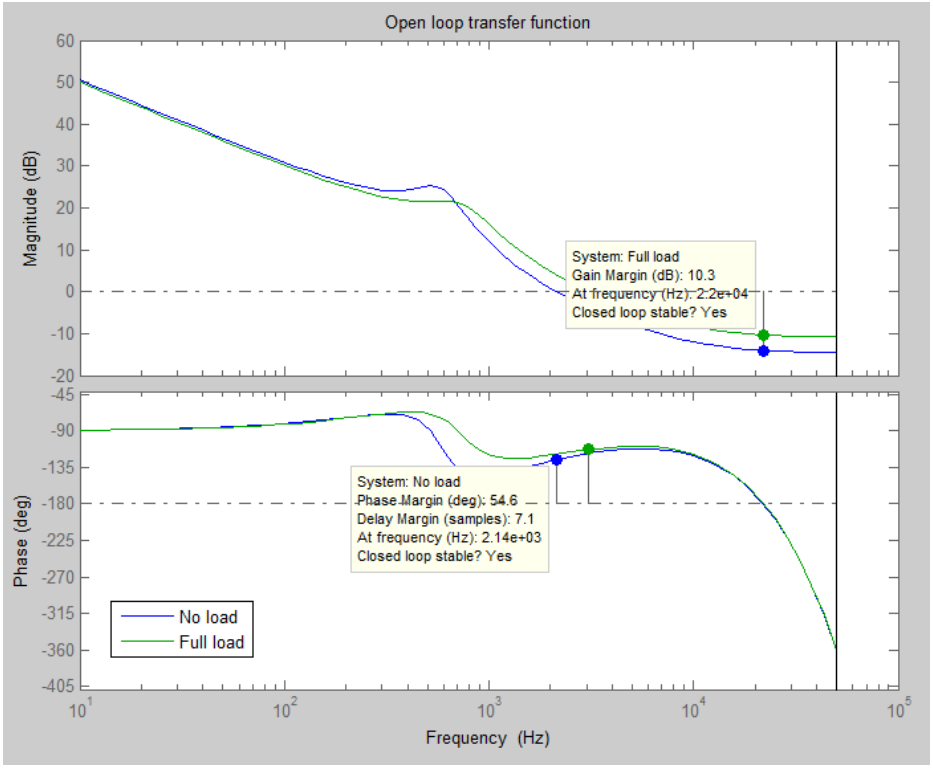

Figure 33 Loop gain frequency response and stability margins under different load conditions (input voltage fixed at nominal value)

4.2 Peak current mode control (PCMC)

PCMC modulation has, like VMC, a fixed frequency and 50% fixed duty for the leading leg as in Figure 27.

Lagging leg also has a fixed frequency and fixed 50% duty cycle in steady-state. However, during transients, pulses have a different duration to adjust the phase shift between both legs.

In PCMC the controller does not fix the timings for the pulses but the peak current to be reached during the power transfers. PWM is chopped right after reaching that value, and both C and D could have a shorter or longer duration to adjust the phase (Figure 34). The control delay is shorter for this modulation scheme, boosting the phase of the discrete controller.

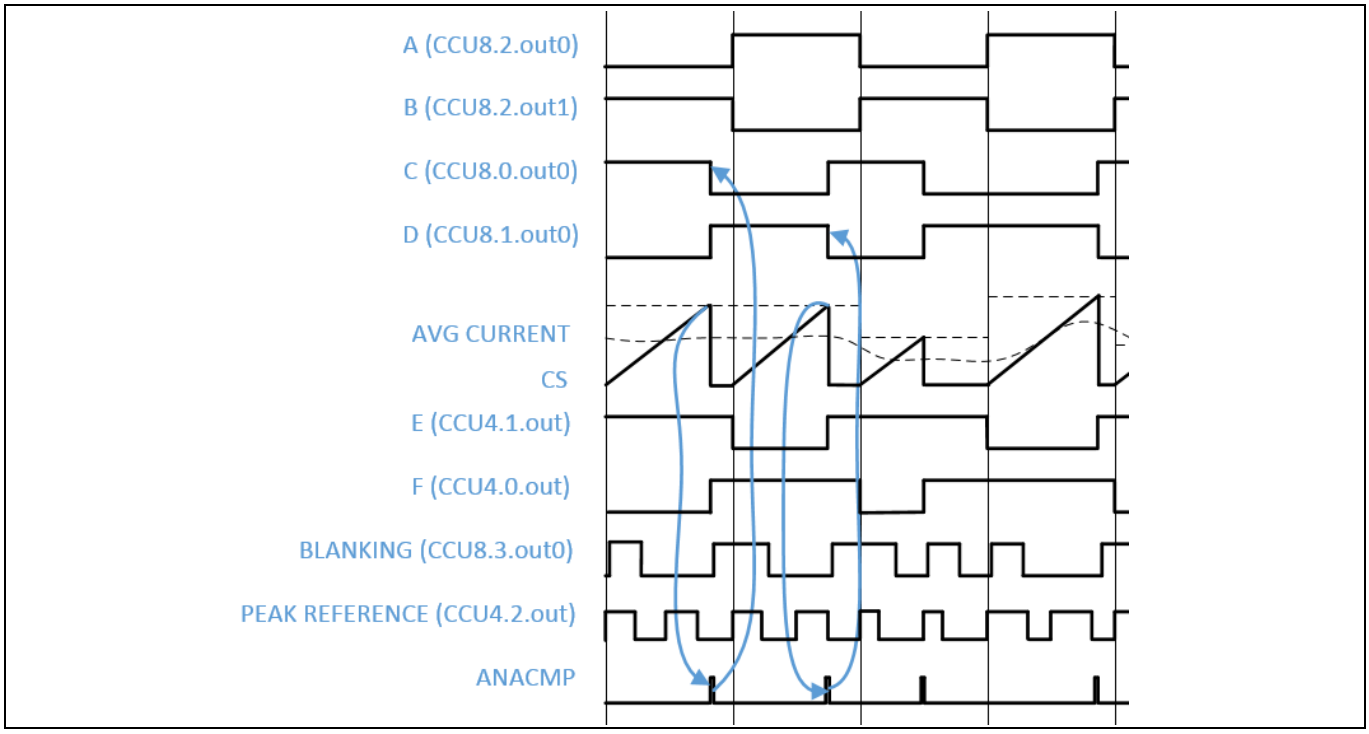

Figure 34 Current level comparison chops the PWM of the lagging leg

PCMC balances the current into the primary side of the transformer cycle-by-cycle. The phase overlap of C and D with A and B could differ, but the current will maintain its symmetry (in VMC only the timing is certain to be symmetrical). Any potential asymmetry of the transformer excitation voltage is corrected, without the need for additional components or careful design.

Advantages of PCMC implementation with XMC4200:

- Current in the primary of the transformer is balanced cycle-by-cycle, which avoids transformer saturation due to magnetizing current drift
- The analog comparators included in XMC42 are equipped with Digital to Analog Converters (DACs) and slope-generation capabilities. No additional external circuitry is required. The slope compensation is required for a stable peak control mode
- Less influence over the input voltage in the gain of the converter without additional compensation complexity

Possible disadvantages of PCMC in the proposed implementation:

- It requires more complex control, with special consideration to blanking times, current measurement signal conditioning, and soft-start procedures
- The included DACs in the XMC42 have up to 1023 possible levels. Resolution is limited in comparison to the VMC high-resolution steps

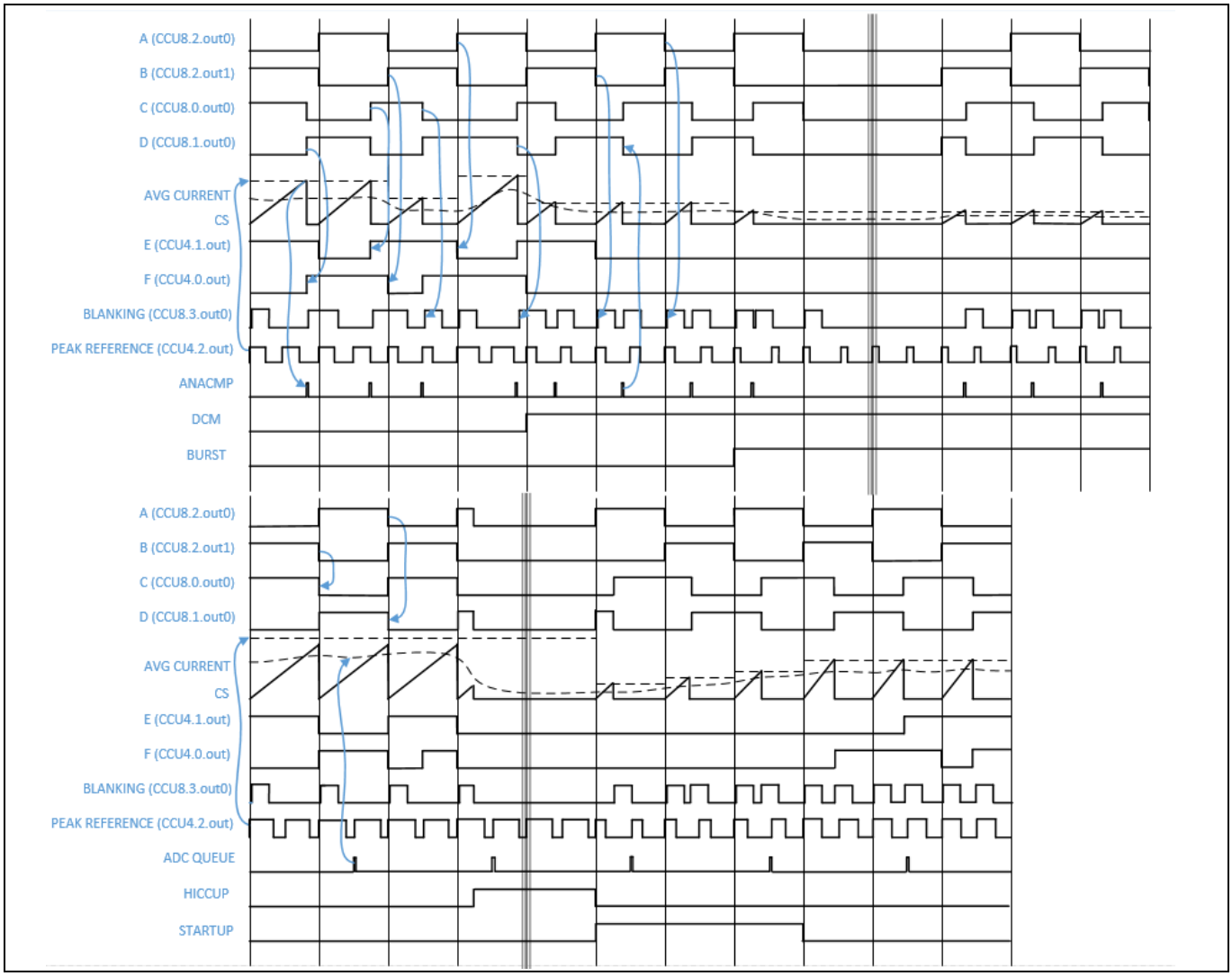

Figure 35 PCMC with XMC42

Figure 35 shows in more detail some signals and states of the controller in PCMC. Compare with VMC in Figure 29.

4.2.1 PCMC small-signal model

Small-signal analysis of PSFB with PCMC modulation can be found in the literature or derived. The model here has been extracted from [9].

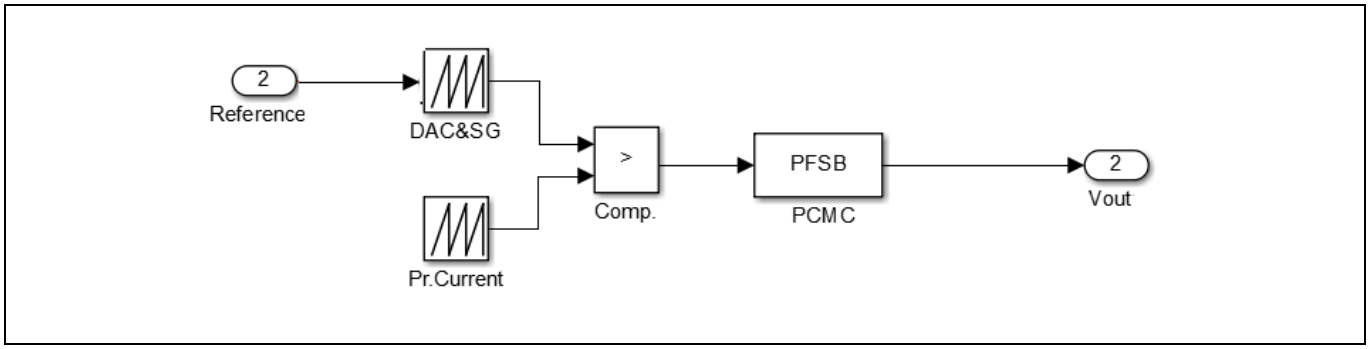

Figure 36 Modulation and converter open-loop path

The slope of the current in the primary side of the transformer including the gain of the signal conditioning is S_n. The slope compensation of the internal DAC is S_e. The gain of the modulation block for the PCMC is F_m (Figure 36).

$$M = V_{dd}/1023 \tag{7}$$

$$F_m = M * 2 * f_s/(S_n + S_e) \tag{8}$$

The gain of the current sense signal path is Fi.

$$Fi = n_{sense} * R_{sense} * A_{gain} \tag{9}$$

The equivalent impedance of the output filter is Zf.

$$Zf = \frac{(Lo * Co * (Ro + Rc) * s^2 + Lo + Ro * Rc * Co * s) + Ro)}{1 + Ro * Co * s} \tag{10}$$

The equivalent impedance of the load and the output capacitor is Zc.

$$Zc = \frac{Ro + Ro * Rc * Co * s}{1 + (Ro + Rc) * Co * s} \tag{11}$$

The transformer equivalent impedance is Rd.

$$Rd = 4 * n^2 * Llkg * fs \tag{12}$$

The transfer function of the converter, reference peak current to output voltage, is Gpv.

$$F2 = n * Vin * \frac{Zc}{Zf + Rd} \tag{13}$$

$$F4 = n * \frac{Vin}{Zf + Rd} \tag{14}$$

$$F7 = 1 + \frac{Rd}{Ro} \tag{15}$$

$$F9 = n * \frac{Vin}{Ro} \tag{16}$$

$$Gpv = Fm * \frac{F2}{1 + Fm * F9 * Fi + F4 * F7 * Fm * Fi} \tag{17}$$

In PCMC the load of the converter has low influence in the gain, and frequency response at full load and no load is almost equal (Figure 37).

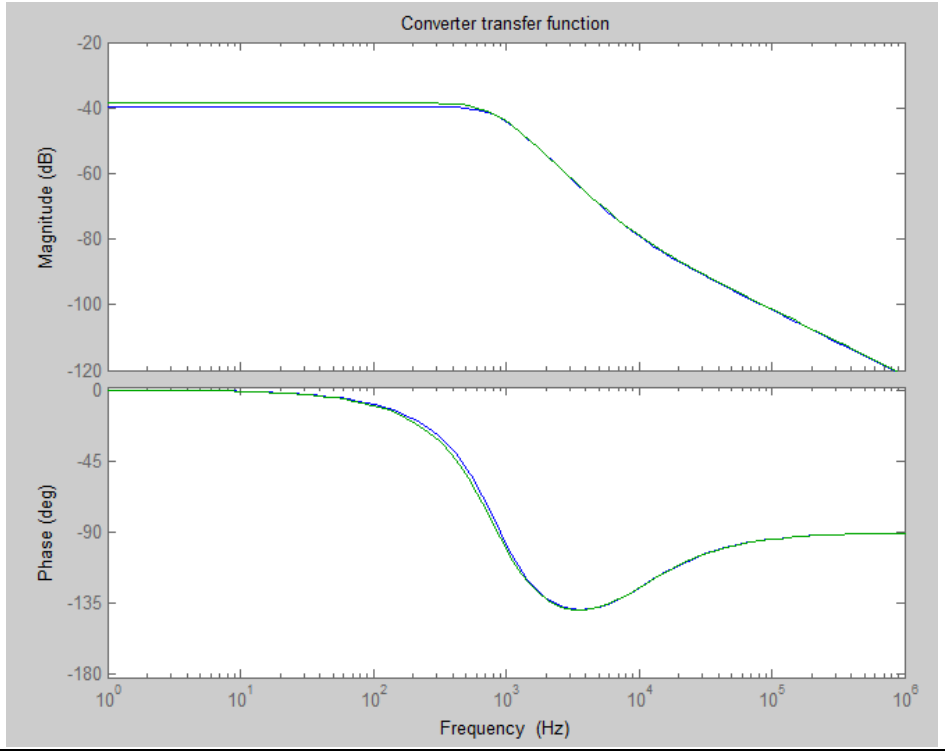

Figure 37 Open-loop frequency response of the converter including the modulation block, for PCMC of the 800 W PSFB

4.2.2 PCMC discrete compensator

In this mode, and for this application, there is only an outer voltage loop compensation network (Figure 38).

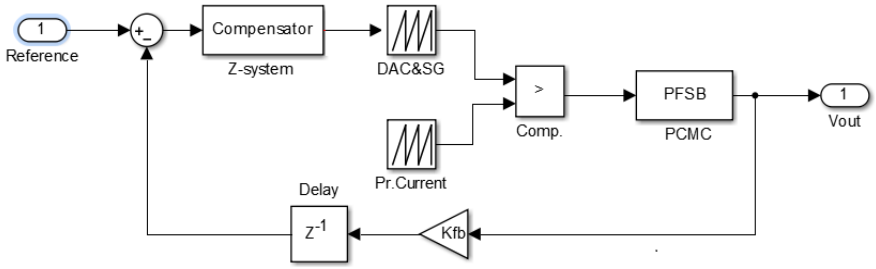

Figure 38 Compensated closed loop for PCMC

There is an inherent inner current control loop, given by the modulation scheme and stabilized by the slope compensation, which is the only control parameter to be designed in such a current loop. In the design shown, the slope compensation is integrated using DACs available in the comparators and slope generation module of the XMC4200 controller. Therefore, no extra circuitry is necessary to implement this control strategy.

A two-pole and two-zero discrete compensator is designed and implemented to achieve 14.7 dB gain and 53.4° phase margin (Figure 39).

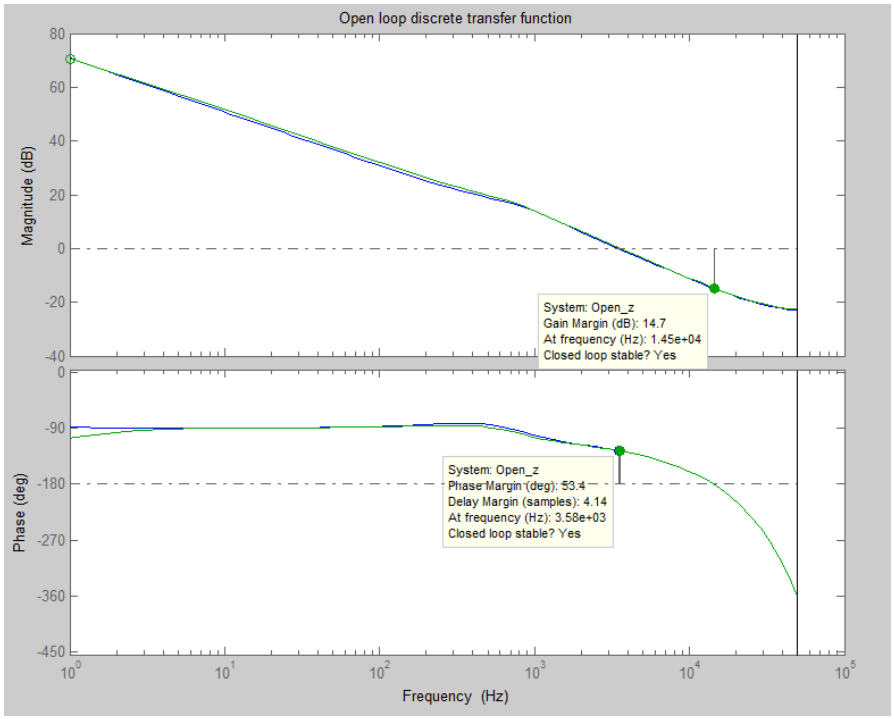

Figure 39 Loop-gain frequency response and stability margins for the designed PCMC control

4.3 Adaptive bridge dead times

Dead times between high side and low side pulses of a bridge leg may avoid short-through and give enough time for the output capacitance of the MOSFETs to be charged or discharged in order to achieve ZVS.

The energy available for the resonant transition changes as a function of the output load of the converter. Furthermore, the output capacitance of the high voltage devices is voltage dependent. As a consequence, the optimum dead times may change.

Leading leg may adapt dead times in order to switch always at the lowest point of the V_{ds} swing (valley) (Figure 40). The resonance period changes due to the non-linear output capacitance of the devices $C_{oss(tr)}$.

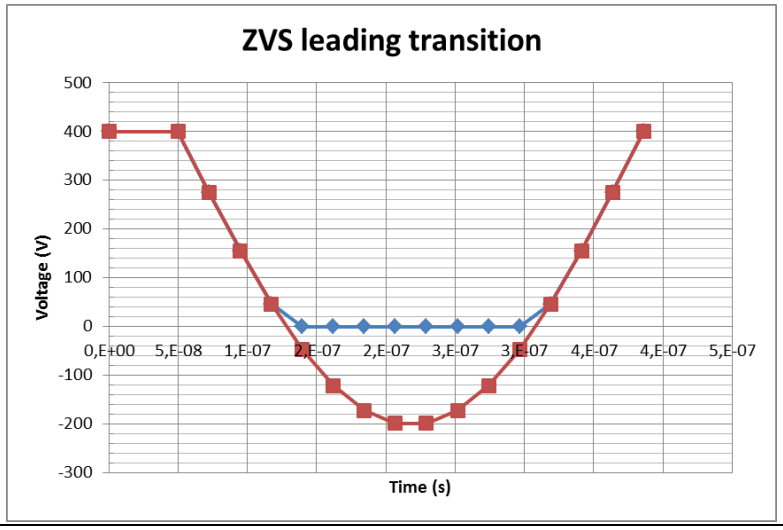

Figure 40 Leading leg resonant transition

The lagging leg may decrease the dead times for increasing loads to minimize the body-diode conduction and maximize the available effective duty cycle. The transition for the lagging leg is quasi-linear, but is also influenced by the non-linear output capacitance of the devices $C_{oss(tr)}$ (Figure 41).

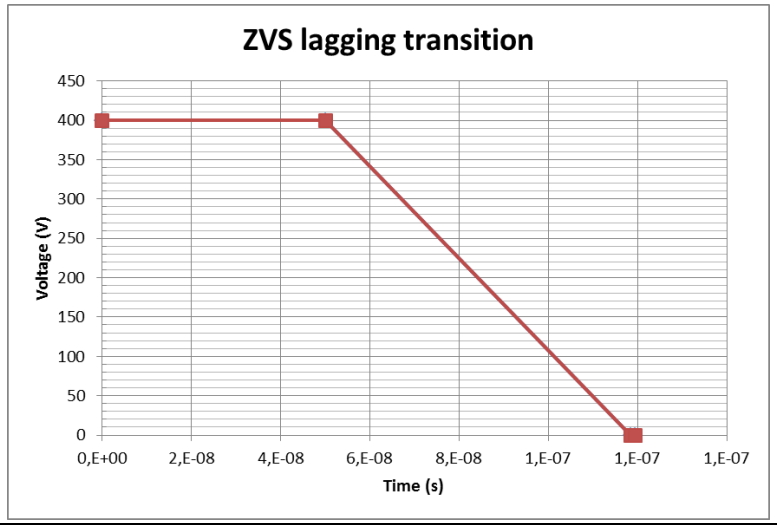

Figure 41 Lagging leg quasi-linear transition

The dependency optimum dead time to output load of the converter can be approximated by these linear formulas:

$$dtAB = dtAB_{nominal} - Io * \frac{dt_{factor}}{2^{ratio}} \quad (18)$$

$$dtCD = dtCD_{nominal} - Io * \frac{dt_{factor}}{2^{ratio}} \quad (19)$$

These formulas have little processing overhead and few parameters to adjust to reduce the optimization procedure effort (see 4.7.3).

4.4 Synchronous rectification

The rising edge of the synchronous gate E follows the falling edge of the switch gate D. The rising edge of the synchronous gate F follows the falling edge of the switch gate C.

A dead time is required between the fall of the bridge signal and the rise of the synchronous gate. The voltage in the drain of the synchronous MOSFET is falling after the resonant transition in the primary side of the transformer. The amount of time after the fall of the bridge signal decreases as a function of the output current of the converter (see 4.3).

The voltage in the drain of MOSFET E would rise again after the falling edge of gate B (a power transfer is about to start through the opposite branch). The time after the falling edge of gate B would increase as a function of the output current due to the effect of the L_{lkg} reducing the effective duty cycle.

Figure 42 Synchronous MOSFET gate pulse (yellow), V_{ds} (purple) and primary current of the transformer (green)– the turn-on delay is highlighted

When the average output current is lower than the current ripple of the output filter, the synchronous conduction goes into discontinuous conduction mode (DCM). Once the current becomes zero through the output choke, synchronous MOSFETS should be off to behave as pure diodes and avoid increased conduction losses due to negative current injection from the output.

There are three possible driving schemes for the synchronous rectifiers to minimize losses and overcome DCM of the output filter.

4.4.1 Synchronous MOSFETs as diodes (mode 0)

At no load or very light load, during start-up and during burst the synchronous driving is deactivated and the body-diodes conduct all the current.

Under certain loads the current through the synchronous MOSFETs is low enough for the conduction losses to be equal or lower than the driving losses. At this point, it is better to stop driving the synchronous MOSFETs.

It also ensures that under DCM of the output filter there is no negative current injected back, which will only increase conduction losses and decrease performance.

4.4.2 Synchronous MOSFETs active during power transfer (mode 1)

In this mode synchronous MOSFETs are only driven during the power transfer.

Figure 43 Synchronous MOSFET gate pulse (yellow), V_{ds} (purple) and primary current of the transformer (green)

Under light load the secondary side may enter DCM. This mode avoids negative current through secondary rectifiers with lower losses than the pure diode conduction mode.

In this mode the modulation scheme of the synchronous MOSFETs changes: the rising edge of gate E is linked to the falling edge of gate A and the falling edge of gate E is linked to the falling edge of gate C, the rising edge of gate F is linked to the falling edge of gate B and the falling edge of gate E is linked to the falling edge of gate D.

4.4.3 Synchronous MOSFETs inactive during opposite power transfer (mode 2)

Synchronous MOSFETs are active during both the power transfer and the recirculation time, only skipping the power transfer of the opposite branch.

For maximum efficiency, the driving of the synchronous MOSFETs should minimize body-diode conduction but should maintain enough margins not to overlap voltage in the drain (V_{ds}) and voltage in the gate (V_{gs}).

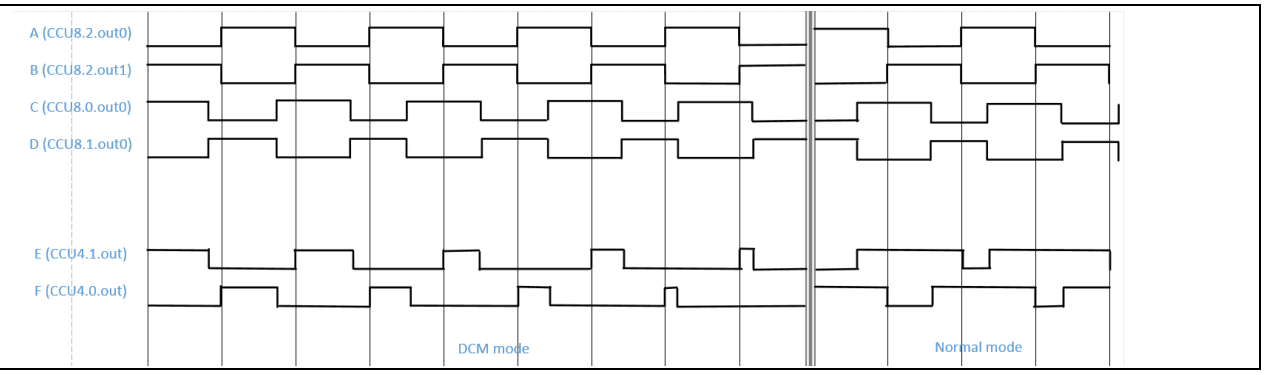

Figure 44 Synchronous MOSFET modulation schemes: modes 1 and 2

4.4.4 Adaptive synchronous conduction time

For increasing output currents, the effective duty cycle is reduced. The margin V_{gs} to V_{ds} of the synchronous MOSFETs increases as well due to the finite time for the resonant inductance current reversion.

A dynamic adjustment of the conduction times of the synchronous MOSFETs, displacing both the rising and falling edges, minimizes the body-diode conduction time. The nominal turn-on and nominal turn-off are indicated by the vertical blue lines in Figure 45. The introduced delays are represented by the shaded blue boxes.

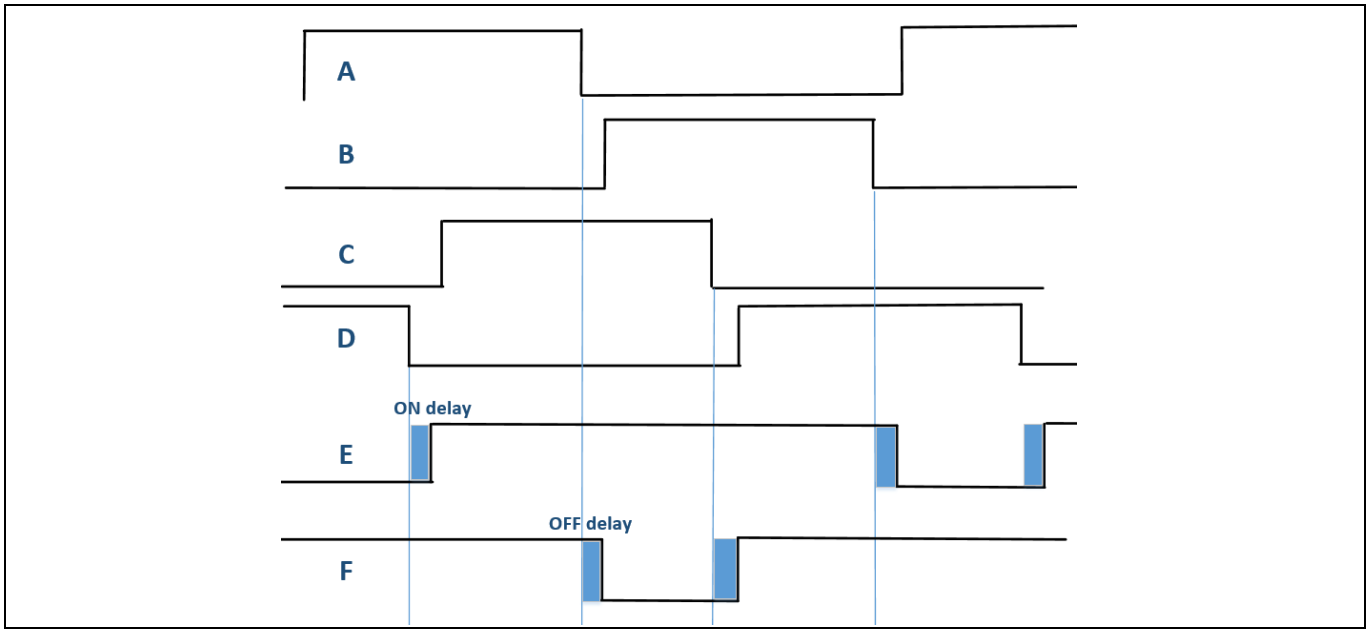

Figure 45 Adaptive delay in the turn-on and the turn-off of the synchronous MOSFETs

A linear function is applied to move the rising and falling edges, based on the average transformer primary current:

$$dtON = dtON_{nominal} - Ipr * \frac{dt_{ONfactor}}{2^{ONratio}} \quad (20)$$

$$dtOFF = dtOFF_{nominal} - Ipr * \frac{dt_{OFFfactor}}{2^{OFFratio}} \quad (21)$$

The parameters for those functions can be set through the GUI and stored in the internal memory of the controller.

4.5 Burst mode

At light load burst mode is used to further decrease losses at the expense of higher output voltage ripple (Figure 46).

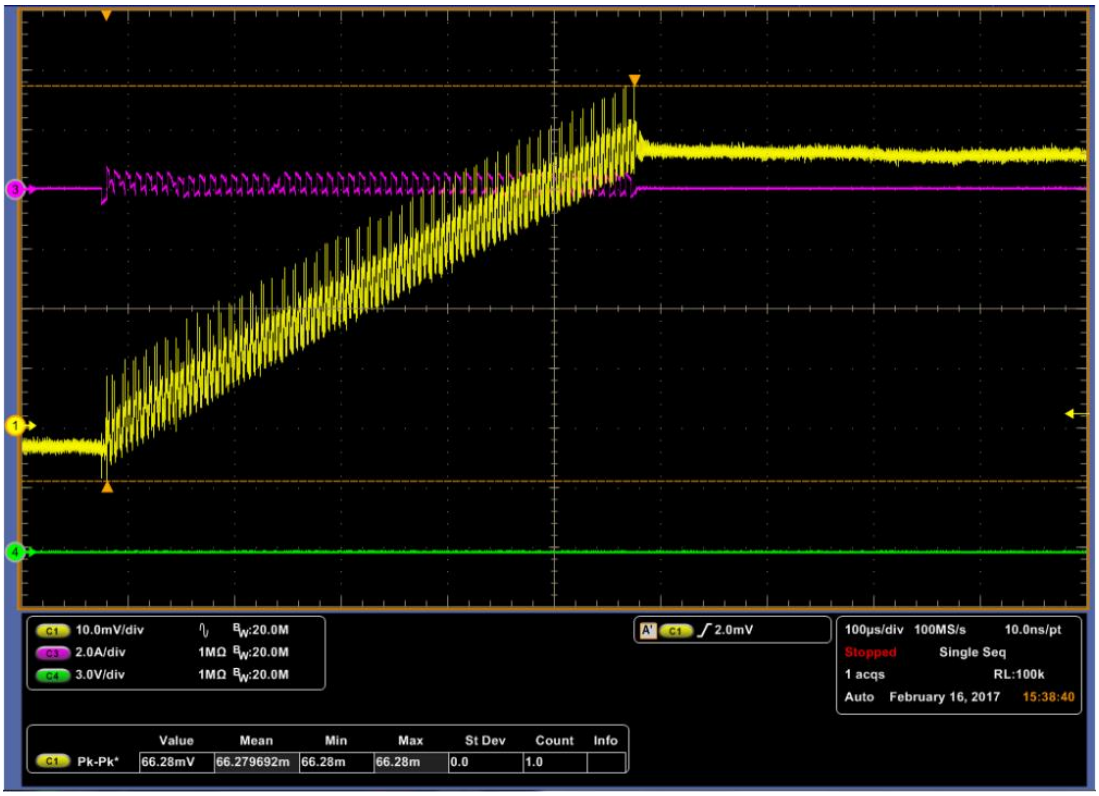

Figure 46 Burst ripple: output voltage (yellow), primary current (purple)

4.5.1 Maximum-frequency limited burst

A fixed number of pulses are applied to the bridge ($BURST_{LENGTH}$). An even number of pulses is preferred, to maintain the transformer excitation voltage symmetry. Bursts of pulses always start at the same gate signal, also to avoid excitation asymmetries.

The amount of time until the next burst starts ($BURST_{TRAP}$) can be configured. In this way there is a fixed relation between the number of pulses and the time between bursts that determines the maximum frequency of the burst.

$$F_{BURSTmax} = \frac{BURST_{TRAP}}{BURST_{TRAP} + BURST_{LENGHT}} * CTRL_{frq} \quad (22)$$

$$CTRL_{frq} = 100kHz \quad (23)$$

The minimum frequency varies depending on the load conditions. A hysteresis window delimits a non-switching, a burst mode and a normal switching range (Figure 48) as a function of the compensation network output.

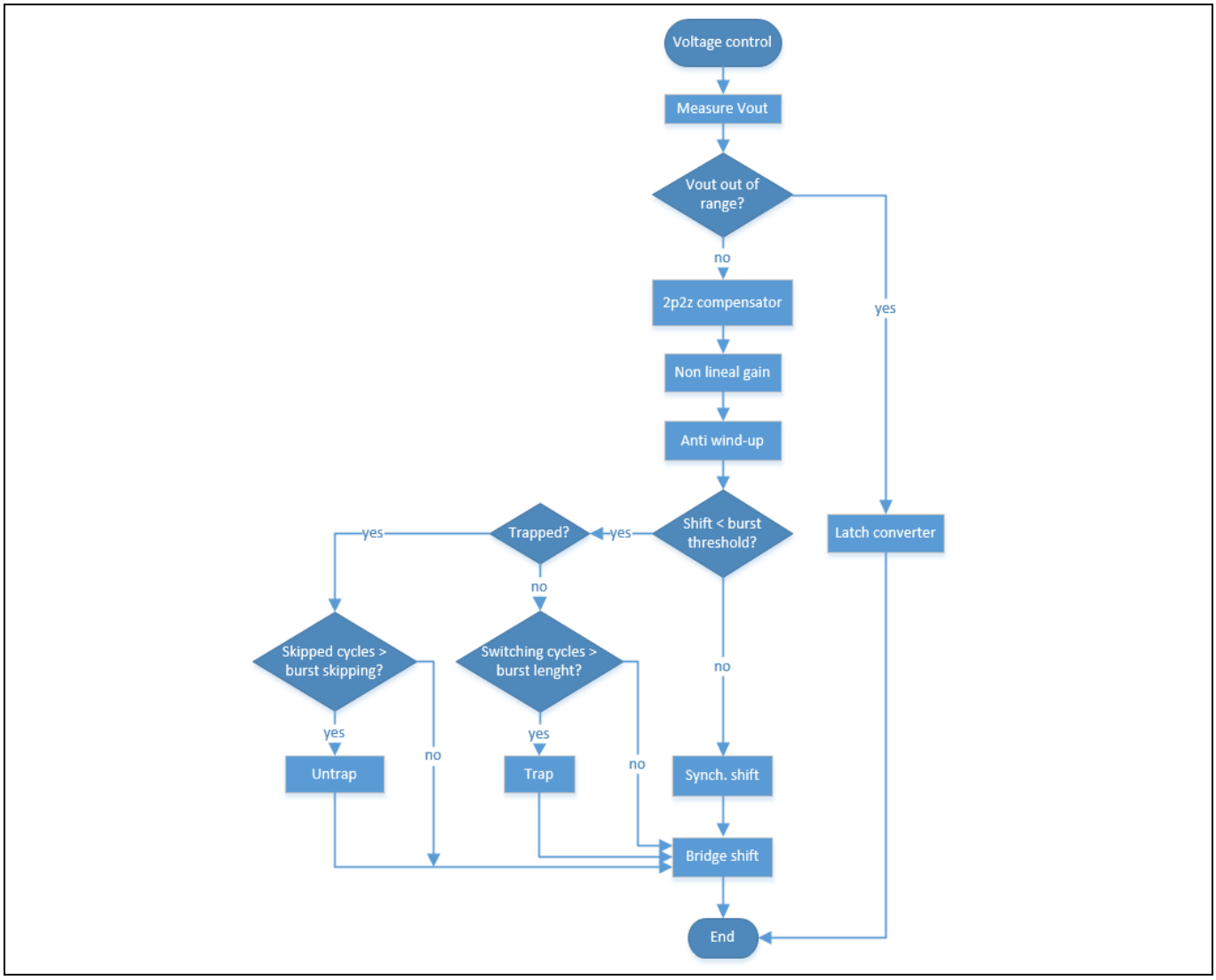

Figure 47 Regulation and burst control flow diagram

The parameters influencing the burst algorithm (Figure 47) behavior are:

- Burst stop: lower limit of the hysteresis window delimiting the non-switching and the burst mode ranges (see Figure 48)
- Burst low threshold: lower limit of the hysteresis window delimiting the burst mode and the normal mode ranges
- Burst high threshold: upper limit of the hysteresis window delimiting the burst mode and the normal mode ranges
- Minimum phase: minimum phase shift applied to the gate signals during normal mode
- Burst phase: minimum phase shift applied during burst mode. Setting high values may increase burst ripple but improve efficiency
- Burst skipping cycles: number of switching cycles skipped after a burst ($BURST_{TRAP}$ in equation 22)
- Burst length: number of pulses applied during a burst ($BURST_{LENGTH}$ in equation 22)

These parameters can be adjusted using the GUI and stored in the internal memory of the microcontroller.

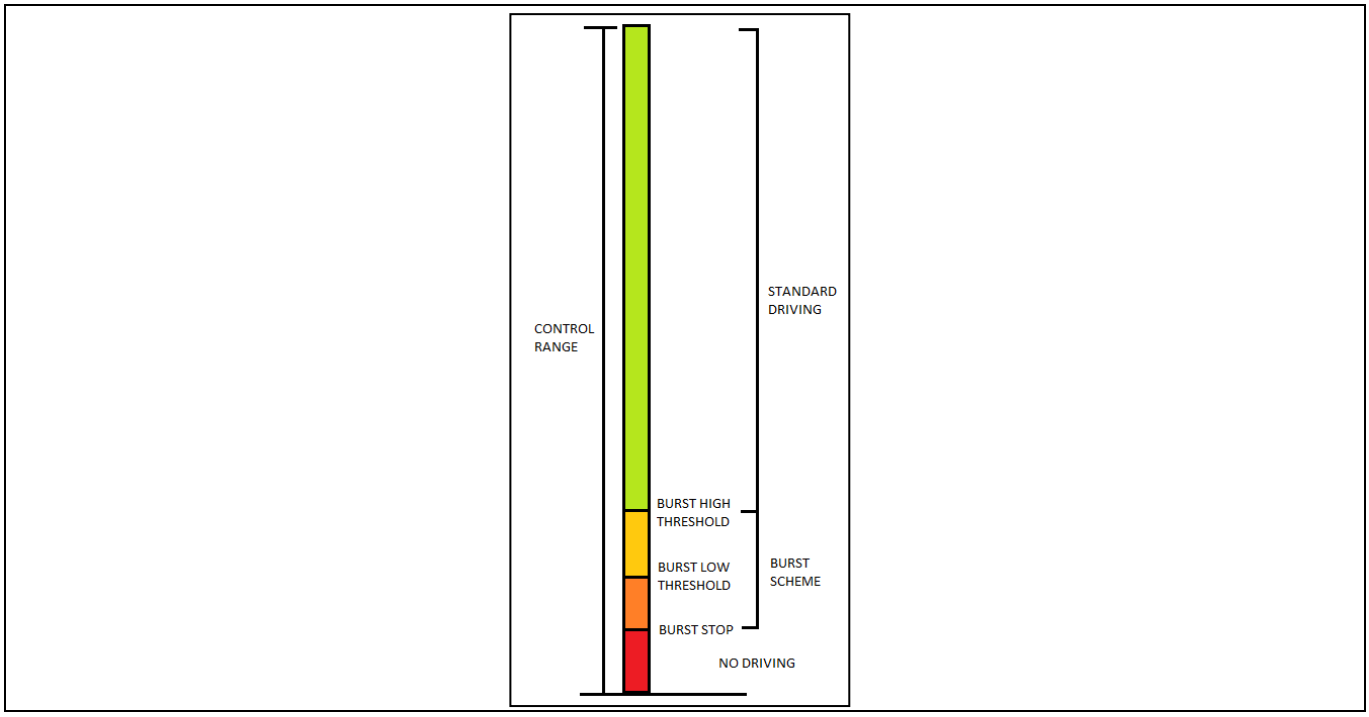

Figure 48 Burst mode thresholds based on the compensator output

4.6 Protections

4.6.1 Overcurrent (OC) protection

There are several redundant mechanisms for OC protection of the converter, described in detail in the following sections.

4.6.1.1 Cycle-by-cycle OC protection

In PCMC there is an inherent cycle-by-cycle peak current limitation of the primary current.

In VMC there is also a cycle-by-cycle peak current limitation, but in this case fixed at the maximum rated current for the bridge. During a cycle-by-cycle limitation VMC will behave like PCMC (Figure 49).

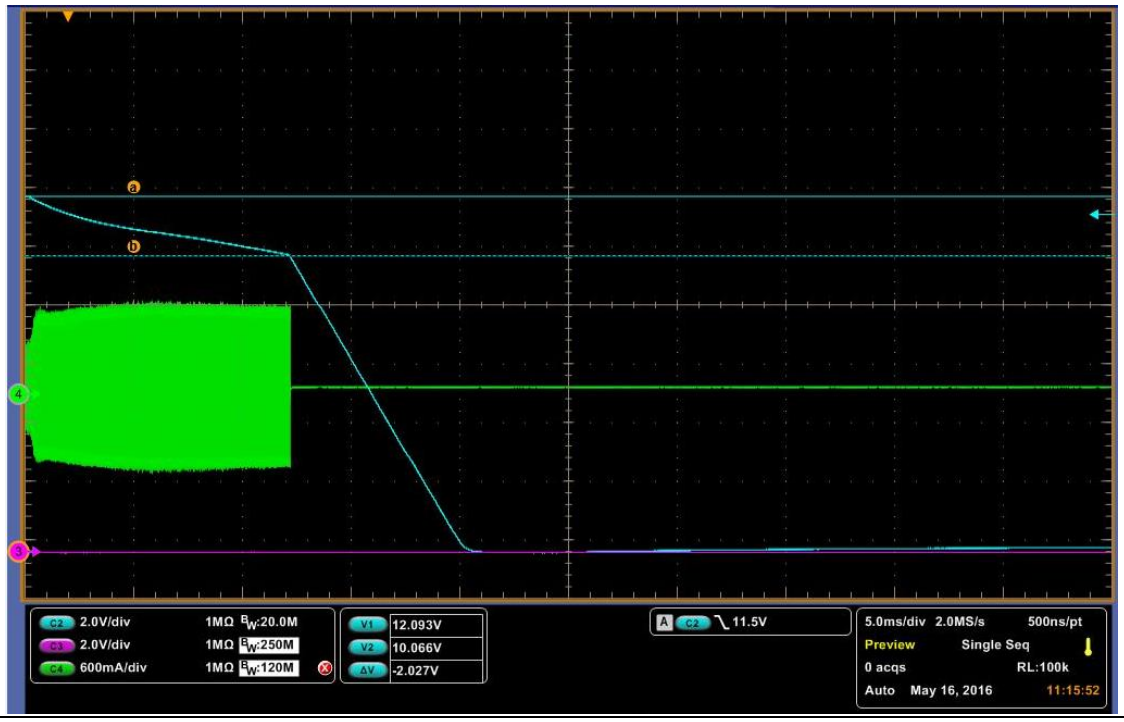

Figure 49 Cycle-by-cycle limitation in an output short-circuit event: primary current (green), output voltage (blue)

4.6.1.2 Output OC protection

There is no direct output current measurement in the PSFB 800 W design. Output current is calculated as a function of the input current and the input voltage. The same input current is proportionally higher output current for higher input voltages.

This is the formula applied for the scaling of the OC protection not requiring direct measurement of the output current:

$$I_{limit} = I_{limit\_nominal} - (Vin - Vin_{min}) * HICCUP_{factor}/2^{HICCUP_{ratio}} \quad (24)$$

$HICCUP_{factor}$ and $HICCUP_{ratio}$ approximate the output current proportional dependency with the input voltage. These parameters are hard-coded into the firmware of the converter.

After a prolonged overcurrent event the converter will enter hiccup mode. It will stop and try to restart after a pause (Figure 50). The converter will operate normally after the over-load resumes.

In the event of a severe output over-load, the start-up sequence will be canceled and the converter latched up.

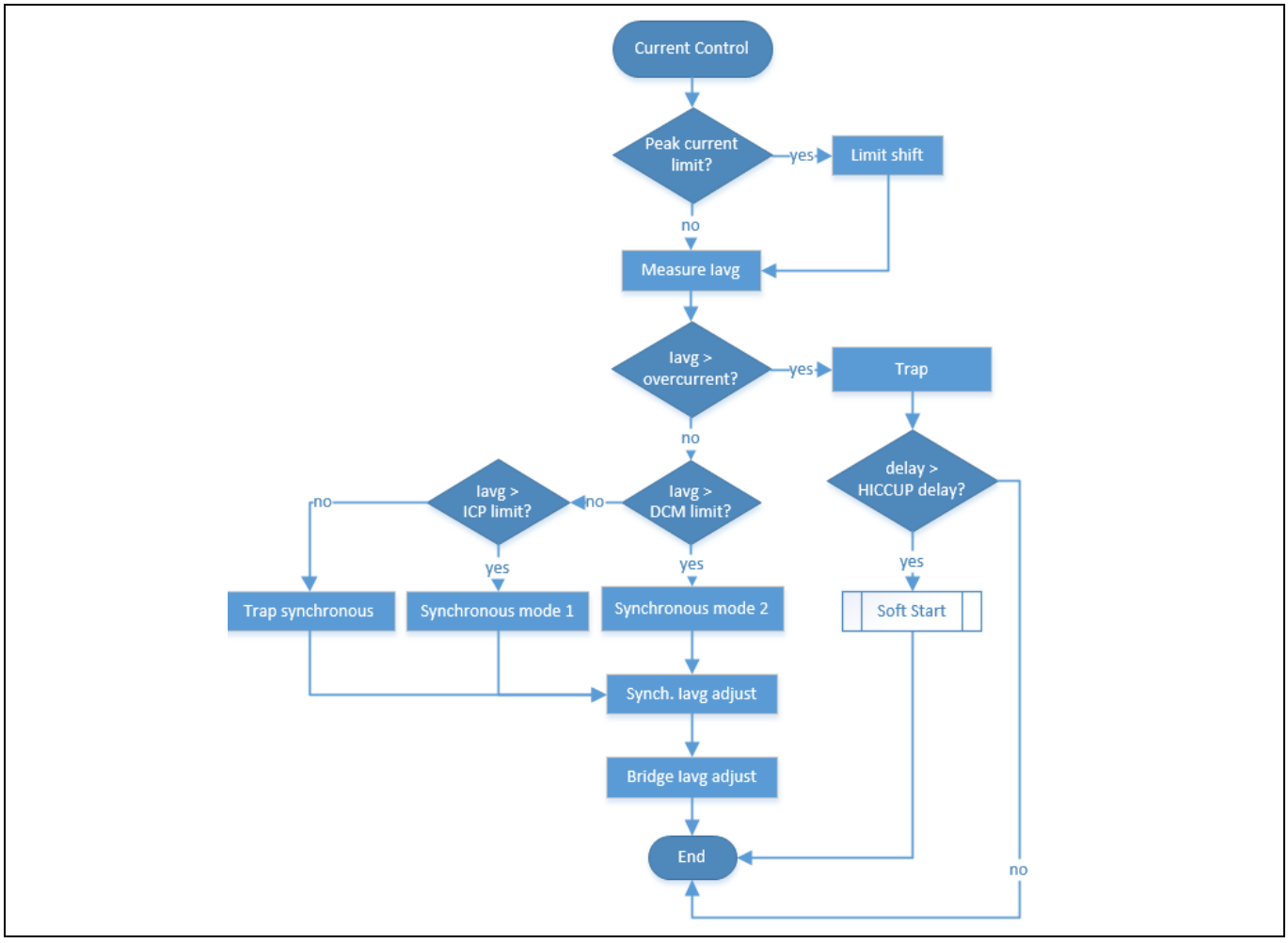

Figure 50 Output overcurrent detection flow diagram

4.6.2 Input undervoltage-overvoltage (UV-OV) lockout

The converter PSFB 800 W is designed to operate at a certain input voltage range. Input UV-OV lockout, hereafter referred to as brown-in and brown-out protection, ensures that the converter does not work outside of those conditions, in order to protect the system and the devices from excessive stress outside of the specifications.

There is a hysteresis window for the brown-in and brown-out thresholds. The converter starts running above 350 V and stops again whenever the input voltage decreases to 340 V.

Above 420 V input the converter stops and will start again if the input voltage decreases to 400 V.

An isolated amplifier is used for the measurement of the input voltage from the secondary side. The isolated amplifier has a deviation in the gain between samples, and due to this, the levels should be tuned.

Only the 350 V level has to be parametrized. The rest of the levels are calculated by the controller as an offset from the 350 V point. The parameter can be adjusted using the GUI provided (Figure 60).

4.6.3 On-off control

If the converter is connected to the user interface there is the option of remote start and stop. The on-off mechanism precede the brown-in-out (see Figure 51).

Note: *Brown-in and brow- out mechanisms prevail over the remote start and stop command. Only under the specified operating range can the converter be started – unless the brown-in-out protection is deactivated from the GUI.*

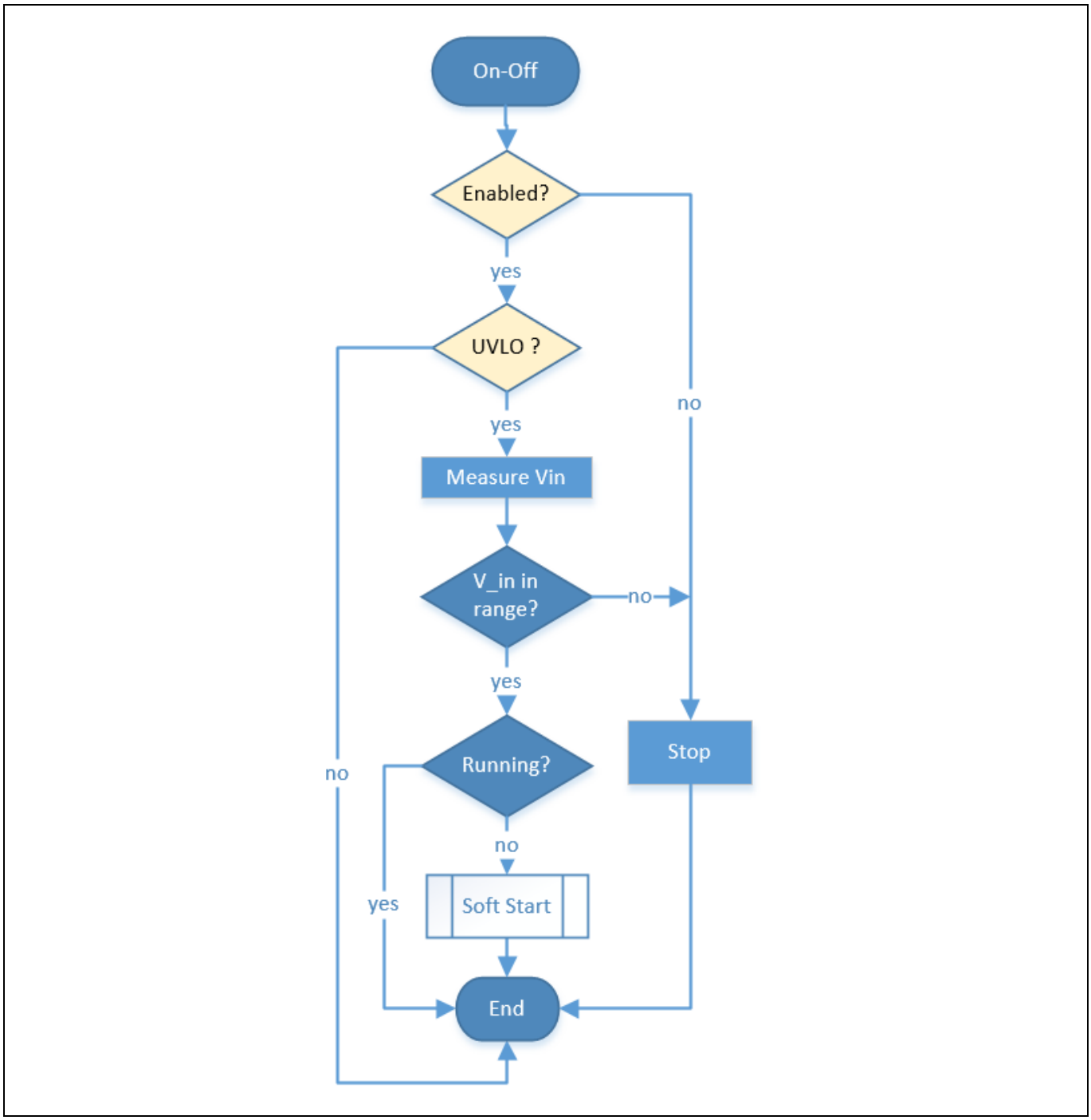

Figure 51 Brown-in-out and on-off flow diagram

4.6.4 Soft-start

The soft-start procedure ensures low stress for the devices when the output capacitor of the converter is discharged.

The soft-start sequence uses closed-loop regulation and ramps up the reference. The reference output voltage starts at the initial remaining value of the output capacitor and increases progressively in defined steps and defined delays (hard-coded into the firmware) up to the final nominal output (see Figure 53 and Figure 54).

The total duration of the soft-start sequence will depend on the compensation bandwidth, the size of the steps and the forced delays mentioned in the previous paragraph. For this application, as seen in Figure 52, soft-start at full load takes approximately 120 ms.

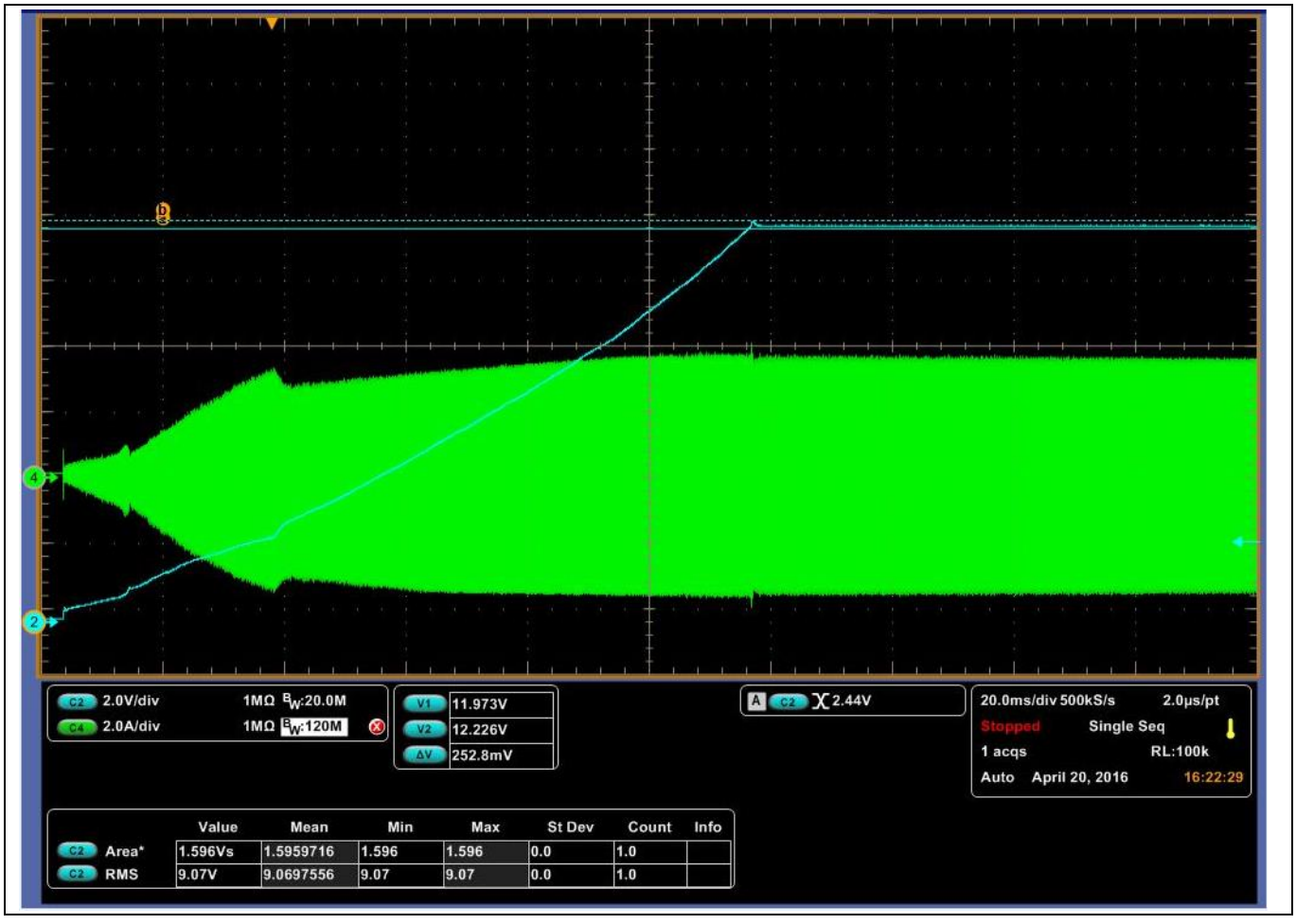

Figure 52 Soft-start at full load: primary current of transformer (green) and output voltage of converter (blue)

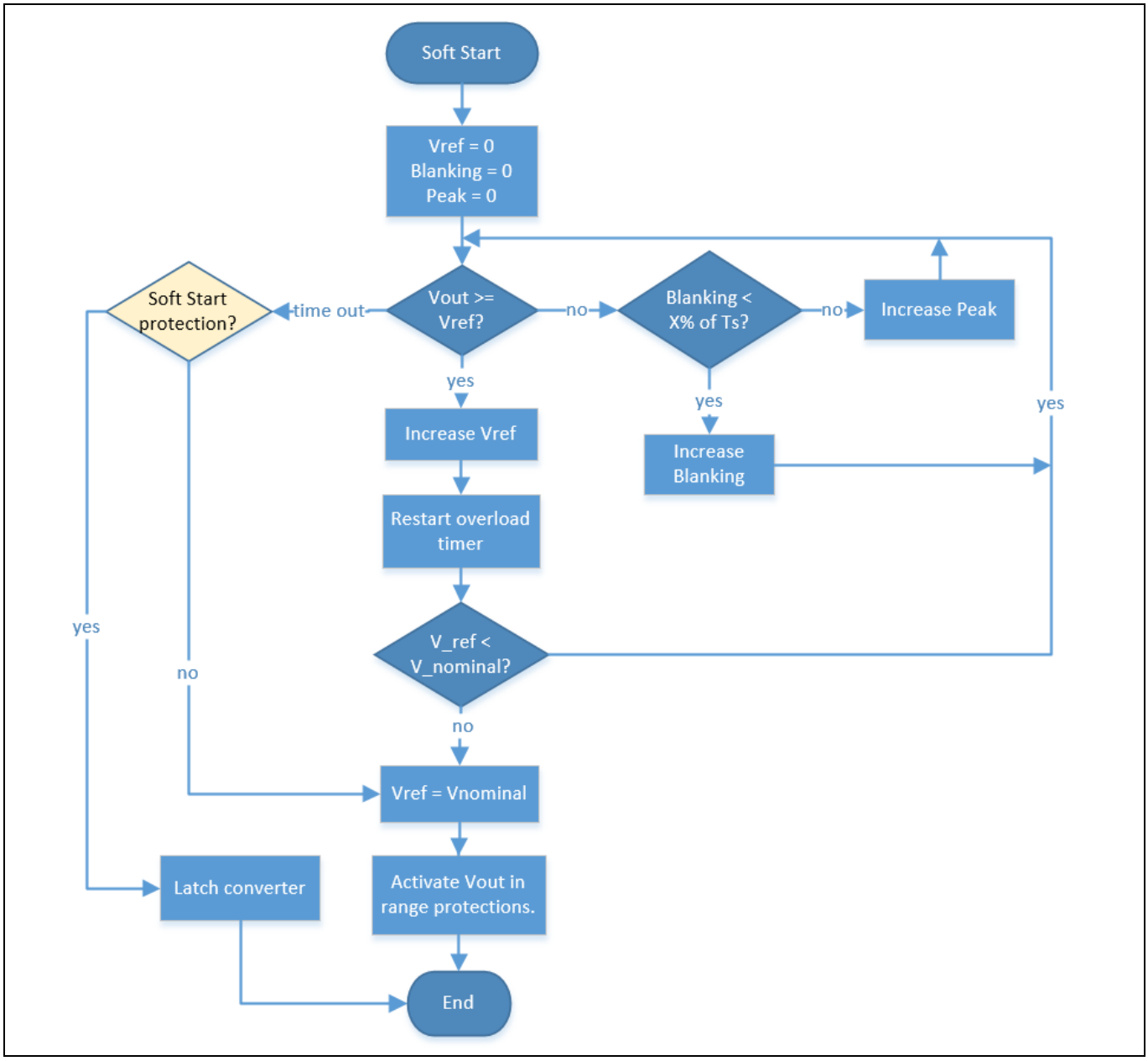

Figure 53 Soft-start procedure, PCMC

A timer would trigger an over-load protection if the output voltage does not rise. This protection will latch the converter.

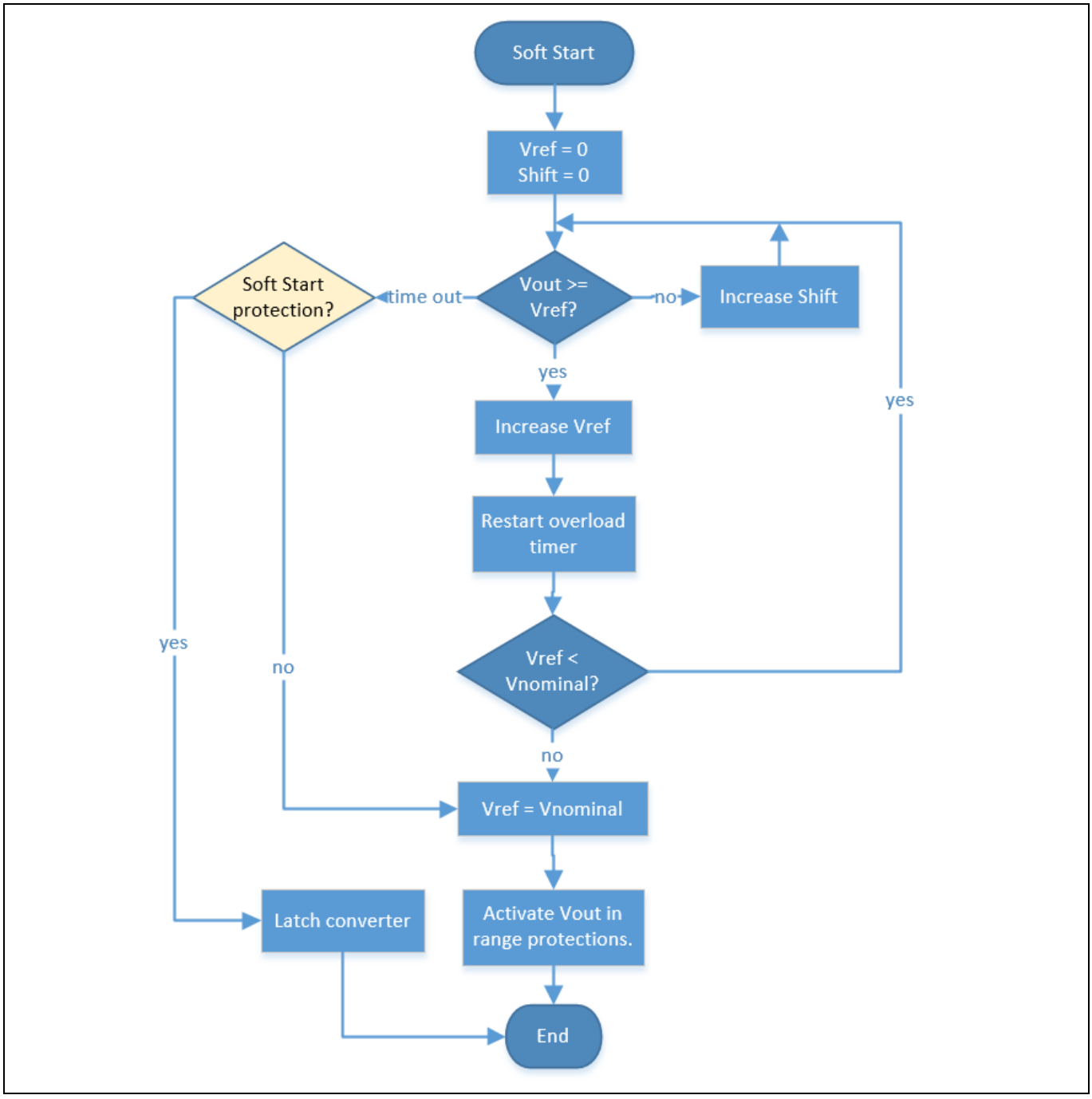

Figure 54 Soft-start procedure in VMC

In case of an OC event the converter will go into hiccup mode. Under extreme conditions, like short-circuit at start-up, a cycle-by-cycle peak current protection will prevent excessive stress on the system.

4.6.5 Output voltage out-of-range protection

Two main mechanisms protect the output voltage going out of the regulation window.

If the output voltage goes above 13.5 V the converter is latched. This will prevent excessive stress in the secondary low voltage devices and detect regulation problems (open-loop protection).

If the output voltage goes below 10.5 V, the converter is latched (Figure 49). Output voltage will fall under this threshold under severe over-load conditions (short-circuit). This mechanism is an extra protection for the bridge and synchronous devices.

The output voltage nominal level can be tuned from the GUI. However, the regulation window is hard-coded into the software (see Figure 55).

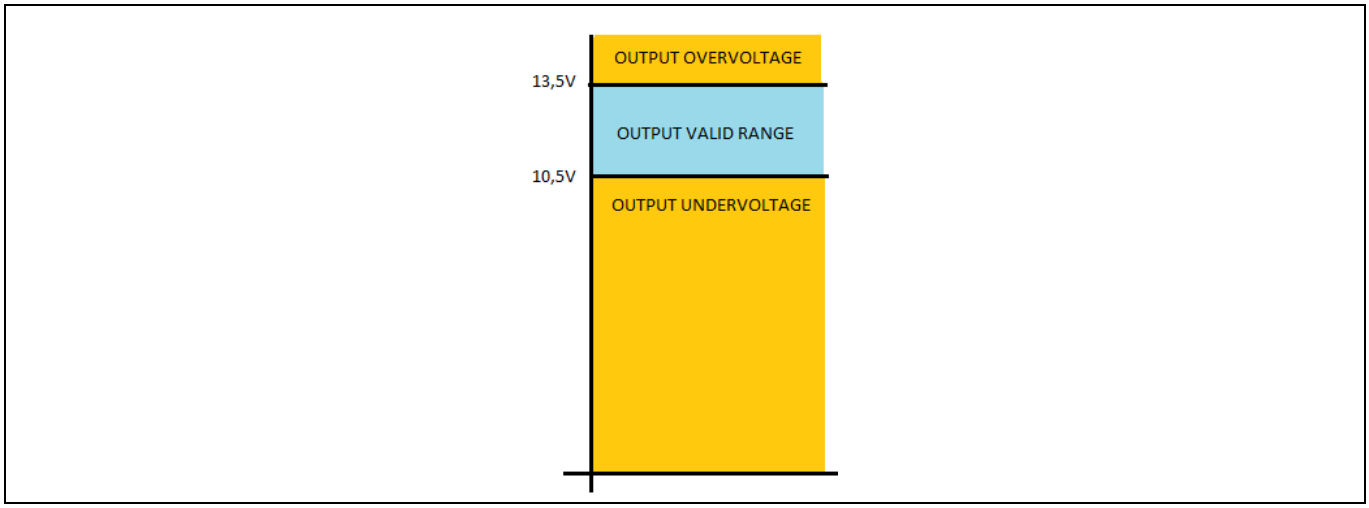

Figure 55 Output voltage out-of-range protection

4.6.6 Temperature control

A PWM-controlled variable-speed fan is mounted on-board, and air-flow will depend on the input current and/or temperature of the transformer (the hottest point of the design). The precedent is for the mechanism to require higher air-flow (see Figure 56).

The fan tachometer signal can be used to prevent a blocked rotor. If no tachometer is available, the protection can be deactivated in the GUI.

Note: Do not run the board without air-flow under heavy loads or during long intervals.

If the temperature of the transformer rises above the warning level the LEDs on the control card will blink with a specific pattern (see 4.7.9). If the temperature increases above the warning range the converter will stop and latch. The warning and overtemperature levels are hard-coded into the firmware.

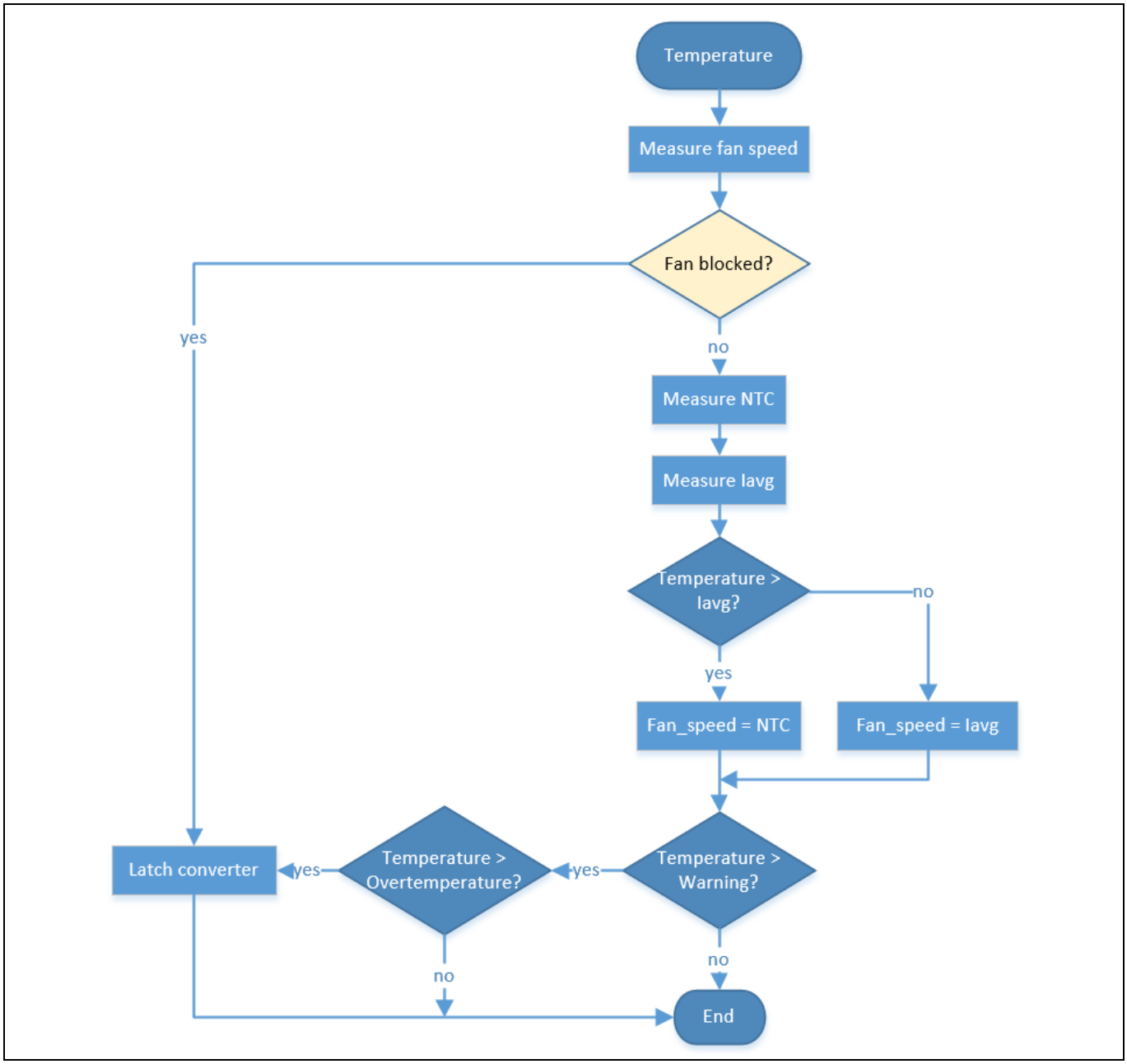

Figure 56 Temperature control flow diagram

4.7 User interface

The XMC42 controller includes communication peripherals with capabilities for UART, SPI, and I2C protocols.

PSFB 800 W control card uses serial communication (UART) to connect with an external system. We provide a user interface (GUI) running under Windows as an example of remote management (see Figure 58). The serial interface provided with the kit can be used to link the converter to a Windows system via a USB port.

Note: *The GUI is optional, for possible customization or monitoring. The converter is fully operational when disconnected from the user interface.*

Note: *The controller implements a proprietary protocol with a reduced set of commands and message types not listed in this guide.*

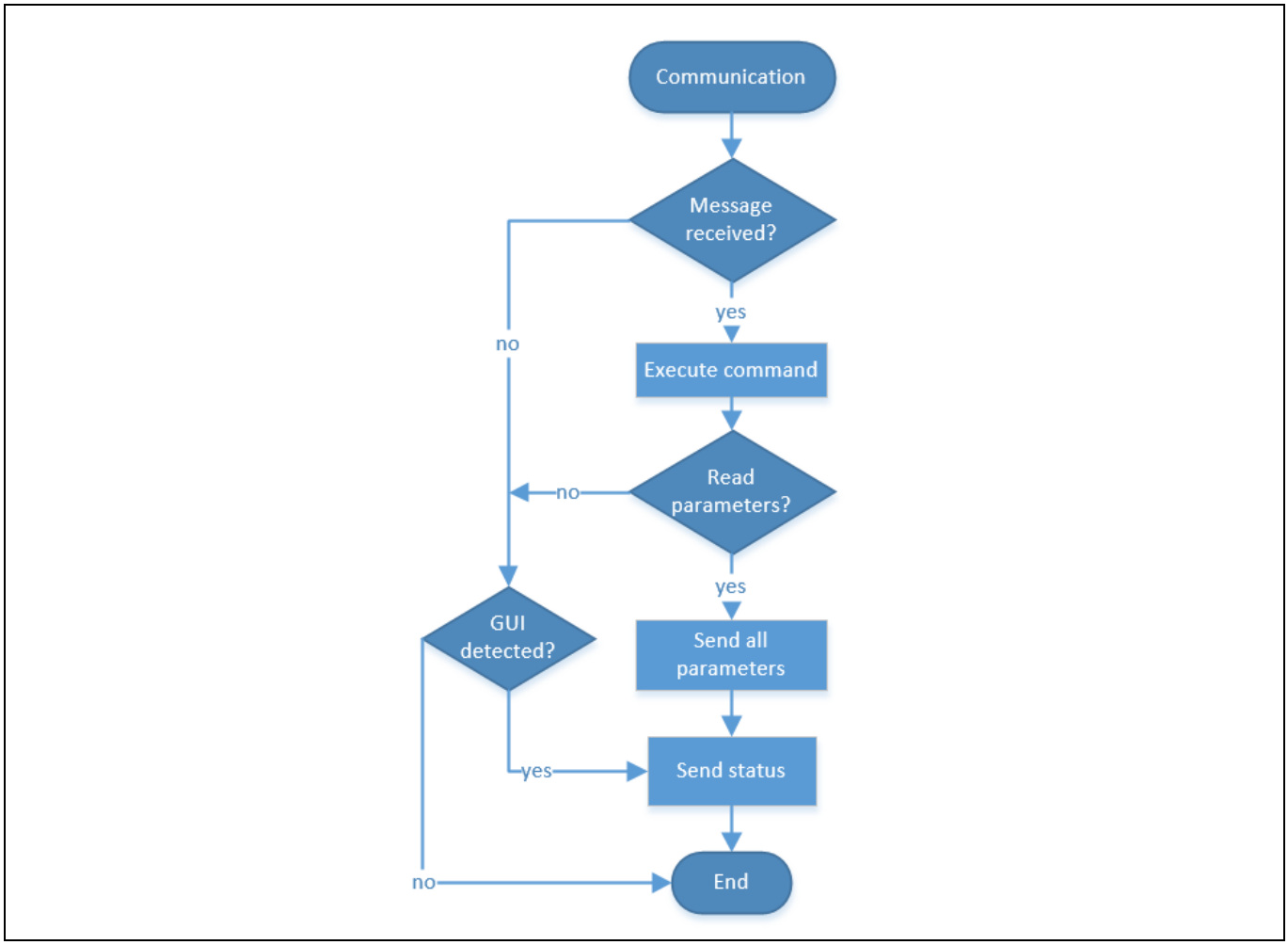

Figure 57 Communication routine flow diagram

Once the controller detects the connection with the GUI it will send the internal configuration of the converter, the current status and possible faults (see Figure 57).

Note: *This is an isolated high voltage system. Use an isolated serial communication port to connect the converter and a computer.*

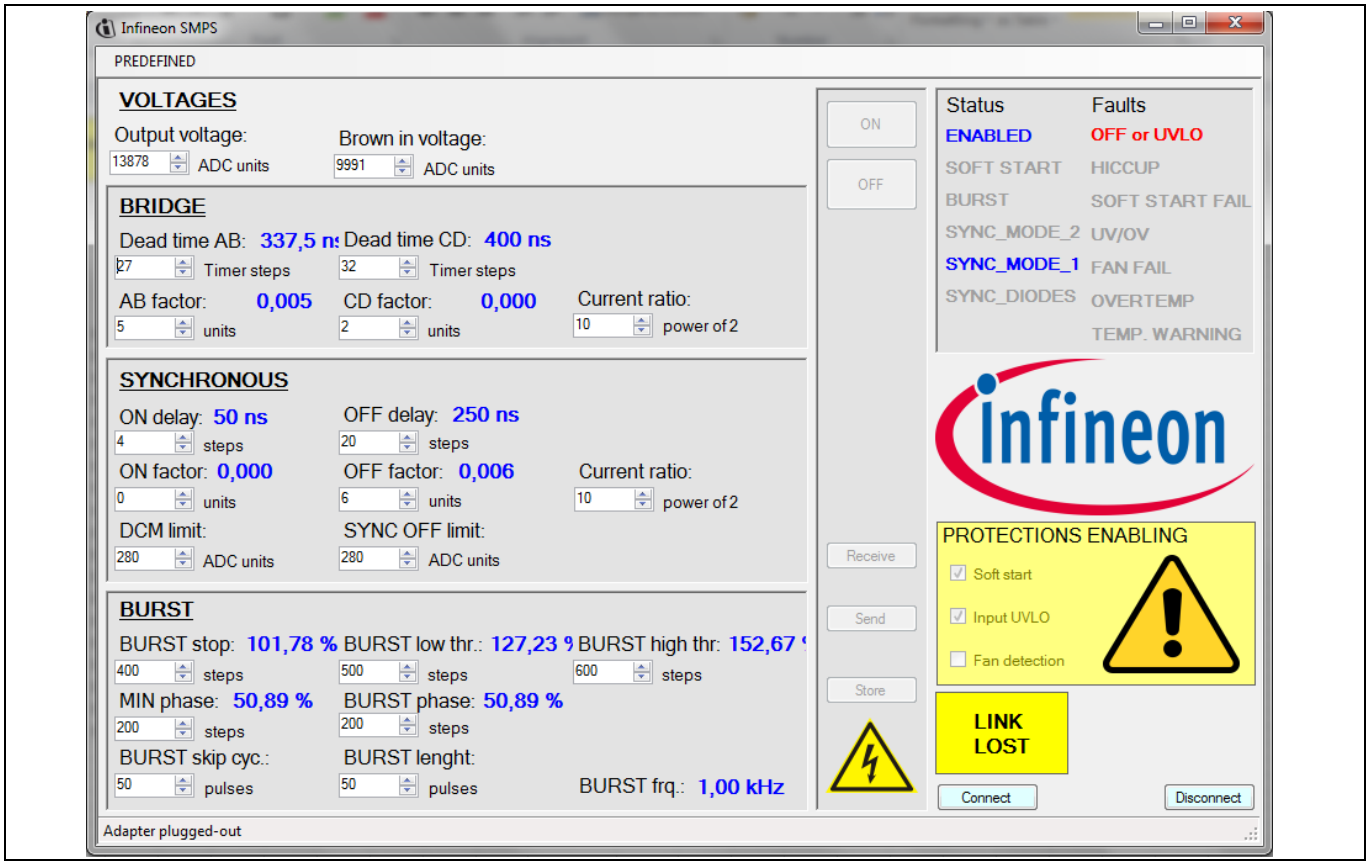

Figure 58 User interface detects the connection to a converter

The panels on the left contain configurable parameters for the converter firmware. The range for each of the values is limited both in the GUI and internally in the converter firmware, but a wrong combination of settings could lead to a system malfunction. The different settings are explained in more detail in the following sections.

The parameter values are permanently stored in the internal memory of the microcontroller. For storing the new values use the STORE button. Use the RECEIVE button for reading back the stored values and the SEND button for updating the microcontroller with the values in the GUI.

4.7.1 Status and faults

The status and faults panel is in the upper right-hand side of the GUI. Possible condition flags appear in faded gray. Flags will be highlighted if the condition applies.

Possible conditions are:

- ENABLED: If you use the OFF button a disable command is sent and the converter will stop (if running) and will not start even at the nominal input voltage range. Using the ON button means the ENABLED flag is highlighted again and the converter will run normally. The converter is enabled by default
- SOFT-START: The converter runs the soft-start sequence
- BURST: The converter is in burst mode
- SYNC_M1: The synchronous rectifiers are in DCM mode (see 4.4.2)
- SYNC_M2: The synchronous rectifiers are activated and in normal mode 2 (see 4.4.3)
- SYNC_DIODES: The synchronous rectifiers are deactivated (see 4.4.1)

- OFF: The converter is off because a fault happened or because it was requested by the GUI. The converter will not run until the fault is removed or an ON command is requested
- HICCUP: The converter is in HICCUP mode (see 4.6.1)
- SOFT-START FAIL: A soft-start failure happened
- UV/OV: The output voltage has risen above or decreased below the valid range after reaching the regulation window (see 4.6.5)
- FAN FAIL: The signal from the fan tachometer is missing (see 4.6.6)
- OVERTEMP: Overtemperature detected. The converter is latched
- TEMP. WARNING: The temperature of the converter is rising over the nominal conditions but the converter will keep running

Note: The flags under STATUS are indicating different running modes. The flags under FAULTS indicate that the converter is switched OFF because of any of the faulty conditions.

4.7.2 Output voltage reference

This parameter adjusts the nominal output voltage of the converter (Figure 59). The parameter is in units of ADC sampled values in the range of 14 bits ([0, 16384]).

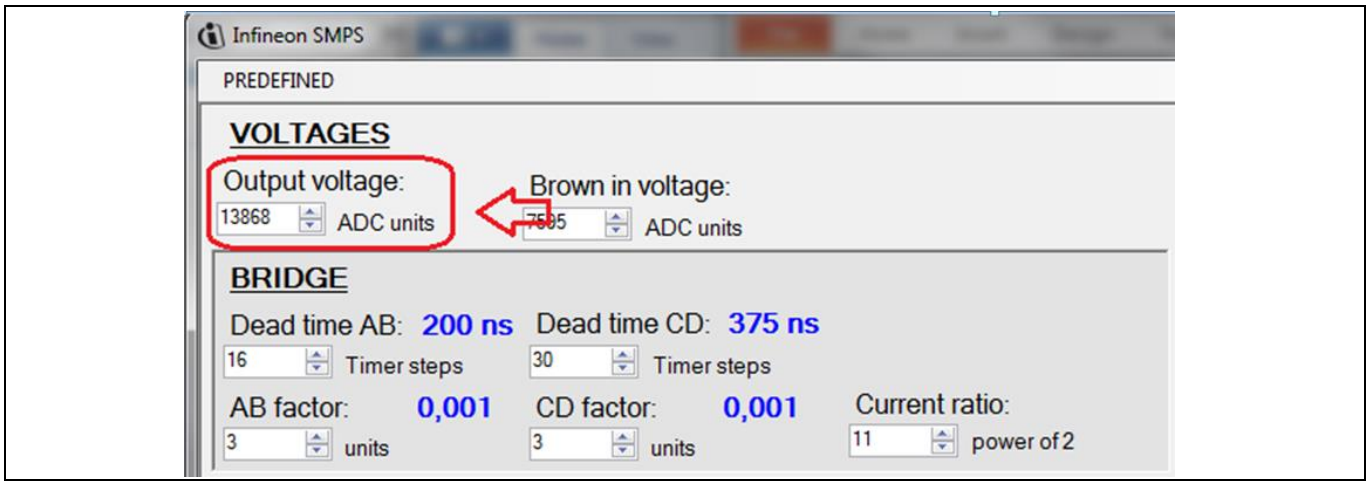

Figure 59 Output voltage nominal value

If the output voltage of the converter is not 12 V, adjust the parameter using the equation (25).

$$OUT_{newADC} = \frac{OUT_{presentADC}}{OUT_{newVoltage}} * OUT_{newVoltage} \quad (25)$$

4.7.3 Brown-in voltage

This parameter sets the brown-in voltage of the converter. The parameter is in the units of ADC-sampled values in the range of 14 bits ([0, 16384]).

If the converter starts up at a different voltage than 350 V, adjust the parameter using the equation (26).

$$BROWN\_IN_{newADC} = \frac{BROWN\_IN_{presentADC}}{BROWN\_IN_{currentVoltage}} * BROWN\_IN_{newVoltage} \quad (26)$$

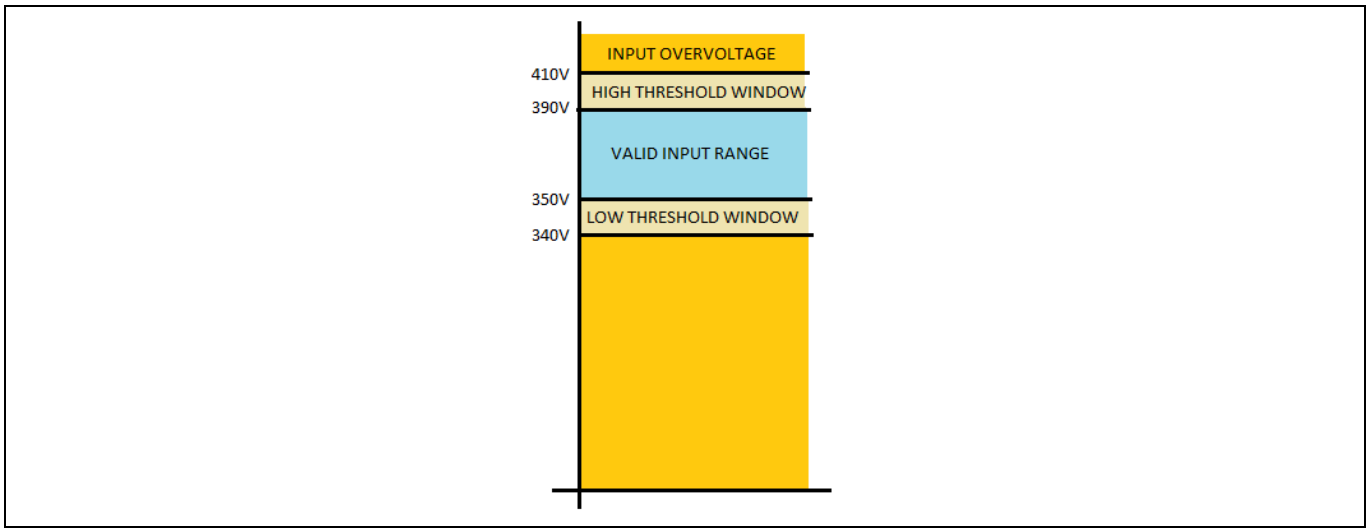

Figure 60 Input voltage range protection

The other input voltage thresholds are calculated by the controller based on the 350 V base level (Figure 60).

4.7.4 Bridge dead times

Dead time settings for each of the legs in the bridge can be adjusted independently and on the fly.

The granularity of the values comes from the microcontroller timer clock period, in this case 12.5 ns. The minimum possible value is five steps, and the maximum is 255 steps.

Optimum dead times vary depending on load and input voltage. The relation can be approximated by a linear formula with the two parameters I_{factor} and I_{ratio}.

$$dt = dt_{nominal} - I_{in} * \frac{I_{factor}}{2^{I_{ratio}}} \quad (27)$$

The leading and lagging leg transitions have different behavior. The leading leg has a resonant transition, with low variation of dead time along the load, and the lagging leg has a quasi-linear transition, much dependent on the load. Separate dead time, factor, and ratio can be adjusted for each of the legs.

4.7.5 Synchronous rectifiers

On-delay (Figure 61) is the time added from the rising edge of A or B (start of the power transfer) and the rising edge of the gate of the corresponding synchronous branch.

Off-delay is the time added from the falling edge of C or D (end of the power transfer) and the falling edge of the gate of the corresponding synchronous branch.

Transition times vary with the load of the converter. The dependency can be approximated to a linear equation with two parameters: factor and ratio. The start and end of the power transfer behave differently; different factors and ratios apply for the turn-on and turn-off delay.

$$ON_{delay} = ON_{delay\_nominal} - I_{in} * \frac{I_{factor}}{2^{I_{ratio}}} \quad (28)$$

$$OFF_{delay} = OFF_{delay\_nominal} - I_{in} * \frac{I_{factor}}{2^{I_{ratio}}} \quad (29)$$

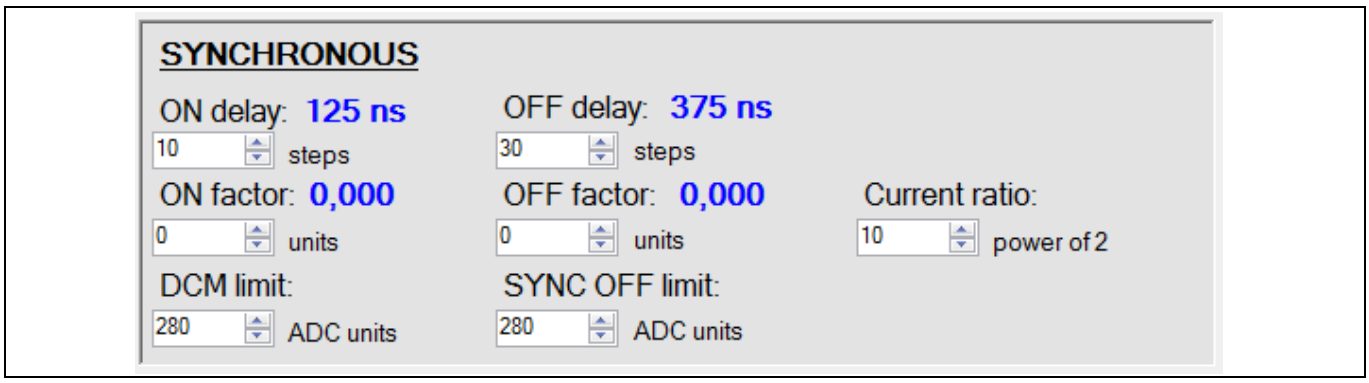

Figure 61 Delay of synchronous gate rising edge after drain voltage falling edge

There are several synchronous driving schemes (see 4.4) valid for different running conditions: DCM limit is the threshold for mode 2, the SYNC OFF limit is the threshold for mode 1, and below the SYNC OFF limit the synchronous MOSFETs are deactivated and behave as pure diodes (mode 0).

Note: The hysteresis window for the different modes is hard-coded into the firmware.

Values of the limit parameters SYNC OFF and DCM account for average input current, in the range of 14 bits ([0, 16384]).

4.7.6 Burst mode thresholds

The burst driving scheme further improves efficiency under light-load or no-load conditions at the expense of increased output ripple (see 4.5).

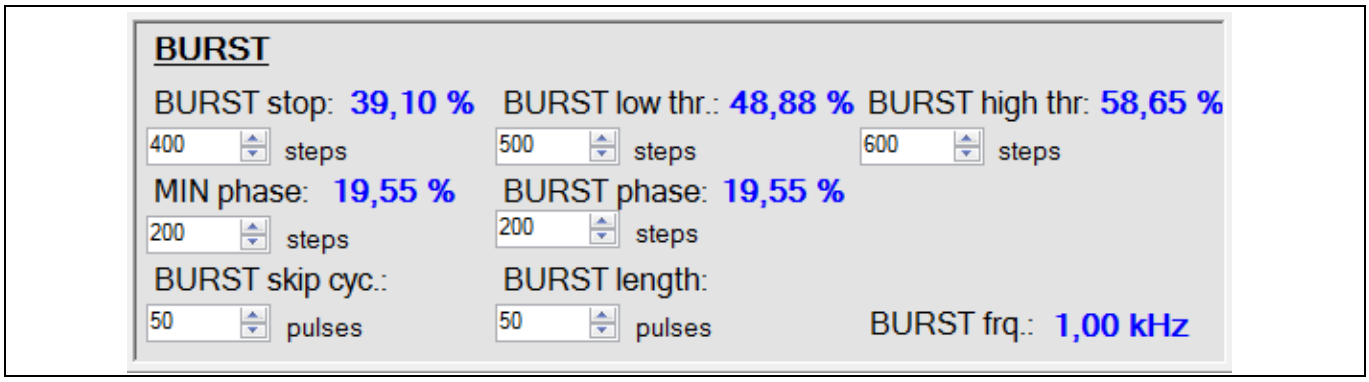

Figure 62 Burst mode thresholds

The different parameters, described in 4.5, determine how the burst scheme behaves: output ripple, burst frequencies, audible noise.

4.7.7 Protections

Some protections can be deactivated for debugging purposes or special testing cases. The protections deactivating panel is on the right-hand side of the GUI (see Figure 63).

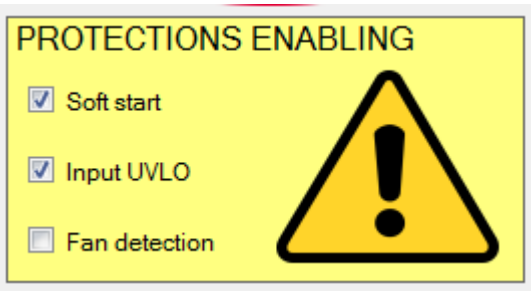

Figure 63 Soft-start protection enabling

Note: Clicking in the check boxes sends the new configuration to the microcontroller, but for the change to be effective after a power recycle use the STORE button.

The soft-start check box deactivates the soft-start sequence time-out protections. The converter can be operated out of nominal conditions, starting from low input voltages and increasing progressively.

The UVLO check box deactivates the input voltage out-of-range protections. The converter will operate at any input conditions.

The fan detection check box deactivates the fan tachometer detection. Fan modulation control is still active, but there is no detection of a broken rotor (temperature protection is always active).

4.7.8 Storage of parameters in Flash

XMC42 on-chip Flash memory can be used as permanent storage. Firmware itself has writing and reading access to the Flash memory, which makes the use of an external Electrically Erasable Programmable Read-Only Memory (EEPROM) unnecessary.

Areas of the memory can be reserved for this special purpose. Firmware can be updated and the reserved sections will remain unmodified.

The parameters can be written or read through the communication interface (UART in this case), under the control of the firmware in the microcontroller, or through the programming interface in a mass-production use case.

4.7.9 LEDs on the daughter card

Three LEDs are mounted on the control card to provide status information for the converter and control card.

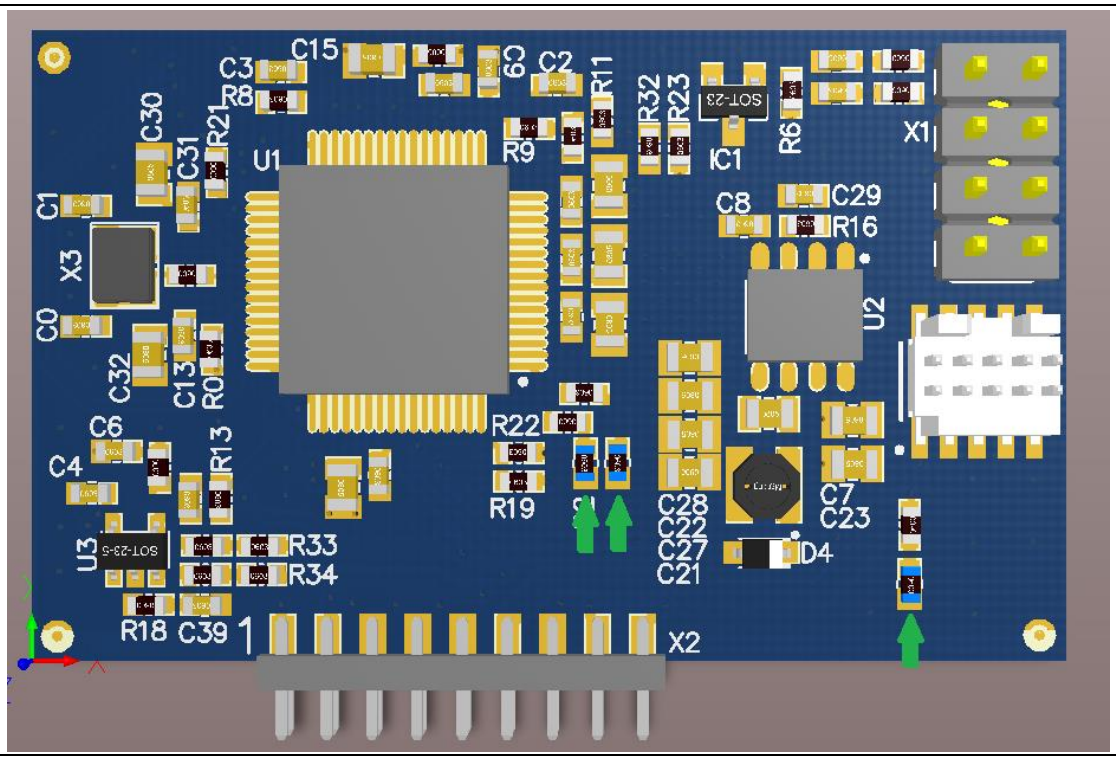

Figure 64 Control card on-board LEDs (green arrows)

The LED in the bottom right-hand corner shows power present in the controller circuitry (3.3 V).

The two other LEDs are used to indicate the status or fault information of the converter. Messages are coded by the color of the LEDs and by a blinking pattern.

- Temperature fault: measured temperature of the converter above the limit. The protection latches the converter. Power has to be recycled to remove latching protections
- Soft-start time-out: over-load during soft-start sequence
- No fan pulses detected: the signal from the tachometer of the fan is missing. If a fan without sensor is used, or the fan is powered externally, deactivate the fan protection (see 4.7.7)
- Output OV/UV: output voltage out of the regulation window after reaching regulation (see 4.6.5)
- Temperature warning: measured temperature of the converter is high. This is not a fault, but status information
- Running with no faults: if the converter is running (input voltage in range) and none of the other conditions apply
- Brown-out: none of the other conditions apply, and the input voltage is out of range

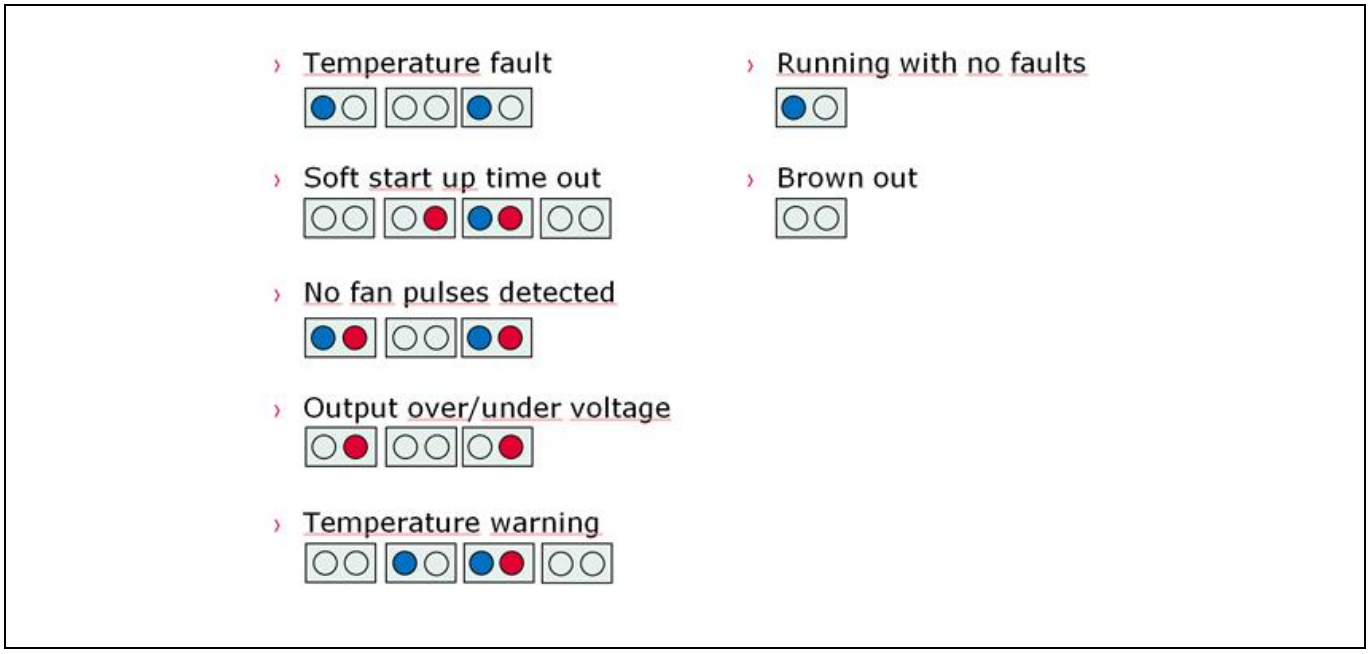

Figure 65 **A square frame represents one of the states of the sequence. A blue dot means a blue LED is lit. A red dot means a red LED is lit. Sequence states are changing at 2 Hz**

5 Performance evaluation

5.1 Primary MOSFETs ZVS

The waveforms are captured with reference to the nomenclature used in the section 2.1.1 “Principle of operation”.

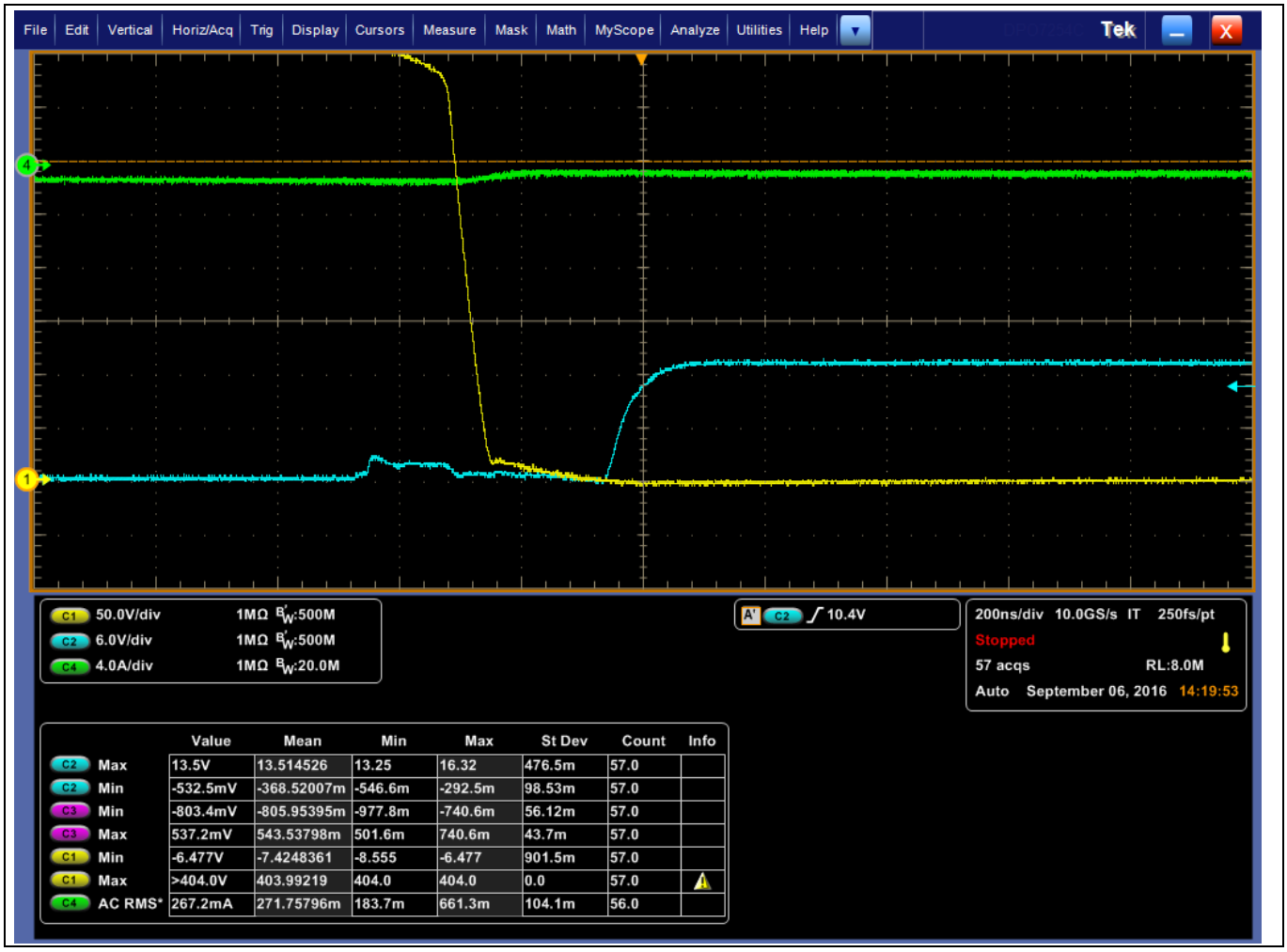

Figure 66 Lagging leg achieves ZVS at 16 A. Waveforms captured on MOSFET D: primary current (green), drain voltage (yellow) and gate voltage (blue)

Figure 65 shows the turn-on of the low side MOSFET in the lagging leg (D) at the minimum load current needed to achieve ZVS. This corresponds to around 24% of full load, as in the original design target. ZVS behavior is as usual clearly recognized by the absence of the Miller Plateau in the V_{GS} waveform.

Figure 66 shows the turn-on of the low side MOSFET in the leading leg (B) at the minimum load current needed to achieve ZVS, which corresponds to around 89% of full load, also as in the original design target. This target is fixed as the best trade-off between the efficiency target under light load (in our case dictated by 80+ Platinum standard) and the amount of resonant inductance needed, which may have some impact on the mid- and full-load efficiency, due to copper losses in the windings. In any case the resonant tank design and the related dead-time settings are optimized for the IPA60R280CFD7 device.

The technology CFD7 allows a very convenient selection of these design parameters, due to its intrinsic benefits with regard to ZVS operation, as already explained in paragraphs 1.1 and 1.2 of the present document.

Figure 67 **Leading leg achieves ZVS at 60 A. Waveforms captured on MOSFET B: primary current (green), drain voltage (yellow) and gate voltage (blue)**

5.2 Synchronous Rectification (SR) MOSFETs operation

5.2.1 Synchronous MOSFET driving schemes

There are three driving schemes for the synchronous MOSFETs in the PSFB 800 W controller (see 4.4).

Under light load, no load, during burst and during soft-start sequence the synchronous MOSFETs are not driven. The body-diode of the device conducts all the current (Figure 68).

Under light load, when the output current ripple is greater than the average output current, the synchronous MOSFETs are driven only during the primary to secondary power transfer (Figure 69).

For any other conditions than those listed, synchronous MOSFETs are driven to always conduct through the device channel. Short body-diode conduction time cannot be avoided during turn-on and turn-off transitions (Figure 70).

The driving is always selected with the goal of allowing the body-diode to conduct as little current as possible in order to preserve efficiency and prevent unwanted voltage overshoot in the SR MOSFETs.

Also, in this case the best trade-off design is achieved.

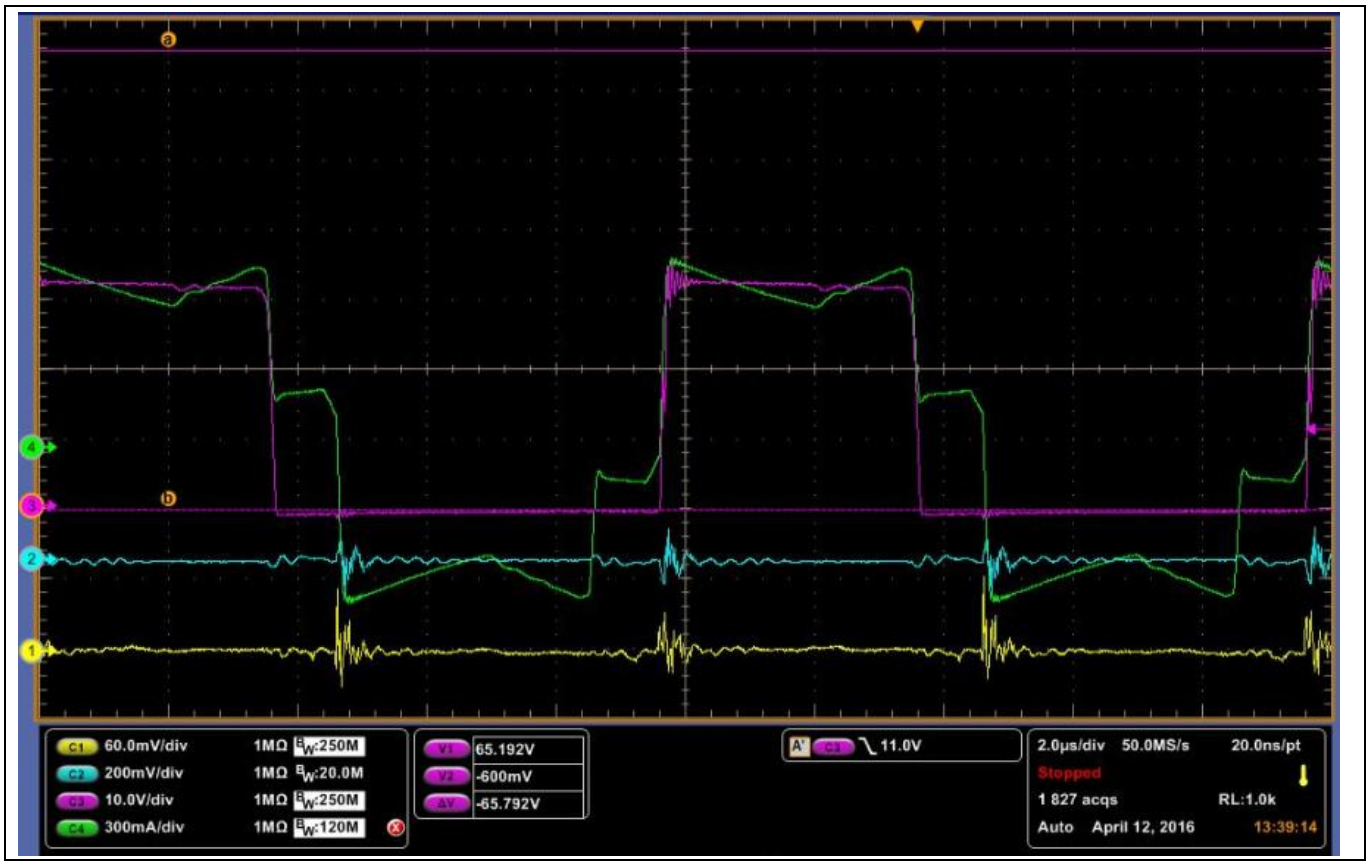

Figure 68 Synchronous mode 0 driving scheme: primary current (green), drain voltage (purple), gate voltage (yellow)

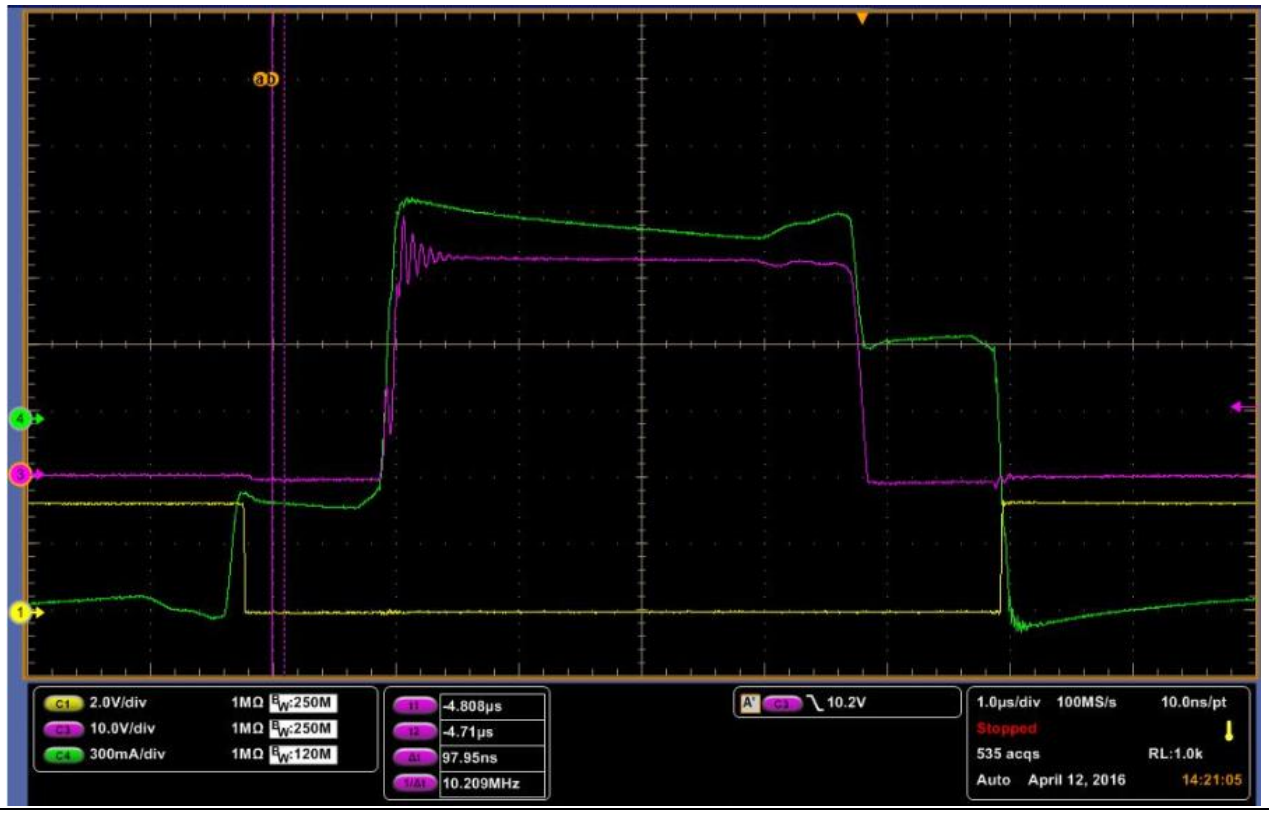

Figure 69 **Synchronous mode 1 driving scheme: primary current (green), drain voltage (purple) and gate voltage (yellow)**

Figure 70 **Synchronous mode 2 driving scheme: primary current (green), drain voltage (purple), gate voltage (yellow)**

5.2.2 Synchronous MOSFETs dead time

In the second driving scheme (see 4.4.3) body-diode conduction is kept to a minimum, but still maintaining a safety margin so as not to overlap the drain voltage and an active channel.

During turn-off transition of the synchronous MOSFETs, the rise of the voltage in the drain is delayed as a function of the load and the input voltage of the converter (the time it takes for the primary-side current to reverse direction). The controller implements a linear approximation of the relation, which can be parametrized to keep the turn-off margin constant at different loads (Figure 71 and Figure 72).

One can appreciate that under any load condition the peak voltage is well below the 80% of the MOSFET voltage rating (80*0.8 = 64 V), according to the typical derating guidelines applied in the SMPS design: this contributes to optimizing the so-called mean time between failures (MTBF), an important index of the SMPS reliability.

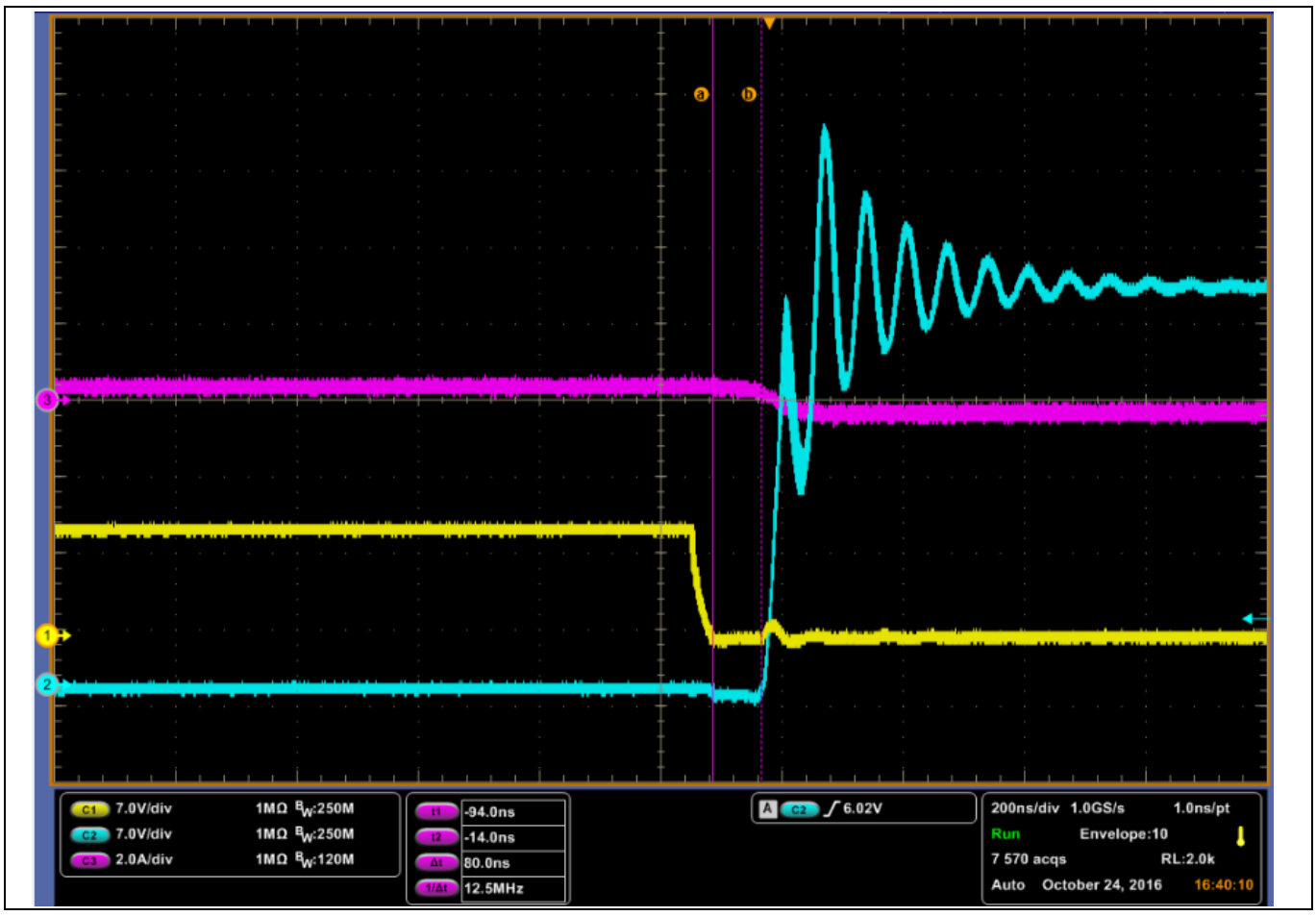

Figure 71 Synchronous turn-off delay @ 10 A load: primary current (purple), drain voltage (blue) and gate voltage (yellow)

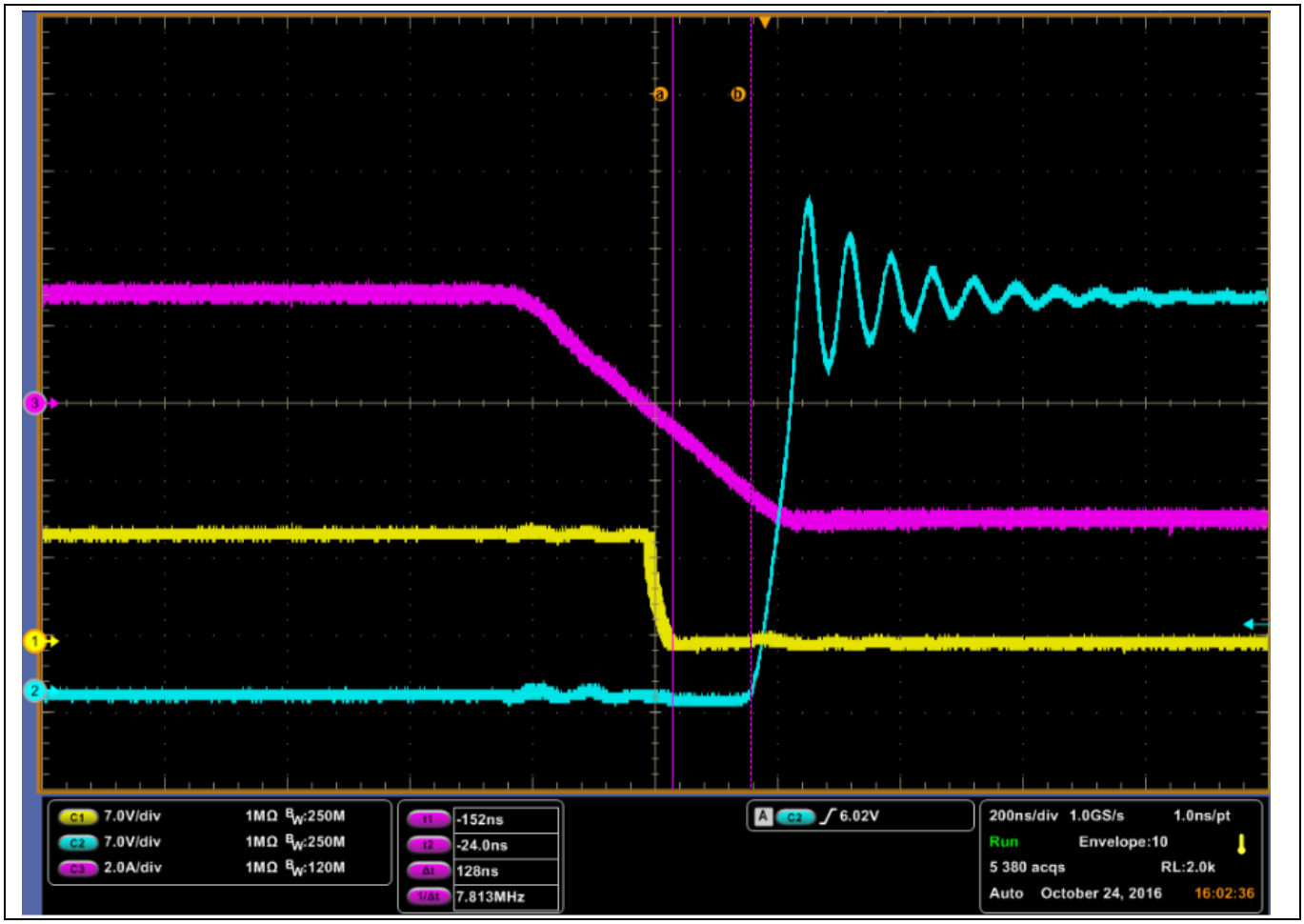

Figure 72 Synchronous turn-off delay @ 67 A load: primary current (purple), drain voltage (blue) and gate voltage (yellow)

The turn-on transition delay is also influenced by the load and input voltage of the converter, but because of the time for the lagging leg bridge transition. During the turn-on dead time, most of the current is conducted by the other branch, and timing is not as critical as for the turn-off transition (Figure 73 and Figure 74).

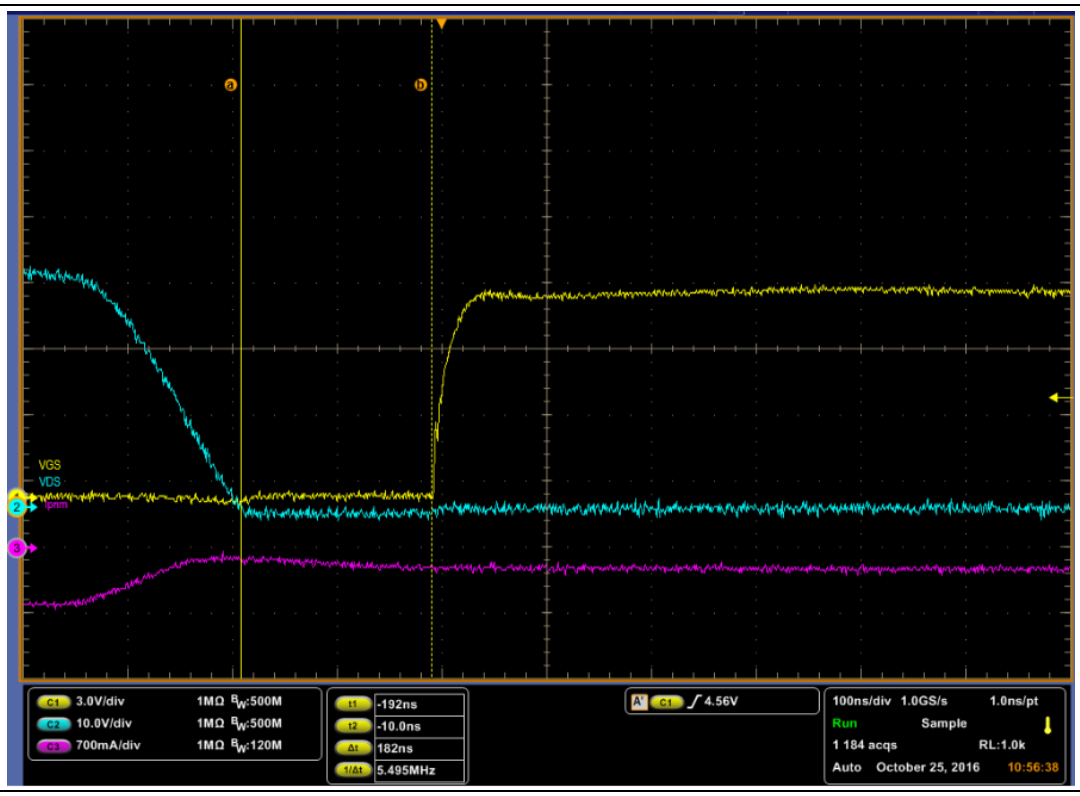

Figure 73 **Synchronous turn-on delay @ 10 A load: primary current (purple), drain voltage (blue) and gate voltage (yellow)**

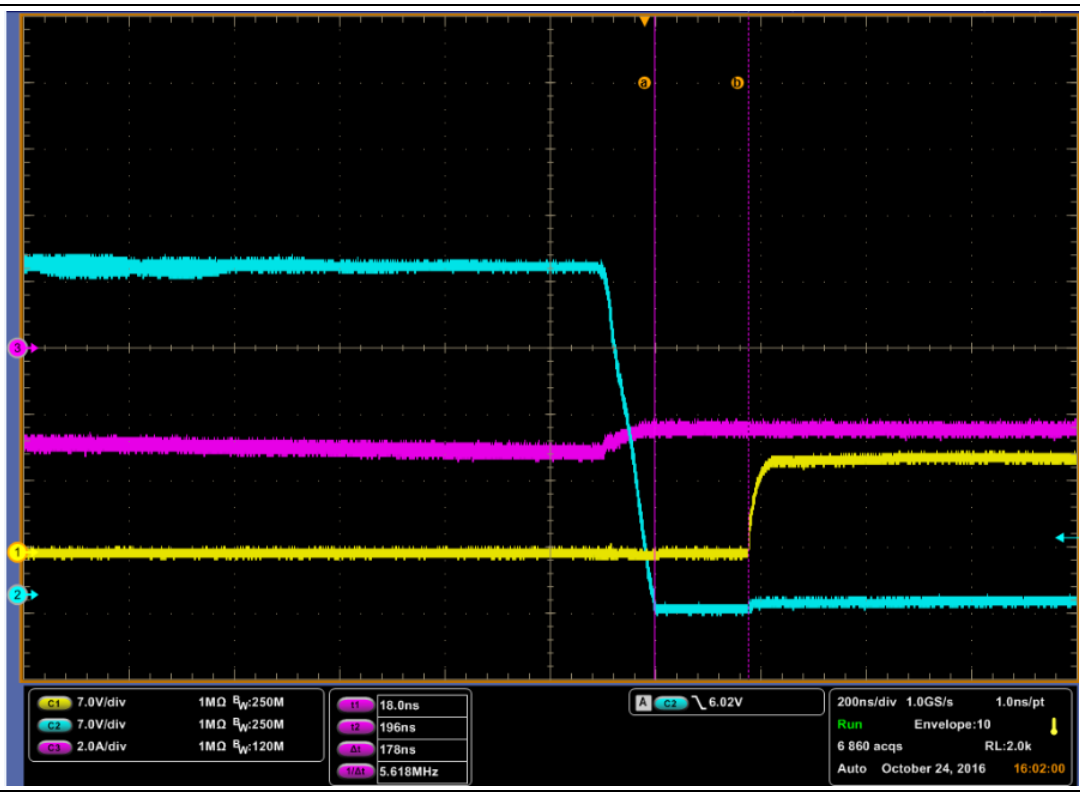

Figure 74 **Synchronous turn-on delay @ 67 A load: primary current (purple), drain voltage (blue) and gate voltage (yellow)**

5.3 Short-circuit protection

A very important protection in a ZVS PSFB converter is the one against output short-circuit. This is because historically there has been trouble in this condition, as already mentioned in introductory paragraph 2.1.

For that reason the waveforms captured during this condition are particularly relevant.

Figures 75 and 76 represent short-circuit under no-load and full-load conditions. Figure 77 analyses in detail the primary current behavior during this occurrence, and shows that the MOSFET_V_{DS} remains well below the rated voltage during this abnormal condition, to guarantee reliable operation.

Figure 75 Short-circuit under no-load at output: primary current (green), output voltage (purple)

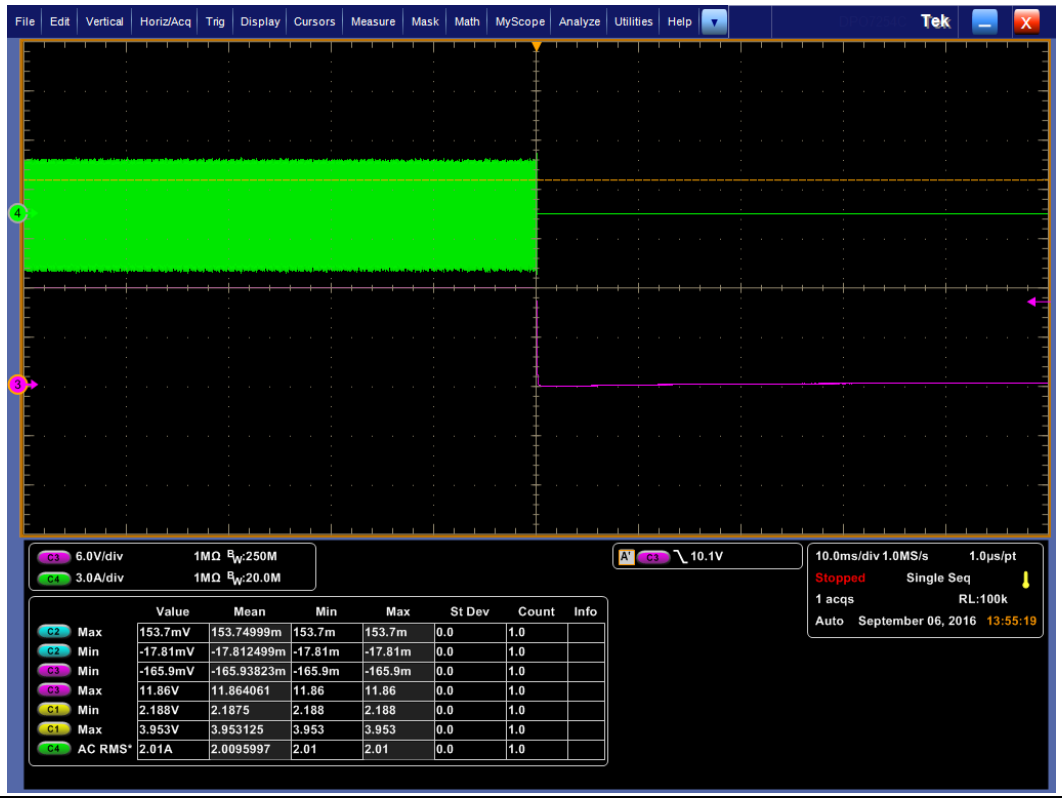

Figure 76 **Short-circuit under full load at output: primary current (green), output voltage (purple)**

Figure 77 **Short-circuit under full load at output: primary current (yellow), MOSFET_V_{DS} (purple), output voltage (blue)**

5.4 Dynamic loading

Figures 78 and 79 show the typical dynamic-load waveforms according to the converters' spec.

The outcome of those waveforms is that the output over-shoot and under-shoot are always below the specified 400mV$_{pk-pk}$.

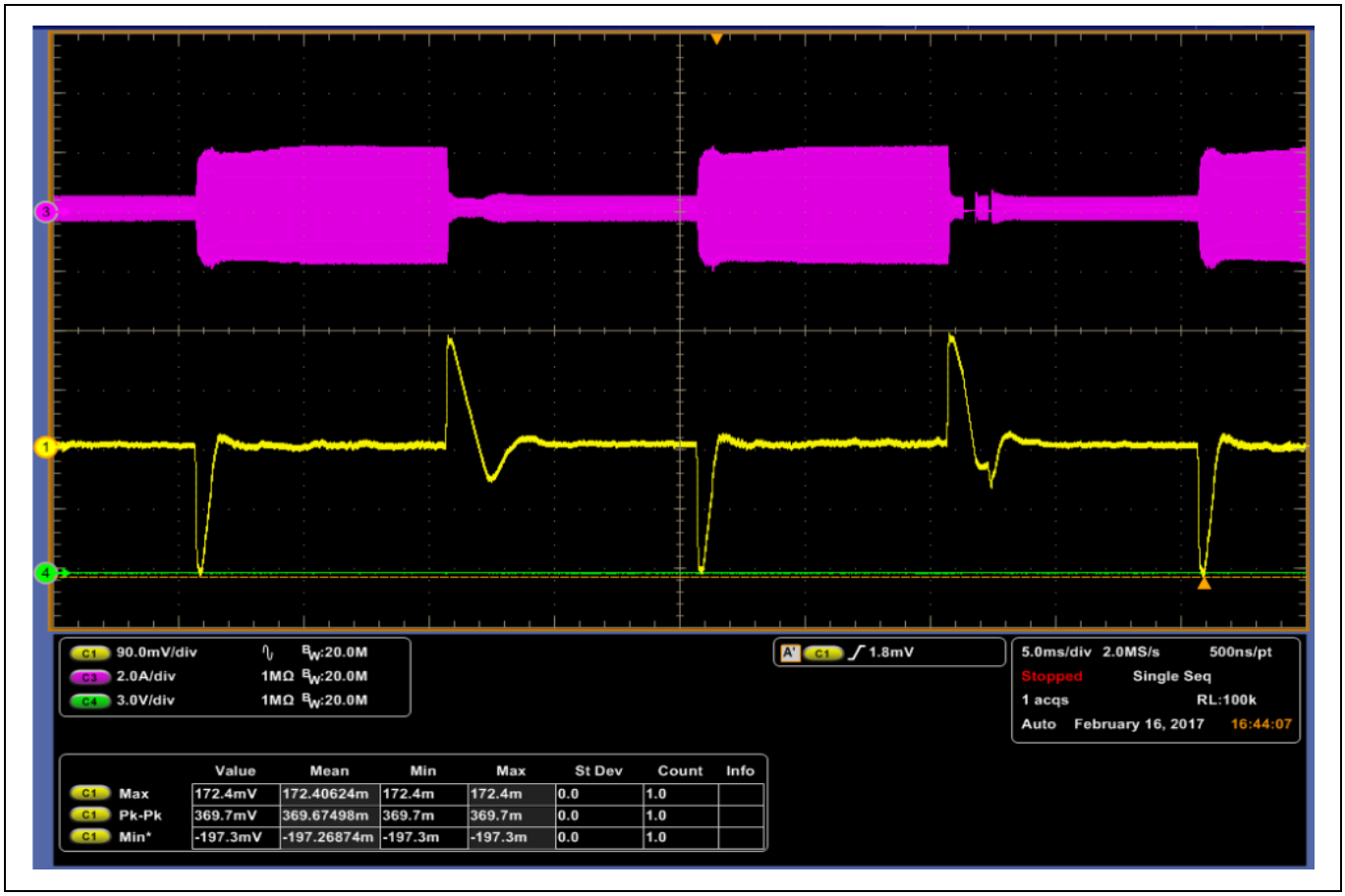

Figure 78 3 A–33.5 A output dynamic load: primary current (purple), output voltage (yellow)

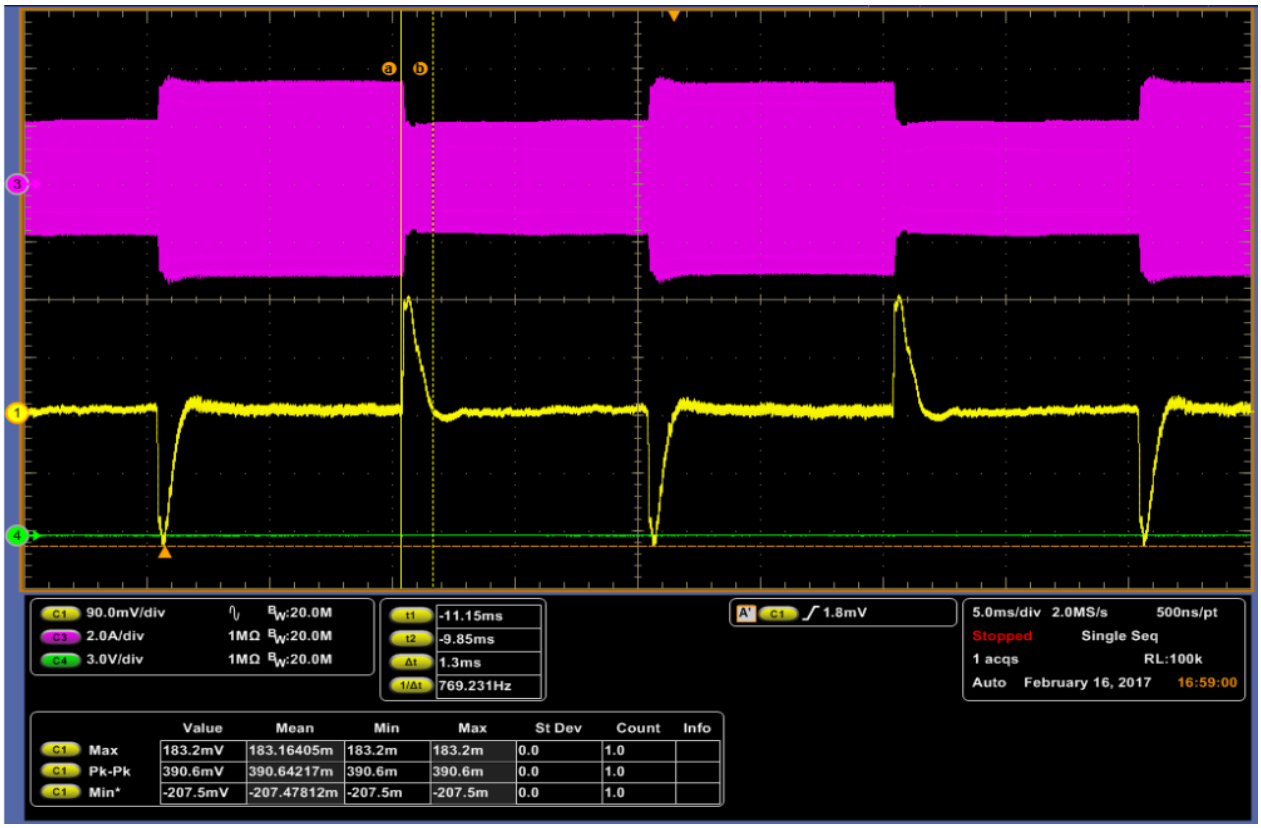

Figure 79 33.5 A–67 A output dynamic load: primary current (purple), output voltage (yellow)

5.5 Efficiency plots

The efficiency plots reported here are measured with a fully automated set-up and following the typical procedures prescribed by the 80+ standard (see [11] for more details).

The plot shown in Figure 80 has been measured including the BIAS absorption, except the power needed for the fan, which is supposed to be supplied by an external source. Of course, the efficiency under light load is strongly influenced by the efficiency of the used auxiliary converter. A further improvement of it is already planned, consisting of the replacement of the BIAS board with a new design, based on the new Infineon CoolSET™ 5 series, as already mentioned in paragraph 3.1.5.1.

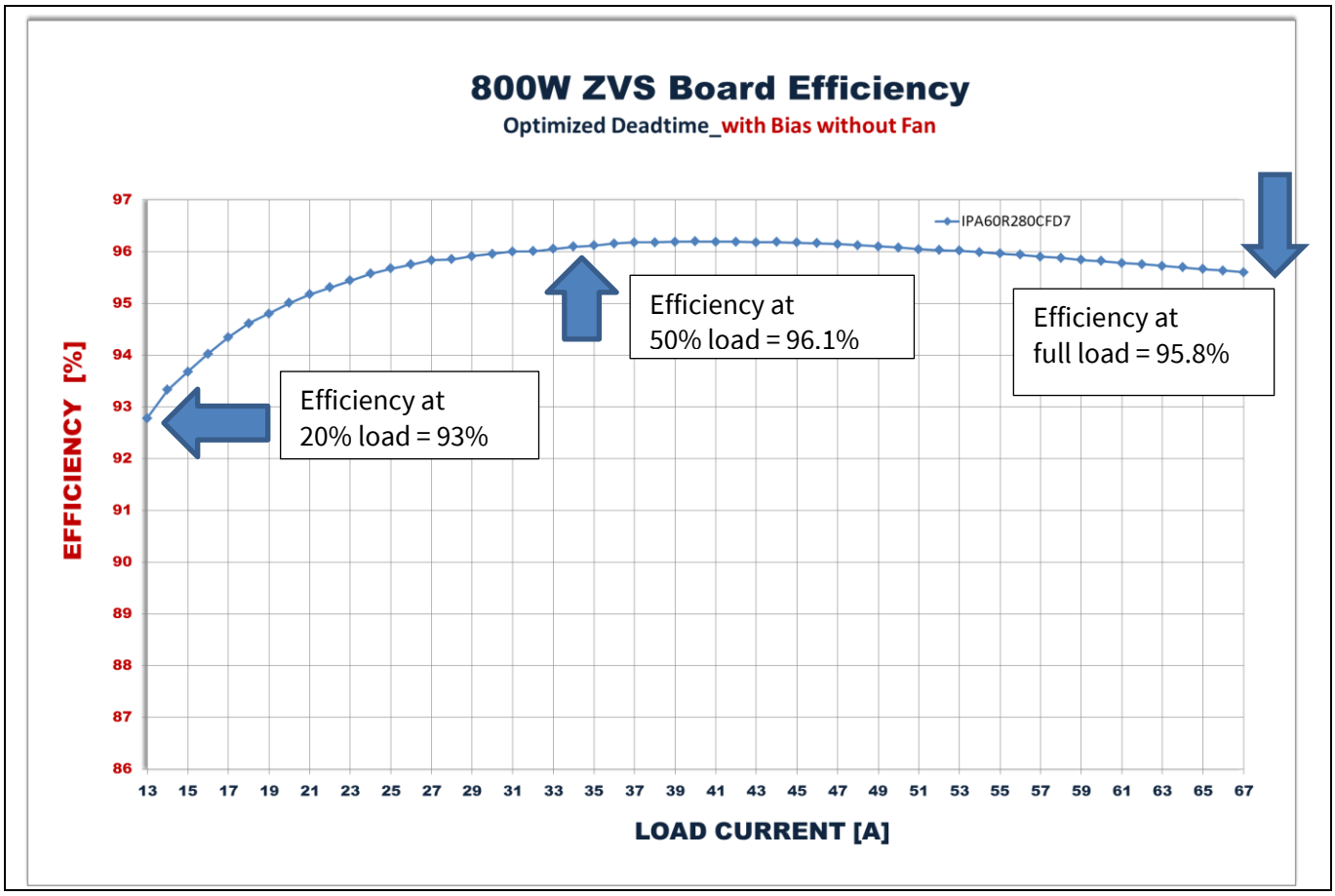

Figure 80 Efficiency plot

Figure 81 shows the efficiency comparison between several MOSFETs in the comparable $R_{DS(ON)}$ range.

The comparison has been performed using the same resonant tank (as in the original design) and by re-setting the dead time for each of the analyzed devices.

At full load, $R_{DS(ON)}$ variation leads to efficiency differentiation, and under light load the E_{oss} is different for DUTs as they are switching at different V_{DS}.

A very impressive result is that at 50% load, IPA60R280CFD7 gives 0.58% better efficiency than Comp T of equivalent $R_{DS(on)}$. This is a very important achievement, because 50% is the most important load condition in server and industrial SMPS applications and the point where standards such as 80+ Platinum require the peak value of the efficiency.

We can conclude that overall IPA60R280CFD7 gives the best performance across the entire load range.

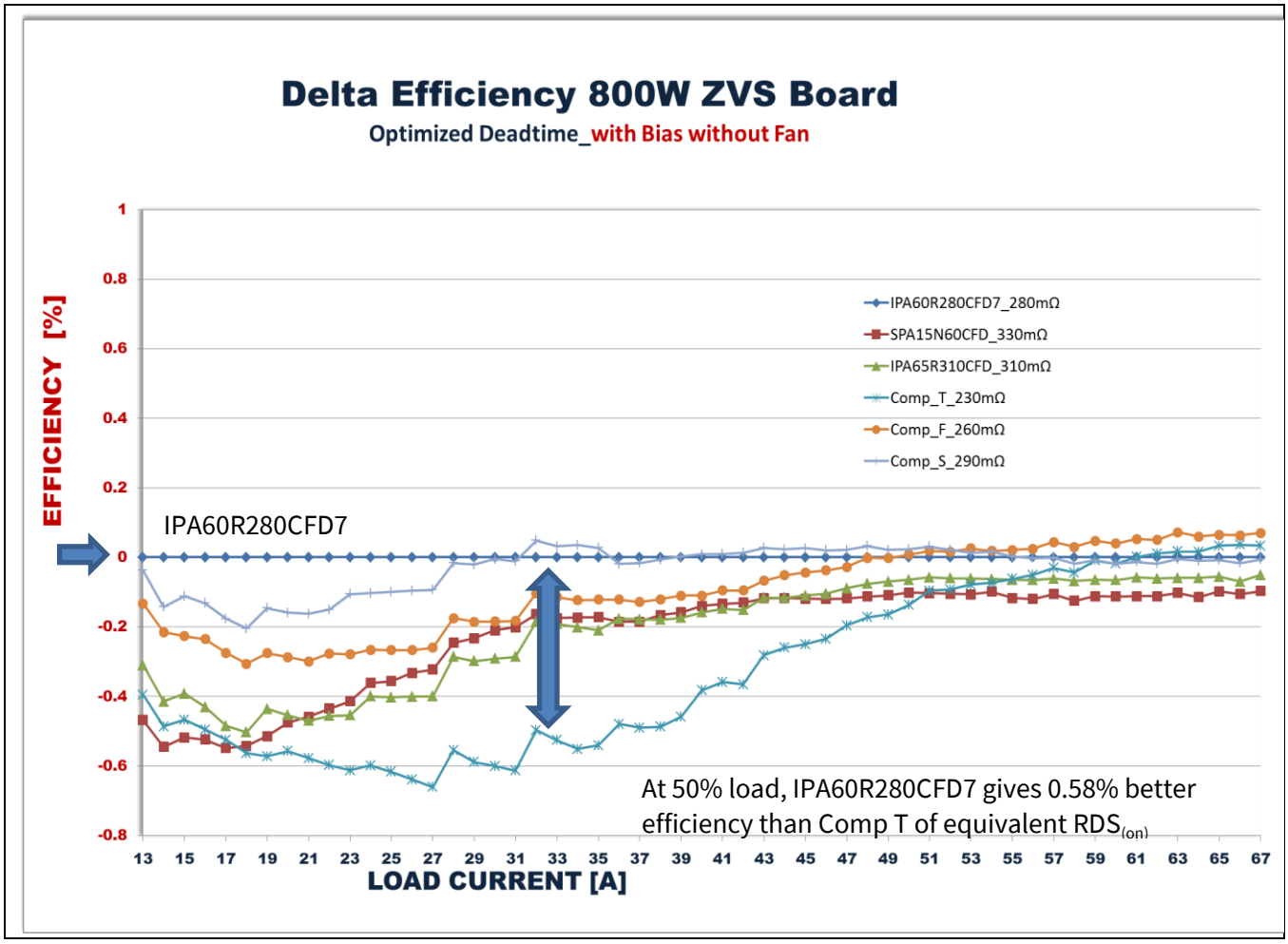

Figure 81 **Efficiency comparisons in 800 W ZVS PSFB evaluation board: CFD7 shows the best performance across the load range**

5.6 Thermal maps

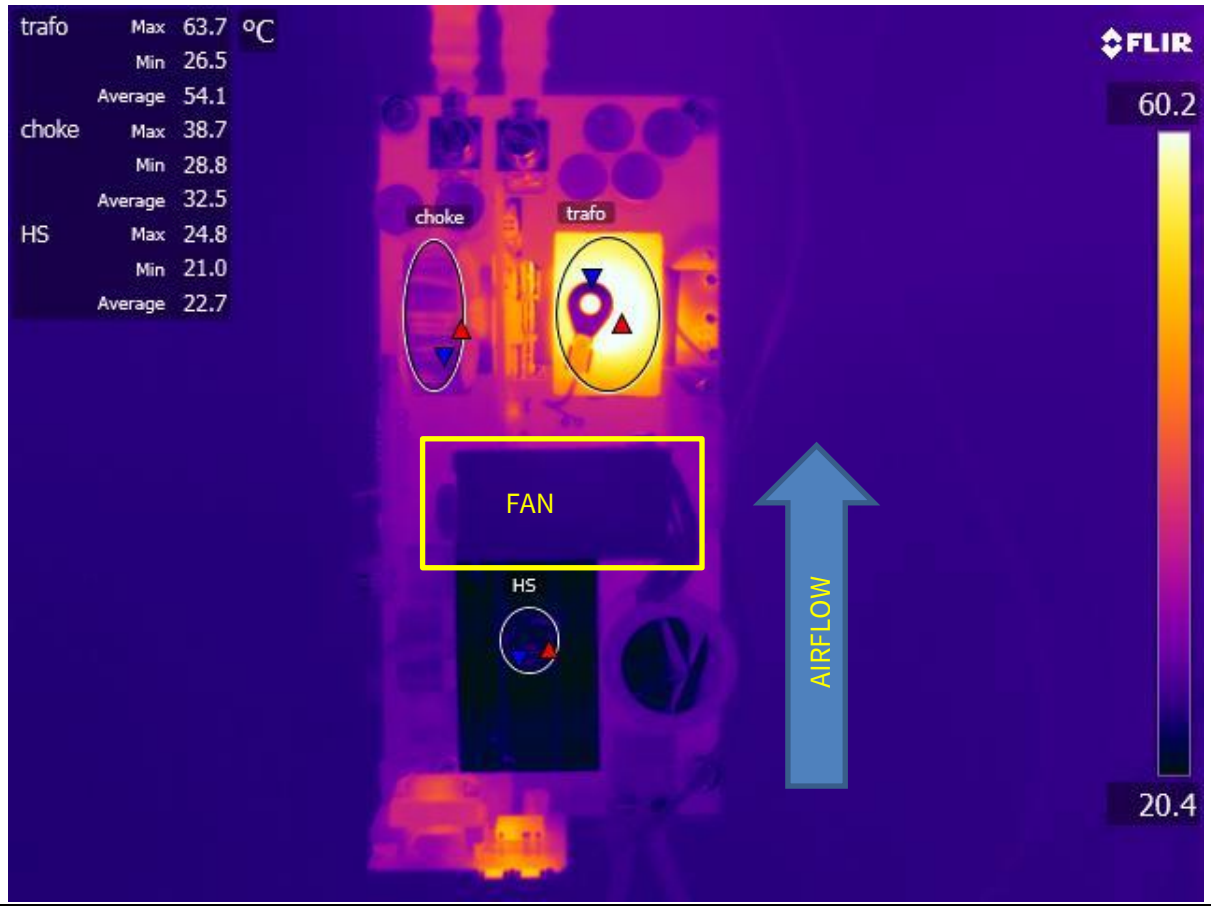

Figure 82 Board thermal map at full load (67 A) at room temperature (~25°C)

Figure 82 shows that the primary full-bridge heatsink stabilizes at around 25°C. This very low temperature is the result of the new CFD7 technology, its efficient driving concept and the cooling applied.

The hotspot on the board is the transformer, at around 65°C. The main losses within the transformer are coming from the secondary copper, as can be seen in the detailed map in Figure 83.

The cooling is specifically designed to optimize the heat dissipation on the transformer, so special care must be given to this aspect in case of translation of the present concept to SMPS applications.

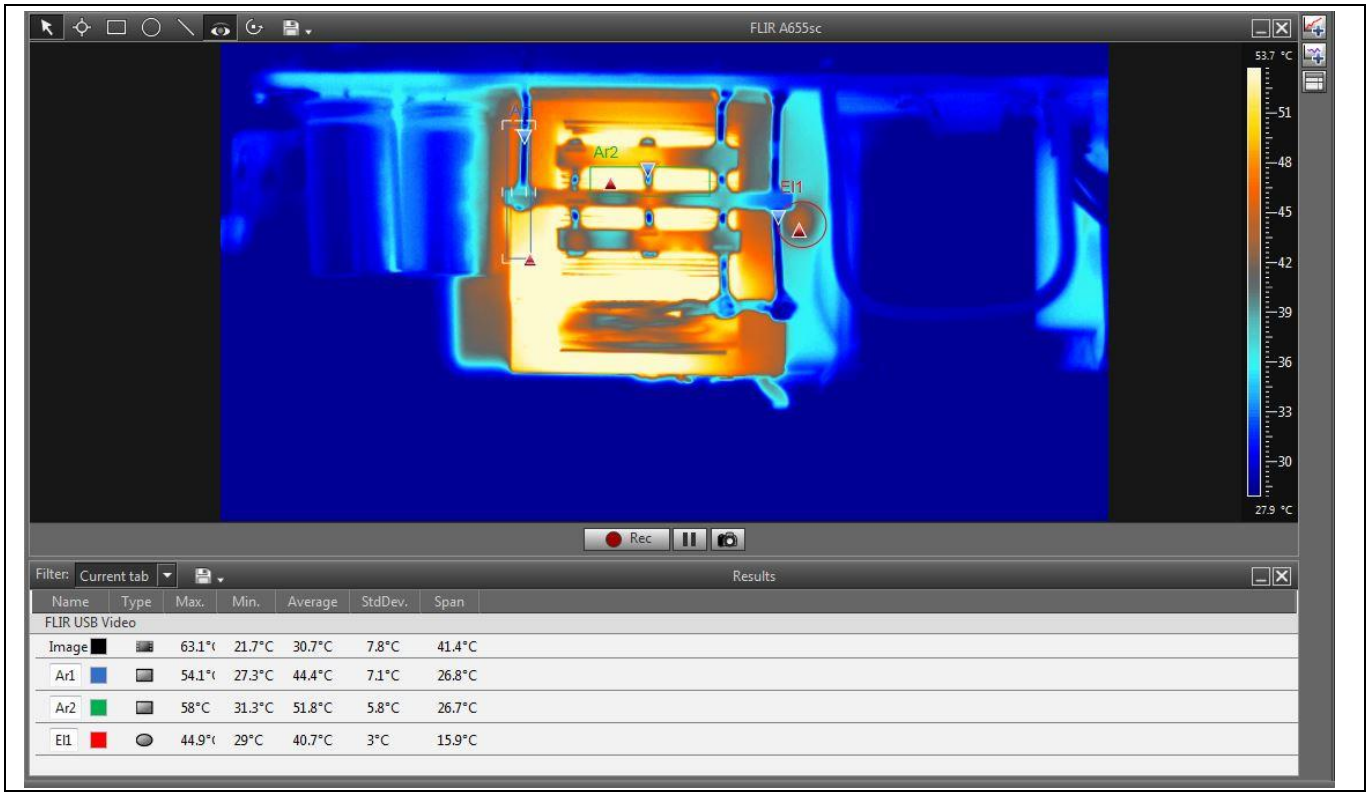

Figure 83 Main transformer detailed thermal map at full load (67 A) at room temperature (~25°C)

6 Conclusion

This document provides an overview of the Infineon 800 W ZVS PSFB demo board based on the new CoolMOS™ CFD7 technology.

The design concept and the performance evaluation are described with special focus on the key contribution of the CFD7 technology to enable high efficiency combined with reliable operation across the whole load range, including the typical critical modes of this topology. In fact the demo board design is optimized for the 280 mΩ 600 V CoolMOS™ CFD7 device, namely IPA60R280CFD7.

An important contribution to the final excellent results also comes out of the applied digital control by Infineon XMC4200. Two possible options, peak current mode and voltage mode, are offered to users for the converter control: these two are in fact the most popular in SMPS application of the PSFB topology. The applied control paths, on both the primary and secondary MOSFETs, with optimized delay time setting, enable an efficiency plot targeting the HV DC-DC stage of an 80+ Platinum level server power supply. A GUI has been designed to help the user interact with the demo board: it enables real-time reading of some key electrical parameters, along with the possibility of designing fine-tuning and protection monitoring.

The planar main transformer with stacked resonant choke helps achieve the high power density of the demo board and minimizes AC and core losses, resulting in high efficiency across the entire load range, along with a perfect heat spread.

The final result is a robust and high-performance design able to fulfill all the general requirements for the HV DC-DC isolated stage of a server or industrial SMPS.

This paper demonstrates that the ZVS PSFB topology is a valuable alternative to the LLC topology in addressing the 80+ Platinum standard. A proper power devices selection, both in the primary and secondary side, and an appropriate control enable a good balance of performance, cost and reliability, avoiding all the pitfalls of a fully resonant approach, as in the LLC topology.

Further developments of the present design are already planned at Infineon.

The first derivative is a 1400 W version in the same form factor, which means with almost 80% increased power density compared to the 800 W version. 800 W and 1400 W will cover two typical power ranges used today in the server SMPS arena.

The 800 W ZVS PSFB demo board is also suitable for combining with the 800 W CCM PFC Infineon demo board [15] in order to provide an example of complete server SMPS achieving 80+ Platinum efficiency levels.

A way to improve the efficiency further, especially under light load conditions, is to replace the BIAS board with a new one based on the latest Infineon CoolSET™ ICE5QSAG controller and 800 V CoolMOS™ P7 MOSFET IPU80R4K5P7.

Finally, the gate-driving concept used for the HV MOSFETs on the primary side is also going to be improved thanks to the upcoming Infineon 2EDS family of driver ICs with reinforced isolation: this will enable replacement of the gate drive transformers and will provide a reliable and efficient solution with an even smaller form factor.

7 Technical data package (TDP)

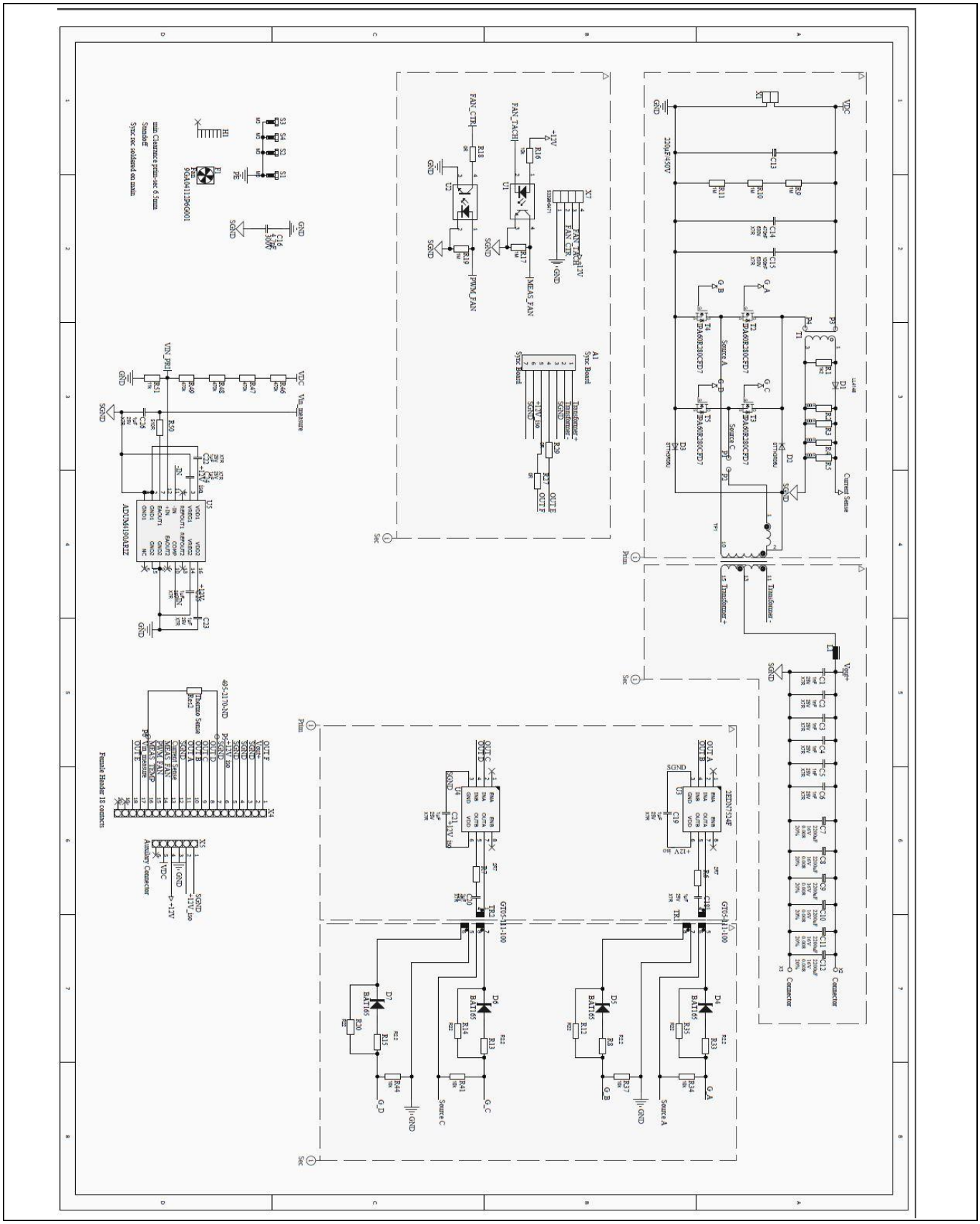

Figure 84 Schematic of main board

Table 1 BOM main board

Quantity	Designator	Comment	Value	Tolerance	Voltage	Footprint	Type	Supplier 1
6	C1, C2, C3, C4, C5, C6	SMT	1 nF		25 V	CAP1206R	Ceramic capacitor	Farnell
6	C7, C8, C9, C10, C11, C12	THT	2200 uF	20%	16 V	C_Aluminium electrolite 10 mm V2	Electrolytic capacitor	Digi-Key
1	C13	THT	220 µF		450 V	C_Aluminium electrolite 10 mm V4	Polarized capacitor	Digi-Key
1	C14	THT	470 nF		630 V	C_Foil capacitor 10 mm grid V3	Ceramic capacitor	Farnell
1	C15	SMD	100 nF		630 V	CAP1812R	Ceramic capacitor	Farnell
1	C16	THT	4.7 nF	Y2	300 V	CAP-DISC 7.5 mm lead space	Ceramic capacitor	Farnell
9	C18, C19, C20, C21, C22, C23, C24, C25, C26	SMD	1 µF		25 V	CAP0805R	Ceramic capacitor	
1	D1	SMD	LL4148			DIOMELF3516N-0	Standard diode	Farnell
2	D2, D3	SMD	STTH3R06U			SMB/DO-214AA	Standard diode	Digi-Key
4	D4, D5, D6, D7	SMD	BAT165			S0D250X125X110-2N	Medium power AF Schottky diode	
1	F1	Fan	9GV3612G301			Fan_40 × 40 × 20 mm	Sanyo Denki San Ace fans 9GV3612G301	Farnell
1	H1	Heatsink	0S529			Black anodized heatsink AAVID 0S529	Aavid heatsink S529	Aavid
1	L1	THT	Output choke			Magnetics inductor C058930A2 - V3	Inductor	ICE
1	R1	SMD	1k2	1%		RES1206R	Resistor	
2	R2, R3	SMD	100 R	1%		RES1206R	Resistor	
2	R6, R7	SMD	2R7	1%		RES0805R	Resistor	
4	R8, R13, R15, R33	SMD	2.2 R	1%		RES0805R	Resistor	

Quantity	Designator	Comment	Value	Tolerance	Voltage	Footprint	Type	Supplier 1
3	R9, R10, R11	SMD	1 M	1%		RES1206R	Resistor	
4	R12, R14, R20, R35	SMD	22 R	1%		RES0805R	Resistor	
1	R16	SMD	10 k	1%		RES0805R	Resistor	
2	R17, R19	SMD	1 M	1%		RES0805R	Resistor	
1	R18	SMD	0R	1%		RES0805R	Resistor	
2	R27, R29	SMD	0R	1%		RES1206R	Resistor	
4	R34, R37, R41, R44	SMD	10 k	1%		RES0603R	Resistor	
4	R46, R47, R48, R49	SMD	470 k	1%		RES0805R	Resistor	
1	R50	SMD	510 R	1%		RES0805R	Resistor	
1	R51	SMD	11 k	1%		RES0805R	Resistor	
4	S1, S2, S3, S4	THT	M3			M3	Screw	Farnell
1	T1	THT				Murata Server CS transformer	WE-CST CS transformer	Digi-Key
4	T2, T3, T4, T5	THT	IPA60R280CFD7			TO220_V	n-MOSFET	
1	TF1	THT				Payton transformer		Payton
1	Thermo Sense	THT				AXIAL-0.4	Resistor	Digi-Key
2	TR1, TR2	SMD	GT05-111-100			ICE transformer	Pulse transformer	
2	U1, U2	SMD	VISHAY SFH6186-2			DIL-4-SMD	Optocoupler	Farnell
2	U3, U4	SMD	2EDN7524F			SOIC127P600X175-8N-2	2EDN752x/ 2EDN852x	
1	U5	SMD				SOIC16	ADUM4190ARIZ	Mouser
1	X1	THT				Connector Phoenix Contact 1714955	Pin-header	Digi-Key
5	X5	Auxiliary connector	Bürklin			Bias Supply	Einlötbuchse LB0, 76	25F3020

Quantity	Designator	Comment	Value	Tolerance	Voltage	Footprint	Type	Supplier 1
			25F3020					
1	X7	SMD	53398-0471			Molex picoBlade 4-pins	4-contact pin-header	Farnell
2	X2,X3	THT	Lugsdirect.com B2A-PCB					Lugsdirect.com
4	Heatsink clip							Aavid
4	PCB stand-off	THT					HARWIN R30-1002002 Abstandhalter	Farnell

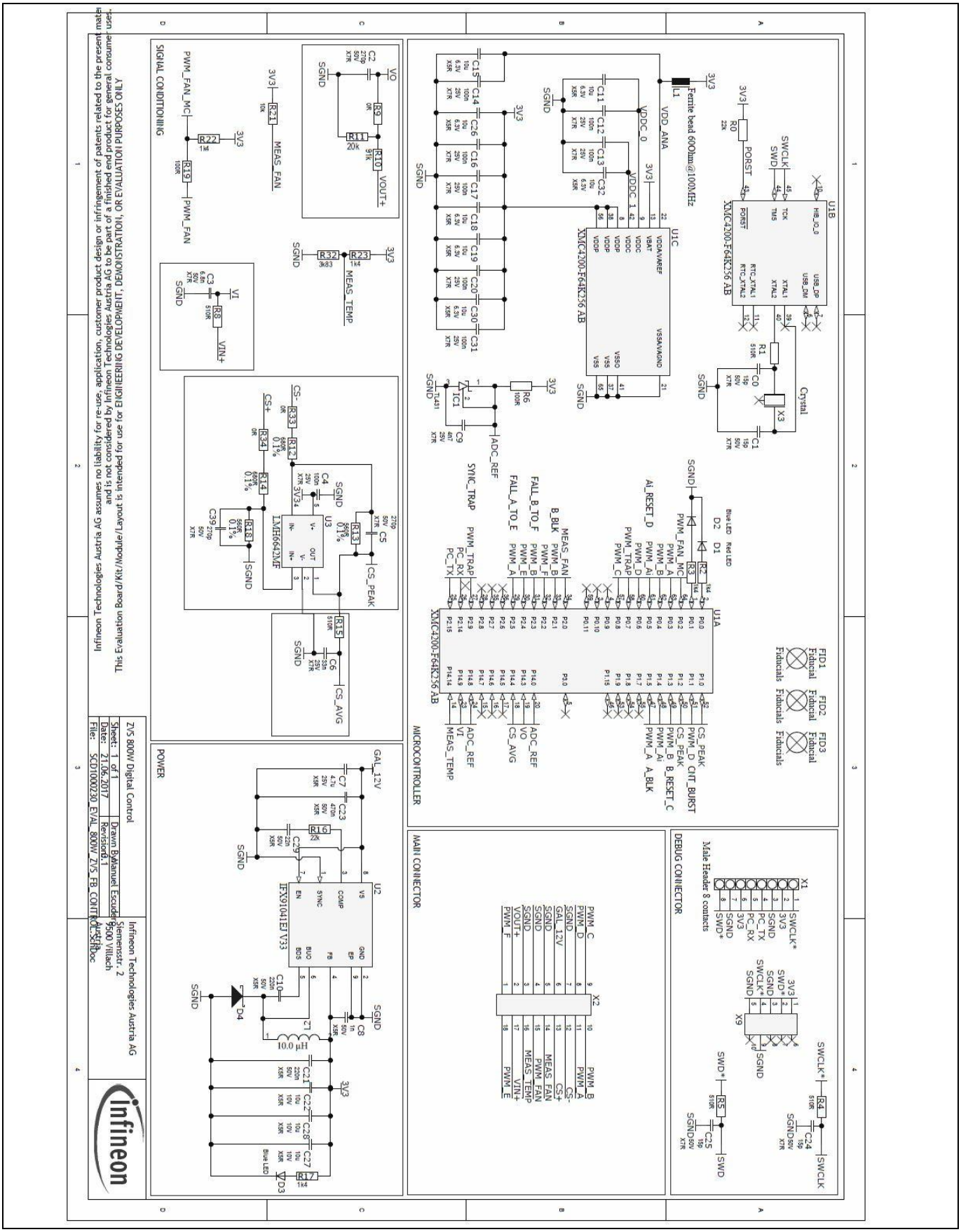

Figure 85 Schematic of digital control board

Table 2 Bill of materials (BOM) control card

Quantity	Designator	Comment	Value	Tolerance	Voltage	Footprint	Type	Part number/ supplier
4	C0, C1, C24, C25	15 p	15 p	X7R	50 V	CAP0603R	Ceramic capacitor	732-7747-1-ND Digi-Key
3	C2, C5, C39	270 p	270 p	X7R	50 V	CAP0603R	Ceramic capacitor	
1	C3	6.8 n	6.8 n	X7R	50 V	CAP0603R	Ceramic capacitor	
8	C4, C12, C13, C14, C16, C17, C20, C31	100 n	100 n	X7R	25 V	CAP0603R	Ceramic capacitor	
1	C6	33 n	33 n	X7R	25 V	CAP0603R	Ceramic capacitor	
1	C7	4.7 u	4.7 u	X5R	25 V	CAP0805R	Ceramic capacitor	8126429 Farnell
1	C8	1 n	1 n	X5R	50 V	CAP0603R	Ceramic capacitor	
1	C9	4n7	4n7	X7R	25 V	CAP0603R	Ceramic capacitor	
2	C10, C21	220 n	220 n	X5R	50 V	CAP0805R	Ceramic capacitor	
10	C11, C15, C18, C19, C22, C26, C27, C28, C30, C32	10 u	10 u	X5R	6.3 V	CAP0805R	Ceramic capacitor	
1	C23	470 n	470 n	X5R	50 V	CAP0805R	Ceramic capacitor	
1	C29	22 n	22 n	X5R	50 V	CAP0603R	Ceramic capacitor	
1	D1	Red LED	Red LED			LED-0603R	LED	1685062 Farnell
2	D2, D3	Blue LED	Blue LED			LED-0603R	LED	1685096 Farnell
1	D4	DO-214-AA/SMB; 2 C-bend leads; body 5.3 × 3.6 mm, inc. leads (L × W)				SOD323	Schottky diode	2432677 Farnell

Quantity	Designator	Comment	Value	Tolerance	Voltage	Footprint	Type	Part number/ supplier
1	IC1	SMD	TL431			SOT23R	IC	296-17328-2-ND Digi-Key
1	L1	Ferrite bead 60 Ω @ 100 MHz	Ferrite bead 60 Ω @ 100 MHz			RES0603R	Inductor	1635704 Farnell
1	L2	10.0 µH				WE-TPC 2828	SMD Shielded Tiny Power Inductor WE-TPC, L=10.0 µH	
2	R0, R16	22 k	22 k	1%		RES0603R	Resistor	
5	R1, R4, R5, R8, R15	510 R	510 R	1%		RES0603R	Resistor	
5	R2, R3, R17, R22, R23	1k4	1k4	1%		RES0603R	Resistor	
1	R6	SMD	100 R	1%		RES0603R	Resistor	
3	R9, R33, R34	0 R	0 R	1%		RES0603R	Resistor	
1	R10	91 k		1%		RES0603R		
1	R11	20 k		1%		RES0603R		
2	R12, R14	680 R	680 R	0.1%		RES0603R	Resistor	
2	R13, R18	560 R	560 R	0.1%		RES0603R	Resistor	
1	R19	100 R	100 R	1%		RES0603R	Resistor	
1	R21	10 k	10 k	1%		RES0603R	Resistor	
1	R32	3k83	3k83	1%		RES0603R	Resistor	

Quantity	Designator	Comment	Value	Tolerance	Voltage	Footprint	Type	Part number/ supplier
1	U1	XMC4200-F64K256 AB	XMC 4200 - F64K 256 AB			INF-PG-LQFP-64-19-5800X5800TP_M	80 MHz XMC4200 MCU with 256 KB program memory, 40 KB SRAM, 3.3 V, -40–125°C, PG-LQFP-64, green	2418736 Farnell
1	U2	IFX91041EJ V33		2(4)%		INF-PG-DSO-8-27_L	1.8 A DC-DC step-down voltage regulator, -40–150°C, PG-DSO-8-27, reel, green	IFX91041EJ V33INTR-ND Digi-Key
1	U3	LMH6642MF	LMH 6642 MF			SOT23-5	LMH664x low-power, 130 MHz, 75 mA rail-to-rail output amplifiers	1468898RL Farnell
1	X1	Male Header 8 contacts				Female double header row 2x4c	TSW-104-06-G-D	Samtec
1	X2					2 mm PCB connector 2x9 - V2	TMM-109-05-T-D	Samtec
1	X3	Crystal	Crystal oscillator			NX3225GD		1253-1151-2-ND Digi-Key
1	X9	SMD				FTSH-105-XX-X-DV-K	2 × 5 pin-header contacts	SAM8799-ND Digi-Key

Synchronous rectification

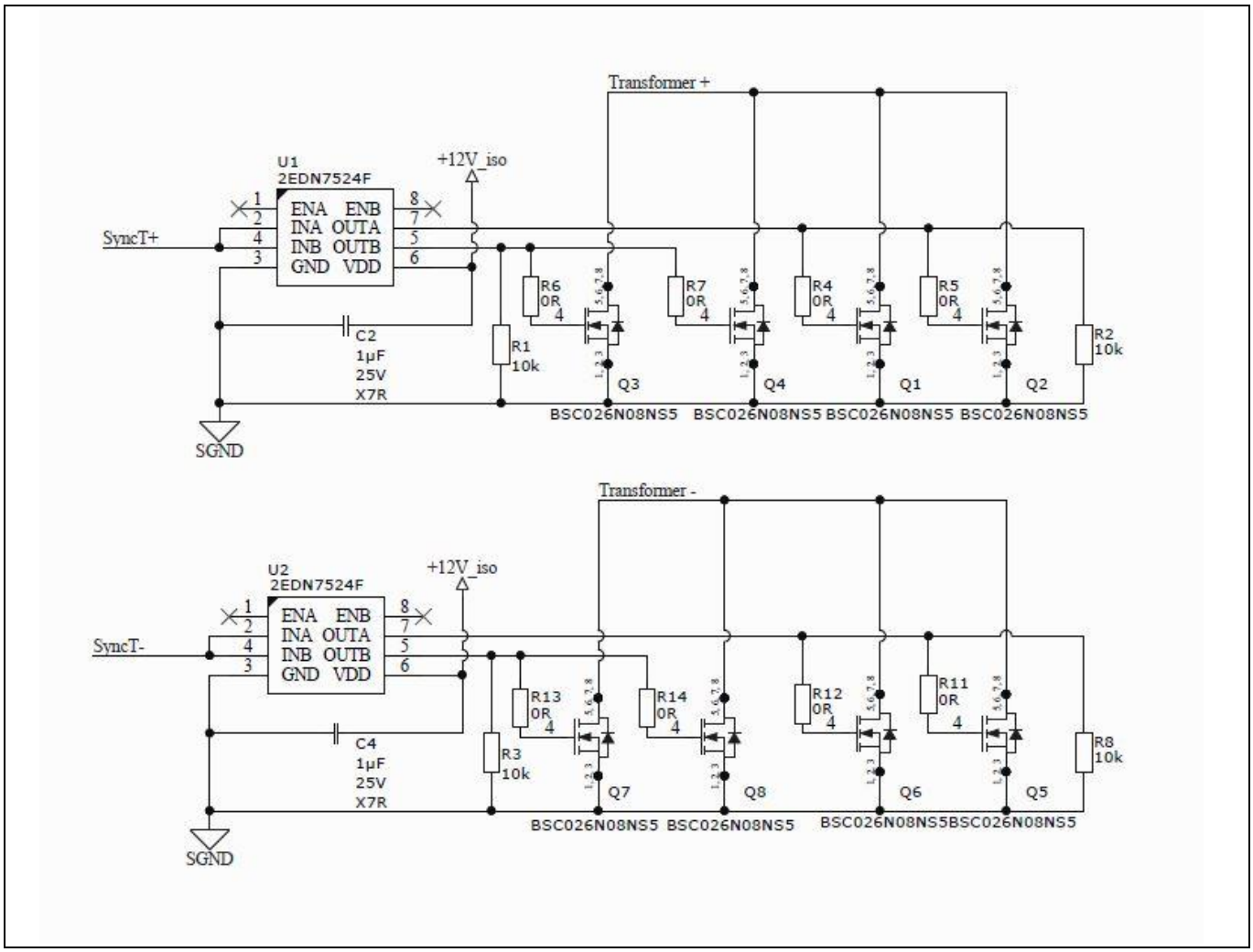

Figure 86 Schematic of synchronous rectification

Table 3 BOM

Quantity	Designator	Comment	Value	Tolerance	Voltage	Footprint	Description
2	C2, C4	Ceramic capacitor	1µF	X7R	25 V	CAP0805R	Ceramic capacitor
8	Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8	BSC026N08 NS5				SuperSO8	OptiMOS™ 3 n-channel power transistor, 40 V VDS, 100 A ID, -55–150°C, PG-TDSON-8-1, reel, green
4	R1, R2, R3, R8	Resistor	10k	5%		RES0805R	Resistor
8	R4, R5, R6, R7, R11, R12, R13, R14	Resistor	0R	5%		RES0805R	Resistor
2	U1, U2	2EDN7524F	2EDN7 524F			SOIC127P60 0X175-8N-2	2EDN752x/2E DN852x

8 Related resources

In the following links, you can find more detailed information about the Infineon devices and magnetic components used.

- Primary HV SJ MOSFETs CoolMOS™ IPA60R280CFD7
- Microcontroller XMC4200
- Advanced dual-channel gate driver 2EDN7524F
- Bias converter controller + switch CoolSET™ ICE3RBR4765JZ
- SR MOSFETs OptiMOS™ BSC026N08NS5
- Planar Magnetics by Payton (main transformer and resonant choke)

Abbreviation and acronyms

Abbreviation	Expanded form
CCU	Capture and Compare Unit
C_{oss}	Output capacitance C_{oss} = CDS + CGD
$C_{o(tr)}$	Effective output capacitance, time related
CSG	Comparator and Slope Generator
di/dt	Steepness of current slope at turn-off/turn-on
EEPROM	Electrically Erasable Programmable Read-Only Memory
ERU	Event Request Unit
FPU	Floating Point Unit
HRC	High Resolution Channel
HRPWM	High Resolution PWM
I_D	Drain to source current
MAC	Multiplication and accumulation unit
NTC	Negative Temperature Coefficient thermistor
PFC	Power Factor Correction
PI	Proportional Integral controller
QG	Gate Charge
Q_{OSS}	Charge stored in the C_{oss}
QR	Quasi Resonant
$R_{DS(on)}$	Drain-source on-state resistance
R_g, on/off	Gate resistor applied at on and off transitions
SPI	Serial Peripheral Interface
SR	Synchronous Rectification
TDP	Technical Data Package
UART	Universal Asynchronous Receiver-Transmitter
USIC	Universal Serial Interface Channel
ZVS PSFB	Zero Voltage Switching Phase-Shift Full-Bridge

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