High-efficiency 3 kW bridgeless dual-boost PFC demo board

90 kHz digital control design based on 650 V CoolMOS™ C7 in TO-247 4-pin

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About this document

Scope and purpose

This document presents design considerations and results from testing a 3000 W 90 kHz power factor correction (PFC) bridgeless dual-boost converter with a peak efficiency higher than 98.5 percent, based on:

- **650 V CoolMOS™ C7** superjunction MOSFET in both TO-247 4-pin configuration for the high frequency PFC MOSFETs, and standard TO-247 configuration for the AC-line frequency active-rectification MOSFETs
- **CoolSiC™ Schottky diode 650 V G5**
- EiceDRIVER™ **1EDI60N12AF** isolated gate driver
- EiceDRIVER™ **2EDN7524F** non-isolated gate driver
- **XMC 1300** microcontroller
- **ICE2QR4780Z** flyback controller

Intended audience

This document is intended for design engineers who want to verify the performance of the 650 V CoolMOS™ C7 TO-247 4-pin MOSFET technology working at 90 kHz in a dual-boost PFC boost converter along with EiceDRIVER™ ICs and CoolSiC™ Schottky diode 650 V G5 using digital control based on the XMC 1300 microcontroller.

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1 Summary of the 3 kW bridgeless dual-boost PFC demo board

This application note provides a very detailed description of the design considerations and operation under both steady-state and abnormal operating conditions, as well as the results of a highly efficient bridgeless power factor (PF) correction topology using several different Infineon semiconductors, ranging from power MOSFETs to microcontrollers.

Below is a summary of the key features that this demo board offers when used as a reference for power supplies in server, telecom and industrial applications:

- Attractive compact design in 60 W/in^3 form factor.
- Efficiency higher than 98 percent from 20 percent of the rated load upward when V_{in} = 230 V AC, and efficiency higher than 96 percent from 20 percent of the rated load upward when V_{in} = 115 V AC. Such results are clearly shown in **Figure 26**.
- Superior performance compared to closest competitors' $R_{DS(on)}$ TO-247 4-pin MOSFETs, seen clearly in **Figure 29** and **Figure 30**.
- High PF and low total harmonic distortion (THD) response at different low-line and high-line input voltages, as shown in **Figure 27** and **Figure 28**.
- Fully digital control implementation using the XMC 1300 microcontroller, as described in the Software and control implementation section.
- High performance achieved by using Infineon's best-in-class devices:
  - Single TO-247 4-pin 650 V CoolMOS™ C7 SJ MOSFETs on each of the legs of the bridgeless dual-boost PFC topology, along with single TO-220 CoolSiC™ Schottky diodes 650 V G5
  - 650 V CoolMOS™ C7 TO-247 devices as active rectification MOSFETs to further boost the efficiency of the topology.
  - EiceDRIVER™ 1EDI isolated and EiceDRIVER™ 2EDN non-isolated gate driver ICs.
  - QR flyback controller ICE2QR2280G CoolSET™.
- Robust and realiable operation under different abnormal conditions:
  - Load-jump reaction and output regulation, as shown in **Figure 32**.
  - Smooth inrush current during start-up, as shown in **Figure 33**.
  - Power line disturbance (PLD) events, like AC-line drop-out and voltage sag, as shown from **Figure 34** to **Figure 37**.
  - 1 kV and 2 kV line-to-GND surge events that do not represent a serious threat to the integrity of the PFC high-switching-frequency MOSFETs or the active-rectification ones, as shown in **Figure 38** and **Figure 39**.
- Even though it is not in the current scope of this AN, anticipating product launches such as 600 V CoolMOS™ P7 and CoolSiC™ Schottky diode 650 V G6, this demo board has been used for evaluating Infineon's latest price-performance solution. These results are shown in **Figure 29** and **Figure 30**.

2 Introduction

A PF current converter shapes the input current of the power supply so that it is synchronized with the mains voltage, in order to maximize the real power drawn from the mains. In actual PFC circuits, the input current should match the input voltage as closely as possible, as if it was a pure resistive load, with quite limited harmonic distortion.

This document is intended to demonstrate the design and practical results of a 3000 W 90 kHz bridgeless dual-boost PFC demo board based on Infineon devices, including power semiconductors, isolated and non-isolated gate drivers, and the microcontroller for the control loop as well as the flyback controller for the auxiliary supply. This demo can be used as reference for the PFC stage for any server, telecom or industrial power supply solution.

2.1 Topology

Although active PFC can be achieved by several topologies, the dual-boost converter (**Figure 1**) is a very attractive solution for high-power supply solutions for the following reasons:

- Compared to the standard/classic PFC rectifier based on a diode bridge (with two active diodes at all times), a single PFC MOSFET and a PFC diode, the dual-boost has lower conduction losses because there are always two power semiconductors (e.g., Q1 + D3 or Q2 + D4) in the current path per AC semi-cycle. However, for ease of control and taking into account impedance on the returning path, even three can be active (e.g., Q1 + D3 || Q2 or Q2 + D4 || Q1).
- Higher efficiency at a higher power density compared to the same rated power standard/classic PFC rectifier, due to less cooling effort and better heat spot distribution.
- More efficient and easier to control compared to an interleaved PFC rectifier, as this is a bridgeless topology with no need for phase shedding between the PFC legs.
- To increase the efficiency further, low $R_{DS(on)}$ MOSFETs (Q3 and Q4) can be placed in parallel with each of the returning path diodes (i.e. D3 and D4). As these MOSFETs will be conducting at the AC-line frequency, the switching losses and gate driving losses are much lower than conduction ones. This benefit comes at the expense of increasing bill of materials (BOM) count and cost, as well as accurate control and driving circuitry.

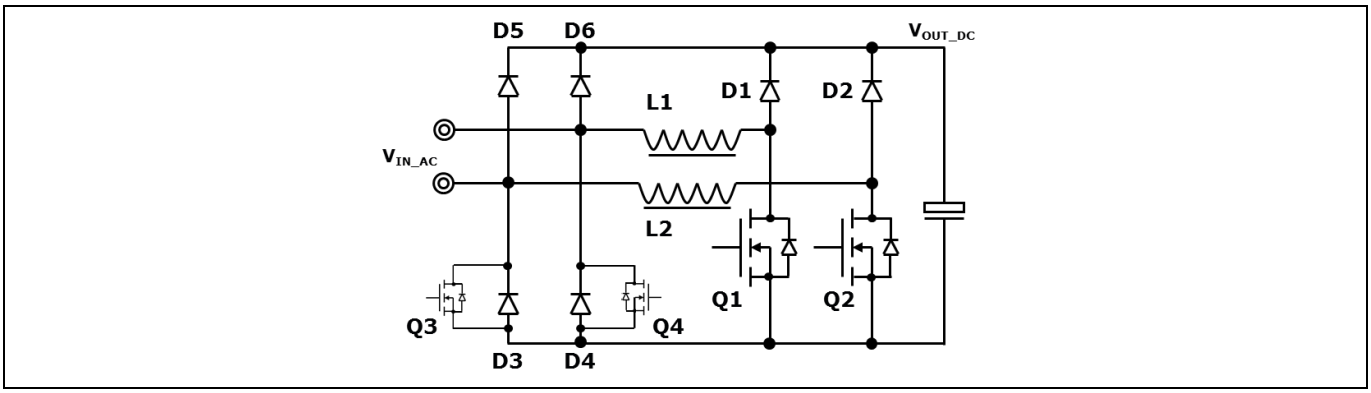


Figure 1 Bridgeless dual-boost PFC converter

2.2 Conduction modes

The boost converter can operate in three modes: continuous conduction mode (CCM), critical conduction mode (CrCM) and discontinuous conduction mode (DCM). **Figure 2** shows actual inductor current waveforms to illustrate the three operating modes under light-load conditions.

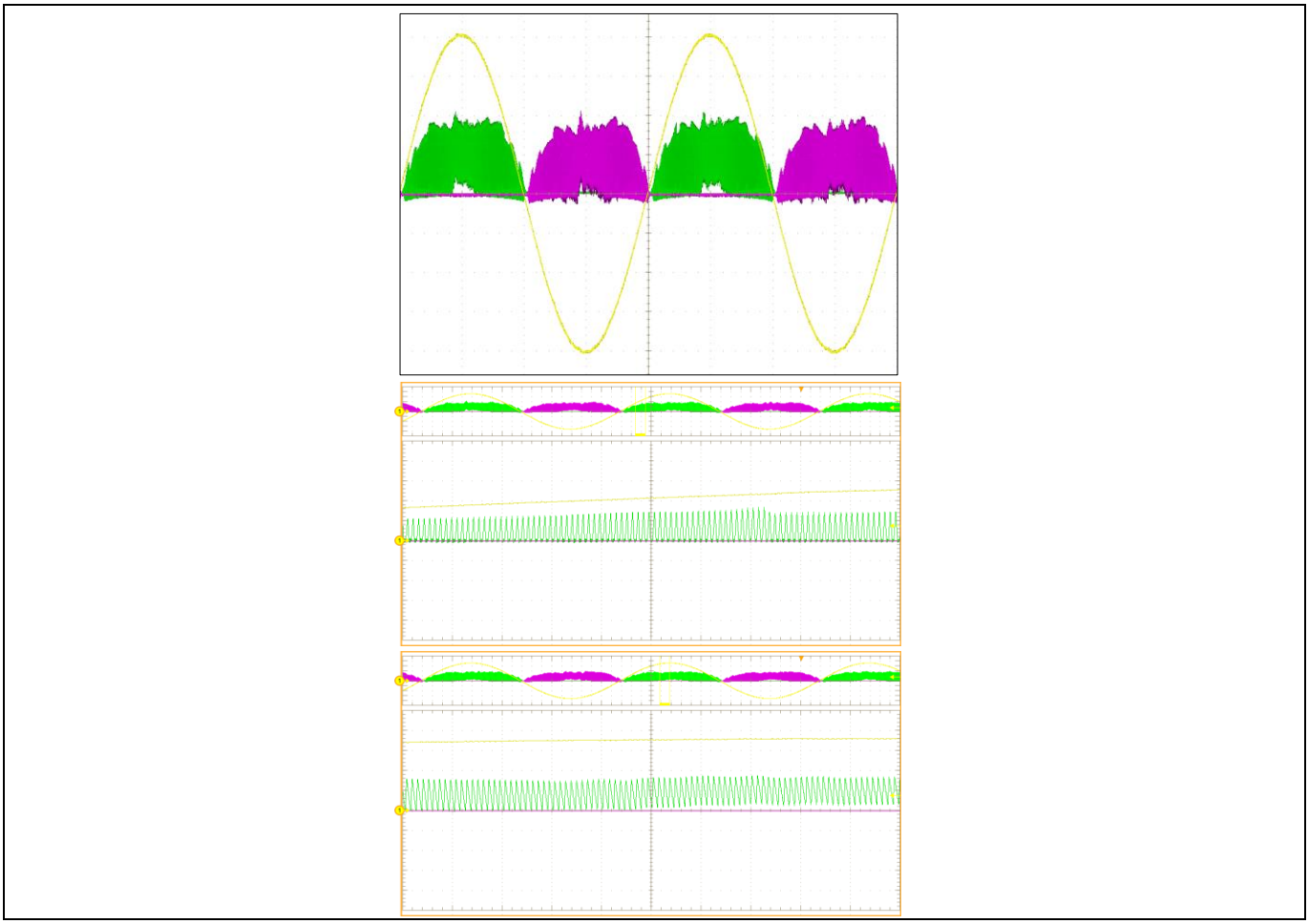


Figure 2 **Top: Both PFC inductor current waveforms at 10 percent of the rated load**
Middle: Detail of one of the inductor currents, showing DCM operation only
Bottom: Detail of one of the inductor currents, showing CrCM and CCM operation

For fixed switching frequency operation, the input voltage and output power of the PFC will determine the operation mode. In this way there can be the following:

- Complete half-AC cycle in DCM operation mode
- DCM, CrCM and CCM operation modes during half-AC cycle
- Complete half-AC cycle in CCM operation mode

The control mode of the dual-boost PFC topology used in this demo board is focused on constant switching frequency operation, with the advantage of having a simplified input filter. The XMC™ microcontroller used for the PFC handles both DCM and CCM operation modes, depending on the input voltage and output load conditions.

2.3 Operation modes per leg

As explained, for ease of control both PFC MOSFETs Q1 and Q2 can be driven by the same PWM signal. Additionally, in order to boost the efficiency of the topology, active rectification MOSFETs Q3 and Q4 are added. This means that the inductor current returns by different paths during the charging and discharging periods of the corresponding inductor. As an example, **Figure 3** clearly shows the different paths taken by the inductor current during the positive AC semi-cycle.

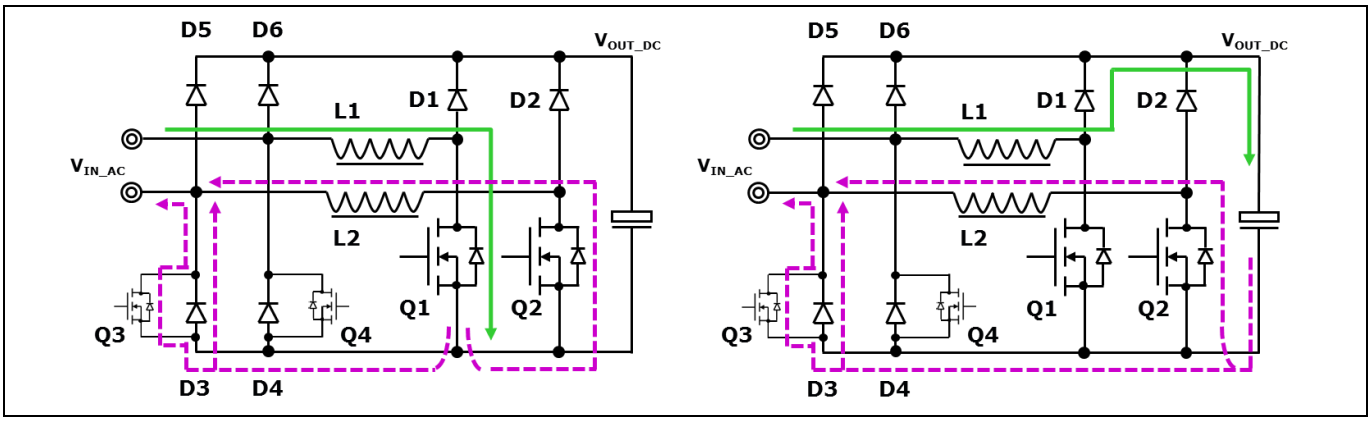


Figure 3 Example of the paths of the inductor current in different operation modes. Left: When the PFC MOSFET Q1 is turned on; Right: When the PFC MOSFET Q1 is turned off

Depending on the impedance of the returning paths, say through Q2 + Z_{L2}, D3 as well as Q3 and including the PCB traces, the inductor current will find its way back to the AC source in different split amounts. The left-hand graph in **Figure 4** shows the current through inductor L1 (green, in the background) and the current through the active rectification MOSFET Q3 (magenta, in front) at 50 percent load. In this condition, almost all of the inductor current flows back to the AC source through Q3; this is clearly seen as the magenta waveform matches the green one.

The right-hand graph in **Figure 4** shows the current through inductor L1 (green) and the current through the active rectification MOSFET Q3 (magenta) at 100 percent of the load. As can be clearly seen, most of the inductor current flows back to the AC source through Q3. This means that part of the current flows back through L2 via Q2 and another part through D3. The effect of the current flowing back through the opposite leg of the converter can be clearly seen as a negative lagging distorted sinusoidal shape on the inductor current waveform. Such behavior is also clearly seen when both inductor currents are measured in the same operating conditions, as shown in **Figure 5**.

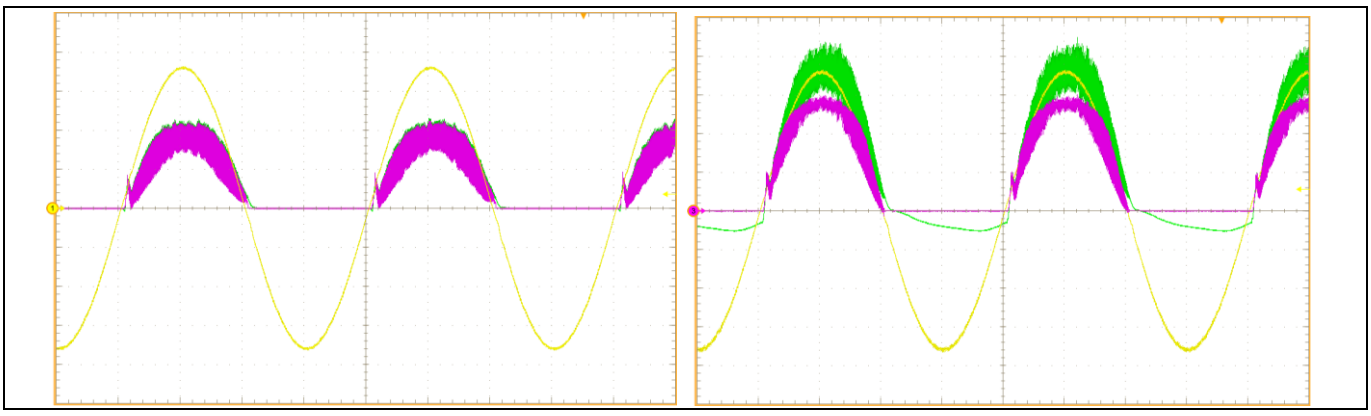


Figure 4 Inductor current (green), e.g., I_{L1}, and active rectification MOSFET current (magenta), e.g., I_{Q3} in half-load (left) and full-load (right) operation

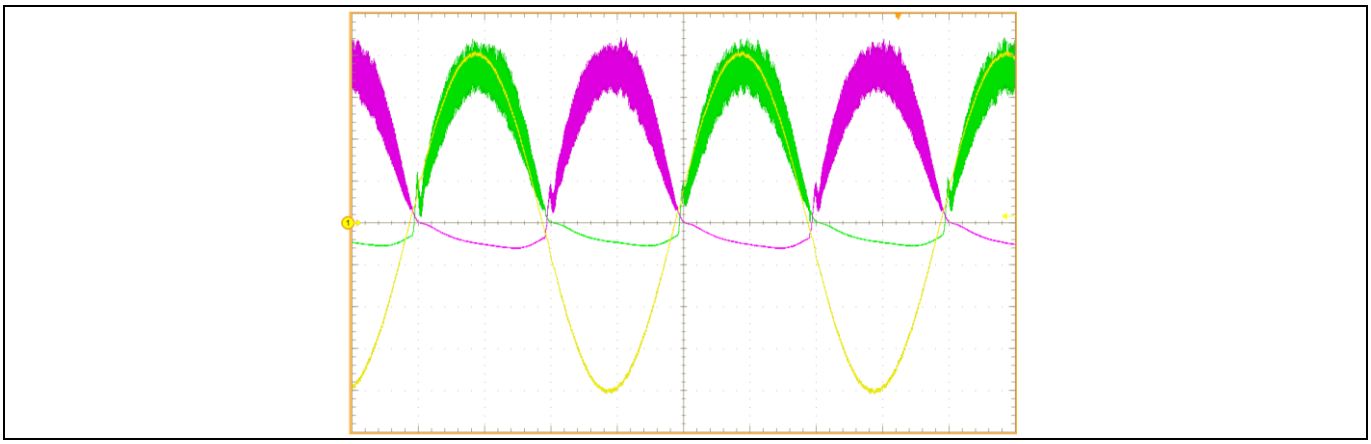


Figure 5 Inductor L1 current (green) and inductor L2 current (magenta) in full-load operation

Due to this complex multiple return path of the current, it would be inappropriate to place only a shunt resistor between the switching legs of the converter and the bridge rectifier, as is done in the standard/classic PFC. In this case, a current transformer is more suitable to enable monitoring of the actual inductor current. This approach can be seen in **Figure 41**.

3 Demo board features

3.1 Specifications

Table 1 Input requirements

Parameter	Value
Input voltage range, V_{in_range}	90–265 V AC
Nominal input voltage, V_{in}	230 V AC
AC-line frequency range, f_{AC}	47–63 Hz
Max peak input current, I_{in_max}	14.9 A_{RMS} at V_{in} = 90 V AC and P_{out} = 1.3 kW 15.46 A_{RMS} at V_{in} = 200 V AC and P_{out} = 3 kW
Turn-on input voltage, V_{in_on}	80–87 V AC, ramping up
Turn-off input voltage, V_{in_off}	75–85 V AC, ramping down
PF (PF)	> 0.95 from 10 percent rated load and above
Hold-up time	10 ms after last AC zero-point at P_{out}, V_{out_min} = 320 V DC 20 ms after last AC zero-point at 0.5 x P_{out}, V_{out_max} = 320 V DC
THD	< 10 percent from 10 percent load at nominal input voltage for class A equipment

Table 2 Output requirements

Parameter	Value
Nominal output voltage, V_{out}	400 V DC
Maximum output power, P_{out}	3 kW
Maximum output current, I_{out_max}	7.5 A
Output voltage ripple	Max 20 V_{pk-pk} at V_{out} and I_{out}
Maximum output Over Voltage (OV) threshold	435 V DC
Minimum output OV threshold	430 V DC

Table 3 Efficiency under different load conditions

Value	Conditions
> 96 percent from 20 percent of the rated load	V_{in} = 115 V AC
> 98 percent from 20 percent of the rated load	V_{in} = 230 V AC
> 98.5 percent at 50 percent of the load	V_{in} = 230 V AC

3.2 EMI filter

The EMI filter is implemented as a two-stage filter, which provides sufficient attenuation for both differential mode (DM) and common mode (CM) noise.

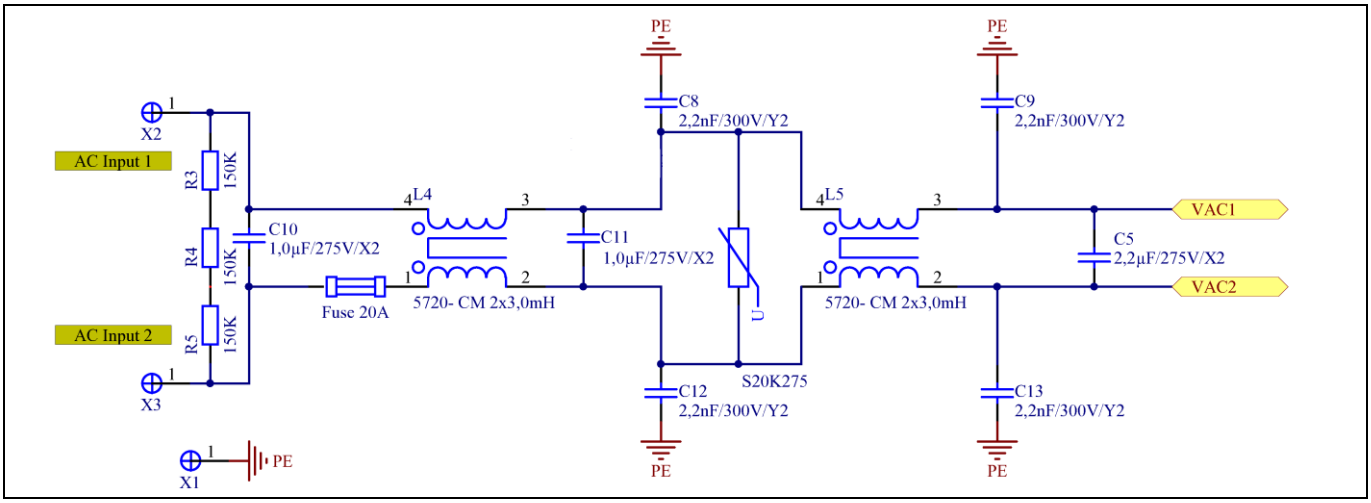


Figure 6 Two-stage filter structure

The two high-current CM chokes L4 and L5 cm are based on high-permeability toroid ferrite cores. Each of these has 2 x 18 turns or 2 x 3 mH inductance.

The relatively high number of turns causes a considerable amount of stray inductance, which ensures sufficient DM attenuation.

In case the fuse is blown due to any abnormal conditions during the operation of the converter, the C10 X-capacitor in **Figure 6** is fully discharged through resistors R3, R4 and R5 in order to prevent any electric shock injuries to the operator of the demo board.

3.3 Bridge rectifier

Taking **Figure 1** as a reference, in contrast with the standard/classic and interleave topologies, the bridge rectifier employed in this demo board has two main purposes:

- Diodes D5 and D6 support the pre-charging of the bulk capacitors to the peak value of the AC-line voltage. Once the bulk capacitors are charged, these diodes are no longer active during the steady-state operation of the topology.
- Diodes D3 and D4 support the returning path between the AC input and the output ground, so the voltage potential of the output is stabilized and the CM noise of the converter is drastically reduced.

To determine the proper selection and losses of the bridge rectifier, it is necessary to calculate the input RMS and average input current under the worst operating conditions, i.e. efficiency of 97 percent at V_{in} = 178 V AC :

Maximum RMS value of the input current:

$$I_{IN_RMS} = \frac{P_{OUT_MAX}}{\eta \cdot V_{IN_RMS}} = \frac{3000W}{0{,}97 \cdot 178V} = 17.37A$$

Maximum RMS current value per diode, D3 or D4:

$$I_{BR-D_RMS} = \frac{\sqrt{2} \cdot I_{IN_RMS}}{2} = 12{,}28\ A$$

Maximum average current value per diode:

$$I_{BR-D_avg} = \frac{\sqrt{2} \cdot I_{IN_RMS}}{\pi} = 7{,}82A$$

Due to the calculated average and effective current values, the rectifier type LVB2560 with very low forward voltage drop was selected. This 600 V device has sufficient voltage reserve with V_{in} = 265 V AC. For the following formula, the instantaneous forward resistance (r_D) and forward voltage drop (V_{BR-D}) are extracted from the characteristic curves of the corresponding data sheet (T_A = 100°C).

Conduction losses of a rectifier diode, D3 or D4, per AC cycle:

$$P_{BR-D} = I_{BR-D_avg} \cdot V_{BR-D} + \left(I_{BR-D_{RMS}}\right)^2 \cdot r_D = 7{,}82 \cdot 0{,}75 + (12{,}28)^2 \cdot 65\ m\Omega \cong 15.6W$$

3.4 PFC choke

The PFC choke design is based on a toroidal high-performance magnetic powder core.

Toroidal chokes have a large surface area and allow a good balance, minimizing core and winding losses, and achieving a homogeneous heat distribution without hot spots. For this reason they are suitable for systems that are targeting the highest power density with forced-air cooling. Very small choke sizes are feasible.



Figure 7 Photos of the PFC choke

The chosen core material is HIGH FLUX from Chang Sung Corporations (CSC), which has an excellent DC bias and good core loss behavior. The part number is CH270060E18. The outer diameter of the core is 27 mm with a height of 19 mm.

The winding was implemented using enameled copper wire AWG 16 (1.37 mm diameter). The winding covers approximately two layers. This arrangement allows a good copper fill factor, while still having good AC characteristics, and is a preferred fill form factor for high-power toroidal inductors.

There are 46 turns, taking advantage of the high permitted DC bias. The resulting small signal bias inductance is 254 µH. The effective inductance with current bias is determined by the core material B-H characteristics, illustrated as follows:

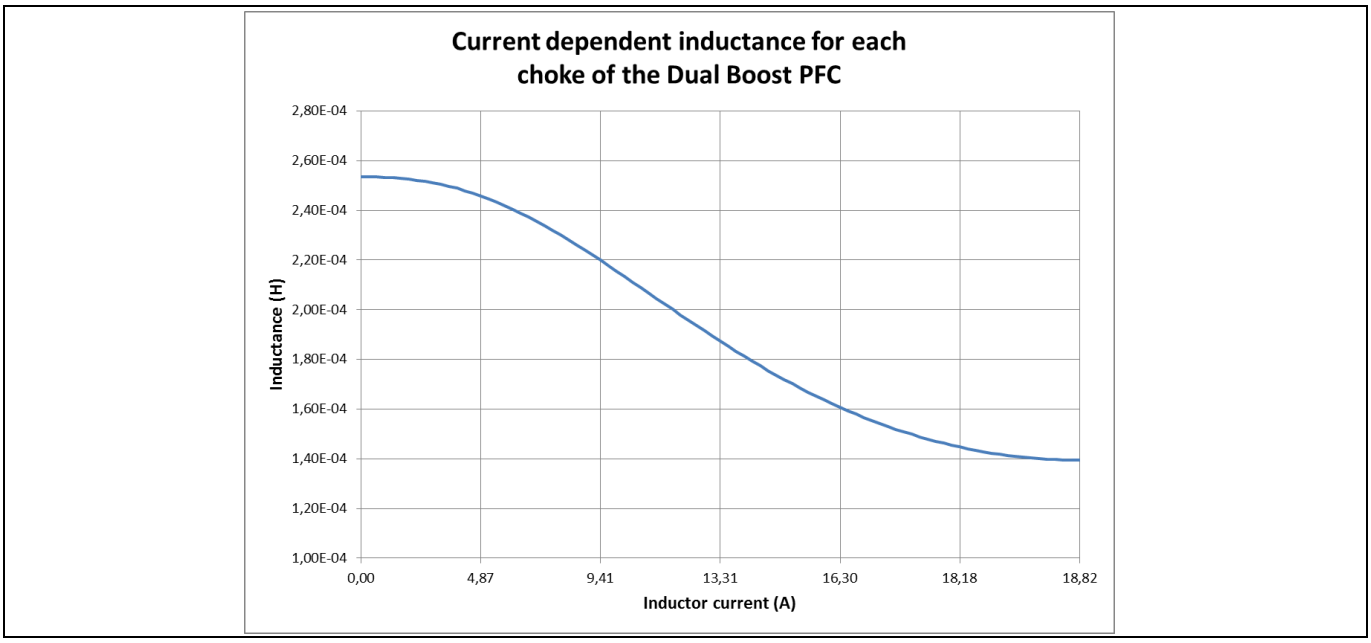


Figure 8 Input current-dependent inductance of the PFC chokes

The effective inductance, with a current ripple ratio of 30 percent per design together with the switching frequency of 90 kHz, produces a low current ripple that supports the whole system performance, as shown in **Figure 9**. Similarly, the low-ripple design achieves low core losses, as shown in **Table 4**.

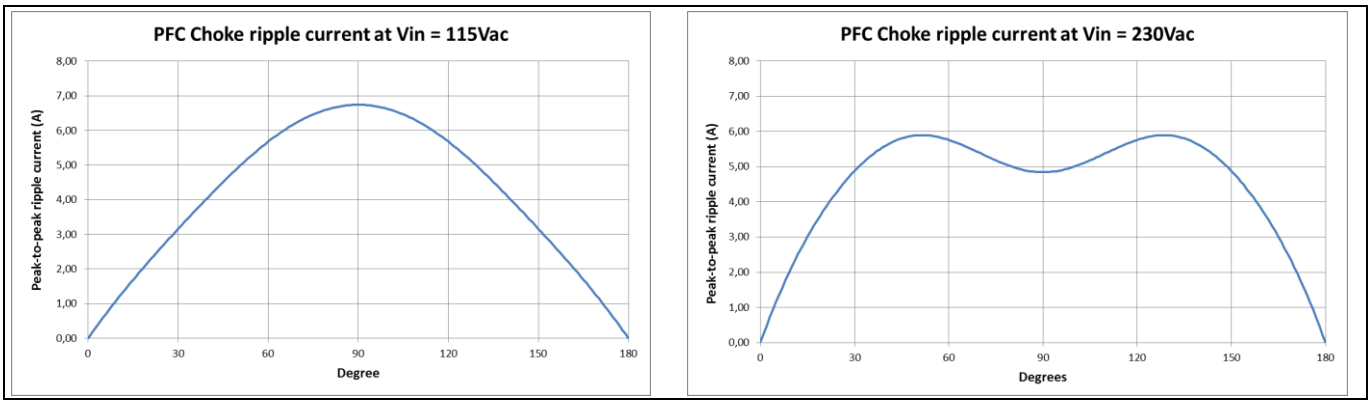


Figure 9 PFC choke peak-to-peak ripple current under full-load (full-CCM) operation at low- and high-line input voltage

Table 4 PFC choke losses at 90 kHz (results calculated from a magnetic design tool)

Operating conditions	P_{CORE} (W)	$P_{WINDINGS_@_80°C}$ (W)	P_{TOTAL} (W)
115 V AC at 1.3 kW	1.92	5.05	6.97
230 V AC at 3 kW	2.04	6.59	8.63

3.5 Infineon semiconductors

3.5.1 650 V CooMOS™ C7

The CoolMOS™ C7 series is a revolutionary step forward, providing the worlds's lowest $R_{DS(on)}$ per package and, thanks to its low switching losses, efficiency improvements over the full load-range. The main features of this technology are:

- Increased MOSFET dv/dt ruggedness
- Better efficiency due to best-in-class figure of merits (FOM) $R_{DS(on)}$ x E_{oss} and $R_{DS(on)}$ x Q_G
- Easy to use/drive due to driver source pin for better control of the gate
- Such features bring meaningful benefits to the final application, including:
- Enabling higher system efficiency, as the parasitic inductance of the power source pin does not interfere in the driving PWM signal at the gate – as a result, undesired re-turn-off events are completely avoided
- Enabling increased power density solutions
- System cost/size savings due to reduced cooling requirements
- Higher system reliability due to lower operating temperatures

3.5.2 Gate driver for MOSFETs

3.5.2.1 EiceDRIVER™ 2EDN non-isolated gate driver for MOSFETs

The 2EDN7524 is a non-inverting fast dual-channel driver for low-side switches. Two true rail-to-rail output stages with very low output impedance and high current capability are chosen to ensure the highest flexibility and cover a wide variety of applications.

All inputs are compatible with LVTTL signal levels. The threshold voltages (with a typical hysteresis of 1 V) are kept constant over the supply voltage range.

Since the 2EDN7524 is particularly aimed at fast switching applications, signal delays and rise/fall times have been minimized. Special effort has been made to minimize delay differences between the two channels to very low values (typically 1 ns).

The 2EDN7524 driver used in this demo board comes in a standard PG-DSO-8 package.

3.5.2.2 EiceDRIVER™ 1EDI galvanically isolated single-channel driver

The 1EDI driver family is based on Infineon's coreless transformer technology, enabling a benchmark minimum common mode transient immunity (CMTI) of 100 kV/µs.

The 1EDI60N12AF driver provides output currents of up to 6 A on separate output pins for applications up to 1200 V. This is ideal for all topologies using **CoolMOS™** in 3- and 4-pin packages in power supplies for servers, and industrial and telecommunications systems.

The input logic pins operate over a wide input voltage range, from 3 V to 15 V, using CMOS threshold levels to support even 3.3 V microcontrollers.

3.5.3 Fifth-generation CoolSiC™ Schottky diode

Because CoolSiC™ Schottky diodes have a capacitive charge, Q_c, rather than a reverse recovery charge, Q_{rr}, their switching loss and recovery time are much lower than a silicon ultrafast diode, leading to enhanced

performance. Moreover, SiC diodes allow higher switching frequency designs. Hence, higher power density converters are achieved. The capacitive charge for SiC diodes is not only low, but also independent of di/dt, current level and temperature, which is different from silicon diodes that have a strong dependency on these conditions.

The recommended diode for CCM boost applications is the CoolSiC™ Schottky diode 650 V G5, which includes Infineon's leading-edge technologies, such as a diffusion soldering process and wafer thinning technology. The result is a new family of products that show improved efficiency over all load conditions, resulting from the improved thermal characteristics. Even with the high surge current capability of SiC Schottky diodes, it is still preferable to use bulk pre-charge diodes. These are low-frequency standard diodes (D5 and D6 in **Figure 1**) with a high I^2t rating to support pre-charging the bulk capacitor to the peak of the AC-line voltage; this is a high initial surge current stress (which should be limited by a series NTC) that is best avoided for the PFC boost rectifier diode.

The proper current rating of the PFC diodes must be calculated by considering 1.3 to 1.5 times the RMS current of the diode, which is expressed as:

$$I_{D_RMS} = \frac{P_{OUT_MAX}}{V_{IN_RMS} \cdot \eta} \times \sqrt{\frac{8 \cdot \sqrt{2} \cdot V_{IN_RMS}}{3 \cdot \pi \cdot V_{OUT}}} = \frac{3000}{178 \cdot 0{,}97} \times \sqrt{\frac{8 \cdot \sqrt{2} \cdot 178}{3 \cdot \pi \cdot 400}} = 12.7\ A$$

In this demo board, 16 A IDH16G65C5 diodes are used.

3.5.4 XMC 1302 microcontroller for PFC digital control implementation

The XMC 1300 devices are members of the XMC 1000 family of microcontrollers based on the ARM Cortex-M0 processor core. The XMC 1300 series addresses the real-time control needs of digital power conversion. The control of power supplies is a strong focus for XMC™ microcontrollers, where users can benefit from features such as analog comparators, PWM timers, co-processors or high-precision analog-to-digital converters.

Some of the XMC 1302 features are listed below:

- 200 KB Flash, 16 KB RAM
- MATH co-processor for CORDIC and HW Divide
- 8 x 16-bit special-purpose timers, dead-time generation
- 12 channel, 12-bit ADC, 2 x parallel sampling
- 3 x comparators
- Real-time clock
- Watch-dog timer

3.6 Output capacitor

Possible OVs require the selection of a 450 V (low-impedance) type capacitor. The minimum capacitance is defined by the minimum hold-up time, t_{hu} = 10 ms, and the minimum allowable DC link voltage of the system, V_{BULK_min} = 320 V, or the maximum allowable voltage from the 2x line-frequency AC ripple current:

$$C_{bulk} \geq \frac{2 \times P_{OUT_{MAX}} * t_{hu}}{V_{BULK}^2 - V_{BULK_min}^2} = \frac{2 \times 3000 \times 10 \times 10^{-3}}{400^2 - 320^2} \geq 1041.67 \mu F$$

The chosen arrangement is three 390 µF at 450 V 30 mm x 35 mm electrolytic type capacitors.

3.7 Heatsink and cooling fan

The heatsink (HS) for the power semiconductors is made from a 1 mm copper plate. In this demo board a 40 mm x 40 mm x 28 mm, 14250 rpm (18.3 CFM) fan is used. The fan speed is fully and accurately controlled by the microcontroller, which continuously monitors HS temperature.

4 Software and control implementation

4.1 Interface between the PFC power stage and the XMC 1300

Figure 10 shows how each of the internal blocks of the XMC 1302 microcontroller is connected to the topology. The red blocks mark the hardware units that are necessary to handle the input and output signals, respectively. Blue boxes show programmed software parts for the application, and finally the gray boxes identify the abnormal conditions and their interactions.

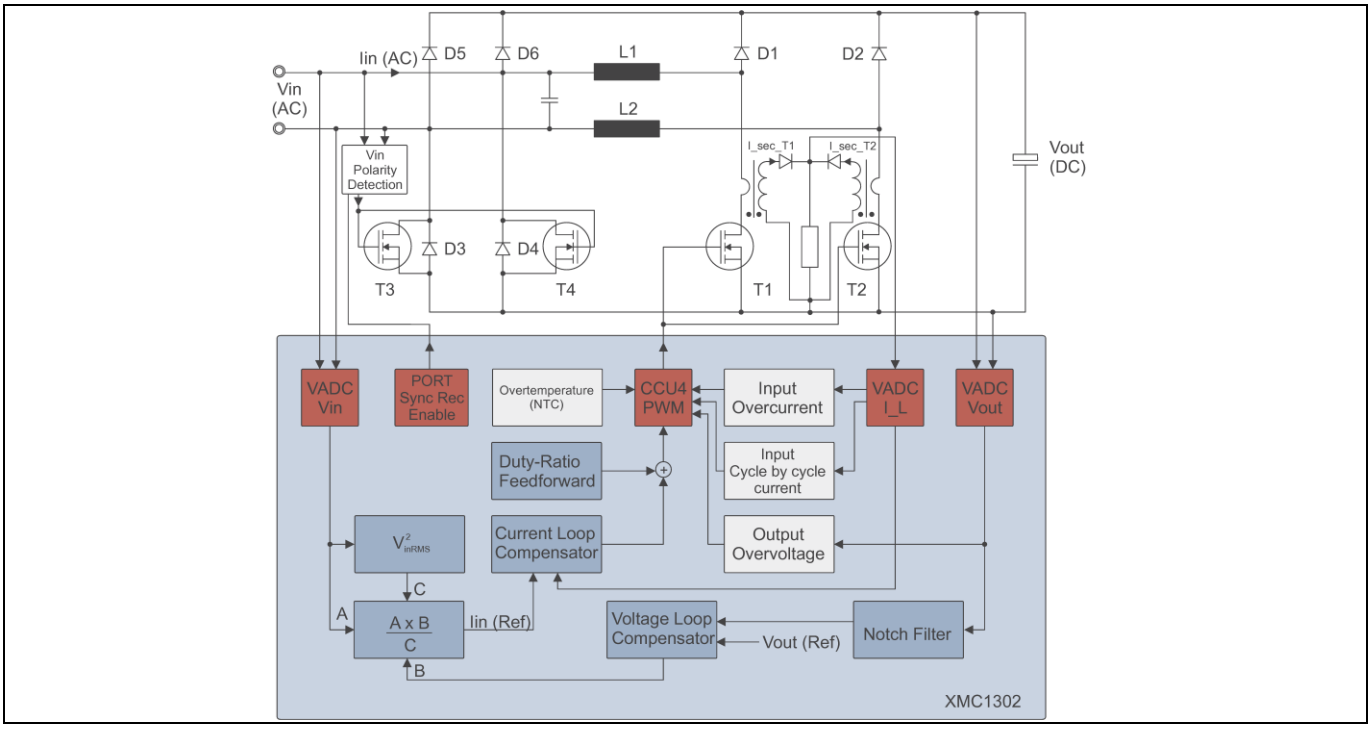


Figure 10 System setup for the dual-boost bridgeless PFC

4.2 Software states

The different states of the PFC-control which are handled in the XMC 1302 software are shown below:

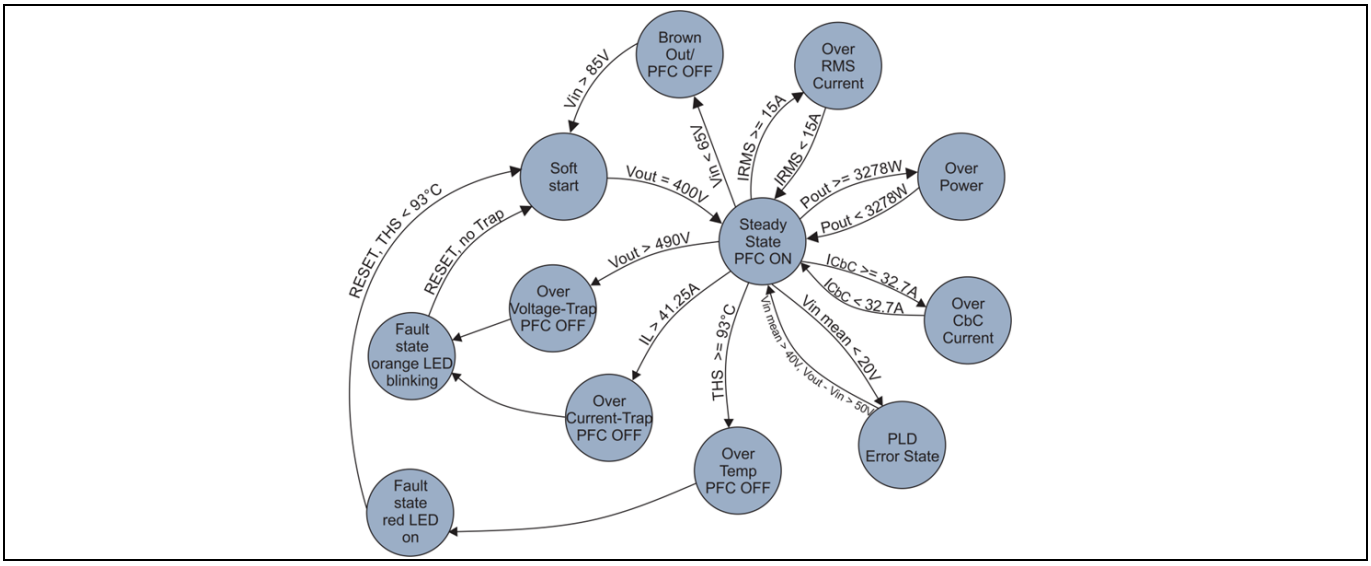


Figure 11 PFC state machine

4.3 Control implementation

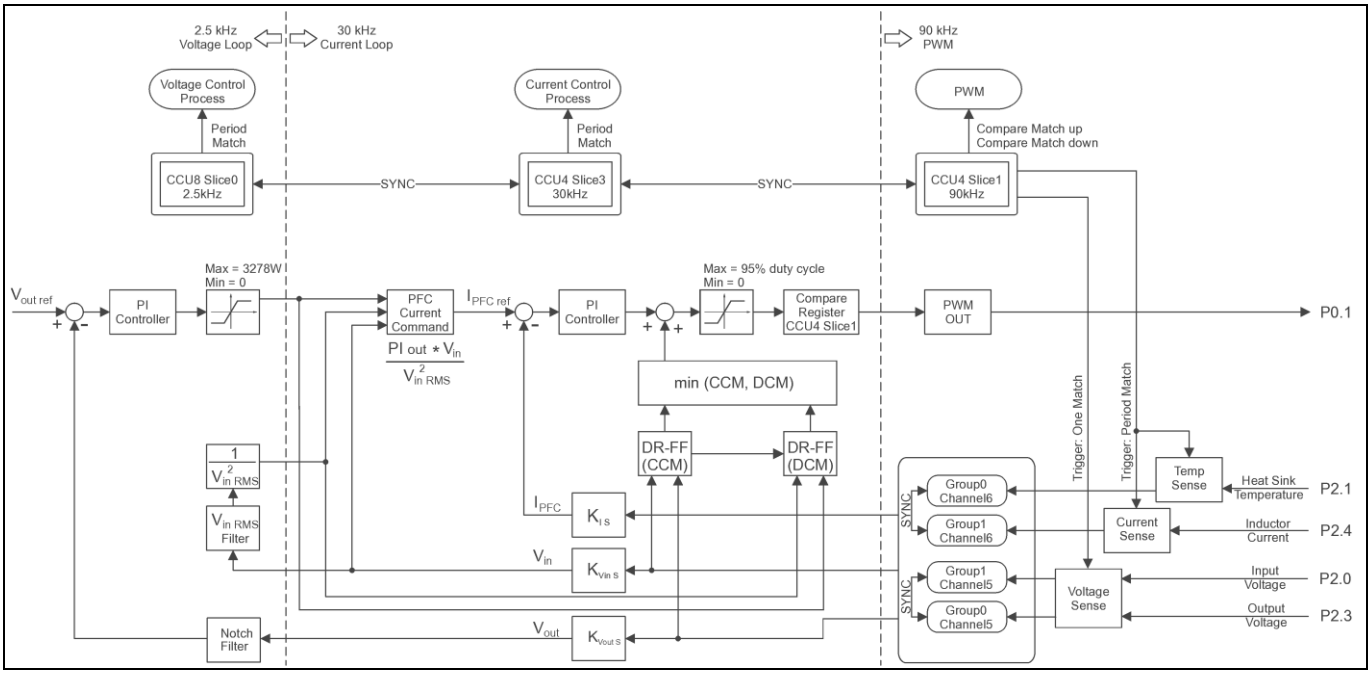


Figure 12 Detailed control structure

4.4 Regulation algorithms

4.4.1 Output voltage control loop

4.4.1.1 Theory

The figure below shows the overall structure of the voltage control loop.

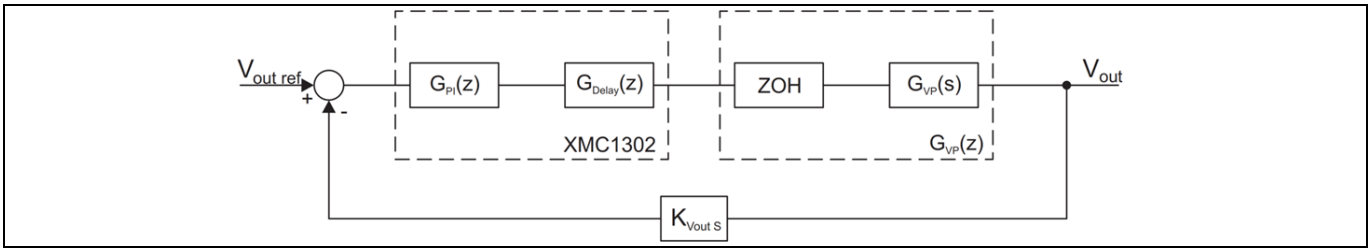


Figure 13 Dual-boost PFC voltage control loop

The basis for an output voltage loop design is the assumption of a constant power load at the output. This is realistic for the case when a DC-DC converter is attached to the output of the PFC stage, and leads to the following plant transfer function, with g_c being the current source to charge the output capacitor C:

$$G_{VP}(s) = \frac{g_C}{sC}$$

The plant transfer function is transformed into the z-plane using a zero order hold (ZOH):

$$G_{VP}(z) = \frac{g_C \cdot T_S}{C \cdot (z-1)}$$

The open loop voltage transfer function, which includes a PI-controller and the digital delay, as well as the plant and output voltage feedback (FB) factor K_{VoutS}, is defined as follows [2]:

$$G_{VOL} = G_{PI}(z) \cdot G_{Delay}(z) \cdot G_{VP}(z) \cdot K_{VoutS} = \frac{K_P(z-N)}{z-1} \cdot z^{-1} \cdot \frac{g_C \cdot T_S}{C \cdot (z-1)} \cdot K_{VoutS}$$

The BW of the voltage loop is chosen such that there is enough dynamic performance for transient conditions. As the notch filter is designed to filter out twice the mains frequency, the zero crossing (ZC) frequency (fc) is set to 200 rad/s/(2π) = 31.8 Hz.

With the demand for a phase margin (PM) of 45° and a maximum gain of 1 at the selected ZC frequency, C_{out} = 3 x 390 µF, T_S = 400 µs, V_{out} = 400 V DC, K_{VoutS} = 1/(449.74 V), the parameters K_p (gain factor) and K_i (integral factor) are determined to: K_p = 0.97; K_i = 0.08.

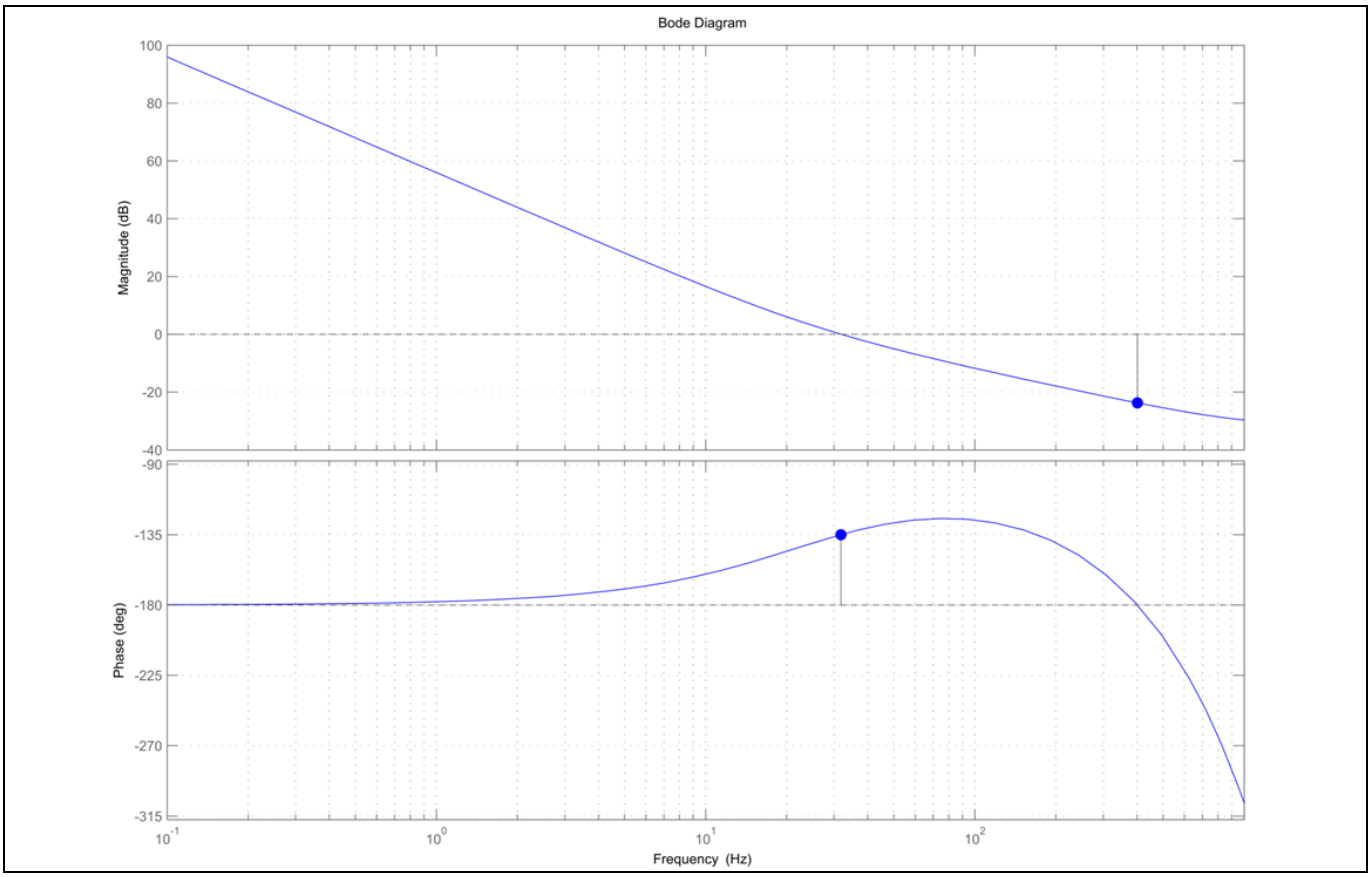


Figure 14 Bode diagram of voltage control loop; fc = 200/(2π) Hz, phase margin (at fc) = 45° and gain margin = 23.7 dB

4.4.1.2 Flow diagram

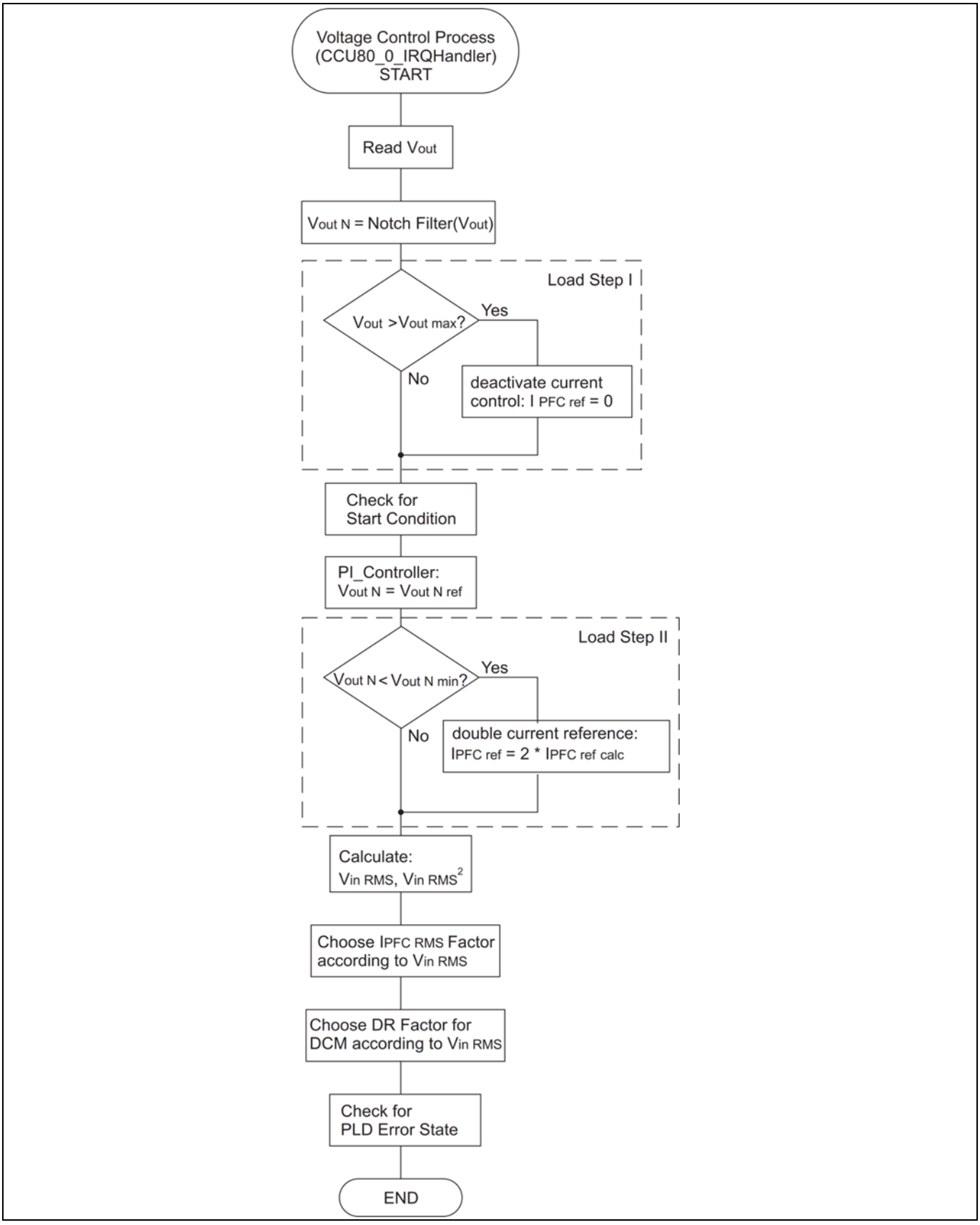


Figure 15 Voltage control loop flow diagram

Explanation of the flow diagram shown in **Figure 15**:

- **Load-step I**: If the output voltage exceeds 425 V DC, the input current regulation is stopped and the PWM signal is set inactive. If the output voltage is below 415 V DC, this state is overcome by starting the input current regulation again with an active PWM signal.
- **Start condition**: If the PFC converter is switched from inactive to active mode, the output voltage reference is incrementally increased until its nominal value (400 V) is reached, i.e soft-start. During that time the fan is switched off.
- **Load-step II**: If the output voltage drops below 375 V DC, then the calculated value for the input current reference is immediately doubled. As this measure may exceed the power range of the board, doubling will be finished after approximately 5 seconds, when the output voltage regulator is at its upper limit, or as soon as the output voltage exceeds 395 V DC again. This doubling is not active during soft-start.
- **V_{in} RMS** calculation: This is done by filtering the input voltage with two low-pass filters in series that each have the same time constant. The time constant is chosen such that the original content of the second harmonic of the input voltage of 66 percent of **V_{in} mean** is reduced to 1.5 percent of **V_{in} mean** [1]. The necessary overall damping of 1.5 percent /66 percent = 0.0227 yields to a damping of 0.15 for each low-pass filter. Eventually, the time-constant for the low-pass can be calculated by defining the necessary cut-off frequency to 0.15 x 100 Hz. The transformation from **V_{in} mean** to **V_{in} RMS** is done with help of the crest factor for sinusoidal input voltages.
- **I PFC RMS factor** calculation: The input current reference is proportional to **1/(V_in_RMS)²** in order to account for changes in **V_{in} RMS** for constant output power delivery. This factor is also used for RMS input current limitation. From 195 V AC downward, the factor is set to 200 V DC x V_in_RMS, rather than being **1/(V_in_RMS)**², yielding a calculated maximum RMS input current value of 3 kW/ 200 V AC = 15 A. In the software, the value is taken from a table, rather than doing a division operation, in order to reduce calculation time in the microcontroller. In other words:

$$I_{PFC\ ref} = \frac{PI_V_out \cdot V_{in}}{V_{in\ RMS}^2}$$

The value in the microcontroller (X') with the appropriate Q 0.15 format is:

$$I'_{PFC\ ref} = PI_{V_{out}}{}' \cdot V'_{in} \cdot I_{PFC\ RMS\ Factor}{}'$$

When 195 V AC < V_{in} ≤ $V_{in\ max}$

$$I_PFC_RMS_Factor' = \frac{N_{Vin}^2}{V_{in\ RMS}^2}$$

When $V_{in\ min}$ ≤ V_{in} ≤ 195 V AC

$$I_PFC_RMS_Factor' = \frac{N_{Vin}^2}{200V \cdot V_{in\ RMS}}$$

Note: N is the measurement range and equal to 1/K, with K being the corresponding scaling factor of analog input signal.

- Duty ratio **(DR) factor** for DCM calculation: The theoretical DR in DCM is proportional to the square root of the input conductance (**Ge**) of the converter. **Ge** is defined as **Pin/V_in_RMS**² in the stationary case and approximated by the microcontroller to **PI_V_out/V_in_RMS**². In the software, a factor proportional to **1/Vin_RMS**² is taken from a table, rather than doing a division operation, in order to reduce calculation time in the microcontroller.

$$DR_DCM_Factor' = \frac{2 \cdot N_{vin} \cdot N_{Iin} \cdot L \cdot f_{SW}}{V_{in\ RMS}^2}$$

- Phase line distortion detection: This error (abnormal) state is detected by calculating the mean input voltage over a time period of 3.2 ms. In case the mean input voltage is less than 20 V AC, the active PFC mode is left by means of switching off the PFC MOSFETs. PWM is set to inactive.

4.4.2 Input current loop control

4.4.2.1 Theory

The figure below shows the overall structure of the current control loop:

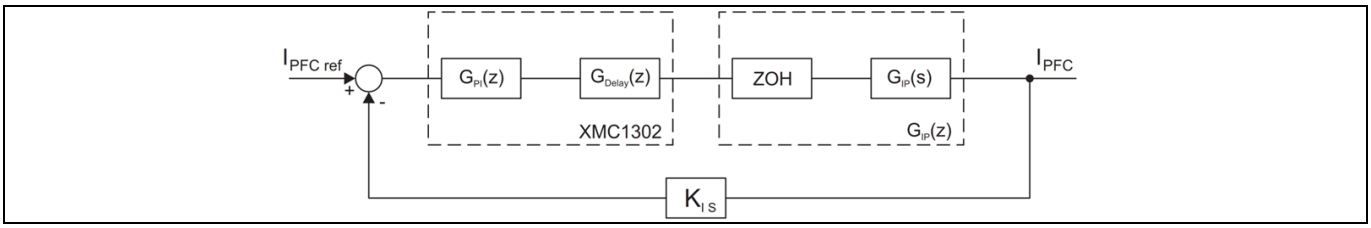


Figure 16 Dual-boost PFC current control loop

The plant transfer function duty cycle to input current ($G_{IP}(s)$) can be derived from the small signal model of the current loop, with L being the inductance of the PFC choke:

$$G_{IP}(s) = \frac{V_{out}}{sL}$$

To account for digital control, this plant transfer function is transformed to a ZOH (ZOH(z)):

$$G_{IP}(z) = \frac{V_{out} \cdot T_S}{L \cdot (z-1)}$$

The transfer function of the digital PWM (DPWM) is unity, $G_{DPWM}(z) = 1$,as the maximum output of the current controller is one and the minimum output is zero. One cycle digital delay is modeled as $G_{Delay}(z) = z^{-1}$. Current FB is given by the factor K_{IS}. A PI-controller of the following form is used:

$$G_{PI} = \frac{K_P(z-1)}{z-1}$$

Then the overall open loop transfer function of the current loop is [2]:

$$G_{IOL} = G_{PI}(z) \cdot G_{DPWM}(z) \cdot G_{Delay}(z) \cdot G_{IP}(z) \cdot K_{IS} = \frac{K_P(z-N)}{z-1} \cdot z^{-1} \cdot \frac{V_{out} \cdot T_S}{L \cdot (z-1)} \cdot K_{IS}$$

With the demand for a phase margin of 45° and a maximum gain of one at the selected 2.5 kHz (= 15707 rad/s) ZC frequency, L = 254 µH, T_s = 33.33 µs, V_{out} = 400 V DC, K_{IS} = 1/(37.5 A), and the parameters K_p (gain factor) and K_i (integral factor) were determined to K_p = 0.35 and K_i = 0.18.

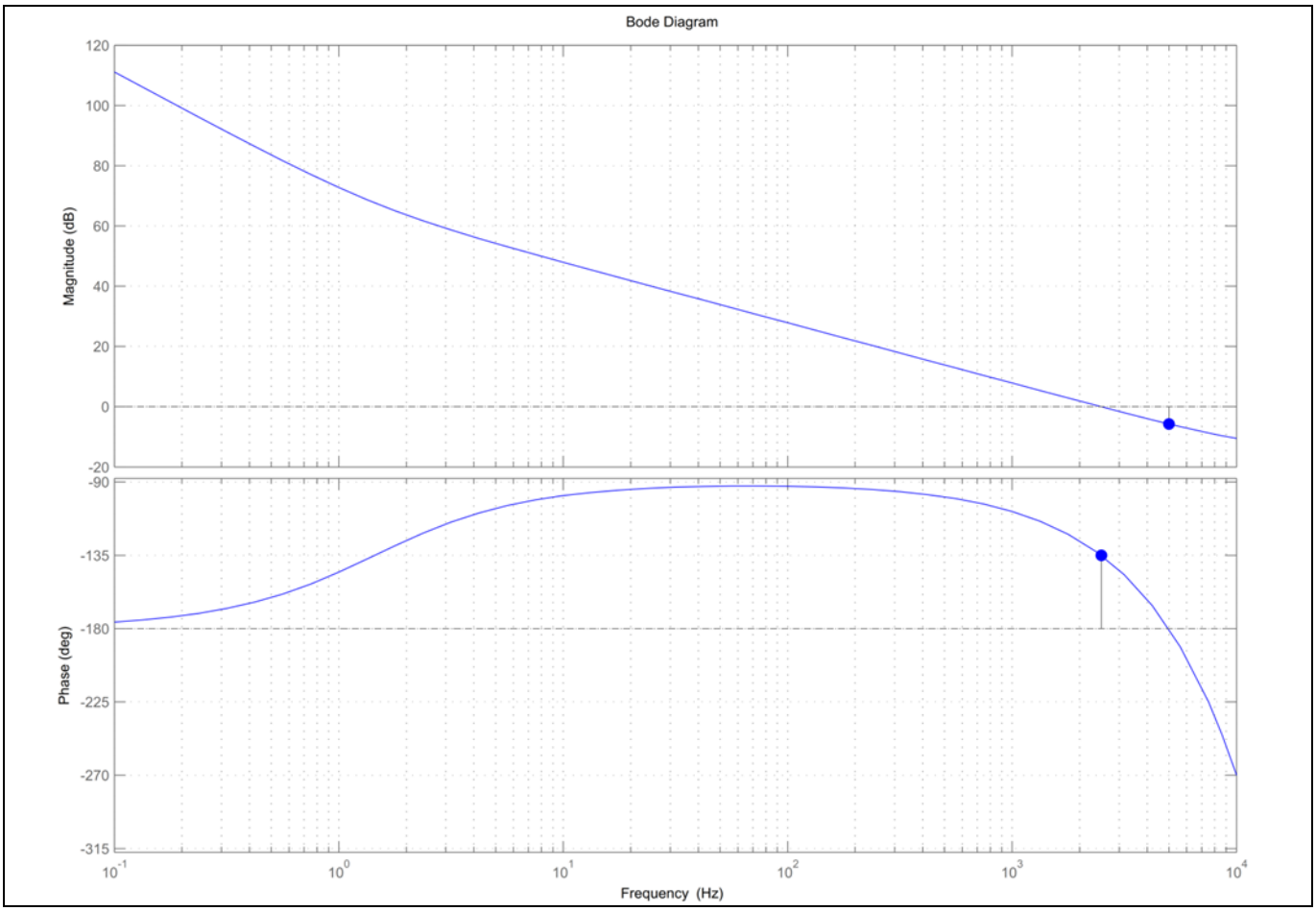


Figure 17 **Bode diagram of current control loop; fc = 2.5 kHz, PM (at fc) = 45°, gain margin (GM) = 5.72 dB**

4.4.2.2 Flow diagram

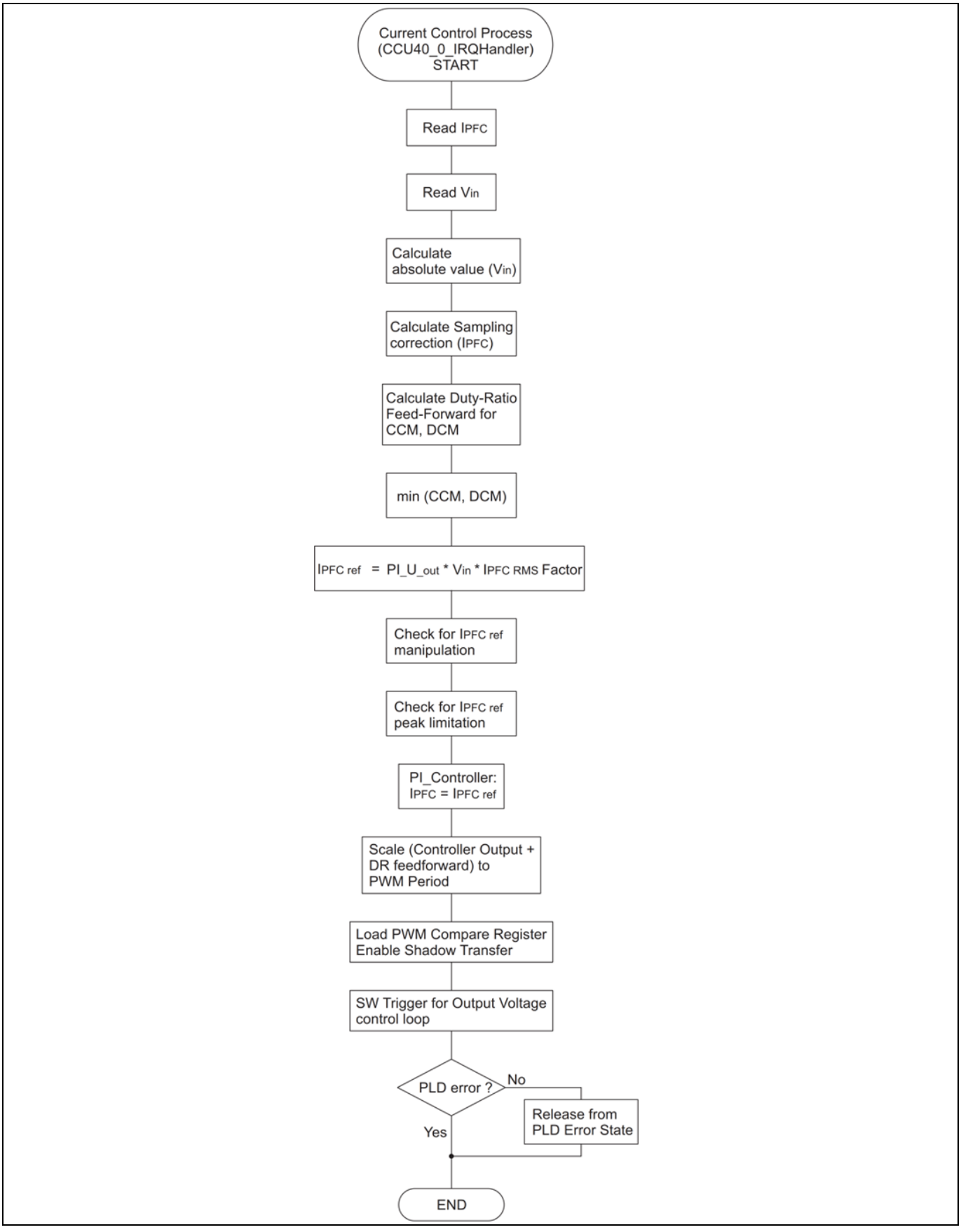


Figure 18 Current control loop flow diagram

Explanation of the flow diagram shown in **Figure 18** :

- Calculation of absolute value of V_{in}: The measured input voltage is a bipolar signal with the mean voltage (= 0 V) being at half (= 16384 at Q 0.15 format) of the measurement range. This value is transformed to a unipolar input value for PF control by means of subtracting half of the measurement range and calculating the absolute value.

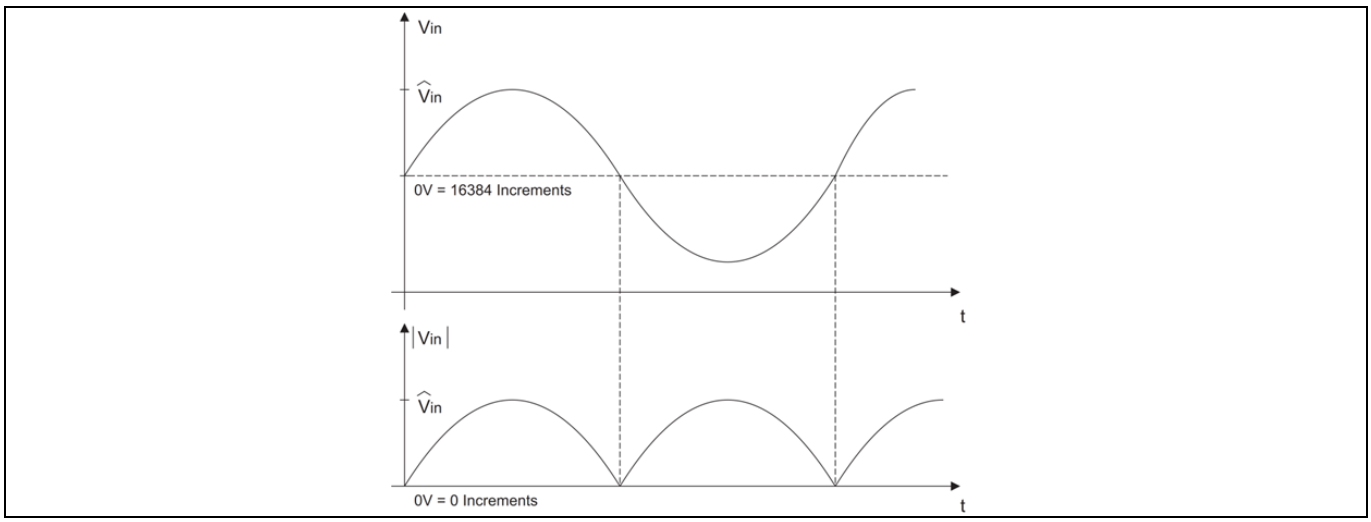


Figure 19 Transformation of the measured input voltage to a unipolar reference input signal

- Calculation of sampling correction: PWM operation is done with Slice0 of CCU4, which is configured for center-aligned PWM:

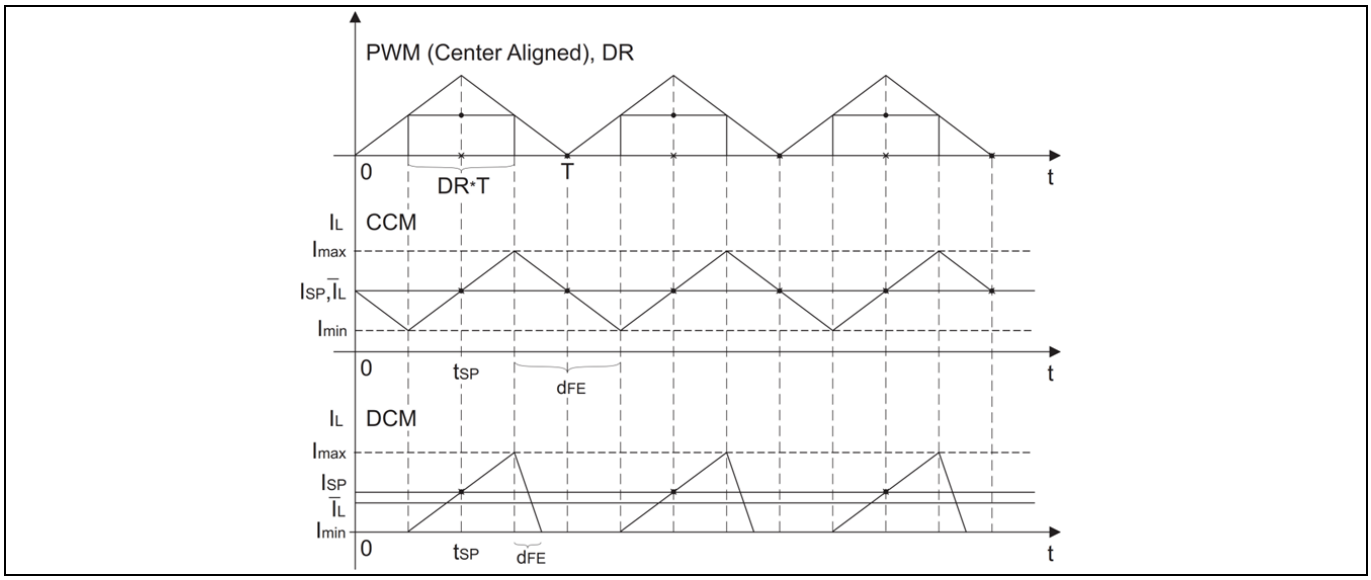


Figure 20 PWM sampling correction between CCM and DCM operation

According to the basic topology shown in **Figure 10**, the inductor current flows through different paths in the positive and negative AC semi-cycles with respect to the MOSFETs' on-state and off-state. To account for this, the average inductor currents are determined using two current transducers, both in the MOSFET on-state path, one for each semi-cycle. These current signals (transformer-ratio I_{prim}:I_{sec} = 50:1) are added together and transformed to a voltage by means of a shunt resistor (V_{Shunt} = (I_{sec_T1} + I_{sec_T2}) * R_{Shunt}). As can be observed in **Figure 20**, the average inductor current is evaluated from V_{Shunt} using the sampling point t_{SP} during the time where the current is rising. A correction due to the sampling of the inductor current is done afterward.

Table 5 Variables used in Figure 20

Nomenclature	Definition
$\bar{I}_L$	Average inductor current over one switching period
I_{SP}	Sampled inductor current by the microcontroller
t_{SP}	Time instant for inductor current sampling (= T/2)
T	Switching period (= 1/fsw)
DR	Duty ratio
PWM	Pulse width modulation
d_{FE}	Time for falling edge of the inductor current
CF	Sampling error correction factor
CCM	Continuous conduction mode
DCM	Discontinuous conduction mode
CrCM	Critical conduction mode
X’	Value X in the microcontroller with appropriate Q 0.15 format (= X/N_X)
N_X	Scaling factor of value X
$\bar{I}_{L_CF}$	Average inductor current over one switching period with sampling correction

The average inductor current for each of the three possible modes (CCM, DCM, CrCM) is:

$$\bar{I}_L = \frac{(I_{max} - I_{min})}{2} \cdot \left(\frac{DR \cdot T + d_F}{T}\right) \dots\dots\dots (1)$$

The sampled inductor current in the microcontroller is:

$$I_{SP} = \frac{I_{max} - I_{min}}{2} \dots\dots\dots (2)$$

From (1) and (2):

$$\bar{I}_L = I_{SP} \cdot \left(\frac{DR \cdot T + d_F}{T}\right) \dots\dots\dots (3)$$

In CCM and CrCM the switching period equals:

$$DR \cdot T + d_{FE} = T$$

And hence from (3): $\bar{I}_L = I_{SP}$. The sampled inductor current in the microcontroller equals the average inductor current over the switching period.

In DCM, the following equations are valid:

$$DR \cdot T + d_{FE} < T$$

And hence from (3): $\bar{I}_L < I_{SP}$

The sampled inductor current in the microcontroller is larger than the average inductor current over the switching period. The microcontroller over-estimates the average inductor current over the switching period. Therefore, in this mode there is a need for correction [3].

One can define the sampling error correction factor CF as:

$$CF = DR + \frac{d_{FE}}{T}$$

Re-writing equation (1):

$$\bar{I}_L = \frac{I_{max} - I_{min}}{2} \cdot CF$$

Considering that the average inductor voltage must be zero over one switching period, the sampling error correction factor can be calculated as:

$$CF = \frac{DR \cdot V_{out}}{V_{out} - V_{in}}$$

Multiplying the analog scaling factors N_{Vin} and N_{Vout} with V'_{in} and V'_{out}, respectively, yields the microcontroller equation for the correction of the sampled input current:

$$CF' = \frac{DR' \cdot V'_{out} \cdot N_{Vout}}{V'_{out} \cdot N_{Vout} - V'_{in} \cdot N_{in}} = \frac{DR' \cdot V'_{out}}{V'_{out} - V'_{in} \cdot \frac{N_{Vin}}{N_{Vout}}}$$

Finally, the sampled inductor current in the microcontroller can be corrected independently from the conduction mode by means of CF':

$$I'_{inCF} = I'_{SP} \cdot CF'$$

- Calculation of theoretical duty ratio (DR) for feed-forward in different modes (CCM, DCM).

For CCM:

$$DR_{CCM} = \frac{V_{out} \cdot V_{in}}{V_{out}} = 1 - \frac{V_{in}}{V_{out}}$$

The value in the microcontroller is:

$$DR_{CCM}' = 1 - \frac{V'_{in} \cdot N_{Vin}}{V'_{out} \cdot N_{Vout}}$$

For DCM:

$$DR_{DCM} = \sqrt{2G_e \cdot L \cdot f_{SW} \cdot \frac{(V_{out} - V_{in})}{V_{out}}} = \sqrt{2G_e \cdot L \cdot f_{SW} \cdot DR_{CCM}}$$

where

$$G_e = \frac{P_{in}}{V_{in\ RMS}^2} \approx \frac{PI_V_out' \cdot N_{Vin} \cdot N_{Iin}}{V_{in\ RMS}^2}$$

and defining

$$DCM_Factor' = \frac{2 \cdot N_{vin} \cdot N_{Iin} \cdot L \cdot f_{SW}}{V_{in\ RMS}^2}$$

Then the value in the microcontroller is:

$$DR_{DCM}' = \sqrt{PI_V_out' \cdot DCM_factor' \cdot DR'_{CCM}}$$

- Use the minimum DR in CCM and DCM for feed-forward: As the valid theoretical DR in the present mode is always the minimum of both modes, parallel computation and the minimum can be used for DR-feed-forward instead of determining the valid mode.
- Calculation of **IPFC reference**: The factor **IPFC RMS** contains the RMS input voltage feed-forward and, if necessary, the RMS input current limitation.
- Check for **I PFC reference manipulation**: According to an output voltage drop, the input current reference value may be doubled for faster transient behavior due to load-steps.
- Check for **I PFC peak limit**: The maximum input current reference of 25 A may not be exceeded.
- Set software trigger for doing the output voltage control loop:

$$f_{Output\ \ Voltage\ \ Control\ \ looop} = \frac{f_{Input\ \ Current\ \ Control\ \ looop}}{12} = \frac{30kHz}{12} = 2.5kHz$$

- Check for PLD: To release control from PLD error state, it is checked whether V_{in} is greater than 40 V AC and the condition $V_{out} - V_{in} > 50$ V holds. These conditions must be calculated 10 times in a row to be true.

4.5 Background calculations

The Sys Tick timer process is used for all non-time-critical (background) calculations.

4.5.1 System Tick timer process

This process is configured to be executed every single millisecond (f_{call} = 1 kHz).

4.5.1.1 Flow diagram



Figure 21 System Tick process flow diagram

Explanation of the flow diagram shown in **Figure 21**:

- **Relay control**: The relay is switched on 200 ms after the 5 V DC supply voltage of the microcontroller is in range.
- **PFC states**: For output voltage and input current control, a valid range of the input voltage and no active error conditions are necessary.
- **PFC steady-state**: DR feed-forward is active in steady-state only.
- Calculation of **mean input power/tuning of control parameters**: This is utilized for tuning the control parameters of the input current error amplifier according to the actual power and input voltage conditions.
- Determine **heatsink (HS) temperature**: The voltage divider curve from the NTC sensor is saved in a table to deliver the present HS temperature.
- **Fan control**: The fan speed is controlled by setting the fan voltage according to the measured temperature of the HS and the following regime:

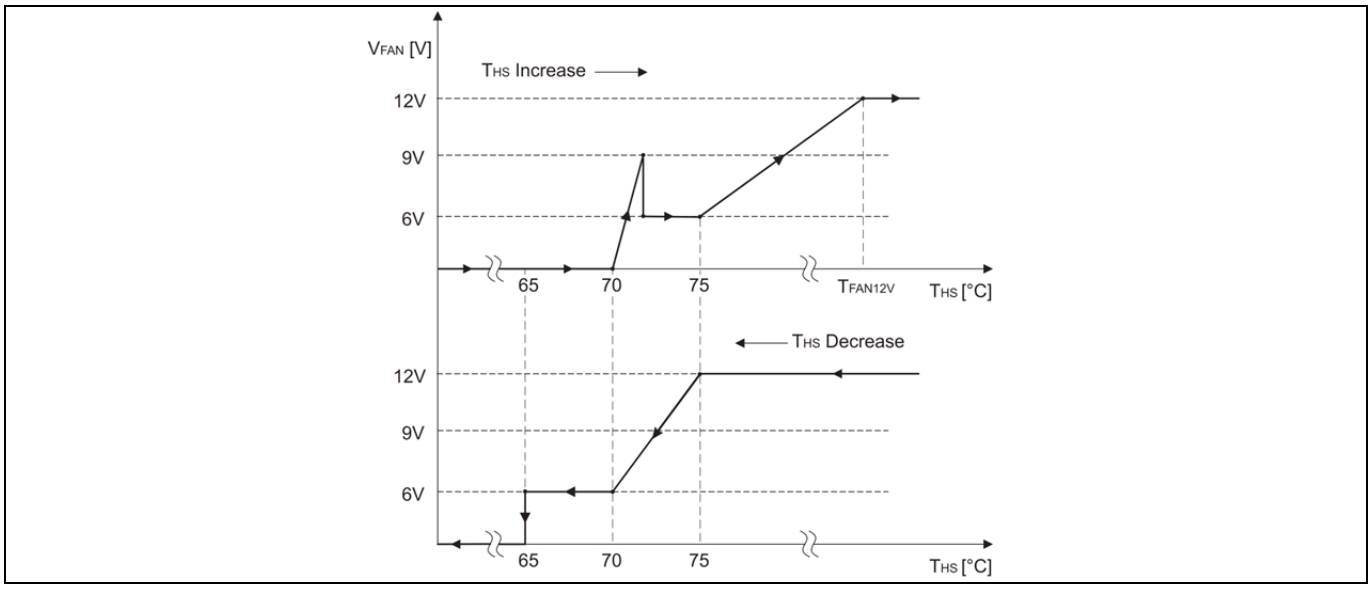


Figure 22 Fan voltage (speed) according to the temperature of the HS

The fan is switched on if the HS temperature is higher than 70°C. This is done with a voltage-ramp, starting from zero up to 9 V within 2 seconds (fan's specification). Afterward, the fan voltage is reduced to its steady-state value of 6 V.

The fan voltage is the output of an I-type-control with an HS temperature reference of 75°C and an integral time-constant of 1 second. The upper limit of the fan voltage is 12 V in case the steady-state HS temperature exceeds 75°C. The lower limit is 6 V DC in case the steady-state HS temperature drops below 75°C. A stationary fan voltage in the range of 6–12 V DC for an HS temperature of 75°C depends on the output power of the converter and the cooling conditions.

If the HS temperature drops below 70°C, the fan voltage is set to its steady-state value of 6 V DC instead of being temperature controlled. The fan is switched off if the HS temperature is lower than 65°C.

- Calculation of **mean output power (MOP)**: The filtering of the voltage controller output is used to get a measurement for the MOP. This is used for manipulation of the input current reference value.

4.6 Analog measurement ranges and hardware filtering

All analog input values are filtered using low-pass filters of first-order type (time-constant T).

Table 6 Analog measurement ranges

Analog input	Value	Time constant
Inductor current for input current control	0–37.5 A	100 ns
Inductor current trap-limit	41.25 A	100 ns
Inductor current cycle-by-cycle-limit	32.7 A	100 ns
Input voltage	0–469.44 V	220 ns
Output voltage	0–449.74 V DC	188 µs
Output voltage trap-limit	495 V DC	188 µs
HS temperature (NTC)	18–111°C	100 µs

4.7 Limits and protections

4.7.1 Hardware

- Trap: The trap functionality of the CCU4 peripheral (slice 1) is used to provide protection to the PFC demo board in the fastest possible way. An active trap condition immediately switches off the PWM signal and brings the PFC into the inactive state. The trap signal is generated by the in-built over range comparators (ORC) in the input current and the output voltage paths, respectively: trap active: I_in > 41.25 A or V_out > 495 V DC
- The trap-state is irreversible and can only be overcome by a power-on reset of the PFC demo board.
- Cycle by cycle (CBC) limit: The external modulation functionality of the CCU4 peripheral (slice 1) is used to peak-limit the input current during each switching period. The level is set by using the analog comparator 0 (ACMP0): CBC limit active: I_in > 32.7 A. The CBC state is reset by hardware at the end of the switching period.

4.7.2 Software

- Peak limit of input current reference (ICR): The software limits the maximum peak ICR to 25 A in the normal operating mode (sinusoidal input current) and in the mode where the ICR is doubled (non-sinusoidal input current). This accounts for a faster transient behavior in case of load-steps where the nominal input current of 15 A_{RMS} can shortly be exceeded.
- RMS limit of ICR: The software limits the RMS ICR to 15 A in case the RMS-value of the input voltage drops below 195 V AC. This is not valid for higher input voltages during a 5-second period caused by ICR doubling. The DC-link voltage will drop in case this protection is active.
- Peak limit of measured output voltage: The PFC is set to inactive state in case a value of more than 425 V DC is measured.
- Temperature: The converter is protected against overtemperature conditions caused by loss of fan cooling or excessive ambient temperature, which could cause failures of internal parts. The converter shuts down when the temperature monitored on the HS exceeds 93°C. This is latching-type protection.
- Brown-out: The converter has brown-out protection. The turn-on input voltage is 85 V AC. The turn-off input voltage is 65 V AC.
- Output power: There is protection for the output power, limiting the output power to 3278 W. The DC-link voltage will drop in case this protection is active.

4.8 Signaling

Three LEDs on the digital control board indicate operating conditions and errors:

- When the orange LED is fully on then it indicates the presence of Vin_range at the input (LED is on if V_{inRMS} > 85 V AC, LED is off if V_{inRMS} < 65 V AC).
- A blinking orange LED indicates the occurrence of an input current trap (fast blinking) or an output voltage trap (slow blinking).
- The green LED indicates the presence of Vout_range at the output (LED is on in the range 370 V DC < V_{out} < 410 V DC).
- A blinking red LED indicates that the XMC 1302 microcontroller is up and running.
- When the red LED is fully on this indicates an active overtemperature protection (THS > 93°C).

5 ICE2QR4780Z controller for the auxiliary converter

5.1 Input and output requirements

The voltage needed to supply the control circuitry and the fan is provided by the dedicated flyback DC-DC converter ICE2QR4780Z, which is assembled on the power board. The DC-link voltage supplies this converter.

Table 7

Parameter	Value
Input voltage range, $V_{aux_in_range}$	125–450 V DC
Nominal primary output voltage, V_{aux_pri}	12 V DC +/- 10 percent
Nominal secondary output voltage, V_{aux_sec}	12 V DC +/- 10 percent
Maximum output power, P_{aux_out}	6 W

5.2 Flyback transformer

The transformer design is based on a gapped ferrite core EE 16/8/5 with a horizontal bobbin. The total air gap is 0.2 mm. The selected core material is TDK N87 or equivalent.

The turn ratio is 184:15:15, resulting in 150 V (approximately) reflected primary transformer voltage.

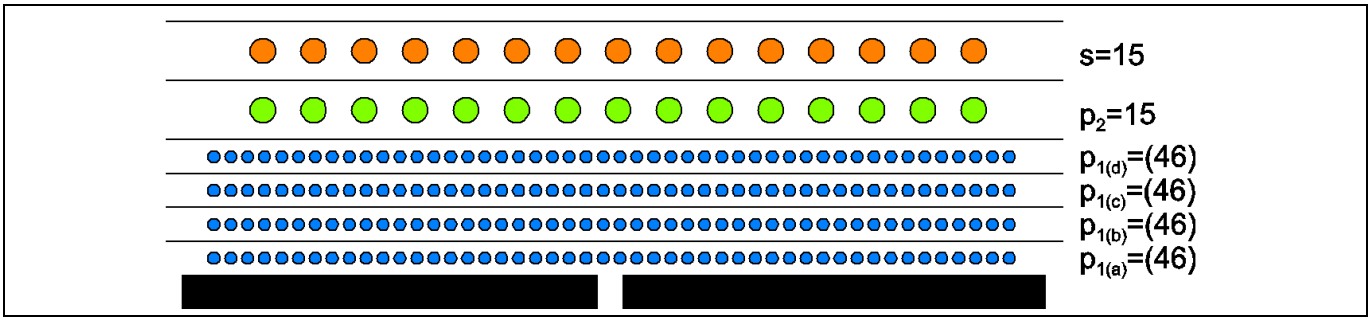


Figure 23 Winding arrangement

The secondary winding (S) has safety insulation from the primary side, which is implemented using triple-insulated wire. The other windings are made of standard enameled wire. The HV primary winding (P1) is split into four layers.

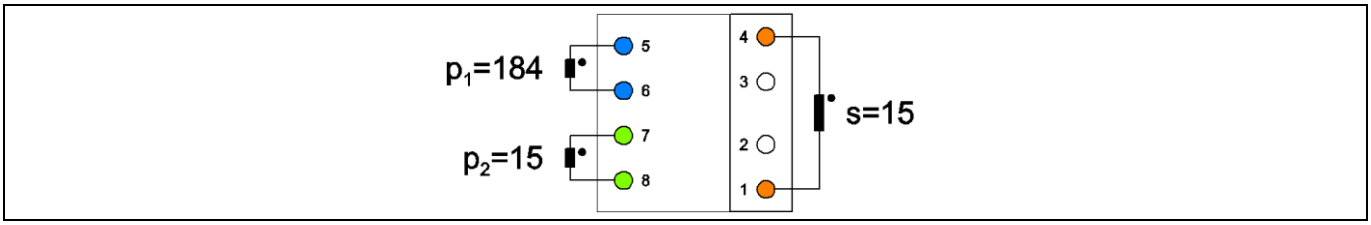


Figure 24 Pin arrangement, top view

5.3 Swiching frequency

The ICE2QR2280Z is a QR PWM controller with integrated 800 V CoolMOS™. The switching frequency depends on load power and input voltage, and is between 37 kHz and 125 kHz.

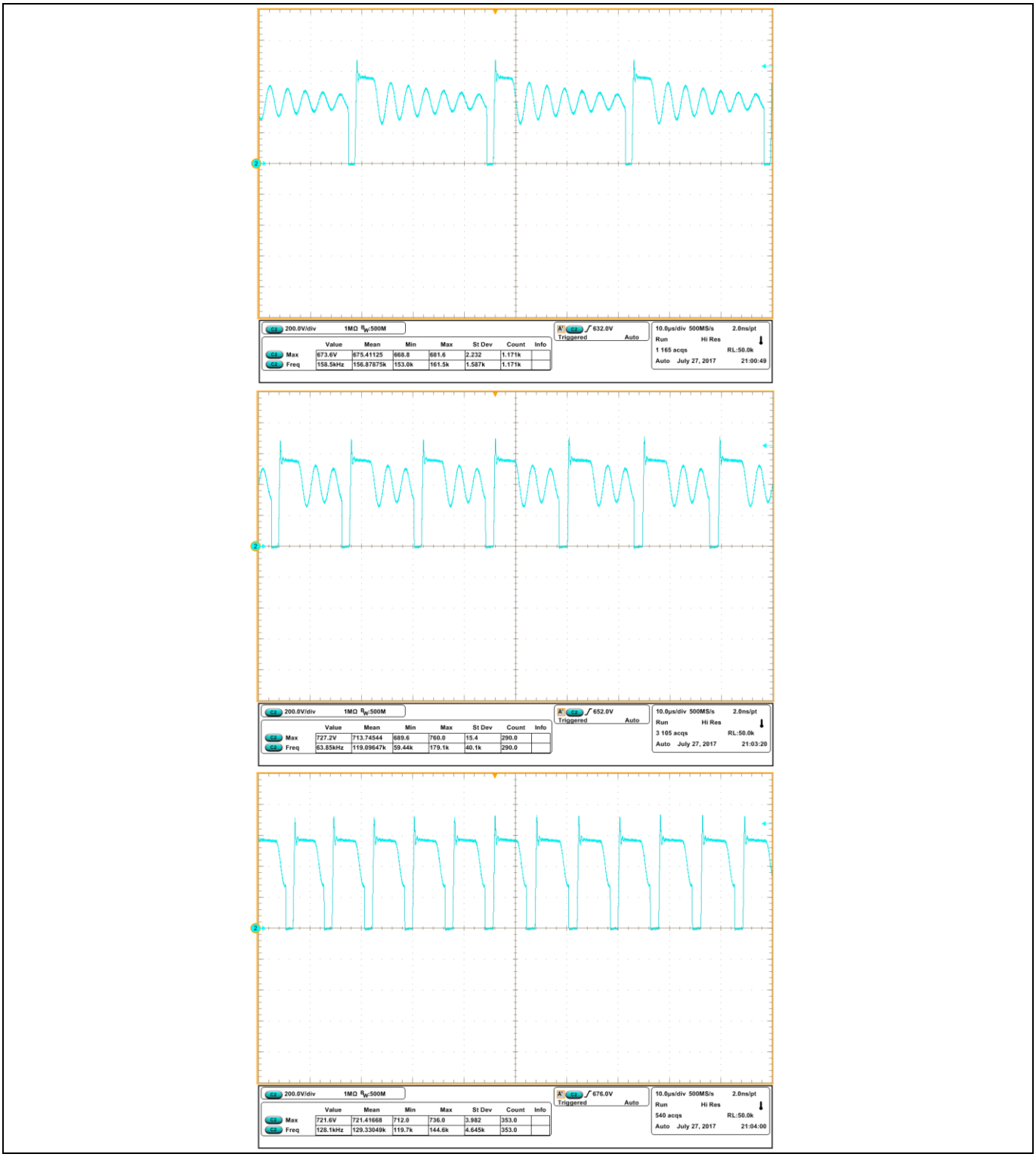


Figure 25 Drain-to-GND waveforms of the auxiliary power supply.
Top: Demo board running at light load and fan not running
Middle: Demo board running at mid load and the fan at a certain speed
Bottom: Demo board running at full load and fan at full speed

6 Experimental results

6.1 Efficiency, PF and THD measurements with 650 V CoolMOS™ C7

Efficiency measurements were carried out with a WT3000 Yokogawa Precision Power Analyser registering 5-minute load-steps. Losses of the EMI and output filter are included. The fan was supplied from an external +12 V voltage source. Worth noting are the efficiencies at half- and full-load at both low-line (power derated to 1.3 kW) and high-line (nominal rated power of 3 kW).

Table 8 Measurements at V_{in_AC} = 115 V AC at P_{out} = 1.3 kW

P_{out_load} (%)	V_{in_AC} (V)	I_{in_AC} (A)	P_{in} (W)	V_{out} (V)	I_{in} (A)	P_{out} (W)	η (%)
10	115.45	1.18	133.63	399.87	0.32	127.45	95.37
20	115.39	2.39	273.56	399.89	0.66	263.78	96.43
30	115.32	3.48	400.52	399.95	0.97	389.04	97.13
40	115.26	4.69	539.00	399.85	1.31	525.26	97.45
50	115.19	5.80	666.78	399.85	1.63	650.26	97.52
60	115.13	6.92	795.45	399.88	1.94	775.38	97.48
70	115.07	8.14	935.79	399.84	2.28	911.75	97.43
80	115.01	9.28	1065.69	399.84	2.59	1036.81	97.29
90	114.95	10.52	1207.67	399.79	2.93	1173.11	97.14
100	114.89	11.67	1338.68	399.80	3.25	1298.11	96.97

Table 9 Measurements at V_{in_AC} = 230 V AC at P_{out} = 3 kW

P_{out_load} (%)	V_{in_AC} (V)	I_{in_AC} (A)	P_{in} (W)	V_{out} (V)	I_{out} (A)	P_{out} (W)	η (%)
10	230.89	1.35	305.24	399.86	0.75	297.92	97.60
20	230.82	2.68	615.01	399.82	1.51	604.77	98.34
30	230.76	3.97	914.05	399.81	2.25	900.59	98.53
40	230.70	5.27	1213.07	399.81	2.99	1196.05	98.60
50	230.63	6.61	1523.35	399.77	3.76	1502.14	98.61
60	230.57	7.92	1823.71	399.75	4.50	1797.61	98.57
70	230.49	9.27	2135.82	399.74	5.26	2104.01	98.51
80	230.43	10.58	2437.29	399.73	6.00	2399.20	98.44
90	230.36	11.95	2750.84	399.72	6.77	2705.42	98.35
100	230.29	13.26	3053.44	399.71	7.51	2999.92	98.25

For the sake of comparison and confirmation of the advantage of using 4-pin devices in terms of efficiency, the 650 V CoolMOS™ C7 45 mΩ in standard TO-247 packages can be also plug-and-play tested. The results are shown in **Figure 26**. One should be aware that the parasitic inductance of the source leads into the gate-driving circuitry, so the turn-off voltage spike in the drain-to-source voltage waveform needs to be carefully monitored, especially at low-line input voltages, e.g., V_{in_LL} = 90 V AC. For this reason, the gate turn-off resistor must be changed and carefully selected. Similarly, the PF and iTHD must also be monitored during this process.

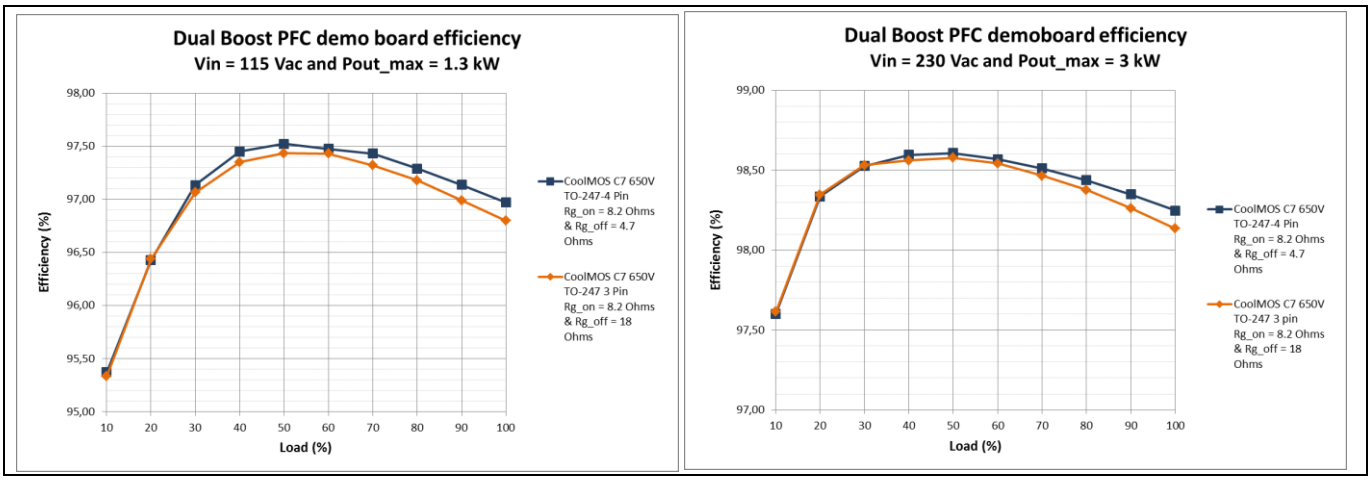


Figure 26 **Low- and high-line efficiency using 650 V CoolMOS™ C7 45 mΩ in TO-247 4-pin with R_{g_on} = 8.2 Ω and R_{g_off} = 4.7 Ω vs TO-247 with R_{g_on} = 8.2 Ω and R_{g_off} = 18 Ω**

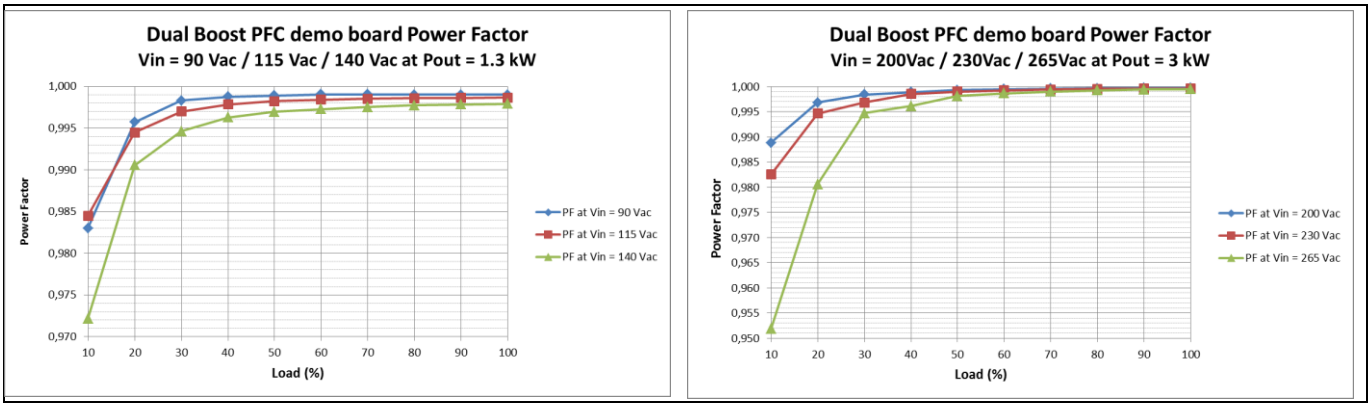


Figure 27 **PF at different low- and high-line input voltages using TO-247 4-pin devices only**

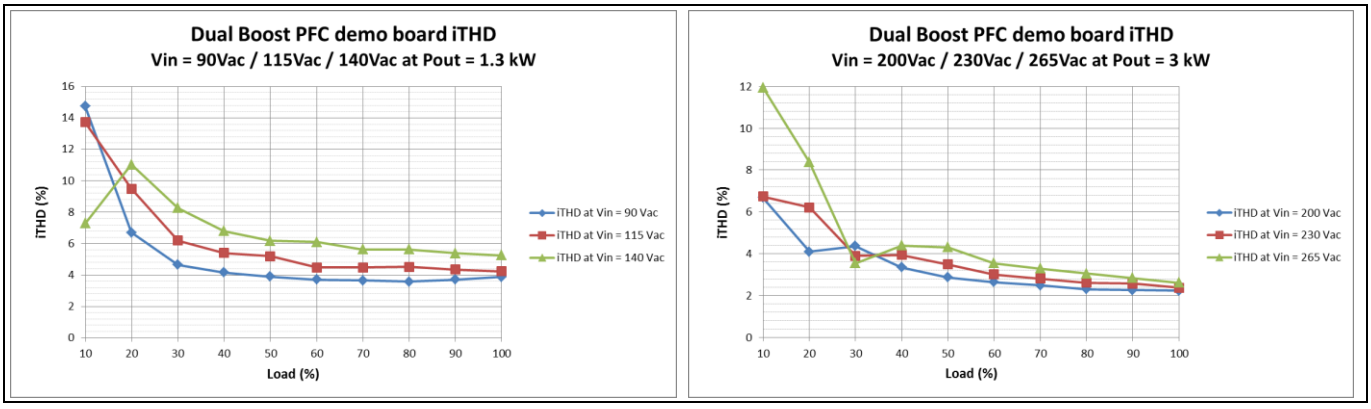


Figure 28 **Input current THD at different low- and high-line input voltages using TO-247 4-pin devices only**

6.2 Efficiency comparison with the latest 600 V CoolMOS™ P7 and competitors' TO-247 4-pin MOSFETs

In order to demonstrate the attractive performance of CooMOS™ C7 and P7, additional efficiency **plug-and-play** tests can be made on the demo board with different TO-247 4-pin devices from closest competitors' $R_{DS(on)}$ MOSFETs.

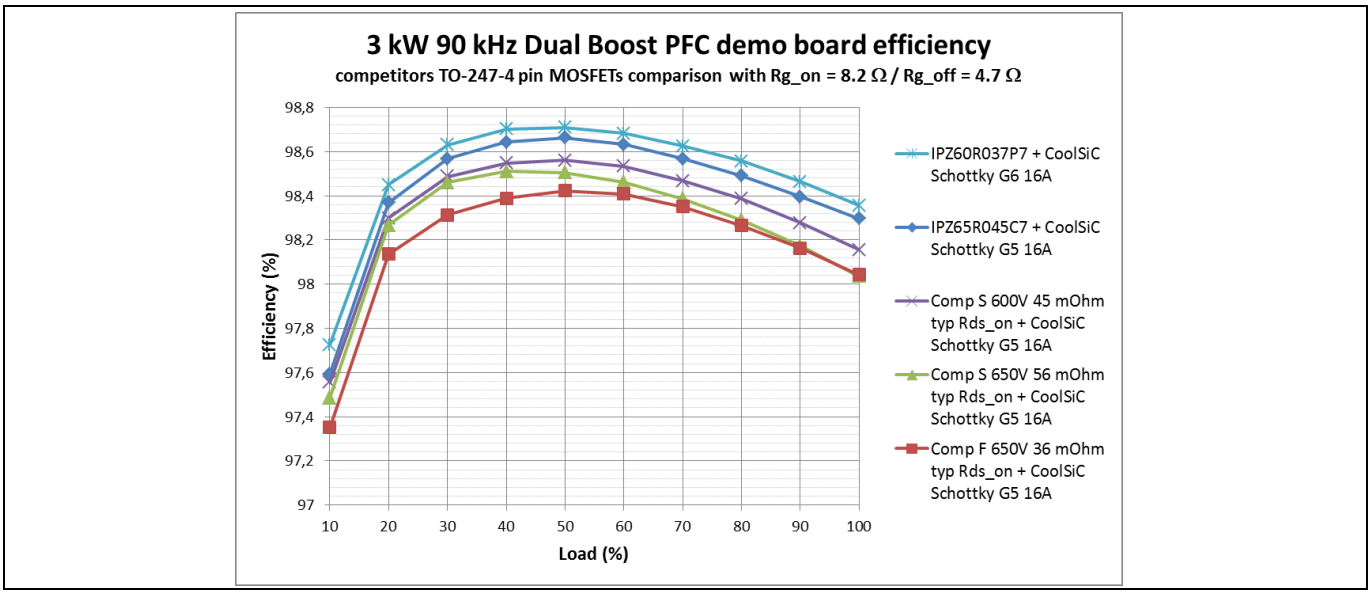


Figure 29 Efficiency comparison when V_{in} = 230 V AC among different TO-247 4-pin MOSFETs from closest competitors' $R_{DS(on)}$ MOSFETs

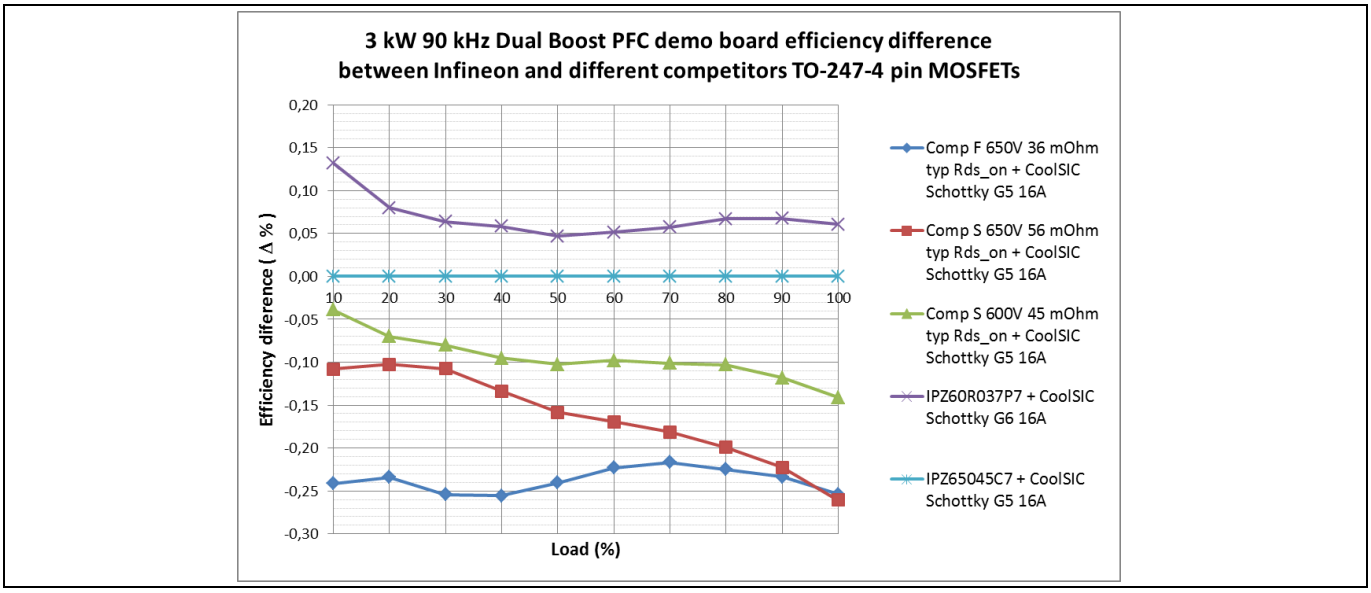


Figure 30 Efficiency difference when V_{in} = 230 V AC among different TO-247 4-pin MOSFETs from closest competitors' $R_{DS(on)}$ MOSFETs

As can be appreciated in **Figure 29** and **Figure 30**, the latest price–performance combination offer of 600 V CoolMOS™ P7 plus CoolSiC™ Generation 6 diodes gives the highest performance among the different tested solutions: around 0.15 percent efficiency difference at half-load compared to the closest competitor and around 0.2 percent more efficient at full-load compared to the closest competitor's device.

6.3 Standby power consumption

Measurements performed with a WT330 Yokogawa digital power meter showed the following results for standby real power consumption of the demo board at no load:

Table 10

V_{in} = 115 V AC	V_{in} = 230 V AC
I_{in} < 160 mA_{RMS}	I_{in} < 300 mA_{RMS}
P_{in} < 7.8 W	P_{in} < 7.4 W

6.4 Efficiency versus MOSFET stress

During the design process, there is always a trade-off between achieving high efficiency and semiconductor stress if the derating guidelines of the IPC 9592 standard are to be fulfilled. This stress depends on drain current, drain-to-source voltage, stray inductances of the package and PCB as well as the switching speed (di/dt). Depending on the requirements of the application, the designer can select the proper value of turn-on and turn-off gate resistors to achieve certain efficiency at a certain stress on the MOSFET.

The design for this board is aimed at achieving high efficiency by having very low switching losses in the MOSFETs. This is achieved by using:

- Very low turn-off resistors for each of the MOSFETs, with a value of 4.7 Ω. Compared to previous CoolMOS™ technologies, the 650V CoolMOS™ C7 technology keeps the drain-to-source voltage below the 80 percent derating factor during normal operation, i.e. < 520 V DC.
- If 600V CoolMOS™ P7 technology is decided to be evaluated by using the same turn-off resistor as mentioned above, be aware that the drain-to-source voltage is below the 90 percent derating factor during normal operation, i.e. < 540 V DC. If such value is not allowed then the turn-off resistor must be increased to the proper value.
- The TO-247 4-pin package, which allows clean PWM signals to the gate pin as the driver is referenced to the driver source (or Kelvin source) pin.

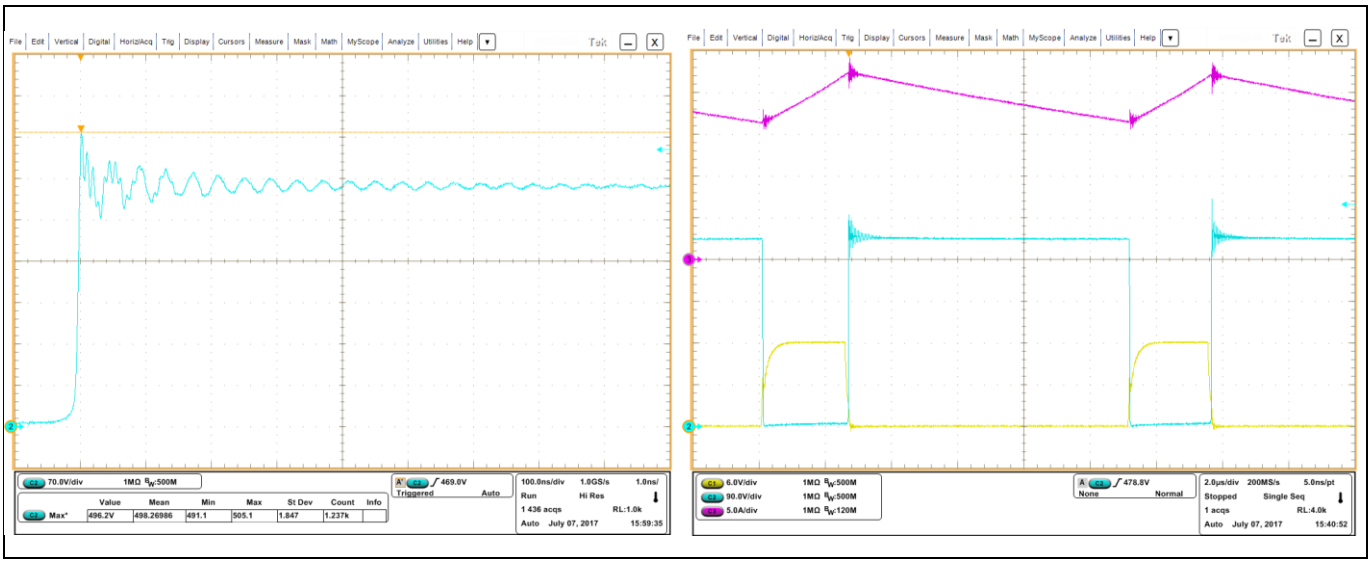


Figure 31 **Left: Drain-to-source voltage waveform at turn-off with a peak voltage within the 20 percent derating limits**
Right: Gate-to-driver source voltage waveform (yellow), drain-to-driver source voltage waveform (cyan) and inductor current (magenta)

Higher efficiencies are possible by lowering the values of the turn-off gate resistors. However, the drain-to-source peak voltages as well the conducted EMI signals may exceed the allowed limits of the converter design. The designer must be aware of such limits during both steady-state and abnormal (AC-line drop-out or start-up) conditions.

6.5 Load-jumps

Key to the following figures:

- CH 2 (blue): PFC output voltage (with an offset of 300 V DC)
- CH4 (green): Load current

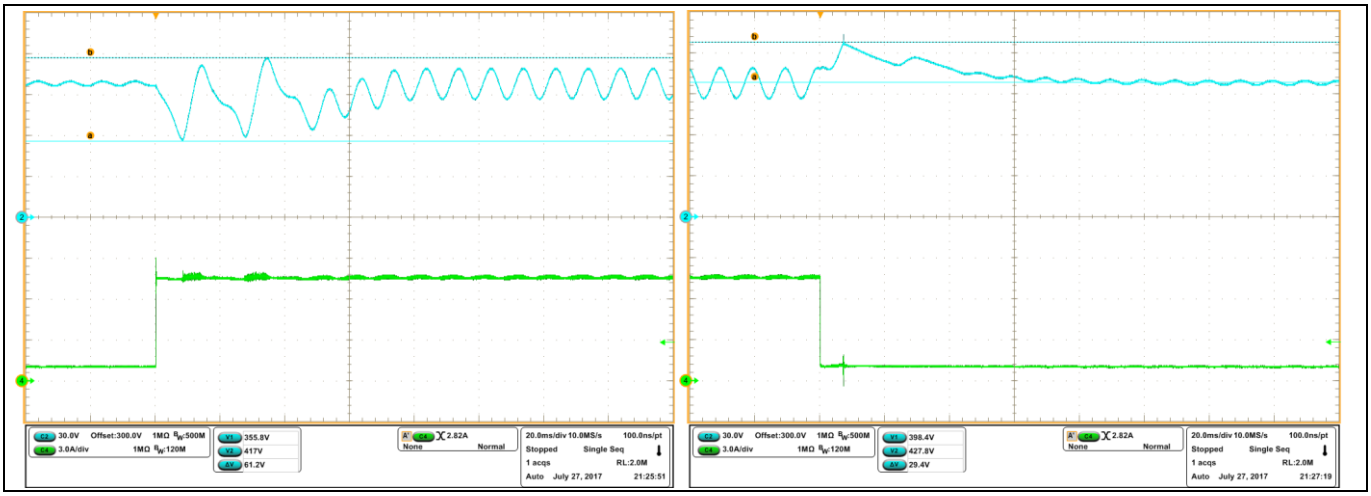


Figure 32 **Left: 1 A ➔ 7.5 A load-step; Right: 7.5 A ➔ 1 A load-step**

Figure 32 illustrates the response of the PFC converter during a load-step from light load to full load and vice-versa. In the first case, after sudden load demand, the minimum undervoltage is around 355 V DC and the maximum overshoot is around 417 V DC. In the second case, after sudden load release, the maximum overshoot is around 427 V DC. In both cases, the PFC controller returns to proper regulation in around 80 ms.

6.6 Start-up

The dual-boost PFC demo board has circuitry to limit the turn-on inrush current to around 35 A_{peak}. Around 600 ms after powering up the system, the auxiliary supply will start-up and provide 12 V. Once all circuits are powered and the input voltage is higher than the brown-out threshold, then the microcontroller starts operating. The NTC limiter is then bypassed by the relay, and this effect can be clearly seen in Figure 33 as a slight increase in the PFC output voltage and the increase of the non-PF-corrected input current. As the microcontroller starts from zero, once it detects sufficient input current it starts to ramp up the output voltage to the desired set-point, 400 V DC. At this moment, the input current starts to become sinusoidal and PF-corrected. The duration from the moment the relay is fully on to the boosting of the output voltage differs according to the input voltage as well as the load conditions.

Key to the following two figures:

- CH 2 (blue): PFC output voltage
- CH 3 (magenta): 12 V DC from the auxiliary supply
- CH 4 (green): Input current

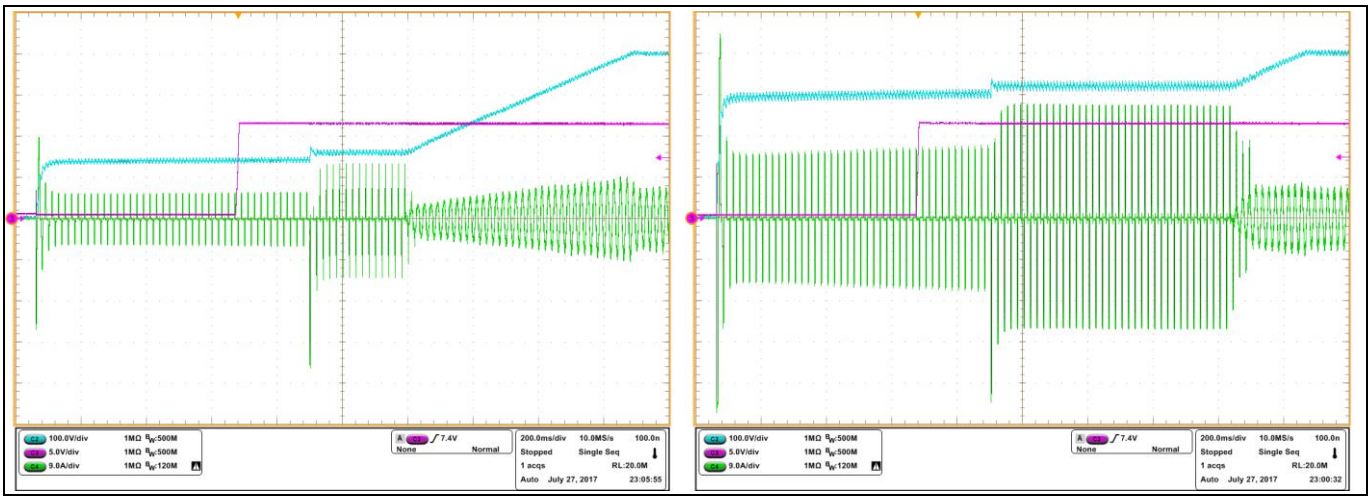


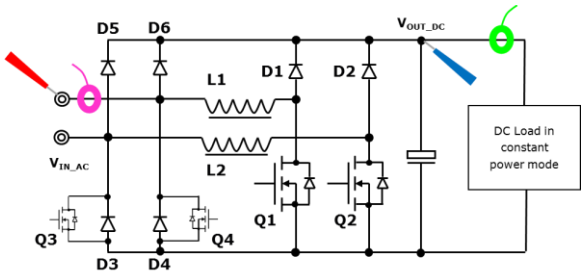
Figure 33 Left: Start-up at V_{in} = 115 V DC with a 500 W load; Right: Start-up at V_{in} = 230 V DC with a 1 kW load

6.7 AC-line drop-out

To demonstrate the robustness of the hold-up time design of the dual-boost PFC demo board, AC Line Drop Out (ACLDO) events can be tested in the worst operating conditions, i.e. no AC voltage from the grid during 10 ms happening at 90° or 270°, and using a DC electronic load demanding full load at constant power.

Key to the following two figures:

CH 1 (blue)	Output voltage of the dual-boost PFC converter with an off-set of 300 V DC
CH 2 (red)	Input voltage of the dual-boost PFC converter
CH 3 (pink)	Input current of the dual-boost PFC converter using a 50 V/A current probe
CH 4 (green)	Output current of the dual-boost PFC converter



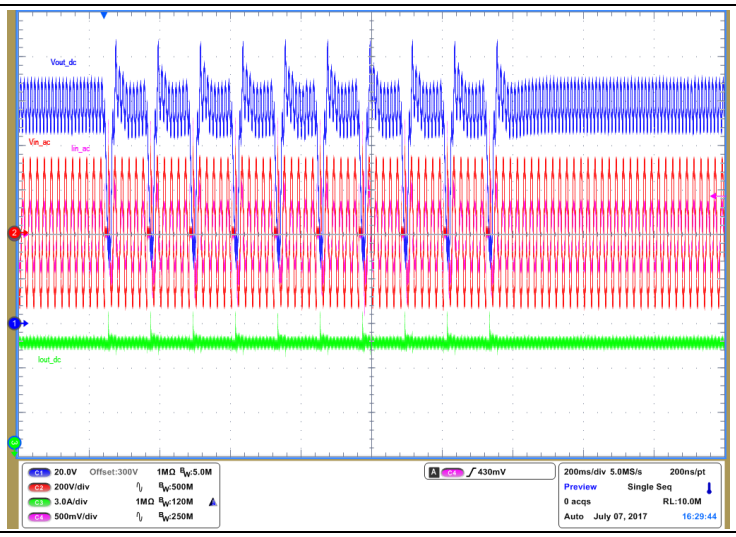


Figure 34 10 x 10 ms ACLDO events when V_{in} = 230 V AC at P_{out} = 3 kW

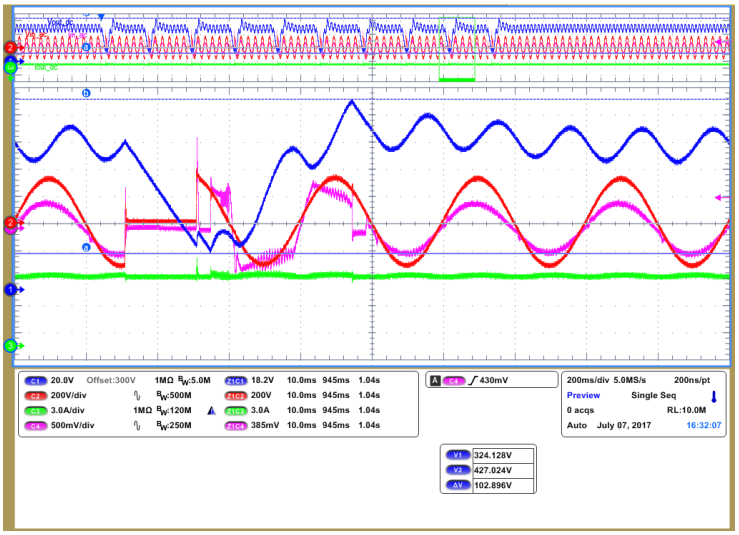


Figure 35 Detail of one of the ACLDO events when V_{in} = 230 V AC at P_{out} = 3 kW

As can be seen in **Figure 34**, the dual-boost PFC converter maintains error-free operation when subjected to the ten ACLDO events. Worth noting is that during this time-slot the ouput current is regulated even when the output voltage drops considerably but within the permited limits. After PLD, the dual-boost PFC converter maintains normal operation.

Figure 35 is a detail of one of these events. The ACLDO event (red) happens at 270°C with a black-out of 10 ms, coming back at the most critical point, i.e. 90°, when the input current has its highest value. During this black-out, the output voltage can drop to a voltage higher than the 320 V limit (as stated in **Table 1**), which is sufficient to keep an LLC or a ZVS phase shift full bridge (PSFB) converter working at the rated load. When the AC-line voltage returns, the PFC controller boosts in current limit operating mode. This results in the sinusoidal truncated input current waveform (pink). When the output voltage reaches the minimum output OV threshold limit (as stated in **Table 2**), the PFC controller turns off immediately in order to avoid a higher output voltage than expected. Once the output voltage is within the regulation limits, the PFC controller starts regulating normally again within 3 AC cycles.

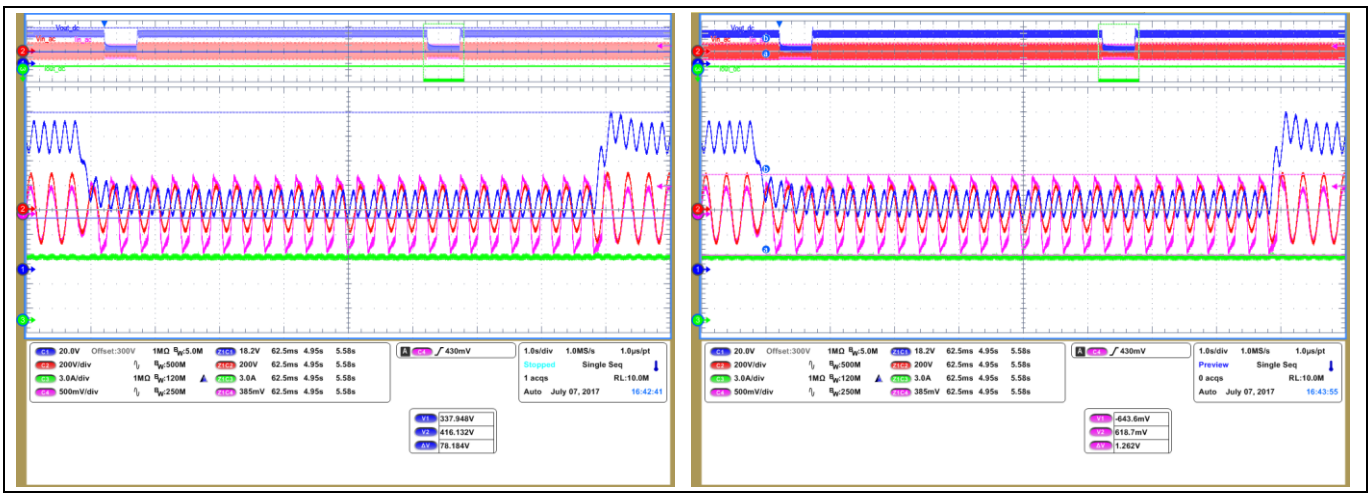


Figure 36 500 ms voltage dips with a voltage decrease to 130 V AC

Figure 36 shows other PLD events, commonly known as voltage dips or sags. In this particular case, the input voltage decreases to 130 V AC in 500 ms. As the graph on the left shows, the output voltage of the dual-boost PFC converter drops to a minimum value of around 338 V DC, but is still higher than the hold-up time output regulation limit. Once the voltage dip or sag is over, the OV seen at the output voltage is around 416 V DC, which is well below the minimum output OV threshold limit.

As can be seen on the right-hand side of **Figure 36**, during this voltage dip or sag there is more current demand on the input of the converter. As a result, the PFC controller works in current limit operation mode in order to maintain constant power at the load. This is shown by the sinusoidal truncated waveform (pink). The maximum peak current during this event, considering the 50 V/A current probe and the peak-to-peak voltage of 1.262 V (from **Figure 36**) is 50 (V/A) x 1.262/2 (V) = 31.55 A.

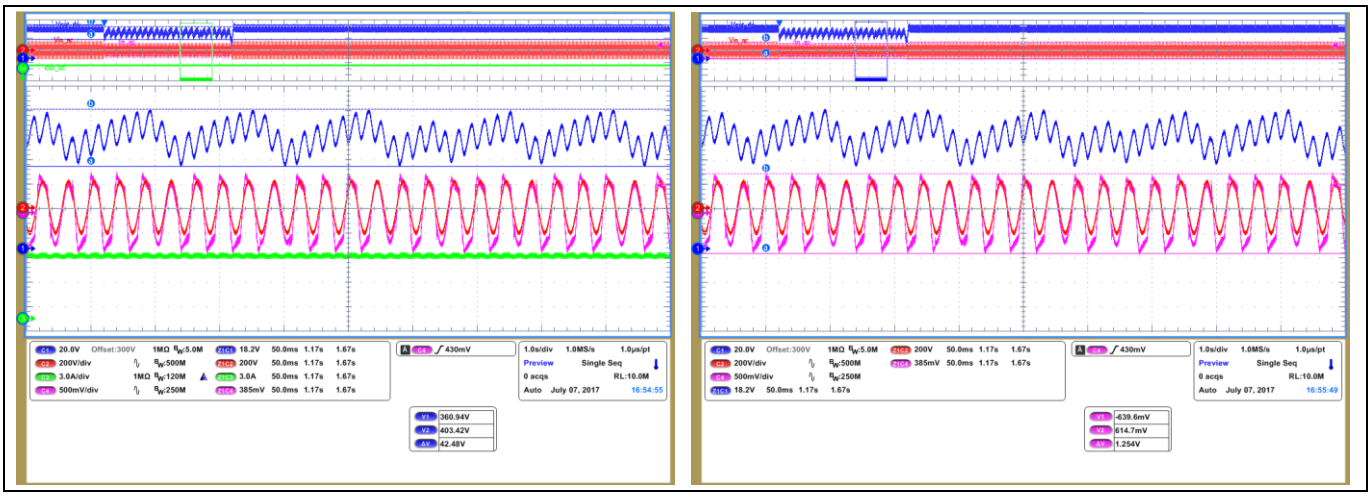


Figure 37 2 s voltage dip with a voltage decrease to 150 V AC

Figure 37 depicts another voltage dip or sag event. In this case, the input voltage decreases to 150 V AC in 2 seconds. As the left-hand image shows, the output voltage (blue) varies from 360 V DC to 403 V DC. This wide variation is due to the fact that the PFC controller tries to keep a constant current (green) at the output at a reduced input voltage while maintaining the current limit operation of the dual-boost PFC converter below the maximum peak current limit of 32 A, as seen in the right-hand image.

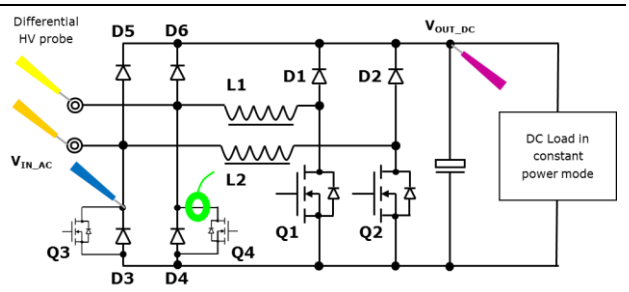
After the sag events shown in **Figure 36** and **Figure 37**, the demo board maintains error-free operation, which is a feature demanded by all PFC converters in server, telecom and industrial applications.

6.8 Surge test

To demonstrate the reliability of the topology when active rectification is employed, 1 kV and 2 kV line-to-neutral surge pulse tests at the input can be run on the demo board to verify the stress on the actual active rectification MOSFETs Q3 and Q4.

Key to the following two figures:

CH 1 (yellow)	Input voltage of the demo board
CH 2 (blue)	Drain-to-source voltage of the active rectification MOSFET Q3
CH 3 (magenta)	Output voltage of the demo board
CH 4 (green)	Drain current through the active rectification MOSFET Q4



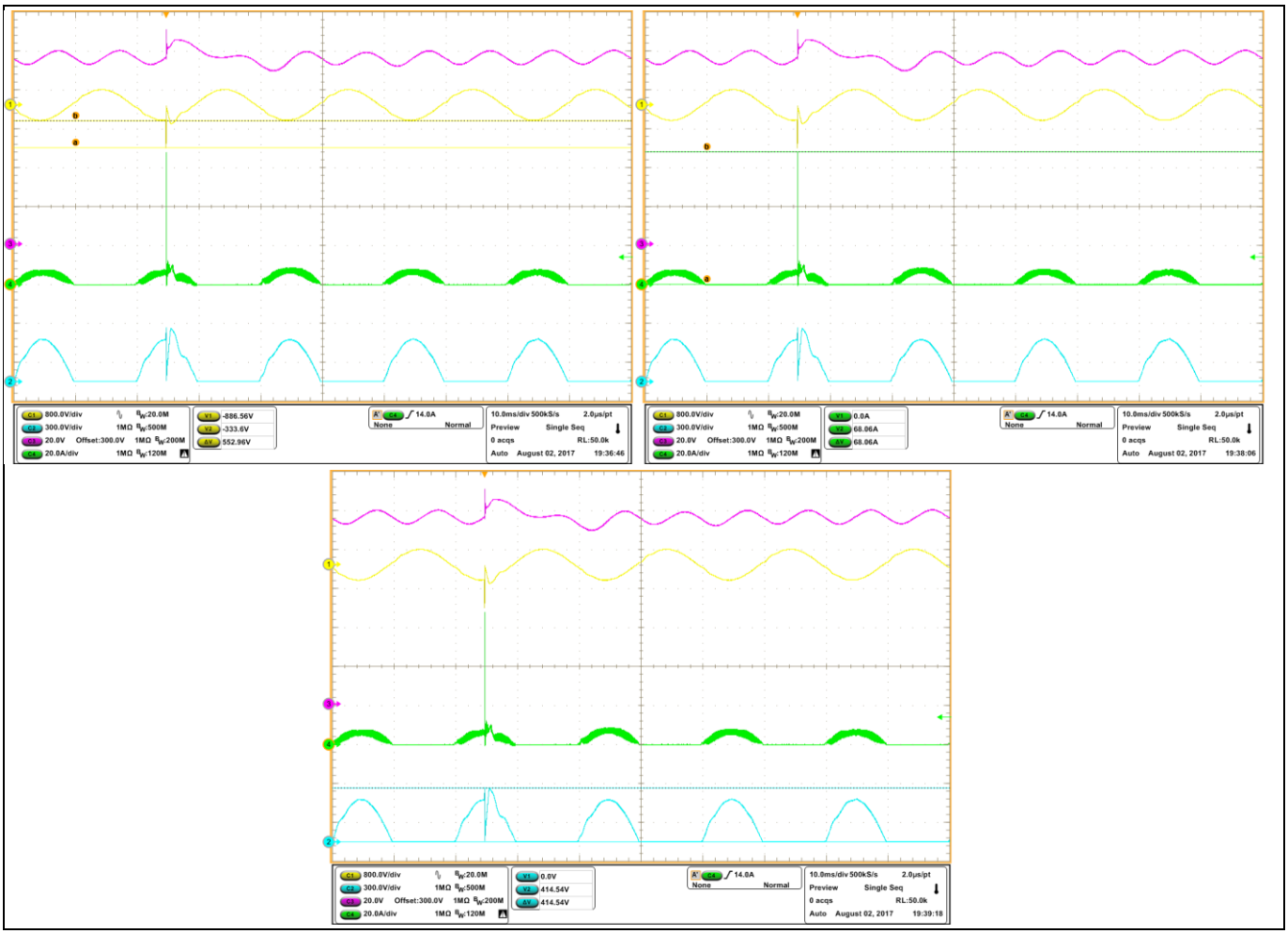


Figure 38 **1 kV line-to-neutral surge tests at 270°C when V_{in} = 230 V AC and P_{out} = 1 kW.**
Top left: The yellow horizonzal lines indicate the 553 V difference between AC-line peak voltage and surge peak voltage
Top right: The green horizontal lines indicate the 68 A surge peak current through the active rectification MOSFET Q4
Bottom: The blue horizontal lines indicate the maximum voltage of 414.5 V across the non-active rectification MOSFET Q3

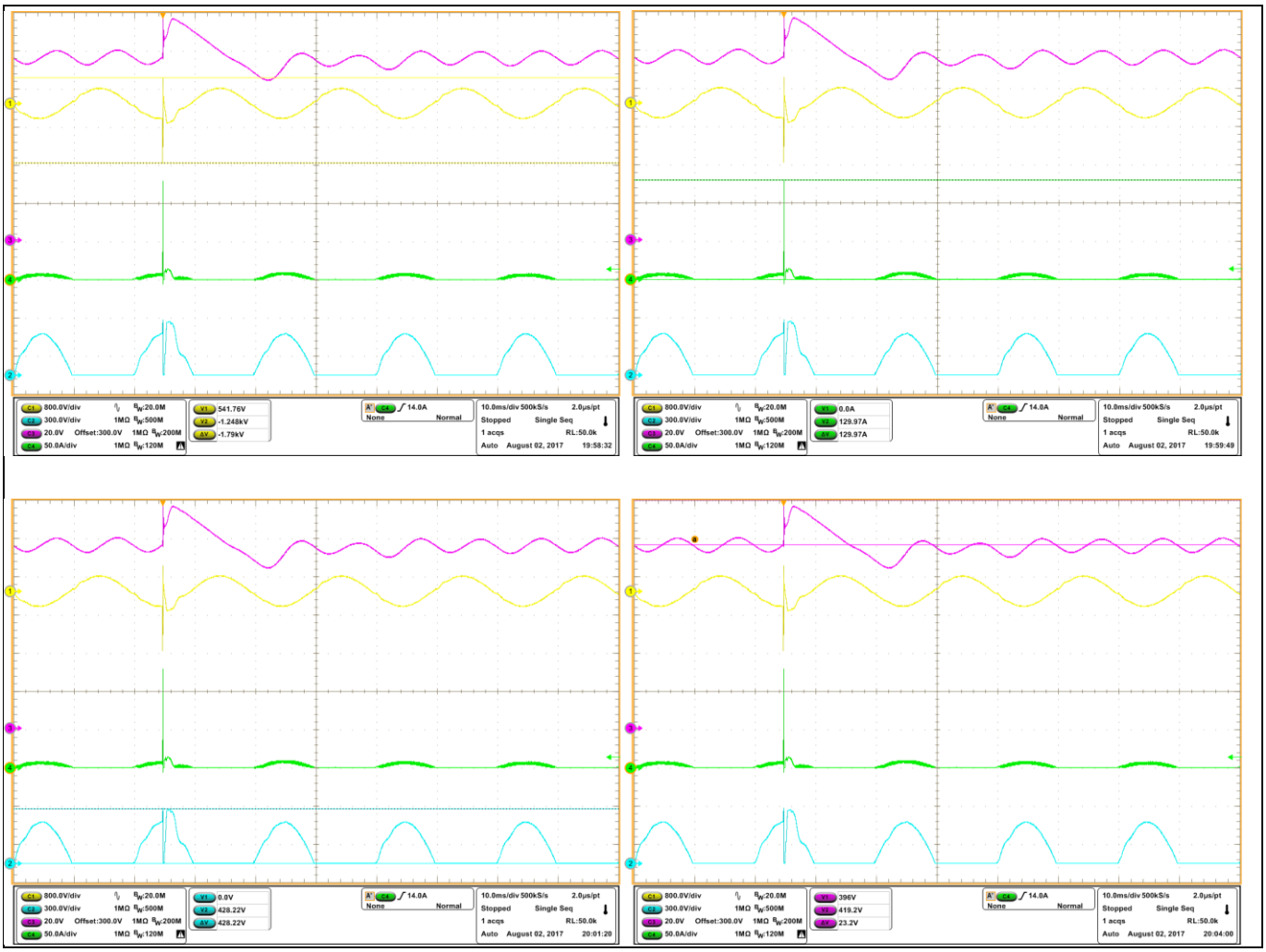


Figure 39 **2 kV line-to-neutral surge tests at 270°C when V_{in} = 230 V AC and P_{out} = 1 kW**
Top left: The yellow horizontal lines indicate the 542 V positive and the 1248 V negative surge peak voltages in the input voltage
Top right: The green horizontal lines indicate the 130 A surge peak current through the active rectification MOSFET Q4
Bottom left: The blue horizontal lines indicate the maximum voltage of 428 V across the non-active rectification MOSFET Q3
Bottom right: The magenta horizontal lines indicate the maximum OV of around 420 V at the output voltage

As clearly shown in **Figure 38** and **Figure 39**, potential surges coming from the AC-line do not represent a serious threat to the integrity of the active rectification MOSFETs Q3 and Q4, because:

- Before the HV surges reach the bridgeless dual-PFC converter, the AC plug, internal cabling and EMI filter present certain impedance that attenuates the energy of the surge, as can be read in the yellow waveform cursor measurements in the previous figures.
- During positive HV surges the bridge rectifier diodes D5 and D6 perform as bypass diodes and the three bulk capacitors absorb the energy of this effect. The eventual huge but quite narrow current surge slightly charges the three capacitors, which results in a noticeable but unharmful voltage overshoot, as shown in the magenta waveforms (converter output) as well as in the blue waveforms (drain-to-source voltage in the

actual untriggered active rectification MOSFET). These eventual voltage overshoots are far below the minimum drain-to-source breakdown voltage of the untriggered active rectification MOSFET.

- The huge but quite narrow current surges also circulate through the actual triggered active rectification MOSFET. However, the peak value of such current spikes, 68 A for the 1 kV surge and 130 A for the 2 kV one, are still lower than the MOSFET/body diode pulsed drain current capability, in this case 212 A.
- During negative HV surges the bridge rectifier diodes D3 and D4 clamp down the voltage at the input of the converter to their corresponding forward voltage.

7 Demo board

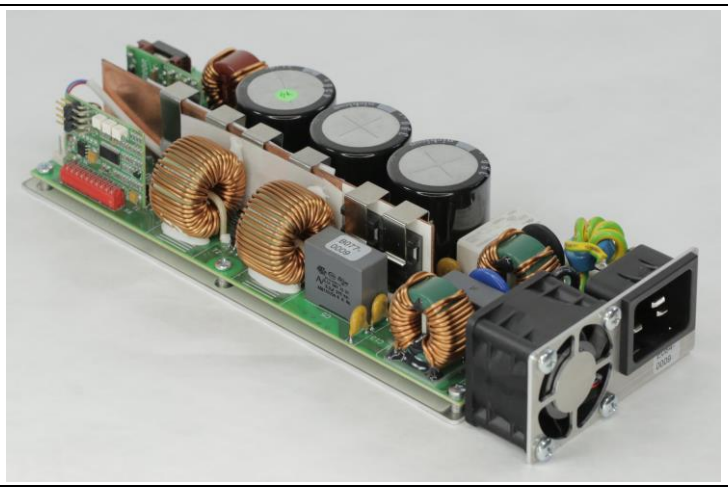


Figure 40 3 kW 90 kHz dual-boost PFC demo board

7.1 Power board

7.1.1 Schematics

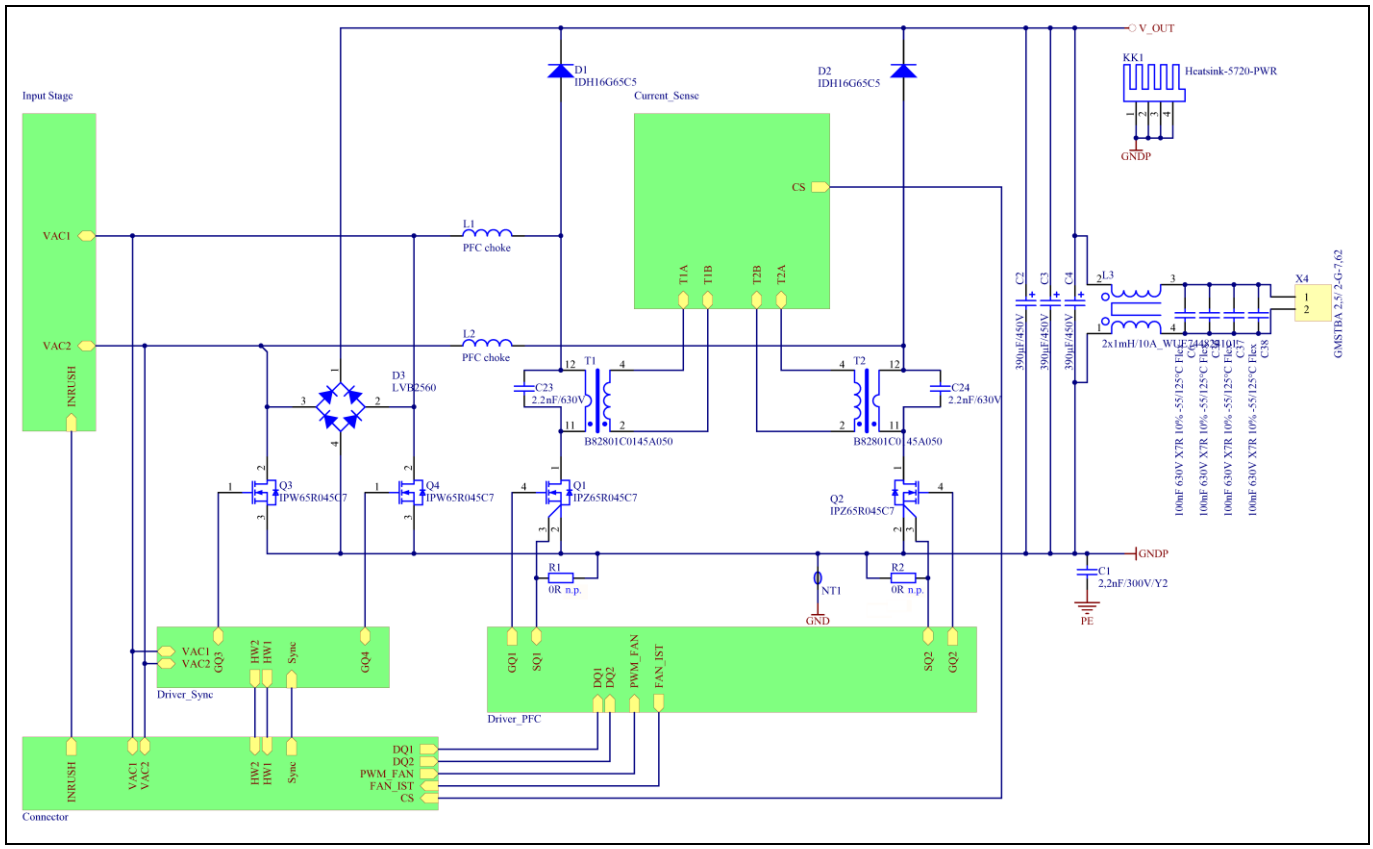


Figure 41 Schematics of the power stage

Filters are not normally used at the output of PFC boost converters. This demo board uses the output filter L3-C6-C36-C37-C38 just for reliable efficiency measurements. If this demo is to be used as reference design for a complete power supply solution, this output filter must be disregarded.

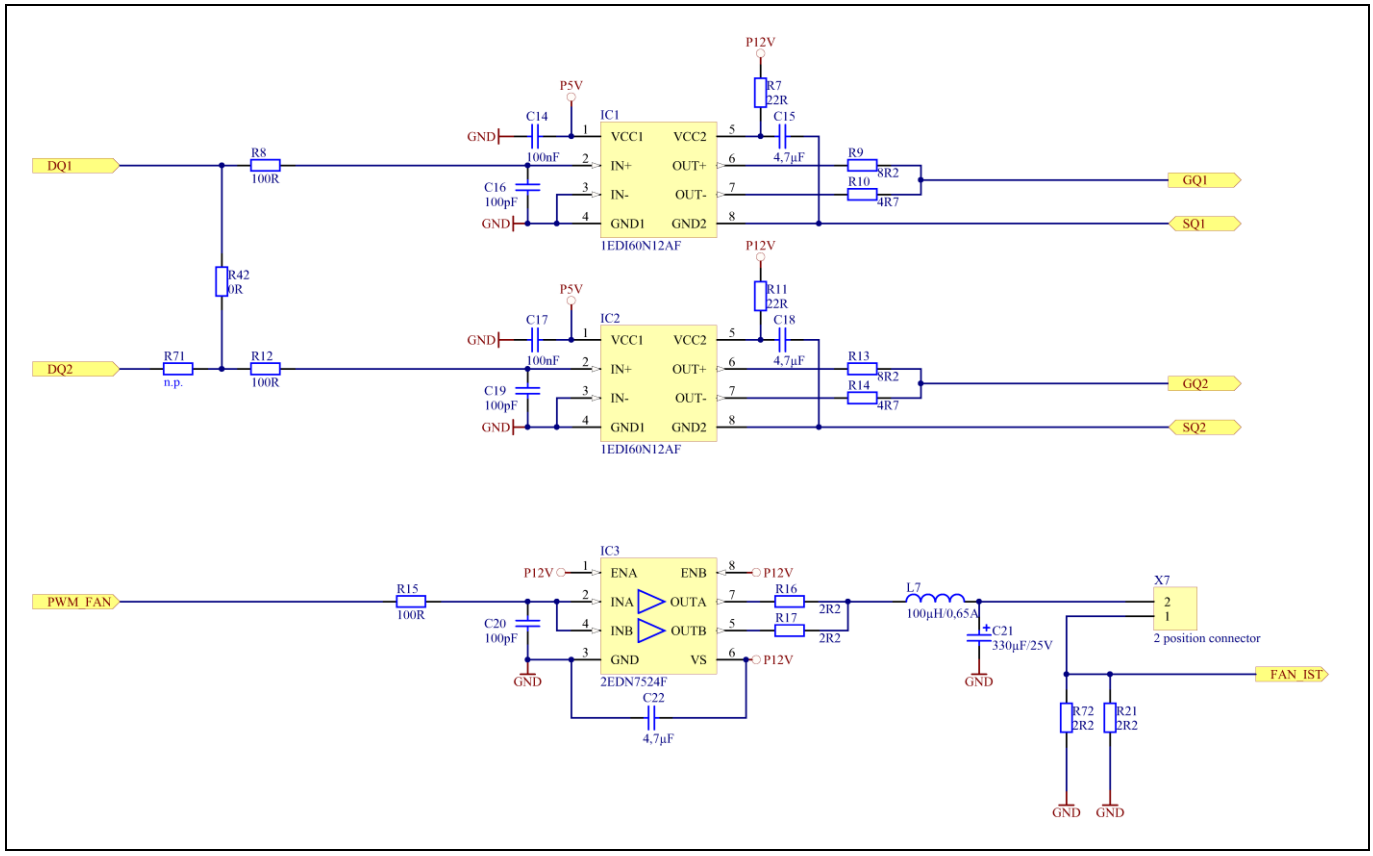


Figure 42 **Schematics of the 1EDIx gate drivers for the PFC MOSFETs as well as the 2EDN gate driver used in this case as a buck converter for controlling the speed of the fan**

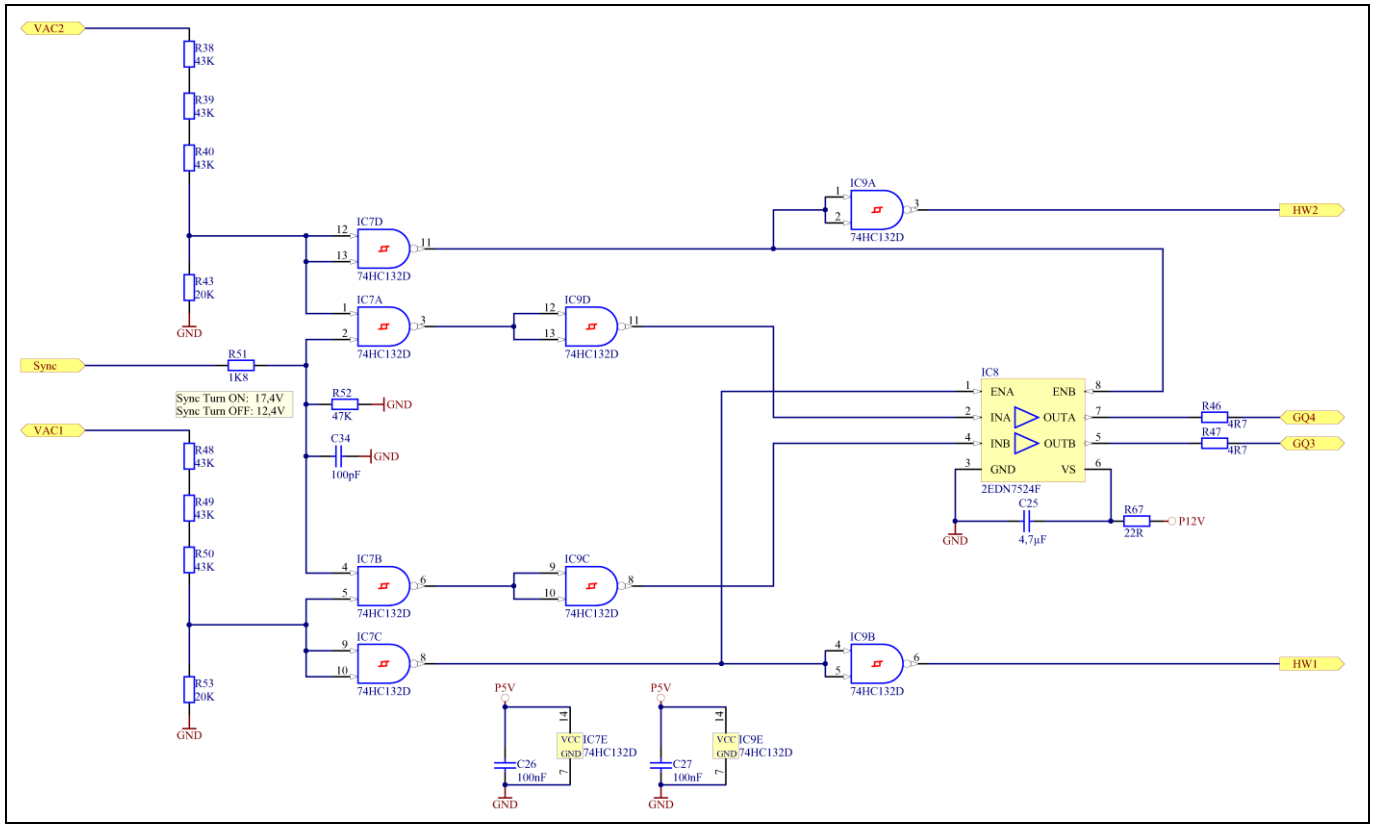


Figure 43 **Schematics of the firing control circuitry for the active rectification MOSFETs Q3 and Q4**

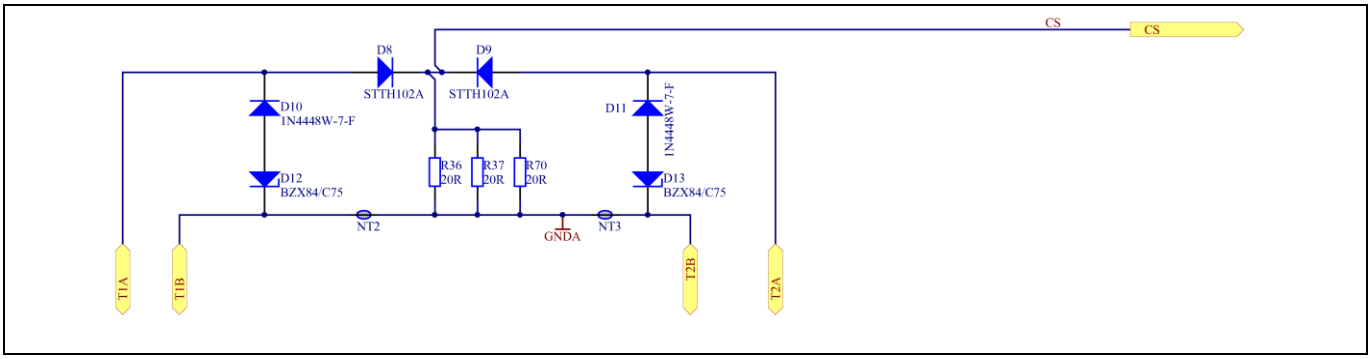


Figure 44 Schematics of the current sense (CS)

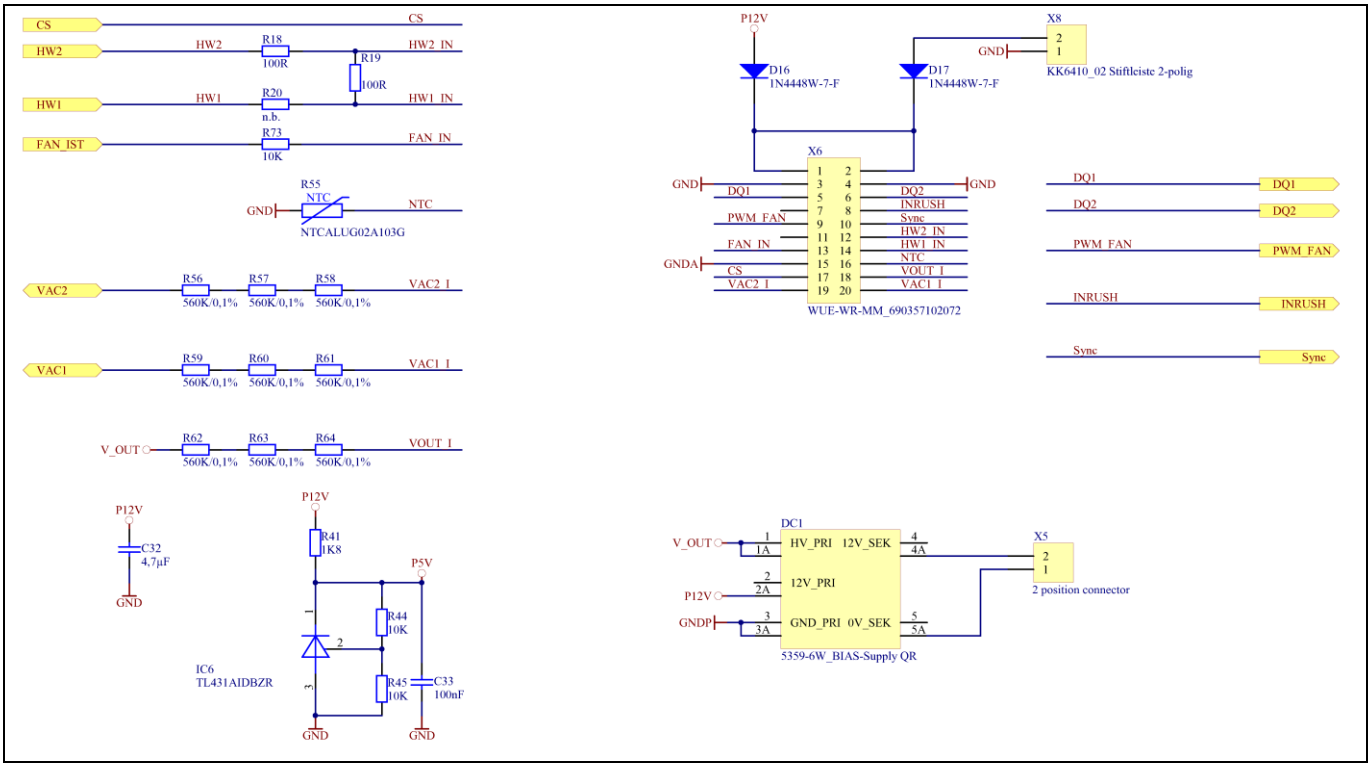


Figure 45 Schematics of the circuitry around the connector where the control daughter card is plugged in

7.1.2 PCB layout

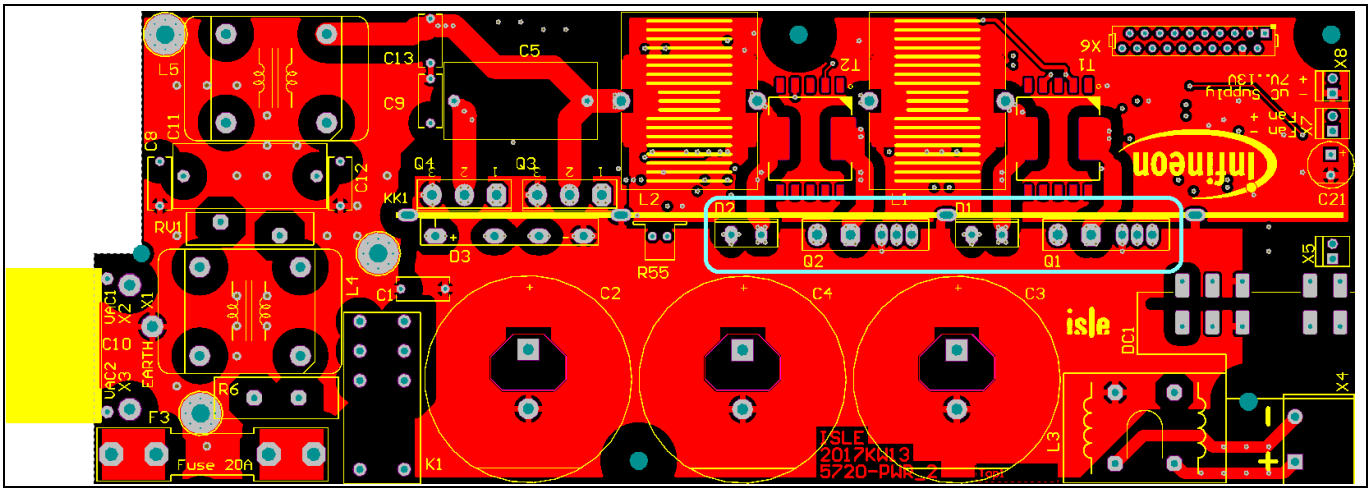


Figure 46 View of the PCB top layer

As shown in the cyan rectangle highlighted in **Figure 46**, the layout of the board allows the user to evaluate the performance of the dual-boost PFC converter using either TO-247 3-pin or TO-247 4-pin Q1 and Q2 PFC MOSFETs. The pin configuration is as follows:



Figure 47 Pin configuration for TO-247 3-pin and TO-247 4-pin devices

Please be aware that when using TO-247 3-pin devices, 0 Ω resistors must be populated in R1 and R2, as indicated by the yellow arrows shown in the figure below.

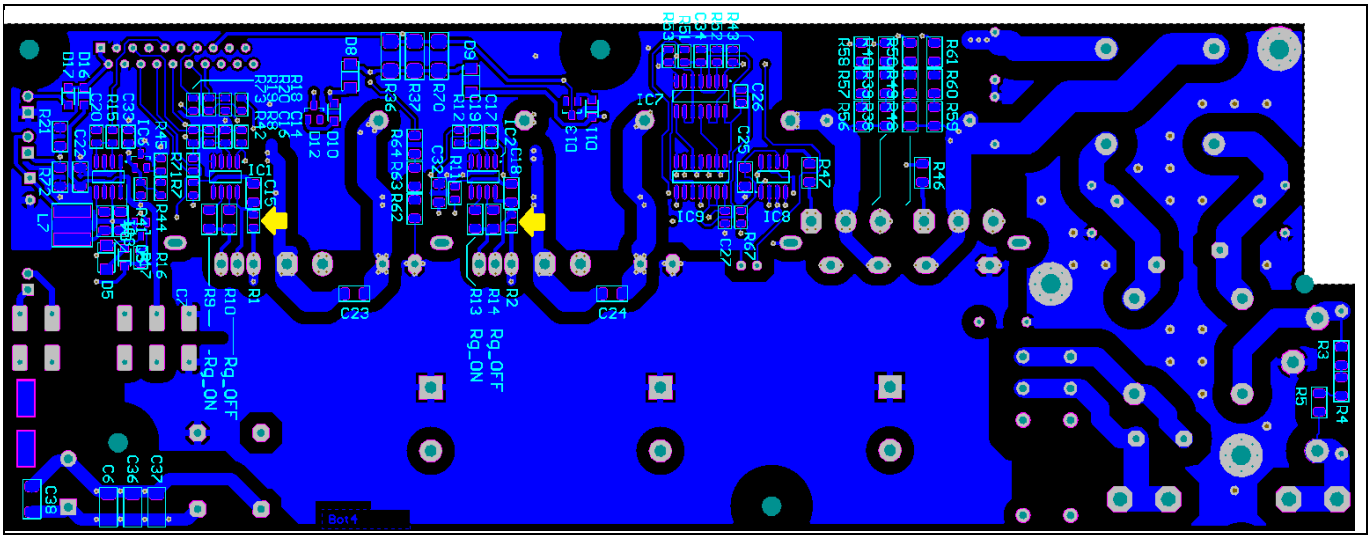


Figure 48 View of the PCB bottom layer

7.1.3 BOM

Table 11 BOM of the power board

Quantity	Designator	Value	Description	Footprint
4	R1, R2, R20, R71	Not populated	Resistors not populated	RESC2012N
1	R52	47 k	0.125 W TK100 1% 150 V	RESC2012N
6	R38, R39, R40, R48, R49, R50	43 k	0.25 W TK100 1% 200 V	RESC3216N
3	R7, R11, R67	22 R	0.125 W TK100 1% 150 V	RESC2012N
3	R36, R37, R70	20 R	1 W TK50 1% 500 V	RESMELF5822N
2	R43, R53	20 k	0.125 W TK100 1% 150 V	RESC2012N
3	R44, R45, R73	10 k	0.125 W TK100 1% 150 V	RESC2012N
2	R9, R13	8R2	0.25 W TK100 5% 200 V	RESC3216N
4	R10, R14, R46, R47	4R7	0.25 W TK100 5% 200 V	RESC3216N
9	R56, R57, R58, R59, R60, R61, R62, R63, R64	560 k/0.1%	0.25 W TK25 0.1% 200 V	RESC3216N
1	R6	B57364S0100M	NTC inrush 10 R 3300 k 7.5 A	B57364-Sxxx
5	R8, R12, R15, R18, R19	100 R	0.125 W TK100 1% 150 V	RESC2012N
3	R3, R4, R5	150 k	0.25 W TK100 1% 200 V	RESC3216N
1	R42	0 R		RESC2012N
4	R16, R17, R21, R72	2R2	0.25 W TK100 5% 200 V	RESC3216N
2	R41, R51	1K8	0.125 W TK100 1% 150 V	RESC2012N
1	RV1	S20K275 Epcos B72220S0271K101	Varistor 275 V 1 W	S20K275
1	R55	NTCALUG02A103G	NTC 10 k 3984K	B57703-Mxxx
4	C16, C19, C20, C34	100 pF	100 pF 50 V C0G 5% -55/125°C	CAPC2012N
4	C6, C36, C37, C38	100 nF/630 V	100 nF 630 V X7R 10% -55/125°C flex	CAPC4520N
6	C7, C14, C17, C26, C27, C33	100 nF	100 nF 50 V X7R 5% -55/125°C	CAPC2012N
3	C2, C3, C4	390 µF/450 V	390 µF 450 V	CAPPR10-35x30
1	C5	2.2 µF/275 V/X2	2.2 µF 275 V X2	CAPR22.5-13X26X22
5	C1, C8, C9, C12, C13	2.2 nF/300 V/Y2		CAPR7.5-9X4
1	C21	330 µF/25 V	330 µF 25 V	CAPPR3.5-8x11
2	C23, C24	2.2 nF/630 V	2.2 nF 630 V NP0 5%	CAPC3216N
5	C15, C18, C22, C25, C32	4.7 µF	4.7 µF 25 V X7R 10%	CAPC3216N
2	C10, C11	1.0 µF/275 V/X2	1.0 µF 275 V X2	CAPR22.5-7X26X16_HOR, CAPR22.5-11X26X20
2	L1, L2	254 mH	PFC choke: CH270060E18 core with	RKV-30X23RM23D1.8

			46 turns of AWG16	
2	L4, L5	CM 2 x 3.0 mH	Input CM choke	
2	T1, T2	B82801C0145A050	SMT CS transformers, 50:1, 1.4 mH	B82801C
1	L7	100 µH/0.65 A	SMD inductor 100 µH/0.65 A	INDP6262N
1	L3	2 x 1 mH/10 A_WUE744824101	Output CM choke	WUE-CM_744824xxx
2	D8, D9	STTH102A	Ultrafast diode	SMA
1	D5	SMAJ15	Supressor diode	SMA
1	D3	LVB2560	Rectifier diode 600 V 25 A	REC-GSIB-5S
2	D12, D13	BZX84/C75	Zener diode	SOT23-3N
5	D4, D10, D11, D16, D17	1N4448W-7-F	Fast-switching diode	SOD123
2	D1, D2	IDH16G65C5	Schottky diode	TO220-AC
1	Q5	BCR503	NPN digital transistor	SOT23-3N
2	Q1, Q2	IPZ65R045C7	CoolMOS™ power MOSFET	TO247-5
2	Q3, Q4	IPW65R045C7	CoolMOS™ power MOSFET	TO247
2	IC3, IC8	2EDN7524F	Treiber low-side dual non-inverting MOSFET	SOIC127P600-8N
2	IC1, IC2	1EDI60N12AF	Isolated gate driver	SOIC127P600-8N
1	IC6	TL431AIDBZR	Adjustable precision shunt regulator	SOT23-3N
2	IC7, IC9	74HC132D	Logic quad dual-input NAND gate with Schmitt trigger inputs	SOIC127P600-14N
1	X6	WUE-WR-MM_690357102072	Mini module plug connector	WUE-WR-MM_MAL_POL_THT
1	X4	GMSTBA 2.5/ 2-G-7.62	Phoenix board connector	GMSTBA2.5/2-G-7.62
2	KC6, KC7	THFA 3	Heatsink clips	
4	KC1, KC2, KC3, KC4	THFA 1	Heatsink clips	
3	X5, X7, X8	KK6410_02	Molex dual-position plug connector	KK6410_2
1	IF1	KUBG20	Thermally conductive thermo-silicone film 90 x 30 mm	
1	IF2	KUBG20	Thermally conductive thermo-silicone film 40 x 30 mm	
1	KK1	Heatsink	1 mm wide x 160 mm long copper heatsink	

1	K1	HF115F/012-1HS3B	SPST relay	Finder_41.61
1	F4	Fuse 20 AT 6.3 x 32	20 A fuse	
1	F3	01220088Z	2x fuse holder clips	SH32B
1	Fan	422JN	ebm-papst 4 W 18.3 CFM/14250 rpm cooling fan	40 mm x 40 mm x 28 mm

7.2 Auxiliary power supply daughter card

7.2.1 Schematics

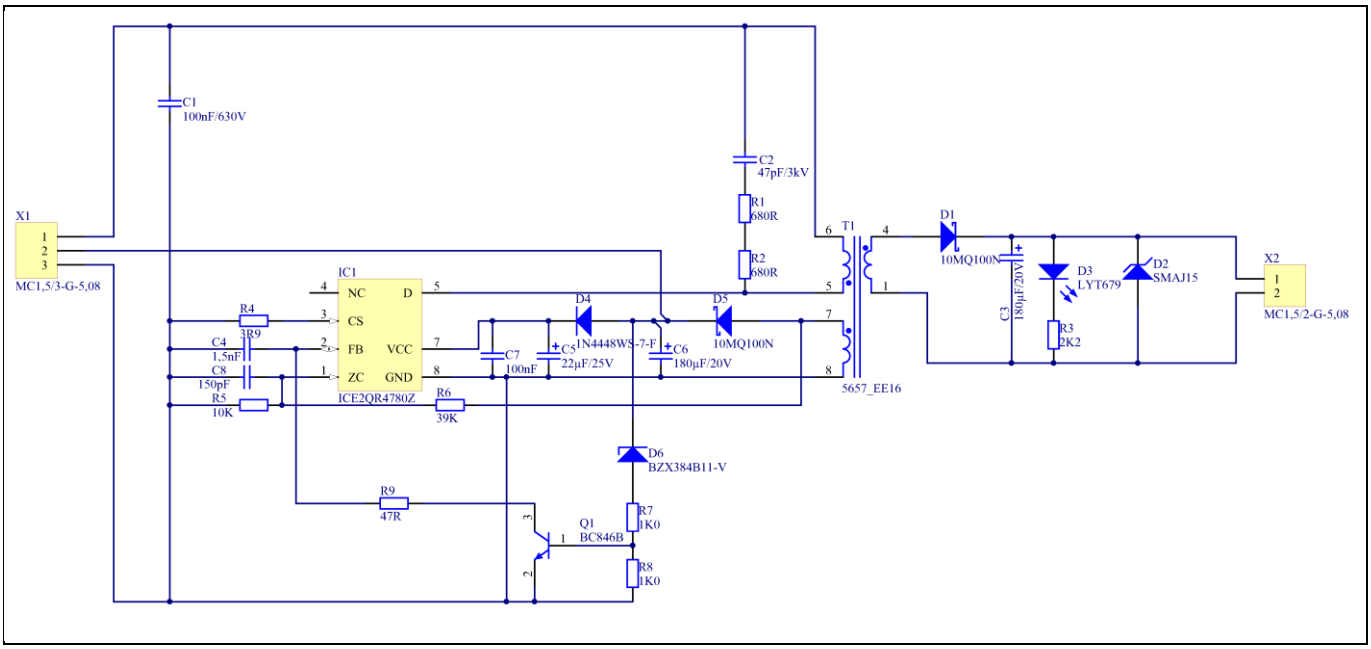


Figure 49 Schematic of the daughter card connector

7.2.2 PCB layout

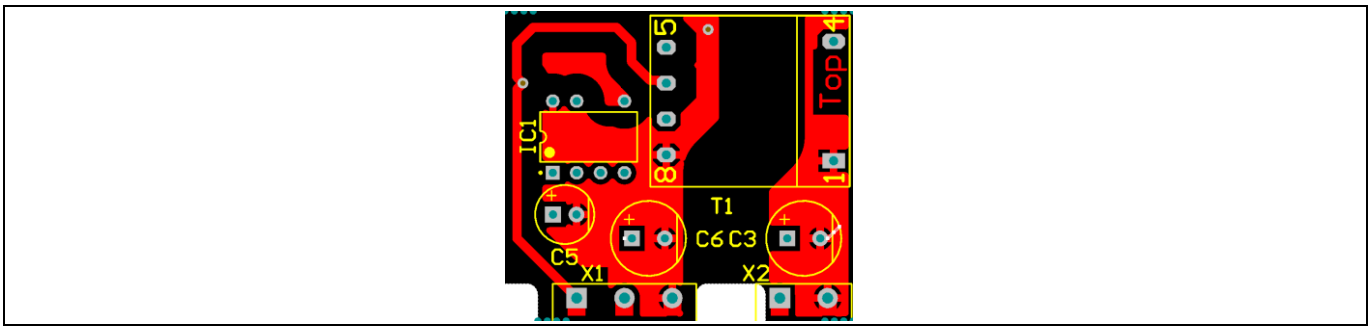


Figure 50 View of the auxiliary power supply daughter card – PCB top layer

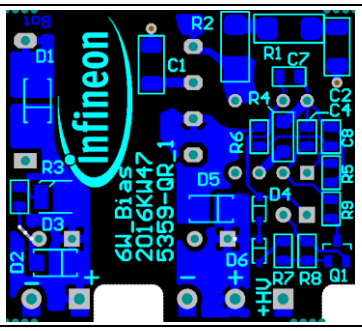


Figure 51 **View of the auxiliary power supply daughter card – PCB bottom layer**

7.2.3 BOM of the power board

Table 12 **BOM of the auxiliary power supply daughter card**

Quantity	Designator	Value	Description	Footprint
1	C4	1.5 nF	1.5 nF 50 V X7R 10% -55/ 125°C	CAPC2012N
1	C8	150 pF	150 pF 50 V C0G 5% -55/ 125°C	CAPC2012N
1	C7	100 nF	100 nF 50 V X7R 5% -55/ 125°C	CAPC2012N
1	C2	47 pF/3 kV	47 pF 3 kV C0G 5% -55/125°C	CAPC4520N
1	C1	100 nF/630 V	100 nF 630 V X7R 10% -55/ 125°C flex	CAPC4520N
1	C5	22 µF/25 V	22 µF 25 V	CAPPR2.5-6.3x11
2	C3, C6	180 µF/20 V	180 µF 20 V OSCON	CAPPR3.5-8x7
1	D3	LYT679	Low-current yellow LED	DIOM3028N
1	IC1	ICE2QR4780Z	PWM controller current mode QR	DIP-8_-6
1	T1	5657_EE16	EF16 bias supply flyback transformer	Hartu_E16-8-P2P3
1	R6	39 k	0.125 W TK100 1% 150 V	RESC2012N
1	R3	2K2		RESC2012N
1	R5	10 k	0.125 W TK100 1% 150 V	RESC2012N
2	R7, R8	1K0		RESC2012N
1	R9	47 R		RESC2012N
1	R4	3R9	0.25 W TK50 1% 200 V	RESMELF3614N
2	R1, R2	680 R		RESMELF5822N
1	D2	SMAJ15	Supressor diode	SMA
2	D1, D5	10MQ100N	Schottky diode	SMA
1	D4	1N4448WS-7-F	Fast-switching diode	SOD323

1	D6	BZX384B11-V	11 V nener diode	SOD323
1	Q1	BC846B	NPN transistor	SOT23-3N

7.3 Digital controller daughter card

7.3.1 Schematics

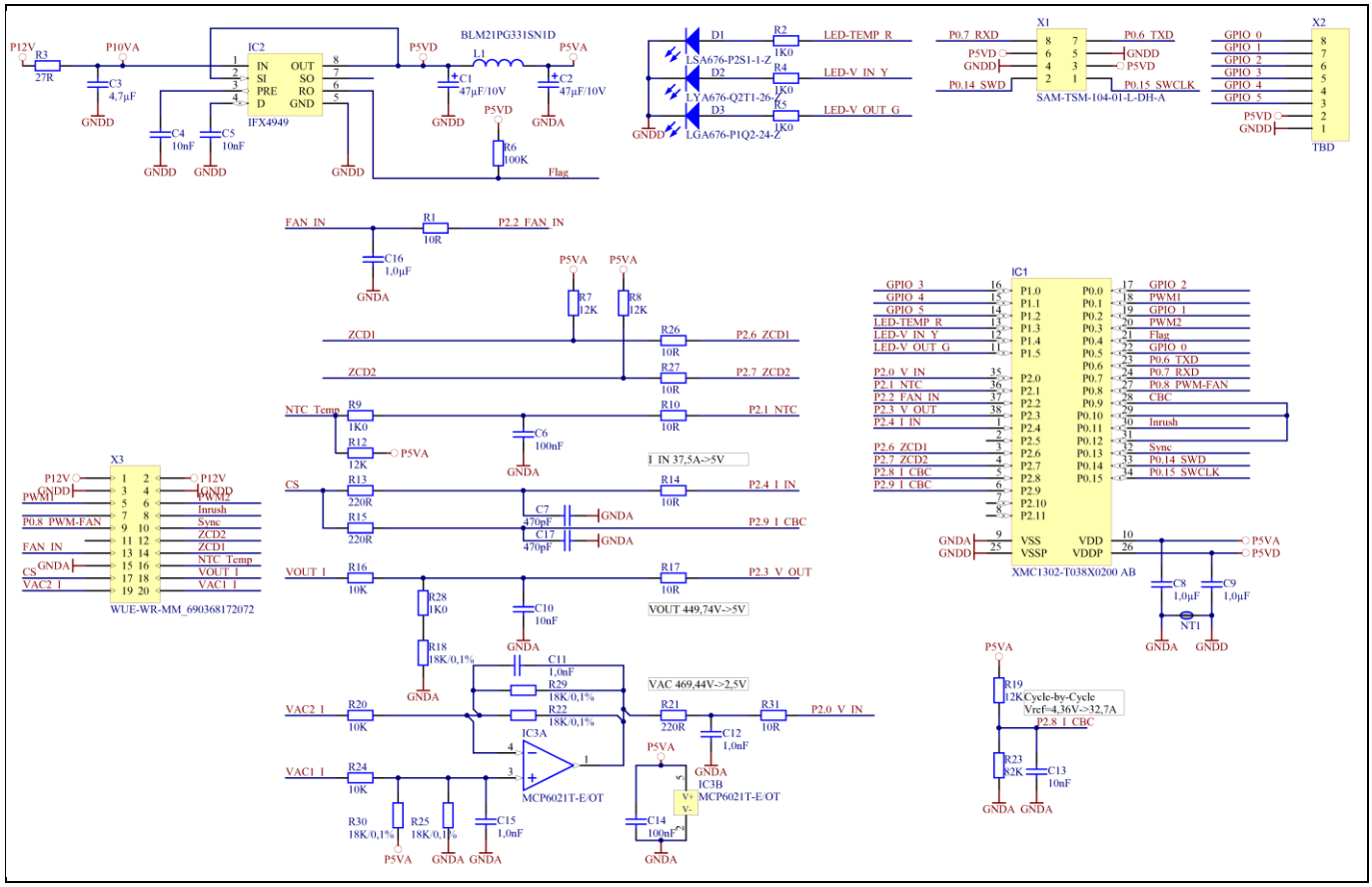


Figure 52 Schematic of the digital controller daughter card

7.3.2 PCB layout

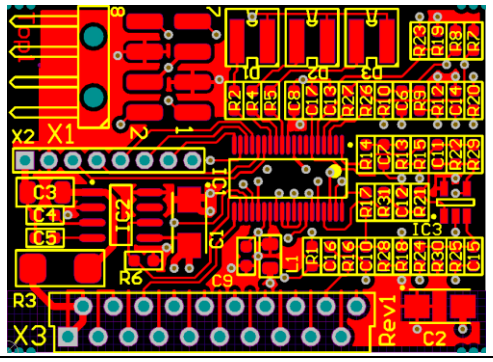


Figure 53 View of the digital controller daughter card PCB top layer

7.3.3 BOM of the digital controller

Table 13 BOM of the digital controller daughter card

Quantity	Designator	Value	Description	Footprint
4	C4, C5, C10, C13	10 nF	10 nF 50 V X7R 10% -55/ 125°C	CAPC1608N
2	C6, C14	100 nF	100 nF 50 V X7R 10% -55/ 125°C	CAPC1608N
2	C7, C17	470 pF	470 pF 50 V 10% -55/125°C	CAPC1608N
3	C8, C9, C16	1.0 µF	1.0µF 16 V X7R 10% -55/ 125°C	CAPC1608N
3	C11, C12, C15	1.0 nF	1.0 nF 50 V C0G 5% -55/ 125°C	CAPC1608N
1	C3	4.7 µF	4.7µF 25 V X7R 10%	CAPC3216N
2	C1, C2	47 µF/10 V	47 µF 10 V 125°C	CAPMP4726X20N
1	L1	BLM21PG331SN1D	Ferrite bead 330 Ω, 1.5 AA	INDP2012N
1	D1	LSA676-P2S1-1-Z	Hyper-bright super-red LED	LED_LxA670
1	D2	LYA676-Q2T1-26-Z	Low-current yellow LED	LED_LxA670
1	D3	LGA676-P1Q2-24-Z	Hyper-bright green LED	LED_LxA670
7	R1, R10, R14, R17, R26, R27, R31	10 R	0.1 W TK100 1.0% 50 V	RESC1608N
5	R2, R4, R5, R9, R28	1K0	0.1 W TK100 1.0% 50 V,	RESC1608N
1	R6	100 k	0.1 W TK100 1.0% 50 V	RESC1608N
4	R7, R8, R12, R19	12 k	0.1 W TK100 1.0% 50 V	RESC1608N
3	R13, R15, R21	220 R	0.1 W TK100 1.0% 50 V	RESC1608N
3	R16, R20, R24	10 k	0.1 W TK100 1.0% 50 V	RESC1608N
5	R18, R22, R25, R29, R30	18 k/0.1%	0.1 W TK25 0.1% 75 V	RESC1608N
1	R23	82 k	0.1 W TK100 1.0% 50 V	RESC1608N
1	R3	27 R	1 W TK50 1% 500 V	RESMELF5822N
1	X1	SAM-TSM-104-01-L-DH-A	2x4 SMT connector	SAM-TSM-104-01-X-DHA-Revers
1	IC2	IFX4949	Voltage regulator	SOIC127P600-8N
1	IC1	XMC1302-T038X0200 AB	Microcontroller	SOP50P640-38N
1	IC3	MCP6021T-E/OT	Operational amplifier	SOT23-5N
1	X3	WUE-WR-MM_690368172072	Mini module socket connector	WUE-WR-MM_FEM_ANG_POL_THT

8 Useful materials, links and references

- 650 V CooMOS™ C7 webpage
  www.infineon.com/650v-C7

- CoolSiC™ Schottky diode 650 V G5 webpage
  http://www.infineon.com/cms/en/product/power/sicarbide-sic/650v-thinq!-tm-sic-diode-generation-5/channel.html?channel=db3a3043399628450139b0536bed2187

- (EiceDRIVER™ 1EDI isolated gate driver
  https://www.infineon.com/cms/en/product/power/gate-driver-ics/galvanic-isolated-gate-driver/1EDI60N12AF/productType.html?productType=db3a3044426a54fb01426c0d4c181378

- EiceDRIVER™ 2EDN7524F non-isolated gate driver
  http://www.infineon.com/cms/en/product/power/motor-control-and-gate-driver-ics/non-isolated-gate-driver-ics-and-controllers/eicedriver-2edn-gate-driver-for-discrete-mosfets/channel.html?channel=5546d4624cb7f111014d334aeae60252

- XMC 1302 32-bit microcontroller with ARM® Cortex-M0
  www.infineon.com/cms/en/product/microcontroller/32-bit-industrial-microcontroller-based-on-arm-registered-cortex-registered-m/32-bit-xmc1000-industrial-microcontroller-arm-registered-cortex-registered-m0/XMC1302-T038X0200+AB/productType.html?productType=5546d4624cb7f111014d47dc5d246d13

- ICE2QR4780Z flyback controller
  https://www.infineon.com/cms/en/product/power/ac-dc-power-conversion/ac-dc-integrated-power-stage-coolset/ac-dc-quasi-resonant-coolset/ICE2QR4780Z/productType.html?productType=db3a30432a7fedfc012ab2458b0c36ff

[1] P. C. Todd, “UC3854 controlled power factor correction circuit design,” in *Product and Application Handbook*, U-134 Application Note, Unitrode Integrated Circuits, 1993

[2] M. Xie, “Digital Control for Power Factor Correction,” Virginia Polytechnic Institute and State University, 2003

[3] Koen De Gusseme, D. M. Van de Sype, A. P. M. Van den Bossche and J. A. Melkebeek, “Digitally controlled boost power-factor-correction converters operating in both continuous and discontinuous conduction mode,” in *IEEE Transactions on Industrial Electronics*, vol. 52, no. 1, pp. 88–97, Feb. 2005

Revision history

Major changes since the last revision

Page or reference	Description of change

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