MOSFET CoolMOS™ C7 Gold 600 V in TO-Leadless

A perfect partnership for power applications

About this document

Scope and purpose

With rising energy costs and space at a premium, designers of switch mode power supplies (SMPS) are under constant pressure to design ever more powerful solutions in ever-smaller form factors. This demands a huge gain in power density with each new product generation.

Modern semiconductors facilitate faster switching speeds and lower losses to support designers in this challenge. By driving down switching losses and on-state resistance, the latest superjunction (SJ) MOSFET technologies pushed the efficiency and power density limits of hard and soft switching applications.

Now, TO-Leadless (TOLL) packages, in combination with Infineon's 600 V CoolMOS™ C7 Gold (G7) technology offer the opportunity to migrate even high-power PFC circuits to SMD solutions for the first time.

This document is intended to describe Infineon's new TOLL (TO-Leadless) SMD package for high voltage applications, fitted with the high performance 600 V CoolMOS™ G7 superjunction (SJ) MOSFET technology.

The major advantages for high voltage and high power, hard switching and soft switching applications such as PFC, TTF and LLC will be discussed in detail. The document will focus on applying 600 V G7 SJ MOSFET technology in the high voltage TOLL SMD package to increase power density and optimize switching performance.

Intended audience

This document is intended for design engineers who want to improve their high voltage power conversion applications by moving from hole packages to SMD devices.

Keypoints

- Explains how combining G7 superjunction MOSFET technology with TOLL SMD packaging enables high-power PFC migration to SMD
- Describes thermal management strategies for SMD devices, including PCB design, thermal vias, and interface materials
- Provides design guidelines for optimizing $R_{DS(on)}$ selection, switching performance, and reliability in high-voltage applications
- Demonstrate efficiency improvements and reduced parasitics in CCM PFC and LLC topologies using G7 in TOLL packages
- Highlights practical assembly considerations such as creepage, clearance, AOI compatibility, and moisture sensitivity for robust designs

About this product family

Product family

Infineon's CoolMOS™ is a high-voltage N-channel silicon power MOSFET that is designed to provide excellent thermal performance, lowest switching and conduction power losses, and optimal $R_{DS(on)}$ for increased system efficiency, supporting a range of application from low power levels to high power levels.

Target applications

- Consumer electronics
- Industrial applications
- Home appliances
- Server
- Telecom
- Renewables

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1 Introduction

The last decade of SMPS (switched mode power supply), development was dominated by the trend towards higher power density and cost optimization.

Ever-faster switching speeds, ever-lower losses, optimization of board space, and minimized total cost of ownership (TCO) are among the critical challenges today's power supply designers are facing. By driving down on-state resistance and switching losses in hard and soft switched topologies, the latest superjunction (SJ) MOSFET technologies hold the key to addressing these challenges for modern hard and soft switching applications.

Recently SMD packaged devices became more popular in order to support fast switching silicon and to reduce the parasitic inductance associated with the long leads of THD's. So far, however, the use of SMD devices was limited to medium and low power applications due to the cooling constraints. These constraints are the main reason why TO-220 and TO-247 are still the main package types used for high power factor correction (PFC) circuits.

TOLL in combination with the G7 technology for the first time, offers the possibility to move away from through-hole packages towards SMD solutions in high power PFC circuits. This is a very important enabler for power density improvements and cost savings.

1.1 Target applications

From Table 1, one can read easily that the 600 V G7 offers highest efficiency in hard-switching topologies and, in parallel, can also be used in LLC applications with some measures taken to minimize the hard commutation of the body diode, as described later in this application note.

Table 1 CoolMOS™ recommended application matrix

Switching category	Applications	650 V G7	600 V G7
Hard switching	Boost, PFC (CCM, DCM)	Increased voltage safety	Highest efficiency
	TTF, ITTF	High efficiency	
Soft switching	LLC	Not recommended due to hard commutation of body diode.	Highest efficiency; More details see section 2.5 - Rugged body diode

1.2 600 V CoolMOS™ C7 Gold (G7) performance

The G7 silicon technology is based on the well-known 600 V CoolMOS™ C7 that was introduced in early 2015. Since then, continued development has further improved the technology. One of the major evolutions of the C7 technology is the reduction of E_{oss} as seen in Figure 1. For hard-switching applications, this energy is always lost because it is converted into heat once the device gets turned on again with a positive gate signal. All the improvements offered by the G7 technology result in reduced switching losses and, very importantly, a reduction in the thermal resistance (R_{th}) of the device.

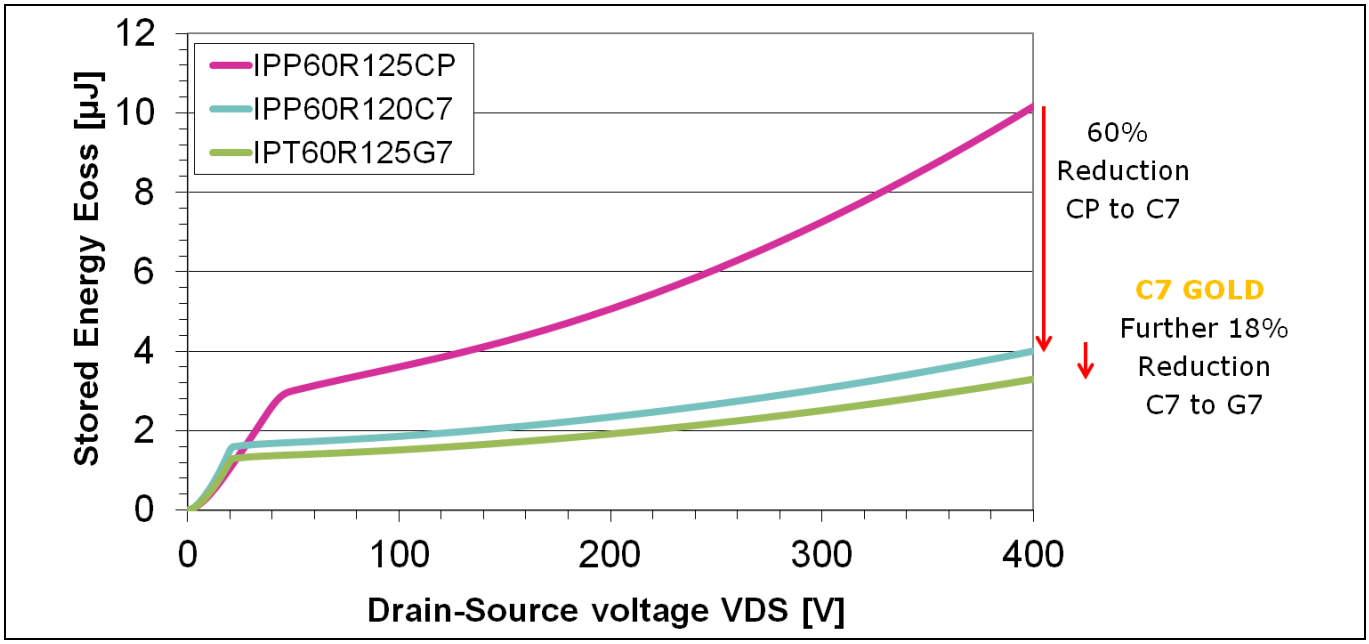


Figure 1 **Stored E_{oss} in the output capacitance for different technologies**

The 600 V G7 will be available with $R_{DS(on)}$ from 28 mΩ up to 150 mΩ. The 28 mΩ device offers the lowest available $R_{DS(on)}$ of any 600 V SMD device worldwide. It is the perfect use case for high power applications like hard switching PFC or soft switching LLC as well as for low switching and conduction loss dominated applications like bridge rectifier replacement or circuit breaker with DC or even AC current.

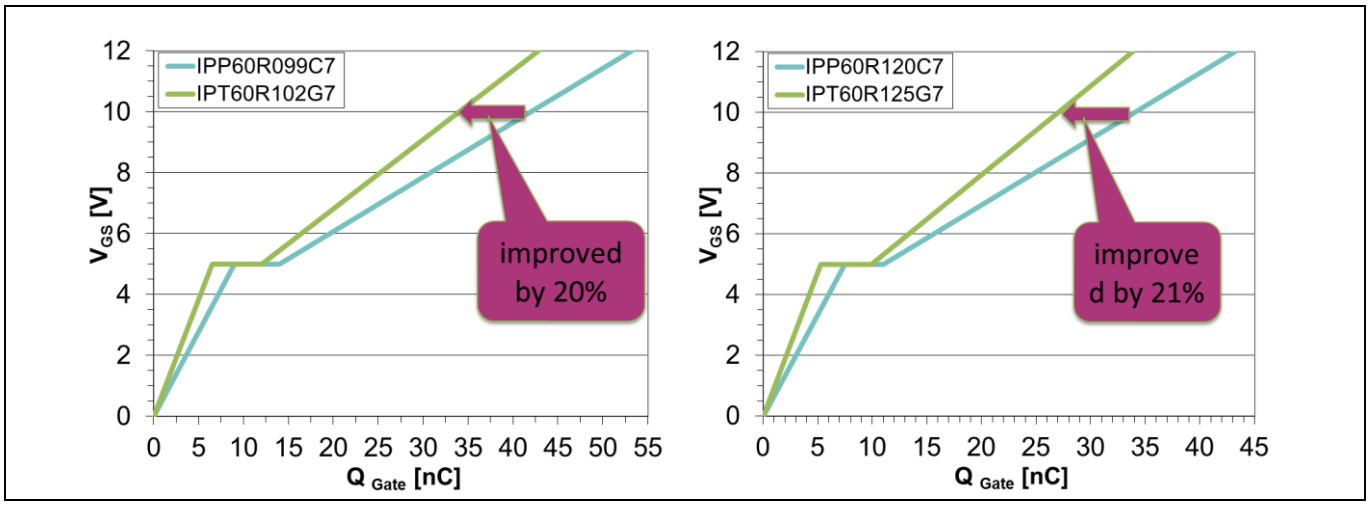


Figure 2 **Gate charge comparison for 102 mΩ and 125 mΩ**

Although lower Q_G means lower gate driving losses, Q_{GD} is a significant parameter related to switching transition times and losses. Figure 2 shows the gate charge comparison between 600 V CoolMOS™ C7 and the 600 V CoolMOS™ G7 based on the 102 mΩ and 125 mΩ devices. One can see that the G7 offers approximately 20% lower gate charge and will, therefore, switch faster with much lower switching losses.

Note: *There is no $R_{DS(on)}$ comparable device from reference technology available to allow a comparison with the other $R_{DS(on)}$ devices of the CoolMOS™ G7 portfolio. Therefore, Figure 2 and Figure 3 focus on the 102 mΩ and 125 mΩ devices.*

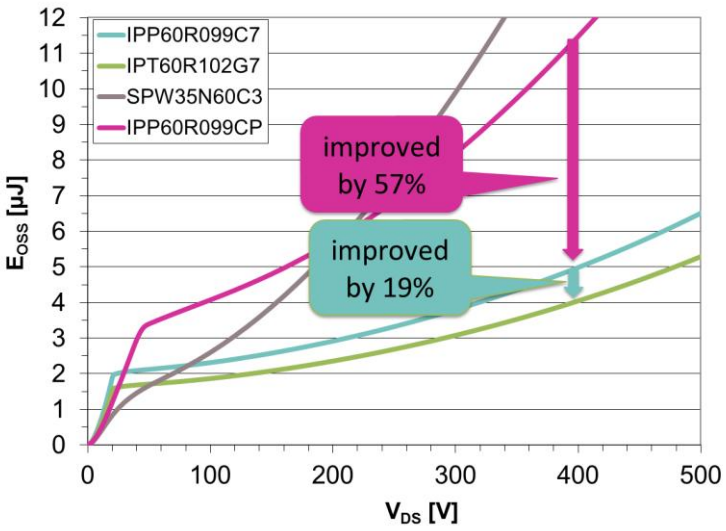


Figure 3 E_{oss} comparison for 102 mΩ range

In Figure 3, the E_{oss} reduction is shown, which has a very high impact on the performance of hard switching applications like conventional PFC or TTF topologies. For this kind of applications, the E_{oss} energy will become power losses during the turn on phase of the MOSFET. The higher the switching frequency, the greater the impact of this performance improvement on overall energy efficiency.

In fact, the switching losses of the CoolMOS™ G7 are reduced similar to the $R_{DS(on)}$ step within the 600 V CoolMOS™ C7 technology. This means that the 102 mΩ G7 device exhibits the same switching losses as the 120 mΩ C7 device. Therefore, it is now possible to use (for the same power range) one step lower $R_{DS(on)}$ in order to reduce the overall power losses but retain the same light-load efficiency.

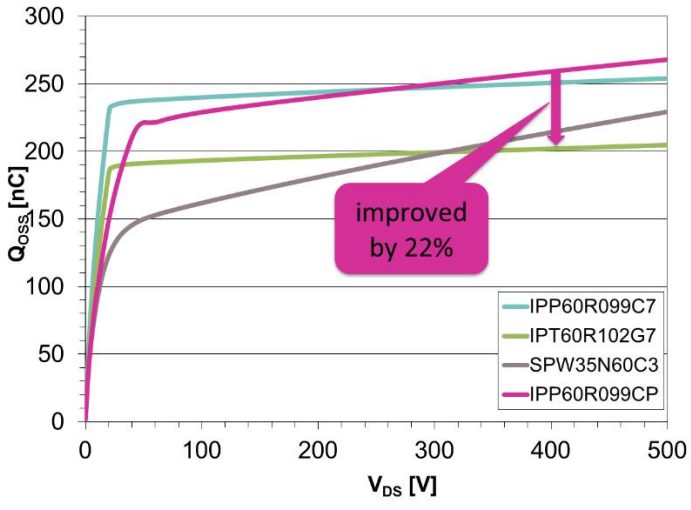


Figure 4 Q_{oss} comparison for 102 mΩ range

The comparison of the Q_{oss} (stored charge in the output capacitance) in Figure 4 depicts the improvement offered by the G7 technology compared to earlier released products. The Q_{oss} is one of the most important key parameters for resonant topologies like LLC and ZVS converter. The lower the Q_{oss}, the faster the transition will be if the resonant tank of the system is kept the same like it would be for simple plug and play replacement.

Beyond this plug-and-play replacement, this reduction in Q_{oss} offers to reduce the energy in the resonant tank, which will have very positive implications to the power density and system efficiency in parallel. In Figure 4, one can see that the Q_{oss} level at 400 V for the G7 technology is even lower than that of the well-known CoolMOS™ C3 technology.

1.3 TOLL (TO-Leadless) SMD package

The TOLL (P/PG-HSOF-8-2) package is a recently developed SMD package optimized for high power, high voltage, and high reliability applications. It is based on the TOLL for low-and medium-voltage version (P/PG-HSOF-8-1), which is successfully used in industrial and automotive applications.

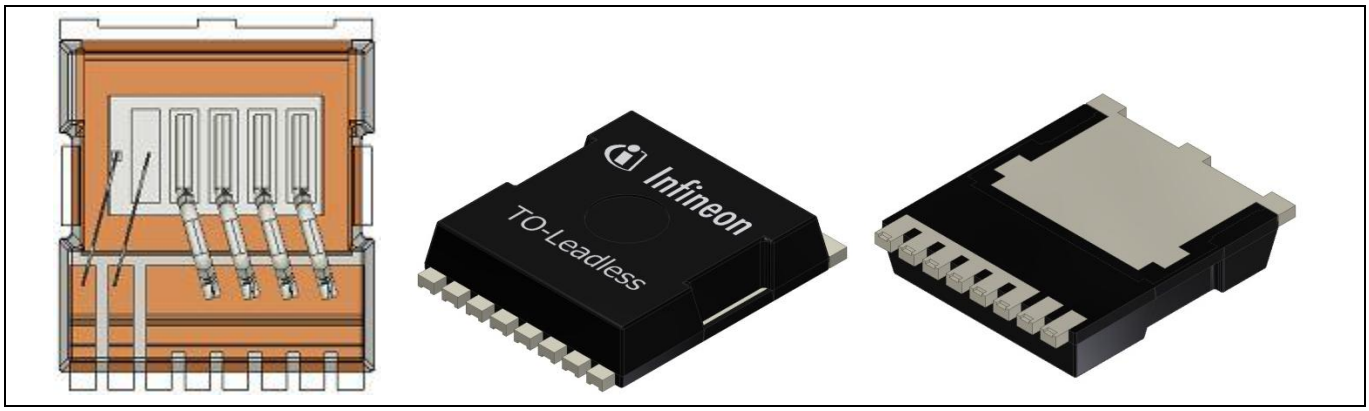


Figure 5 TOLL drawing from inside, top and bottom view

The small mechanical dimensions allow compact designs to be realized. The high current capability combined with the low thermal resistance (R_{thJC}) results in lower chip temperatures and therefore enables the designer to achieve higher power density and higher reliability.

One of the best quality aspects of the TOLL package is the TCOB (thermal cycling on board) reliability - especially when focused on FR4 PCB assembling. Please refer to the separate section in this document for more information about TCOB.

All mechanical details shown in the following chapters and a general recommendation on how to handle Infineon's SMD devices can be found at www.infineon.com/packages.

Detailed mechanical information about the TOLL (P/PG-HSOF-8-2) is also available at http://www.infineon.com/cms/en/product/package.html?package=/packages/SMD_-_Surface_Mounted_Devices/P-PG-HSOF/.

Note: The TOLL package will be one of the packages of choice for Infineon's future CoolGaN™ portfolio.

2 The combination of G7 and TOLL

The combination of the 600 V CoolMOS™ G7 with the TOLL package is a very powerful combination.

The improved silicon G7 technology offers better switching performance which reduces the switching losses when compared with devices of the same $R_{DS(on)}$. Due to the very low switching losses, the technology is predominantly used to increase the switching frequency in order to reduce the size of the magnetic components, which offers significant cost reduction and increased power density.

The TOLL SMD package accepts an increased size silicon chip inside and offers 4-pin functionality in order to optimize the switching behavior. The lowest $R_{DS(on)}$ offered in the TOLL package is 28 mΩ compared to 40 mΩ in the TO-220 or D²PAK for the same voltage rating.

2.1 R_{thJC} improvement

The thermal resistance (R_{thJC}) of the device is a very important measure for the cooling performance of the device. The R_{thJC} improvement of G7 is shown in Figure 6. For the same $R_{DS(on)}$, there is a 20% improvement achieved.

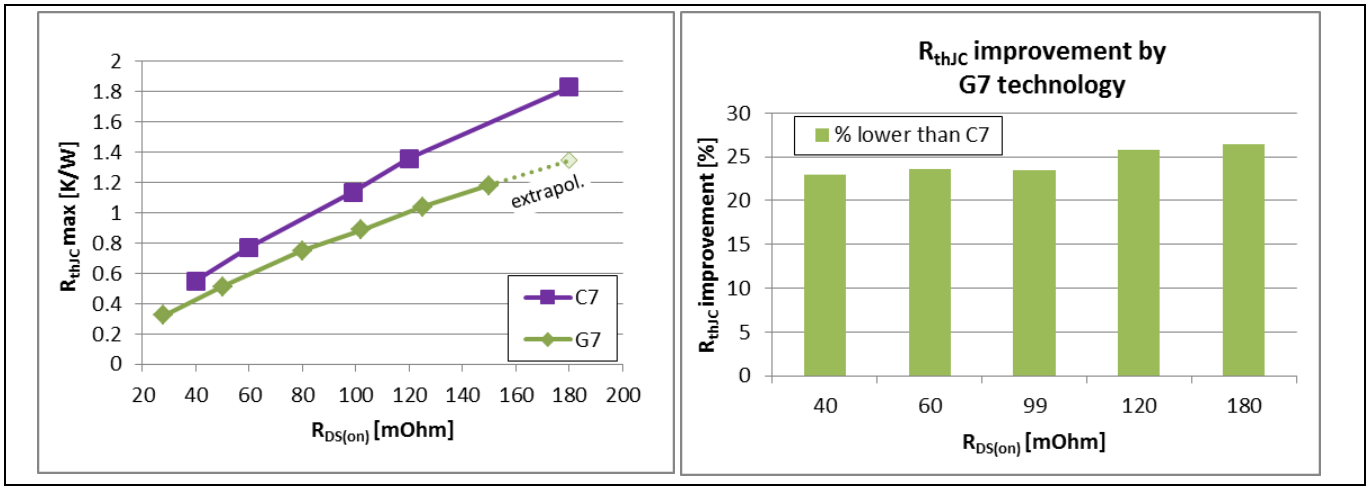


Figure 6 R_{thJC} vs. $R_{DS(on)}$ comparison between G7 in TOLL and C7 in D²PAK package

The R_{thJC} improvement shown in Figure 6 results (according the equation shown in Figure 7) in lower silicon temperatures for same level of heat transfer or power losses. The chart on the right shows the normalized improvement as a percentage, based on interpolated $R_{DS(on)}$ for G7 devices compared to the $R_{DS(on)}$ offered by C7 technology. According to the equation shown in Figure 7, one can conclude that a lower R_{thJC} will result in a lower device temperature, which in turn reduces conduction losses, as $R_{DS(on)}$ significantly increases with the temperature of the device.

$$R_{thJC} = \frac{\Delta_T}{P_v} \gg \Delta T = R_{thJC} \times P_v$$

Figure 7 R_{thJC} impact on temperature difference

Knowing the lower temperature of the device, it is possible to either reduce the cooling effort or to increase the power range for a given application configuration. Alternatively, a design engineer might consider increasing the reliability by maintaining a lower temperature within the whole system.

2.2 4-pin functionality

The TOLL package offers six source connections for the drain current and one source sense connection for the gate reference potential. This source sense connection is designed for the gate charging power and should not be used to carry the main drain current, as it does not have the current-handling capability of the other six power source connections. It is possible to connect all the source connections (power and sense) together without using the 4-pin functionality of the package.

The most important reason to use a separate source sense pin for controlling the gate is to improve the efficiency by reducing switching losses and therefore, minimizing heat generation. Reducing switching time is a well-understood method for improving efficiency – the faster a switch turns on and off, the shorter the time period during which a voltage exists across it and a current is flowing through it. Voltage multiplied by current is equal to power (loss), hence a switch that spends less time dissipating power is by definition a more efficient switch.

In addition to the important advantage of the 4-pin functionality, the gate waveforms will be much cleaner by using the source sense connection as the drain current will cause induced voltage spikes in the driving circuit of the gate. For the 4-pin setup shown in the right schematic of Figure 8, the power source inductance will not feed back into the driving circuit as would happen in the standard configuration with only a single source connection to the MOSFET, as shown in the left schematic of Figure 8.

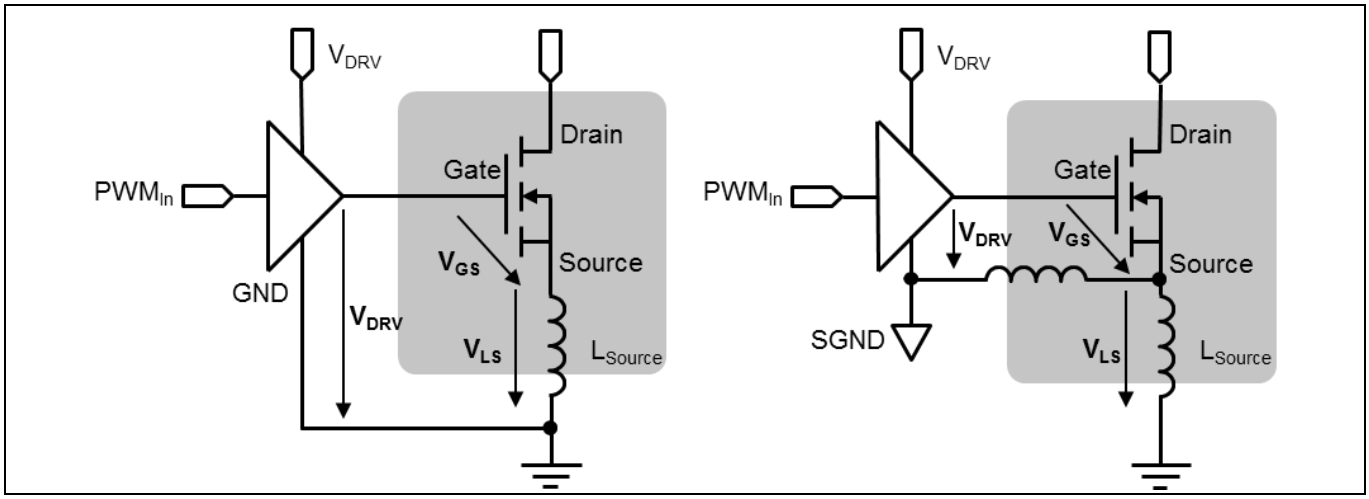


Figure 8 Driving scheme comparison for standard and 4-pin setup

Due to the low pin inductance of the TOLL package (approximately 1 nH), the bouncing of the signal ground is much lower compared to the TO-247 4-pin package, where the source inductance is in the range of 15 nH. The higher inductance causes higher voltage spikes during the turn-on and turn-off of the transistor.

2.3 Improved switching performance has impact to $R_{DS(on)}$ selection

As discussed in the earlier sections of this document, the G7 has reduced switching losses compared to equal $R_{DS(on)}$ of other earlier developed technologies. This has an important impact on the selection of the optimized $R_{DS(on)}$ for a given power class in a certain topology.

There is a very important phenomenon driving overall losses to an optimum when the switching losses are equal to the conduction losses, as shown in Figure 9. Both types of loss depend on the chip area. As the chip size increases, $R_{DS(on)}$ will decrease with a square function and switching losses will increase linearly.

For hard switching topologies, the switching losses are a combination of turn-on and turn-off losses. For the turn-off losses, C_{OSS} is the root cause for E_{OSS} which is needed to charge the output capacitance. This capacitance will be shorted by the MOSFET once the device is turned on again and therefore, be converted into heat. In order to reduce complexity and to minimize the impact of the gate resistor for the switching losses, the calculation for Figure 9 uses only E_{OSS} and ignores other switching losses as they are also determined by the current and the gate resistor. This means that the final switching losses will be higher than the capacitive switching losses shown in this chart.

Out of this loss comparison, designers can conclude that for technologies with improved switching losses, the optimum $R_{DS(on)}$ for a certain power range will be found at lower $R_{DS(on)}$, provided the switching frequency is not increased at the same time. This can be clearly seen in Figure 9 where the crossing point between the C_{OSS} related capacitive losses and the $R_{DS(on)}$ related conduction losses lies at a lower $R_{DS(on)}$ value for the G7 technology due to its improved switching losses.

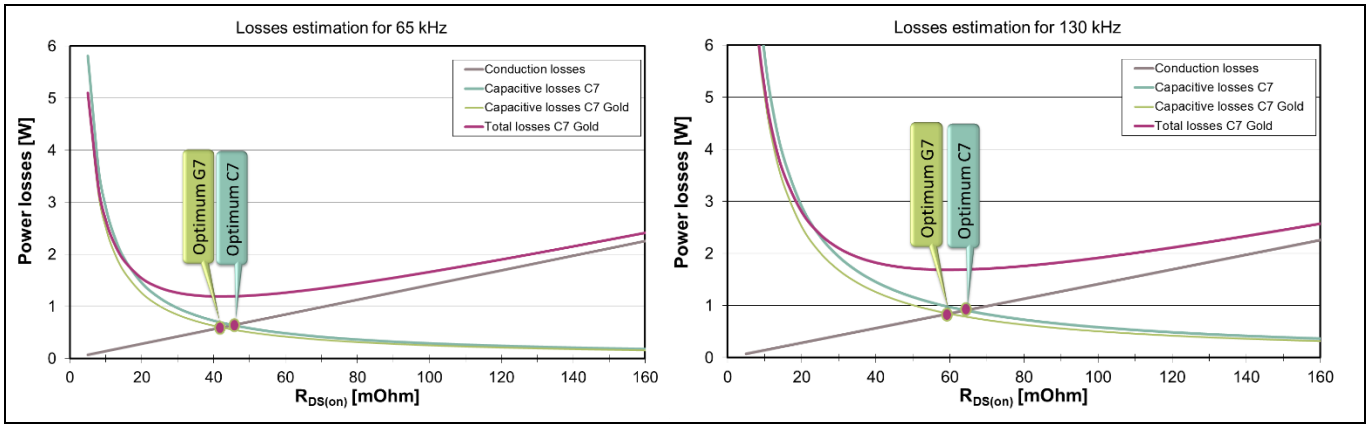


Figure 9 C_{oss} and $R_{DS(on)}$ based losses calculation for 65 kHz and 130 kHz

It can also be seen in Figure 9 that for higher switching frequencies, the optimum $R_{DS(on)}$ is also higher. To increase the switching frequency in a given application without losing efficiency, it is very important to use MOSFET technologies that offer lower switching losses for the same $R_{DS(on)}$. The new G7 technology follows this strategy.

The new G7 technology supports this by introducing nominal $R_{DS(on)}$ ranges, as shown in Figure 10.

$R_{DS(on)}$ max. [mΩ]	TOLL G7 600V
150	IPT60R150G7
125	IPT60R125G7
102	IPT60R102G7
80	IPT60R080G7
50	IPT60R050G7
28	IPT60R028G7

Figure 10 Portfolio of G7 products

Having the 28 mΩ device in the portfolio allows SMD devices to be used for higher power ranges in applications which were dominated by trough hole devices in the past (that is, 3 kW in a standard CCM PFC). By the combination of lower $R_{DS(on)}$ and improved switching losses, the G7 has lower overall power losses and, therefore, the cooling of the devices is much easier. This is described in the following sections in more detail.

2.4 Low C_{oss} dissipation factor

Every capacitor technology has a dissipation factor (tanð=ESR*ωC) from which a practical capacitor has a series resistor ESR. Similarly, superjunction MOSFETs also can be simply modeled with a series output resistance (R_{oss}), Figure 11, resulting in some dissipated energy during charging and discharging the C_{oss}.

600V CoolMOS™ G7 series is optimized for low C_{oss} energy dissipation. This is evident by the higher dv/dt, which can be explained by the efficient charging of the C_{oss}, and by being less damped by any structure impedance (R_{oss}).

Moreover, the energy dissipated in R_{oss} during charging and discharging C_{oss} is a function of the passing charge Q_{oss}. Since 600 V CoolMOS™ G7 is featured with lowest Q_{oss}, shown in Figure 4, this result in a further reduction in C_{oss} dissipated energy.

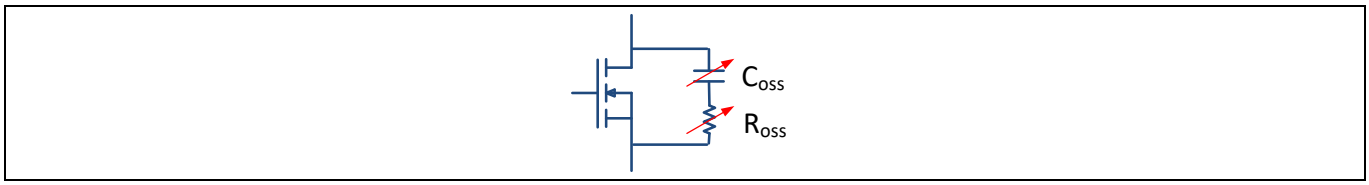


Figure 11 Schematic C_{oss} circuit

This feature plays a significant role in soft-switching applications, such as resonant LLC circuits, where in theory the E_{oss} is completely recycled, while in reality, the inclusion of the C_{oss} dissipation affects the effectiveness of soft switching. Especially at high switching frequencies, the C_{oss} dissipation energy is important to be minimized, as it determines what portion of the E_{oss} is practically dissipated rather than recycled back.

This low C_{oss} dissipation energy resulted in performance improvement shown in Figure 40 by the efficiency comparison of a 600 W LLC circuit. The light load improvement is mostly related to the low C_{oss} dissipation, since other switching losses are minimal when operating at the resonant frequency.

2.5 Rugged body diode

The 600 V CoolMOS™ G7 body diode ruggedness was tested and proved a maximum dv/dt rating of 25 V/ns. Furthermore, its hard commutation was characterized in a double-pulse test fixture as shown in Figure 12. The high side MOSFET is turned on to ramp the choke current to the specific value to be tested. When the high side MOSFET is turned off, the choke current will freewheel through the body diode of the low side MOSFET (DUT). After short freewheeling time, the high side is turned on again causing the low side diode to hardly commutate the current and a negative reverse recovery current spike is seen in the diode current waveform (LS_ISD), as in Figure 13.

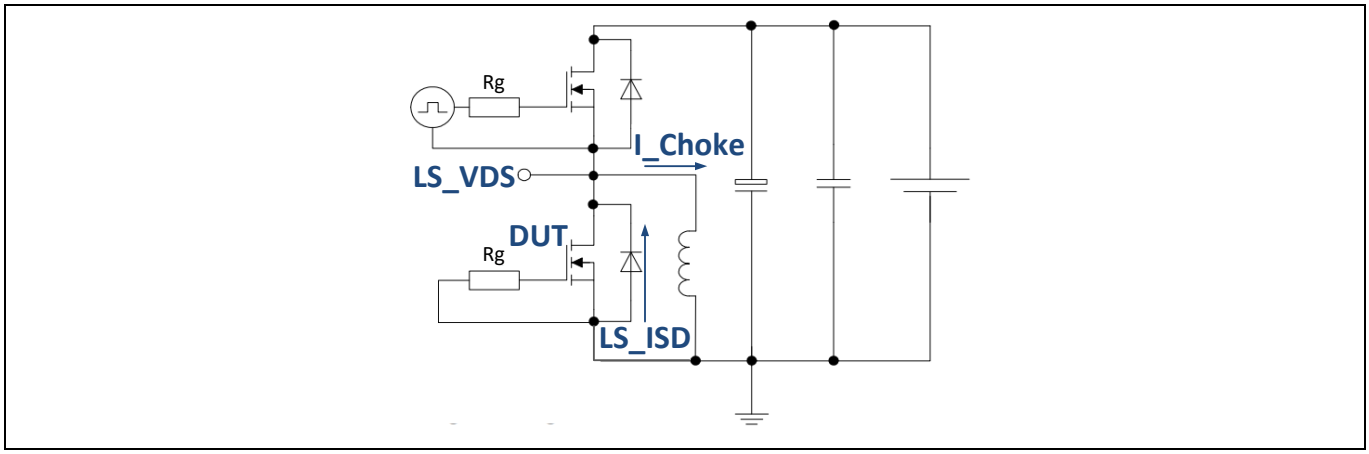


Figure 12 Double pulse circuit for testing diode characteristics

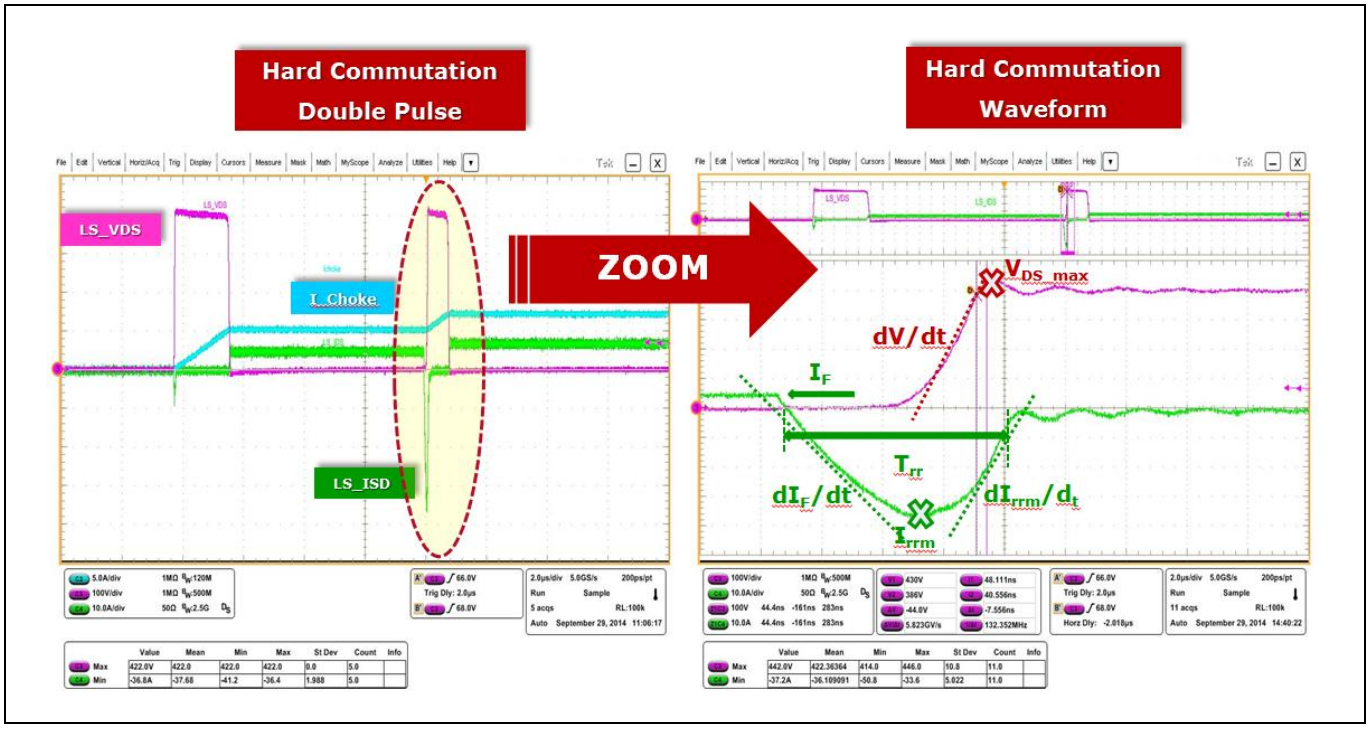


Figure 13 Diode hard commutation waveform in a double pulse test circuit

One can see the dv/dt rating of the 600 V CoolMOS™ G7 already very close to such devices having fast body diode. Nevertheless, the designer should take care to minimize such hard commutation events and their current level as far as possible to limit the stress for the whole application.

3 PCB assembly considerations for TOLL

The assembly process for SMD devices offers advantages in mass production. Firstly, SMD devices save space on the board and secondly the placement can be automated while most THD are inserted manually which increases cost and reduces quality.

The PCB design and construction are key factors for achieving highly reliable solder joints. For example, TOLL packages should not be placed in the same location on opposite sides of the PCB (if double-sided mounting is used), because this results in a stiffening of the assembly which can lead to earlier solder joint failure when compared to a design where the component locations are offset. Furthermore, it is known that board stiffness has a significant influence on the reliability (temperature cycling) of the solder joint, if the system is used in fluctuating temperature conditions.

The outline of the TOLL devices is shown in Figure 14. More detailed information about the physical dimensions is available in the relevant datasheet(s) on the Infineon website.

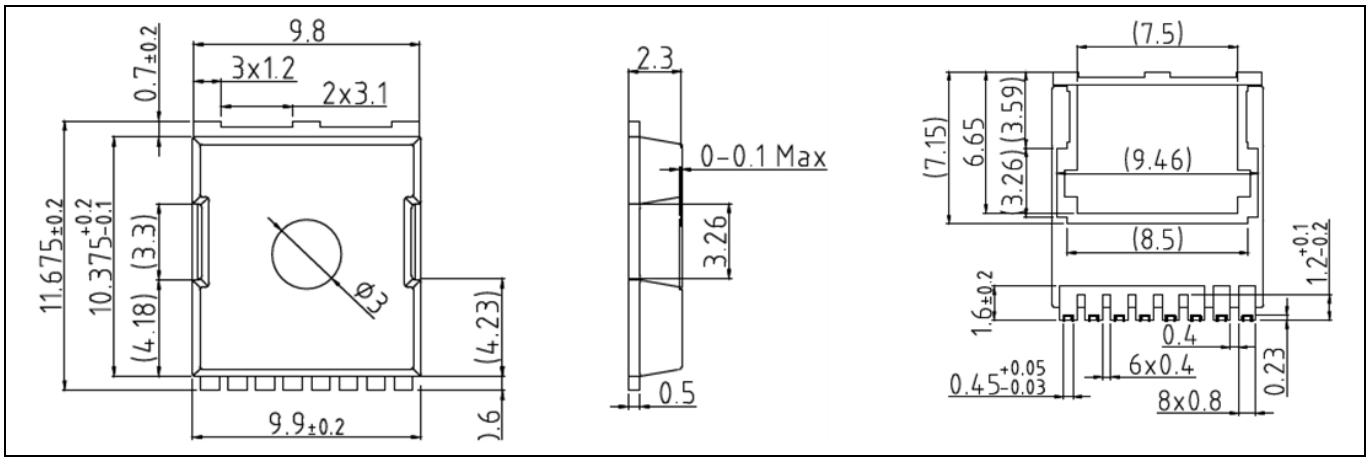


Figure 14 Outline drawing of the TOLL (HSOF-8-2)

Figure 15 shows the recommended PCB pad designs (including appropriate dimensions) for TOLL. This design is also used for thermal cycling on board (TCOB) testing according to IPC9701A standard at Infineon.

Please note that the recommendations can only give dimensions for the solder-mask openings. Generally, the copper dimensions depend on the capability of the board manufacturer. For high current applications, the copper dimensions for drain and source pads should be as large as possible to increase the conductor cross-sectional area.

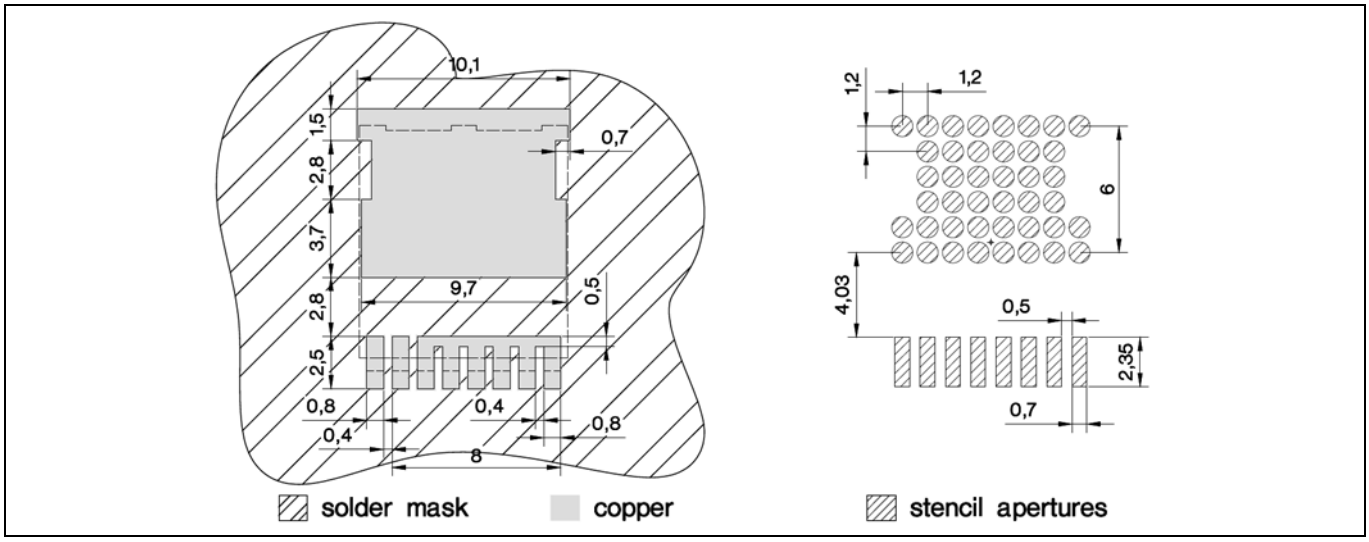


Figure 15 Footprint and stencil recommendation for PCB assembling

To connect the drain pad directly (thermally and electrically) to inner and/or bottom copper planes of the board, plated-through vias can be used. These vias help to distribute the heat into the board area, which spreads from the chip directly through the drain contact. Locating vias too near to (or within) the open solder mask can lead to solder wicking and could result in soldering issues and/or reduced reliability.

Thermal and electrical analysis and/or testing are recommended to determine the optimum number of vias needed for a specific application.

3.1 Lead design for manufacturing support

Conventional leadless packages such as ThinPAK, DirectFET™ or SuperSO8 are not compatible with automatic optical inspection (AOI) because the solder joints are (partially) hidden under the package.

The connections of the TOLL package feature special grooves (as shown in Figure 16), located on the bottom side of the gate and source pins. The trapezoidal grooves lead to a visible solder joint, avoiding the necessity of an expensive X-ray inspection. The grooves also increase the wetting of the solder and therefore, enhance the performance of the solder joint.

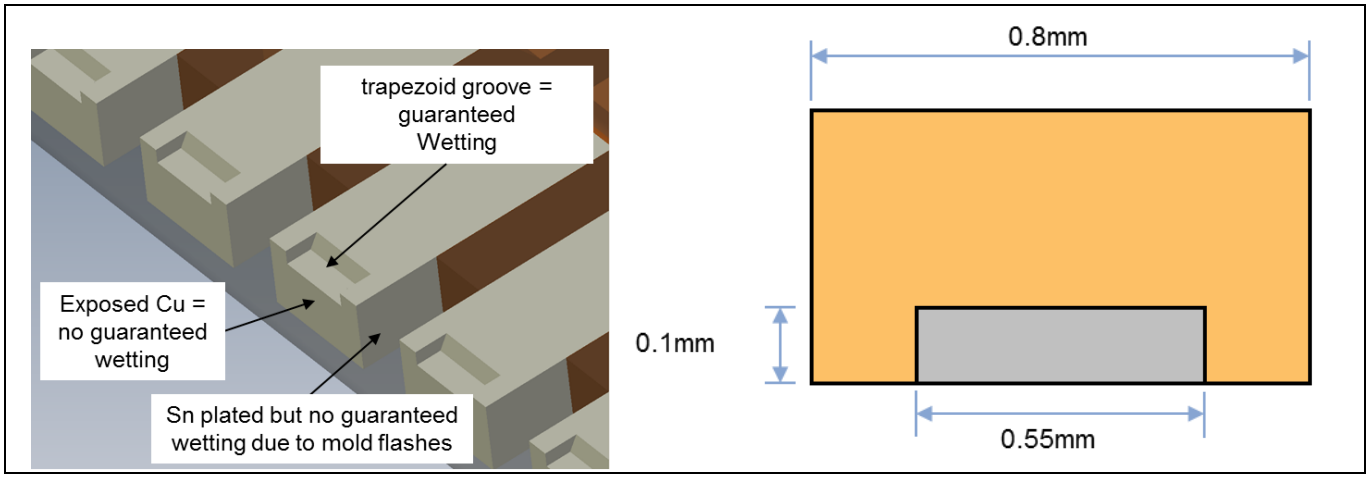


Figure 16 Grooves in the pins enhance better soldering

After soldering, it is easy to identify a good solder joint using standard AOI. In Figure 17, a typical result of soldering is highlighted. Cutting through a source connection shows the solder (light yellow). The groove is completely filled and additionally, a solder meniscus is visible on the left, allowing an assessment of the solder connection.

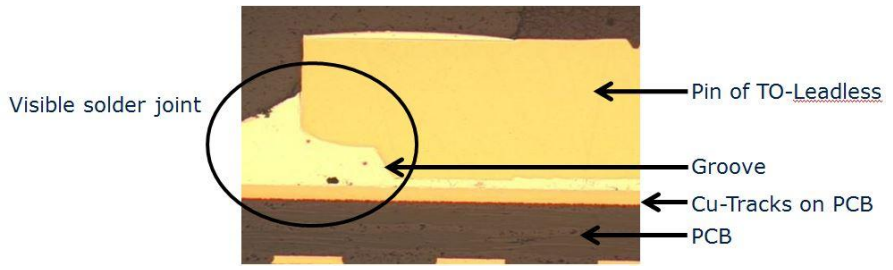


Figure 17 Visible solder meniscus allows a simple AOI inspection

3.2 TCOB reliability of the TOLL package

IPC9701 defines thermal cycling test at the PCB level. The TCOB test is designed to detect failure modes, which are due to the thermo-mechanical mismatch between devices and printed circuit board (PCB). These are mainly solder joint fatigue, but also potential internal package defects from the stress related to the CTE (coefficient of thermal expansion) mismatch to the PCB (for example, delamination's, cracks and so on).

A standard failure criteria during in-situ-monitoring is a resistance increase of the daisy chain (contact resistance monitoring between two contacts) of more than 20% (according to IPC9701A). In the case of very small daisy-chain resistances, a higher resistance threshold is used and documented within the test report.

Topic	Description		Comment
	Value	Unit	
Test Vehicle			
PG-HSOF-8-2	10 x 12	mm²	
Chip	25	mm²	MOSFET
Stress Boards			
Board material	a) high T_g FR4 b) IMS	-	a) Std. TCoB test board PMM b) For high power application
Board thickness/ layer	a) 1.6 mm/ 4-layer b) 3.2 mm IMS	-	
Finishing	Chem. Sn	-	
Solder material	SAC305	-	
Stencil thickness	120	µm	
Stress Condition			
Temperature range	-40° C ... 125° C	° C	1 cycle/ hour according to IPC 9701
Monitoring	Electrical readout & Cross sectioning	-	Online readout

Figure 18 TCOB test setup for TOLL

In Figure 18, the setup for the TCOB test is shown. The tests were performed for 4-layer PCB and IMS (isolated metal substrate).

Reviewing the test results of the TCOB based on the table in Figure 18:

- For the PCB version: no electrical failure and no optical objection detected up to 10,000 cycles

- For the IMS version: no electrical failure and no optical objection detected up to 896 cycles

Due to higher thermo-mechanical mismatch, lifetime of the IMS assembly is reduced significantly with respect to assembly on FR4 PCB.

3.3 Creepage and clearance

According to UL/EN60950, the minimum distance between electrical connections for SMPS is defined as follows:

- Creepage: The distance upon the surface between two electrically conductive areas is called creepage. The minimum creepage distances depend on the real RMS working voltages
- Clearance: The clearance is defined as the shortest direct distance between two electrically conductive areas without any other material in between. Minimum clearance distances depend on peak working voltages

Distances between electrically conductive areas shall be so dimensioned that overvoltages, including transients, which may enter the equipment, and peak voltages which may be generated within the equipment, do not break down the function or safety of the device for a given pollution degree.

Comparing the minimum distances between drain and other connections of the device, one can see in Figure 19 that the TOLL with its 2.7 mm is offering more safety margin than the very popular TO-247 package with 2.54 mm clearance. Therefore, the TOLL package is perfectly suitable for replacement of any TO-247 device.

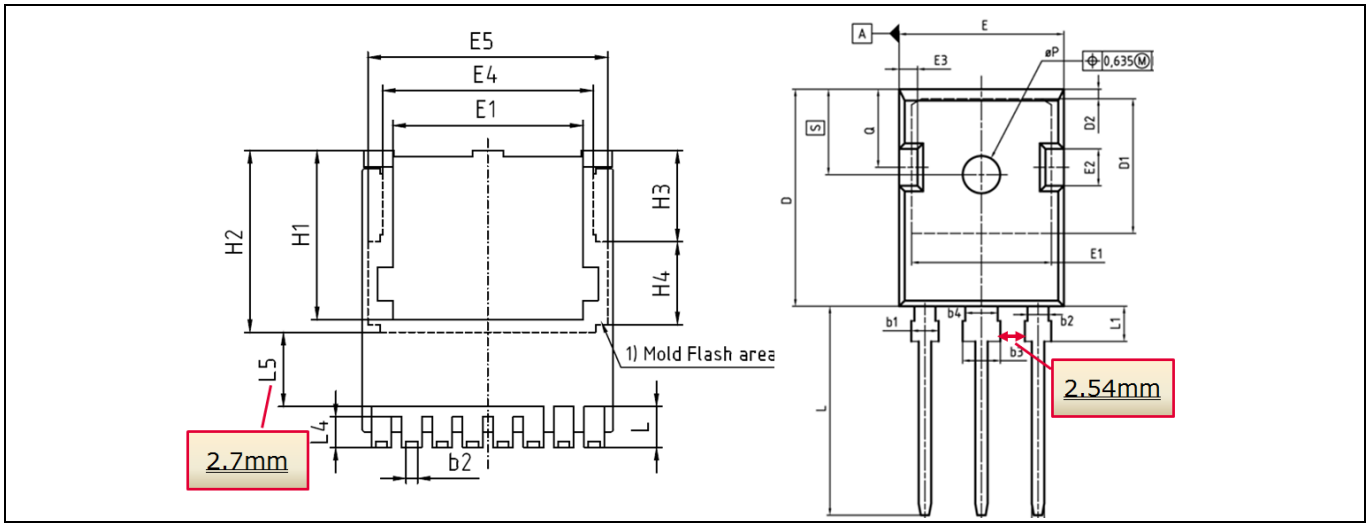


Figure 19 Comparison of TOLL and TO-247 clearances

3.4 Storage and transportation conditions

Improper transportation and unsuitable storage of components can lead to a number of issues during subsequent processing, including poor solderability, delamination, and package cracking effects.

The following standards should be considered:

- IEC 60721-3-0 classification of environmental conditions: Part 3: Classification of groups of environmental parameters and their severities; introduction
- IEC 60721-3-1 classification of environmental conditions: Part 3: Classification of groups of environmental parameters and their severities; Section 1: Storage

- IEC 60721-3-2 classification of environmental conditions: Part 3: Classification of groups of environmental parameters and their severities; Section 2: Transportation
- IEC 61760-2 surface mounting technology – Part 2: Transportation and storage conditions of surface mounting devices (SMD) – Application guide
- IEC 62258-3 semiconductor die products – Part 3: Recommendations for good practice in handling, packing, and storage
- ISO 14644-1 clean rooms and associated controlled environments - Part 1: Classification of airborne particulates

Maximum storage time: The conditions to be complied with to ensure issue-free processing of active and passive components are described in IEC 61760-2.

3.5 Moisture sensitivity level (MSL)

For moisture-sensitive packages, it is necessary to control the moisture content of the components. Penetration of moisture into the package molding compound is generally caused by exposure to ambient air. In many cases, moisture absorption leads to moisture concentrations in the component that are high enough to damage the package during the reflow process. Thus, it is necessary to dry moisture-sensitive components, seal them in a moisture-resistant bag, and only remove them immediately prior to assembly to the PCB. The permissible time (from opening the moisture barrier bag until the final soldering process) that a component can remain outside the moisture barrier bag is a measure of the sensitivity of the component to ambient humidity (moisture sensitivity level, MSL). The most commonly applied standard IPC/JEDEC J-STD-033* defines eight different MSLs (see Figure 20). Please refer to the “Moisture sensitivity caution label” on the packing material, which contains information about the moisture sensitivity level of our products. IPC/JEDEC-J-STD-20 specifies the maximum reflow temperature that shall not be exceeded during board assembly.

Level	Floor Life (out of bag)	
	Time	Conditions
1	Unlimited	≤30°C/85% RH
2	1 year	≤30°C/60% RH
2a	4 weeks	≤30°C/60% RH
3	168 hours	≤30°C/60% RH
4	72 hours	≤30°C/60% RH
5	48 hours	≤30°C/60% RH
5a	24 hours	≤30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤30°C/60% RH

Figure 20 Moisture sensitivity levels (according to IPC/JEDEC J-STD-033, RH=relative humidity)

If moisture-sensitive components have been exposed to ambient air for longer than the permitted time according to their MSLs, or the humidity indicator card indicates too much moisture after opening a moisture barrier bag (MBB), the components must be baked prior to the assembly process. Please refer to IPC/JEDEC J-STD-033* for details. Baking a package too often can cause solderability issues due to oxidation and/or intermetallic growth upon the open contact areas. In addition, packing material (such as, trays, tubes, reels, tapes, and so on) may not withstand higher baking temperatures. Please refer to imprints/labels on the packing to determine the maximum allowable temperature.

For Pb-free components, two MSLs can be given: One for a lower reflow peak temperature (Pb-containing process) and one for a higher reflow peak temperature (Pb-free). Each one is valid for the respective application.

The new G7 technology supports highest moisture sensitivity level MSL1. Therefore, it can be shelfed in this respect for unlimited time.

4 Thermal handling

Working with SMD devices can be very challenging if they are used for high power applications where high-power losses are expected. Naturally, the power losses will convert into heat. For standard SMD devices, it is necessary to extract this heat towards the soldering area on the PCB as the package itself is mostly isolated on the top side by the mold compound itself.

For the selection of the proper cooling method, the designer will consider the art of PCB and the environment of the devices. In the case of single layer PCB, the solution will be different for one on more layer board as discussed in the following sections.

4.1 SMD cooling for single layer board

Several applications in cost-driven markets have been using single-layer PCBs due to cost constraints for many years. In the past, all power devices were available only in through-hole device (THD) versions; however, this is now increasingly changing to SMD solutions. Therefore, the common cooling concept for power devices by assembling them to a heatsink while having the copper trace and soldering on the other side of the PCB, as shown in left image of Figure 21, does not work any longer. SMD devices must be soldered directly to the copper side of the PCB, and in most cases, the heatsink should be placed on the opposite side, where there is more vertical space available for other components such as inductors and capacitors.

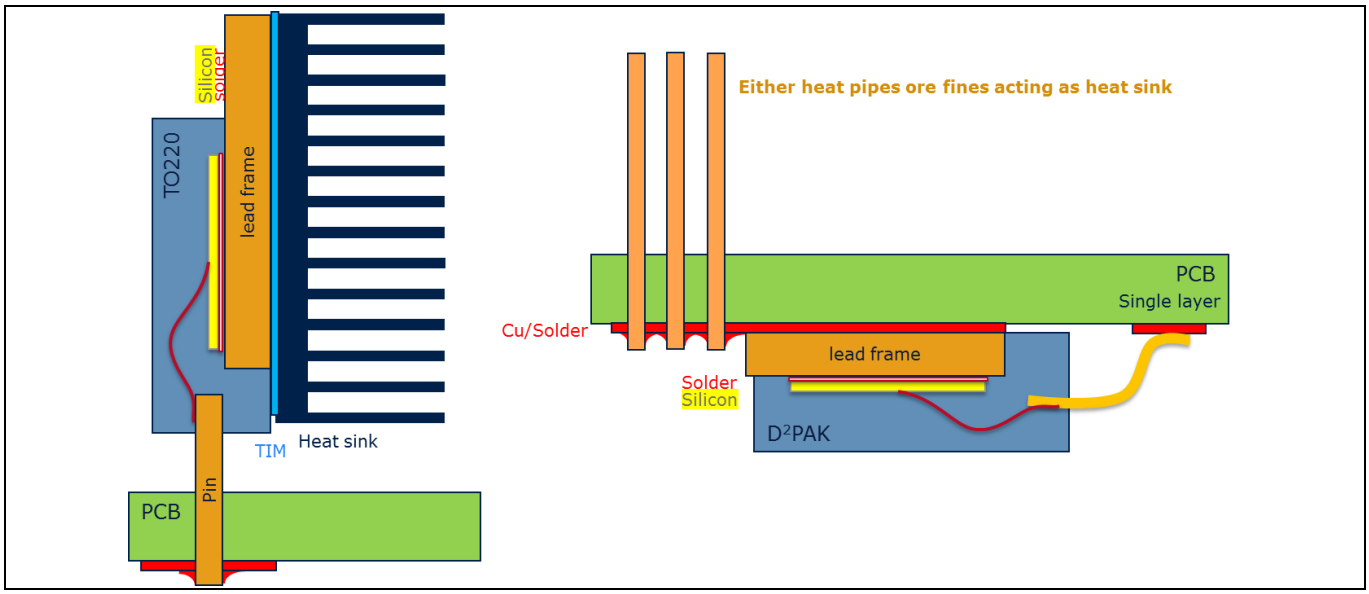


Figure 21 Schematic for conventional THD cooling on the left side versus SMD cooling on the right side

The heat produced in the SMD device, as shown in the right-side picture in Figure 21 will be transported either by heat pipes or by heat fines to the top side. The material for this kind of heat sink can either be made of copper or any other thermal conductive metal, plated with tin to offer good solderability. Besides this, it is also possible to coat this metal with some isolation layer to prevent electrical sparking to any other component.

Furthermore, one can modify the shape of such heat sink to any shape, fitting best to the available space on the PCB.

4.2 Cooling through the PCB

The first method for the SMD cooling strategy on multi-layer board comes most of the time to the cooling through the PCB. Such a system could look like the one shown in Figure 22, where the PCB must consist of at least two copper layers, and the heatsink is placed on the opposite side.

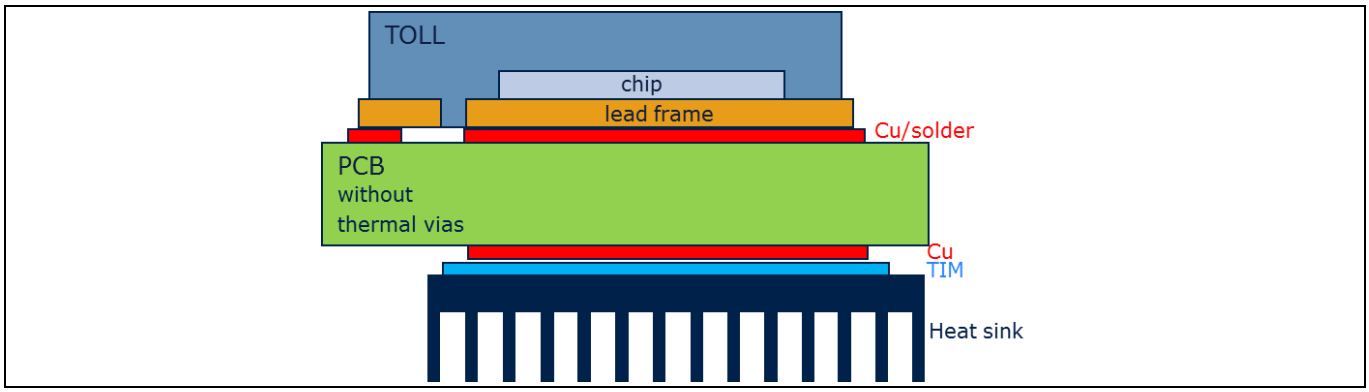


Figure 22 Schematic PCB assembly for TOLL on two-layer FR4 board

In normal cases such as the one shown in Figure 22, the additional thermal resistance of the PCB will dominate the overall R_{th} of the cooling path and therefore, limit the maximum power range for using SMD devices. Therefore, it is important to have a closer look at the thermal system of the application. To get a clearer idea of the thermal system, Table 2 shows the thermal resistance breakdown for the single layer of the whole stack.

To understand the bottleneck for the thermal resistance of the whole system, one can consider the size of the soldering area of the SMD device for the cooling path. In case of TOLL, this area is shown in Figure 15 and is approximately 80 mm^2 (8 mm x 10 mm).

Table 2 R_{th} breakdown for IPT60R028G7 assembly based on Figure 22

Layer	λ [W/(m*K)]	Thickness [mm]	Rth [K/W]
IPT60R028G7	na	2.2	0.32
Solder (Sn/Ag –mixture)	50	0.05	0.038
80 mm^2 Copper (Cu)	400	0.07	0.0022
PCB (FR4)	0.3	1.6	66.67
80 mm^2 Copper (Cu)	400	0.07	0.0022
(Solder resist)	(0.25)	(0.05)	(2.5)
Isolation foil TIM (K10)	0.8	0.15	2.38
Heat sink (SK 566)	300	na	5
Total system	**na**	**na**	**74.41 (76.91)**

It is very crucial to not coat the copper plane on the heat sink side with solder resist as this will also increase the total resistance of the thermal path as shown by the entries with brackets in Table 2. Such solder resist would increase the system R_{th} by another 2.5 K/W and will not help to increase the electrical isolation on the other hand. Therefore, all the cooling systems with heat sink in this document refer to solder resist free cooling path.

From Table 2, the total thermal resistance is 74.41 K/W and is dominated by the thermal resistance of the PCB. According to the equation shown in Figure 23, the R_{th} of the thermal system will be improved linearly by reducing the PCB thickness linearly. Such a reduction of the PCB thickness is limited by the desired mechanical

stability of the system. To minimize this stability issue, the use of daughter boards can be considered for high power devices.

A well-established technique to increase the area of the thermal path through the PCB is to apply copper planes on both sides of the PCB to spread the heat transfer to a larger area.

$$R_{th} = \frac{\mathrm{d}}{\lambda \times A}$$

Figure 23 Thermal resistance for heat dissipation

Where,

d is the thickness of plain [m]

λ is the specific thermal conductivity [W/mK]

A is the area of heat flow [m^2]

There are some challenges to consider when increasing the area for heat transport though the PCB such as parasitic capacitance due to the coupling of the heatsink and power density limitations.

4.2.1 Reducing the thermal resistance of the PCB by vias and copper planes

To reduce the thermal resistance of the system, the use of thermal vias and copper planes for heat spreading is a well-established technique for SMD assemblies.

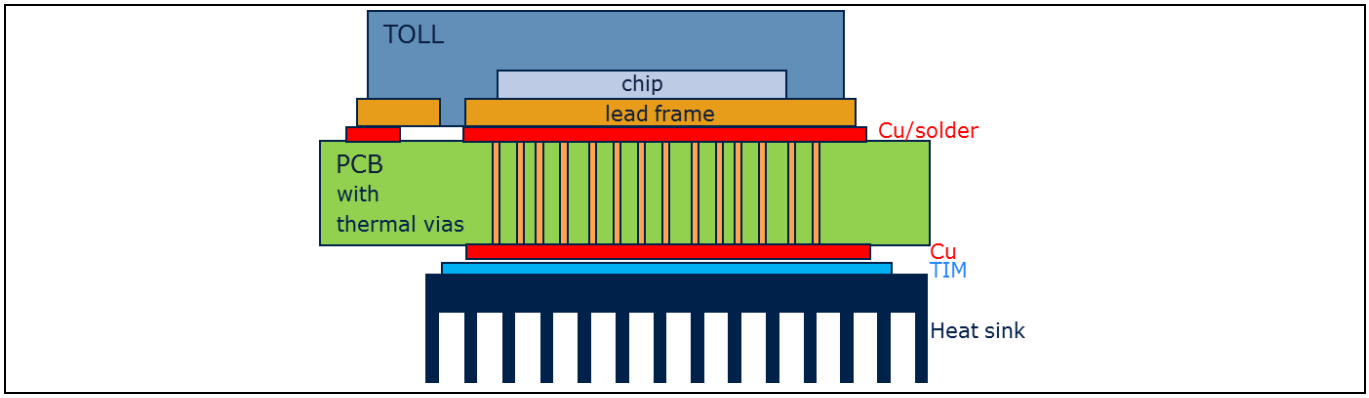
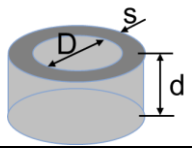


Figure 24 Schematic PCB assembly for TOLL with thermal vias on FR4 board

The dimension of the thermal vias offers a lot of opportunities for the designer. In our experience, the optimum diameter of the vias is in the range of 0.3 mm to 0.5 mm as this size does not add additional cost to the PCB manufacture as it would for smaller diameters. In parallel, this allows use of spot masks for the soldering process. It is important to not allow solders to reach the opposite copper plane as it must remain flat for applying the heat sink. The thermal interface material has limited capability to level any surface roughness.

For the distance between the vias, there is a sweet spot in the range of 0.5 mm to 1 mm. The calculation in Table 3 is based on vias with 0.3 mm diameter and a stepping of 1 mm. Additionally, there is an overlay of a matrix shifted by half the stepping distance which defines a final diagonal distance between each via of 0.7 mm. With this arrangement a total of 160 vias are recommended for the 80 mm^2 soldering area of the TOLL.

The thermal resistance of one single via is calculated, as shown in Figure 25. For the calculation in Table 3, the R_{th} of a single via results in a value of 108.6 K/W.



$$R_{th,via} = \frac{d}{\lambda \pi s(D+s)}$$

Figure 25 R_{th} of thermal vias

Where,

d is the thickness of PCB [m]

λ is the specific thermal conductivity [W/mK]

s is the thickness of the side wall coating [m]

D is the diameter of the via [m]

Table 3 R_{th} breakdown for IPT60R028G7 assembly based on Figure 24

Layer	λ [W/(m*K)]	Thickness [mm]	Rth [K/W]
IPT60R028G7	na	2.2	0.32
Solder (Sn/Ag –mixture)	50	0.05	0.038
80mm² Copper (Cu)	400	0.07	0.0022
PCB (FR4 including 160 thermal vias with 0.3 mm)	na	1.6	0.68
80 mm² Copper (Cu)	400	0.07	0.0022
(Solder resist)	(0.25)	(0.05)	(2.5)
Isolation foil TIM (K10)	0.8	0.15	2.38
Heat sink (SK 566)	300	na	5
Total system	**na**	**na**	**8.46 (10.96)**

In Table 3, the improvement from introducing thermal vias is demonstrated as compared to Table 2. The total R_{th} of the system is reduced to 8.46 K/W from the previous 74.41 K/W. This is a significant improvement by 88.6% or in other words only 11.4% of the R_{th} without thermal vias.

In this version with the thermal vias, one can see the impact of having solder resist between the copper plane and the TIM will cause the R_{th} of the total system to increase by 29.5%. Besides the additional thermal resistance of the solder resist, it will also reduce the mechanical force applied to the TIM, which also might affect the thermal performance of the thermal interface as most of the material increase the performance with the pressure applied. Therefore, we suggest designing the solder resist free area according to the shape of the TIM sheet if possible.

4.2.2 Thermal management of PCB by means of HSP (Heat Sink Paste) and TIP (Thermal Interface Paste)

The need to dissipate the heat generated from the component can be satisfied in different ways. For those applications where the amount of heat does not require a mechanical heat sink (with its additional costs and space requirements), but the FR4 substrate is not sufficiently dissipative in itself, the application of a specific thermo-dissipative paste is a viable solution. The dissipative paste distributes and transfers the heat to the

surrounding environment. The paste is applied by screen printing during the construction of the bare PCB, and will partially fill the thermal vias, thus improving their performance.

Thermo-dissipative paste is also resistant to reflow and wave soldering, allowing a considerable time and cost saving for the assembly process when compared to thermo-dissipative preformed interface solutions applied after soldering.

As well as its thermal properties (thermal conductivity equal to 2 W/mK), the paste also has good electrical insulation (30 kV/mm) properties.

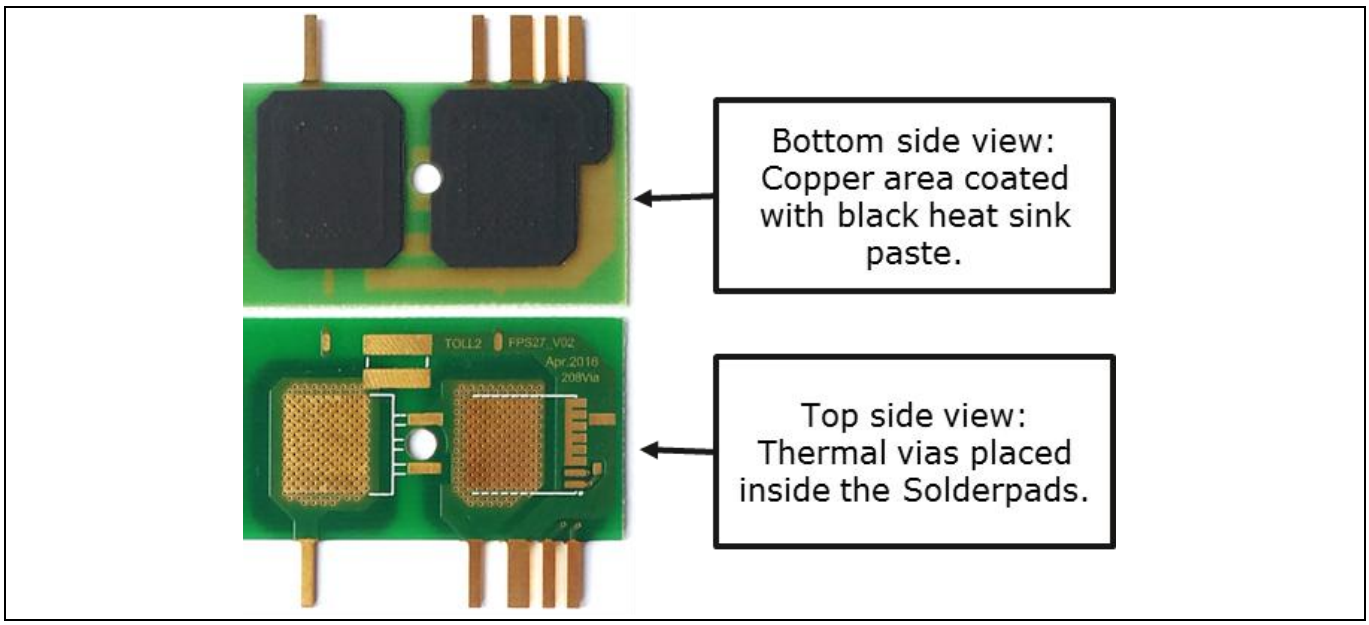


Figure 26 Daughter PCB with heat sink paste

For applications where the amount of heat requires a mechanical heat sink, the thermal coupling can either be designed like conventional THD solutions, or use the thermal interface paste as shown in Figure 23 which offers some additional value in respect of handling and automatization.

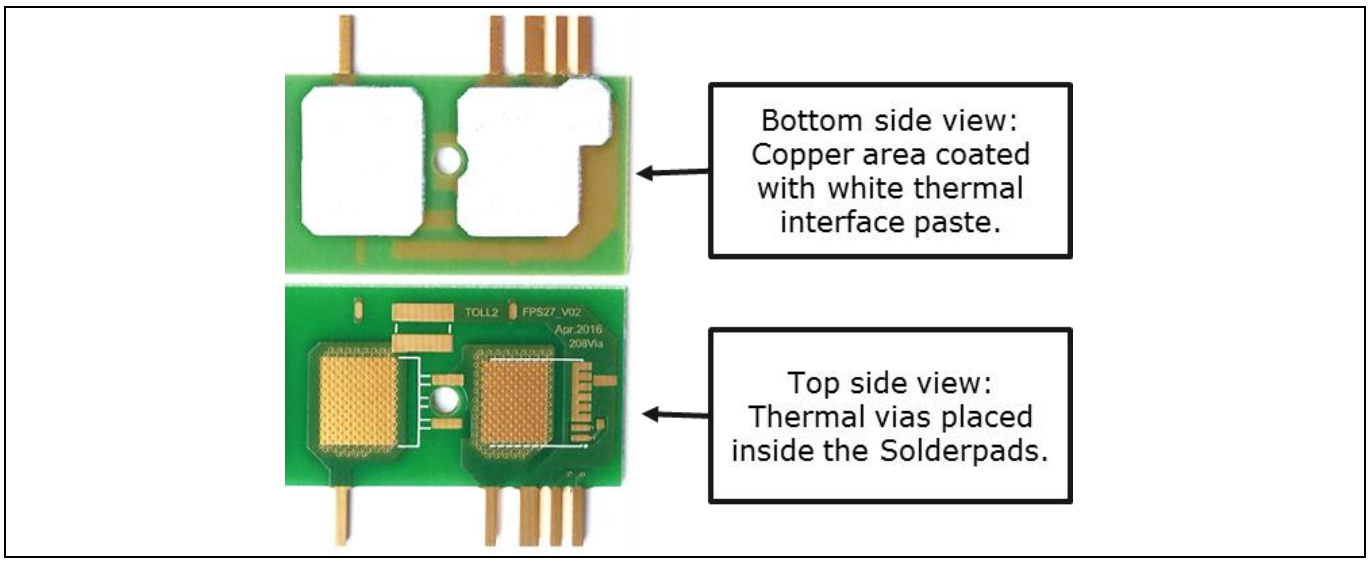


Figure 27 Daughter PCB with thermal interface paste

The conductive thermal interface paste is electrically insulating and reflow/wave soldering resistant.

It is normally applied to the PCB before soldering, as the last process in the manufacture of the bare PCB.

Its high conformability feature eliminates gaps between the heat sink and copper on the bottom side of the PCB, ensuring optimum heat transfer from the substrate to the heatsink.

As well as the thermal properties (thermal conductivity equal to 2.2 W/mK) typical thermal interface paste has good electrical insulation properties (60 kV/mm).

Both solutions shown in Figure 26 and Figure 27 do not have any solder resist on the bottom side in order to ensure the best thermal performance. For the version shown in Figure 27, this also guarantees the mechanical force concentrates to the copper plane area.

4.3 Silicon instead of heat sink

Previous chapters described how the power losses affect the cooling. Now, we can consider reducing the losses by the selection of a lower $R_{DS(on)}$ to decrease the thermal complexity.

$$P_V = I^2 * R_{DSon}$$

Figure 28 Conduction losses calculation for MOSFET

The correct $R_{DS(on)}$ selection allows the designer to reduce the conduction losses of the MOSFET according the equation shown in Figure 28. The higher the power of the application, the higher the current will be. This current increases the conduction losses by a square function. Therefore, it is very important to reduce the $R_{DS(on)}$ as much as possible within the limitations shown in Figure 9.

In the application comparison (which will be discussed in following sections), this technique has been used in the comparison of the 600 V 40 mΩ C7 devices with the 28 mΩ G7 ones.

Reducing the $R_{DS(on)}$ of the MOSFET means increasing its size of silicon. If the $R_{DS(on)}$ reduction leads to reduced overall losses, the size of the heat sink can also be reduced which leads to the so-called silicon instead of heatsink.

5 Application results

The 600 V CoolMOS™ G7 technology is optimized to offer best performance for both, hard-and soft-switching topologies and therefore, the application analysis is divided into hard-switching CCM PFC section and soft-switching (resonant) LLC part.

5.1 CCM PFC analyses

The CCM PFC application testing for the G7 devices shown in this document is performed by adding a daughter board to the 2.5 kW PFC evaluation board – including the Infineon CCM PFC controller (ICE3PCS01G) as shown in Figure 29.

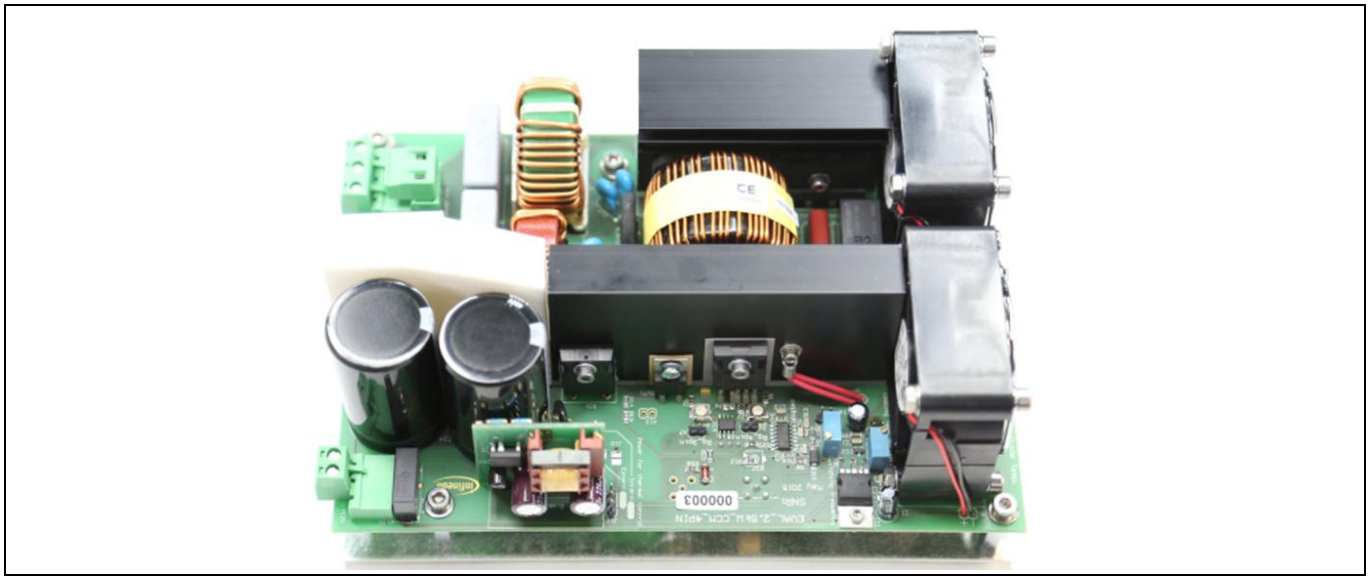


Figure 29 EVAL_2.5kW_CCM_4PIN evaluation board

The 2.5 kW evaluation board is an excellent example of a complete Infineon solution, and includes a PFC controller, MOSFET driver and Silicon Carbide (SiC) diode allowing evaluation of the 4-pin functionality and its advantages for efficiency and signal quality. The layout of the board is intended to allow easy access to the different devices and to add measurement probes to areas of interest. The evaluation board is fitted with double connectors for the power line input and 400 V output to allow sense techniques for precise efficiency measurements.

For more detailed information about the evaluation board please review www.infineon.com/C7-600V.

The original design of this evaluation board is fitted with TO-247 MOSFET. To use the TOLL G7 devices in this evaluation board, some modification with daughter boards is required. The special daughter board shown in Figure 30 is designed to fit into the pin arrangement of the main PFC evaluation board.

The daughter boards have been designed as shown in Figure 26 and Figure 27. This board contains the power MOSFET, the boost diode and the ceramic high frequency bulk capacitor to minimize the parasitic loop inductance of the circuit. The pin layout aligns with the main PCB of the evaluation board. Thus, it is possible to remove the total heat sink of this board and replace it with the module shown in Figure 32.

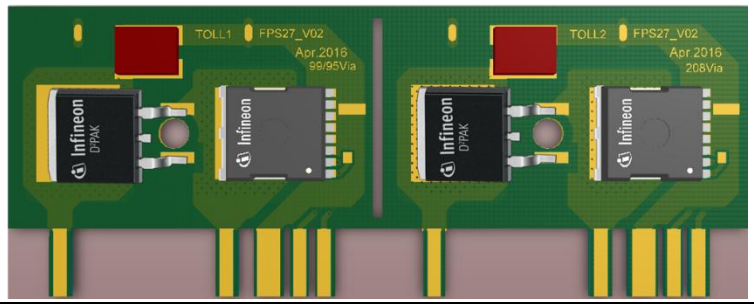


Figure 30 Top view of the TOLL daughter board for PFC circuit

The daughter board offers two different via layouts. The right one shown in Figure 30 does not have any vias in the soldering area of the SMD device - only around it. This version is suitable for any reflow soldering process, as there is no protection needed for preventing solder getting to the backside of the PCB. The left variant is made for best thermal performance and the whole area underneath the device contains thermal vias. It is understood that the variant with the high vias density is the better choice for high power applications while the one with no vias in the solder area might be a better choice for lower power ranges if solder protection is not easy to implement into the production process.

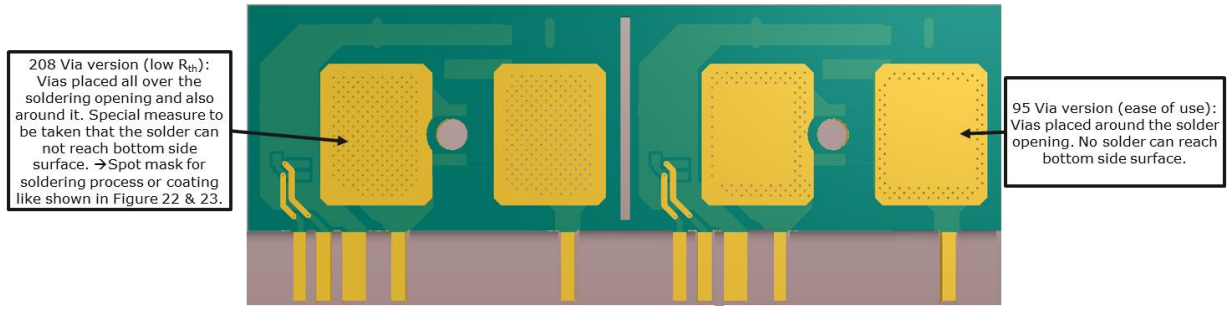


Figure 31 Bottom view of the TOLL daughter board

To not suck the solder through the vias during soldering process, special measures are required. The best solution will vary with the choice of assembly process as is described in section 4.2.2.

The daughter boards with vias in the solder area use a coating (solder mask) added to the bottom side during the device soldering process. The coating acts as a protection layer to prevent the solder getting sucked to the bottom side of the PFC because this would disrupt the flatness of the cooling interface area. It is necessary to remove this solder spot mask after the soldering as it would worsen the thermal conductivity similar to a thermal interface layer. This daughter board is assembled with the same kind of thermal interface material as used for the THD version to have some fair comparison for the efficiency and temperature comparison between SMD and THD solutions. This is the simple reason why the daughter board is not using the very modern technic described in the section above.

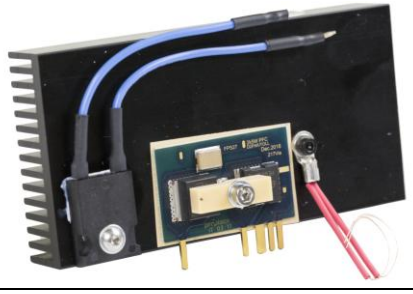


Figure 32 CoolMOS™ G7 TOLL upgrade for EVAL_2.5KW_CCM_4PIN demo board

The mechanical fixing of the daughter board is possible with conventional springs or by screwing through the drilled hole in the middle of the PCB as it is done for the G7 TOLL upgrade module in Figure 32.



Figure 33 EVAL_2.5kW_CCM_4PIN evaluation board after modification for TOLL packages

5.1.1 Clean waveforms by low parasitic

For high power applications, parasitic inductances are a well-known issue for the designer. They not only cause oscillations but also voltage spikes. One way to limit this is to increase the gate resistance to slow down the switching speed but this has the drawback of reducing efficiency. The other way is to minimize the parasitic inductances of the leads by moving away from THD towards SMD, such as TOLL, which offers extremely low lead inductances.

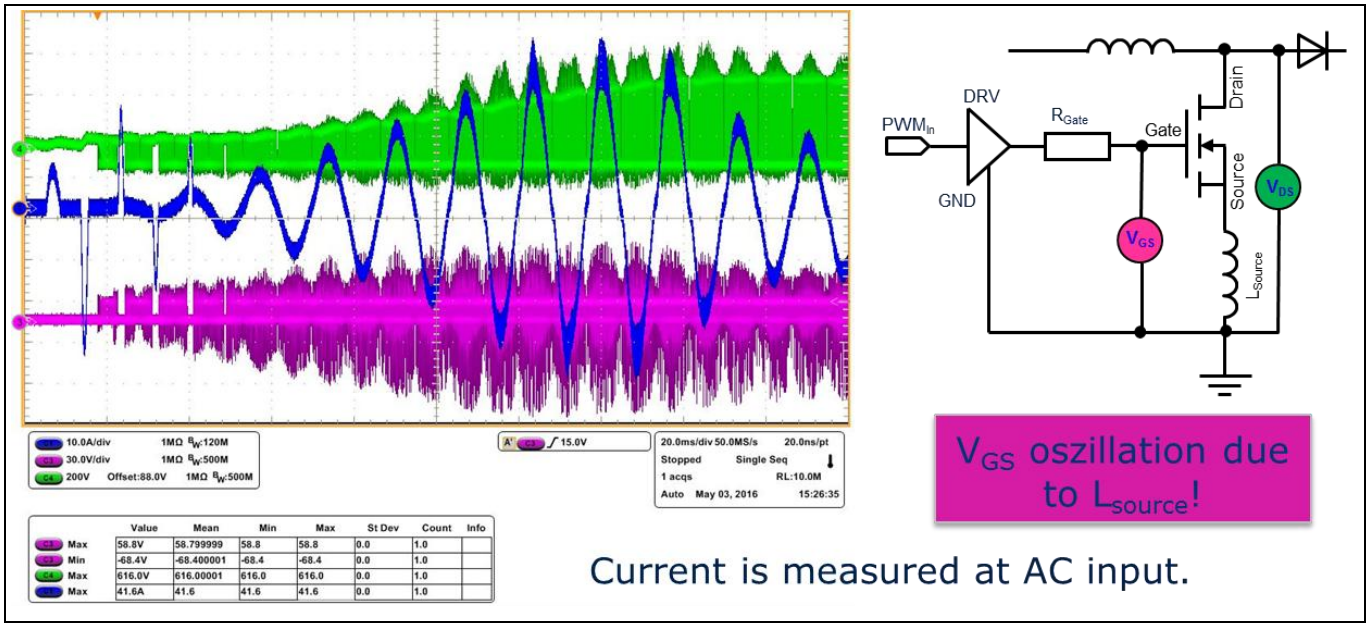


Figure 34 Startup at 90 V_{AC} with 1 kW load for IPW65R045C7 (TO247)

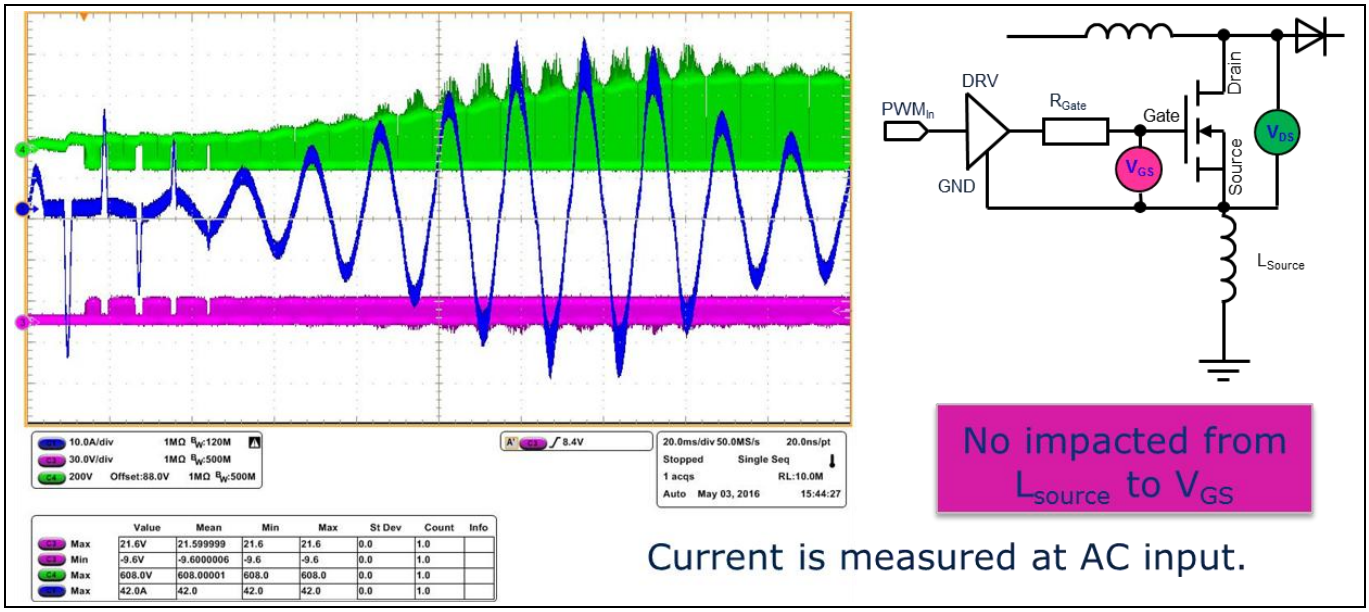


Figure 35 Startup at 90 V_{AC} with 1 kW load for IPT65R033C7 (TOLL)

In Figure 28 and Figure 29, the startup of the PFC-evaluation board is documented to allow a TO-247 4-pin and TOLL comparison. The blue line (channel 1) shows the AC input current, the magenta line (channel 3) shows the gate to power source voltage and the green line (channel 4) shows the drain to source voltage. The comparison between Figure 34 and Figure 35 shows the signal quality advantage for TOLL very clearly. Not only do the voltage spikes on the gate remain below 22 V, the drain-source voltage is also much more stable than for the TO-247, which is one important requirement for fast and efficient switching.

5.1.2 Efficiency impact to CCM PFC

One of the most important aspects of the application testing is the monitoring of the device efficiency impact. For the G7 technology offered in the TOLL package, there have been several positive impacts discussed which all contribute to the overall efficiency of the whole PFC circuit.

The comparison shown in Figure 30 is based on a switching frequency of 65 kHz and a heat sink temperature of 60°C. The gate resistor used for both devices is set to 3 Ω. For the TOLL the daughter PCB with the vias underneath the whole package area was used as the power range is up to 3 kW. This PCB is fitted with 208 vias for each of the SMD (MOSFET and diode) to minimize the additional thermal resistance of the PCB.

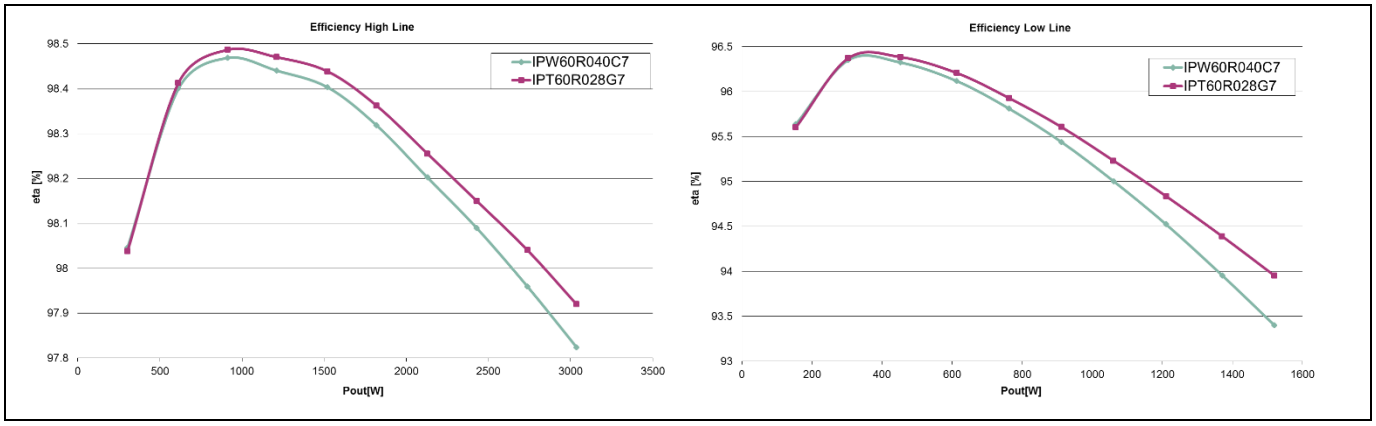


Figure 36 Efficiency for high line (230 V_{AC}) and low line (90 V_{AC}) input voltage

The comparison shows the operation up to 3 kW in high line mode and 1.5 kW in low line operation. In both cases, the efficiency with the IPT60R028G7 is higher in the high load region due to better switching performance and lower $R_{DS(on)}$. This effect is more pronounced in the low line testing as the contribution from the MOSFET is stronger than in the high line example. Looking to the high line measurement at light load, one can see that due to the very low switching losses increase by using 28 mΩ device instead of 40 mΩ, the light load efficiency is still very similar which is very unique for the G7 technology as any other technology would show in this case much more disadvantage in the light load efficiency. This proves the simulation results shown in Figure 9.

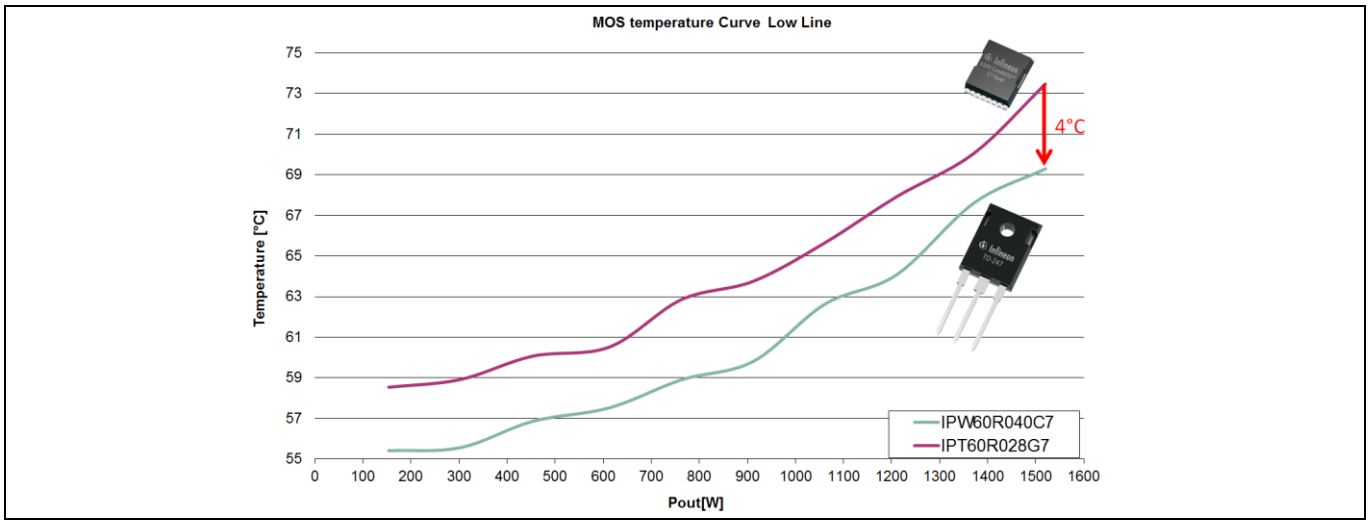


Figure 37 Temperature monitoring for 90 V_{AC} input voltage

As a result of the significantly increased efficiency for the thermally very critical low line at high load area, the temperature of the TOLL MOSFET stay very cool as shown in Figure 37. At 1500 W, the IPT60R028G7 remains to the temperature measurement difference to the equivalent TO-247 C7 device - although the cooling path for the TOLL in addition includes the R_{th} of the PCB as discussed in Table 3 compared to the conventional method with TO-247 assembling.

5.2 LLC application analyses

The LLC application testing for the G7 devices shown in this document is performed by adding a daughter board to the 600 W LLC evaluation board offered by Infineon. This board is designed to prove the high performance of the 600 V CoolMOS™ C7 series in resonant topologies. It shows how to design a half-bridge LLC stage of a server SMPS with the target to meet 80Plus® Titanium standard efficiency requirements. On this purpose, it has been fitted with IPP60R180C7 600 V power MOSFET on the primary side and OptiMOS™ low voltage power MOSFET in SuperSO8 BSC010N04LS in the synchronous rectification secondary stage, in combination with QR CoolSET™ ICE2QR2280Z, hi-low side driver 2EDL05N06PF, low-side gate driver 2EDN7524F and a LLC controller ICE2HS01G for the analog or XMC4200 in the digital version.

For more detailed information about the evaluation board please review www.infineon.com/C7-600V.

For the LLC application, analyses the 600 W LLC demo board with the analog control version has been used by adding some special daughter PCB to analyze the surface mound devices offered by the 600 V CoolMOS™ G7 technology.



Figure 38 600 W LLC demo board

The SMD daughter board has been designed to fit exactly to the THD holes on the main board. One can see within Figure 39 the additional added pins to the PCB to be able to stick the module onto the main board. The daughter board itself is coupled to the heatsink by the same thermal interface (K10 foil) as it is done in the original setup with TO-220 devices. With this setup it is possible to get fast and relevant comparison results.

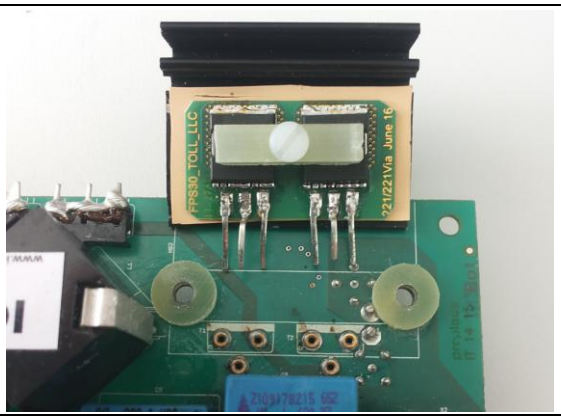


Figure 39 SMD daughter board assembly for the LLC evaluation board

5.2.1 Efficiency impact to LLC topologies

The 600 V CoolMOS™ G7 offers best performance not only for hard switching topologies but also for resonant topologies like the LLC. Figure 40 illustrates the efficiency benefit the designer can archive using the G7 device in LLC by simply plug and play if compared with the P6 devices, which have been the leading technology for LLC up to now.

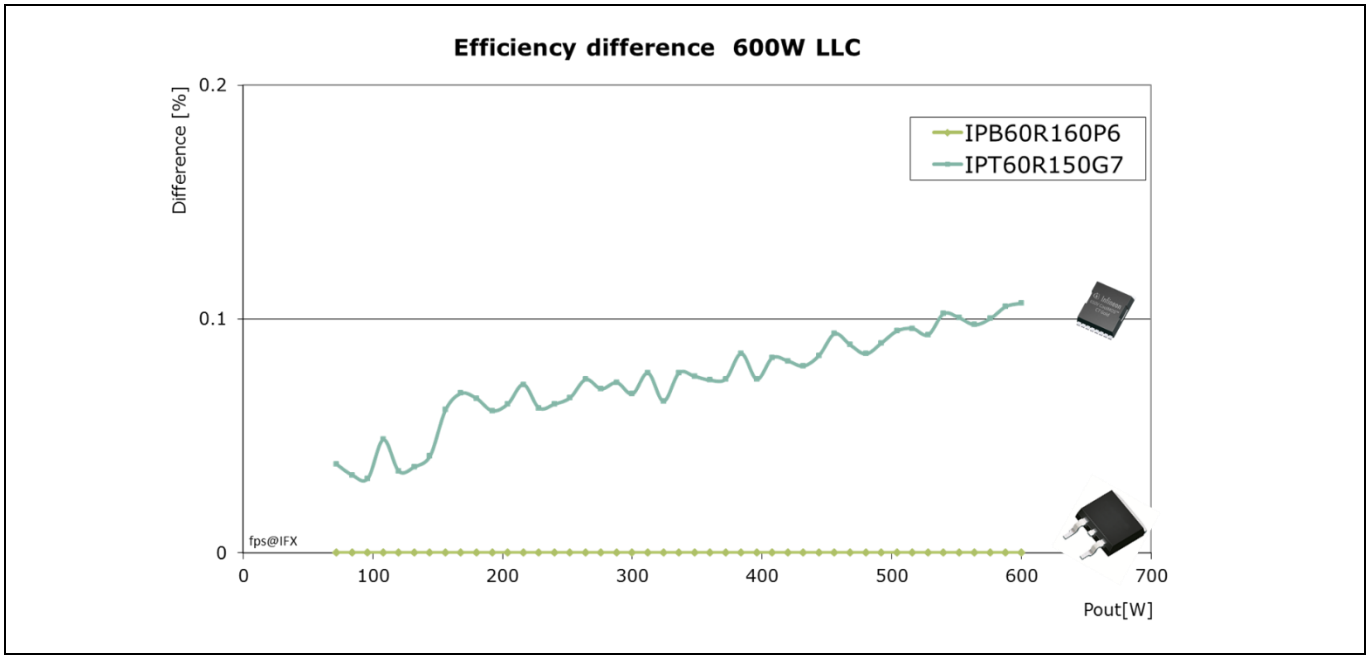


Figure 40 LLC efficiency comparison of P6 and G7 based on differential chart

The comparison shown in Figure 40 is limited to 600 W by the demo board as this has been designed for 180 mΩ devices. One can understand that the benefit of the IPT60R150G7 will grow with the power range further and the maximum output power for such $R_{DS(on)}$ would be in the range up to 800 W.

5.3 Application conclusion

The application testing highlights the advantage of the G7 TOLL SMD compared to the conventional TO-247 package. G7 technology with improved switching performance enables use of a lower $R_{DS(on)}$ for a given power range. This offers a totally new optimization point for the applications that improves the high load range while not impacting the light load efficiency. Having better full load efficiency is an excellent starting point for reducing the cooling effort, thus supporting the drive towards increasing power density.

It has been shown that the G7 technology enables first time to use SMD devices for single stage standard PFC up to 3 kW for high line operation which has been the clear domain for TO-247 in the past.

Besides this the highest performance in resonant topologies has been proven by the efficiency gain shown in the LLC evaluation board.

As a result of the best performance within hard and soft switching topologies the 600 V CoolMOS™ G7 is the right device to design switched mode power supplies with fully SMD semiconductor switches.Click or tap here to enter text.

6 Related resources

- 600 V CoolMOS™ G7
- Developer Community

Revision history

Document revision	Date	Description of changes
V 1.0	2017-03-28	Initial release
V 1.1	2026-02-18	Lifecycle review: Updated to the latest template and branding update

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