# 500 V CoolMOS™ CE

## 500 V Superjunction MOSFET for consumer and lighting applications

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### About this document

### Scope and purpose

The new CoolMOS™ CE is the fourth technology platform of Infineon's market leading high voltage power MOSFETs designed according to the revolutionary superjunction (SJ) principle in the 500 V class. 500 V CE portfolio provides all benefits of a fast switching superjunction (SJ) MOSFET while keeping ease of use and implementation. The complete CE series of MOSFETs achieve very low conduction and switching losses, and can make applications more efficient, more compact, lighter and thermally cooler.

This application note will describe the fundamental differences between a SJ MOSFET and a standard MOSFET. Additionally, all features and benefits impacting the target applications will be described. Furthermore, these features will be illustrated from both a theoretical point of view and in hardware measurements. It will also be shown that CoolMOS™ CE is a cost effective alternative compared to standard MOSFETs, which enables reaching higher efficiency levels while offering an attractive price/performance ratio.

### Intended audience

This application note is written to give an application engineer a fundamental understand of the superjunction principle. Furthermore, it should represent the benefits of using a faster switching device in real applications and describe general design rules implementing this new technology

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# 1 Features and benefits

The following table represents the features and benefits of CoolMOS™ CE in comparison to standard MOSFETs, which will be discussed in depth in the main part of this application note.

**Table 1 Features and benefits**

| FEATURES | BENEFITS |
|---|---|
| Reduced energy stored in output capacitance ($E_{oss}$) | Reduction of switching losses, improvement of light load efficiency |
| High body diode ruggedness | Higher reliability under critical operating conditions |
| Reduced reverse recovery charge ($Q_{rr}$) | Lower possibility of hard commutation in resonant topologies |
| Reduced gate charge ($Q_g$) | Improvement in light load efficiency |
| | Lower gate drive capability required |
| Overall features | Easy control of switching behavior |
| | Outstanding reliability with proven CoolMOS™ quality |

## 1.1 Applications (target market)

The following table represents the target applications and topologies for these new MOSFETs.

**Table 2 Target applications and topologies**

| Application | PFC | PWM |
|---|---|---|
| PC Silverbox | Boost-stage | TTF |
| | | LLC |
| LCD/LED/PDP TV | Boost-stage | LLC |
| Gaming | Boost-stage | TTF |
| | | LLC |
| Lighting | Boost-stage | LLC |

All the features and benefits of the 500 V CE in connection with the target applications and topologies will be analyzed in section 4. The following section will describe the differences between SJ MOSFETs and standard MOSFETs.

# 2 Superjunction (SJ) principle

In the past the consumer market has been dominated by standard MOSFETs. Therefore this chapter is included to show the difference to SJ MOSFETs.

## 2.1 General description

“All CoolMOS™ series are based on the Superjunction principle, which is a revolutionary technology for high voltage power MOSFETs [1, 2], Infineon Technologies has been the first company worldwide to commercialize this idea into the market [4]. Where conventional power MOSFETs just command on one degree of freedom to master both on-state resistance and blocking voltage, the Superjunction principle allows two degrees of freedom for this task. Therefore conventional MOSFETs are stuck with the limit of silicon, a barrier which marks the optimum doping profile for a given voltage class. This limit line has been theoretically derived by Chen and Hu in the late 1980 [3]. No commercial product has an on-state resistance better than the limit line of silicon.” [5] Figure 1 represents the area-specific on-resistance versus breakdown voltage.

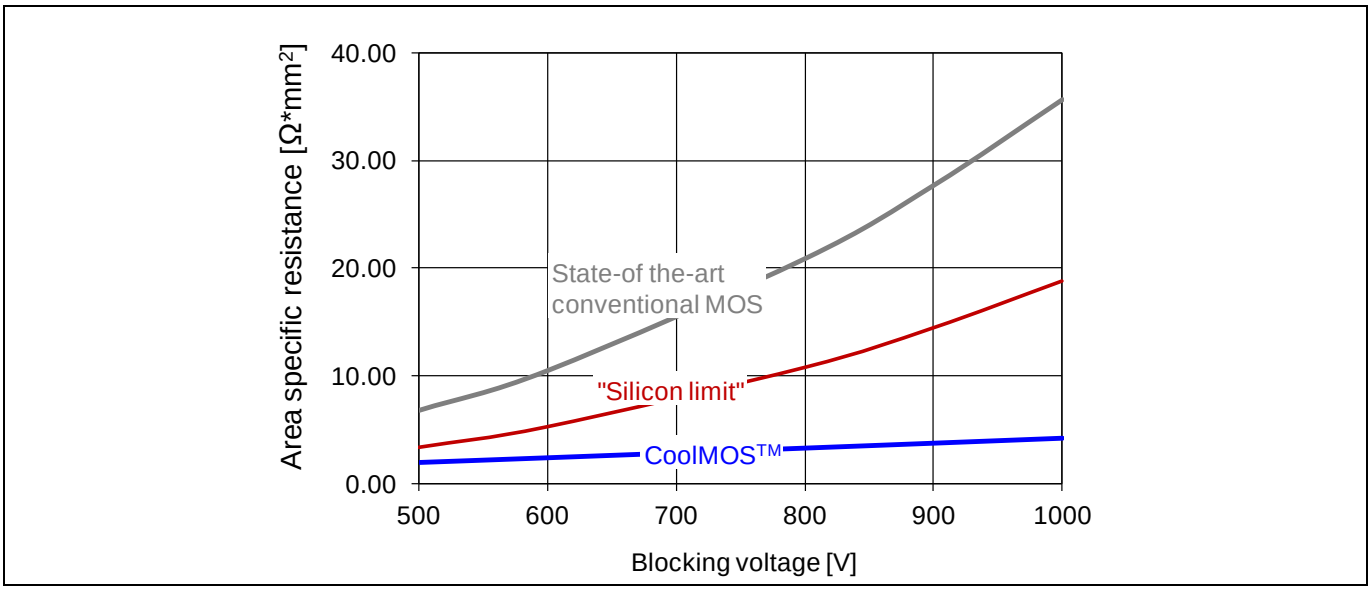



**Figure 1 Area-specific on-resistance versus breakdown voltage comparison of standard MOSFET and CoolMOS™ technology [6]**

“In contrast to that the Superjunction principle allows to reduce the on-state resistance of a high voltage MOSFET virtually to zero, limited only by technology efforts and manufacturing capabilities.” [5]

“The basic idea is simple: instead of having electrons flowing through a relatively high resistive (high voltage blocking) n-area, we allow them to flow in a very rich doped n-area, which gives naturally a very low on-state resistance. The crucial point for the SJ technology is to make the device block its full voltage, which requires a careful balancing of the additional n-charge by adjacently positioned deep p-columns, which go all the way straight through the device close to the back side n+ contact. This is where manufacturing capability comes in, as the charges within the device need to be compensated precisely under the constraints of a mass market production line.” [5] Figure 2 shows the cross section of a standard MOSFET (left) and a SJ MOSFET (right).

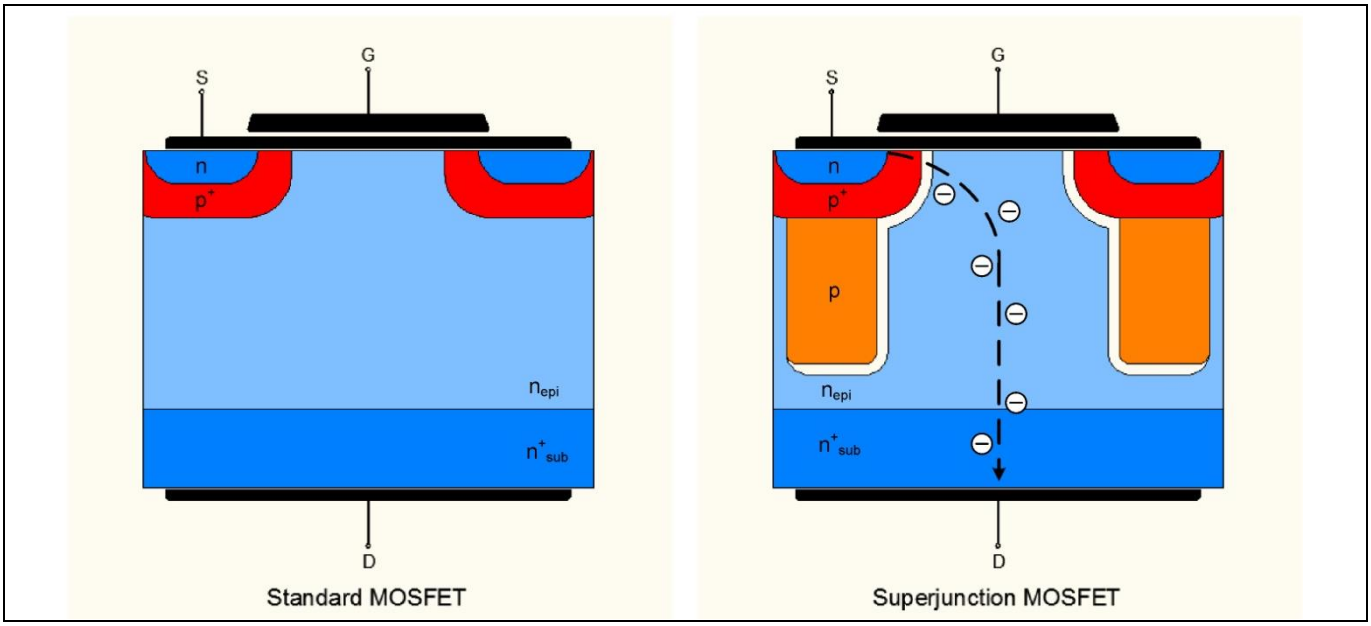



Figure 2 Cross section of standard MOSFET (left) and SJ MOSFET (right) [5]

"The SJ principle gives us the opportunity to create best-in-class types, which have not been possible before such as a 100 mΩ/600 V part in a TO-220 package. Furthermore it allows making parts with very low capacitances for a given $R_{DS(on)}$ as the silicon chip is much smaller than for a conventional power MOSFET. Both input and high voltage level of the output capacitance scale directly with the chip size, whereas reverse capacitance and to some extent the low voltage level of the output capacitance is technology dependent. Characteristic of all Superjunction devices is a strong non-linearity of the output capacitance with high values at low voltage and low values at high voltage. This behavior can be easily understood if you take into account that the output capacitance is proportional to the area of the blocking pn-junction and inverse proportional to the width of the space charge layer (or the voltage sustaining area). At low voltage the p-columns are not depleted and form a very big surface, furthermore the width of the space charge layer is very narrow (the white area seen in" Figure 2). " At high voltage however the p-columns are fully depleted and the space charge layer has reached its full extension of roughly 45 µm for a 600 V device. Important is that the non-linearity of the output capacitance allows a quasi zero-voltage-switching (ZVS) turn-off of the device, lowering turn-off losses. Superjunction devices are by nature fast in switching. Very small capacitances together with a low gate charge make rise and fall times of a few nanoseconds a reality." [5] For more information on Superjunction devices please read the article "Mastering the Art of Slowness" which is available on www.infineon.com.

## 2.2 Superjunction benefit of 500 V CE

Chapter 2.1 illustrated the general characteristics of a SJ MOSFET in comparison to a standard MOSFET. Now the question arises "What is the benefit for the 500 V CE?" This application note will describe two of the most important factors starting with the switching speed.

### 2.2.1 Switching speed

As mentioned in the general description the switching speed increases dramatically. This behavior comes from the low parasitic capacitances of a SJ MOSFET in comparison to the standard MOSFET. A SJ MOSFET has about half of the value of input and output capacitance, which brings the benefits for switching losses and driving losses. Figure 3 represents these parasitic capacitances (marked in red) in a simplified schematic.

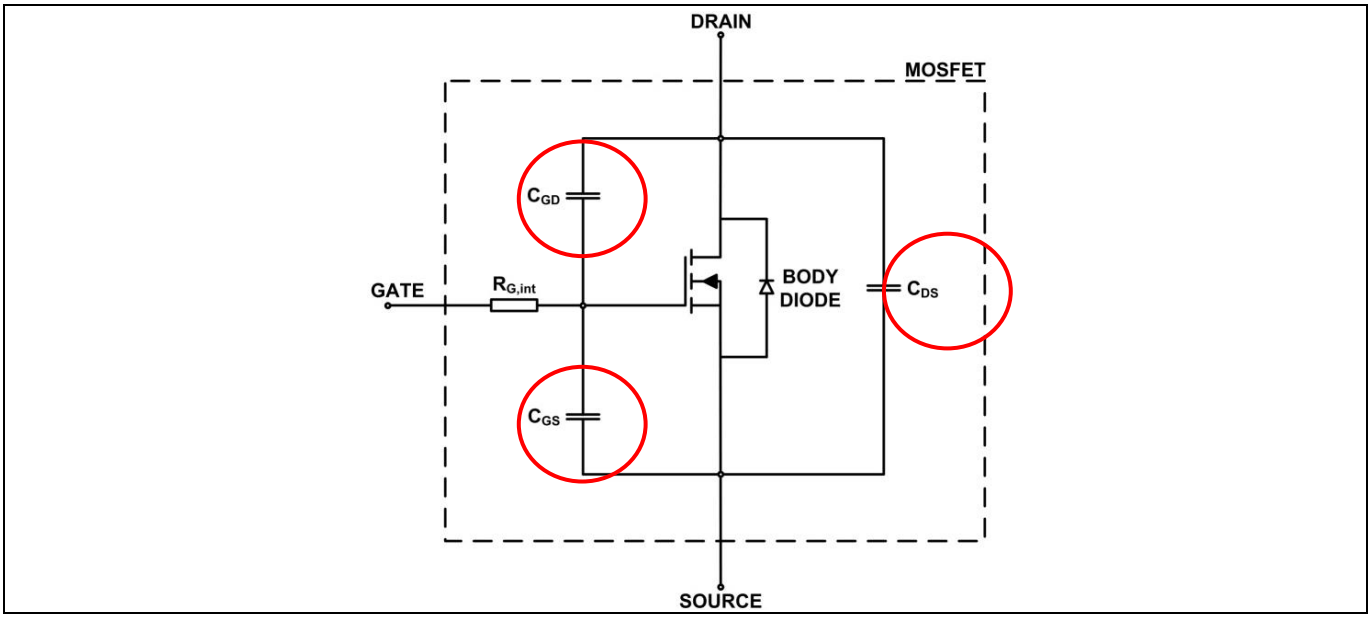



**Figure 3 Simplified small signal MOSFET equivalent circuit**

Because of this capacitance reduction the $E_{on}$ and $E_{off}$ of the 500 V CE is about half in comparison to a standard MOSFET. Furthermore this reduction of capacitances results also in a reduced gate charge Qg which gives the benefit of reduced driving losses, and the possibility to use a lower cost driver with less gate drive capability. Figure 4 represents the capacitance comparison of the 500 V CE (280 mΩ) vs. a comparable standard MOSFET.

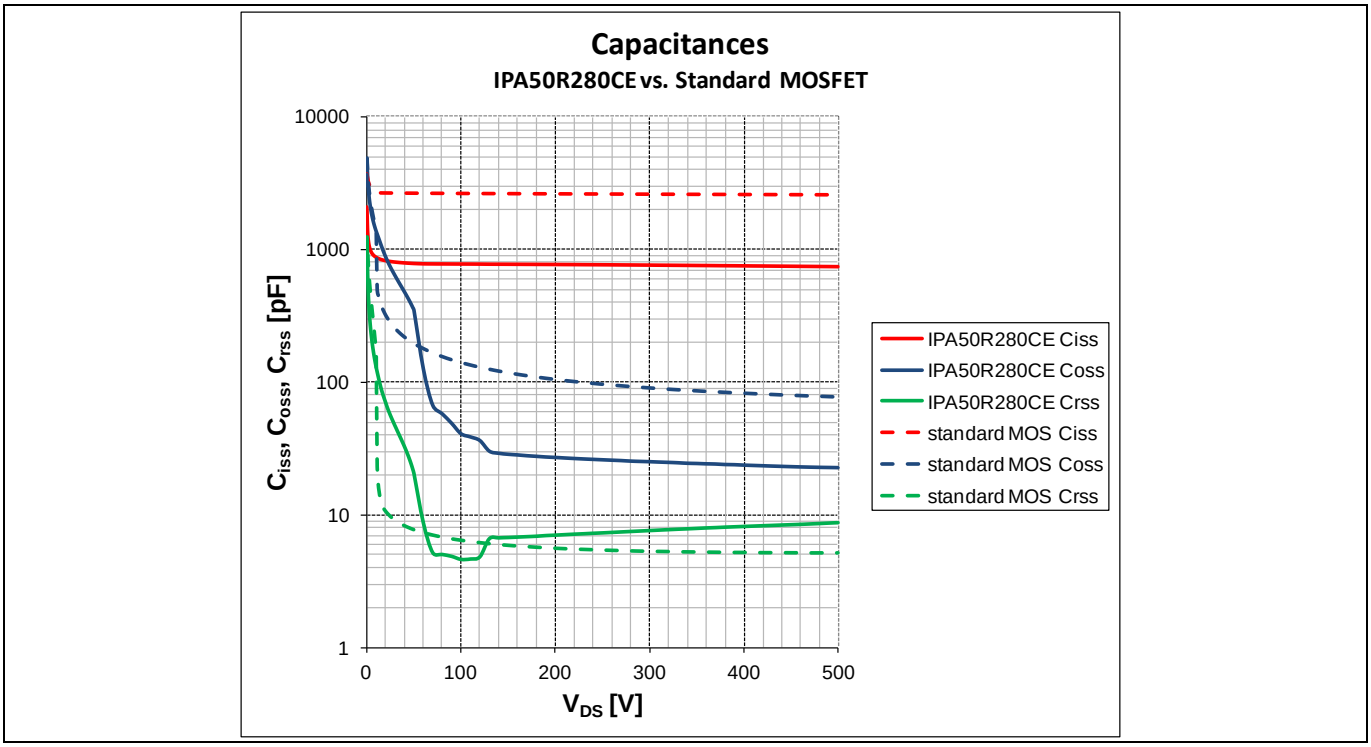



**Figure 4 Capacitance comparison 500 V CE vs. standard MOSFET**

"A fundamental characteristic of all Superjunction devices is, that both the output and reverse capacitance show a strong non-linearity. The non-linearity in Superjunction capacitance characteristics comes from the fact that at a given voltage – typically in the range of 1/10th of the rated blocking voltage – p- and n-columns

deplete each other leading to a fast expansion of the space charge layer throughout the structure. This means that at a voltage beyond 50 V for 500 V rated devices both output and reverse capacitance reach minimum values of a few pF only, resulting in a dv/dt of more than 100 V/ns and di/dt of several thousand A/µs if the load current is allowed to fully commute into the output capacitance during turn-off. The output capacitance is charged up to the level of the bus voltage where the voltage rise follows then the formula:

$$dv/dt = \frac{I_{load}}{C_{oss}} \quad (1)$$

The voltage rise is therefore proportional to the load current $I_{load}$ and inverse proportional to the value of the output capacitance $C_{oss}$. Because of the decreasing $C_{oss}$ towards higher voltages, the highest dv/dt is reached shortly before reaching the bus voltage. The according di/dt is mainly limited by the inductances of package and PCB circuit. The highest efficiency can now be reached by turning-off the device in this manner, because the occurring switching losses can be ideally reduced down to the level of the stored energy in the output capacitance." [7]

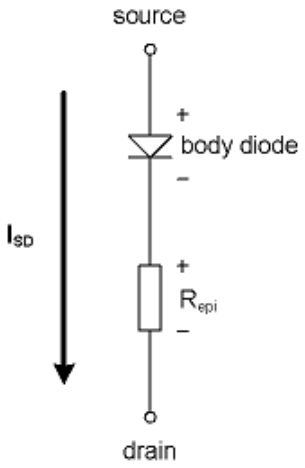
All these benefits will be clearly visible in the efficiency results, which will be described in chapter 4. The second difference is the so called BJT-Effect.

### 2.2.2 BJT (Bipolar Junction Transistor)-effect

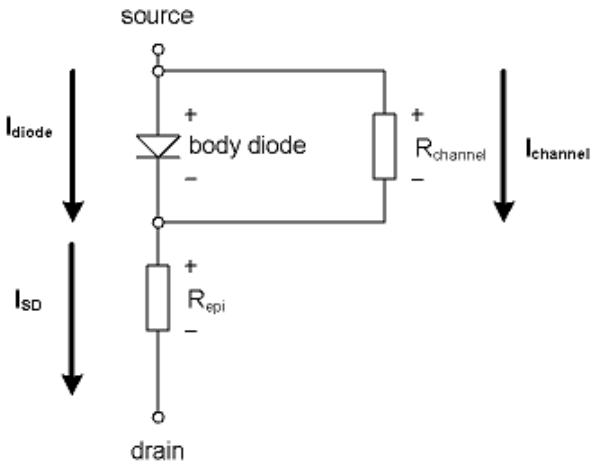
If the body diode conducts in forward direction, minority carriers remaining in the base region during diode recovery can cause a BJT action with destructive results (short circuit of drain source while high voltages are applied).

How is it possible to trigger the BJT-Effect? This is shown step by step in the following:

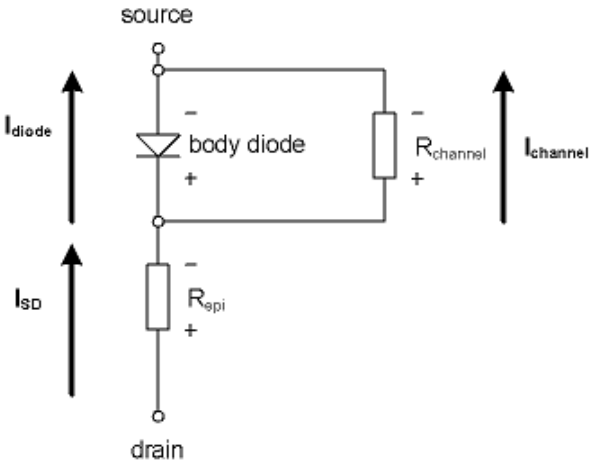
In a zero voltage switching topology the forward current ($I_{SD}$) is forced into the body diode to clamp the output at either the positive or negative rail following a current driven drain to source transition. This forward current causes the generation of minority carriers in both the p doped body (electrons) and $n_{epi}$ regions (holes).



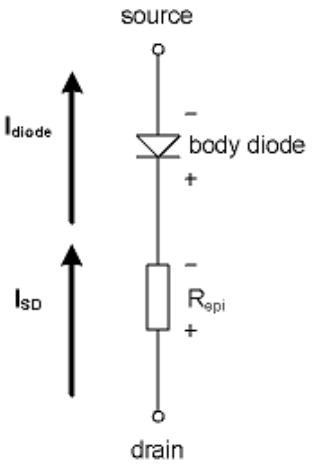
The MOSFET channel is turned ON and diverts a portion of the current through the channel away from the body diode, that is still forward conducting (MOSFET can conduct current in both directions). This lower current flowing through the body diode will reduce the generation of minority carriers but will not stop it.




The external circuitry reverses the current flow through the device -> small amount of reverse current flows in body diode (small due to the very weak voltage generated by very low current flowing in the low resistive channel, especially at light load operation). Some minority carriers will be removed from the p-n-junction, but not all due to a conduction period that is short in relation to the intrinsic carrier lifetime.




If the MOSFET completely turns ON the current will be completely diverted to the channel, but if the MOSFET turns OFF when there are still minority carriers in the body diode the following happens: The MOSFET will begin to block voltage imposing a higher reverse voltage on the body diode, with high dv/dt. The application of high reverse voltage on the body diode will sweep the remaining carriers across the junction very quickly. Minority carriers in the $n_{epi}$ region are swept towards the p+ body. -> if this current (flowing into $R_B$, represented in Fig. 5) reaches a magnitude sufficient to activate the intrinsic bipolar transistor, second breakdown will occur destroying the MOSFET.




In a conventional MOSFET the hole current, fed by reverse recovery charge, flow laterally into the p doped region crossing the area below the n region before they reach the top side of the device below the gate electrode: so this current flows through $R_B$ of the parasitic bipolar structure, with the risk of forward biasing of npn-junction and consequent triggering of parasitic BJT.

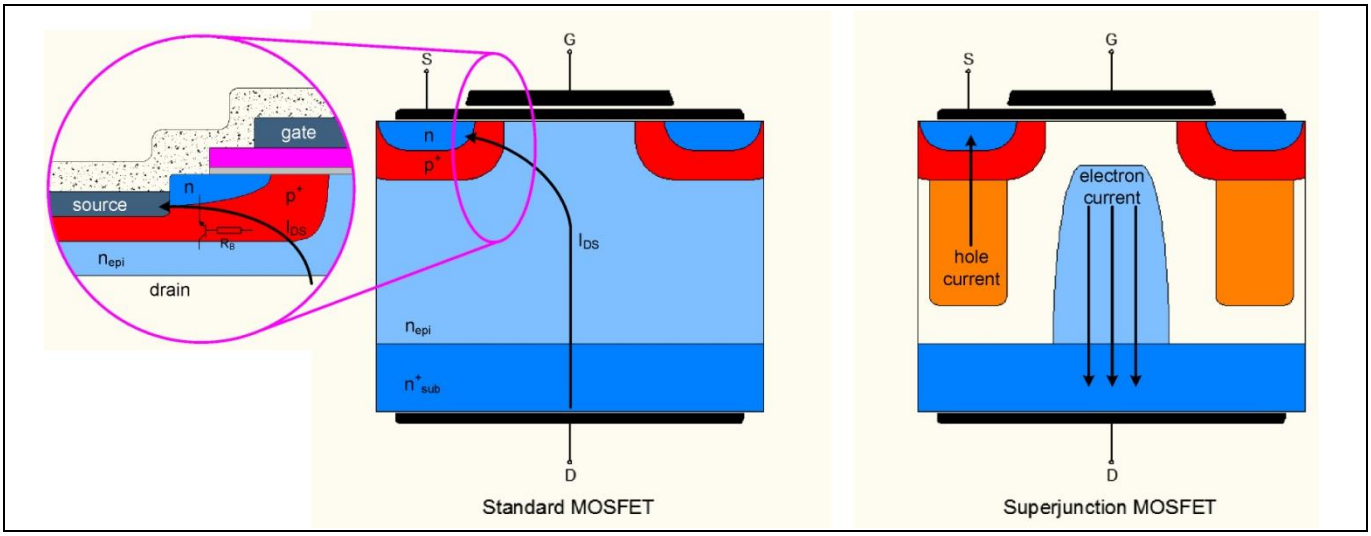



**Figure 5 BJT-effect**

As visible in Figure 5 (right) in a CoolMOS™ the hole current flows upwards through the p doped column, before it reaches the metalized contact, but no lateral current will pass through the p doped well and therefore no current flows through RB reducing the possibility of triggering the BJT-Effect to nearly zero.

Now that the basics of the SJ MOSFET have been discussed, this paper is going to continue with technology parameters and their influence on the applications in the specific topologies.

# 3 Technology parameters

## 3.1 Gate charge ($Q_g$)

One of the most important improvements is the Qg reduction which brings benefits especially in light load conditions due to reduced driving losses. In general the 500 V CE has about 40% $Q_g$ reduction in comparison to an comparable standard MOSFET over the whole $R_{DS(on)}$ range. Figure 6 shows the $Q_g$ in nC of the 500 V CE against a standard MOSFET over the $R_{DS(on)}$,max range from 190 mΩ to 950 mΩ.

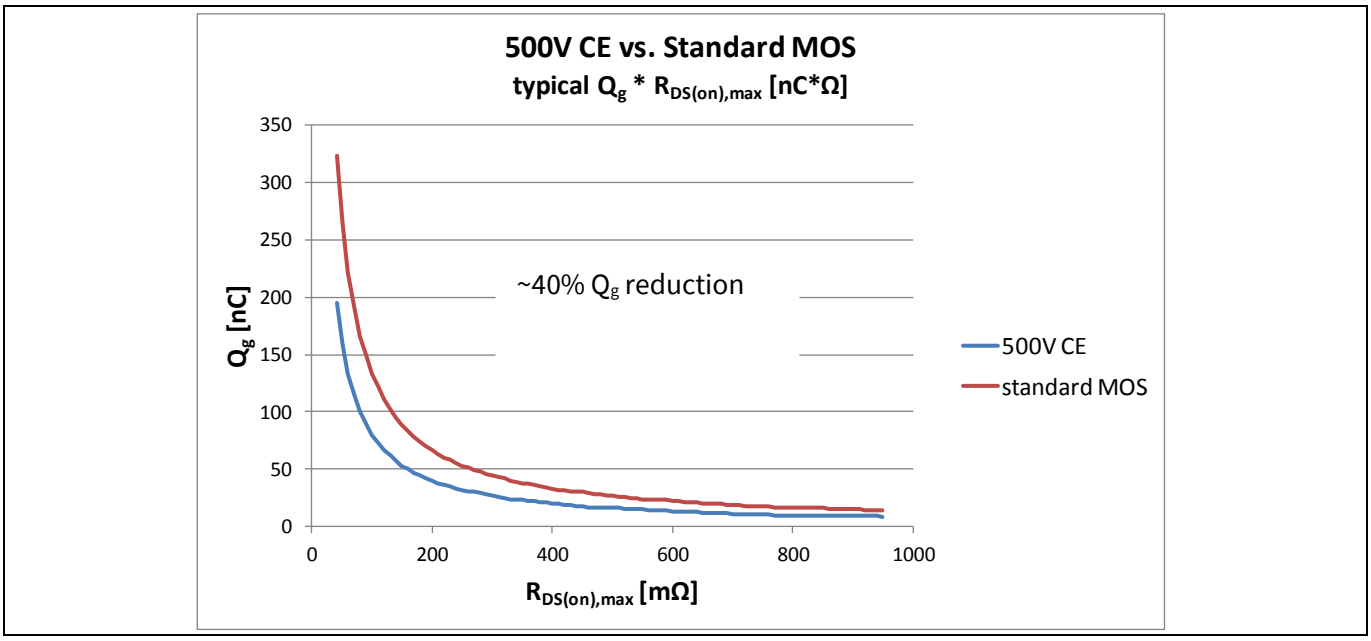



Figure 6 $Q_g$ comparison 500 V CE vs. standard MOSFET

## 3.2 Energy stored in output capacitance ($E_{oss}$)

The reduced energy stored in the output capacitance brings the most important difference in hard switching topologies but nevertheless it affects also the switching losses in a resonant topology. Normally it is possible to choose between zero voltage switching (ZVS) or zero current switching (ZCS). In these two cases it is possible to eliminate the turn-on losses (ZVS) or the turn-off losses (ZCS), but it is not possible to work in these two operation modes at the same time. Normally for MOSFETs the ZVS operation is preferred due to the usually important contribution of the output capacitance to the turn-on losses (if hard switching). Therefore, one part of the switching losses is still always in action and the reduction of $E_{oss}$ brings a reduction of those switching losses. Fig.7 represents the $E_{oss}$ comparison between the 500 V CE and a comparable standard MOSFET of the 500 mΩ devices.

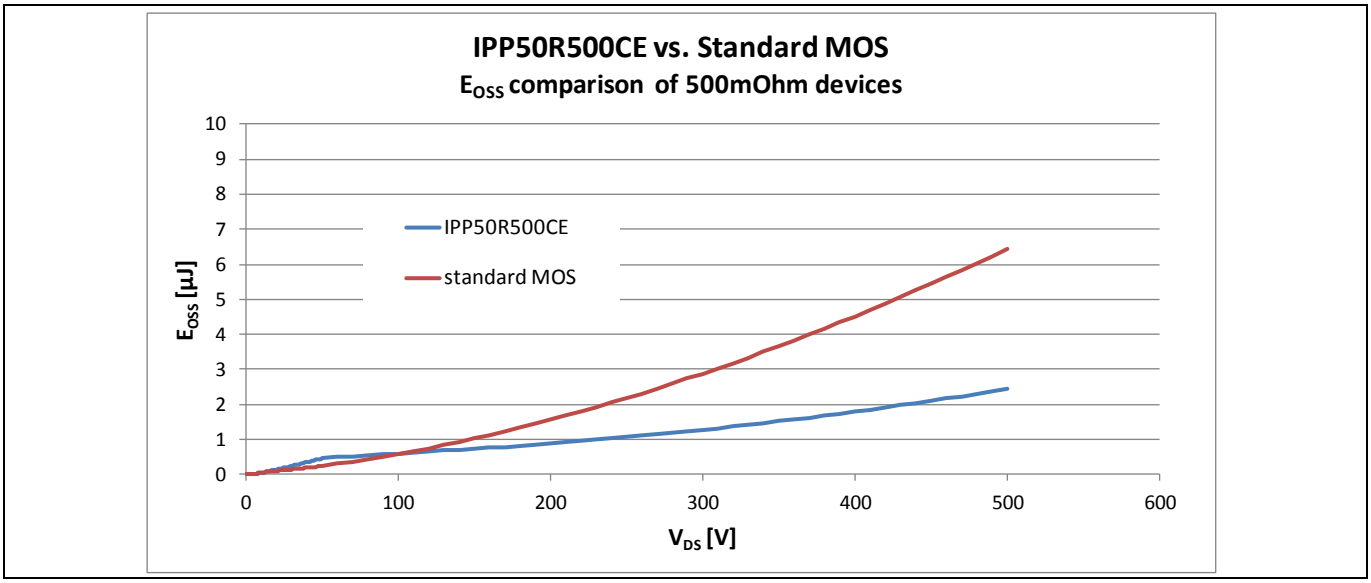



**Figure 7** **$E_{oss}$ comparison 500 V CE vs. standard MOSFET**

The $E_{oss}$ loss is in direct proportion to the output capacitance as a function of drain to source voltage of the MOSFET. In this case the effect of a reduction of $C_{oss}$ is clearly visible. One further benefit out of this is a faster $V_{DS}$ transition time in resonant topologies, which means that it is possible to reduce the resonant inductance and circulating current loss, because it is possible to completely discharge the $C_{oss}$ with lower currents.

# 4 Measurement results

In order to show the impact of the mentioned technology parameters this section will describe some measurements starting with the efficiency comparison in a CCM PFC, which is one of the most suitable topologies to verify the new MOSFETs in hard switching.

## 4.1 Efficiency in CCM PFC

In this measurement the 500 V CE is compared to a comparable standard MOSFET in the 280 mΩ $R_{DS(on)}$ range.

Setup parameters:

- CCM PFC
- $V_{in}$=90 VAC
- $V_{out}$=400 $V^{DC}$
- $P_{out}$=0 W to 400 W
- Frequency=100 kHz
- $R_{G,ext}$=5 Ω
- Ambient temperature 25°C
- Heat sink temperature preheated to 60°C
- Plug and play scenario between 500 V CE and standard MOSFET

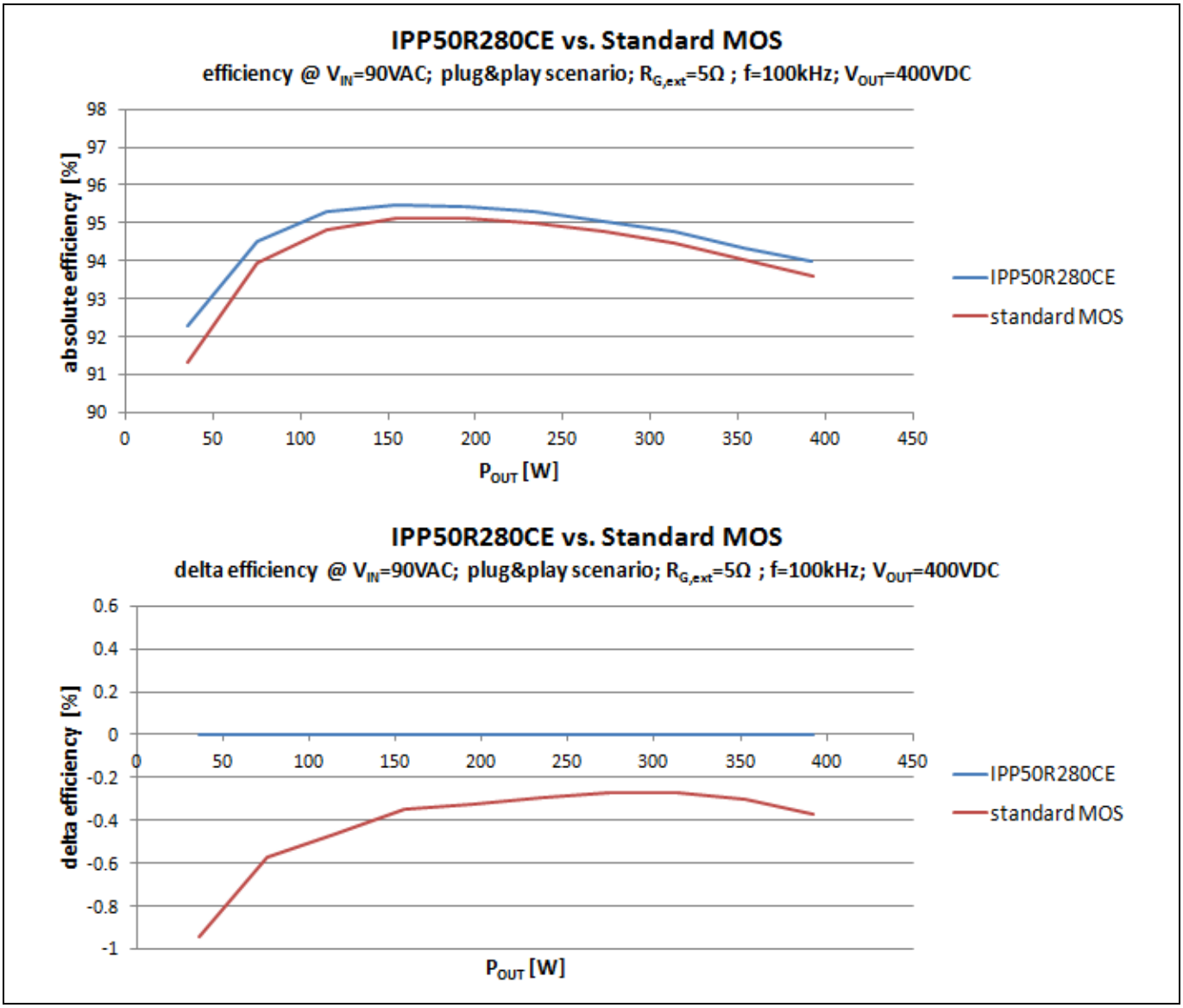



**Figure 8** **500 V CE vs. standard MOSFET comparison in absolute efficiency (upper) and delta efficiency (lower)**

This plug and play measurement shows the benefit of a SJ MOSFET in comparison to a standard MOSFET. In light load condition (~40 W). Due to the $Q_g$ reduction an efficiency difference in light load operation (~40 W) of more than 0.9% is visible. The efficiency of the IPP50R280CE is on average 0.4% higher than the comparable standard MOSFET over the whole load range. Here also the effects of the lower $E_{on}$ and $E_{off}$ are visible.

Fig. 9 represents the $E_{on}$ and $E_{off}$ values of an IPA50R500CE in comparison to a comparable standard MOSFET over $R_{G,ext}$ at different drain currents ($I_D$) and test ambient temperature ($T_C$) of 25°C.

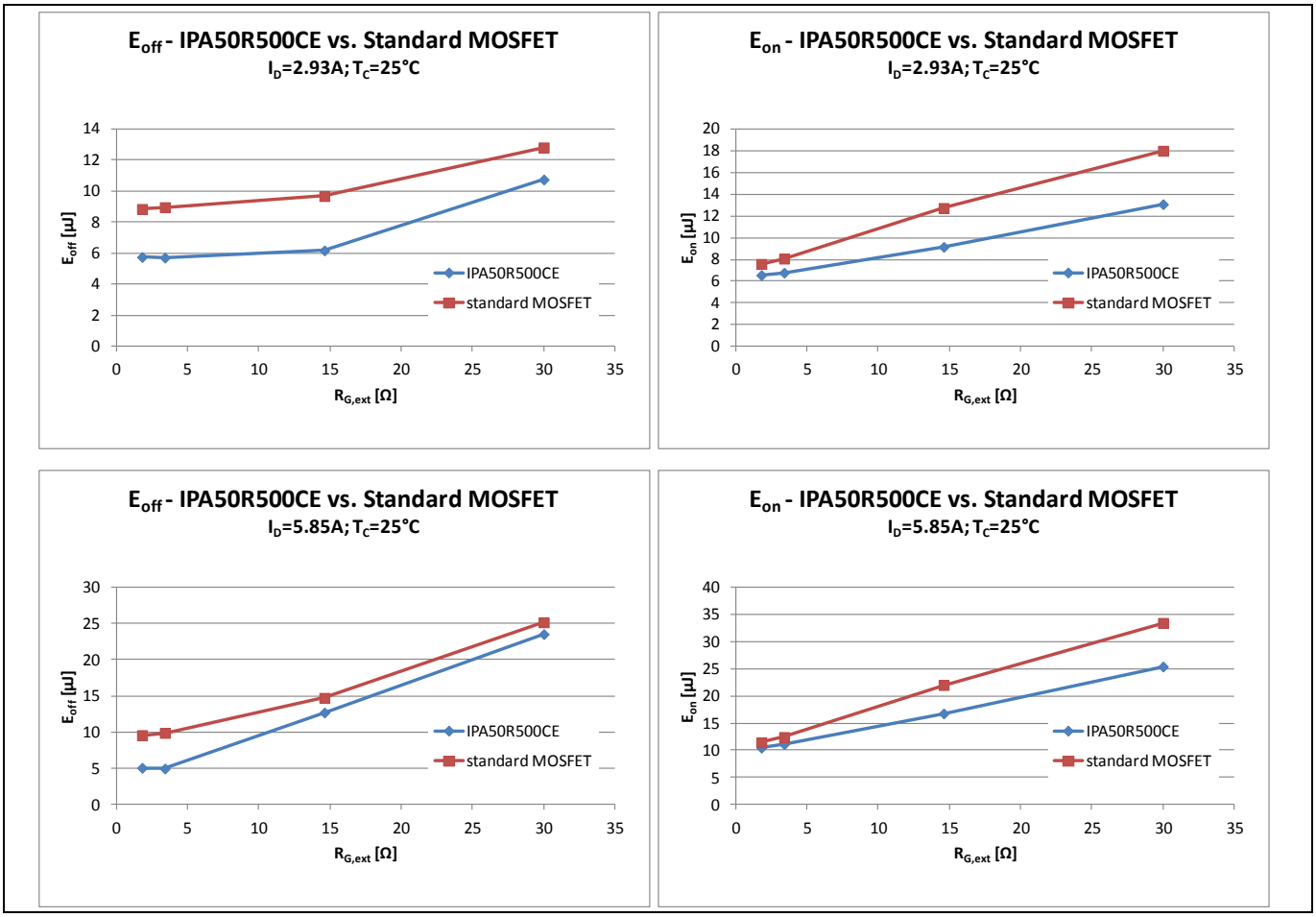



**Figure 9** **$E_{on}$ and $E_{off}$ comparison IPA50R500CE vs. standard MOSFET at $I_D$=2.93 A (upper) and $I_D$=5.85 A (lower)**

It is shown that the $E_{on}$ and $E_{off}$ are much lower on the 500 V CE. Furthermore, it is visible that due to the differences in the $E_{off}$ behavior, it is possible to reduce the switching losses in comparison to the standard MOSFET both in hard switching DCM Mode PFC and soft switching/resonant topologies where the turn-off losses are dominant. Especially at higher loads it is visible that the reduction to for example 4 Ω $R_{G,ext}$ brings you about 5 µJ lower $E_{off}$.

## 4.2 Hard commutation on conducting body diode

Higher switching speeds could also cause drawbacks in case of, for example, high di/dt which could provoke high voltage peaks during hard commutation on a conducting body diode. The following figure represents this voltage peaks in comparison to a comparable standard MOSFET at hard commutation followed after 2 µs body diode conduction time (under normal operation conditions you will not find longer body diode conduction times than 400 ns).

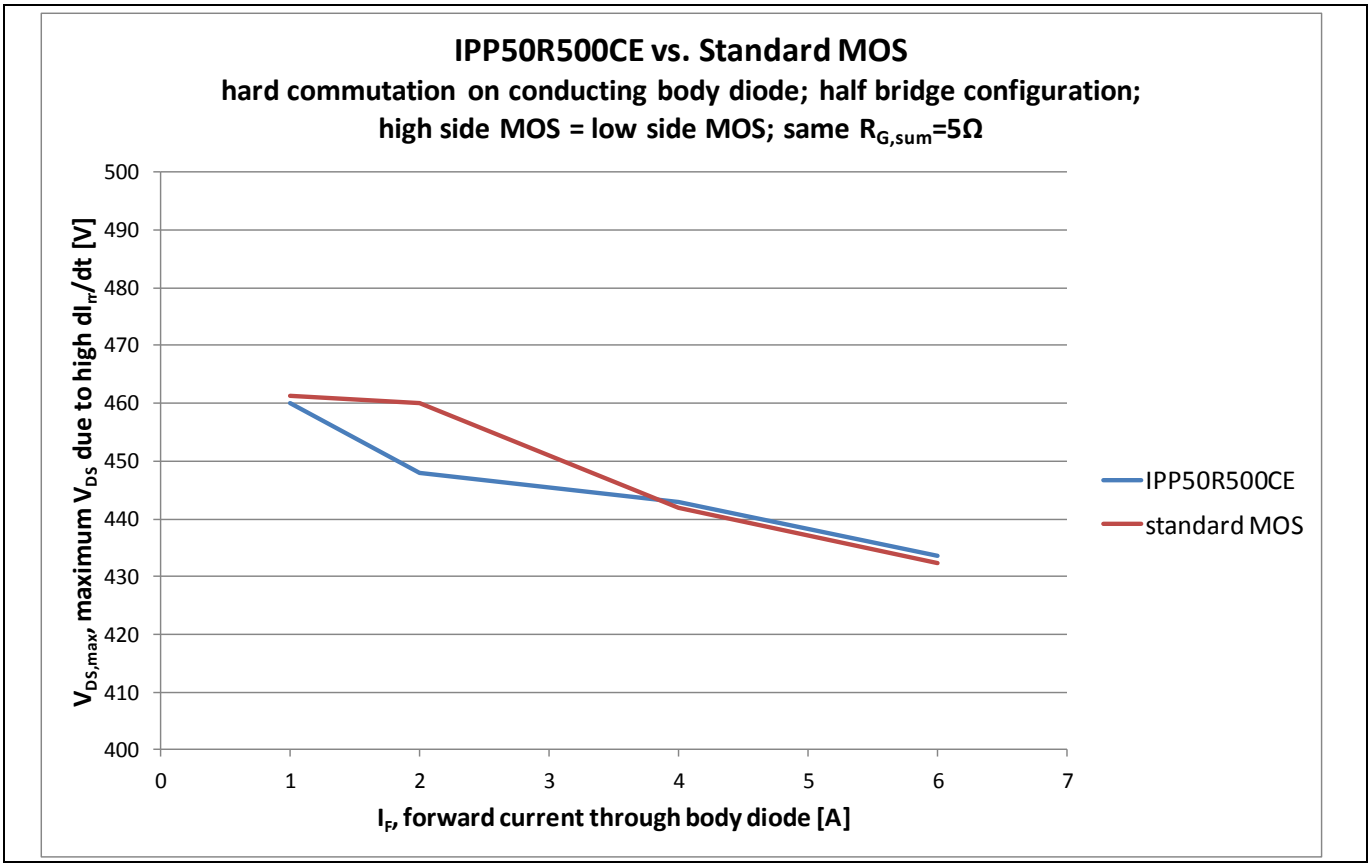



Figure 10 Hard commutation on conduction body diode

It is shown in Gig. 10 that the maximum $V_{DS}$ has lower or the same values as the slower standard MOS. In other words the 500 V CE has the same or, even better, behavior than the comparable standard MOSFET due to the self-limiting dv/dt behavior of this SJ MOSFET family.

These two measurements and the technology parameters show that the 500 V CE brings benefits in hard switching topologies and in soft switching topologies.

The following chapter will represent an important design guideline for using these SJ MOSFETs.

# 5 Design guideline for using 500 V CE

## 5.1 Minimum external gate resistor ($R_{G,ext}$)

The $R_{G,int}$ (internal gate resistor) is defined in the datasheets nevertheless it is recommended to use an $R_{G,ext}$ (external gate resistor) with a value higher than 2 Ω.

## 5.2 Paralleling of 500 V CE

For paralleling 500 V CE, the use of ferrite beads on the gate or separate totem poles is generally recommended.

## 5.3 Safe operation after protection mode

This chapter is going to describe one design guideline which should be followed as a safety precaution. This guide should be followed when using the 500 V CE in a LLC topology in combination with a controller with auto-restart after any kind of protection (over voltage protection (OVP), over current protection (OCP), over power protection (OPP), etc.). If the controller is used in the application with a complete latch-off protection (system has to be manually restarted) this guideline is not applicable.

In order to provide safe operation the pause time between occurring of a protection state and auto-restart (in this document named as pause time $t_{p_restart}$) should be set with respect to the following equation.

$$t_{p_restart} = (L_r + 5\mu H) \cdot \frac{0.5 \cdot I_S}{V_F} \quad \textbf{(2)}$$

| | | | |
|---|---|---|---|
| $t_{p_restart}$ | $[\mu s]$ | … | pause time between occurring of protection state and auto-restart |
| $L_r$ | $[\mu H]$ | … | resonant inductance or leakage inductance of main transformer |
| $I_S$ | $[A]$ | … | continuous forward current of body diode |
| $V_F$ | $[V]$ | … | forward voltage of body diode |

The following figure represents a simplified schematic that represents an LLC half bridge and the $t_{p_restart}$ in correspondence of the gate signal.

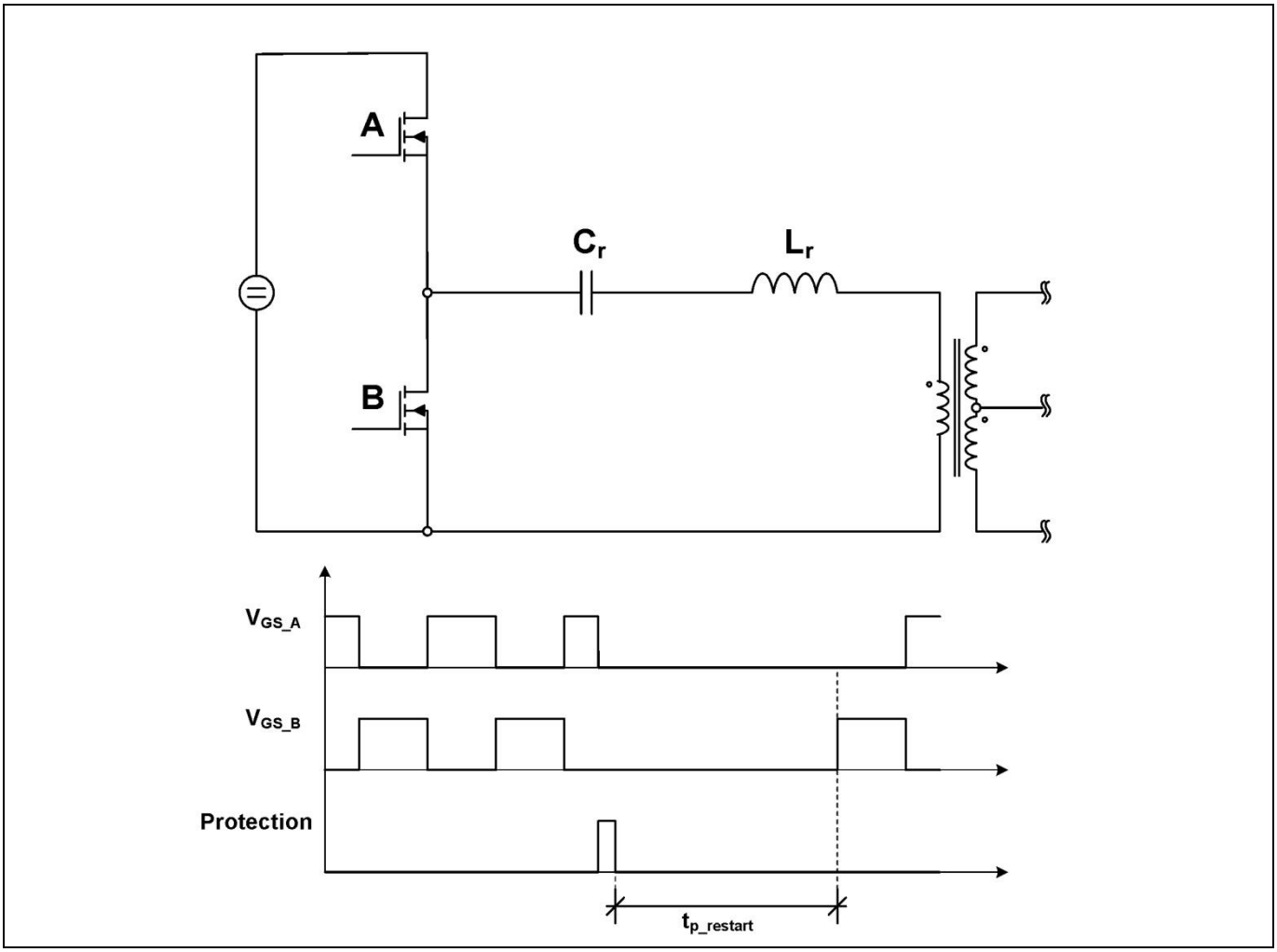



**Figure 11 Simplified circuitry for LLC half bridge and corresponding gate drive signal with auto-restart**

Last but not least the next chapter is going to illustrate the 500 V CoolMOS™ CE naming system and product portfolio.

# 6 Portfolio

500 V CoolMOS™ CE series follows the same naming guidelines as already established with the CP series e.g. IPP50R500CE:

I … Infineon Technologies
P … power MOSFET
P … package type (TO-220)
50 … voltage class divided by 10
R500 … on-state resistance in milli Ohms
CE … name of the serie

| $R_{DS(on)}$ [mΩ] |  TO-220 FullPAK |  TO-220 |  TO-252 DPAK |  TO-251 IPAK |  TO-247 |  SOT-223 |
|---|---|---|---|---|---|---|
| 3000 | | | IPD50R3K0CE | IPU50R3K0CE | | IPN50R3K0CE |
| 2000 | | | IPD50R2K0CE | IPU50R2K0CE | | IPN50R2K0CE |
| 1400 | | | IPD50R1K4CE | IPU50R1K4CE | | IPN50R1K4CE |
| 950 | IPA50R950CE | | IPD50R950CE | IPU50R950CE | | IPN50R950CE |
| 800 | IPA50R800CE | | IPD50R800CE | | | IPN50R800CE |
| 650 | IPA50R650CE | | IPD50R650CE | | | IPN50R650CE |
| 500 | IPA50R500CE | IPA50R500CE | IPD50R500CE | | | |
| 380 | IPA50R380CE | IPA50R380CE | IPD50R380CE | | | |
| 280 | IPA50R280CE | IPA50R280CE | IPD50R280CE | | IPW50R280CE | |
| 190 | IPA50R190CE | IPA50R190CE | | | IPW50R190CE | |

**Figure 12 Portfolio 500 V CoolMOS™ CE**

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[1] T. Fujihira: “Theory of Semiconductor Superjunction Devices”, Jpn. J. Appl. Phys., Vol.36, pp. 6254-6262, 1997

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[7] Dr. H. Kapels: “Superjunction MOS devices – From device development towards system optimization”, paper EPE 2009 – Barcelona, ISBN 9789075815009, pp. 3

## Revision History

### Major changes since the last revision

| Page or Reference | Description of change |
|---|---|

| Page or Reference | Description of change |
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