Application note: safety limits for ISO1I8xx-ICs

ISOFACE™: ISO1I811T/ISO1I813T/ISO1I815T

About this document

Scope and purpose

This is an application note describing the safety limits for the ISO1I8xx-ICs series of isolated eight-channel digital-input ICs with IEC61131-2 type 1/2/3 characteristics.

Intended audience

For engineers interested in industrial automation.

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1 Introduction

Safety limits of allowed current or allowed power dissipation are intended to prevent an over-temperature condition. They are also intended to prevent potential damage to the isolation barrier and a voltage breakdown between the two voltage domains.

Precautions were taken during the conception phase of the architecture (described in chapter 2). In chapter 3 the electrical and thermal parameters are listed, which are used for calculation of the allowed current in the sense chip. Chapter 4 deals with the split of the sense current into an external and internal part. Only the internal part has be considered for the calculation of safety limits.The most important chapters are 5 and 6. In these chapters the junction temperature T_j is calculated based on the variable ambient temperature and the temperature rise due to the I_{VBB} current in the sense chip, the I_{VCC} current in the uC interface chip and the sink current in the sense chip. The related power dissipation is multiplied with the thermal resistance junction-to-air. The criterion for the allowed currents is T_j less than 150°C and for the maximum power dissipation of the whole chip it is P_{tot_max} less than or equal to 0.8 W. From these requirements a limitation for the allowed ambient temperature and for I_{VBB} and I_{VCC} is derived.

All figures and curves are calculated with reference to the electrical and thermal characteristics of the datasheet.

2 Safety-relevant architecture

Figure 1 emphasizes the location of the coreless transformer. It is placed on the uC interface chip (DIE 2). The temperature-critical chip is the sense chip (DIE 1). The chips DIE1 and DIE2 are located on a split lead-frame to establish the isolation. Any temperature increase on the sense chip has only indirect influence on the uC interface chip and therefore on the coreless transformer only via the split lead-frame and the package.

The internal current sinks limit the sense current of each external attached sensor. The external resistor network splits the sense current into an external current over the resistor R_{ext} (= 12 kΩ for type 1 and 3 or = 8.5 kΩ for type 2) and the internal current into the chip inputs I × H, × = 0, …, 7.

Therefore only a limited portion of the sense current enters the IC and therefore only a limited portion of the sense current contributes to the internal power dissipation (Figure 2).

The chip is not equipped with any temperature shut-down mechanism.

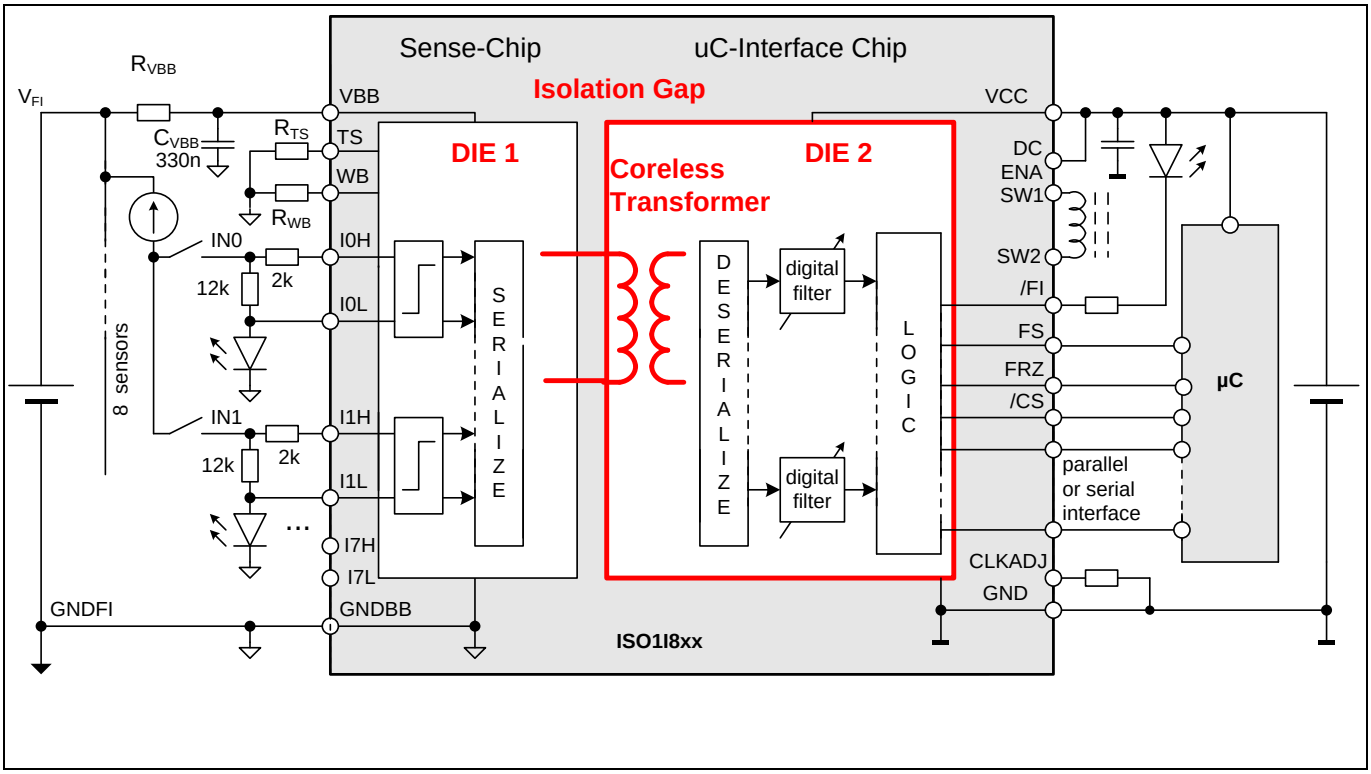


Figure 1 Typical application diagram with internal structure of galvanic isolation

3 Prerequisites for calculating safety limits

For calculating the safety limits the maximum values of the relevant parameters are chosen. All underlying calculations refer to these parameters.

Table 1 Prerequisites for calculating safety limits

Parameter	Maximum values used	Comment
$R_{th(JA)}$	88.6 K/W	Thermal resistance junction-ambient, maximum, see Note: Thermal resistance, PCB
$I_{VCC=2.85V}$ $I_{VCC=3.6V}$ $I_{VCC=5.5V}$	0.005 A 0.006 A 0.006 A	Maximum V_{CC} current of uC interface chip
ISO1I813/815: $I_{VBB=9.6V}$ $I_{VBB=24V}$ $I_{VBB=35V}$	 0.0115 A 0.012 A 0.0125 A	Maximum quiescent current of sense chip, all sense currents equal zero Coreless transformer frequency: 500 kHz
ISO1I811: $I_{VBB=9.6V}$ $I_{VBB=24V}$ $I_{VBB=35V}$	 0.0085 A 0.009 A 0.0095 A	Maximum quiescent current of sense chip, all sense currents equal zero Coreless transformer frequency: 100 kHz
P_{tot_max}	0.8 W	Maximum rating of total dissipated power
T_{jmax}	150.0°C	Maximum junction temperature
$I_{INxsnkM13}$	3.4 mA	Sink current limit at maximum input voltage type 1 and 3, V_{VBB} = 35 V, V_{INx} = 30 V, V_{ixL} = 2.5 V
$I_{INxsnkM2}$	4.8 mA	Sink current limit at maximum input voltage type 2, V_{VBB} = 35 V, V_{INx} = 30 V, V_{ixL} = 2.5 V
$P_{VCC=2.85V}$ $P_{VCC=3.6V}$ $P_{VCC=5.5V}$	0.014 W 0.022 W 0.033 W	Maximum quiescent power dissipation of uC interface chip
ISO1I813/815: $P_{VBB=9.6V}$ $P_{VBB=24V}$	 0.110 W 0.288 W	Maximum quiescent power dissipation of sense chip, all sense currents equal zero Coreless transformer frequency: 500 kHz

Parameter	Maximum values used	Comment
$P_{VBB=35V}$	0.438 W	
ISO1I811: $P_{VBB=9.6V}$ $P_{VBB=24V}$ $P_{VBB=35V}$	0.082 W 0.216 W 0.333 W	Maximum quiescent power dissipation of sense chip, all sense currents equal zero Coreless transformer frequency: 100 kHz
$P_{Sink_1_3_max}$	23 mW	Type 1 and 3 Maximum internal power dissipation due to sense current/channel Due to current into pin I × H
$P_{Sink_2_max}$	33 mW	Type 2 Maximum internal power dissipation due to sense current/channel Due to current into pin I × H

Note: Thermal resistance at 2 cm^2 cooling area (thermal conductance only by radiation and free convection). Device on 50 mm × 50 mm × 1.5 mm epoxy PCB FR4 with 2 cm^2 (one layer, 35 µm thick) copper area. PCB is vertical without blown air.

Table 2 Formulas for calculating safety limits

Purpose	Formula
Total power dissipation	$\mathbf{P_{tot}(T) = P_{VCC=xV} + P_{VBB=xV} + P_{Sink_1_3_max} *8}$ $\mathbf{P_{tot}(T) = P_{VCC=xV} + P_{VBB=xV} + P_{Sink_2_max} *8}$ 8 channels
Condition for $I_{VBB}(T_A)$	**Condition: T less than or equal to 150°C and P_{tot} less than 0.8 W --> allowed I_{VBB}** $\mathbf{150°C = T_A + (P_{VCC=xV} + P_{VBB=xV}) *R_{TH(JA)} + P_{Sink_1_3_max} *8 *R_{TH(JA)}}$ $\mathbf{150°C = T_A + (P_{VCC=xV} + P_{VBB=xV}) *R_{TH(JA)} + P_{Sink_2_max} *8 *R_{TH(JA)}}$
$I_{VBB_Allowed}(T_A)$	**Allowed I_{VBB}:** $\mathbf{I_{VBB_Allowed} = (150 - T_A - P_{VCC=xV} *R_{TH(JA)} - P_{Sink_1_3_max} *8 *R_{TH(JA)})/(V_{VBB=xV} *R_{TH(JA)})}$ $\mathbf{I_{VBB_Allowed} = (150 - T_A - P_{VCC=xV} *R_{TH(JA)} - P_{Sink_2_max} *8 *R_{TH(JA)})/(V_{VBB=xV} *R_{TH(JA)})}$

Figure 2 explains that only a part of the sense current is propagated through the internal current sinks of the sense chip. Figure 2 is contained in the datasheet (ISO1I815: Chapter 3.4 Sensor Input). The sense current is separated into a sink current and into an external current. In case of high sense voltage V_{INx} a great part of the sense current is propagated through the external resistor network. In the case of low sense voltage V_{INx} the sense current is mostly internally dissipated via the internal sinks. Therefore the power dissipation within the sense chip is minimized. In Figure 2 the sense current is assumed to be I_{INx} = 2.1 mA.

The x-axis is the time during a simulation when the sensor voltage V_{INx} is ramping up and down (from 0 V to 30 V) with different slopes.

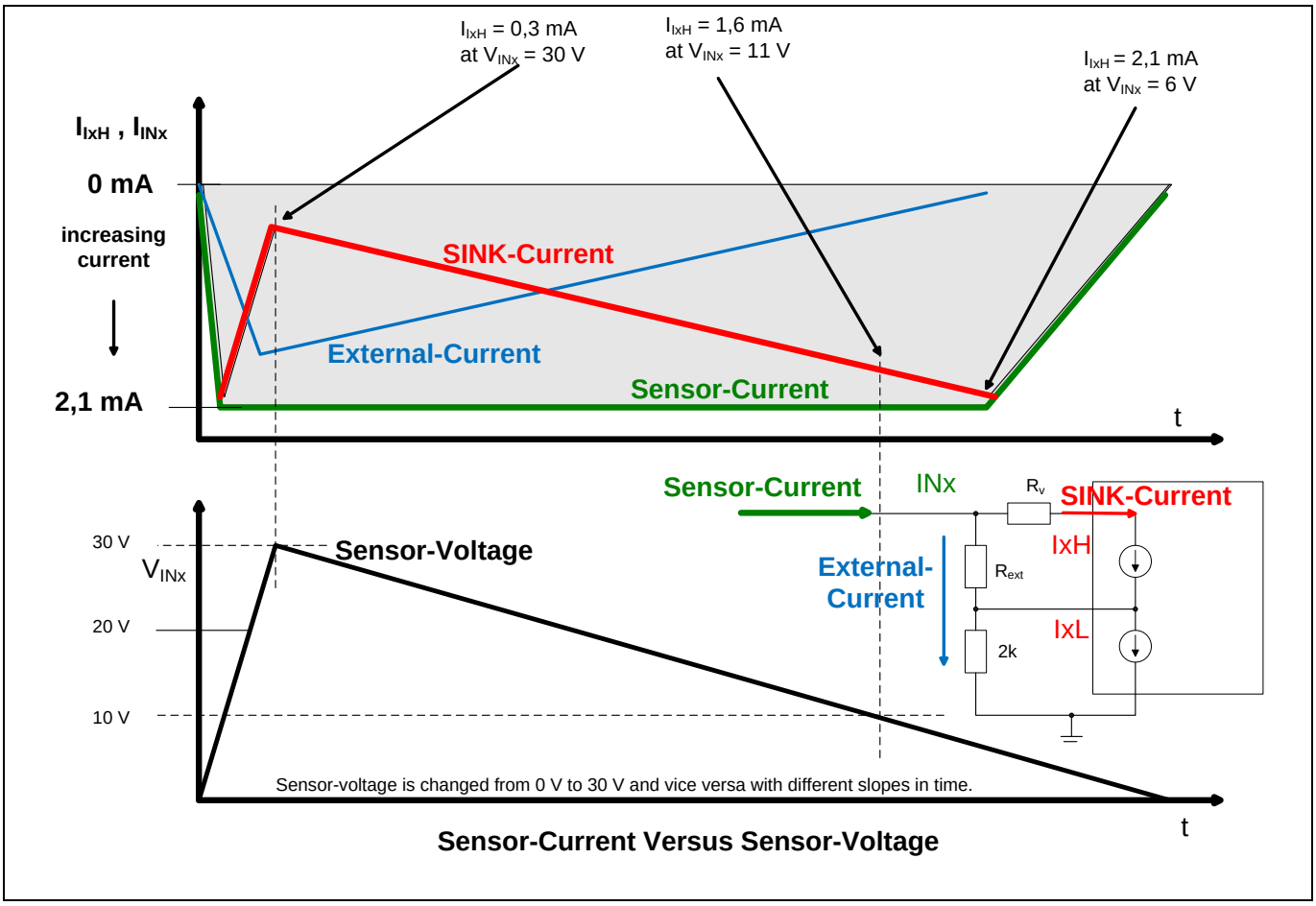


Figure 2 **Splitting of sensor current into sink current and external current for type 1 and 3 (IEC61131-2)**

4 Sink current

In Figure 2 the sense current is assumed to be I_{INx} = 2.1 mA. This current is split into an internal sink current and an external current. Test results are available for this split. These results are extrapolated to the maximum values in the datasheet.

$I_{INxsnkM13}$ for type 1 and 3

and

$I_{INxsnkM2}$ for type 2.

Figure 3 and Figure 4 determine the split values including the internal sink power dissipation for type 1 and 3.

Figure 5 and Figure 6 determine the split values including the internal sink power dissipation for type 2.

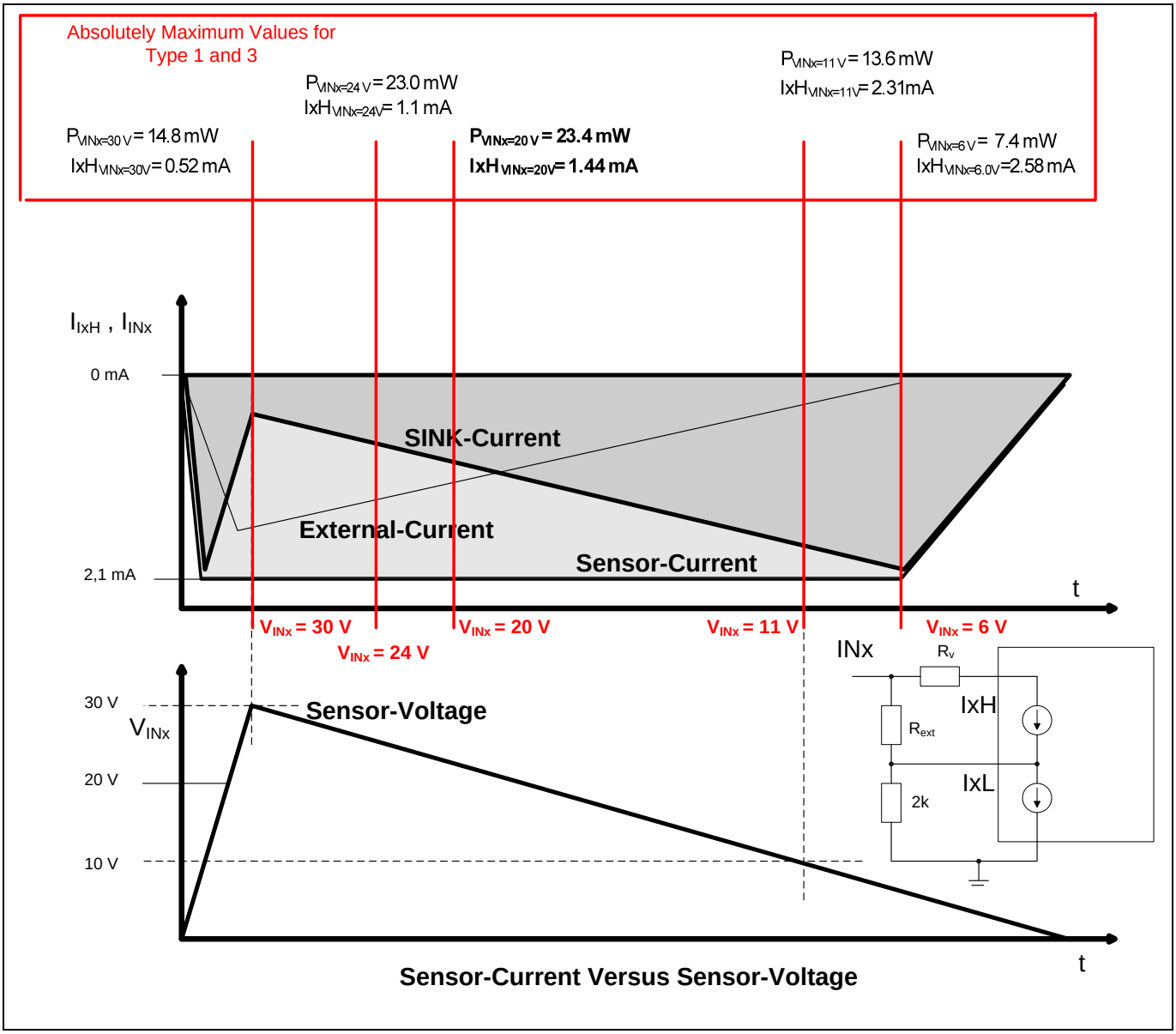
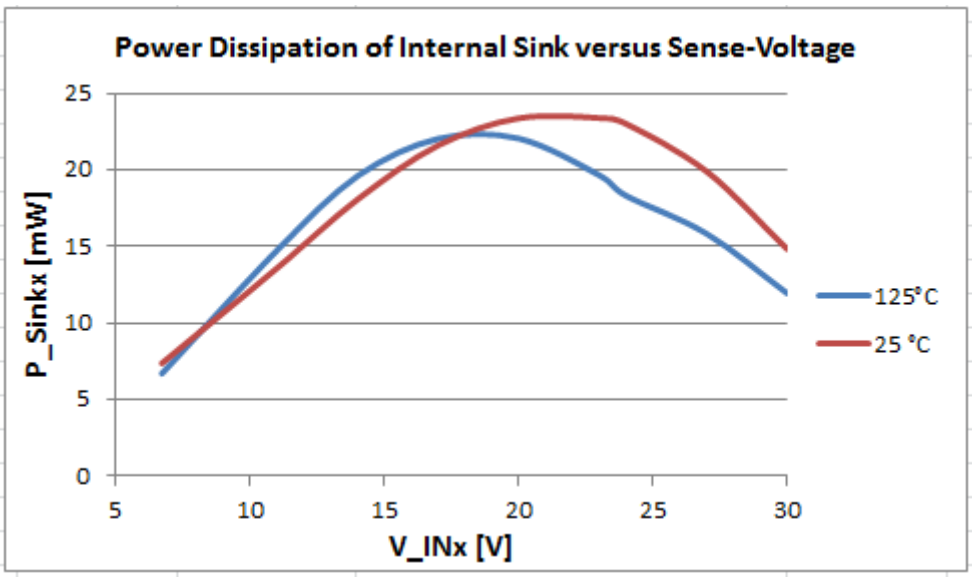
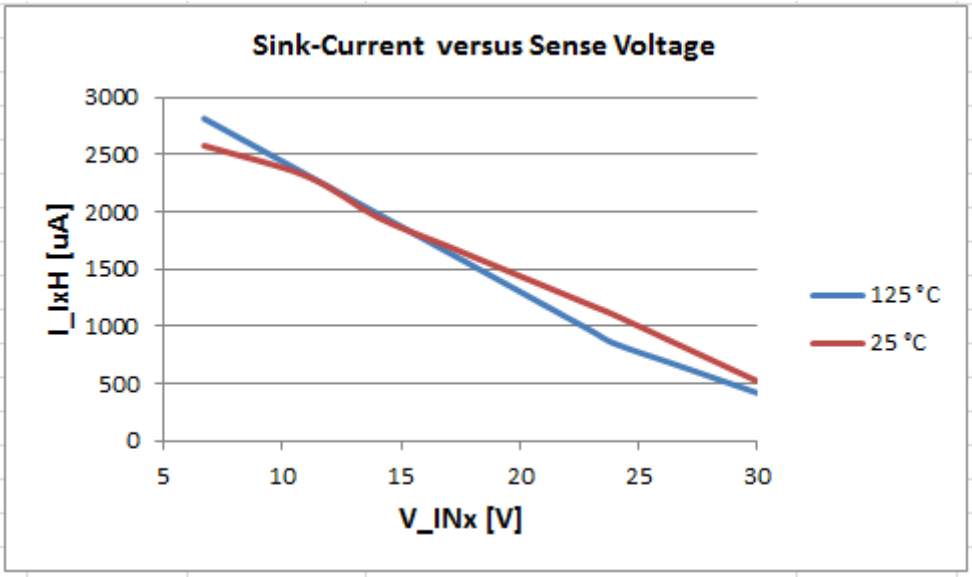


Figure 3 Split of sense current, internal power dissipation, type 1 and 3





Type 1, 3

Figure 4 Determination of worst-case internal power dissipation due to sink current, type 1 and 3

For type 1 and 3 the maximum sink power dissipation is $P_{Sink_1_3_max}$ = 23.4 mW.

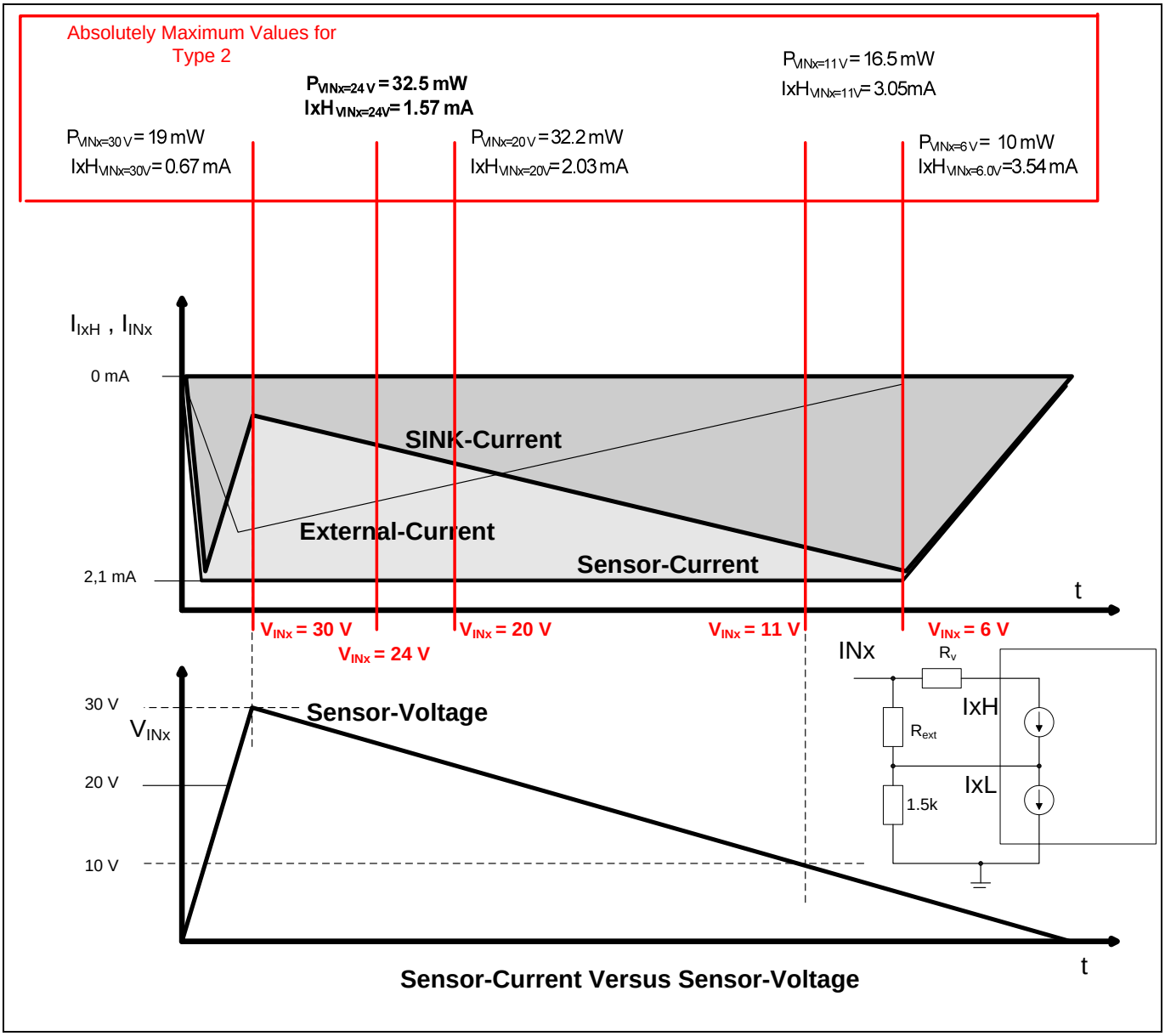
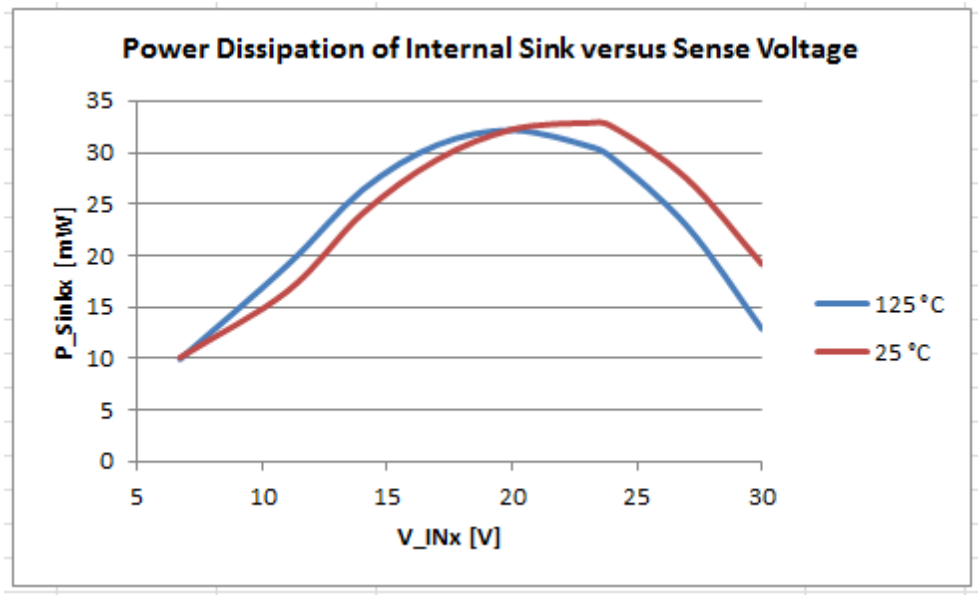
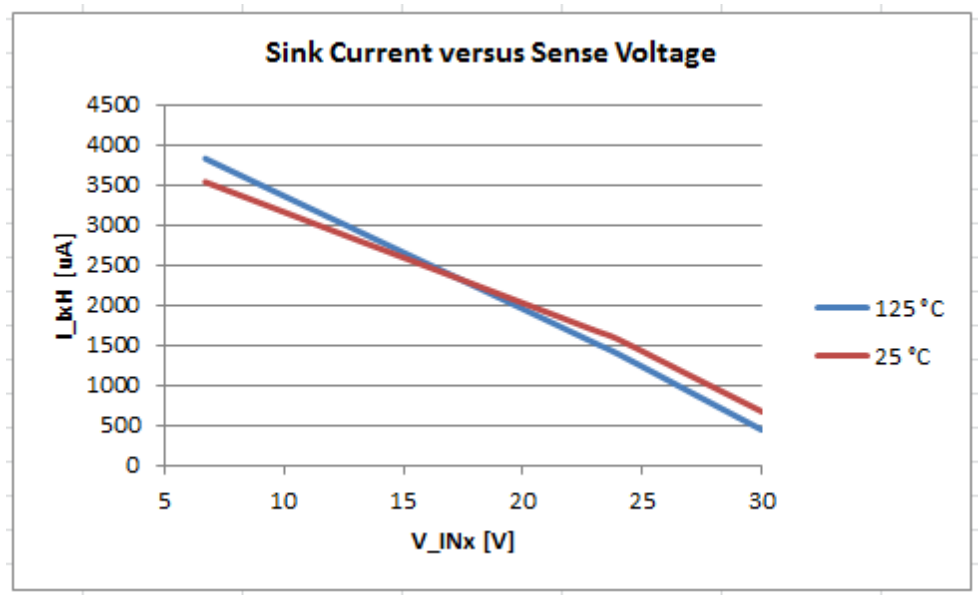


Figure 5 Split of sense current, internal power dissipation, type 2





Type 2

Figure 6 Determination of worst-case internal power dissipation due to sink current, type 2

For type 2 the maximum sink power dissipation is $P_{Sink_2_max}$ = 32.5 mW.

5 Safety limits ISO1I813T, ISO1I815T

The maximum allowed power dissipation of the total chip (including two dies) is limited by two constraints: the junction temperature has to be less than T_j = 150°C and the total power dissipation of the total chip (including two dies) has to be less than 0.8 W.

Based on the ambient temperature the temperature increase is calculated due to three power dissipation parts:

1. power dissipation of uC interface chip (dependent on V_{CC})

2. power dissipation of sense chip (dependent on V_{BB}) and

3. power dissipation due to the sink currents.

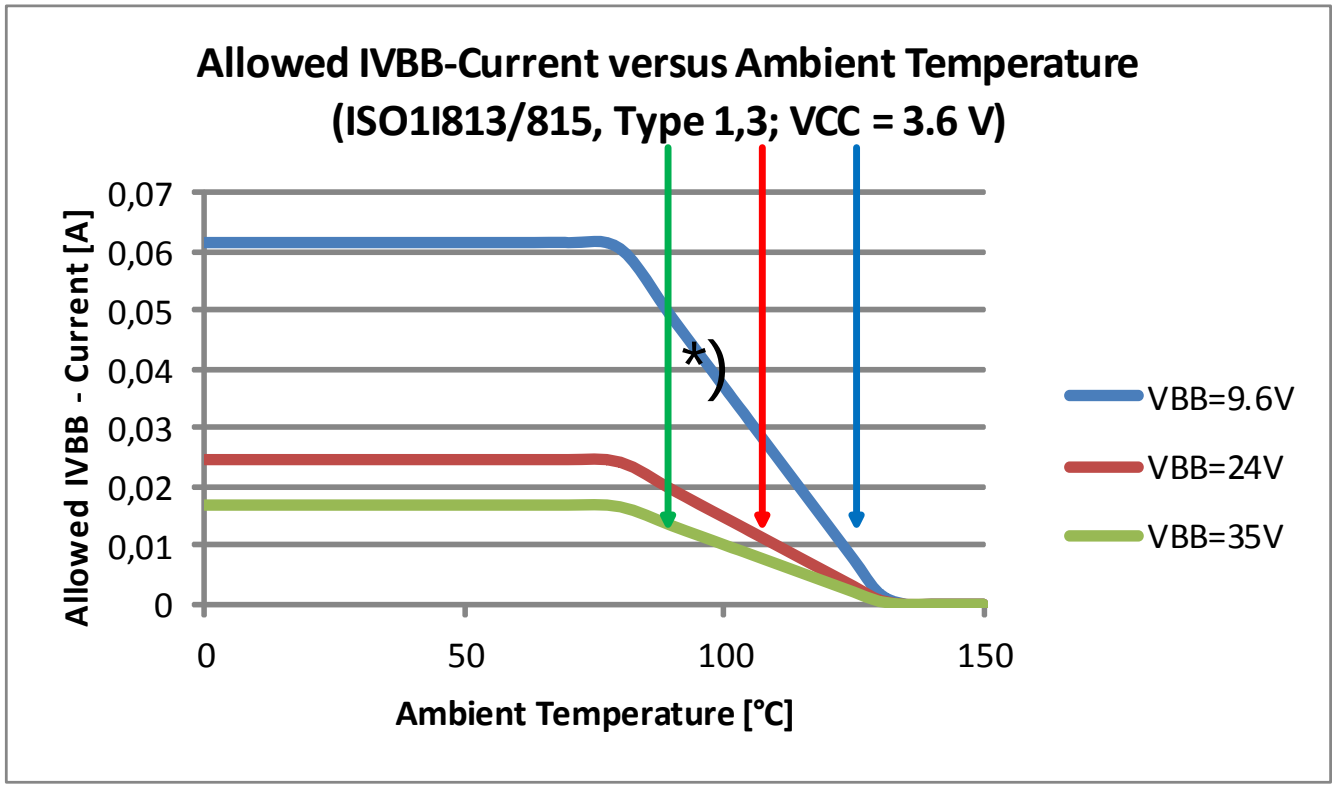
Figure 7 and Figure 8 give the allowed I_{VBB} current independent of the ambient temperature. These figures contain the absolute worst-case condition of all incorporated parameters (except V_{CC} = 3.6 V is fixed). The internal current consumption of the sense chip in addition to the value of V_{BB} has the most severe effect on the power consumption.

In this calculation V_{CC} = 3.6 V and V_{BB} = 9.6 V, 24 V, 35 V.

Condition:
T less than or equal to 150°C and
P_{tot} less than P_{tot_max} = 0.8 W --> **allowed I_{VBB}:**

$$150°C = T_A + (P_{VCC=3.6V} + P_{VBB=xV}) * R_{TH(JA)} + P_{Sink_1_3/_2_max} * 8 * R_{TH(JA)}$$

$$P_{tot_max} = P_{VCC=3.6V} + P_{VBB=xV} + P_{Sink_1_3/_2_max} * 8$$



*) :Reduction of I_{VBB}-current to limit junction temperature to less than 150 °C would affect functional operation.

Figure 7 ISO1I813T/815T: Safety I_{VBB} current limits for type 1 and 3

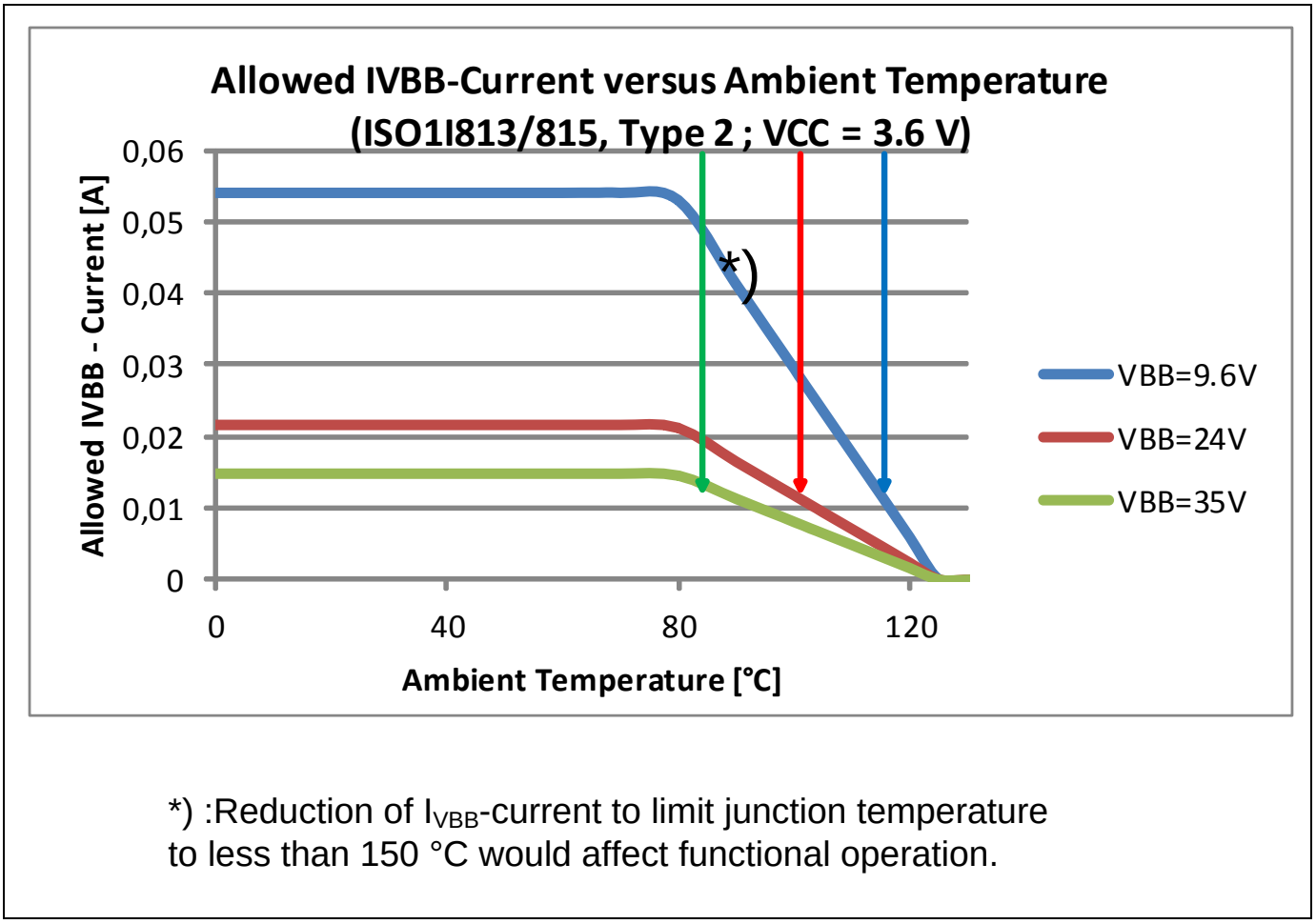


Figure 8 ISO1I813/815: Safety I_{VBB} current limits for type 2

Figure 7 and Figure 8 classify the lower values of ambient temperature from which no operation is allowed because the internal power dissipation already leads to a junction temperature of 150°C.

Figure 9 and Figure 10 give the allowed I_{VCC} current independent of the ambient temperature. These figures contain the absolute worst-case condition of all incorporated parameters.

In this calculation V_{CC} = 2.85 V, 3.6 V, 5.5 V and V_{BB} = 24 V, 35 V.

Condition:
T less than or equal to 150°C and
P_{tot} less than P_{tot_max} = 0.8 W --> **allowed I_{VCC}:**

$150°C = T_A + (P_{VCC=xV} + P_{VBB=xV}) * R_{TH(JA)} + P_{Sink_1_3/_2_max} * 8 * R_{TH(JA)}$

$P_{tot_max} = P_{VCC=xV} + P_{VBB=xV} + P_{Sink_1_3/_2_max} * 8$

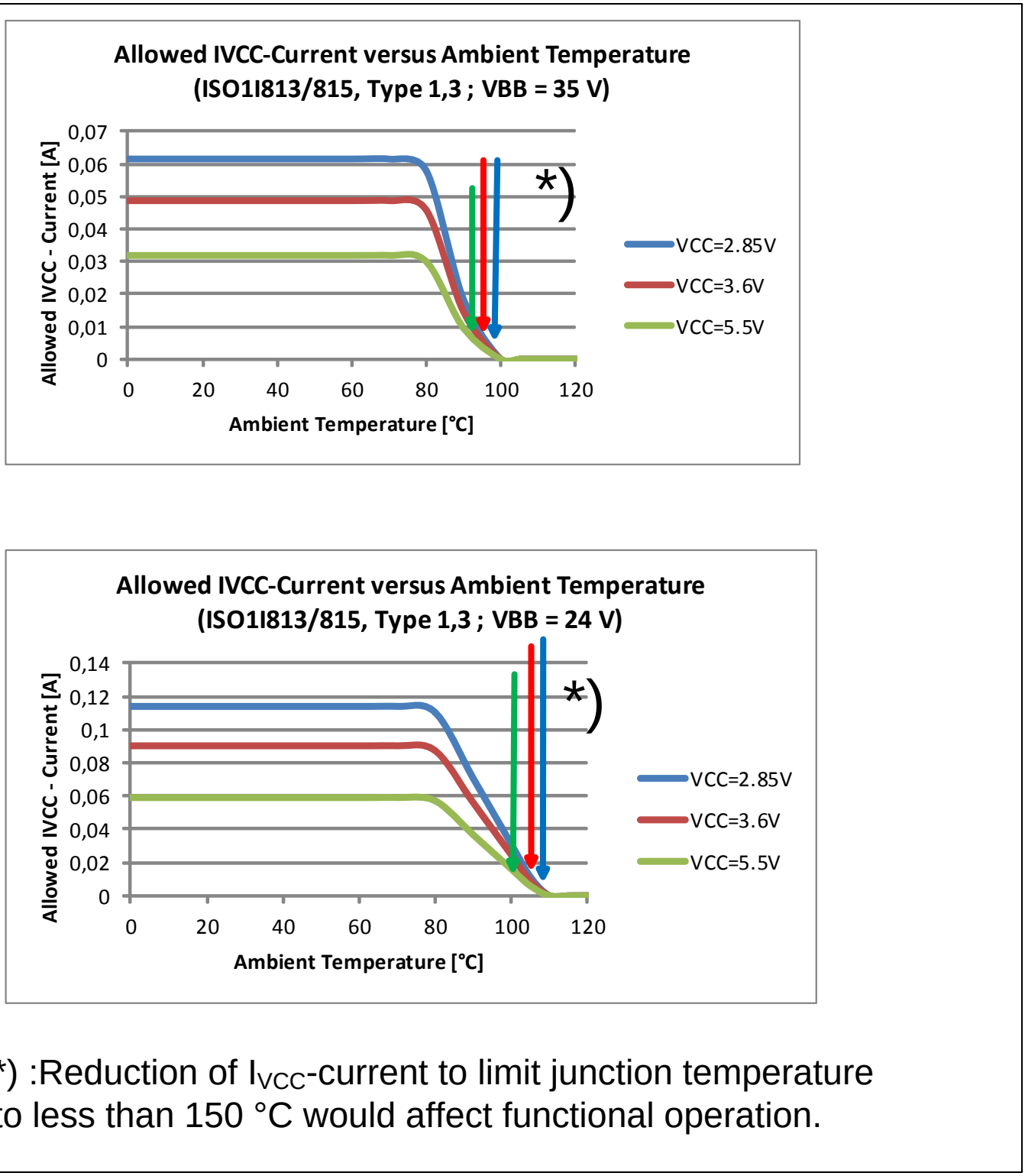


Figure 9 ISO1I813T/815T: Safety I_{VCC} current limits for type 1 and 3

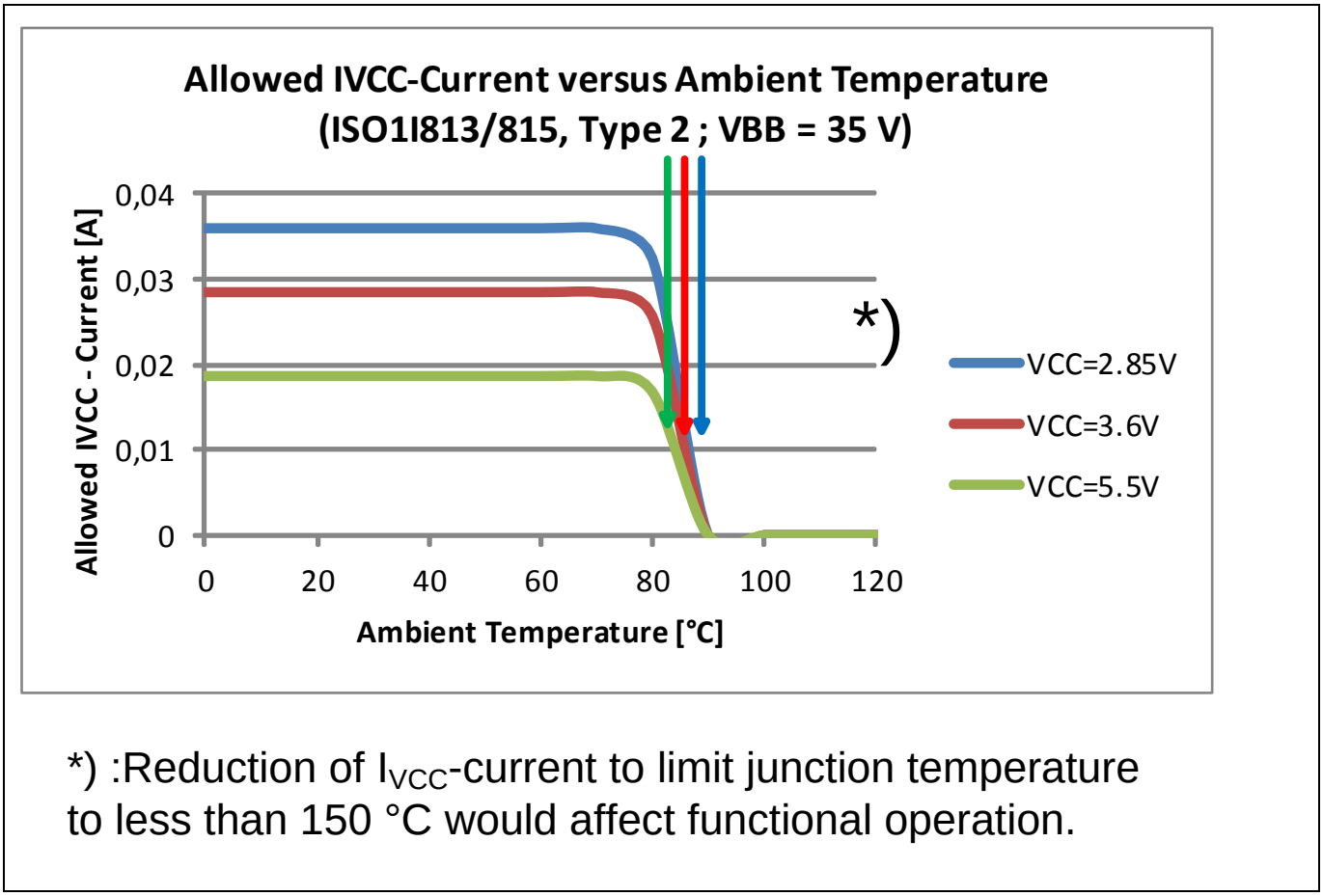


Figure 10 ISO1I813T/815T: Safety I_{VCC} current limits for type 2

Figure 9 and Figure 10 classify the lower values of ambient temperature from which no operation is allowed because the internal power dissipation already leads to a junction temperature of 150°C.

6 Safety limits ISO1I811T

In the following the same safety limiting curves are calculated for the ISO1I811T. This circuitry operates with a reduced coreless transformer (CT) data rate (in the region of 100 kHz). Therefore the current consumption is less than for the ISO1I813/815. Figure 11 explains the linear behavior of the internal current consumption with the CT frequency. Figure 12 shows the method of adjustment of the CT frequency. Both figures are available in the datasheets.

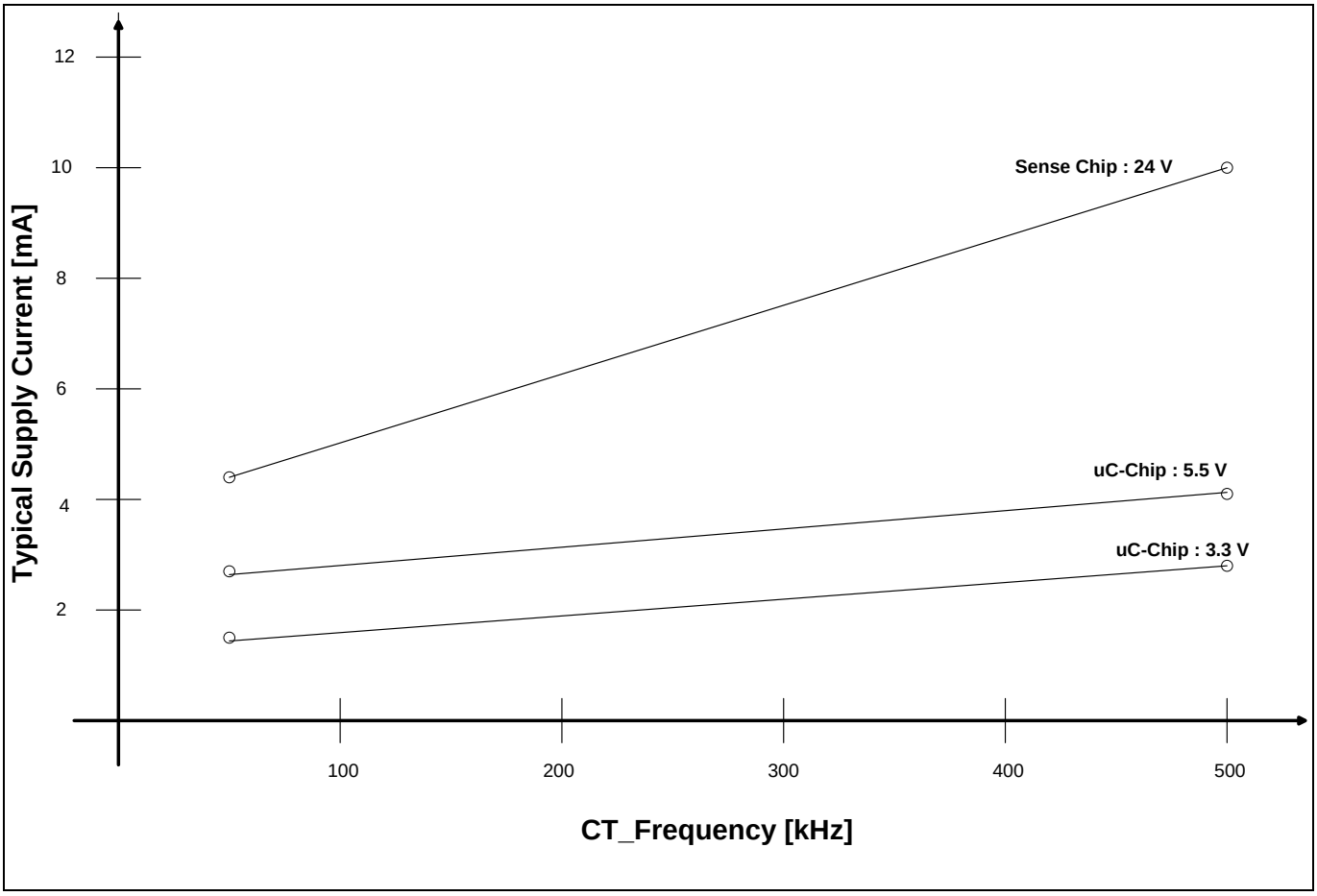


Figure 11 Dependency of the internal current consumption on the CT frequency

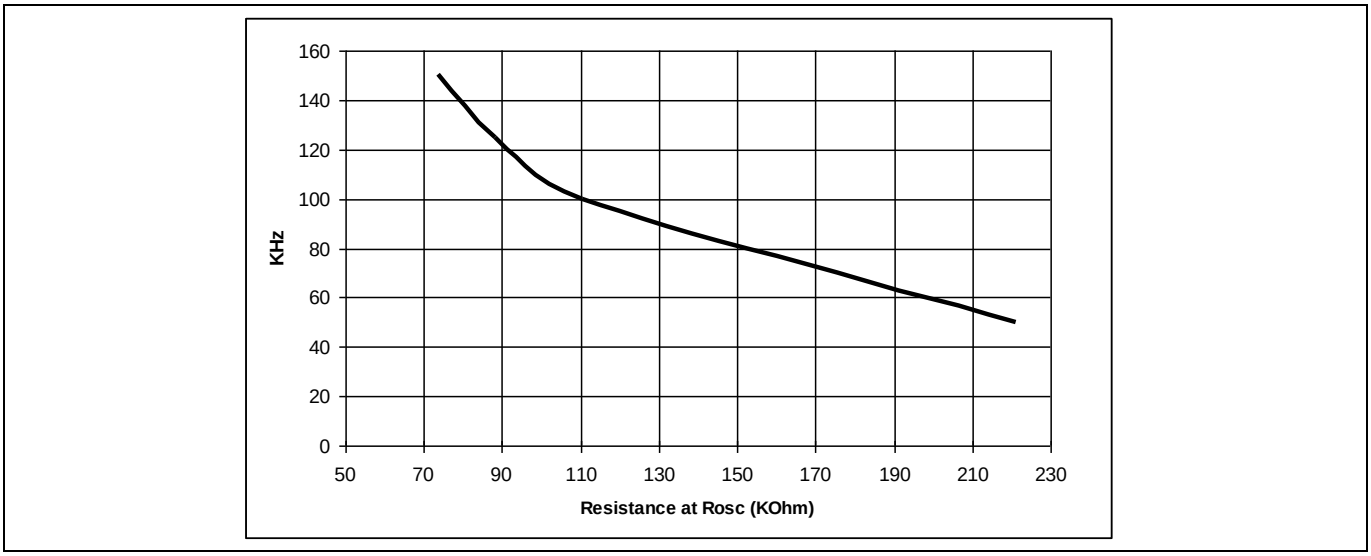
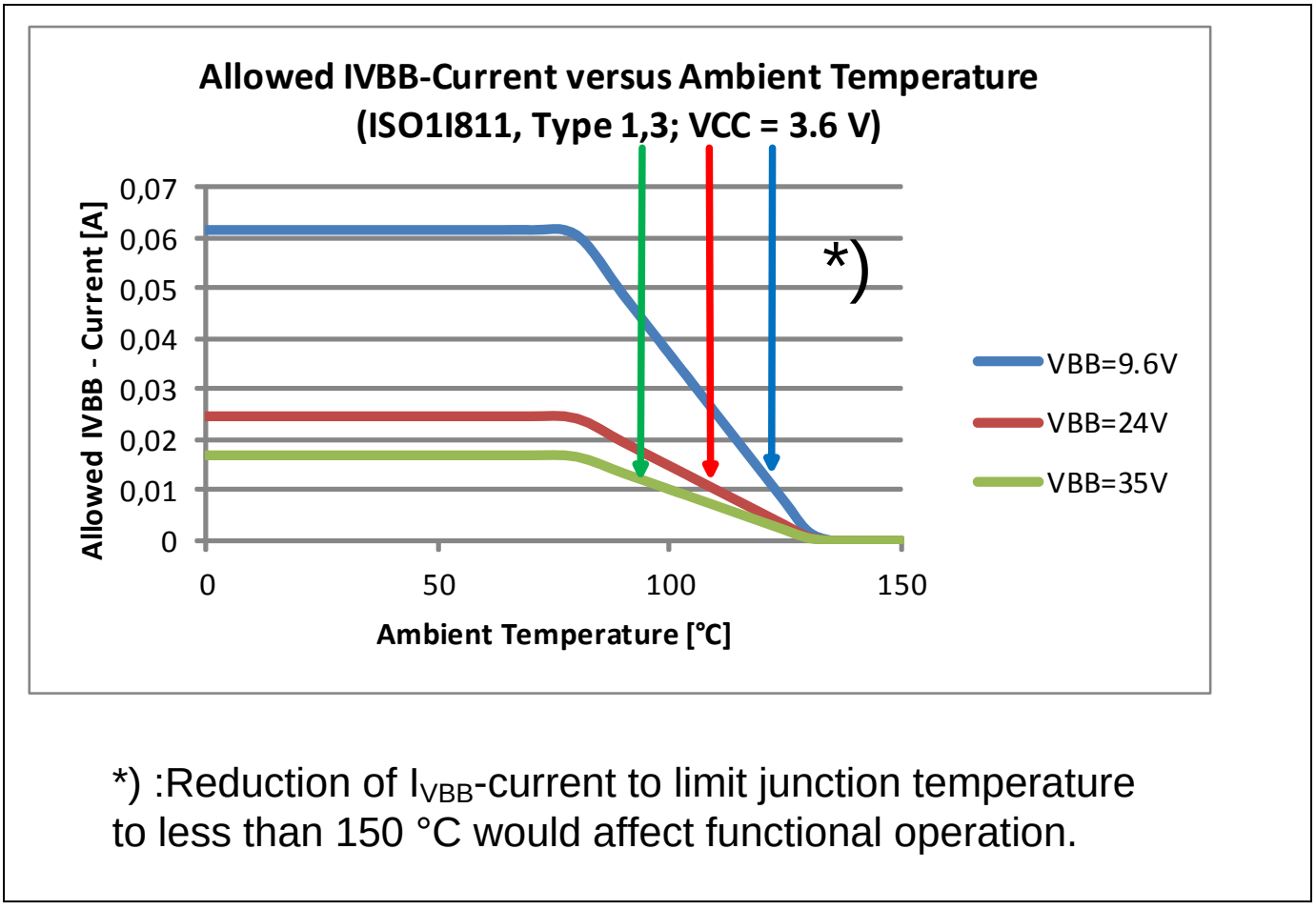
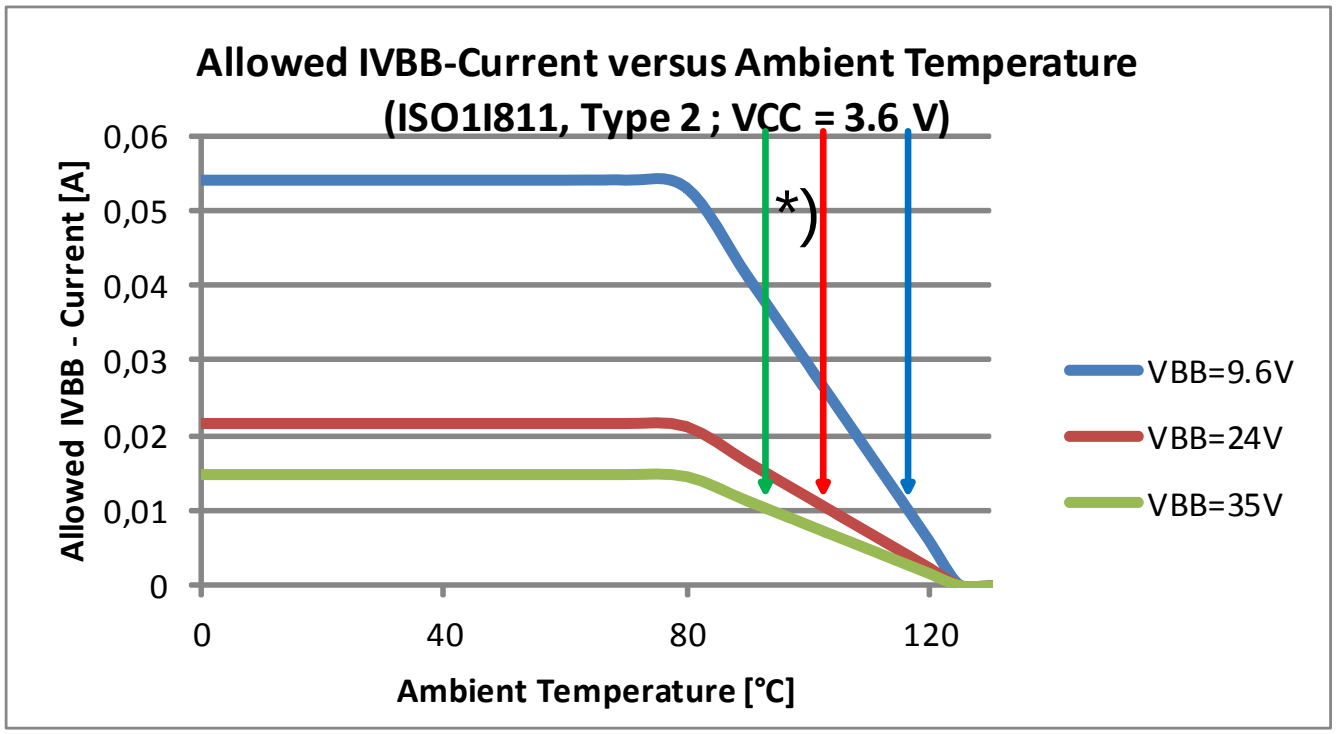


Figure 12 Adjustment of the CT frequency by the R_{osc} resistance



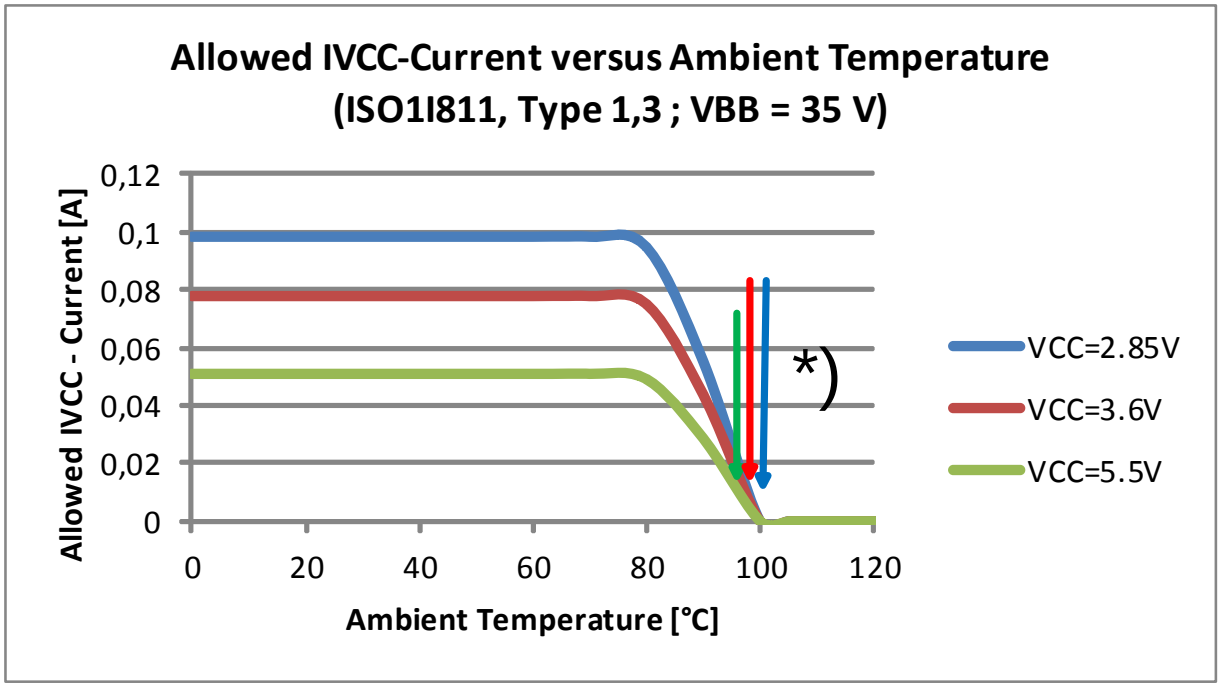
*) :Reduction of I_{VBB}-current to limit junction temperature to less than 150 °C would affect functional operation.

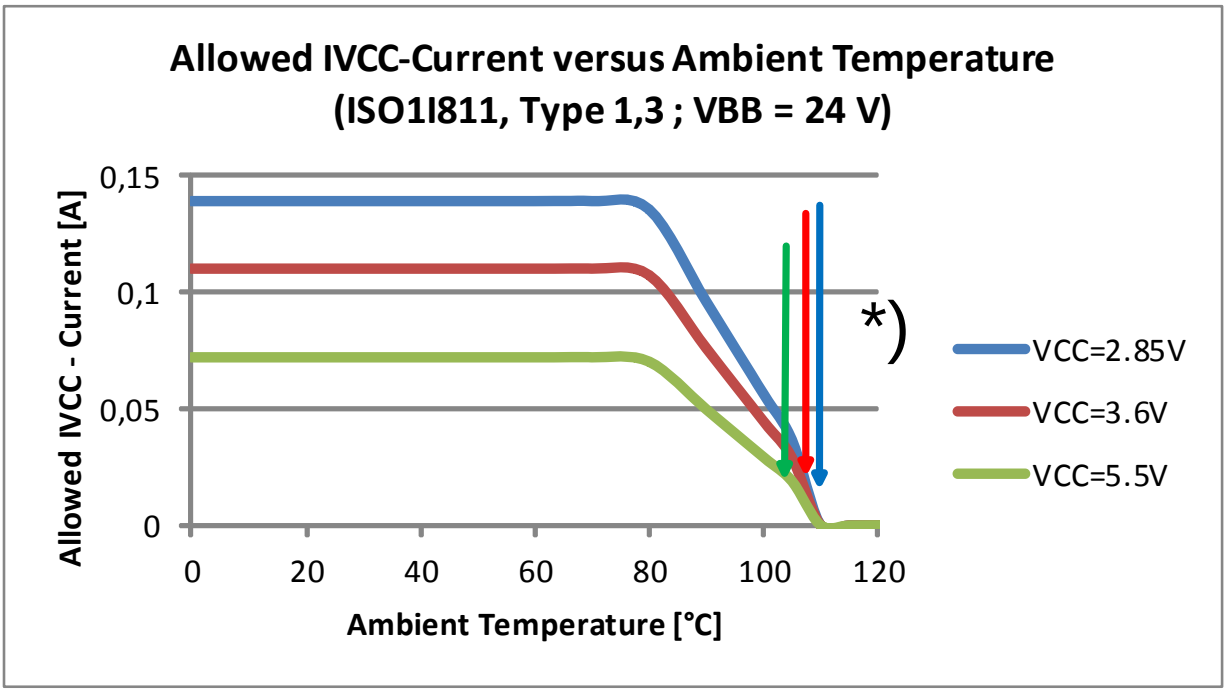
Figure 13 ISO1I811T: Safety I_{VBB} current limits for type 1 and 3



*) :Reduction of I_{VBB}-current to limit junction temperature to less than 150 °C would affect functional operation.

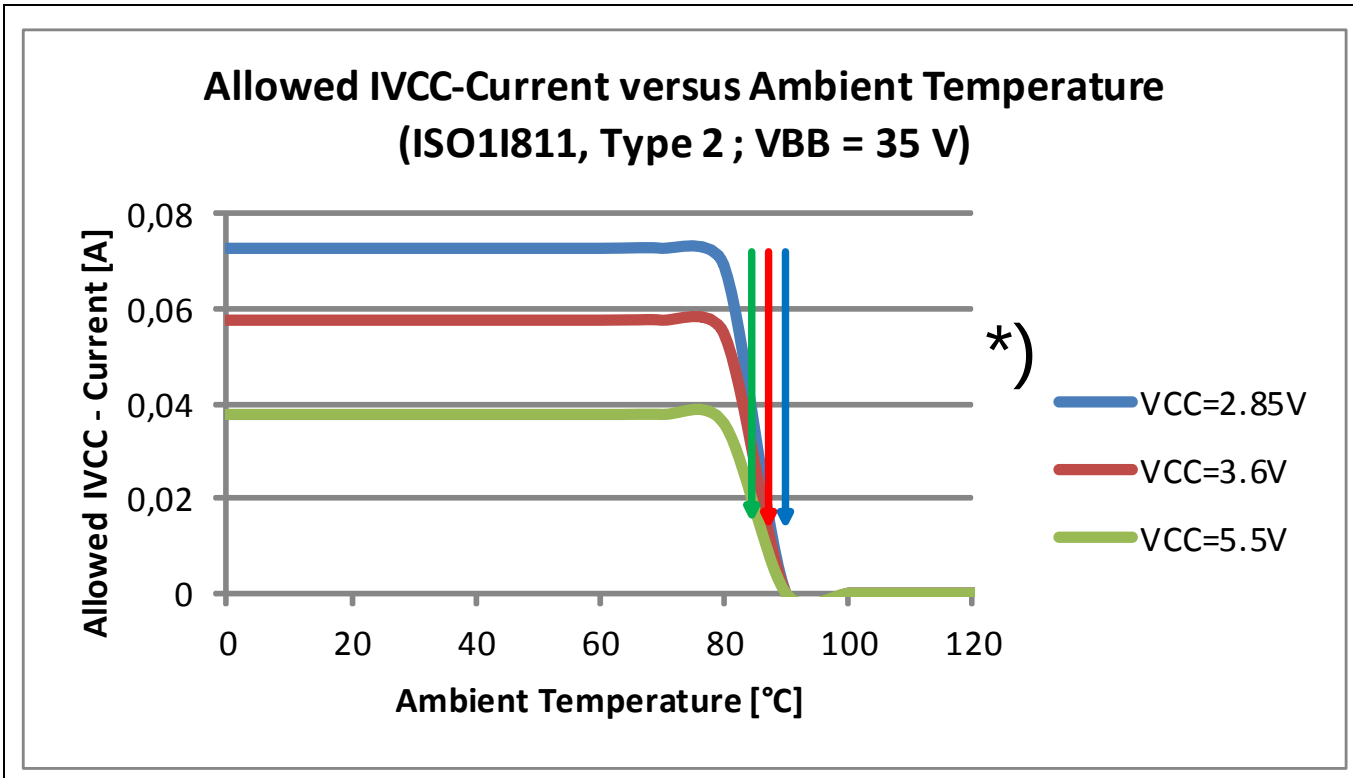
Figure 14 ISO1I811T: Safety I_{VBB} current limits for type 2





*) :Reduction of I_{VCC}-current to limit junction temperature to less than 150 °C would affect functional operation.

Figure 15 ISO1I811: Safety I_{VCC} current limits for type 1 and 3



*) :Reduction of I_{VCC}-current to limit junction temperature to less than 150 °C would affect functional operation.

Figure 16 ISO1I811T: Safety I_{VCC} current limits for type 2

Revision history

Document version	Date of release	Description of changes
V1.0	2018-05-17	1st release

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