40W isolated PFC Flyback converter based on the IRS2505L IRuFB1

Authors: Akos Hodany, Peter B. Green

About this document

Scope and purpose

The purpose of this document is to provide a comprehensive functional description and guide to using the IRuFB1 voltage regulated PFC flyback converter evaluation board based on the IRS2505L. The scope describes the operation of the converter and covers technical aspects that should be considered in the design process, including calculation of external component values, MOSFET selection, PCB layout optimization as well as additional circuitry that may be added if needed in certain cases. Test results and waveforms are included.

Intended audience

Power supply design engineers, applications engineers, students.

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1 Introduction

The IRuFB1 40W Isolated Flyback PFC design is presented in this document. This power supply circuit provides power factor correction (PFC), output voltage regulation and full protection against over-current/short-circuit and over-voltage conditions. Schematic, BOM, PCB layout example are included in this application note as well as a detailed design aid for circuit dimensioning. The circuit comprises a one-stage isolated Flyback AC/DC converter operating in Critical Conduction Mode (CrCM), controlled by the IRS2505L PFC control IC**Error! Reference source not found.**, providing high power efficiency, compact size, low cost and excellent power factor and line current THD figures.

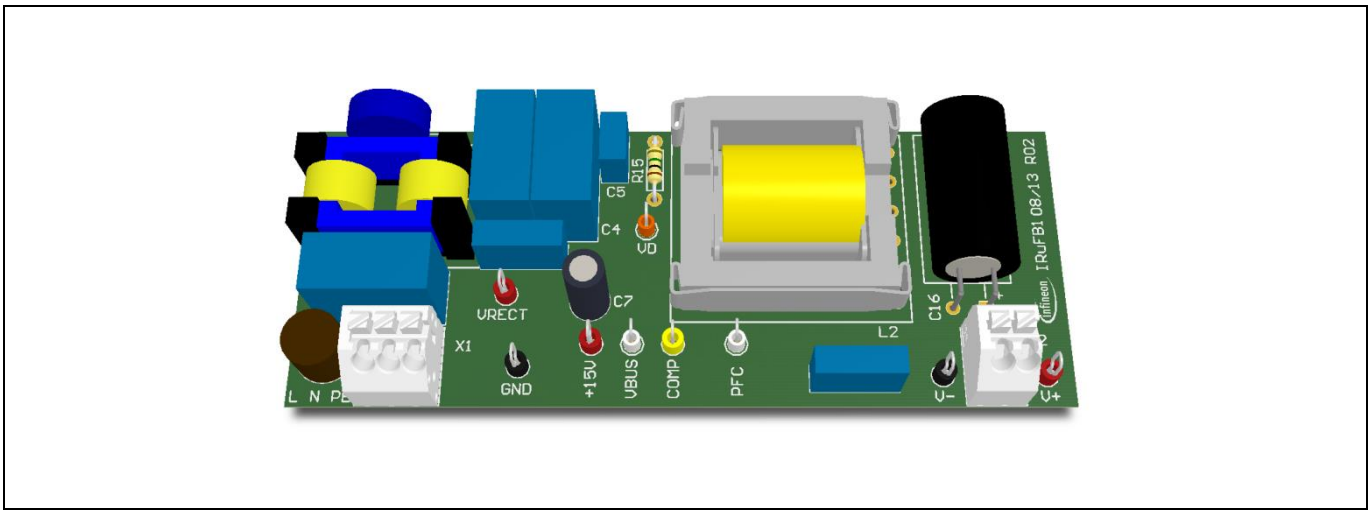


Figure 1 IRuFB1 CV PFC Flyback evaluation board

Safety Warning

The presented circuit operates from the AC line voltage. The maximum on-board DC voltage may be as high as 600V. However, the output provides galvanic isolation from the line voltage; an **electrical shock hazard** exists at any time when operating the circuit. The IRuFB1 demo circuit should be handled by qualified electrical engineers only! Note that the flyback transformer used provides only functional isolation.

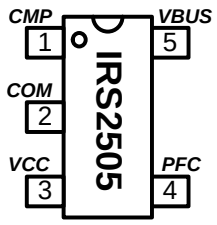
Disclaimer

The IRuFB1 40W Isolated Flyback PFC reference design board is intended for evaluation purposes only and has not been submitted or approved by any external test house for conformance with UL or international safety or performance standards. Infineon Technologies does not guarantee that this design will conform to any such standards.

2 IRS2505L functional overview

The IRS2505L is a control IC intended primarily PFC boost pre-converters operating in critical-conduction mode, but able to also operate in certain Buck and flyback applications. The IC incorporates a voltage feedback loop for output voltage regulation combined with smart zero crossing detection to control the gate drive output without the need for an additional inductor winding. DC output over-voltage protection and cycle-by-cycle over-current protection are also included.

The IRS2505L uses an SOT23-5 package as shown below:



Pin	Name	Description
1	*CMP*	High Voltage Start-up Input
2	*COM*	Feedback Input
3	*VCC*	Compensation and averaging capacitor input
4	*PFC*	Zero-Crossing & Over-Voltage Detection input
5	*VBUS*	Current Sensing Input

Figure 2 IRS2982S pin assignments

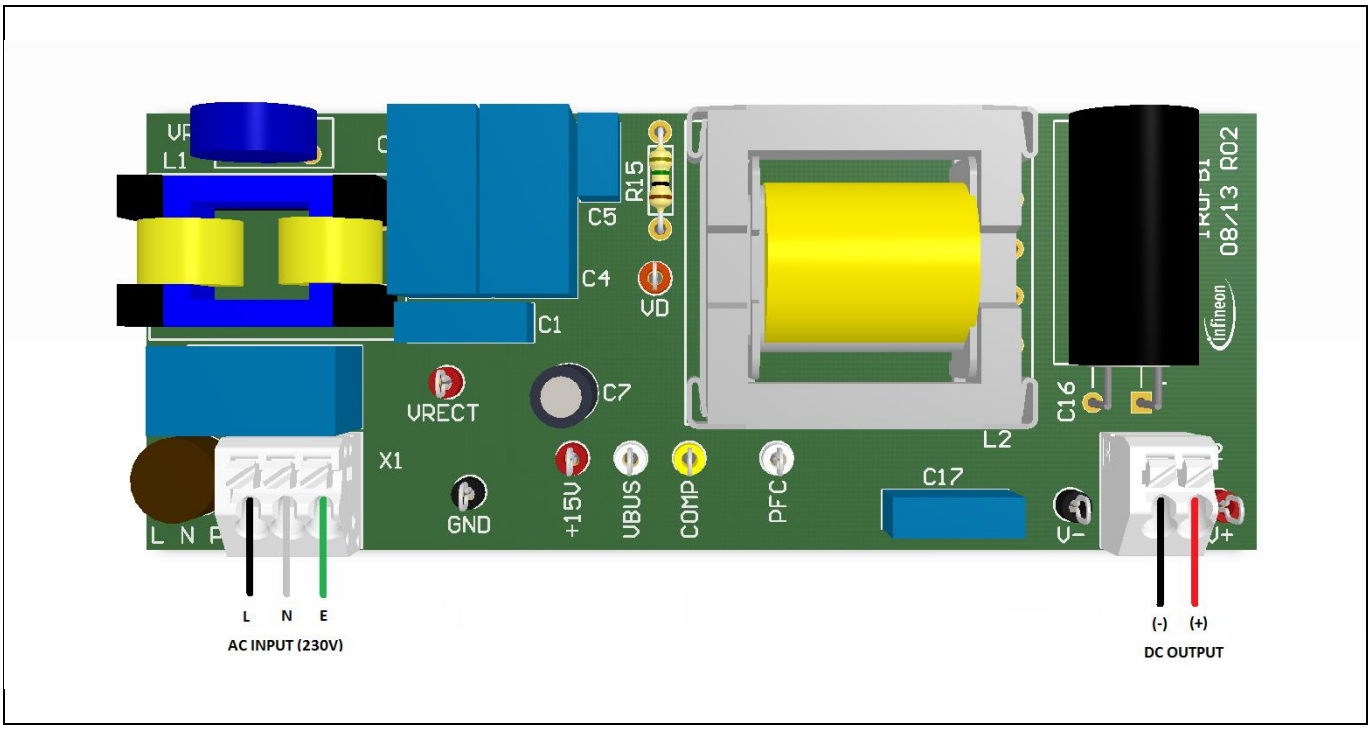


Figure 3 IRuFB1 Connection Diagram

3 Flyback converter IRuFB1

3.1 Flyback converter types

There are several configurations of Flyback converter that may be used with the IRS2505L depending on the application. These can be classified according to isolation and regulation requirements as follows:

1. Isolated or non-isolated,
2. Current or voltage regulation,
   In the case of voltage regulation current limiting is needed for protection against overload or short circuit and in the case of current regulation over-voltage protection is necessary for an open-circuit.

The IRS2505L can operate in any of the four combinations of (1) and (2). Extremely accurate voltage regulation is possible in non-isolated converters since direct feedback to the VBUS input is possible. Isolation is however required in the majority of Flyback converters. For isolated constant current regulation an opto-isolator is necessary; for isolated constant voltage regulation feedback may be taken from an auxiliary winding with a small loss of line and load regulation accuracy. An opto-isolator is also necessary for highly accurate voltage regulation.

3.2 Evaluation board specifications

Input and output at normal operation:

- AC Input voltage 195 VAC up to 265 VAC (55 to 65 Hz)
- Output voltage 50VDC +/- 5% (10% to 100% of rated maximum load)
- Maximum output current 800mA
- Maximum output continuous power 40 W
- PF >0.95 at maximum load, 195 to 265 VAC input voltage
- THD <10% at maximum load, 195 to 265 VAC input voltage
- Efficiency >90% at maximum load at 230 VAC input voltage.
- Startup time to reach the secondary nominal output voltage during full load condition and 230 VAC input voltage <1s.

Protection features

- Primary output over-voltage protection @ VOUT <= 65 VDC
- Cycle by cycle primary over-current protection
- Output short circuit protection (hiccup mode)
- High AC line input protection

No load operation

- Burst mode during no load condition.
- Max power losses during no load condition ≤500mW @230VAC input voltage

Max component temperature

During worst case scenario (ambient temperature 60 °C) the max allowed component temperature is:

- Resistor < 105 °C
- Ceramic capacity, film capacity and electrolyte capacity <85 °C
- Flyback Transformer and chokes <105 °C
- MOSFET, transistor and diodes <110 °C
- IC <100 °C

Dimensions of evaluation board

- Max width 1.77” (45.0 mm), max length 4.51” (114.5 mm).

WARNING!

Output is not isolated! Risk of electric shock! The board should be used only by qualified engineers and technicians.

3.3 Circuit description

The IRuFB1 reference design circuit consists of an EMI filter, a bridge rectifier and a flyback power stage driven by the IRS2505L control IC (*Figure 1*), which provides output voltage regulation and active power factor correction (PFC).

The converter operates in Critical Conduction Mode (CrCM). The high-voltage startup is implemented with the *R17-R18* resistors, while the control circuitry is supplied from the auxiliary winding of the flyback transformer in steady-state operation. This winding also serves as voltage feedback for output voltage regulation. An additional small charge pump (*C8-D3*) is also included to provide additional VCC current.

This also improves output voltage regulation by limiting the load applied to the 15V feedback voltage at C7, which provides better tracking between this feedback voltage and the output voltage.

The IRS2505L includes a novel zero-crossing detection (ZX) circuit for CrCM operation [1] optimized for boost power stages. This ZX solution requires a capacitive coupling from the drain of the power MOSFET to the *PFC* pin. In the flyback converter, it is necessary to add the shown trigger circuitry in order to implement a robust ZX triggering even in output short circuit condition and avoid false triggering due to drain voltage ringing. The *D2-Q1-D4* circuit serves as gate decoupling, while the trigger circuit constructed around *Q2* provides a clean and consistent ZX signal from the auxiliary winding of the flyback transformer.

ZX sensing through the drain of T1 as done in IRS2505L based PFC circuits is also possible, however the drain voltage ringing that occurs at MOSFET switch off can cause false triggering under some line/load conditions. For more basic low cost designs this may be an acceptable solution.

The *D1-C5-R13-R14* snubber limits the peak voltage of the drain spikes caused by the leakage inductance of the flyback transformer.

The overcurrent detection of the IRS2505L requires an AC-coupled current signal, superimposed on the *VBUS* voltage feedback signal. The current signal is fed by *C9-R7* from the shunt resistors to the *VBUS* node. The IRuFB1 can tolerate a short circuit at the output, which causes it to enter hiccup mode where VCC will drop below the IRS2505L under-voltage lockout negative threshold and then C7 re-charges through R17 and R18 to determine the re-start time.

The last included function is a line input current THD improvement circuit. The *R1-R2-R3-R4* voltage divider feeds a portion of the rectified line voltage to the error amplifier output signal (*COMP*), thus it reduces the applied on time of the PWM signal. This results in a reduced harmonic content over the operating range.

D4 provides high AC line shutdown to prevent damage to the MOSFET T1 due to excessive drain voltage in the event of an abnormal high line voltage appearing at the input.

4 Schematic

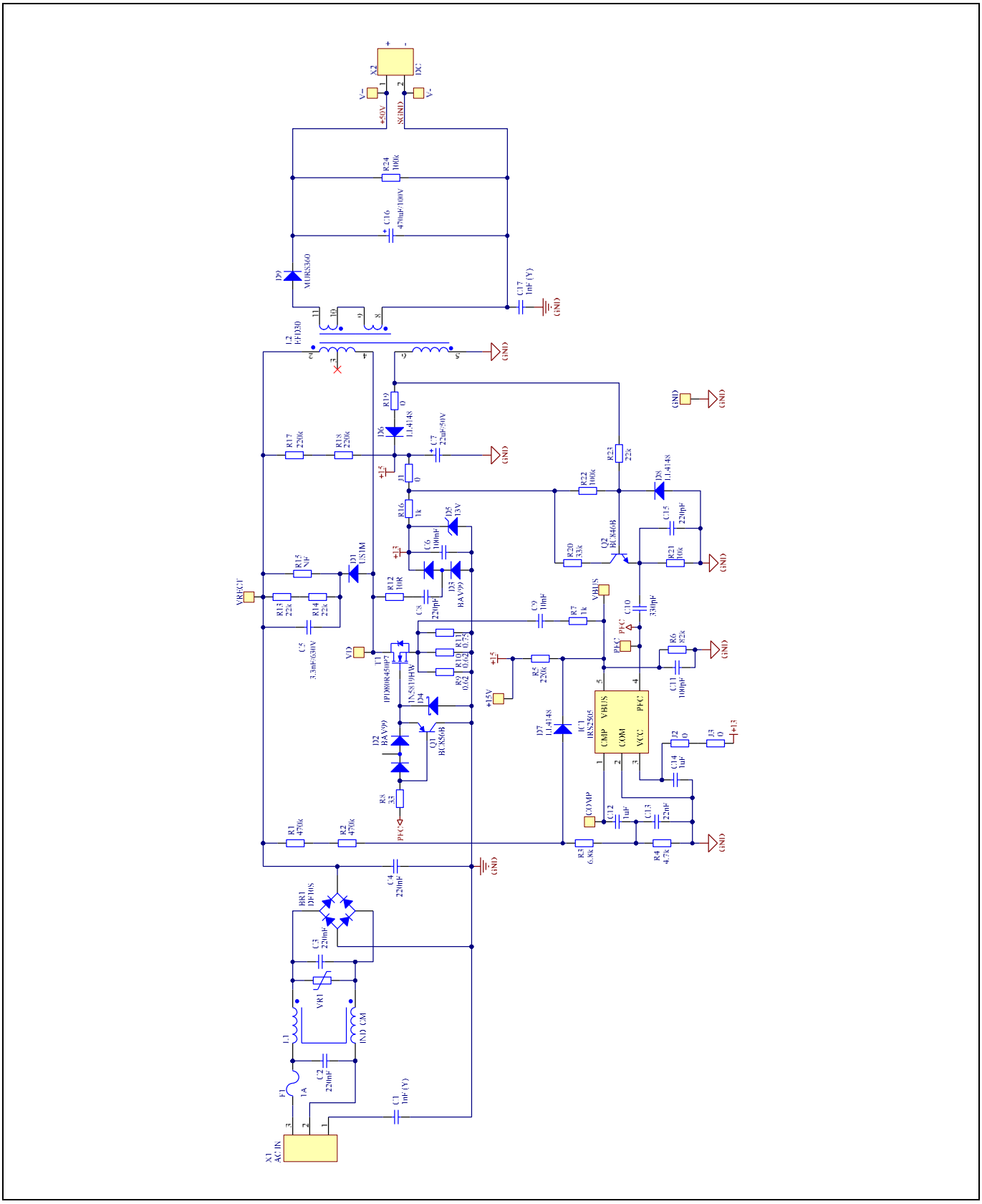


Figure 4 IRuFB1 40W CV PFC Flyback schematic

5 Dimensioning

5.1 Flyback inductor

Define the total output power for the Flyback:

$$P_{OUT,FLY} = P_{OUT} + P_{AUX} = 40W + 15V \cdot 0.1A = 41.5W \quad [1]$$

Where, P_{AUX} represents the load from the auxiliary VCC supply winding. Now approximate the input power with the expected power efficiency:

$$P_{in} = \frac{P_{out}}{\eta} = \frac{41.5W}{0.9} = 46.1W \quad [2]$$

Define the desired duty cycle and the minimum switching frequency at the peak of the sinusoid line voltage ($\theta = 90°$):

$D_{MAX} = 0.25$

$f_{MIN} = 50kHz$

The maximum on-time can be defined as:

$$T_{ON,MAX} = \frac{D_{MAX}}{f_{MIN}} = \frac{0.25}{50kHz} = 5\mu s \quad [3]$$

Calculate the maximum primary inductance:

$$L_{PRI} \le \frac{V_{IN,MIN}^2 T_{ON,MAX} D_{MAX}}{2P_{IN}} = \frac{195V^2 \cdot 5\mu s \cdot 0.25}{92.2W} = 516\mu H \quad [4]$$

Round down the result to 500µH.

Determine the transformer turns ratio:

$$n = \frac{N_P}{N_S} = \frac{\sqrt{2} \cdot V_{IN,MIN}}{V_{OUT} + V_F} \cdot \frac{D_{MAX}}{1 - D_{MAX}} = \frac{\sqrt{2} \cdot 195V}{50V + 1V} \cdot \frac{0.25}{1 - 0.25} = 1.8 \quad [5]$$

In order to achieve good regulation, very tight coupling is required between the windings. The primary leakage inductance must therefore be very low. The transformer used is wound specially for low leakage.

Where $V_F = 1V$ is the forward voltage of the rectifier diode in the secondary side, recalculate the maximum on-time:

$$T_{ON,MAX} = \frac{2L_{PRI} P_{IN}}{V_{IN,MIN}^2 D_{MAX}} = \frac{2 \cdot 500\mu H \cdot 46.1W}{(195V)^2 \cdot 0.25} = 4.849\mu s \quad [6]$$

Dimensioning

Check the maximum V_{DS} voltage required for the flyback MOSFET. The maximum voltage reflected from the secondary (consider $V_{OUT,\,MAX} = 1.2.V_{OUT}$ in no-load condition):

$$V_{REFL,MAX} = n \cdot V_{OUT,MAX} = 1.8 \cdot 60V = 108V \quad [7]$$

The maximum drain-source voltage is:

$$V_{DS,MAX} = \sqrt{2}V_{IN,MAX} + V_{REFL,MAX} + V_{PEAK} \quad [8]$$

Where: V_{PEAK} is the peak voltage of the ringing caused by the secondary leakage inductance and the parasitic capacitances, occurring at the beginning of the off-time. Note that V_{PEAK} must be limited by the snubber circuit; *D_1, C_5, R_{13}, R_{14}*. By assuming $V_{PEAK} \approx 100V$ maximum peak voltage:

$$V_{DS,MAX} \approx \sqrt{2} \cdot 265V + 108V + 100V \approx 580V \quad [9]$$

A MOSFET with 650V rating could therefore be used at the given maximum line voltage, however a MOSFET with higher breakdown voltage rating of 800V improves the reliability of the circuit by preventing avalanching from occurring due to high voltage drain transients present at switch off. This also improves robustness under line surge conditions. The exact value of V_{PEAK} can only be verified by measurements and the snubber must be optimized in order to limit the switch off transient voltage to alevel below the MOSFET breakdown voltage at high line condition.

Determine the primary peak current:

$$I_{PK,PRI} = \frac{\sqrt{2} \cdot V_{IN,MIN}}{L_{PRI}} T_{ON,MAX} = \frac{\sqrt{2} \cdot 195}{500\mu H} 4.849\mu s = 2.674A \quad [10]$$

Calculate the minimum number of turns for the primary:

$$N_{PRI} \geq \frac{L_{PRI} \cdot \Delta I_{MAX}}{A_e \cdot \Delta B_{MAX}} \quad [11]$$

Where: $\Delta I_{MAX} = I_{PK,\,PRI}$ is the peak magnetizing current, ΔB_{MAX} is the maximum flux density and A_e is the effective core area.

An EFD 30/15/9 core is selected:

$A_e = 69mm2$ and $A_L = 2050nH$ for N87 material

The minimum number of turns is given by:

$$N_{PRI} \geq \frac{L_{PRI} \cdot \Delta I_{MAX}}{A_e \cdot \Delta B_{MAX}} = \frac{500\mu H \cdot 2.674A}{69mm^2 \cdot 0.35T} = 55.36 \quad [12]$$

Rounding up the turns (preferably, select a multiple of 2 in order to split the primary in two equal parts later) $N_{PRI} = 60$.

For the secondary the result becomes:

$$N_{SEC} = \frac{N_{PRI}}{n} = \frac{60}{1.8} \cong 33 \quad [13]$$

Determine the effective current through the primary (note: worst-case at D_{MAX}):

$$I_{RMS,PRI,MAX} = I_{PK,PRI}\sqrt{\frac{D_{MAX}}{3}} = 2.674A \cdot \sqrt{\frac{0.25}{3}} = 0.772A \quad [14]$$

Since this effective current is a worst-case value at D_{MAX} ($\theta = 90°$), estimating the effective current over the line period with $0.7.I_{RMS,\,PRI,\,MAX}$.

Calculate primary copper wire cross-section with $J_{MAX} = 6A/mm^2$ maximum current density:

$$A_{CU,PRI} \geq \frac{0.7 \cdot I_{RMS,PRI,MAX}}{J_{MAX}} = \frac{0.7 \cdot 0.772A}{6A/mm^2} = 0.09mm^2 \quad [15]$$

Using a multi-strand wire with d = 0.1mm diameter, the copper cross section of 1 wire:

$$A_{WIRE} = \frac{d^2\pi}{4} = \frac{(0.1mm)^2\pi}{4} = 7.85 \cdot 10^{-3} mm^2 \quad [16]$$

Number of strands necessary:

$$S_{PRI} = \frac{A_{CU,PRI}}{A_{WIRE}} = \frac{0.09mm^2}{7.85 \cdot 10^{-3} mm^2} \cong 11 \quad [17]$$

With some compromise, 10 x 0.1mm multi-strand wire is acceptable for the primary winding. The peak secondary current (note: worst-case at D_{MAX}):

$$I_{PK,SEC} = 2 \cdot \frac{2I_{OUT}}{1 - D_{MAX}} = 2 \cdot \frac{2 \cdot 0.8A}{1 - 0.25} = 4.267A \quad [18]$$

Determine the maximum effective current through the secondary (note: worst-case at D_{MAX}):

$$I_{RMS,SEC,MAX} = I_{PK,SEC}\sqrt{\frac{1 - D_{MAX}}{3}} = 4.267A \cdot \sqrt{\frac{1 - 0.25}{3}} = 2.134A \quad [19]$$

Calculate secondary copper wire cross-section with $J_{MAX} = 6A/mm^2$ maximum current density:

$$A_{COPPER,SEC} \geq \frac{0.7 \cdot I_{RMS,SEC,MAX}}{J_{MAX}} = \frac{0.7 \cdot 2.134A}{6A/mm^2} = 0.249mm^2 \quad [20]$$

Use a multi-strand wire with d = 0.1mm diameter. The copper cross section of 1 wire as described in [16]. Number of strands necessary for the secondary:

$$S_{SEC} = \frac{A_{COPPER,SEC}}{A_{WIRE}} = \frac{0.178mm^2}{7.85 \cdot 10^{-3} mm^2} \cong 32 \quad [21]$$

Therefore, a 30 x 0.1mm multi-strand wire can be used for the secondary winding.

The window area of the selected core is relatively small, so it may be necessary to reduce the number of wires in the primary and/or in the secondary multi-strands. A ~10% reduction of the strand number is in most cases still acceptable. Consider copper losses carefully.

Calculate the number of turns for the auxiliary winding so that it provides ~15V at the nominal output voltage:

$$N_{AUX} = N_{SEC} \frac{V_{AUX} + V_{FW}}{V_{OUT,MIN} + V_{FW}} = 33 \cdot \frac{15+1}{50+1} = 10.3 \cong 10 \quad [22]$$

5.2 Over current limit

Define a current limit margin as follows: CLM = 10%.

The primary shunt resistor required for the overcurrent detection:

$$R_{SH,PRI} = \frac{V_{BUSOC+}}{(1+CLM) \cdot I_{EQ}} \frac{R_5 \| R_6 + R_7}{R_5 \| R_6} \cong \frac{V_{BUSOC+}}{(1+CLM) \cdot I_{EQ}} \quad [23]$$

Where: $V_{BUSOC+} = 0.56V$ and I_{EQ} is the equivalent sensed current (due to current sense DC decoupling):

$$I_{EQ} = I_{PK,PRI} - I_{SH,AV} = I_{PK,PRI} \left(1 - \frac{D_{MAX}}{2}\right) = 2.674 \cdot \left(1 - \frac{0.25}{2}\right) = 2.34A \quad [24]$$

With the component values given in **Error! Reference source not found.** we get:

$$R_{SH,PRI} = \frac{0.56V}{1.1 \cdot 2.34A} = 0.22\Omega \quad [25]$$

Set shunt resistors so that, $R_{SH,PRI}$ = R9 ‖ R10 ‖ R11:
R9 = R10 = 0.62Ω, R11 = 0.75Ω

5.3 Output voltage regulation

Now set the nominal output voltage by setting the R5/R6 voltage divider fed from the auxiliary voltage. The resulting feedback voltage is:

$$V_{BUS} = V_{AUX} \frac{R_6}{R_6 + R_5} \quad [26]$$

In steady-state, $V_{BUS} = V_{BUSREG} = 4.1V$ as per datasheet. Now set the R5 resistor as follows:

$$R_5 = R_6 \left(\frac{V_{AUX} - V_{BUS}}{V_{BUS}} \right) = 82k\Omega \cdot \left(\frac{15V - 4.1V}{4.1V} \right) \cong 220k\Omega \quad [27]$$

5.4 MOSFET selection

The CoolMOS™ P7 series is the latest CoolMOS™ product family and targets customers looking for high performance and at the same time being price sensitive. Though optimizing key parameters (C_{oss}, E_{oss}, Q_g, C_{iss}, and $V_{GS(th)}$ et al.); integrating Zener Diode for ESD protection and other measures, this product family fully addresses market concerns in performance, ease-of-use, and price/performance ratio, delivering best-in-class performance with exceptional ease-of-use, while still no compromise in price/performance ratio. The 700V and 800V CoolMOS™ P7 series have been designed for flyback and could also be used in PFC topology; they are not recommended for soft switching topologies where hard commutation could happen due to its body diode ruggedness. However, the 600V CoolMOS™ P7 could be used in both soft and hard switching topologies including PFC, flyback, LLC, and TTF.

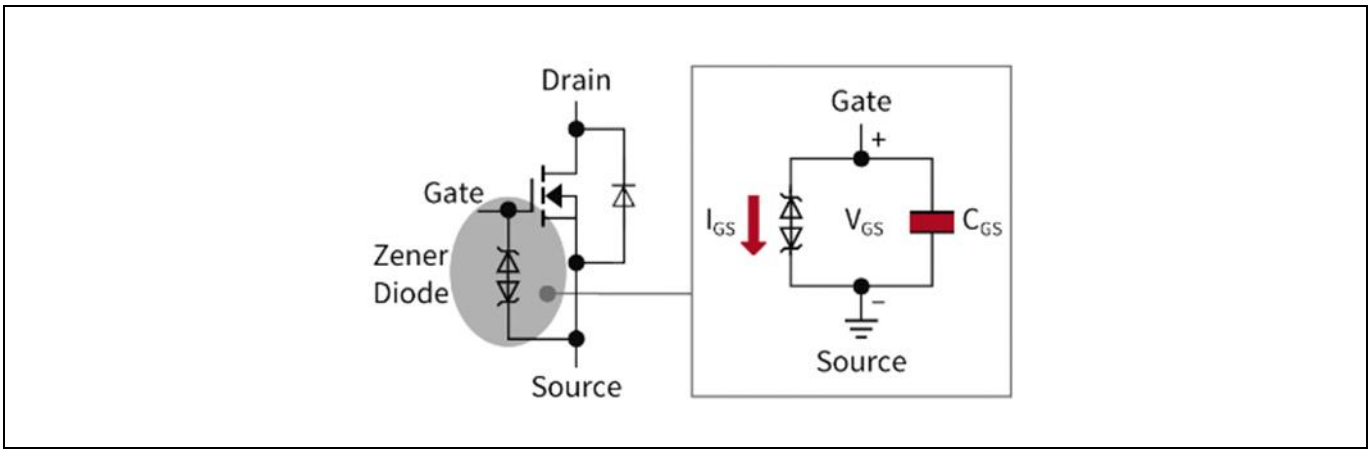


Figure 5 Switching MOSFET parasitics

The IPD80R450P7 is an 800V device with $R_{DS(ON)}$ of 450mΩ recommended for hard and soft switching boost and flyback topologies for LED lighting, low power chargers and adapters, audio and other low power SMPS applications. At the power level of the IRuFB1 design the DPAK package is sufficient, enabling improved efficiency and higher power density.

6 PCB layout

6.1 Layout considerations

In order to ensure correct circuit functionality and to avoid issues caused by high-frequency signal disturbance, proper care should be taken when designing the PCB layout. Typical design problems due to poor layout can include high-frequency voltage and/or current spikes, poor EMC results, latch up, abnormal circuit behavior, component failures, low manufacturing yields and poor system reliability. The following layout tips should be followed as early in the design phase as possible in order to reduce potential problems of the implemented circuit, shorten design cycles, and to increase reliability and manufacturability:

1. Keep the traces of the switching signals as short as possible (like: drain switching node, output diode node, etc.). This will help to reduce high-frequency ringing and noise coupling due to parasitic inductance of PCB traces.
2. Keep high-frequency switching nodes away from sensitive circuit nodes (like: low voltage control signals). This will help to reduce noise coupling from switching nodes to critical circuit nodes.
3. Place the VCC filter capacitor as close to the control IC pins as possible. This will ensure the best possible filtering.
4. Route separate traces for power and signal grounds and connect the small-signal ground to the power ground at a single point only. Place this star ground connection close to the current sense resistors and minimize the distance from the IC ground pin. This will minimize the cross coupling between power ground and signal ground, providing noise-free current and voltage sense signals for the control IC.
5. Reduce the distance of the power switches to their gate drive pins as much as possible. This will help reduce the parasitic inductance in the traces, thus reduces possible voltage spikes at gate drive switching and help prevent latch up due to voltage over- or under-shoot.
6. Place critical sensing nodes (sensing filters, etc.) as close to the IC as possible. This will help to eliminate false triggering or circuit malfunction due to noise being coupled onto the sensitive control signals.

6.2 Board 3D views

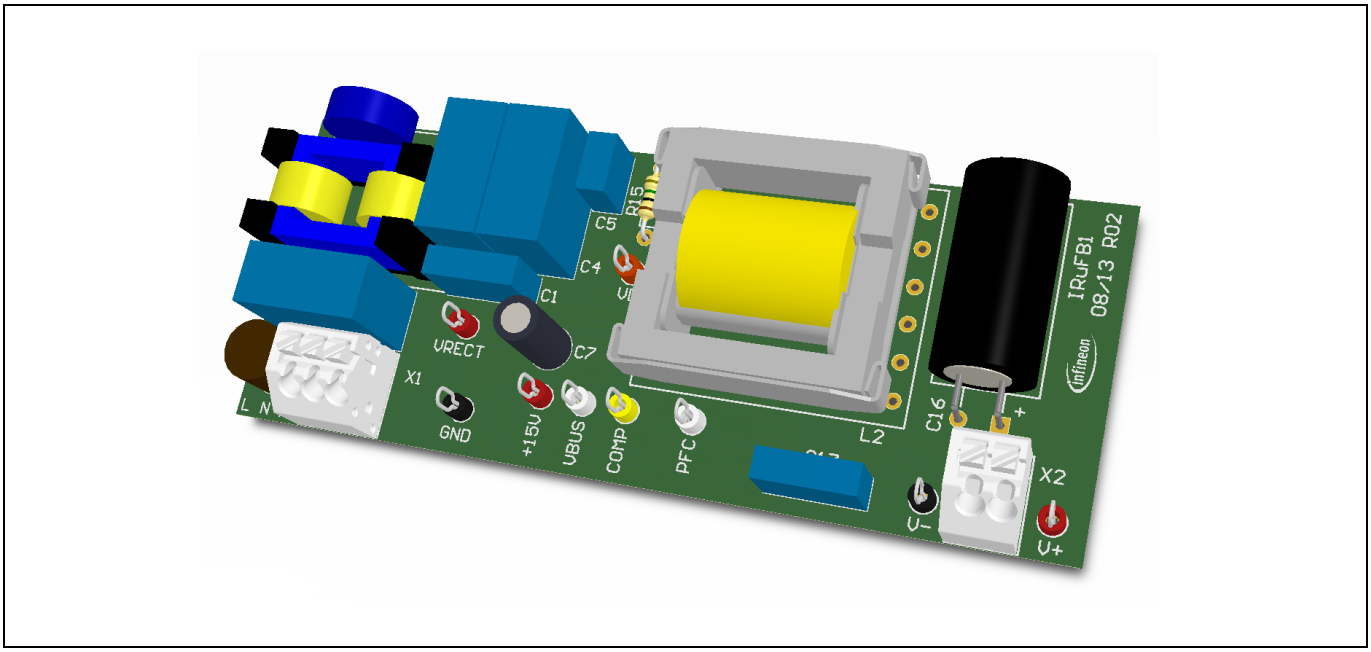


Figure 6 IRuFB1 top side 3D

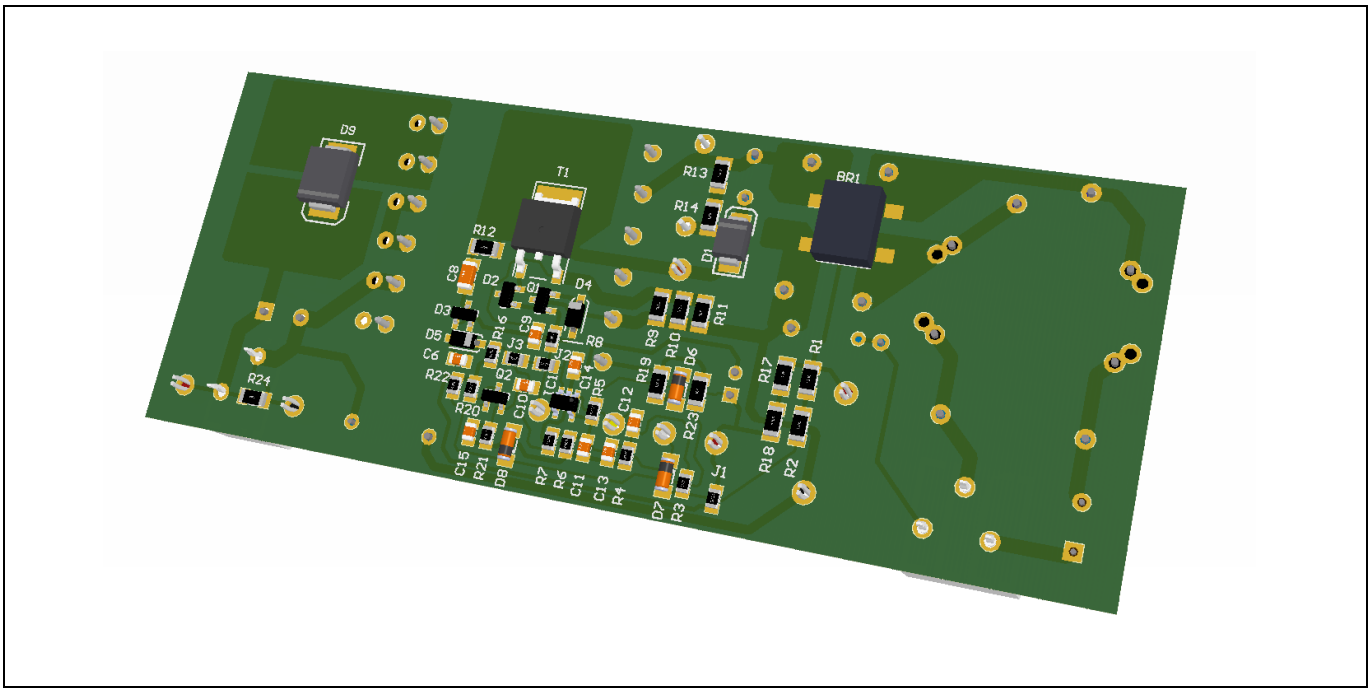


Figure 7 IRuFB1 bottom side 3D

6.3 PCB assembly drawings

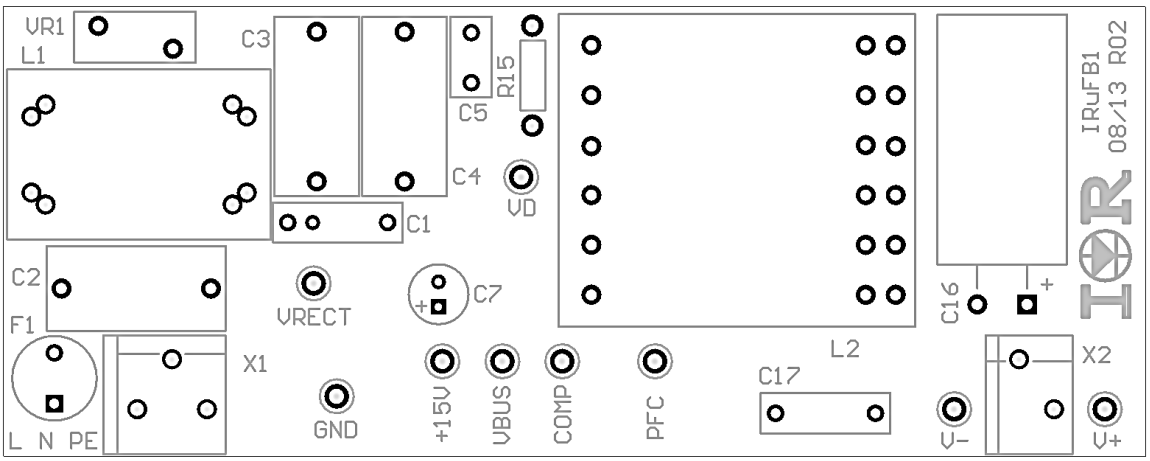


Figure 8 PCB top assembly drawing

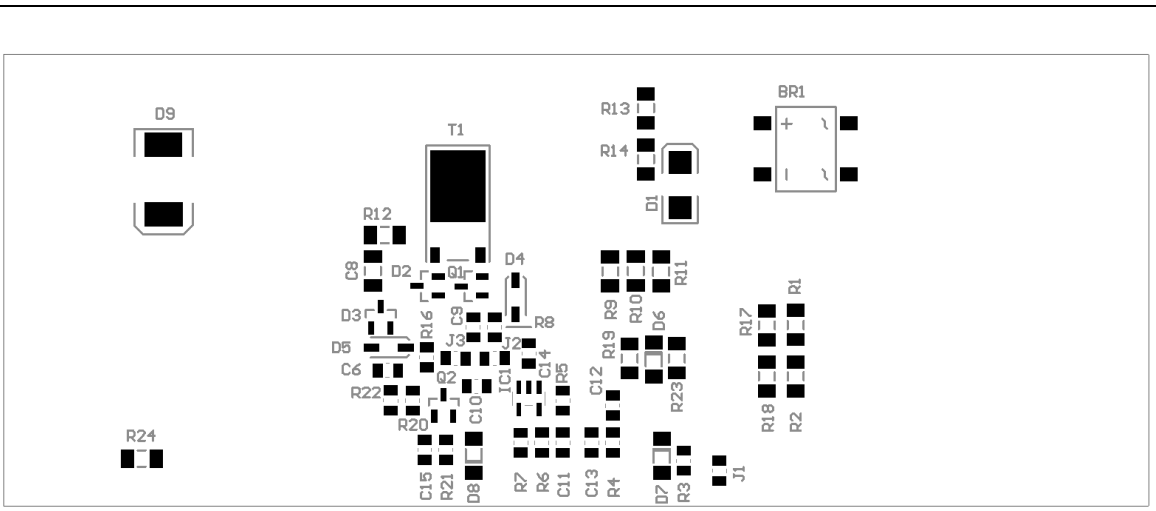


Figure 9 PCB bottom assembly drawing

6.4 PCB bottom layer

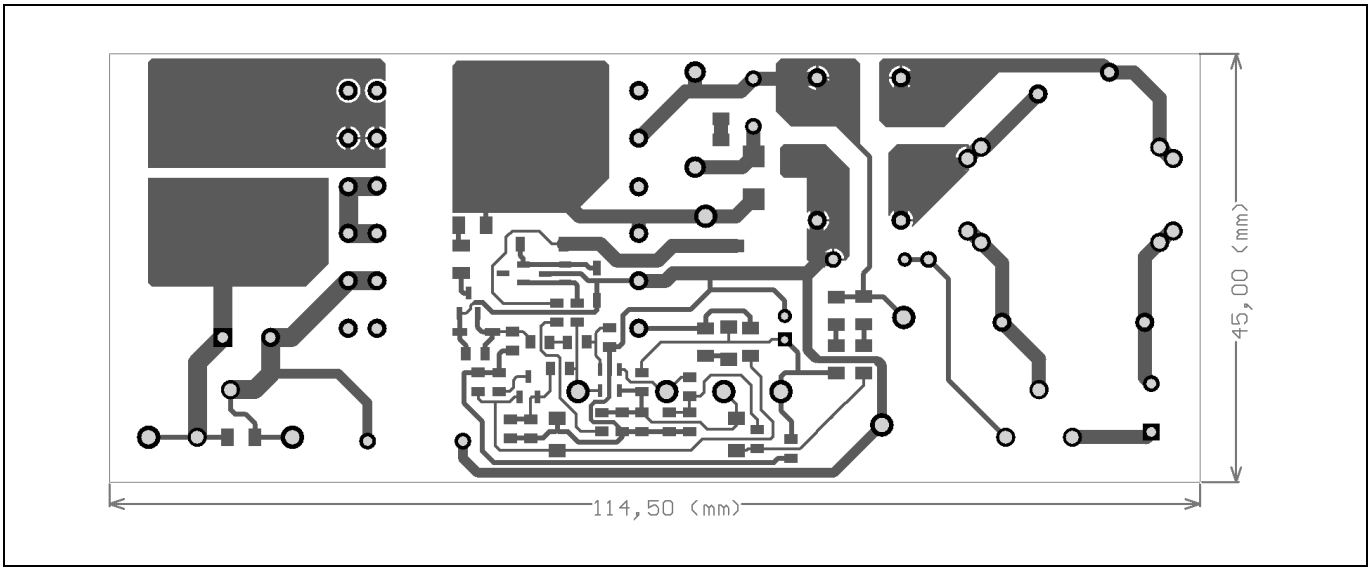


Figure 10 PCB bottom layer

7 Bill of materials

Designator	Manufacturer	Part Number	Quantity	Value/Rating
+15V, V+, VRECT	Keystone Electronics	5000	3	Red
BR1	Diodes Inc	DF10S	1	1000V/1A
C1, C17	Epcos	B32021A3102M	2	1nF/400VAC/Y2
C2, C3, C4	Epcos	B32922C3224M	3	220nF/305VAC/X2
C5	Epcos	MKP2J013301B00KSSD	1	3.3nF/630V/MKP
C6	TDK	C2012X8R1H104K125AA	1	100nF/50V/10%/0805
C7	Panasonic	ECEA1HKA220	1	22uF/50V
C8	TDK	C3216C0G2J221J	1	220pF/630V/1206
C9	TDK	C2012C0G1H103J060AA	1	10nF/50V/5%/0805
C10	TDK	C2012C0G2W331K060AA	1	330pF/450V/10%/0805
C11	TDK	CGJ4C2C0G1H101J060AA	1	100pF/50V/5%/0805
C12, C14	TDK	C2012X7R1H105K085AC	2	1uF/50V/10%/0805
C13	TDK	C2012C0G1E223J125AA	1	22nF/25V/5%/0805
C15	TDK	CGJ4C2C0G1H221J060AA	1	220pF/50V/5%/0805
C16	Panasonic	ECA2AHG471	1	470uF/100V
COMP	Keystone Electronics	5004	1	Yellow
D1	Diodes Inc	US1M	1	1000V/1A/SMB
D2, D3	NXP	BAV99	2	100V/200mA/SOT-23
D4	Diodes Inc	1N5819HW	1	40V/1A/SOD-123
D5	Diodes Inc	BZT52C13	1	13V/500mW/SOD-123
D6, D7, D8	Vishay	LL4148	3	75V/200mA/SOD-80

D9	Vishay	MURS360	1	600V/3A/SMC
F1	Multicomp	MCMET 1A 250V	1	T1A/250V
GND, V-	Keystone Electronics	5001	2	Black
IC1	Infineon	IRS2505L	1	PFC Controller IC, SOT23-5
J1, J2, J3	Panasonic	ERJ-6GEY0R00V	3	0/0805
L1	Epcos	B82732F2701B001	1	2x47mH/0.7A
L2	Precision Inc	019-8510-00R	1	Flyback transformer
PFC, VBUS	Keystone Electronics	5002	2	White
Q1	NXP	BC856B	1	65V/100mA/PNP/SOT-23
Q2	NXP	BC846B	1	65V/100mA/NPN/SOT-23
R1, R2	Panasonic	ERJ8ENF4703V	2	470k/0.25W/1%/1206
R3	Panasonic	ERJ6ENF6801V	1	6.8k/0.125W/1%/0805
R4	Panasonic	ERJ6ENF4701V	1	4k7/0.125W/1%/0805
R5	Panasonic	ERJ6ENF2203V	1	220k/0.125W/1%/0805
R6	Panasonic	ERJ6ENF8202V	1	82k/0.125W/1%/0805
R7, R16	Panasonic	ERJ6ENF1001V	2	1k/0.125W/1%/0805
R8	Panasonic	ERJ6ENF33R0V	1	33/0.125W/1%/0805
R9, R10	Panasonic	ERJ-S8QFR62V	2	0.62/0.25W/1%/1206
R11	Panasonic	ERJ-S8QFR75V	1	0.75/0.25W/1%/1206
R12	Panasonic	ERJ8ENF10R0V	1	10R/0.25W/1%/1206
R13, R14, R23	Panasonic	ERJ8ENF2202V	3	22k/0.25W/1%/1206

R15			1	Not Fitted
R17, R18	Panasonic	ERJ8ENF2203V	2	220k/0.25W/1%/1206
R19	TDK	ERJ-8GEY0R00V	1	0/0.25W/1206
R20	Panasonic	ERJ6ENF3302V	1	33k/0.125W/1%/0805
R21	Panasonic	ERJ6ENF1002V	1	10k/0.125W/1%/0805
R22	Panasonic	ERJ6ENF1003V	1	100k/0.125W/1%/0805
R24	Panasonic	ERJ8ENF1003V	1	100k/0.25W/1%/1206
T1	Infineon	IPD80R450P7	1	800V/11/0.45Ohm/PG-TO252 (DPAK)
VD	Keystone Electronics	5003	1	Orange
VR1	Epcos	S10K320	1	10mm/320VAC
X1	Phoenix Contact	PTSA 1.5/3-3,5-Z	1	Terminal block, 3 position
X2	Phoenix Contact	PTSA 1.5/2-3,5-Z	1	Terminal block, 2 position

8 Transformer specification

Core size	EFD 30/15/9
Core material	Epcos N87 or equivalent
Bobbin	Horizontal
Pins	12
Primary inductance	500µH ±10%
Primary leakage inductance	3uH
Primary peak voltage	600V max.
Maximum core temperature	100ºC
Electrical isolation (primary to secondary and auxiliary to secondary)	3000VAC / 1 min

Winding	Start pin	Finish pin	Turns	Wire
Primary 1.	2	3	30	10x0.1mm
Secondary 1.	8	9	17	30x0.1mm
Primary 2.	3	4	30	10x0.1mm
Secondary 2.	10	11	16	30x0.1mm
Auxiliary	5	6	10	1x0.2mm

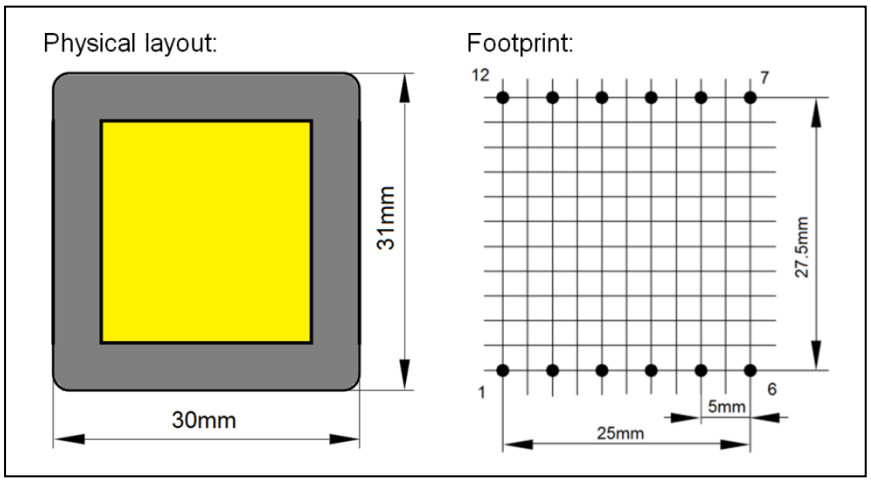


Figure 11 Flyback transformer specification

9 Test results

9.1 Test measurements

Table 1 Input 195 VAC

Load	Pout [W]	Vout [V]	Iout [A]	Pin [W]	η	PF	THD	Voutrp [Vrms]	Voutrp [Vpp]
100%	38.32	48.32	0.793	41.69	91.91%	0.974	5.20%	1.60	4.53
50%	19.25	48.86	0.394	21.64	88.96%	0.912	6.20%	0.80	2.26
20%	7.75	50.63	0.153	9.28	83.47%	0.714	16.40%	0.40	1.13
0	0.00	62.80	0.000	0.36	0.00%			0.03	0.07

Table 2 Input 230 VAC

Load	Pout [W]	Vout [V]	Iout [A]	Pin [W]	η	PF	THD	Voutrp [Vrms]	Voutrp [Vpp]
100%	38.14	48.10	0.793	41.56	91.78%	0.955	5.00%	1.60	4.53
50%	19.60	49.74	0.394	21.91	89.45%	0.863	5.40%	0.80	2.26
20%	7.73	50.54	0.153	9.63	80.30%	0.637	23.00%	0.40	1.13
0	0.00	64.70	0.000	0.50	0.00%			0.03	0.07

Table 3 Input 265 VAC

Load	Pout [W]	Vout [V]	Iout [A]	Pin [W]	η	PF	THD	Voutrp [Vrms]	Voutrp [Vpp]
100%	37.72	47.57	0.793	41.30	91.34%	0.926	5.00%	1.60	4.53
50%	19.42	49.28	0.394	22.08	87.94%	0.801	7.30%	0.80	2.26
20%	7.68	50.20	0.153	9.89	77.66%	0.561	25.70%	0.40	1.13
0	0.00	61.20	0.000	0.55	0.00%			0.03	0.07

9.2 Power factor and distortion

All measurements are made at 60Hz line frequency using an AC electronic load and power analyser.

Measurements made at 50Hz line frequency are not shown here but these do not show a significant difference in results except for a higher output voltage and current ripple.

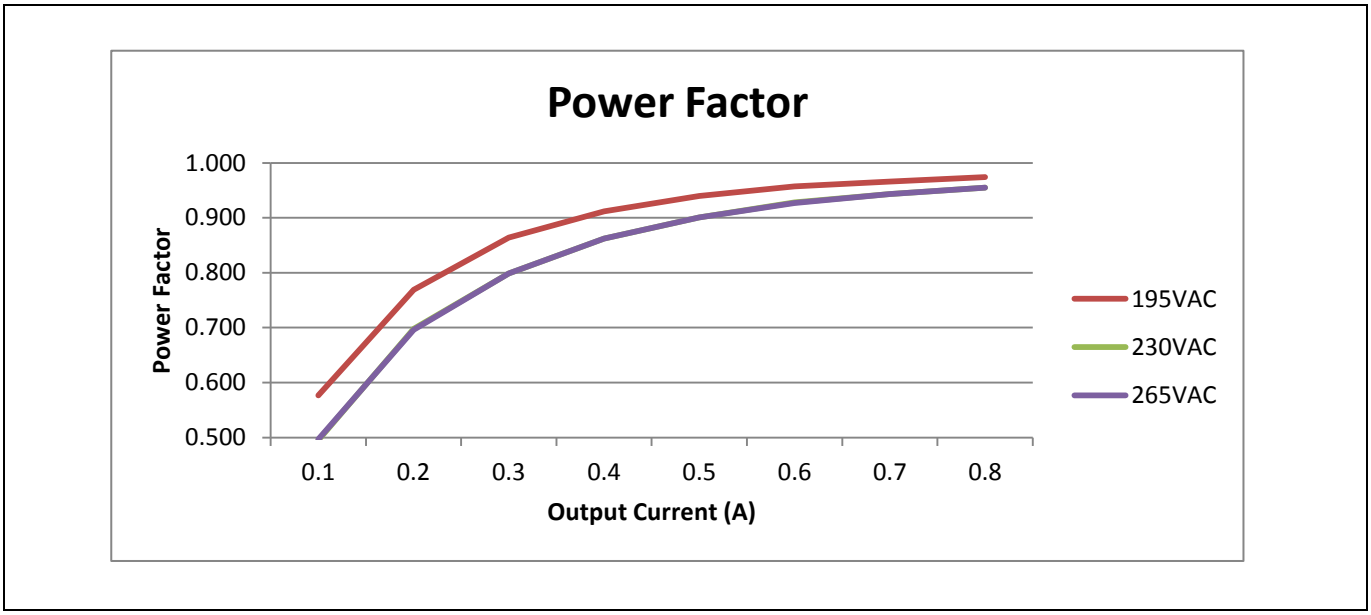


Figure 3 Power factor

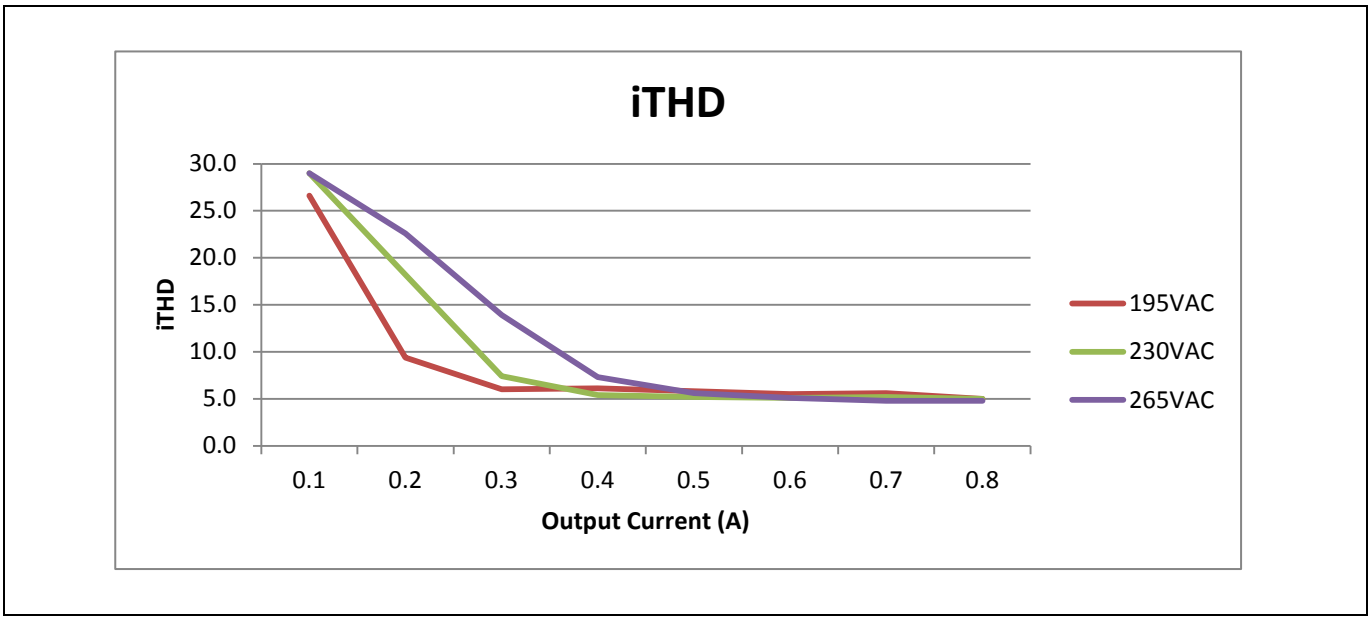


Figure 4 THD of the input current

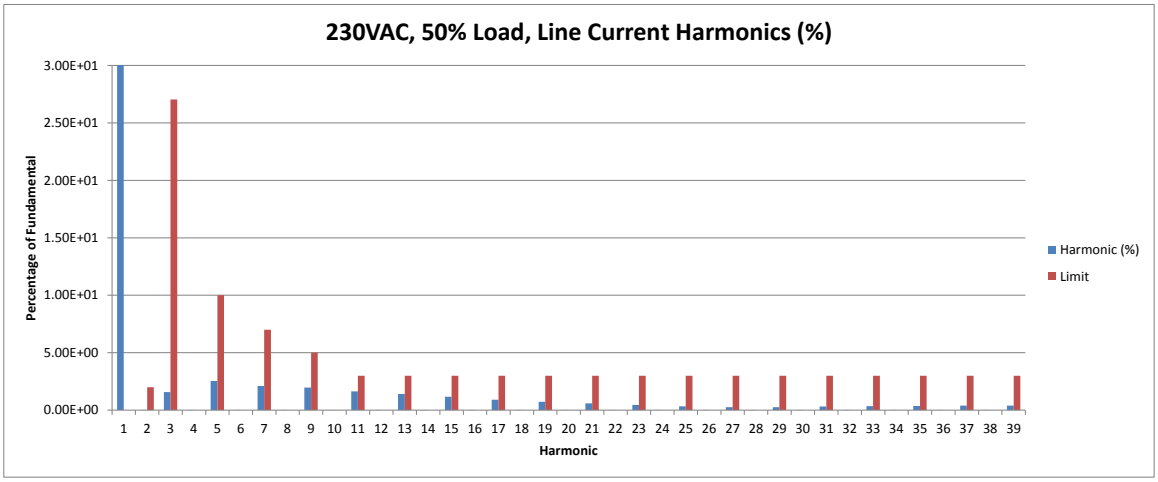


Figure 5 Line input current harmonics at 230V, half load

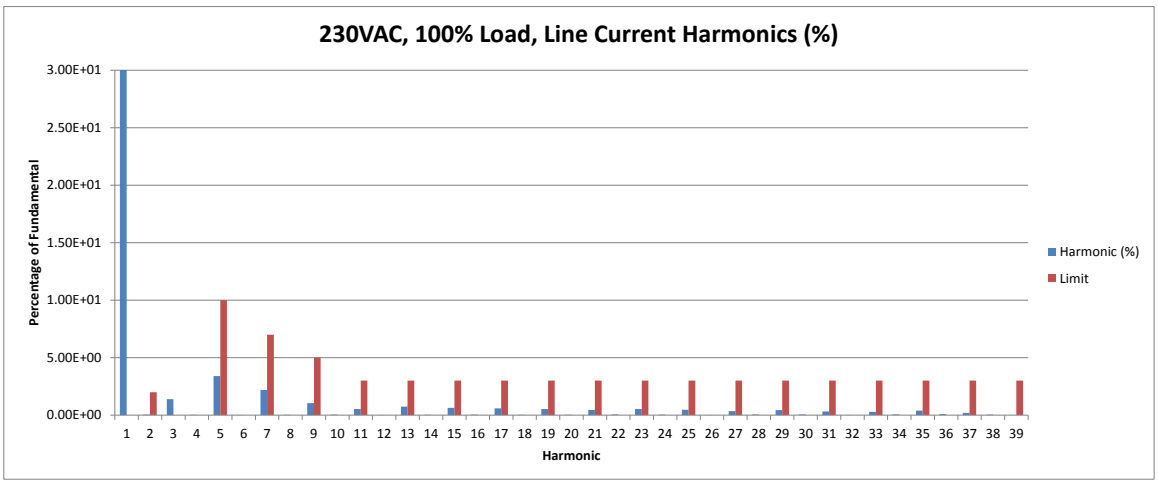


Figure 6 Line input current harmonics at 230V, full load

Table 4 EN61000-3-2 Class C limits for system power >25 W

Requirements	Harmonics Limits Class C according EN 61000-3-2 for System Power > 25W	
	Harmonics order n	Maximum value expressed as a percentage of the fundamental input current
	2	<2%
	3	<30 λ %
	5	10%
	7	<7%
	9	<5%
	11 ≤ n ≤ 39	<3%
		λ = power factor

9.3 Power losses and efficiency

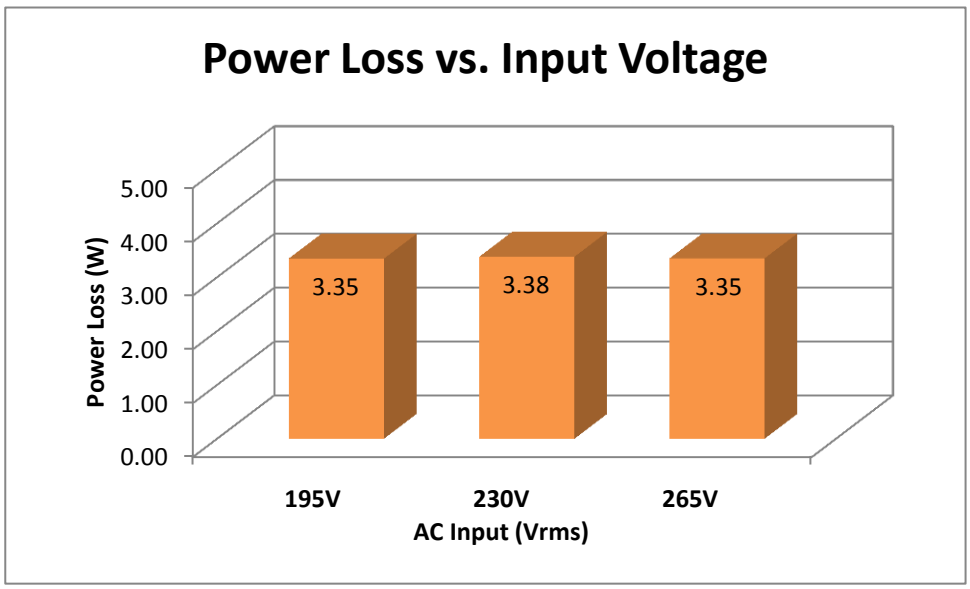


Figure 7 Measured power losses at 230V, full load

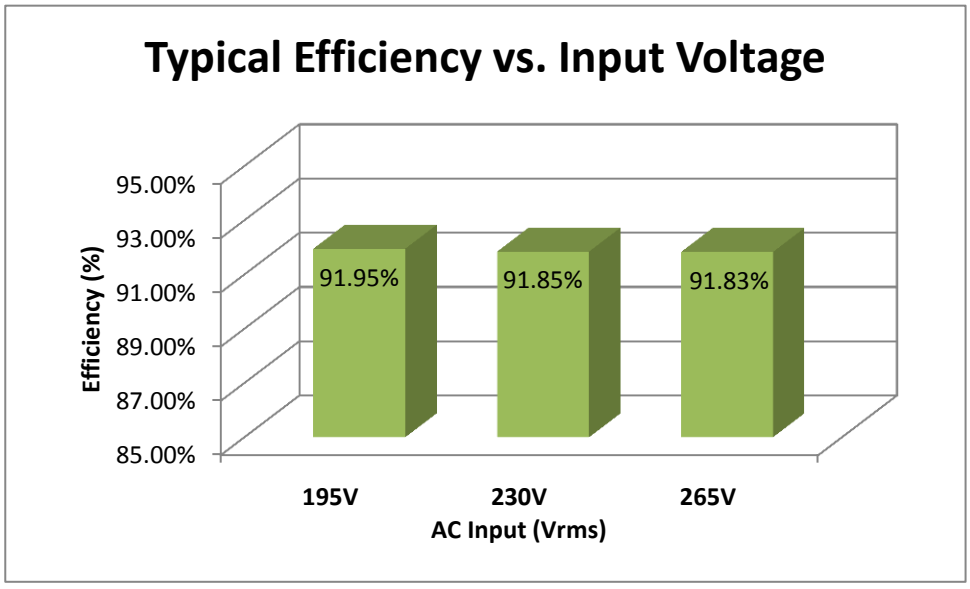


Figure 8 Measured power efficiency at full load

9.4 Line and load regulation

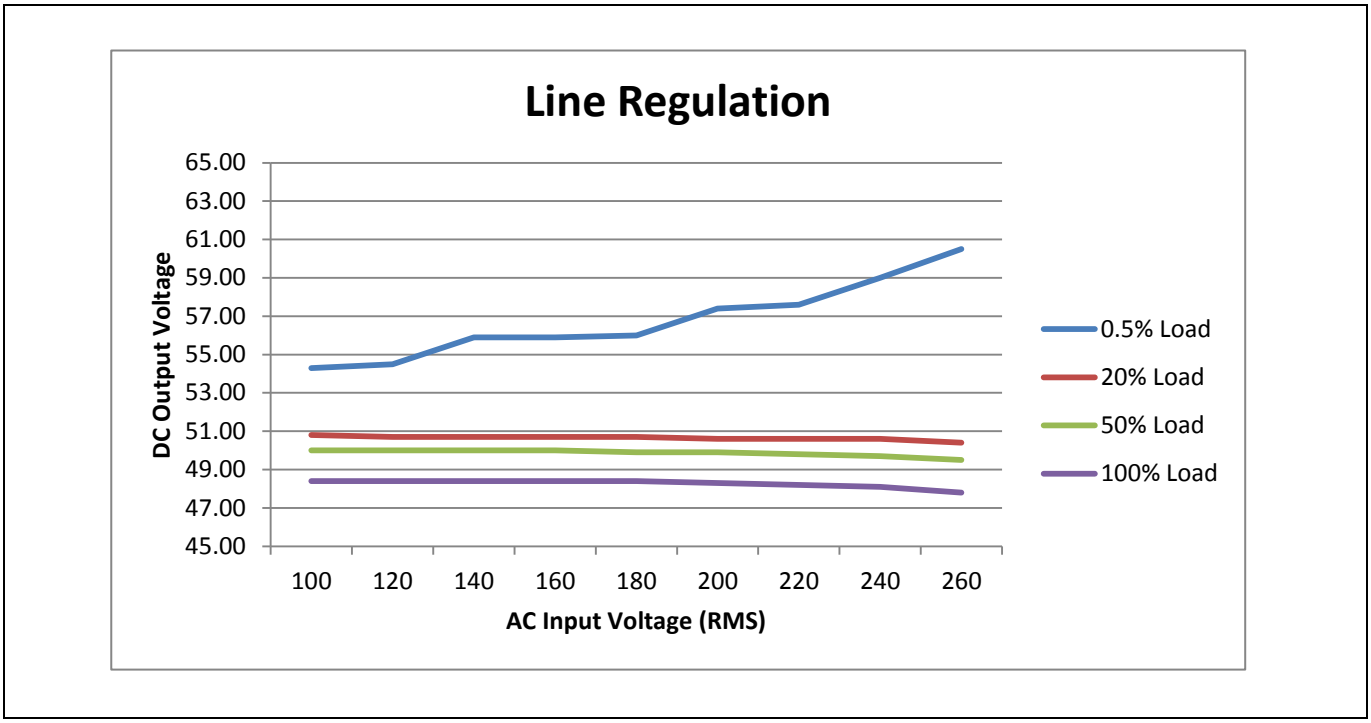


Figure 9 Line regulation

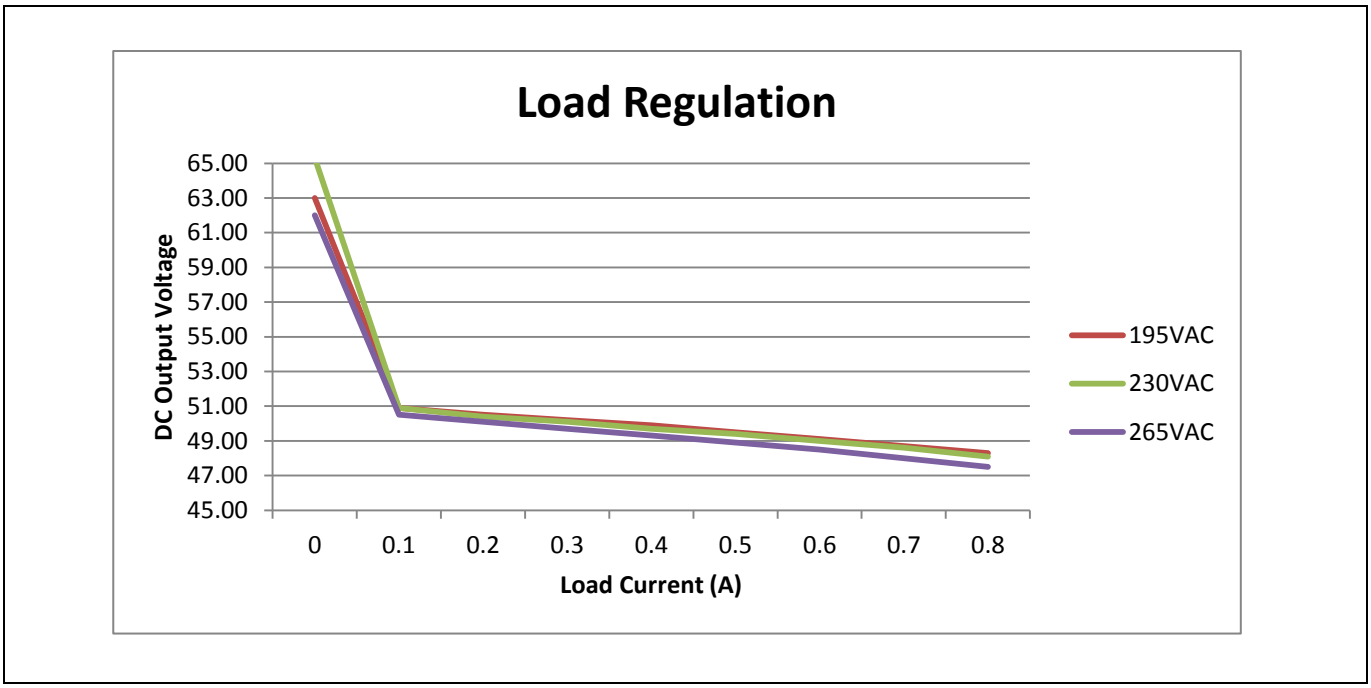


Figure 10 Load regulation

9.5 Operating waveforms

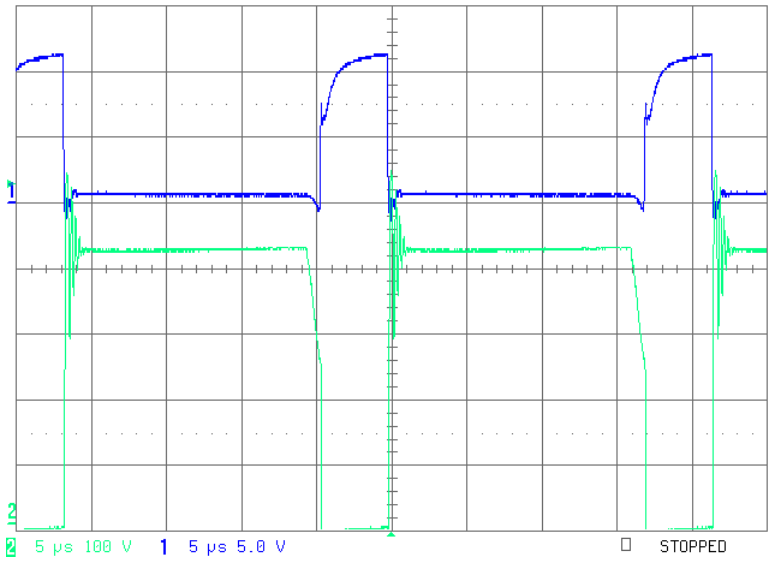


Figure 11 Line peak at 230Vrms, full load
Gate drive (blue), Vdrain (green)

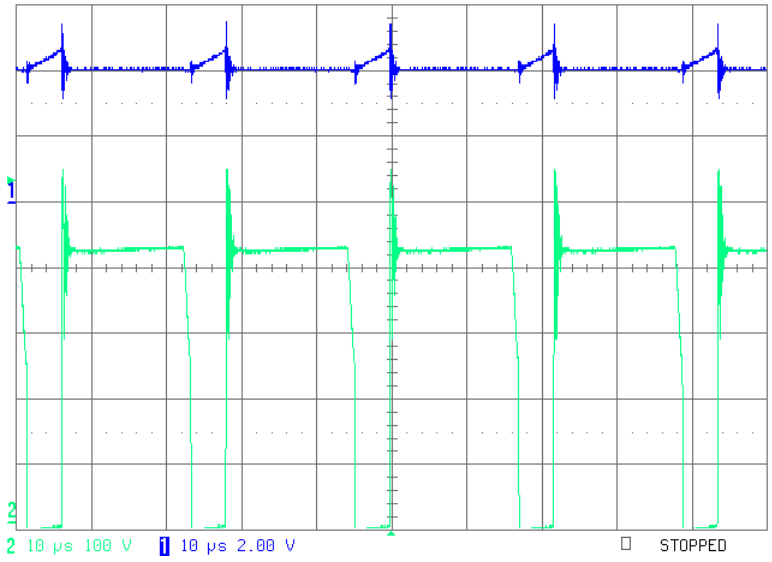


Figure 21 Line peak at 230Vrms, full load
VBUS input (blue), Vdrain (green)

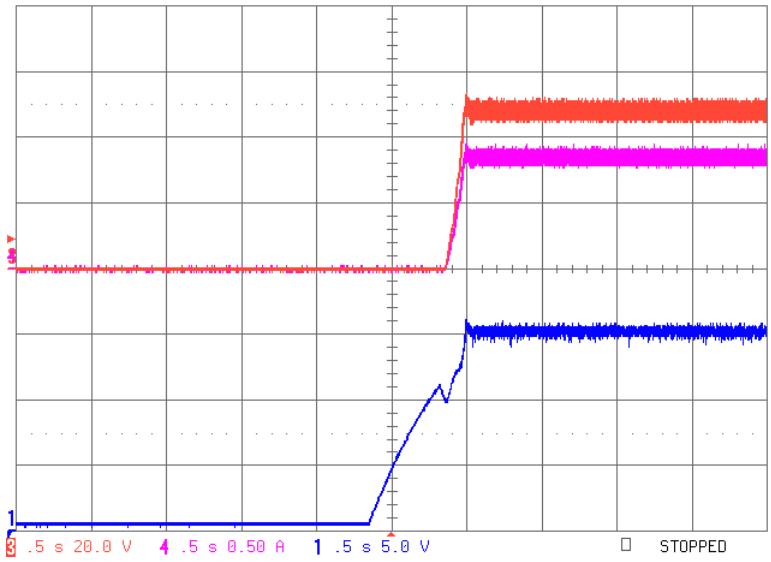


Figure 22 Start-up at 230Vrms, full load
VCC (blue), VOUT (red), IOUT (purple)

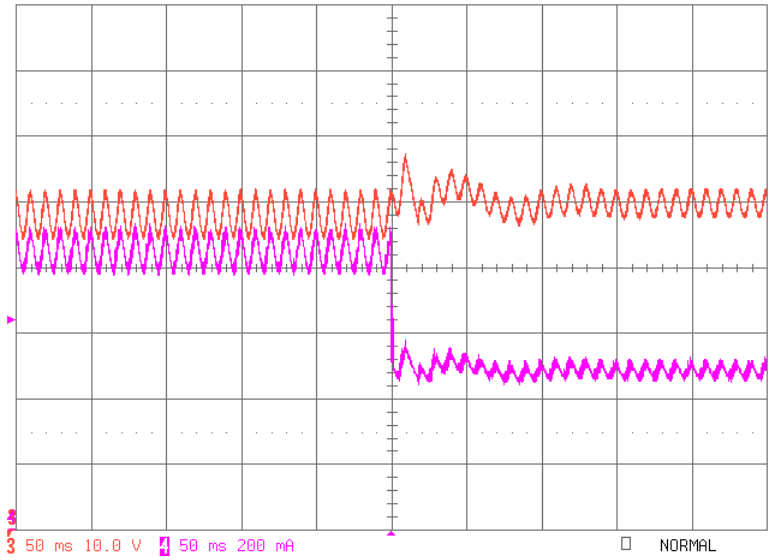


Figure 23 Step reduction in load from 100% to 60%
VOUT (red), IOUT (purple)

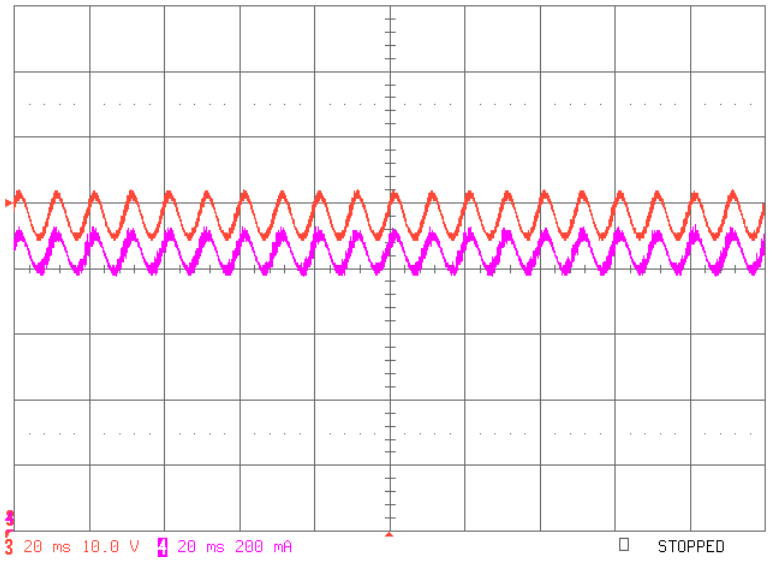


Figure 24 Output ripple at 230Vrms, full load
VOUT (red), IOUT (purple)

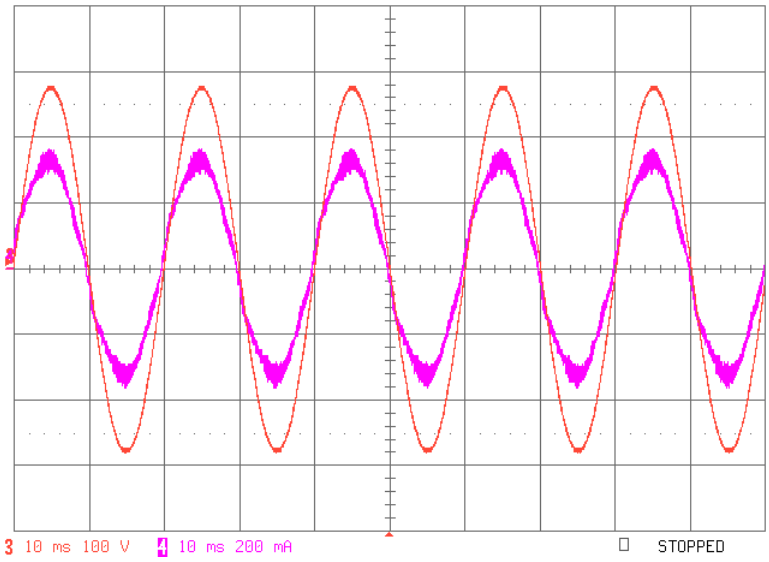


Figure 25 Input voltage and current at 195Vrms, full load
VIN (red), IIN (purple)

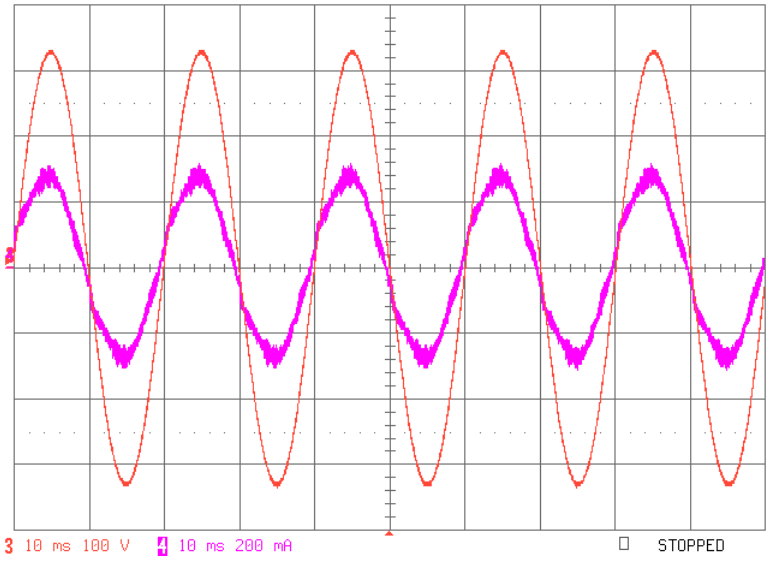


Figure 26 Input voltage and current at 230Vrms, full load
VIN (red), IIN (purple)

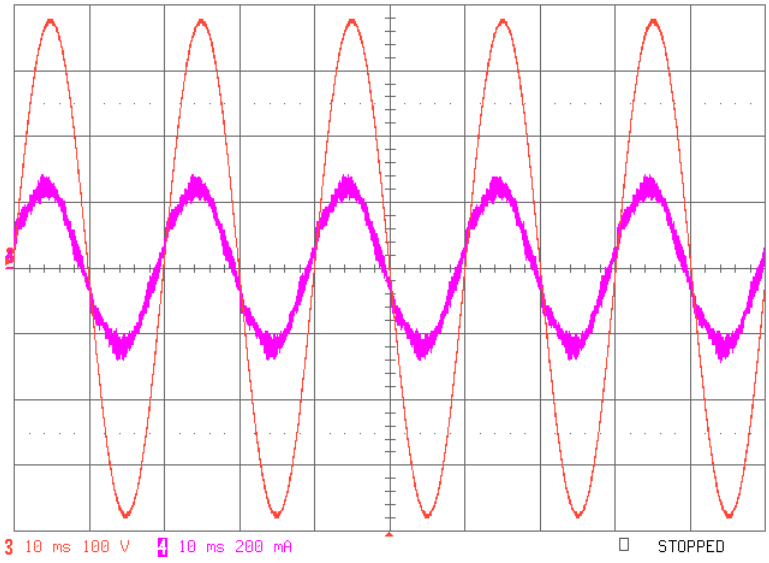


Figure 27 Input voltage and current at 265Vrms, full load
VIN (red), IIN (purple)

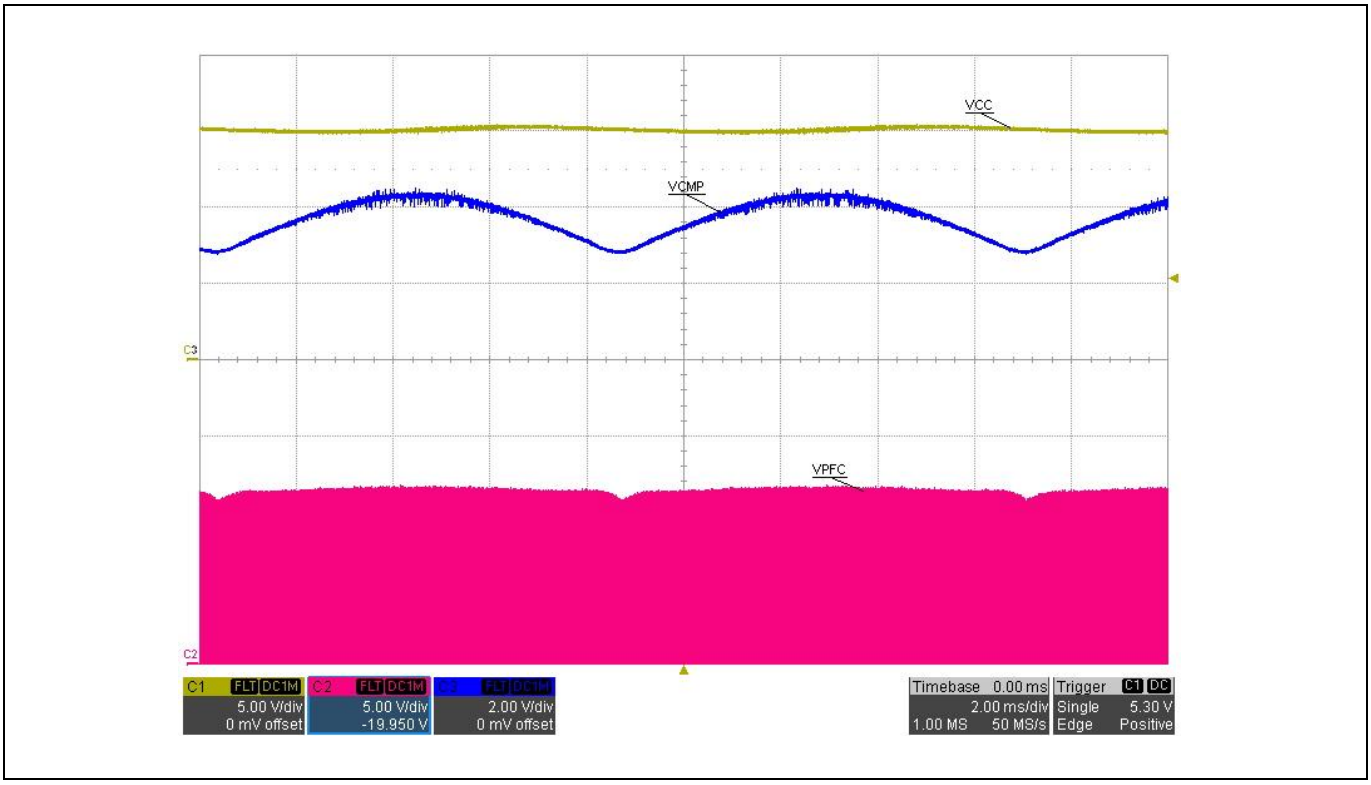


Figure 26 VCC, gate drive and CMP at 230Vrms, full load steady state operation
VCC (yellow), VPFC Gate Drive (red), VCMP (blue)

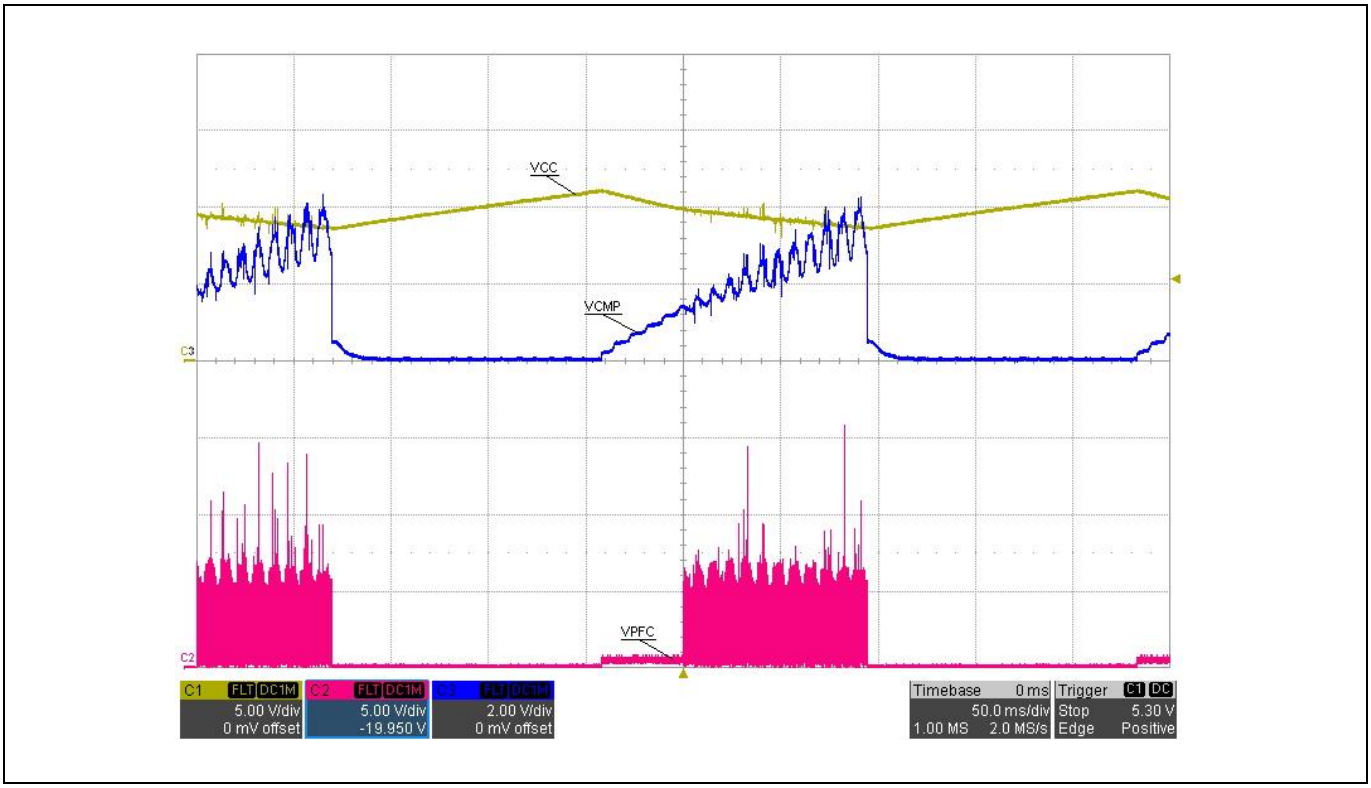


Figure 29 VCC, gate drive and CMP at 230Vrms, full load under short circuit condition
VCC (yellow), VPFC Gate Drive (red), VCMP (blue)

9.6 Thermal performance

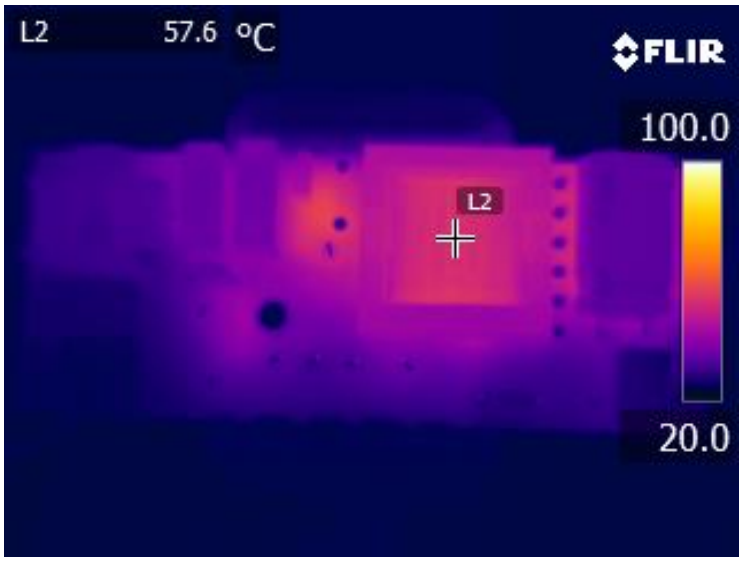


Figure 30 Top side thermal image after one hour in open air (ambient 25°C) at 230V, full load

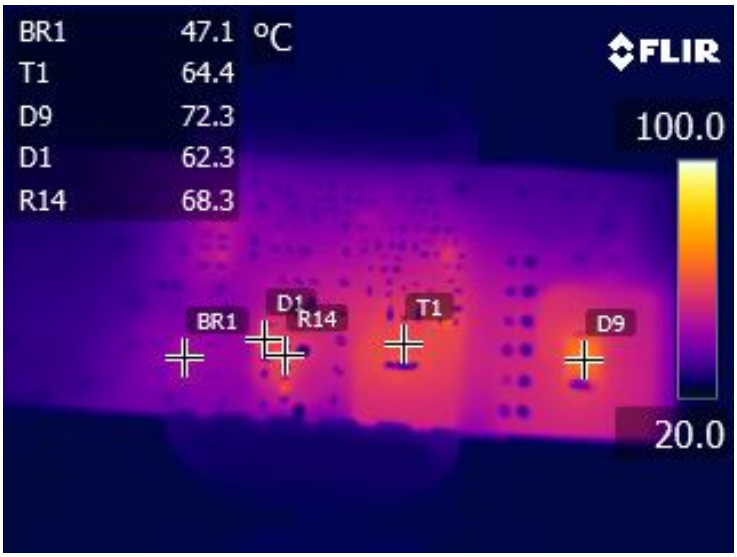


Figure 31 Bottom side thermal image after one hour in open air (ambient 25°C) at 230V, full load

10 Conclusion

The IRuFB1 evaluation board meets specifications. The output voltage remains within the 47.5 to 52.5V range from 10% to 100% of rated load and below the 65V limit under a zero load condition. Voltage regulation performance is met due to the transformer design being optimized for low primary leakage inductance. In the case of a higher leakage inductance, R19 can be replaced with a resistor in the 10-47 Ohm range to filter out high frequency leading edge oscillations.

Output voltage ripple at twice the line frequency is approximately 5V peak to peak at full load in the 50 to 60Hz line frequency range. This is a typical result for a PFC flyback converter and could be reduced by increasing the output capacitor. Power factor at full load remains above 0.95 over the input voltage range and iTHD remains at around 5%. EN61000-3-2 class C limits are met comfortably.

Component temperatures measured in open air at room temperature (assumed 25 degrees C) remain below the maximum specified limits assuming a 35 degree rise for the highest case ambient of 60 degrees C.

It has been demonstrated that a practical low cost, voltage regulated, isolated PFC flyback converter may be built around the IRS2505L provided that the gate drive and zero-crossing detection circuit modifications are incorporated as shown. In addition, adequate protection against over-volatge, over-load and short circuit conditions has been included without additional cost.

Operation at lower line voltage in the 120VAC range is also possible, however some modifications to the transformer may be required to accommodate higher primary peak and RMS current operating at a higher maximum duty cycle. The start-up delay and recovery from short-circuit period however would be significantly increased at lower line.

References

[1] IRS2505LPBF SMPS control IC datasheet, Infineon Technologies.

[2] IRuFB1 40W Isolated flyback PFC, International Rectifier (an Infineon Technologies company)

Attention:

Revision History

Major changes since the last revision

Page or Reference	Description of change
October 27, 2016	First Release
December 8, 2017	Added information

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