

Design of a 600 W HB LLC Converter using 600 V CoolMOS™ P6

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Application Note

About this document

Scope and purpose

This note will describe the design and performance of a 600 W LLC SMPS Demo Board. This is a high performance example with a complete Infineon solution, including HV & LV power MOSFETs, controllers, and drivers, demonstrating a very effective way to design the HV DC/DC isolation stage of a Server PSU fulfilling the 80Plus® Titanium Standard.

Besides design information and documentation of the LLC converter, the reader will receive additional information how the 600 V CoolMOS™ P6 behaves in this LLC board and what benefits will be achieved. Plus insights in how to develop LLC converters in similar power ranges adapted to your own requirements.

Intended audience

This document is intended for design engineers who wish to evaluate high performance alternative topologies for medium to high power SMPS converters, and develop understanding of the design process. Also, how to apply the somewhat complex LLC design methods to their own system applications.

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1 Introduction

The reduction of size in power converters by increasing switching frequency and reducing magnetics component size is a goal pursued for decades. The development of resonant converters with Zero Voltage Switching (ZVS) has been a cornerstone of this effort, but for a long time they have been considered as a way to “make good power from mediocre semiconductors”, in fact limiting their usage. Moreover, with the advent of CoolMOS™ high performance silicon switches based on the superjunction concept, the improvements in Figure of Merit even lessened the need for using resonant topologies for many years. Now, the industry requirements for high efficiency in converter performance, which drove a trend towards resonant switching square wave converters, such as the Phase Shift Full Bridge converter, are creating a need for a closer look at the somewhat more difficult to design multiresonant LLC converter.

Classically, fully resonant converters have had a nominal disadvantage in conduction losses compared with soft switching square wave converters like the Phase Shift Full Bridge, due to the difference in peak versus RMS current for sinusoidal current waveshapes versus trapezoidal. However, with the advent of the multi-resonant converter, and its boost up mode of operation, it is possible with modern MOSFETs and their excellent Figure of Merit to achieve better-optimized results with the LLC converter. This is in large due to the fact that the square wave converter is optimized at maximum duty cycle, which is only achieved at low line condition. Hence, to provide operational capability with typical PFC front ends, and some converter hold up time capability, they will typically need to be optimized for DC input as low as 325 V or 300 V, wherein they will normally operate at 380 V with a less favorable crest factor and higher net RMS current.

In contrast, an LLC converter can be optimized for the nominal DC input voltage, and use the boost up mode below the main resonance to achieve low line regulation with proper design. Combine this with a favorable silicon Bill of Material (BOM) situation, compared with a Phase Shift Full Bridge topology, the proper design approach, and a high performance converter is readily in reach.

In Figure 1, you can find a very synthetic comparison of several Figure of Merit metrics based on cost and performance between the Phase Shift Full Bridge converter and the LLC HB.

You see that the first (blue arrows) still keeps some important features especially in controllability and flexibility in wide output regulation range, but the HB LLC (red arrows) provides some very important benefits in a modern SMPS design, like reduced BOM, easier ZVS and more performant Synchronous Rectification.

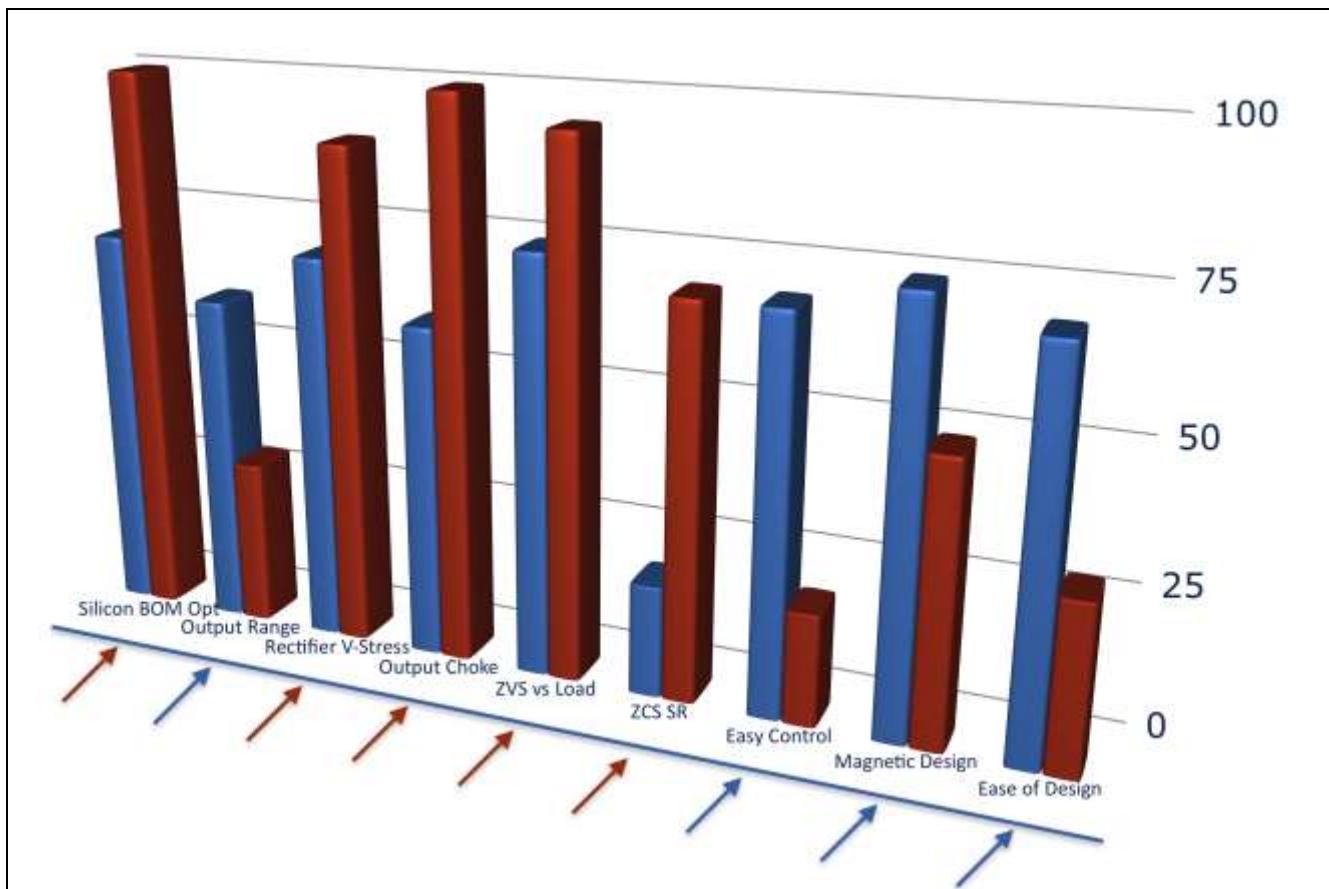


Figure 1 Comparison of several Figure of Merit metrics based on cost and performance between the PS FB (blue) converter and the LLC HB (red).

The principles of operation for the LLC converter will be examined in the next section, and the main tank design concepts reviewed. This will be followed by detailed design methodologies using both First Harmonic Approximation (FHA) and supplemented by exact design concepts.

The scope of this document is to describe the details of an analog controlled 600 W Half Bridge (HB) LLC demo board fully designed using Infineon products. (Order information in ISAR: *EVAL_600W_12V_LLC_P6_A*)

The target efficiency of this design is fixed according to the need to fulfill at complete PSU stage the 80+ Titanium Standard; that means certain minimum efficiency requirements for the HV DC/DC stage are fixed at 10%, 20%, 50% and 100% load conditions.

2 HB LLC converter principles of operation

The typical modes of operation of the LLC converter will be discussed in this chapter using an initial description of the concept behind First Harmonic Approximation (FHA). The reasoning behind the basic configuration of the resonant tank will be shortly introduced. Finally, the concepts and challenges for successful implementation of synchronous rectification will be outlined.

The most important concepts are referred to here, in order to better understand the design considerations.

2.1 Tank Configuration and Operational Modes

The principle schematic of a Half Bridge LLC converter is shown in Figure 2.

C_r , L_r and L_m represent the so called “resonant tank”: together with the main transformer, they are the key components in the LLC design.

The primary half bridge and the output rectification are the other two stages to be defined.

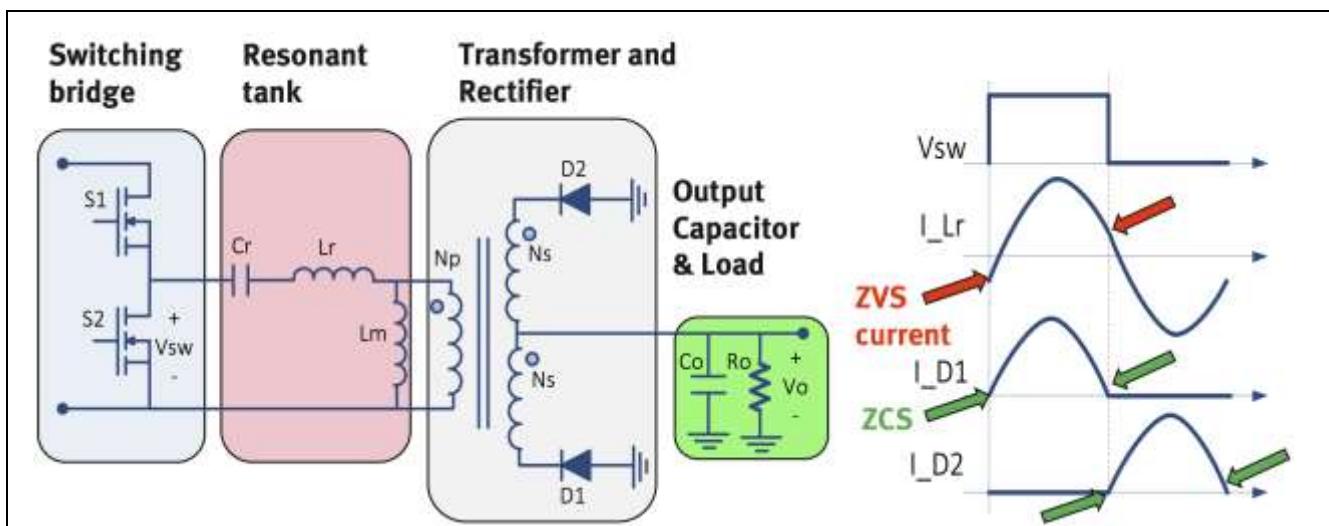


Figure 2 Principle schematic of a half Bridge LLC converter

The LLC is a resonant converter that operates with frequency modulation instead of the Pulse Width Modulation (PWM), traditional approach to power conversion.

The following Figures 3, 4, 5 and 6 will graphically explain the fundamental operating mode of a HB LLC converter.

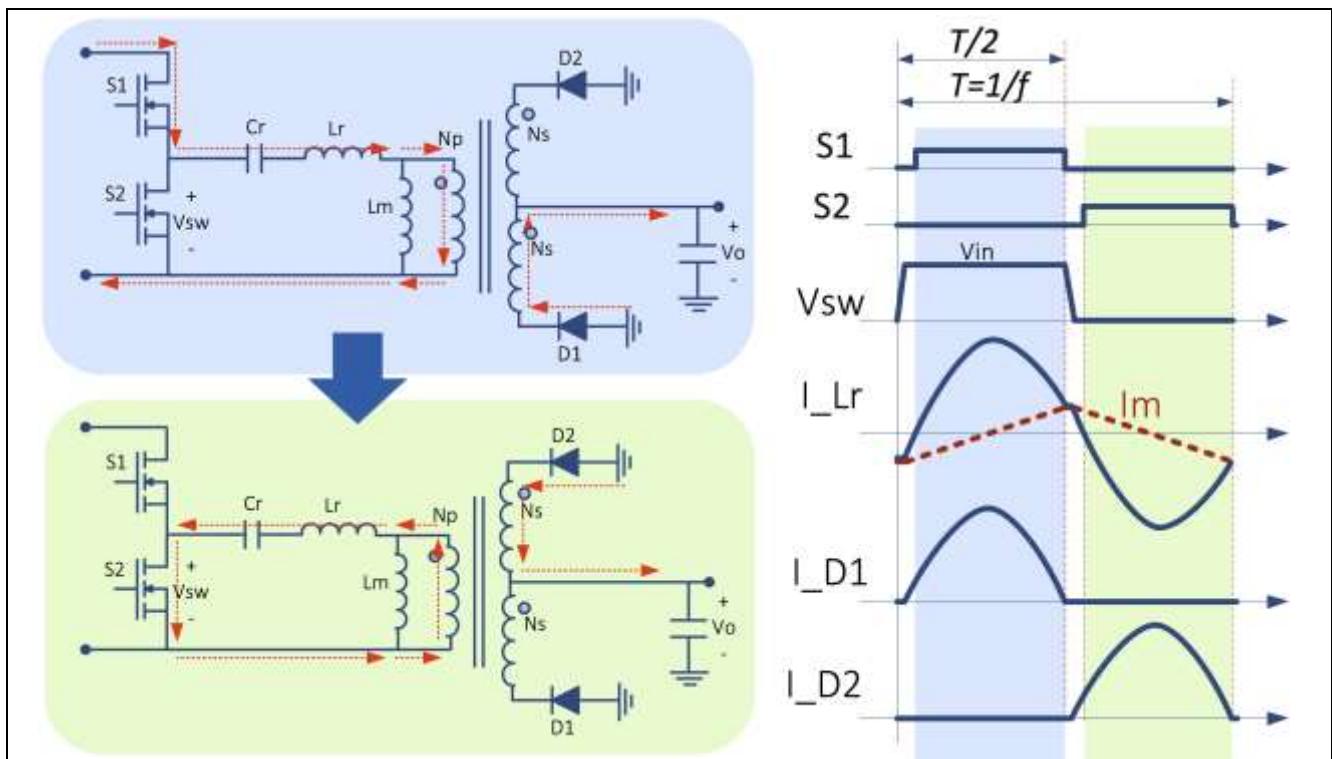


Figure 3 Fully resonant operating mode, at resonant point for C_r and L_r , with near ZCS turn-off of primary side MOSFETs.

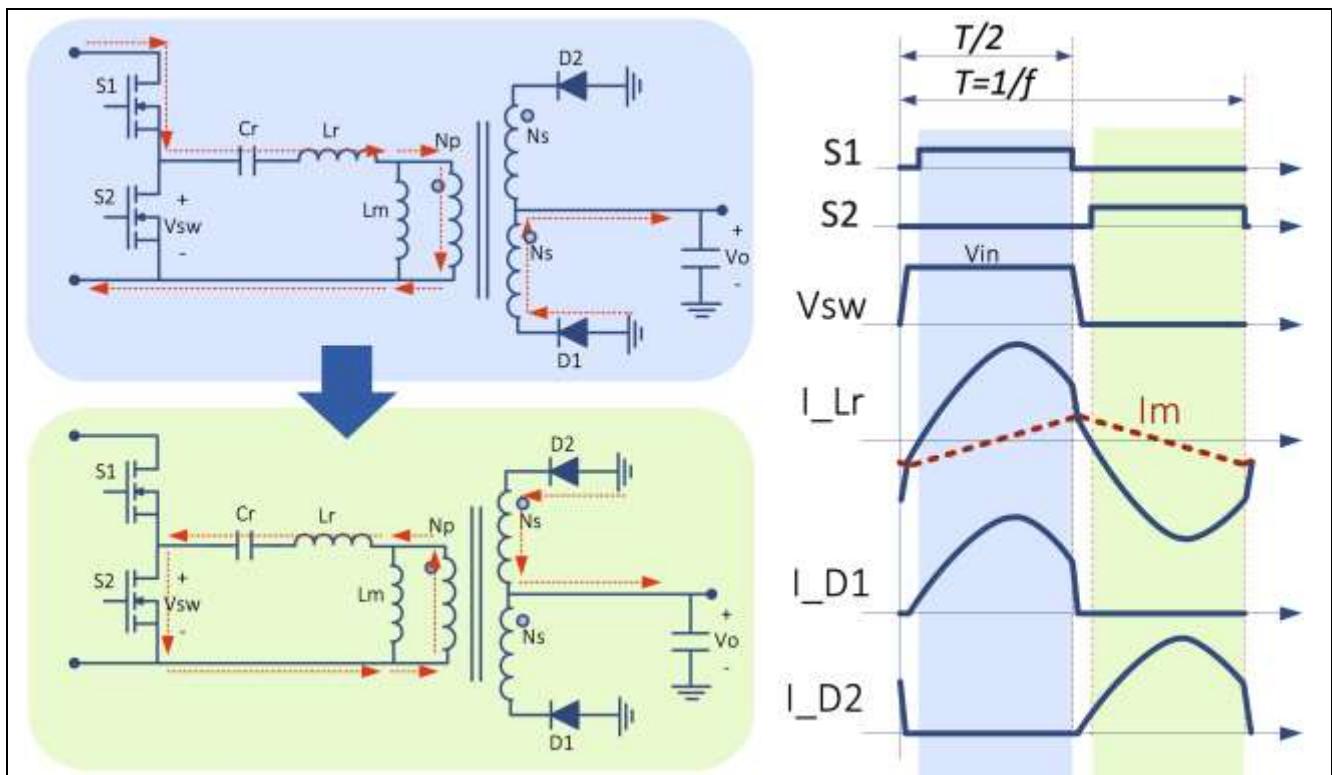


Figure 4 Over resonant operation, above C_r - L_r resonance, for both half cycles, showing tank current waveforms and non-ZCS turnoff of the primary side MOSFETs

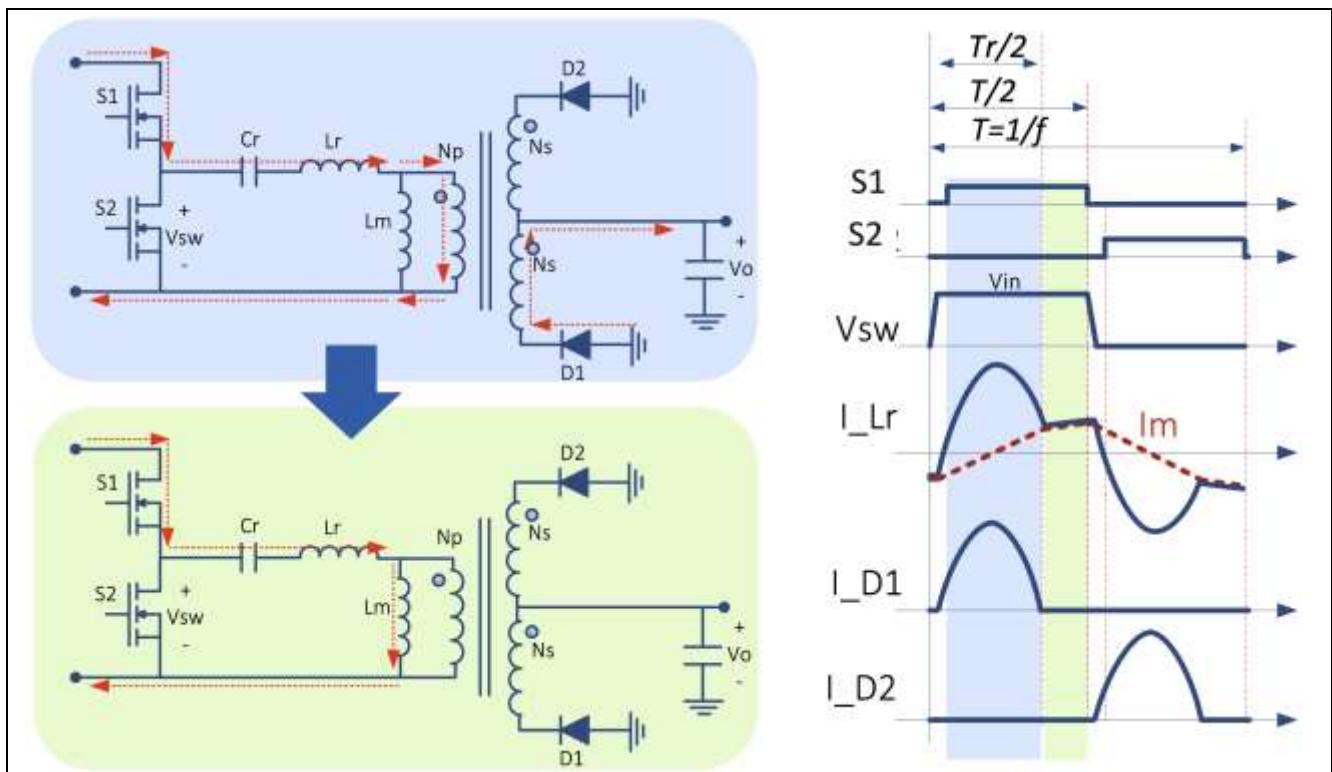


Figure 5 Under resonant DCM operation, (between resonant point of C_r and L_r , versus resonant point of C_r and L_r+L_m) half cycle 1

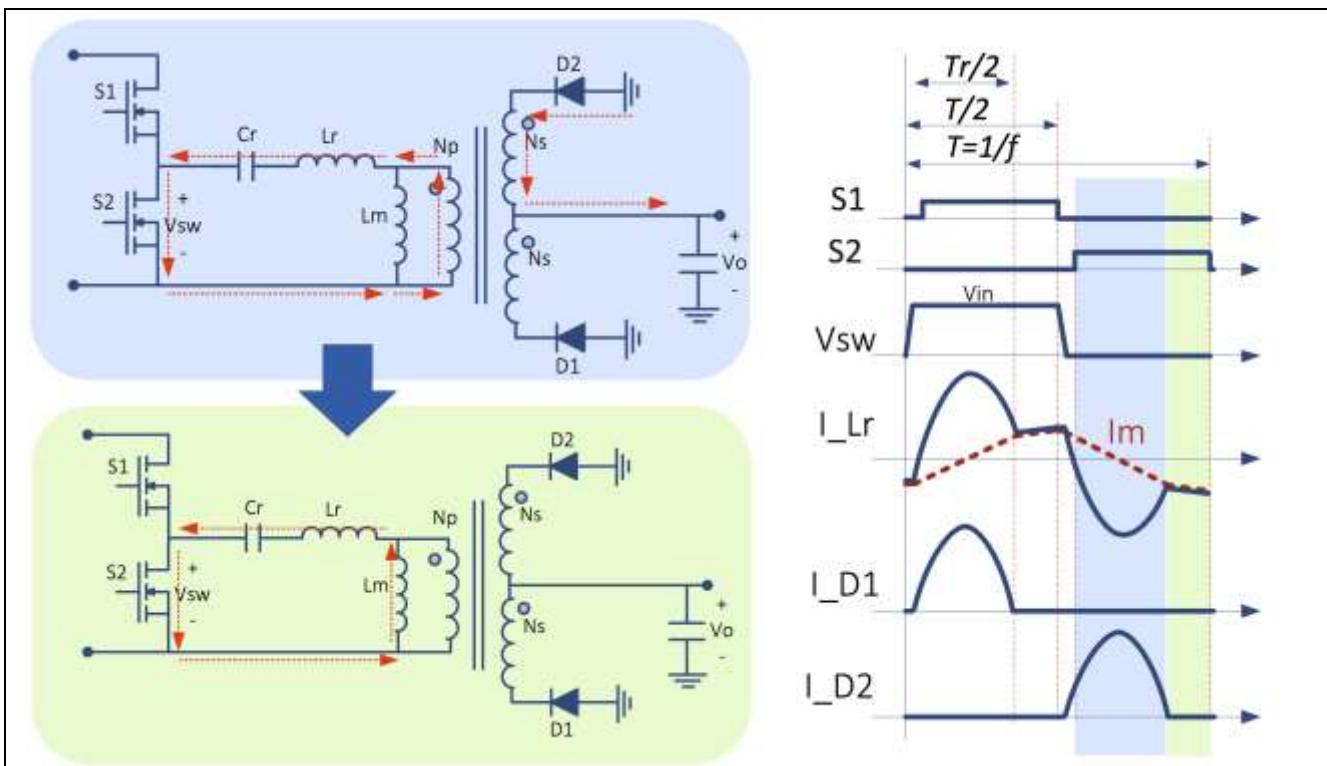


Figure 6 Under resonant DCM mode operation, (between resonant point of C_r and L_r , versus resonant point of C_r and L_r+L_m) 2nd half cycle

2.2 Analysis of the Basic Tank Characteristics using FHA

Starting point in a resonant converter design is the definition of an energy transfer function, which can be seen as a voltage gain function, so a mathematical relationship between input and output voltages of the converter. Trying to get this function in an “exact” way involves several nonlinear circuital behaviors governed by complex equations. However, under the assumption that the LLC operates in the vicinity of the series resonant frequency, important simplifications can be introduced.

In fact, under this assumption, the current circulating in the resonant tank can be considered purely sinusoidal, ignoring all higher order harmonics: this is the so-called First Harmonic Approximation Method (FHA), which is the most common approach to the design of a LLC converter.

In the FHA, the voltage gain is calculated with reference to the equivalent resonant circuit shown in Figure 7.

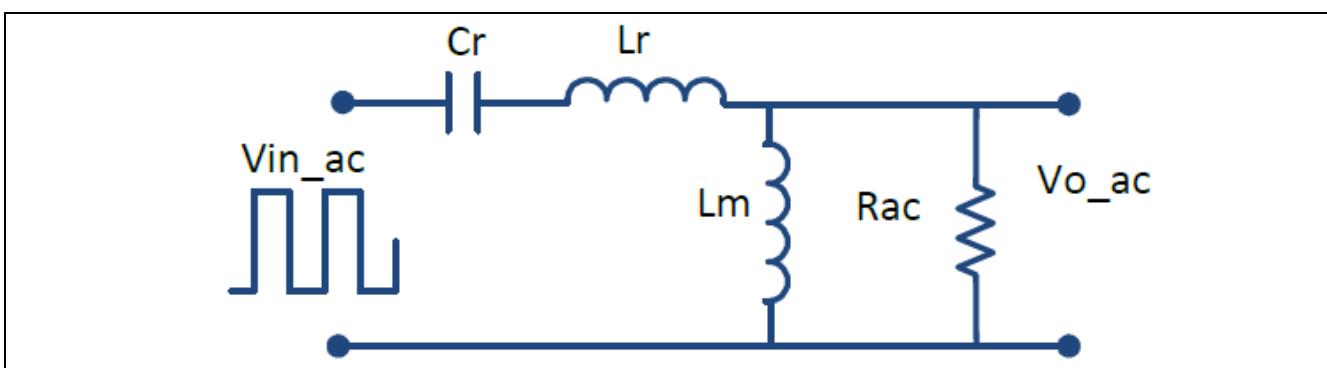


Figure 7 First Harmonic Approximation equivalent resonant circuit

The mathematical expression of the gain K is given in terms of a normalized resonant frequency F_x :

$$K(Q, m, F_x) = \left| \frac{V_{o_ac}(s)}{V_{in_ac}(s)} \right| = \frac{F_x^2(m-1)}{\sqrt{(m \cdot F_x^2 - 1)^2 + F_x^2 \cdot (F_x^2 - 1)^2 \cdot (m-1)^2 \cdot Q^2}} \quad (1)$$

Where:

$$m = \frac{L_r + L_m}{L_r}; \quad f_r = \frac{1}{\sqrt{L_r \cdot C_r}}; \quad F_x = \frac{f_s}{f_r}; \quad R_{ac} = \frac{8}{\pi^2} \cdot \frac{N_p^2}{N_s^2} \cdot R_o; \quad Q = \frac{\sqrt{L_r/C_r}}{R_{ac}}; \quad (2)$$

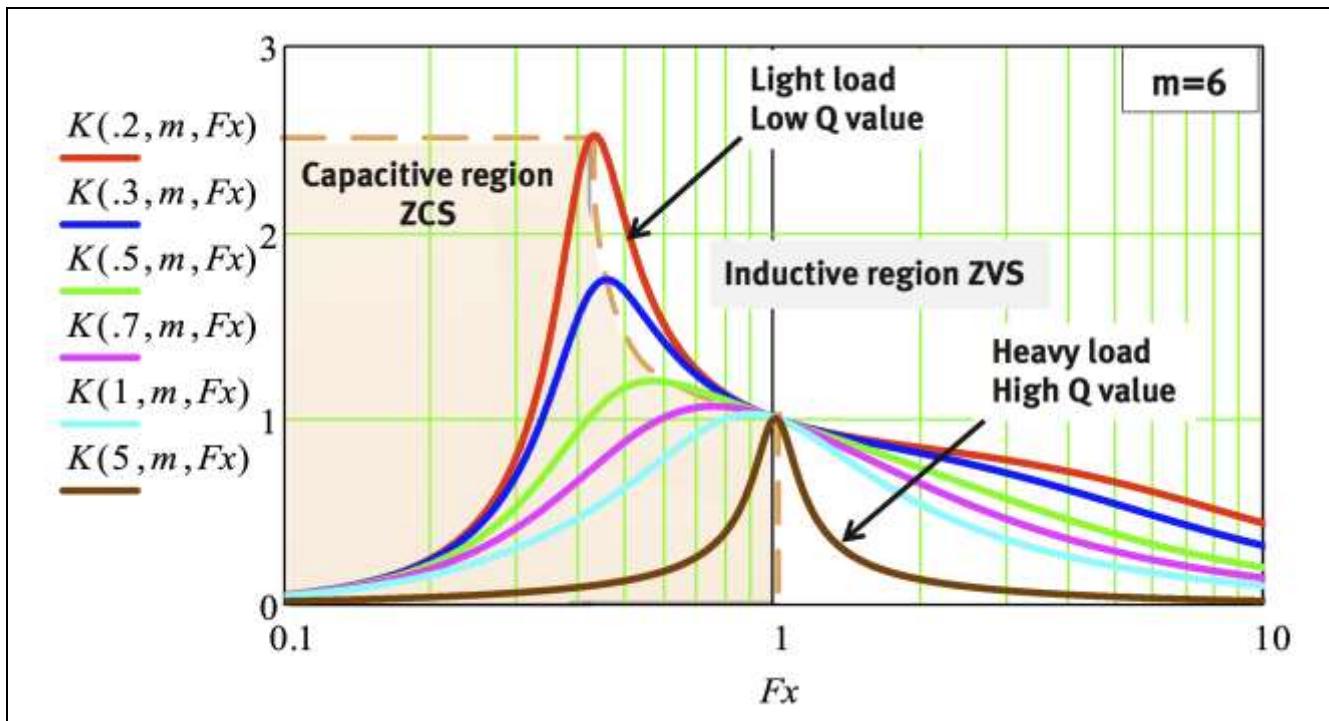


Figure 8 Family of Q curves for a fixed m inductance ratio of 6

2.3 Tank Q Values and m Inductance Ratio: System Implications

The resonant tank gain K can be plotted as a function of the normalized driving frequency f_x for different values of the quality factor Q and any single value of the inductance ratio factor m .

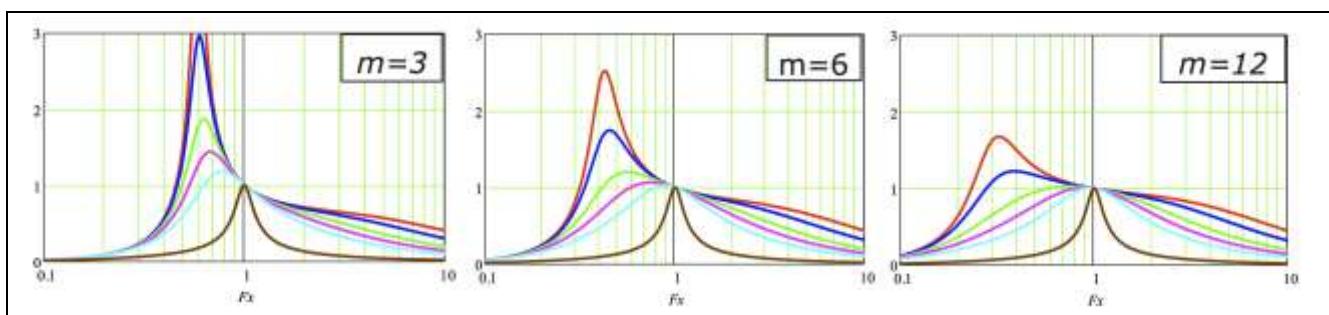


Figure 9 Family of Q curves for m inductance ratios of 3, 6, and 12

2.4 Benefits of Split Capacitor C_r

The design described in the present document uses the configuration shown in Figure 10, typically known as “split resonant capacitor technique”. This solution provides a couple of important benefits.

The first one is the reduction of the AC current stress on the resonant and input “bulk” capacitors, with consequent relaxed AC current requirements on those components, thus cost reduction and extended lifetime.

The second one involves the typically critical LLC start-up sequence.

In fact, the split capacitor technique provides the possibility to charge the resonant capacitance simultaneously to the input bulk cap, thus reducing the needed charging time. In fact, until the resonant capacitor is completely charged, the transformer is not driven symmetrically, so there is a significant difference in the up and down slopes of the resonant current and the current may not reverse in a switching half-cycle. This condition might create a very dangerous operation where a MOSFET is turned on while the body diode of the other HB MOSFET is conducting: this is the condition typically known as “hard commutation on conducting body diode”, which submits the turning-off device to heavy stress and this may happen for several cycles at the converter start-up.

Using the split resonant capacitor technique, the risk of having hard commutation is significantly reduced in case the HV DC/DC converter is powered up in relatively short time after the input bulk capacitor has been charged to the DC-link voltage.

Of course, we would like to make clear that this technique only may reduce the possible occurrence of hard commutation, but does not guarantee 100% prevention.

A safe and reliable operation at start-up is only possible through a proper control algorithm and HV MOSFET driving technique, along with a power device with rugged body diode.

For further details about this topic, please refer to the paragraph 4.4 of the present document and [4].

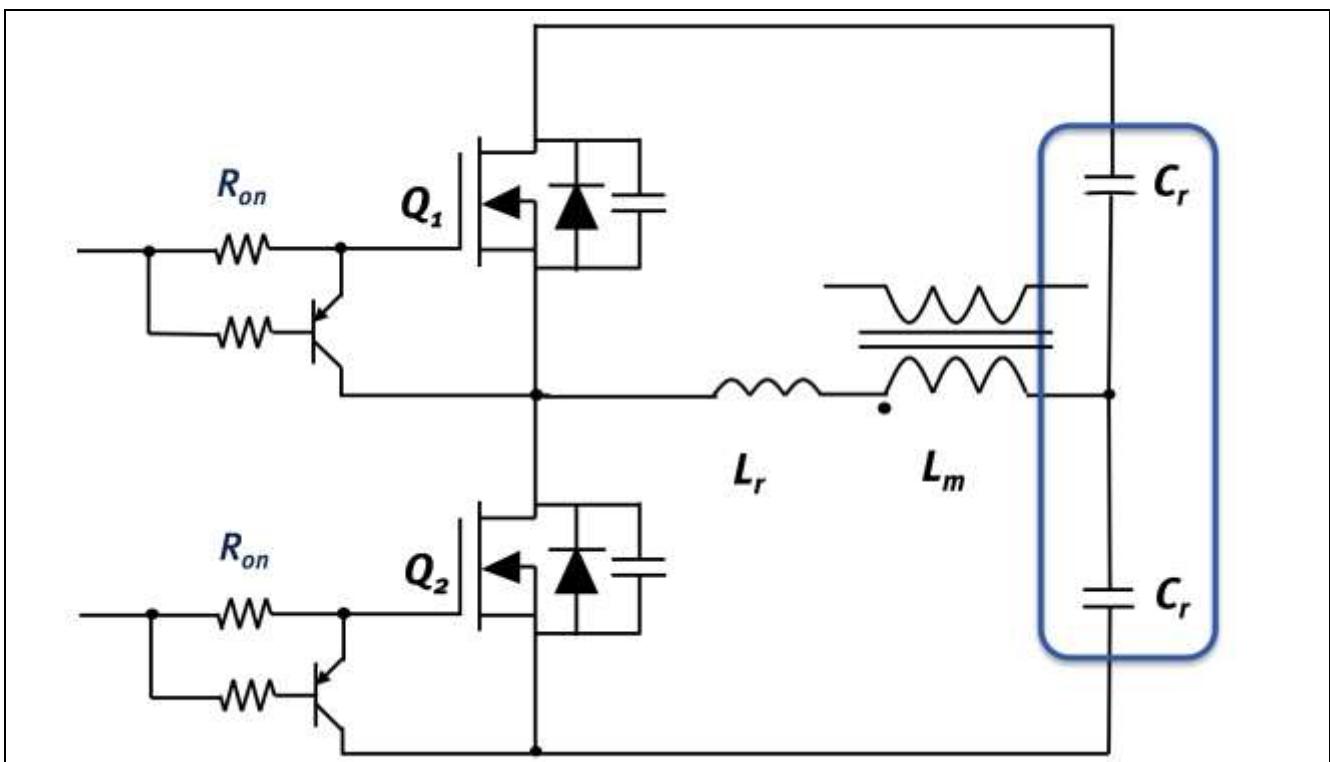


Figure 10 Re-arranging the resonant capacitor into a split capacitor Half Bridge configuration

2.5 Synchronous Rectification Concepts for LLC

Figure 11 shortly summarizes the technique to manage Synchronous Rectification in HB LLC Converter

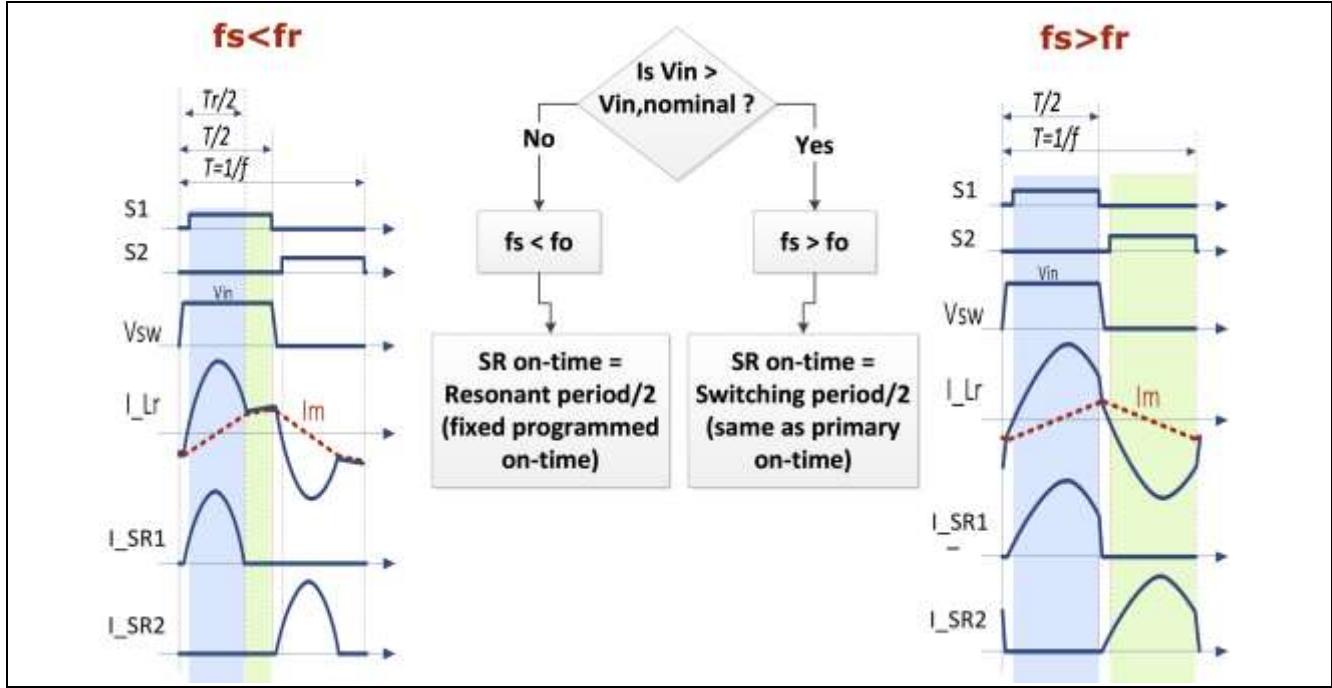


Figure 11 SR in HB LLC Converter

3 LLC design methodologies for specific application requirements

An optimization procedure for the selection of the main LLC parameters, for both FHA method and using exact calculation or simulation will be shown in the next section. The goal will be to achieve the best performance while fulfilling input and output regulation requirements.

At the same time, Zero Voltage Switching operation of the primary HB MOSFETs must be ensured in order to get full benefits out of the soft switching behavior, especially at light load.

3.1 Input Design Data

In Table 1, an overview of the major design parameter is displayed.

Table 1 Design parameters

Description	Minimum	Nominal	Maximum
Input Voltage	350 V _{DC}	380 V _{DC}	410 V _{DC}
Output Voltage	11.9 V _{DC}	12 V _{DC}	12.1 V _{DC}
Output Power			600 W
Efficiency at 50% P _{max}	97.4%		
Switching Frequency	90 kHz	150 kHz	250 kHz
Dynamic Output Voltage regulation (0-90% Load step)			Max. overshoot =0.1 V Max. undershoot=0.3 V
V _{out_ripple}			150 mV _{pk-pk}

From the table above, the first important design parameters can be derived:

Main transformer turn ratio

$$n = \frac{N_p}{N_s} = \frac{V_{in_nom}}{2 \cdot V_{out_nom}} \approx 16 \quad (3)$$

Minimum needed Gain

$$K_{\min}(Q, m, F_x) = \frac{n \cdot V_{o_min}}{\sqrt{V_{in_max}^2 - V_{in_min}^2}} \approx 0.95 \quad (4)$$

Maximum needed Gain

$$K_{\max}(Q, m, F_x) = \frac{n \cdot V_{o_max}}{\sqrt{V_{in_max}^2 - V_{in_min}^2}} \approx 1.08 \quad (5)$$

3.2 Gain Curve

The resulting gain curves, Figure 3, for loads between 10% and 100% P_{max} are in the following plot:

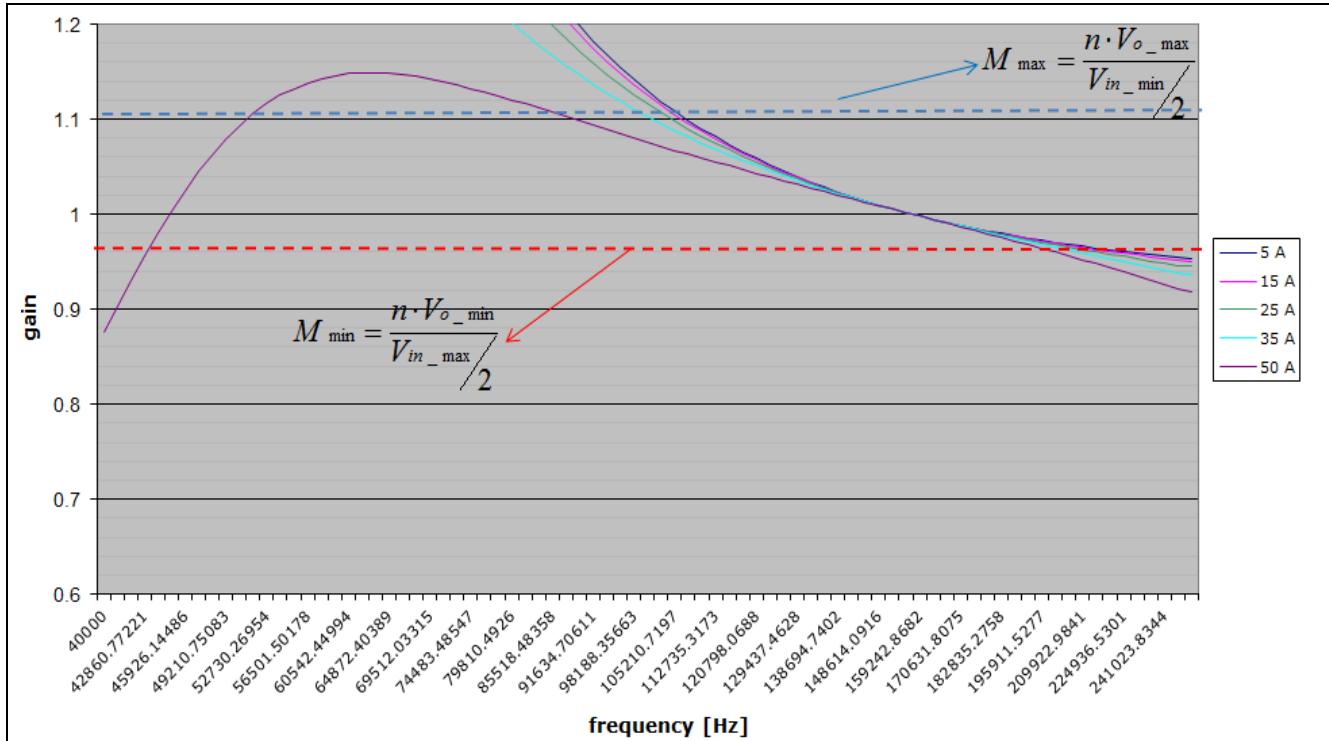


Figure 12 Gain Curve

Both the M_{min} and M_{max} limits cross all the gain curves of our LLC converter: that means the in-out regulation is fully achieved in the specified ranges.

3.3 Suggested FHA Optimization Process

Figure 13 shows a flow-chart including all the steps in the design of a HB LLC converter.

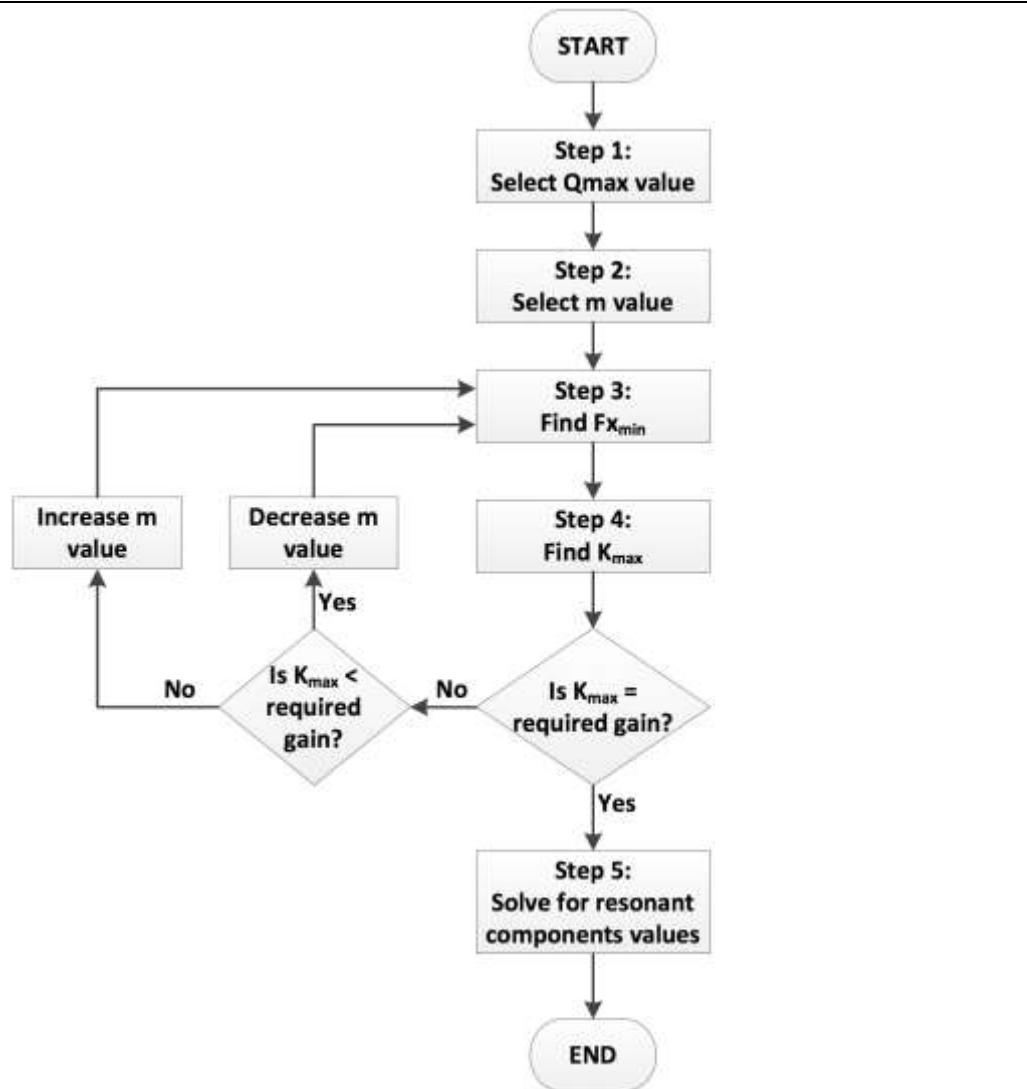


Figure 13 Suggested FHA Optimization Process

For all the details of this method you can refer to [2]

3.4 Notes on the Selection of the Inductance Factor m

The inductance factor (Equation 2) has an important impact on the converter operation. Lower values of m achieve higher boost gain and narrower range of the frequency modulation, that means more flexible control and regulation, which is valuable in applications with very wide input voltage range.

On the other hand, this also means smaller values of L_m , which leads to significantly high magnetizing current circulating in the primary side: this current does not contribute to the power transferred, but mainly generates conduction losses on the primary side.

In other words, there is a trade-off between flexible regulation and overall efficiency requirements, especially at light load.

In the case of the demo board described in the present document, the main goal is to achieve high efficiency, so relatively high m is selected. This minimizes the circulating current from the magnetizing inductance. This is allowable because the stated input range is relatively narrow, and a higher value of L_m will be acceptable as long as sufficient current is available to achieve resonant transitions under light load conditions.

We rely on the bulk capacitor in case of specific hold up time requirement at the complete AC/DC SMPS level. However, high-density designs may not permit this, as the bulk capacitor does not shrink with increasing switching frequency. In some cases, adjustment of the input voltage range may be needed.

In this case, the chosen value is $m \approx 12$.

3.5 Resonant Components Calculation

Combining equations (1) and (2), we get a system where the unknown variables are L_r , C_r and L_m

Solving it, the following values are set for the LLC converter:

$$n = \frac{N_p}{N_s} = \frac{V_{in_nom}}{2 \cdot V_{out_nom}} \approx 16 \Rightarrow N_p = 16; N_s = 1 \quad (6)$$

$$m = \frac{L_r + L_m}{L_r} \approx 12 \Rightarrow L_m = 195 \mu H; L_r = 17 \mu H \quad (7)$$

$$C_r = 66 nF \quad (8)$$

$$f_r = \frac{1}{2\pi \cdot \sqrt{L_r \cdot C_r}} \approx 150 KHz \quad (9)$$

3.6 The ZVS Behavior: Energy and Time Considerations

The ZVS calculations involve two kinds of analysis, the one in the energy domain and the other in the time domain. The goal is to have enough energy in the resonant tank able to discharge the output capacitance of the primary MOSFET, but also an appropriate dead time between the two devices.

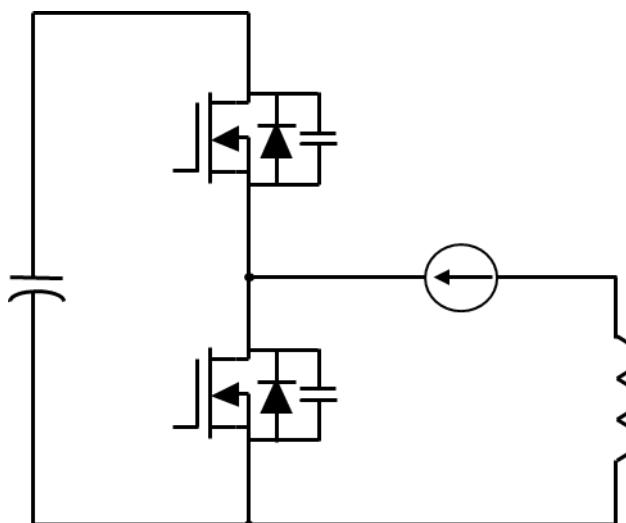


Figure 14 Equivalent circuit in resonant drain to source transitions

The two key parameters in our analysis are the following:

$C_{o(er)}$ is the C_{oss} energy related component of the used HV MOSFET, in our case IPP60R190P6.

Q_{oss} is the charge stored in C_{oss} at $V_{in(nom)} = 380 V_{DC}$. Q_{oss} is linked to the so called $C_{o(tr)}$ by the formula

$$Q_{oss} = C_{o(tr)} * V_{in(nom)}$$

$C_{o(er)}$ and $C_{o(tr)}$ are the effective output capacitances of the MOSFET, respectively energy and time related.

3.6.1 Energy Related Equations

$$I_{mag_min} = \frac{2 \cdot \sqrt{2}}{\pi} \cdot \frac{n \cdot V_o}{2\pi \cdot f_{sw_max} \cdot L_m} = 0.672A \quad (10)$$

$$En_{res_min} = \frac{1}{2} \cdot (L_m + L_r) \cdot I_{mag_min}^2 = 95.1\mu J \quad (11)$$

$$En_{cap_max} = \frac{1}{2} \cdot (2C_{o(er)}) \cdot V_{DS_max}^2 \approx 9\mu J \quad (12)$$

$$\Rightarrow En_{res_min} > En_{cap_max} \quad (13)$$

3.6.2 Time Related Equations

It can be demonstrated that:

$$t_{dead} = \frac{t_{ecs}}{2} + \frac{2 \cdot Q_{oss, @ 400V}}{I_{m, pk}} \quad (14)$$

where t_{dead} is the dead time set between the conduction time of the two HB devices and t_{ecs} is the time when the channel of each MOSFET is still in conduction after turning it off (linear mode operation), which is function of some device parameters like $V_{gs(th)}$, $R_{g(tot)}$ and C_{gs}/C_{gd} .

Using that formula, together with the min. and max. values of the magnetizing current and considering $t_{ecs}=10$ ns:

$$I_{mag_min} = \frac{2 \cdot \sqrt{2}}{\pi} \cdot \frac{n \cdot V_o}{2\pi \cdot f_{sw_max} \cdot L_m} = 0.672A \quad (10)$$

$$I_{mag_max} = \frac{2 \cdot \sqrt{2}}{\pi} \cdot \frac{n \cdot V_o}{2\pi \cdot f_{sw_min} \cdot L_m} = 1.66A \quad (11)$$

$$t_{dead, min} = \frac{t_{ecs}}{2} + \frac{2 \cdot Q_{oss, @ 400V}}{I_{m, ag, max}} \approx 130nsec \quad (14)$$

$$t_{dead, max} = \frac{t_{ecs}}{2} + \frac{2 \cdot Q_{oss, @ 400V}}{I_{mag, min}} \approx 311nsec \quad (15)$$

3.7 The Main Transformer Design

The most critical condition for the main transformer is the full load, mainly due to thermal reasons. The selection of the core size and material is done according to this condition along with the power density target (thus switching frequency) and the available airflow.

Keeping a due margin room in the design, the minimum efficiency requirement at full load is fixed for the HB LLC converter to 97%, which means our goal is to keep the total dissipated power in that condition below 18 W.

In order to guarantee a balanced spread of power and heating, a good rule in the design of the LLC Converter is to keep the total power dissipated on the main transformer below 1/6 of the total dissipated power, which means the max allowed power should be 3 W. This is our first important design input.

$$P_{trafo_MAX} = 3W \quad (16)$$

The max. operating temperature is 55°C, as in typical server applications. Due to the transformer safety isolation approvals, the max. operating temperature of the transformer must be lower than 110°C, so:

$$\Delta T_{trafo_MAX} = (110 - 55)^\circ C = 55^\circ C \quad (17)$$

From (16) and (17) the max. thermal resistance of the core shape can be easily derived:

$$R_{th_trafo_MAX} = \frac{\Delta T_{trafo_MAX}}{P_{trafo_MAX}} = \frac{55^\circ C}{3 W} = 18.3^\circ C/W \quad (18)$$

Our selected core shape must have thermal resistance lower than 18.3°C / W.

This requirement can be fulfilled through different methods: the preferred one will allow maximizing the ratio between available winding area and effective volume, of course compatibly with the eq. (18).

Also considering the power density target (in the range of 20 W / inch³), the most suitable selection is PQ 35/35, shown in Figure 15.

The related coil former shows a minimum winding area of 1.58 cm² and a thermal resistance of 16.5°C / W, so lower than (18), thus able to dissipate up to 3.33 W by keeping the $\Delta T_{MAX} < 55^\circ C$.

Once verified that the thermal equations are fulfilled, we can proceed with the design of the primary and secondary windings and the core material selection with some important goals:

- Fitting the geometry/overall dimensions of the core
- Fulfilling the condition (16)
- Try to split the losses between core and windings as equally as possible: ideally, “fifty-fifty” should be achieved at full load, but any percentage close to it would be acceptable.

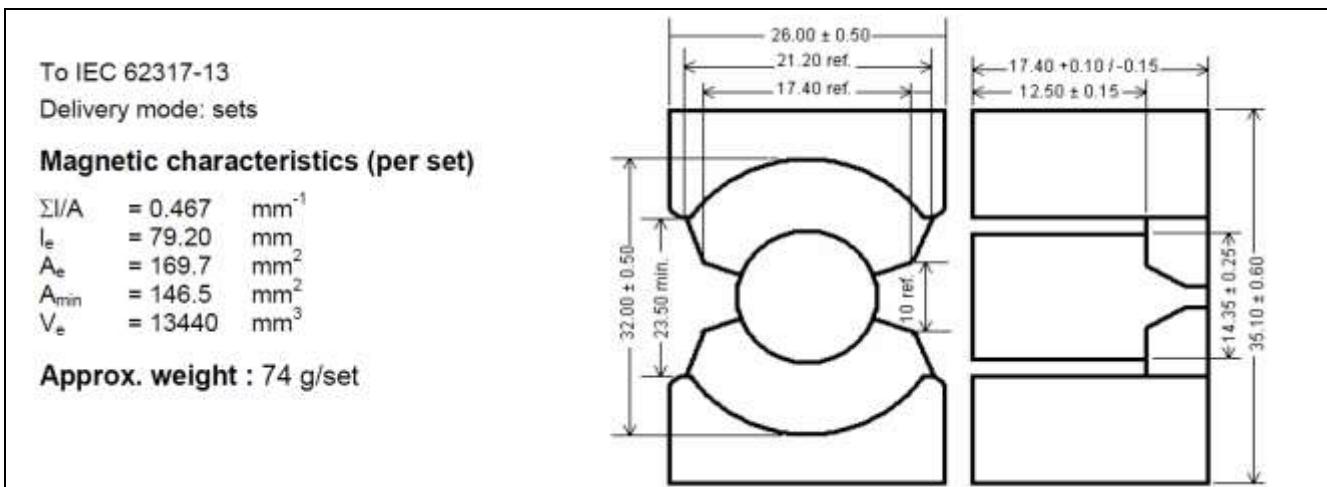


Figure 15 TDK-Epcos PQ35/35 core

The selected core material is the ferrite TDK PC95, showing a very interesting plot of Core Losses (PCV) vs. Flux Density vs. frequency (see Figure 16).

The final structure of the main transformer is shown in Figure 17 below. This has been developed in cooperation with the partner company Kaschke Components GmbH, Göttingen - Germany

So the primary is realized in a “sandwich” technique using 16 turns of 4 layers of Litz wire 45 strands 0.1 mm diam. This allows to minimize the AC losses due to skin and proximity effect. The secondary is done with copper band 20x0.5 mm.

Material: PC95

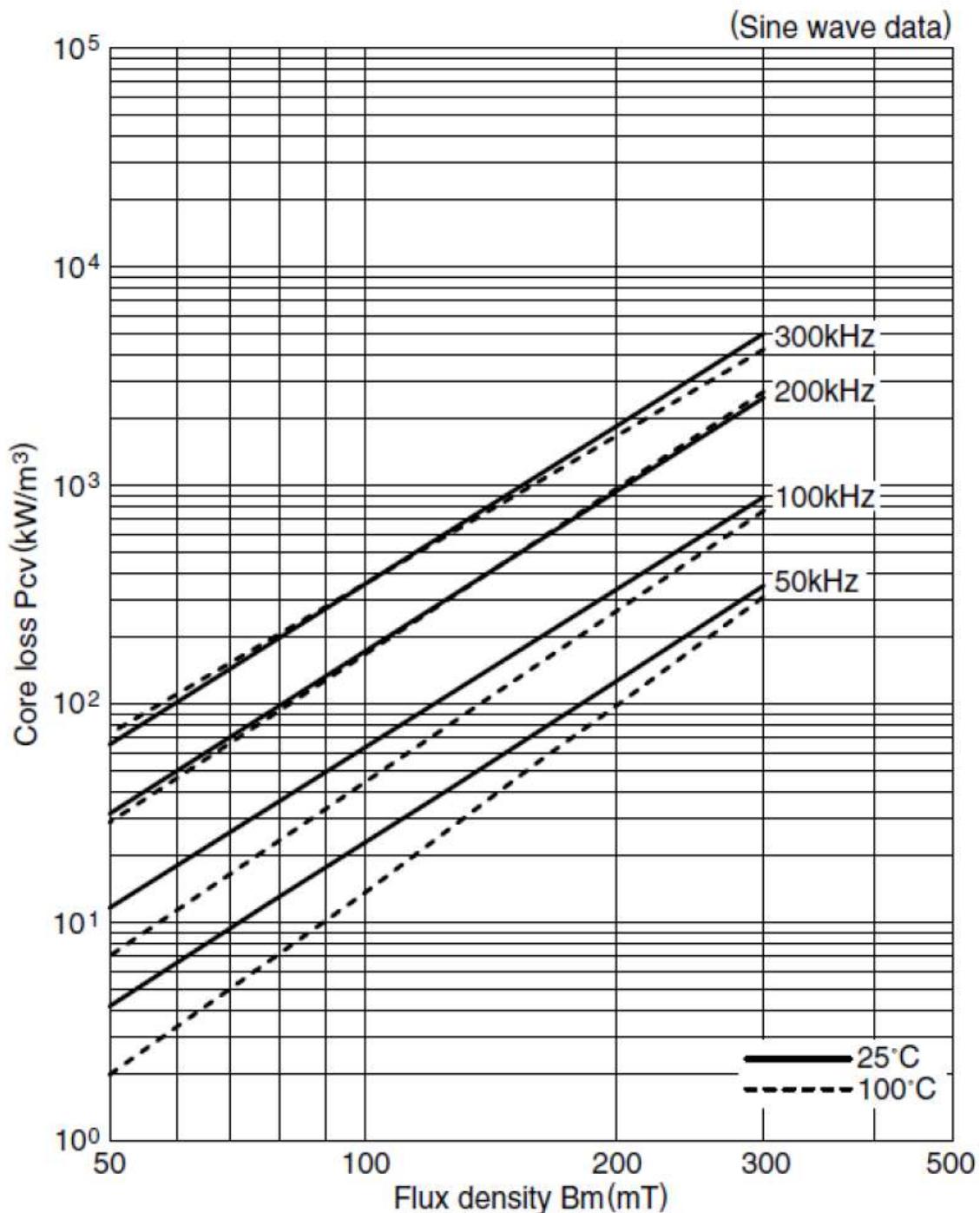


Figure 16 Ferrite core material TDK PC95

With this choice, at full load condition, the total copper losses (primary + secondary, DC+AC components) are 1.1 W, the core losses are 1.8 W, so overall:

$$P_{trafo} = P_{copper} + P_{core} = 2.9W < P_{trafo_MAX} = 3W \quad (19)$$

In other words, the (19) fulfils the thermal equation (18)

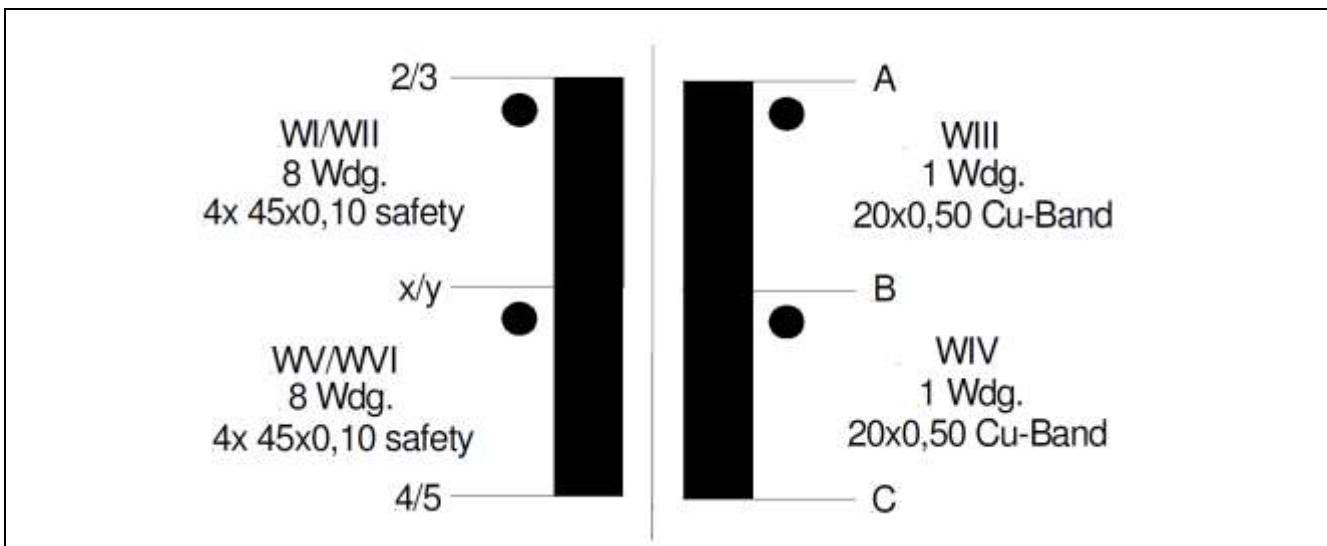


Figure 17 Winding structure of the PQ 35/35 LLC transformer (Kaschke Components GmbH)

An important transformer parameter involved in the LLC design is the primary or magnetizing inductance L_m , which, according to eq. (7), must be $195 \mu\text{H}$. This value is obtained with distributed air-gap on the side legs of the PQ core: this construction is preferred since it minimizes the effect of the so called “fringing flux” which generates additional losses in the windings close to the inner limb.

3.8 The Resonant Choke Design

In LLC designs with stringent power density requirements, the resonant choke is typically embedded in the transformer, in the sense that the leakage inductance is utilized on this purpose. This technique has the big advantage to save space and the cost of an additional magnetic component, but also some drawbacks, like the not easy controllability of the L_r value in mass production.

In the case of the present design, it has been decided to use an external L_r . This is because the demo board is intended to be primarily used for testing and benchmarking, and high power density is not in the main focus: having the resonant inductance externally allows changing in a more flexible way the resonant tank.

According to eq. (7), the overall value of L_r shall be $17 \mu\text{H}$, including the contribution of the transformer primary leakage inductance.

The external resonant choke is realized using a RM-12 core and a winding construction illustrated in Figure 18 below and implemented by the partner company Kaschke Components GmbH, Göttingen - Germany.

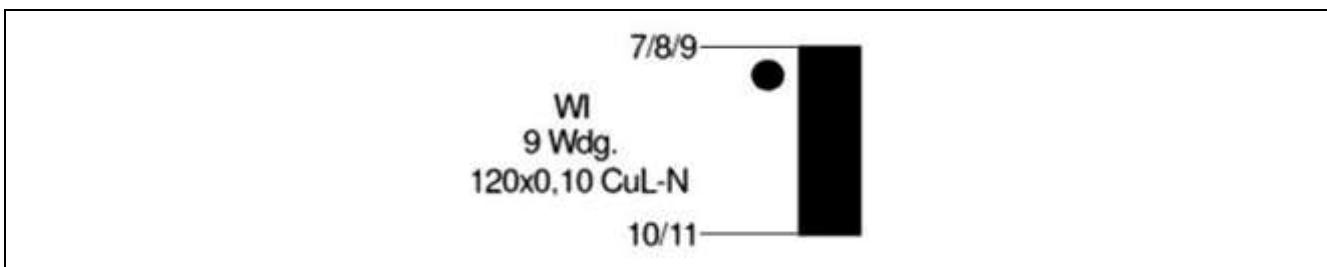


Figure 18 Winding structure of the RM12 resonant choke (Kaschke Components GmbH)

3.9 The Synchronous Rectification Stage

In applications that target high efficiency both at low and high loads (such as 80PLUS Titanium), while often requiring high power densities, it is critical to select for the Synchronous Rectification Stage MOSFETs that combine multiple key characteristics.

First of all, these Sync Rec MOSFETs should exhibit very low $R_{DS(on)}$. Indeed, due to the low voltages observed on the secondary side of server power supplies, large currents flow through the Sync Rec MOSFETs. Moreover, compared with other topologies such as ZVS PS FB (Zero Voltage Switching Phase-Shifted Full Bridge), using LLC topology leads to not only increased peak currents for the Sync Rec MOSFETs, but also higher root-mean-square currents I_{RMS} .

The conduction losses P_{cond} of each Sync Rec MOSFET are given by:

$$P_{cond_SR} = R_{DS(on)} \cdot (I_{RMS})^2 \quad (20)$$

These losses can only be mitigated through the use of a part with very low $R_{DS(on)}$.

Secondly, it is critical for these Sync Rec MOSFETs to exhibit low gate charges Q_g .

At light load, the switching losses of the Sync Rec MOSFETs predominate over the conduction losses. In the case of LLC topology, the main contributor of these switching losses is in fact Q_g .

Most of the time, a driving voltage of 12 V is applied to Sync Rec MOSFETs. Although 12 V is not necessarily the optimized driving voltage for Sync Rec MOSFETs, this driving voltage is very popular in server PSUs because it is readily available: there is no need to derive it from another voltage rail. Therefore, we decided to follow this trend for this demo board by driving the Sync Rec MOSFETs with 12 V.

This requirement for low Q_g puts extra-strain on MOSFET manufacturers, especially considering that Sync Rec MOSFETs need to exhibit at the same time a very low $R_{DS(on)}$. Such a feature was however possible for Infineon because of the new Infineon OptiMOS™ 40 V generation, whose gate charges have been significantly reduced in comparison with the previous generation.

Thirdly, the paralleled Sync Rec MOSFETs should turn on almost simultaneously.

This can be achieved because of a tightening of the voltage threshold $V_{GS(th)}$ range. For the new OptiMOS™ 40 V generation, the datasheet guarantees a very narrow $V_{GS(th)}$ range, with min. and max. values equal to 1.2 V and 2.0 V respectively.

Finally, the MOSFET package is critical for a variety of reasons.

The package should exhibit low parasitic inductances in order to confine its contribution to the V_{DS} overshoot to a strict minimum. This is even more critical in server applications using LLC topology, due to the limited headroom for the V_{DS} overshoot between the transformer secondary voltage (25 V) and the 90% derating (36 V max) or even 80% derating (32 V max) applied to the V_{DS} of the Sync Rec MOSFETs;

Moreover, due to the conflicting requirements for high power density and high current capability, the package should combine a minimum footprint with good power dissipation.

Because of the high current densities arising at the source pins, which can lead to electro-migration and thereafter destruction of the Sync Rec MOSFETs, the package should provide an enlarged source connection. While the first two sub-items are tackled by standard SuperSO8 packages, it is the addition of source-fused leads implemented in the new Infineon OptiMOS™ 40 V generation that reduces the high current densities above mentioned.

4 Board description

4.1 General Overview

Figure 2 is the top view, bottom view and the assembly of 600 W HB LLC demo board. Key components are: (1) heatsink assembly of primary side switches IPP60R190P6 (2) Resonant capacitor (3) LLC analog controller ICE2HS01G (4) Resonant inductor (5) Main transformer (6) PCB assembly of the auxiliary circuit with bias QR Flyback controller ICE2QR2280Z (7) Heatsink assembly for cooling the synchronous rectifiers (8) Output capacitors (9) Output inductor (10) Half-Bridge MOSFET gate driver 2EDL05N06PFG and (11) Synchronous Rectifier OptiMOS™ BSC010N04LS.

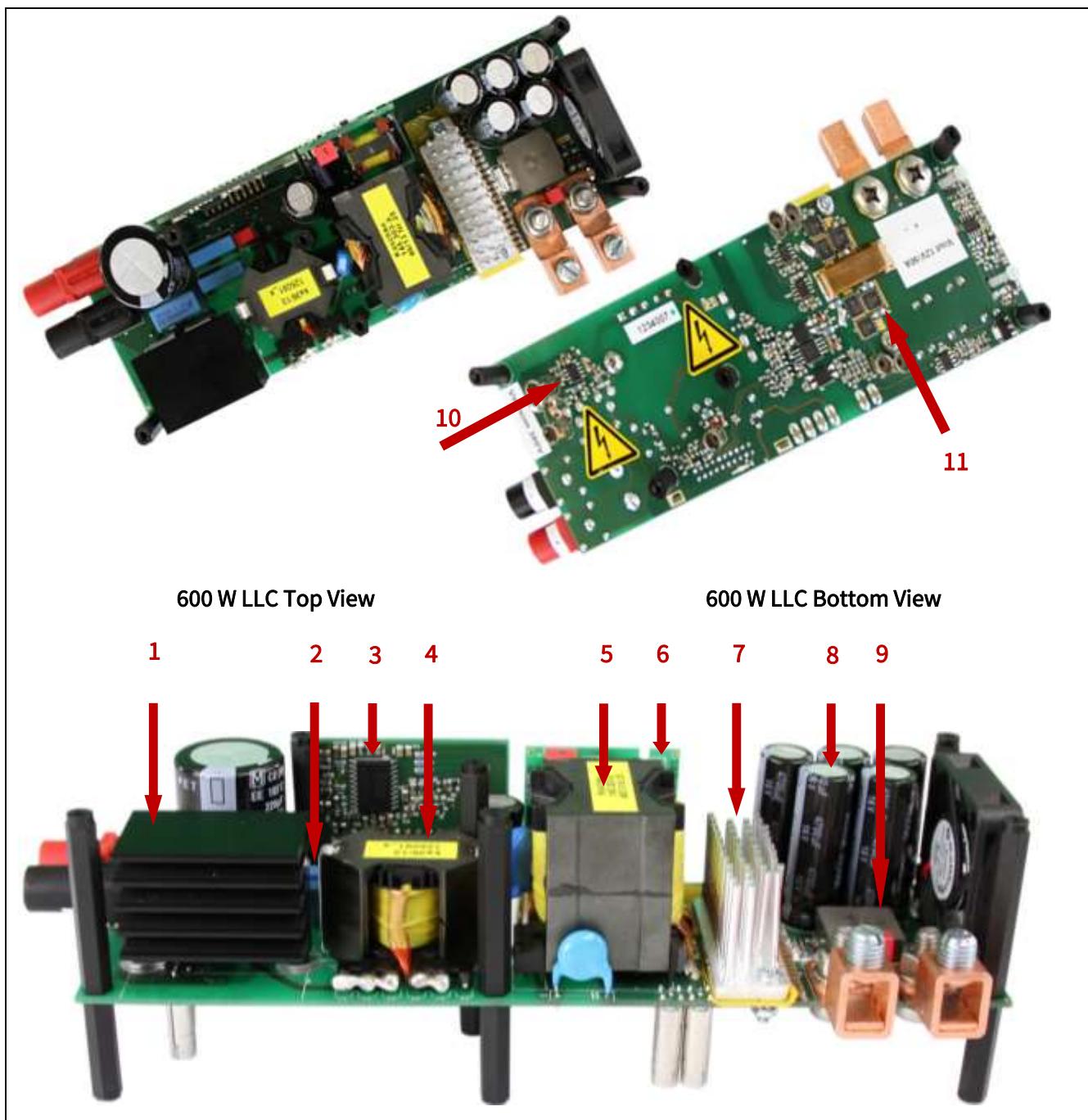


Figure 19 IFX 600 W LLC Demonstration Board

4.2 Infineon BOM

This HB LLC 600 W demo board is a full Infineon solution meeting the highest efficiency standard 80PPLUS® Titanium using the following parts:

4.2.1 Primary HV MOSFETs CoolMOS™ IPP60R190P6

The 600 V CoolMOS™ P6 is a new addition to Infineon's market leading high voltage CoolMOS™ portfolio. It is the seventh technology platform of high voltage power MOSFETs designed according to the revolutionary superjunction principle. This new and highly innovative product family is designed to enable higher system efficiency whilst being easy to design in.

In LLC application, converter is in resonant operation with guaranteed ZVS even at a very light load condition. Switching loss caused by E_{oss} during turn-on can be considered negligible in this topology. With this consideration, CoolMOS™ P6 offers superior price/performance ratio with low FOMs ($R_{on} \cdot Q_g$ and $R_{on} \cdot Q_{oss}$), which means that MOSFET switching transitions can happen in a shorter dead time period. This will result in lower turn-off losses, pushing further the efficiency. The following are the additional features and benefits of CoolMOS™ P6 making it suitable and advantageous for resonant switching topologies like LLC:

1. Reduced gate charge (Q_g) improves the efficiency especially in light load condition due to a lower driving capability requirement
2. Lower Q_{oss} reduces the turn-on and turn-off time for a better usage of ZVS window
3. Optimized gate threshold voltage (V_{th}) lowers the turn-off losses in soft switching applications
4. Optimized integrated R_g ensures an optimum balance between efficiency and good controllability of the switching behavior
5. Improved dv/dt compared to previous technologies assures high robustness.
6. Good body diode ruggedness
7. Outstanding reliability with proven CoolMOS™ quality

4.2.2 LLC Analog Controller ICE2HS01G

ICE2HS01G is Infineon's 2nd generation half-bridge LLC controller designed especially for high efficiency half-bridge or full-bridge LLC resonant converter with synchronous rectification (SR) control for the secondary side. With its new driving techniques, the synchronous rectification can be realized for LLC converter operated with secondary switching current in both CCM and DCM conditions. No special synchronous rectification controller IC is needed at the secondary side. The maximum switching frequency is supported up to 1 MHz. Apart from the patented SR driving techniques, this IC provides very flexible design and integrates full protection functions as well. It is adjustable for maximum/minimum switching frequency, soft-start time and frequency, dead time between primary switches, turn-on and turn-off delay for secondary SR MOSFETs. The integrated protections include input voltage brownout, primary three-levels over current, secondary over load protection and no-load regulation. It also includes a burst mode function which offers an operation with low quiescent current maintaining high efficiency at low output load while keeping output ripple voltage low.

4.2.3 HB Gate Drive 2EDL05N06PFG

Developers of consumer electronics and home appliances strive continuously for higher efficiency of applications and smaller form factors. One area of interest in power supply design is the switching behavior and power losses of new power MOSFETs, such as the latest generations of CoolMOS™ with dramatically reduced gate charges, as dedicated driver ICs can optimize it.

The 2EDL05N06PFG IC is one of the drivers from Infineon's 2EDL EiceDRIVER™ Compact 600 V half bridge gate driver IC family with monolithic integrated low-ohmic and ultrafast bootstrap diode. Its level-shift SOI technology supports higher efficiency and smaller form factors of applications. Based on the used SOI-technology there is an excellent ruggedness on transient voltages. No parasitic thyristor structures are present in the device. Hence, no parasitic latch-up may occur at all temperature and voltage conditions. The outputs of the two independent drivers are controlled at the low-side using two different CMOS resp. LSTTL compatible signals, down up to 3.3 V logic. The device includes an under-voltage detection unit with hysteresis characteristic, which is optimized for either IGBT or MOSFET. 2EDL05N06PF (DSO-8) and 2EDL05N06PJ (DSO-14) are driver ICs with undervoltage-lockout for MOSFETs. These two parts are recommended for Server/Telecom SMPS, Low-Voltage Drives, e-Bike, Battery Charger and Half Bridge Based Switch Mode Power Supply Topologies.

4.2.4 Bias QR Flyback Controller ICE2QR2280Z

ICE2QRxxxx is a second generation quasi-resonant PWM CoolSET with power MOSFET and startup cell in a single package optimized for off-line power supply applications such as LCD TV, Notebook Adapter and Auxiliary/Housekeeping Converter in SMPS. The digital frequency reduction with decreasing load enables a quasi-resonant operation until very low load. As a result, the system average efficiency is significantly improved compared to conventional solutions. The active burst mode operation enables ultra-low power consumption at standby mode operation and low output voltage ripple. The numerous protection functions give a full protection of the power supply system in failure situation. Main features of ICE2QR2280Z which make it suitable as an auxiliary converter of this LLC demonstration board are:

- High voltage (650 V/800 V) avalanche rugged CoolMOS™ with startup cell
- Quasi-resonant operation
- Load dependent digital frequency reduction
- Active burst mode for light load operation
- Built-in high voltage startup cell
- Built-in digital soft-start
- Cycle-by-cycle peak current limitation with built-in leading edge blanking time
- Foldback Point Correction with digitalized sensing and control circuits
- V_{CC} undervoltage and overvoltage protection with Autorestart mode
- Over Load /open loop Protection with Autorestart mode
- Built-in Over temperature protection with Autorestart mode
- Adjustable output overvoltage protection with Latch mode
- Short-winding protection with Latch mode
- Maximum on time limitation
- Maximum switching period limitation

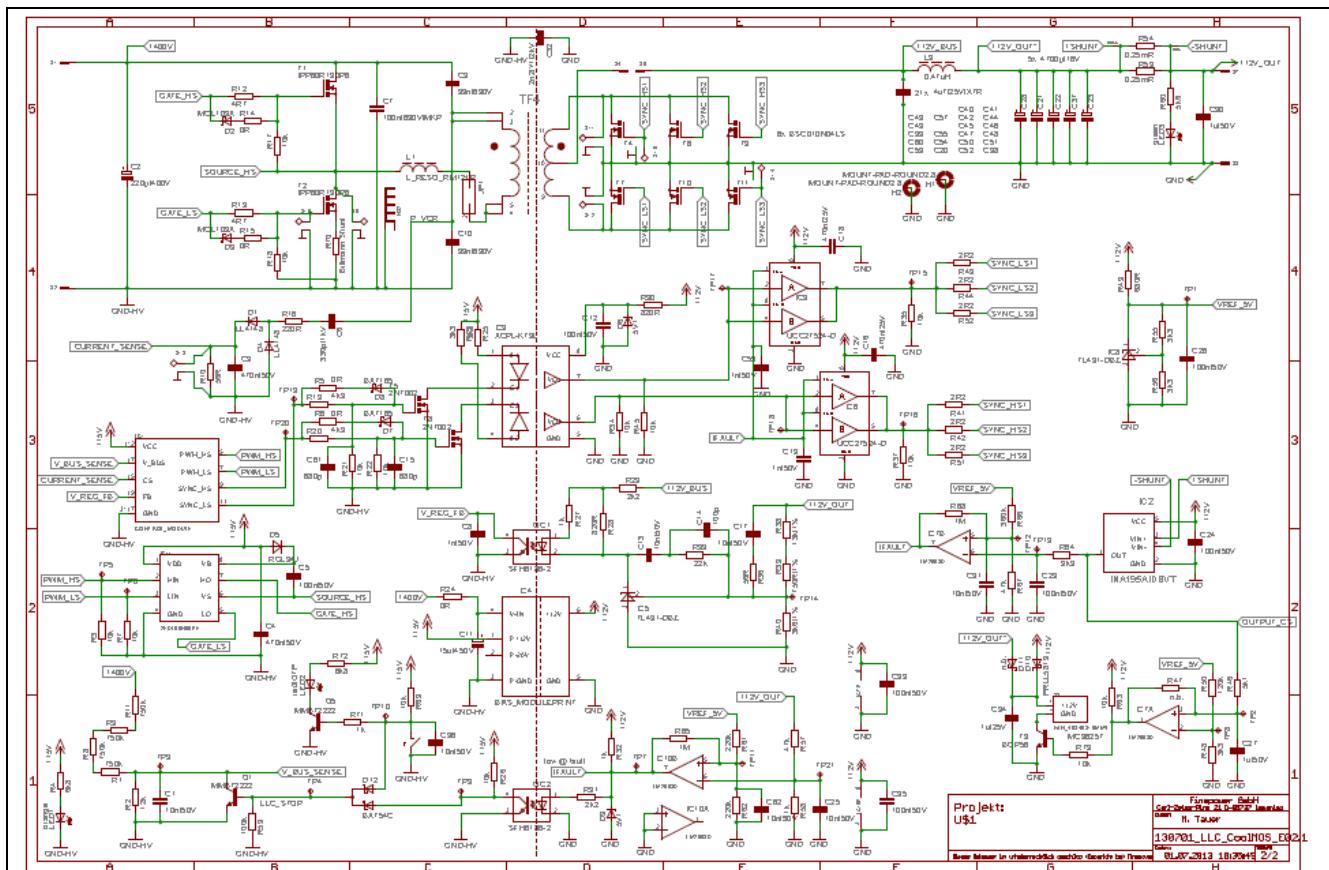
4.2.5 SR MOSFETs OptiMOS™ BSC010N04LS

For the synchronous rectification stage, the selected device is BSC010N04LS, from the latest OptiMOS™ 40 V family. SR is in fact naturally the best choice in high efficiency designs of low output voltage and high output current LLC, as in our case. In applications that target high efficiency both at light and heavy loads – such as 80PLUS® Titanium- while often requiring high power densities, it is critical to select SR MOSFETs that combine following key characteristics:

- Very low $R_{DS(on)}$: BSC010N04LS provides the industry's first $1\text{ m}\Omega$ 40 V product in SuperSO8 package
- Low gate charge Q_g , which is important in order to minimize driving losses, with benefits on light load efficiency
- Very tight $V_{GS(th)}$ range: in fact, in case of paralleling this allows the MOSFETs to turn-on almost simultaneously. Selected OptiMOS™ offer very close min. and max. of $V_{GS(th)}$, respectively 1.2 and 2 V
- Monolithically integrated Schottky like diode, in order to minimize the conduction losses on it
- Package; BSC010N04LS in SuperSO8 with source fused leads is able to address all the typical crucial requirements for a suitable SR MOSFET package:
 - Minimizing parasitic inductances
 - Combining compact footprint with good power dissipation
 - Enlarged source connection in order to minimize electro-migration occurrence.

4.3 Board Schematics

4.3.1 Mainboard Schematic



4.3.2 Controller Board Schematic

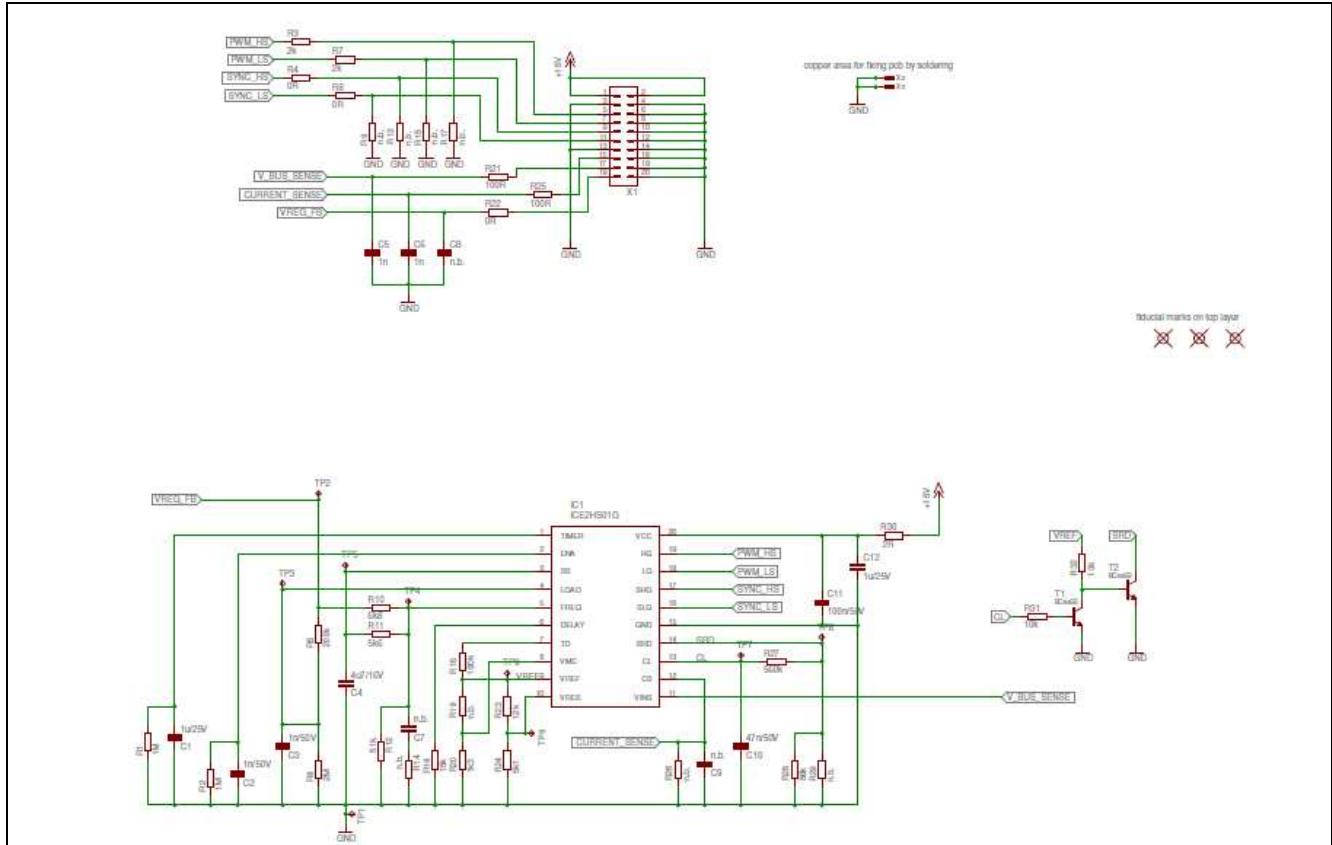


Figure 21 Controller Board Schematic

4.3.3 Bias Board Schematic

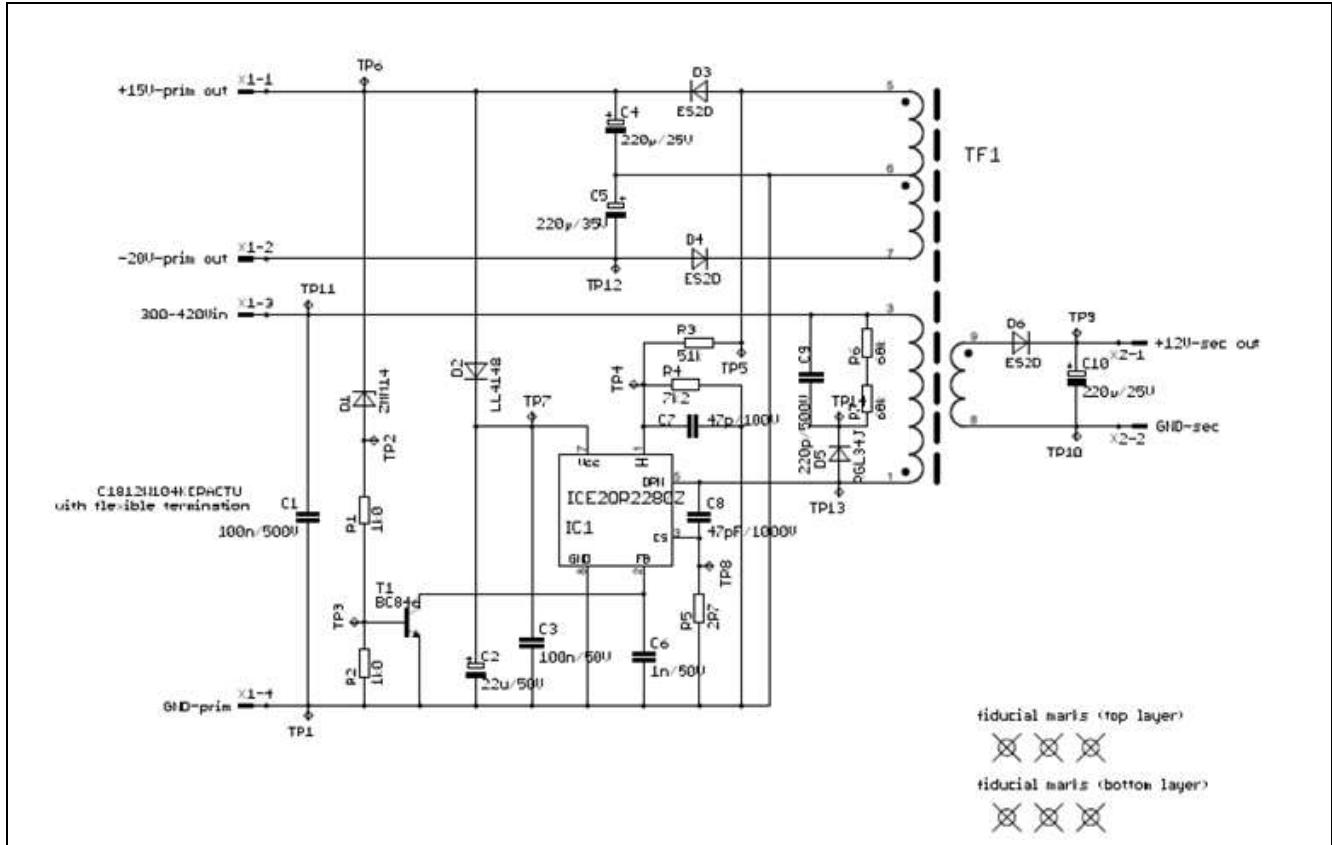


Figure 22 Bias Board Schematic

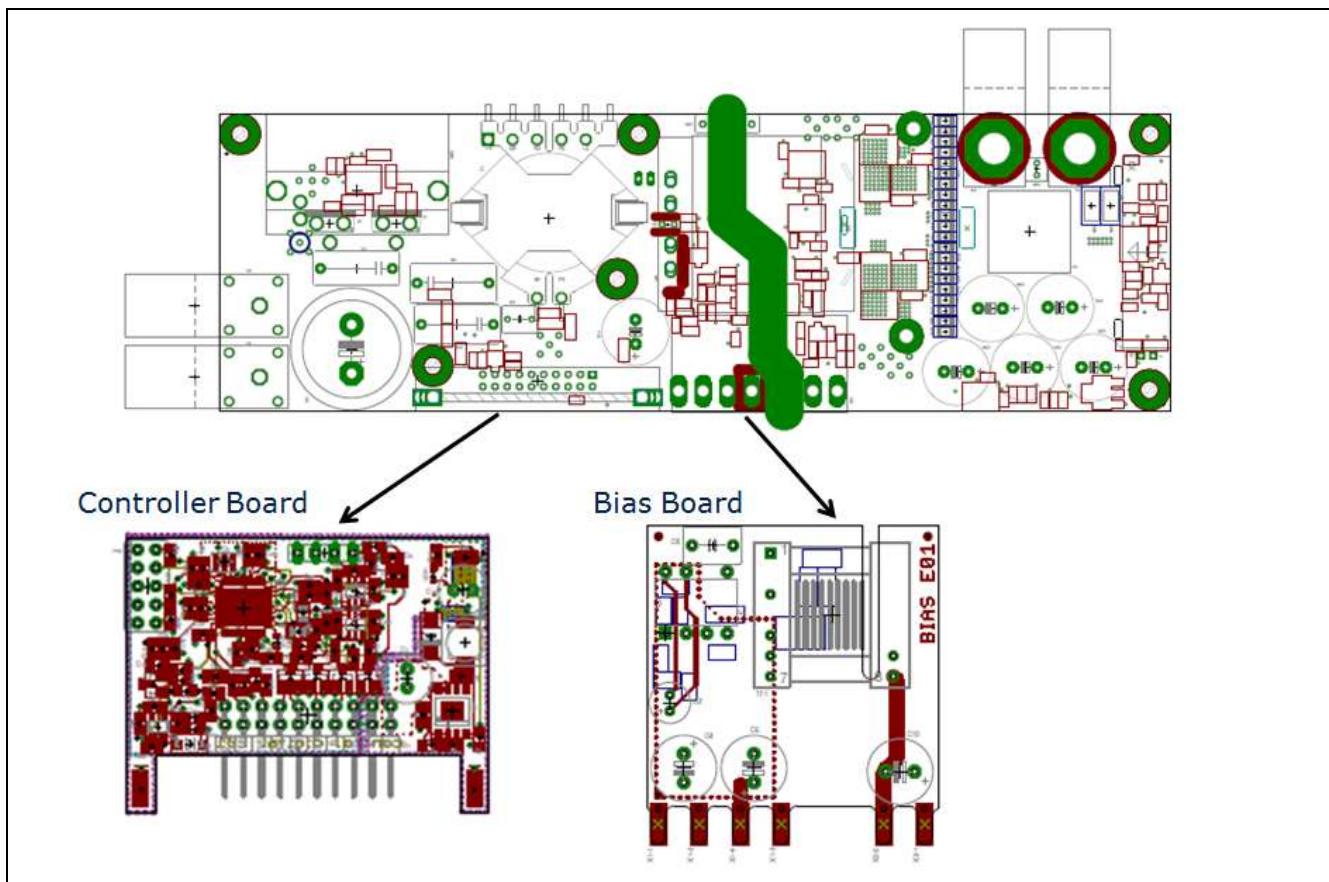


Figure 23 Mainboard PCB with Controller – and Bias Board

4.4 Critical LLC Operation - Hard Commutation

In the LLC converter, hard commutation of the body diode might occur during the start-up, burst mode, overload and short circuit condition. The occurrence of this condition can be prevented in the design by using a proper control technique, a correct selection of resonant components and a proper setting of the minimum and maximum operating frequency. Hard commutation happens in LLC during the commutation period of the body diode. During this time, resonant inductor current is flowing through body diode of the MOSFET creating ZVS condition upon this MOSFET's turn-on. When the current is not able to change its direction prior to the turn-on of the other MOSFET, more charges will be stored in the P-N junction of that MOSFET. When the other MOSFET turns on, a large shoot-through current will flow due to reverse-recovery current of the body diode. This results in high reverse recovery peak current I_{RRM} and high reverse recovery dV/dT , which sometimes could lead into MOSFET breakdown.

In this 600 W LLC analog controlled demonstration board, only the burst mode condition has the tendency of undergoing hard commutation. In Figure 24, hard commutation at burst mode is minimal, so that IPP60R190P6 is able to withstand without any problem.

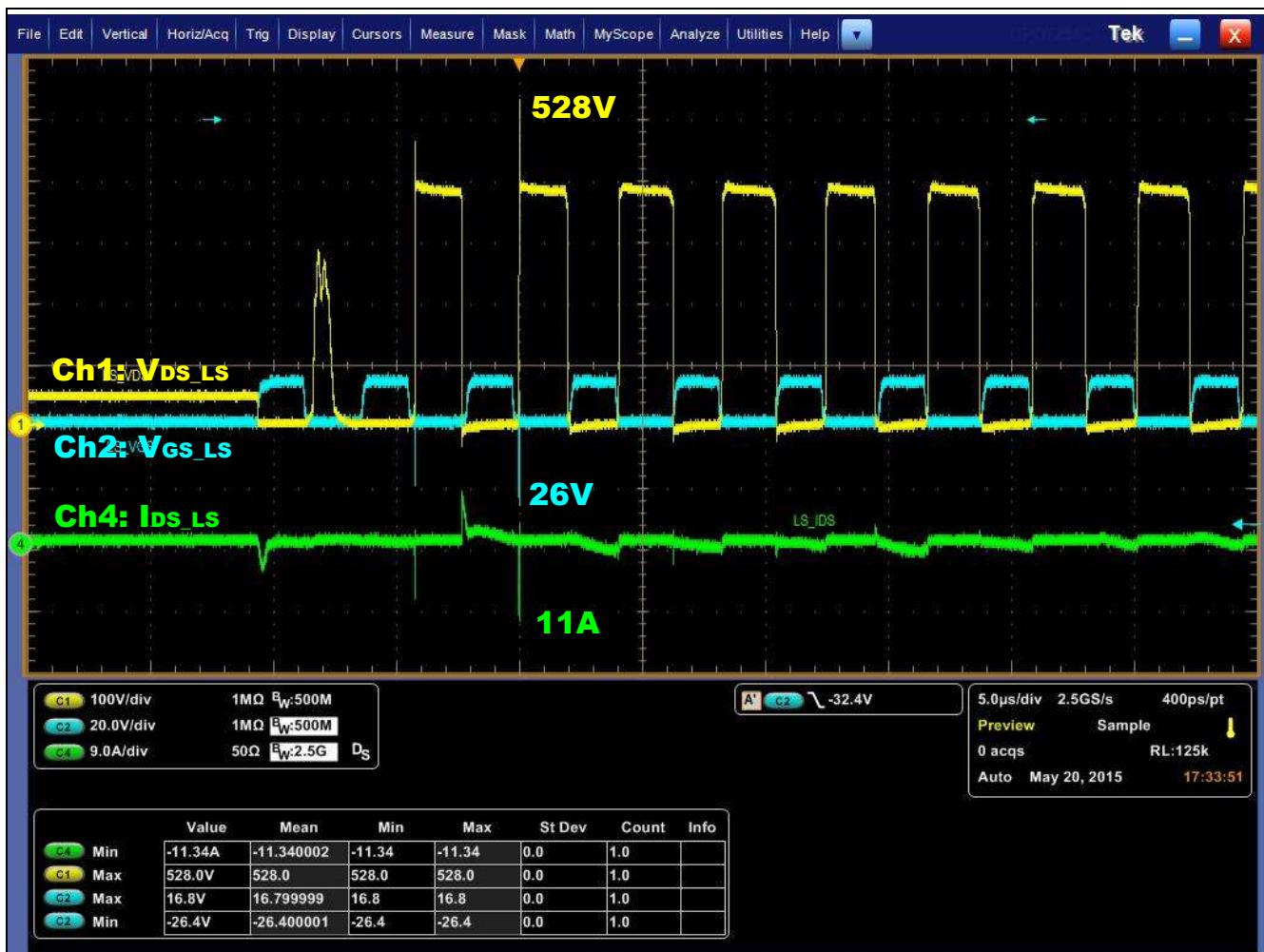


Figure 24 Hard Commutation During Burst Mode Operation, V_{DS_pk} , $V_{GS_max/min}$ and I_{RMM}

The voltage spike on the gate V_{GS} and drain V_{DS} can be influenced by varying both turn-on and turn-off gate resistors in the range of 10 ohm. This increased R_g will not affect the efficiency, thanks to the P6 technology switching behavior.

It is important to highlight that in the present 600 W Analog LLC Demonstration board there is no other observed hard commutation event, neither during start-up, nor at output short-circuit conditions.

4.5 ZVS Behavior Analysis

Nearly full ZVS is achieved on the entire output load range as shown in Figure 25.

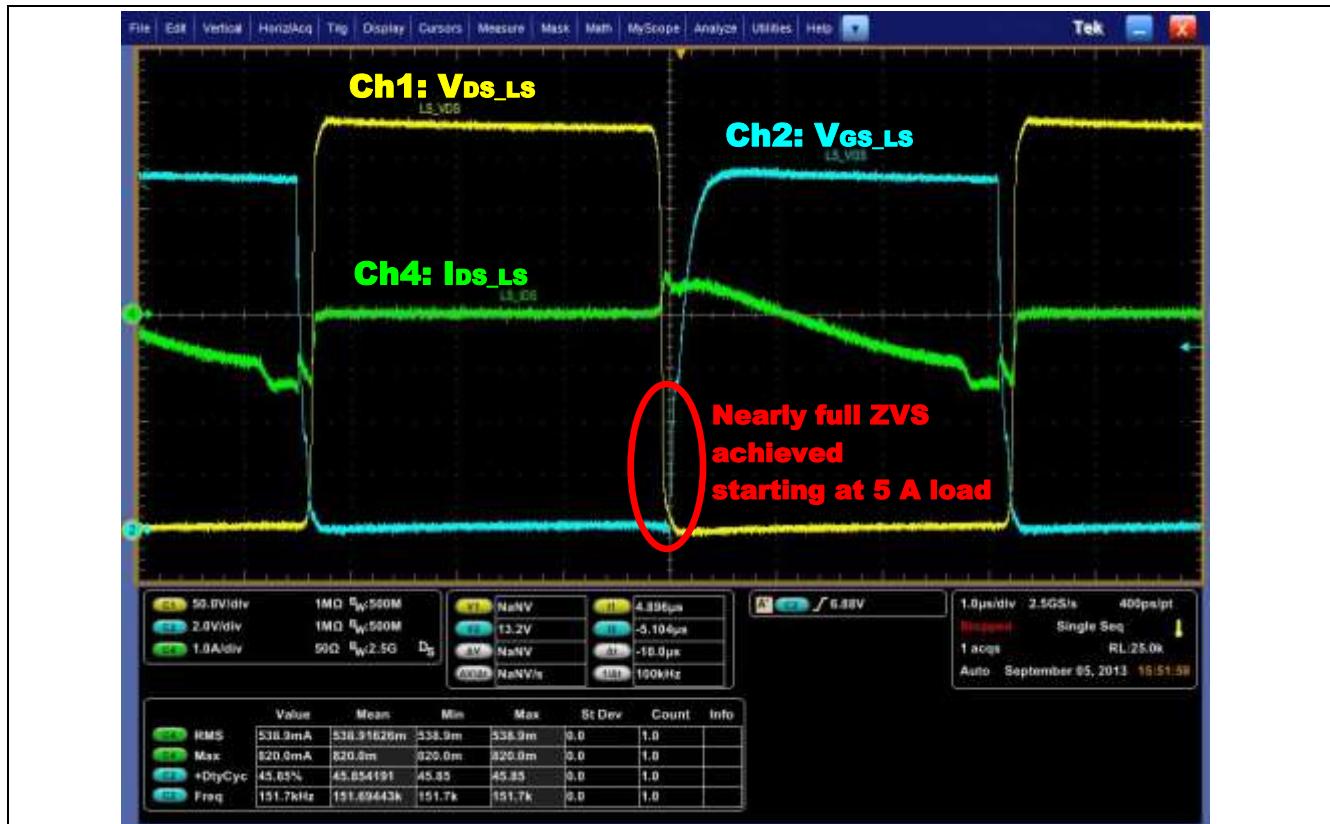


Figure 25 Nearly Full Zero Voltage Switching (ZVS) starting at 5 A load

4.6 Burst Mode Operation

At no load or a very light load condition, LLC controller provides frequency approaching to its maximum setting. In this condition, in order to still achieve full ZVS, magnetizing current should be high enough to discharge the output capacitances. Due to magnetizing current limitation, switching loss especially turn-off loss is relatively high if the devices, will continue to switch at the highest frequency. In order to overcome this phenomenon, burst mode function is enabled and implemented. This results in effective lower switching losses and driving losses, because of the low burst frequency.

Additionally, this helps to achieve regulation even at no load condition, preventing the problems often seen in LLC in that condition. These regulation problems are typically due to parasitic components like the primary-secondary main transformer coupling capacitance and the SR MOSFETs output capacitance. The combination of these factors generates the so-called third resonant frequency in the LLC gain curve, making the converter virtually not controllable at no load. The burst mode allows overcoming this problem, by limiting the unwanted primary to secondary power transfer, due to the above-mentioned parasitic effects.

For further details about this tricky operation of the LLC converter, please refer to the specific literature [7]. The waveforms in Figure 26 illustrate the Burst Mode technique applied in our 600 W LLC demo board.

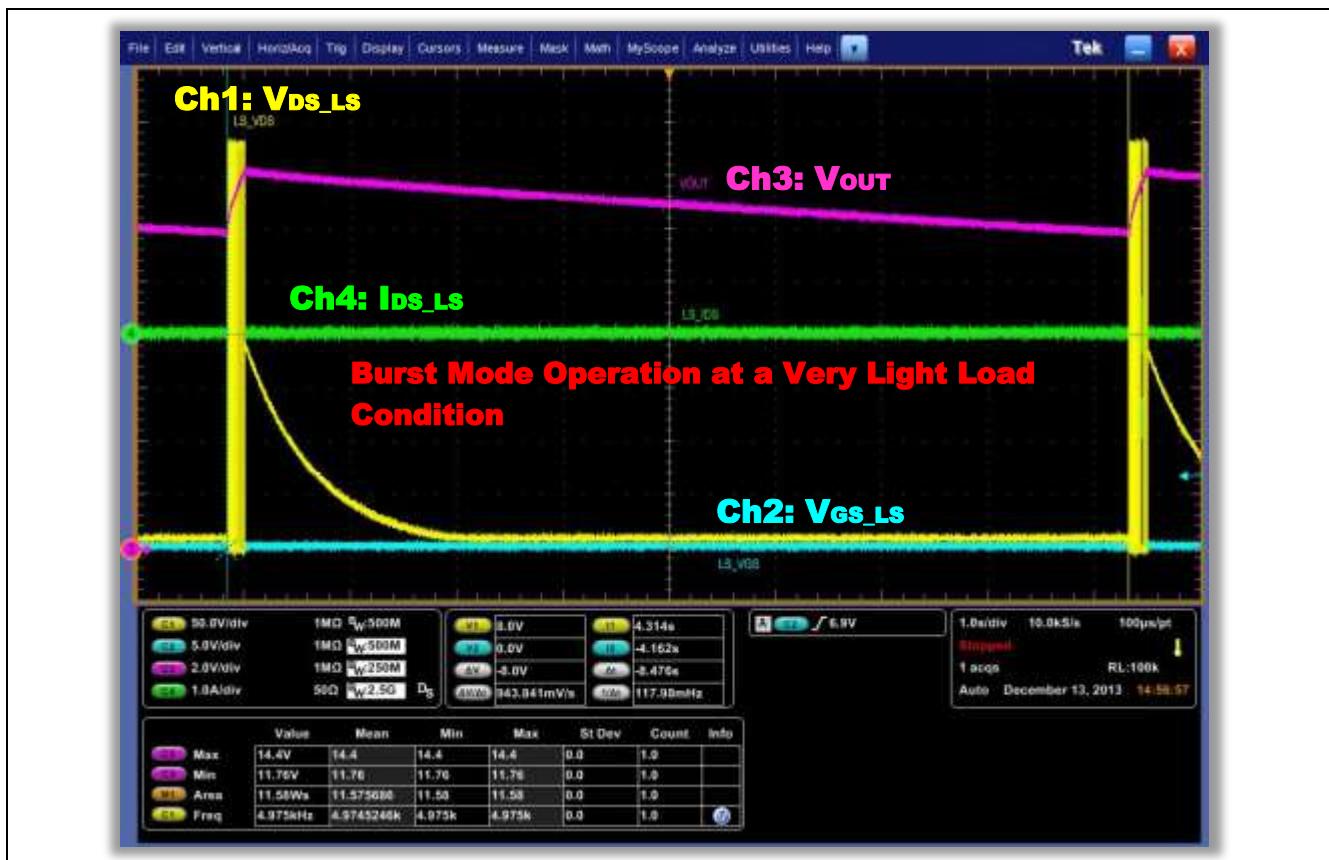


Figure 26 Burst Mode Operation at No-Load and Very Light Load Condition

4.7 Efficiency

4.7.1 80+ Titanium Efficiency Target

Figure 27 shows the efficiency measurement done on the 600 W LLC demo board with reference to the 80+ Titanium Standard Efficiency. As well known, the Titanium Standard fixes the minimum efficiency requirement at the three most important load conditions in a Computing/Server Application, 10%, 50% and 100%.

The combination of proper converter design (resonant tank, transformer) and HV device selection allows to fulfil with reasonable margin the efficiency targets especially in the range 10-40% load.

Proper selection of SR LV device and secondary side design more influences the performance in the range 40-100% load.

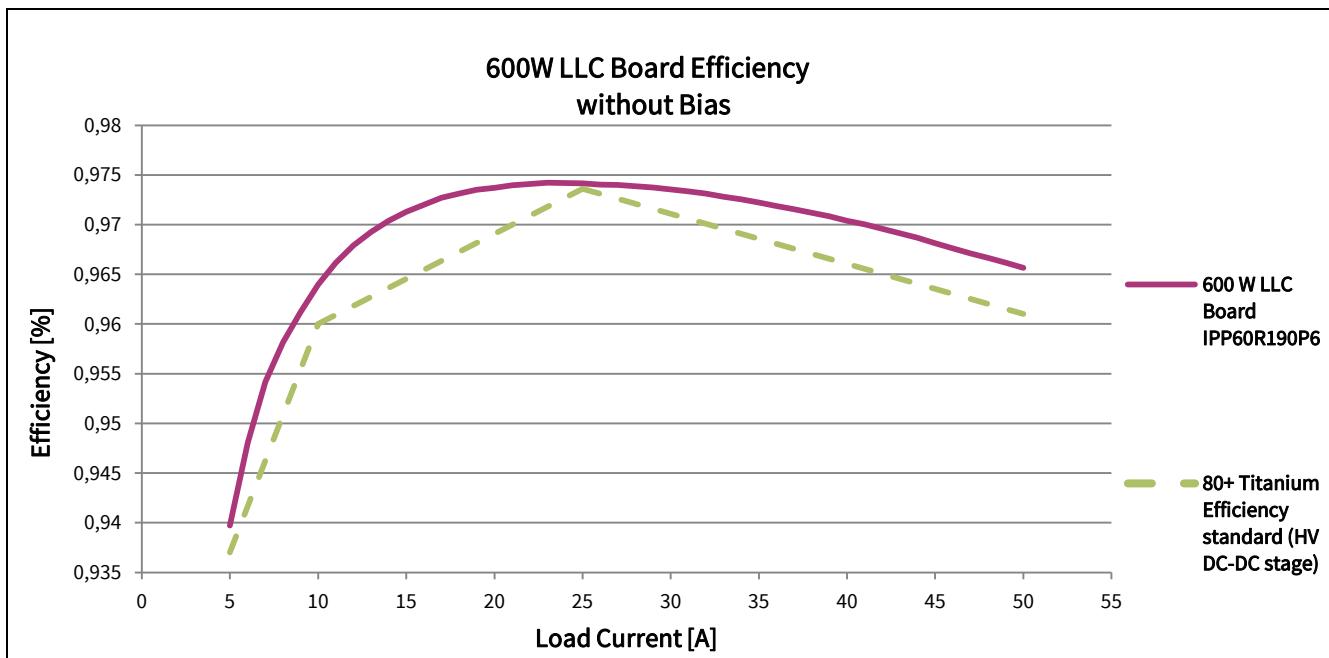


Figure 27 IFX 600 W LLC Demonstration Board Efficiency vs Titanium STD Efficiency

The measurement has been done in a fully automated setup, shown in Fig. 29. The total accuracy of the measurement is in the $\pm 0.1\%$ range.

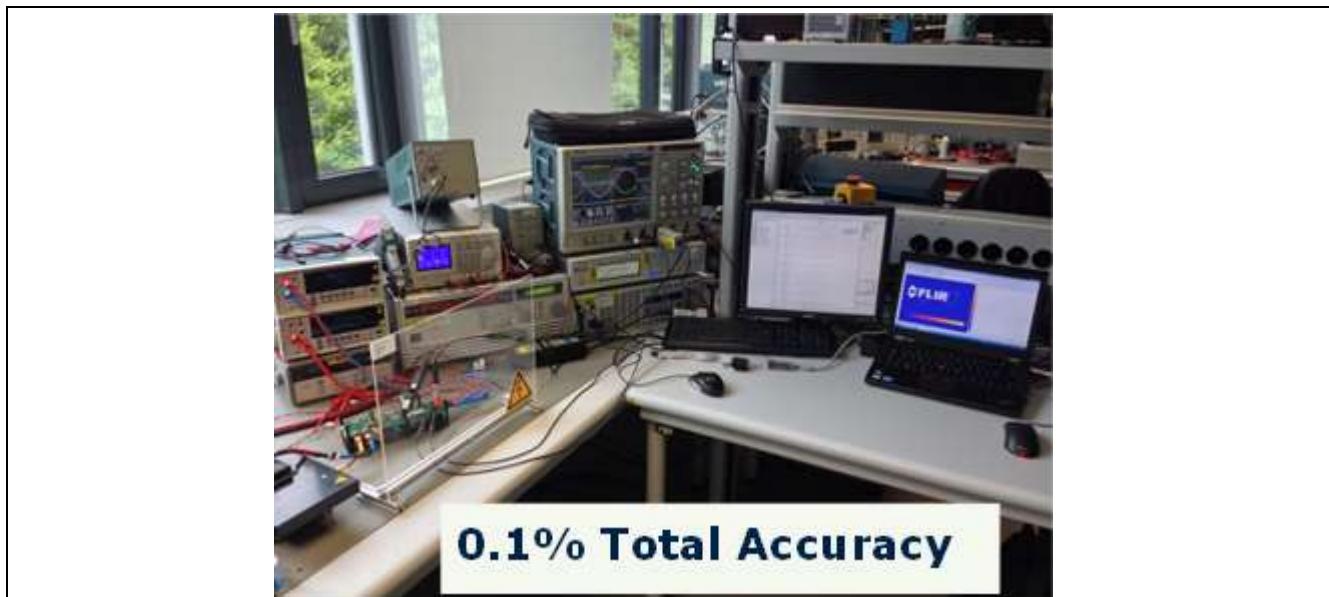


Figure 28 IFX 600 W LLC Automated Efficiency Measurement Setup

4.7.2 Losses Breakdown

In the graphs below, you can find the losses breakdown among the different components of the demo board.

You can see how the contribution of Primary MOSFETs is progressively increasing from light to heavy load. On the other side, the contribution of the main transformer is important at 10% load, but it tends to decrease at higher load: this is mainly due to the core losses (higher at light load due to higher switching

frequency) and the magnetizing inductance, which is almost constant and independent on the load. In fact, this feature allows the HB LLC topology to easily achieve ZVS down to very light load and definitely differentiates the HB LLC topology from other soft switching approaches, like the ZVS Phase Shift Full Bridge.

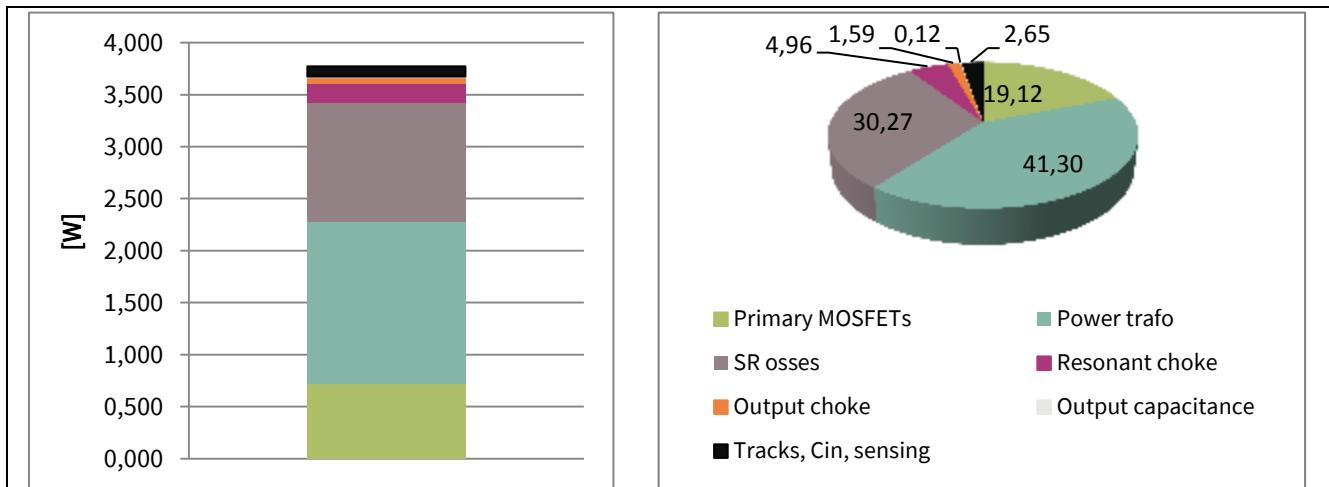


Figure 29 10% Load Losses Breakdown and Spread (@10% P_{max} and 100 kHz)

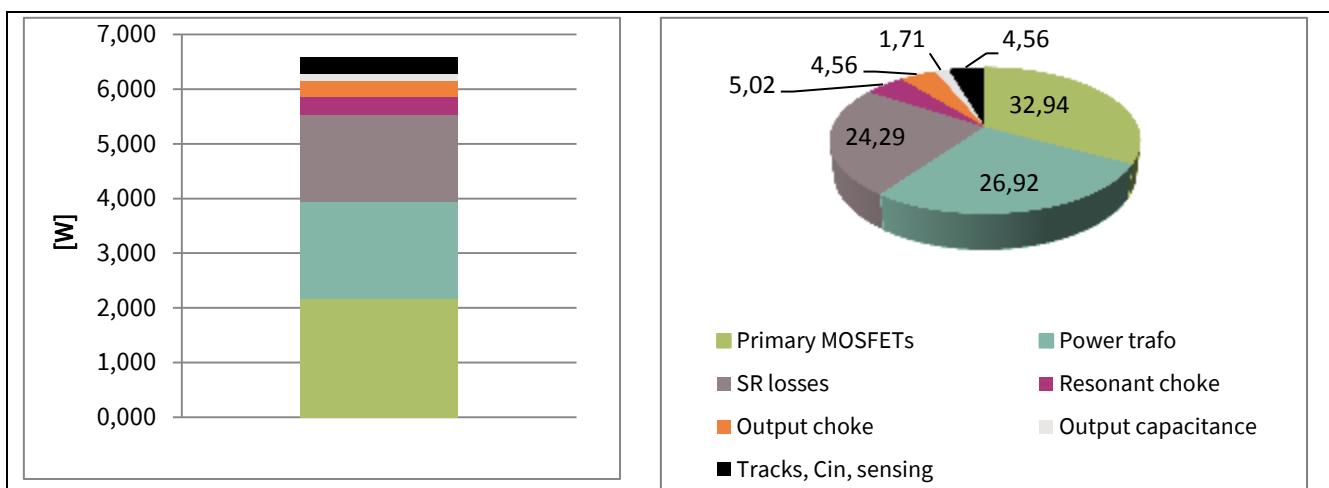


Figure 30 50% Load Losses Breakdown and Spread (@50% P_{max} and 100 kHz)

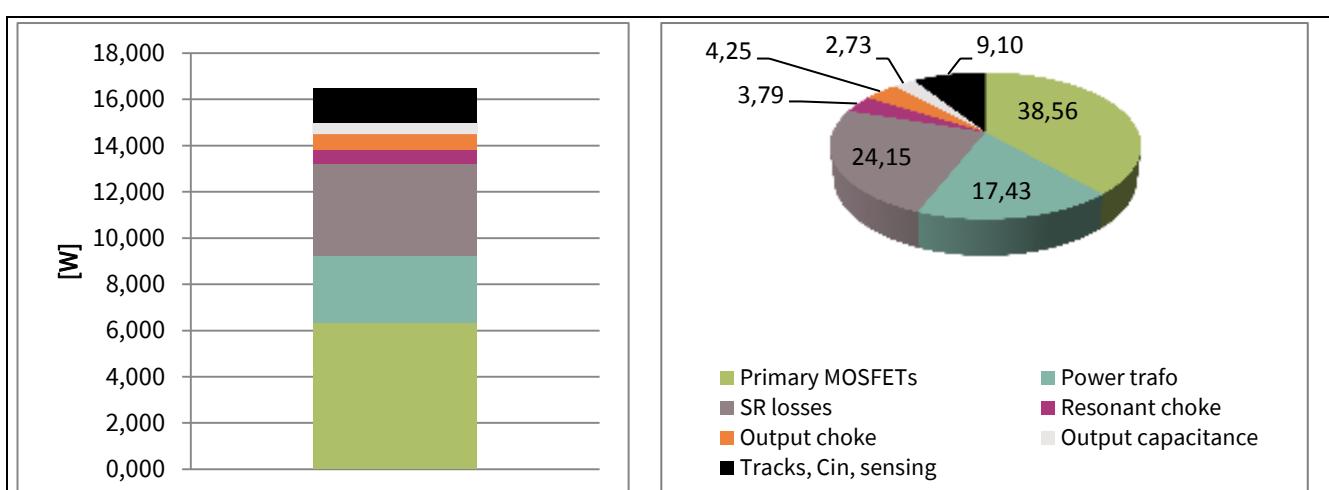


Figure 31 100% Load Losses Breakdown and Spread (@100% P_{max} and 100 kHz)

5 Test/Power-up Procedure

Test	Test procedure	Condition
1. Auxiliary Circuit Turn-On	Apply 30 V _{dc} on the input.	V _{in} : ~30 V _{dc}
		Orange LED will light up
2. LLC Converter Turn-On	Apply 350 V _{dc} Converter will give V _{out} =12 V _{dc}	V _{in} : 350 V _{dc}
		V _{out} : 12 V
3. Operational switching frequency	Using voltage probe, monitor switching frequency at following test conditions:	V _{in} : 380 V _{dc}
	@5 A Output Load 10% Load - ~ 155 kHz*	I _{out} : 5 A
	@25 A Output Load 50% Load - ~ 142 kHz*	I _{out} : 25 A
	@50 A Output Load 100% Load - ~ 132 kHz*	I _{out} : 50 A
	(*measure freq. at "Pri_LS_VGS"- connector)	
	[* +/- 10 kHz]	
4. Fan enable	Switch the load from 50 A to 5 A. Increase the output load current from 11-14 A, fan should turn on.	V _{in} = 380 V _{dc}
		I _{out} = 5 A
		► Fan is off
		V _{in} = 380 V _{dc}
		I _{out} = 11-14 A
		► Fan is on
5. Switch off Input Start-up at No load	Switch off the Input	V _{in} = 0 V _{dc}
		I _{out} = 0 A
	Switch at 380 V _{dc} on no load output. Operation should be in burst mode.	V _{in} = 380 V _{dc}
		I _{out} = 0 A
		V _{out} = 11,5 – 12,5 V _{dc}
6. Switch off Input; Start-up at Full load	Switch off the Input	V _{in} = 0 V _{dc}
		I _{out} = 0 A
	Apply 380 V _{dc} with full load @50 A output. V _{out} is in between 11.8 – 12.2 V _{dc} * (*measure on the board-connector)	V _{in} = 380 V _{dc}
		I _{out} = 50 A
7. Running No Load -> Output Short Circuit	Switch off load from 380 V _{dc} 50 A to 380 V _{dc} 0 A.	V _{in} = 380 V _{dc}
	Short circuit the load using the short circuit function of the e-load. Converter should latch.	(after short circuit) V _{out} = 0 V _{dc}
		I _{out} = 0 A

8. Switch off Input & remove short circuit	Switch off the Input.	$V_{in} = 0 \text{ V}_{dc}$
9. Running Full Load -> Over Current Protection	Remove short circuit function on the load. Apply 380 V _{dc} 50 A with full load output. Increase the current on the output 1A each step until the converter goes into protection starting from 50 A. OCP occurs between 55 A and 62 A.	$I_{out} = 0 \text{ A}$ $V_{in} = 380 \text{ V}_{dc}$ $I_{out} = 50 \text{ A}$ OCP = between 55 A – 62 A
10. Running Full Load -> Output Short Circuit	Apply 380 V _{dc} 50 A with full load output. Short circuit the load using the short circuit functions of the load. Converter should latch.	$I_{out} = 0 \text{ A}$ $V_{in} = 380 \text{ V}_{dc}$ $I_{out} = 50 \text{ A}$ <i>(after short circuit) $V_{out} = 0 \text{ V}_{dc}$</i>
11. Switch off Input; Start- Up -> Output Short Circuit	Switch off the Input. Apply 380 V _{dc} with output load short circuit. <i>Converter should be in hiccup/latch mode.</i>	$V_{in} = 0 \text{ V}_{dc}$ $I_{out} = 0 \text{ A}$ $V_{in} = 380 \text{ V}_{dc}$ $I_{out} = \text{short circuit}$ $V_{out} = 0 \text{ V short circuit (hiccup/latch)}$
12. Switch off Input & remove short circuit	Switch off the Input. Remove short circuit function on the load.	$V_{in} = 0 \text{ V}_{dc}$ $I_{out} = 0 \text{ A}$
13. Dynamic Loading	Apply 380 V _{dc} . Set the electronic load to dynamic loading mode with the following settings: CCDH1: $I_{out} 5 \text{ A}$ CCDH2: $I_{out} 50 \text{ A}$ Dwell time: 10 ms Load slew rate: 1 A/ μs	$V_{in} = 380 \text{ V}_{dc}$ $I_{out} = 5 \text{ A} \dots 50 \text{ A}$ $V_{out} = 11,5 - 12,5 \text{ V}_{dc}$

6 Useful material and links

In the following Links you can find more detailed information about the used devices from Infineon and the magnetic components.

- Primary HV MOSFETs CoolMOS™ IPP60R190P6:

https://www.infineon.com/dgdl/Infineon-IPX60R190P6-DS-v02_01-en.pdf?fileId=db3a30433f2e70c5013f37c80e24240f

- LLC analog controller ICE2HS01G

http://www.infineon.com/dgdl/ICE2HS01G_PDS_v2.1_20110524_Public.pdf?folderId=db3a304412b407950112b408e8c90004&fileId=db3a30432a40a650012a458289712b4c

HB Gate Drive 2EDL05N06PFG

http://www.infineon.com/dgdl/Infineon-2EDL05x06xx-DS-v02_05-EN.pdf?fileId=db3a30433e30e4bf013e3c649ffd6c8b

- Bias QR Flyback controller ICE2QR2280Z

http://www.infineon.com/dgdl/Datasheet_ICE2QR2280Z_v21_20110830.pdf?folderId=db3a304412b407950112b408e8c90004&fileId=db3a30432a7fedfc012a8d8038e00473

- SR MOSFETs OptiMOS™ BSC010N04LS

http://www.infineon.com/dgdl/BSC010N04LS_rev2.0.pdf?folderId=db3a304313b8b5a60113cee8763b02d7&fileId=db3a3043353fdc16013552c1c63647c4

- Main Transformer and Resonant Choke ferrite cores

<http://en.tdk.eu/blob/519704/download/2/ferrites-and-accessories-data-book-130501.pdf>

7 References

- [1] T. Fujihira: "Theory of Semiconductor Superjunction Devices", Jpn. J. Appl. Phys., Vol.36, pp. 6254-6262, 1997
- [2] Sam Abdel Rahman: "Resonant LLC Converter: Operation and Design: 250 W 33Vin 400 V_{out} Design Example", Infineon Technology AN 2012
- [3] Alois Steiner, Francesco Di Domenico and others: "600 W Half Bridge LLC Evaluation Board with 600 V CoolMOS™ C7", Infineon Technologies AN 2015
- [4] Lawrence Lin, Gary Chang: "Consideration of Primary side MOSFET Selection for LLC topology", Infineon Technologies AN 2014
- [5] Liu Jianwei, Li Dong: "Design Guide for LLC Converter with ICE2HS01G", Infineon Technologies AN V1.0, July 2011
- [6] Alois Steiner, Johnald Catly: "600 V CoolMOS P6: 600 V Superjunction MOSFET for Server, Telecom , PC Power and Consumer
- [7] Jae-Hyun Kim, Chong-Eun Kim and others: "Analysis for LLC Resonant Converter Considering Parasitic Components at Very Light Load Condition", 8th International Conference on Power Electronics, 2011 - Korea

8 List of abbreviations

BOM.....	Bill Of Materials
C_{GD}	Internal Gate Drain Capacitance $C_{GD}=C_{rss}$
C_{iss}	input capacitance $C_{iss}=C_{GS}+C_{GD}$
$C_{o(er)}$	effective output capacitance
C_r	resonant capacitance
di/dt	steepness of current slope at turn off / turn on
DUT	device under test
dv/dt	steepness of voltage slope at turn off / turn on
E_{off}	energy losses at switch off
E_{on}	energy losses loss at switch on
E_{oss}	stored energy in output capacitance (C_{oss}) at typ. $V_{DS}=400$ V
FHA.....	First Harmonic Approximation Method
FOM.....	Figures of Merit
f_r	resonant frequency
I_D	drain current
I_{RMS}	effective root mean square current
I_{mag}	magnatizing current
$I_{m,pk}$	peak magnetizing current
K.....	gain factor
L_r	resonant inductance
L_m	magnetizing inductance
m	inductance factor
N_p	primary winding
N_s	secondary winding
n	transformer turn ratio
MOSFET.....	metal oxide semiconductor field effect transistor
P_{cond_SR}	synchronous rectification conduction losses
PFC.....	power factor correction
PNP.....	bipolar transistor type (pnp vs. npn)
Q_{oss}	Charge stored in the C_{oss}
Q	quality factor
R_{ac}	total equivalent resistor
$R_{DS(on)}$	drain-source on-state resistance
$R_{g,tot}$	total gate resistor
R_o	output resistor
R_{th}	thermal resistance
t_{dead}	dead time
t_{ecs}	early channel shut down time
V_{DS}	drain to source voltage, drain to source voltage
$V_{gs,th}$	drain to source threshold voltage
V_{O_AC}	output voltage, alternating current

V_{in_AC}	input voltage, alternating current
V_{in_nom}	nominal input voltage
V_{out_nom}	nominal output voltage
ZCS	zero current switching
ZVS	zero voltage switching

Revision History

Major changes since the last revision

Page or Reference	Description of change
--	First Release

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