12W 12V SMPS Demo Board with ICE2QR4780G

AN-DEMO-2QR4780G

About this document

Scope and purpose

This document is an engineering report that describes universal input 12 W 12 V off-line flyback converter using Infineon Quasi-Resonant CoolSET™ ICE2QR4780G which offers high efficiency, very low standby power, wider V_{VCC} operating range and various mode of protections for a high reliable system. This demonstrator board is designed for users who wish to evaluate the performance of ICE2QR4780G in ease of use.

Intended audience

This document is intended for power supply design/application engineer, students, etc.) who wish to design low cost and high reliable systems of off-line Switched Mode Power Supply (SMPS) for enclosed adapter, blu-ray/DVD player, set-top box, game console, smart meter, auxiliary power supply of white goods, PC, server, etc.

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Abstract

1 Abstract

This application note is an engineering report of 12 W 12V demo board designed in a quasi resonant flyback converter topology using ICE2QR4780G Quasi-resonant CoolSET™ .The target applications of ICE2QR4780G are set-top box, portable game controller, Blue-Ray/DVD player, netbook adapter and auxiliary power supply of PC, printer, TV, home theater/audio system, etc. With the CoolMOS™ integrated in this IC, it greatly simplifies the design and layout of the PCB. Due to valley switching, the turn on voltage is reduced and this offers higher conversion efficiency comparing to hard-switching flyback converter. With the DCM mode control, the reverse recovery problem of secondary rectify diode is relieved. And for its natural frequency jittering with line voltage, the EMI performance is better. Infineon's digital frequency reduction technology enables a quasi-resonant operation till very low load. As a result, the system efficiency, over the entire load range, is significantly improved compared to conventional free running quasi resonant converter implemented with only maximum switching frequency limitation at light load. In addition, numerous adjustable protection functions have been implemented in ICE2QR4780G to protect the system and customize the IC for the chosen application. In case of failure modes, like open control-loop/over load, output overvoltage, and transformer short winding, the device switches into Auto Restart Mode or Latch-off Mode. By means of the cycle-by-cycle peak current limitation plus foldback point correction, the dimension of the transformer and current rating of the secondary diode can both be optimized.Thus, a cost effective solution can be easily achieved

2 Demonstrator board

This document contains the list of features, the power supply specification, schematic, bill of material and the transformer construction documentation. Typical operating characteristics such as performance curve and scope waveforms are showed at the rear of the report.

Figure 1 DEMO-2QR4780G (Top View)

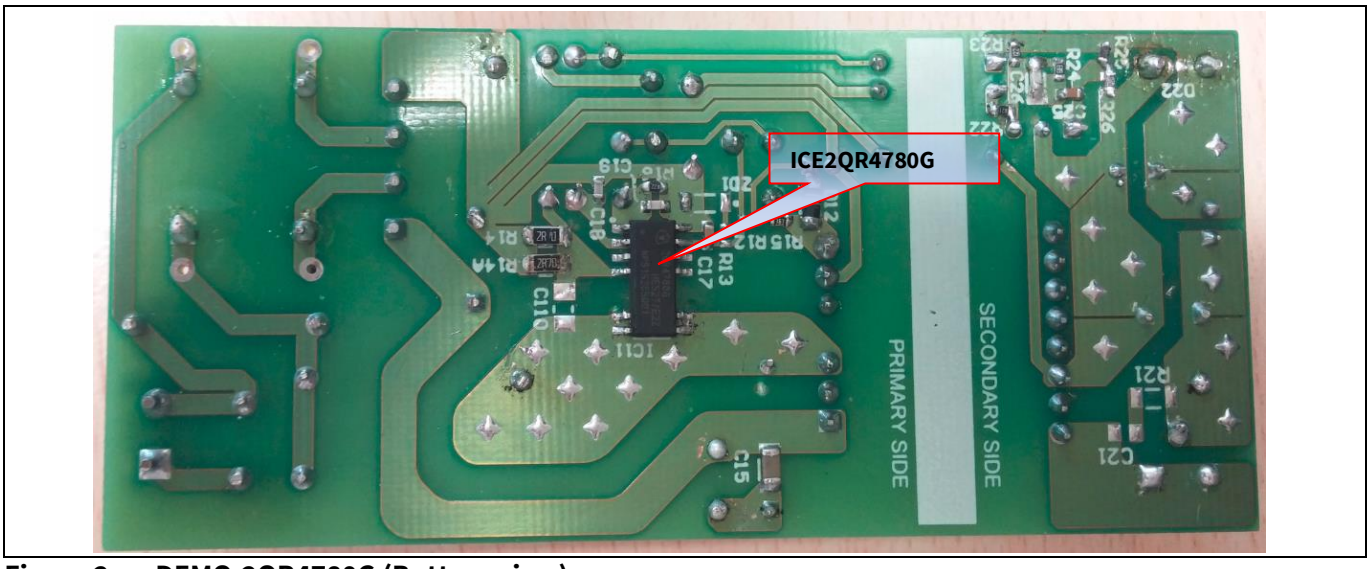


Figure 2 DEMO-2QR4780G (Bottom view)

3 Specifications of Demonstrator Board

Table 1 Specifications of DEMO-2QR4780G

Input voltage and frequency	85 V_{AC} (60 Hz) ~ 265 V_{AC} (50Hz)
Output voltage, current and power	12 V, 1 A, 12 W
Dynamic load response (10% to 100% load, slew rate at 1.5 A/µs, 100 Hz)	±3% of nominal output voltage ($V_{ripple\_p\_p}$ < 200 mV)
Output ripple voltage (full load, 85 V_{AC} ~ 265 V_{AC})	±1% of nominal output voltage ($V_{ripple\_p\_p}$< 60 mV)
Active mode four point average efficiency (25%, 50%, 75%, 100% load) (EU CoC Version 5, Tier 1) 10% load efficiency (EU CoC Version 5, Tier 1)	>86% at 115 V_{AC} and >85% 230 V_{AC} >83% at 115 V_{AC} and >82% 230 V_{AC}
No load power consumption (EU CoC Version 5, Tier 1)	< 50 mW at 265 V_{AC}
Conducted emissions (EN55022 class B)	Pass with 10 dB margin for 115 V_{AC} and 6 dB margin for 230 V_{AC}
ESD immunity (EN61000-4-2)	Special Level (±16 kV for both contact and air discharge)
Surge immunity (EN61000-4-5)	Installation class 4 (±2 kV for line to line and ±4 kV for line to earth)
Form factor case size (L x W x H)	(98 x 44 x 24) mm^3

4 Circuit description

4.1 Line input

The AC line input side comprises the input fuse F1 as over-current protection. The choke L11, X-capacitor C11 and Y-capacitor C12 act as EMI suppressors. Optional spark gap devices SA1, SA2 and varistor VAR can absorb high voltage stress during lightning surge test. A rectified DC voltage (120~374 V_{DC}) is obtained through the bridge rectifier BR1 together with bulk capacitor C13.

4.2 Start up

Since there is a built-in startup cell in the ICE2QR4780G, there is no need for external start up resistor, which can improve standby performance significantly.

When V_{VCC} reaches the turn on voltage threshold 18V, the IC begins with a soft start. The soft-start implemented in ICE2QR4780G is a digital time-based function. The preset soft-start time is 12 ms with 4 steps. If not limited by other functions, the peak voltage on CS pin will increase step by step from 0.32 V to 1 V finally. After IC turns on, the V_{VCC} voltage is supplied by auxiliary windings of the transformer.

4.3 Integrated MOSFET and PWM control

ICE2QR4780G is comprised of a power MOSFET and the Quasi-Resonant controller; this integrated solution greatly simplifies the circuit layout and reduces the cost of PCB manufacturing. The PWM switch-on is determined by the zero-crossing input signal and the value of the up/down counter. The PWM switch-off is determined by the feedback signal V_{FB} and the current sensing signal V_{CS}. ICE2QR4780G also performs all necessary protection functions in flyback converters. Details about the information mentioned above are illustrated in the product datasheet.

4.4 RCD clamper circuit

A clamper network (R11, C15 and D11) dissipates the energy of the leakage inductance and suppress ringing on the SMPS transformer.

4.5 Output stage

On the secondary side, 12 V output, the power is coupled out via a schottky diode D21. The capacitor C22 provides energy buffering followed by the L-C filters L21 and C24 to reduce the output ripple and prevent interference between SMPS switching frequency and line frequency considerably. Storage capacitor C22 and C23 is designed to have an internal resistance (ESR) as small as possible. This is to minimize the output voltage ripple caused by the triangular current.

4.6 Feedback loop

For feedback, the output is sensed by the voltage divider of R26 and R25 and compared to IC21 (TL431) internal reference voltage. C25, C26 and R24 comprise the compensation network. The output voltage of IC21 (TL431) is converted to the current signal via optocoupler IC12 and two resistors R22 and R23 for regulation control.

4.7 Primary side peak current control

The MOSFET drain source current is sensed via external resistor R14 and R14A. Since ICE2QR4780G is a current mode controller, it would have a cycle-by-cycle primary current and feedback voltage control which can make sure the maximum power of the converter is controlled in every switching cycle.

For a Quasi-Resonant flyback converter, the maximum possible output power is increased when a constant current limit value is used for all the line input voltage range. This is usually not desired as this will increase additional cost on transformer and output diode in case of output over power conditions.
The internal foldback point correction is implemented to adjust the V_{CS} voltage limit according to the input line voltage. Here, the input line voltage is sensed using the current flowing out of ZC pin, during the MOSFET on-time. As the result, the maximum current limit will be lower at high input voltage and the maximum output power can be well limited versus the input voltage.

4.8 Digital frequency reduction

During normal operation, the switching frequency for ICE2QR4780G is digitally reduced with decreasing load. At light load, the MOSFET will be turned on not at the first minimum drain-source voltage time, but on the nth. The counter is in range of 1 to 7, which depends on feedback voltage in a time-base. The feedback voltage decreases when the output power requirement decreases, and vice versa. Therefore, the counter is set by monitoring voltage V_{FB}. The counter will be increased with low V_{FB} and decreased with high V_{FB}. The thresholds are preset inside the IC.

4.9 Active burst mode

At light load condition, the SMPS enters into Active Burst Mode. At this stage, the controller is always active but the V_{VCC} must be kept above the switch off threshold. During active burst mode, the efficiency increase significantly and at the same time it supports low ripple on V_{out} and fast response on load jump.

For determination of entering Active Burst Mode operation, three conditions apply:

1. The feedback voltage is lower than the threshold of V_{FBEB}(1.25 V). Accordingly, the peak current sense voltage across the shunt resistor is 0.17;
2. The up/down counter is 7;
3. And a certain blanking time (t_{BEB}=24 ms).

Once all of these conditions are fulfilled, the Active Burst Mode flip-flop is set and the controller enters Active Burst Mode operation. This multi-condition determination for entering Active Burst Mode operation prevents mis-triggering of entering Active Burst Mode operation, so that the controller enters Active Burst Mode operation only when the output power is really low during the preset blanking time.

During active burst mode, the maximum current sense voltage is reduced from 1 V to 0.34 V so as to reduce the conduction loss and the audible noise. At the burst mode, the FB voltage is changing like a sawtooth between 3.0 V and 3.6 V.

The feedback voltage immediately increases if there is a high load jump. This is observed by one comparator. As the current limit is 34% during Active Burst Mode a certain load is needed so that feedback voltage can exceed V_{FBLB} (4.5 V). After leaving active burst mode, maximum current can now be provided to stabilize V_{out}. In addition, the up/down counter will be set to 1 immediately after leaving Active Burst Mode. This is helpful to decrease the output voltage undershoot.

5 Protection features

5.1 V_{CC} over voltage and under voltage protection

During normal operation, the V_{CC} voltage is continuously monitored. When the V_{CC} voltage increases up to $V_{CC,OVP}$ or V_{CC} voltage falls below the under voltage lock out level $V_{CC,off}$, the IC will enter into autorestart mode.

5.2 Over load/Open loop protection

In case of open control loop, feedback voltage is pulled up with internally block. After a fixed blanking time, the IC enters into auto restart mode. In case of secondary short-circuit or overload, regulation voltage V_{FB} will also be pulled up, same protection is applied and IC will auto restart.

5.3 Over temperature protection

The IC has a built-in over temperature protection function. When the controller's temperature reaches 140°C, the IC will shut down switch and enters into auto restart. This can protect power MOSFET from overheated.

5.4 Adjustable output overvoltage protection

During off-time of the power switch, the voltage at the zero-crossing pin ZC is monitored for output overvoltage detection. If the voltage is higher than the preset threshold 3.7 V for a preset period 100 µs, the IC is latched off.

5.5 Short winding protection

The source current of the MOSFET is sensed via external resistor R14 and R14A. If the voltage at the current sensing pin is higher than the preset threshold V_{CSSW} of 1.68 V during the on-time of the power switch, the IC is latched off. This constitutes a short winding protection. To avoid an accidental latch off, a spike blanking time of 190 ns is integrated in the output of internal comparator.

Table 2 Protection function of ICE2QR4780G

Protection Function	Failure Condition	Protection Mode
VCC Overvoltage	V_{VCC} > 25 V & last for 10 µs (normal mode only)	Auto Restart
VCC Undervoltage/ Short Optocoupler	V_{VCC} < 10.5 V	Auto Restart
Overload/Open Loop	V_{FB} > 4.5 V & last for 30 ms	Auto Restart
Over Temperature (Controller Junction)	T_J > 140 °C	Auto Restart
Output Overvoltage	V_{ZCOVP} > 3.7 V & last for 100 µs	Latch
Short Winding	V_{CSSW} > 1.68 V & last for 190 ns	Latch

6 Circuit diagram

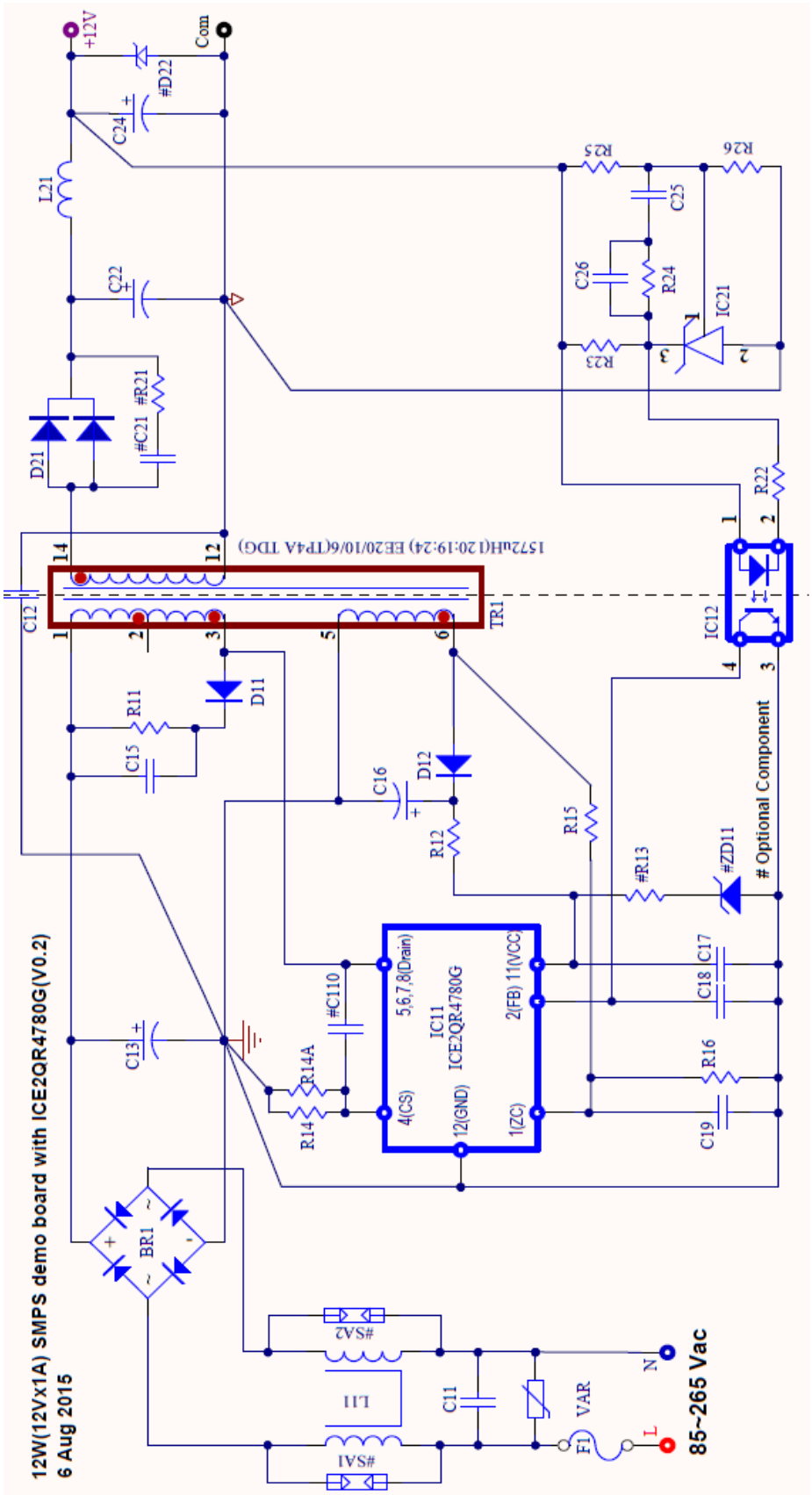


Figure 3 Schematic of DEMO-2QR4780G

Circuit diagram

Note: General guideline for layout design of Printed Cirduit Board (PCB):

1. *Star ground at bulk capacitor C13: all primary grounds should be connected to the ground of bulk capacitor C13 seperately in one point. It can reduce the switching noise going into the sensitive pins of CoolSET™ device effectively. The primary star ground can be split into five groups as follows,*
    i. *Signal ground includes all small signal grounds connecting to the CoolSET™ GND pin such as filter capacitor ground C17, C18, C19 and opto-coupler ground.*
    ii. *VCC ground includes the VCC capacitor ground C16 and the auxiliary winding ground, pin 5 of the power transformer.*
    iii. *Current Sense resistor ground includes current sense resistor R14 and R14A.*
    iv. *EMI return ground includes Y capacitor C12.*
    v. *DC ground from bridge rectifier, BR1*
2. *Filter capacitor close to the controller ground: Filter capacitors, C17, C18 and C19 should be placed as close to the controller ground and the controller pin as possible so as to reduce the switching noise coupled into the controller.*
3. *High voltage traces clearance: High voltage traces should keep enough spacing to the nearby traces. Otherwise, arcing would incur.*
    i. *400 V traces (positive rail of bulk capacitor C13) to nearby trace: > 2.0 mm*
    ii. *600V traces (drain voltage of CoolSET™ IC11) to nearby trace: > 2.5 mm*
4. *Recommended minimum 232mm^2 copper area at drain pin to add on PCB for better thermal performance.*
5. *Power loop area (bulk capacitor C13, primary winding of the transformer TR1 (Pin 1 and 3), IC11 Drain pin, IC11 CS pin and current sense resistor R14/R14A) should be as small as possible to minimize the switching emission.*

7 PCB layout

7.1 Top side

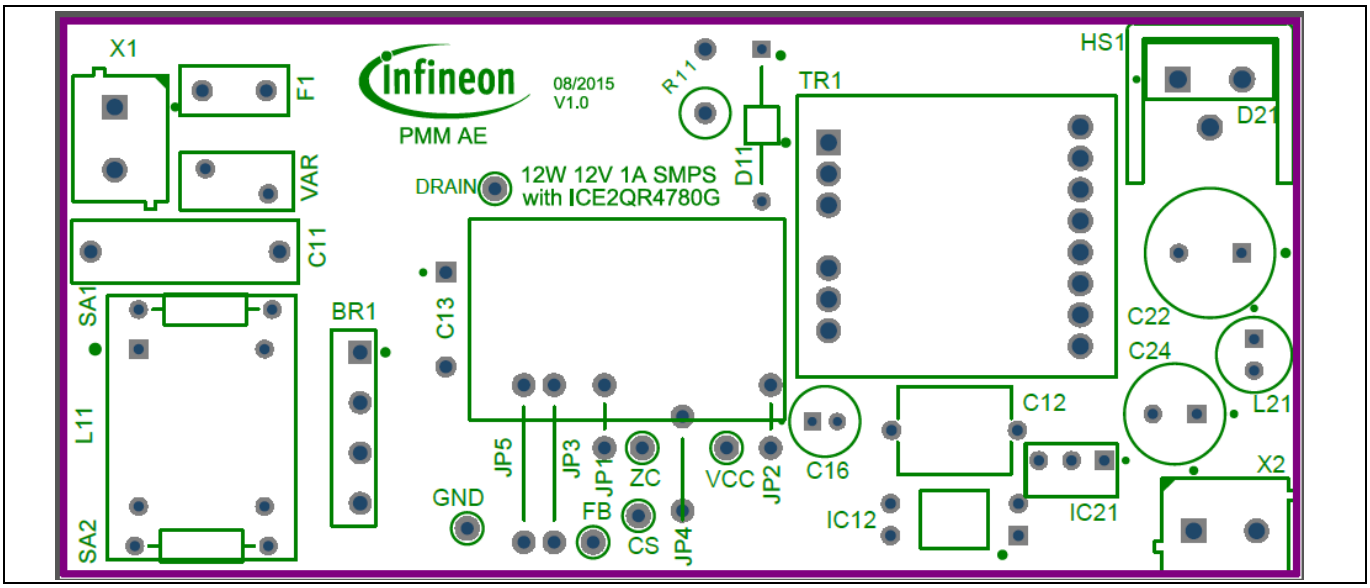


Figure 4 Top side component legend

7.2 Bottom side

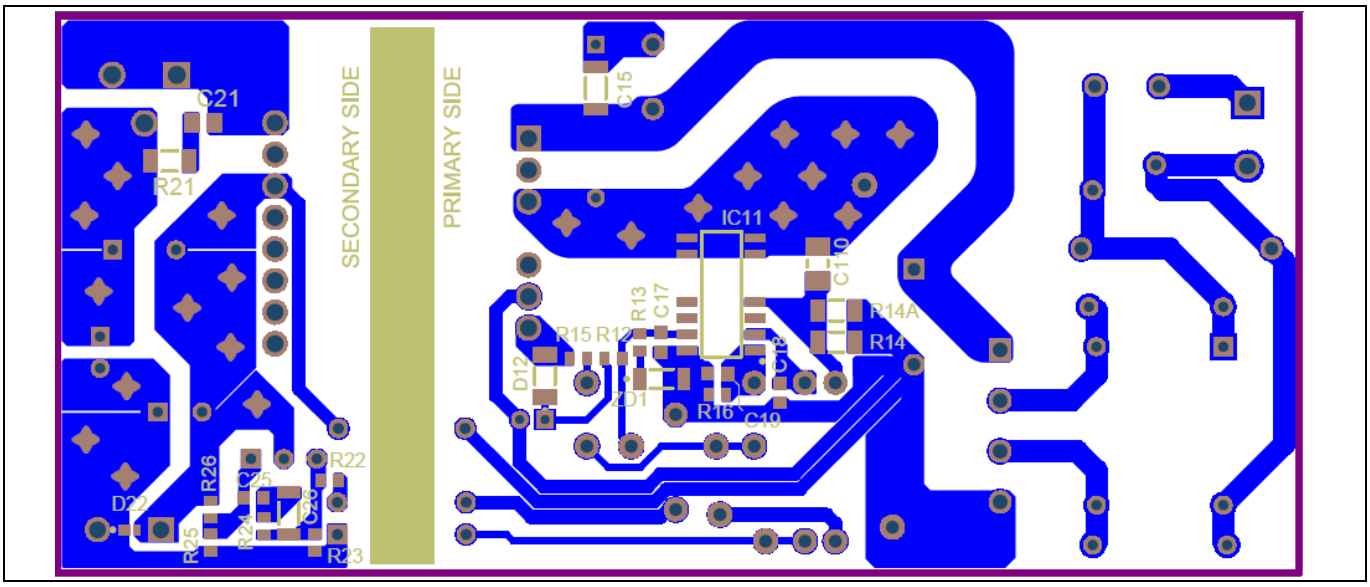


Figure 5 Bottom side copper and component legend

8 Bill of material

Table 3 Bill of material (V0.2)

No.	Designator	Description	Part Number	Manufacturer	Quantity
1	BR1	600V/1A	S1VBA60	Shindengen	1
2	C11	0.1µF/305V	B329221C3104K	Epcos	1
3	C12	2.2nF/250V	DE1E3KX222MA4BN01F	Murata	1
4	C13	33µF/450V	450BXC33MEFC16X25	Rubycon	1
5	C15	1nF/600V	GRM31A7U2J102JW31D9	Murata	1
6	C16	22µF/50V	50PX22MEFC5X11	Rubycon	1
7	C17	100nF/50V	GRM188R71H104KA93D	Murata	1
8	C18, C26	1nF/50V	GRM1885C1H102GA01D	Murata	2
9	C19	100pF/50V	GRM1885C1H101GA01D	Murata	1
10	C22	1000uF/16V	16ZLH1000MEFC10X16	Rubycon	1
11	C24	680uF/16V	16ZLH680MEFC8X16	Rubycon	1
12	C25	220nF/50V	GRM188R71H224KAC4D	Murata	1
13	D11	0.8A/600V	D1NK60	Shindengen	1
14	D12	0.5A/200V	GL34D		1
15	D21	30A/100V	STPS30M100SFP		1
16	F1	1.6A/300V	36911600000		1
17	HS1		577202B00000G		1
18	IC11	ICE2QR4780G	ICE2QR4780G	Infineon	1
19	IC12	SFH617A-3	SFH617A-3		1
20	IC21	TL431A	TL431A		1
21	L11	68mH/0.4A	B82731M2401A033	Epcos	1
22	L21	1uH/8A	744 746 201 0	Wurth Electronics	1
23	R11	330K/2W/500V	MCF 2W 330K		1
24	R12	10Ω			1
25	R14, R14A	2.7R/ 0.33W/ ±1%	ERJ8BQF2R7V		2
26	R15	38kΩ/1%			1
27	R16	8.2kΩ/1%			1
28	R22	820Ω/5%			1
29	R23	1.2kΩ/5%			1
30	R24	68kΩ/1%			1
31	R25	38kΩ/1%			1
32	R26	10kΩ/1%			1
33	TR1	1572µH(120:19:24)	750342983	Wurth Electronics	1
34	Test Point	ZC,FB,CS,Drain,Vcc,Gnd	5003		1
35	VAR	0.25W/300V	B72207S2301K101	Epcos	1
36	(L N), (+12V Com)	Connector	691102710002	Wurth Electronics	2

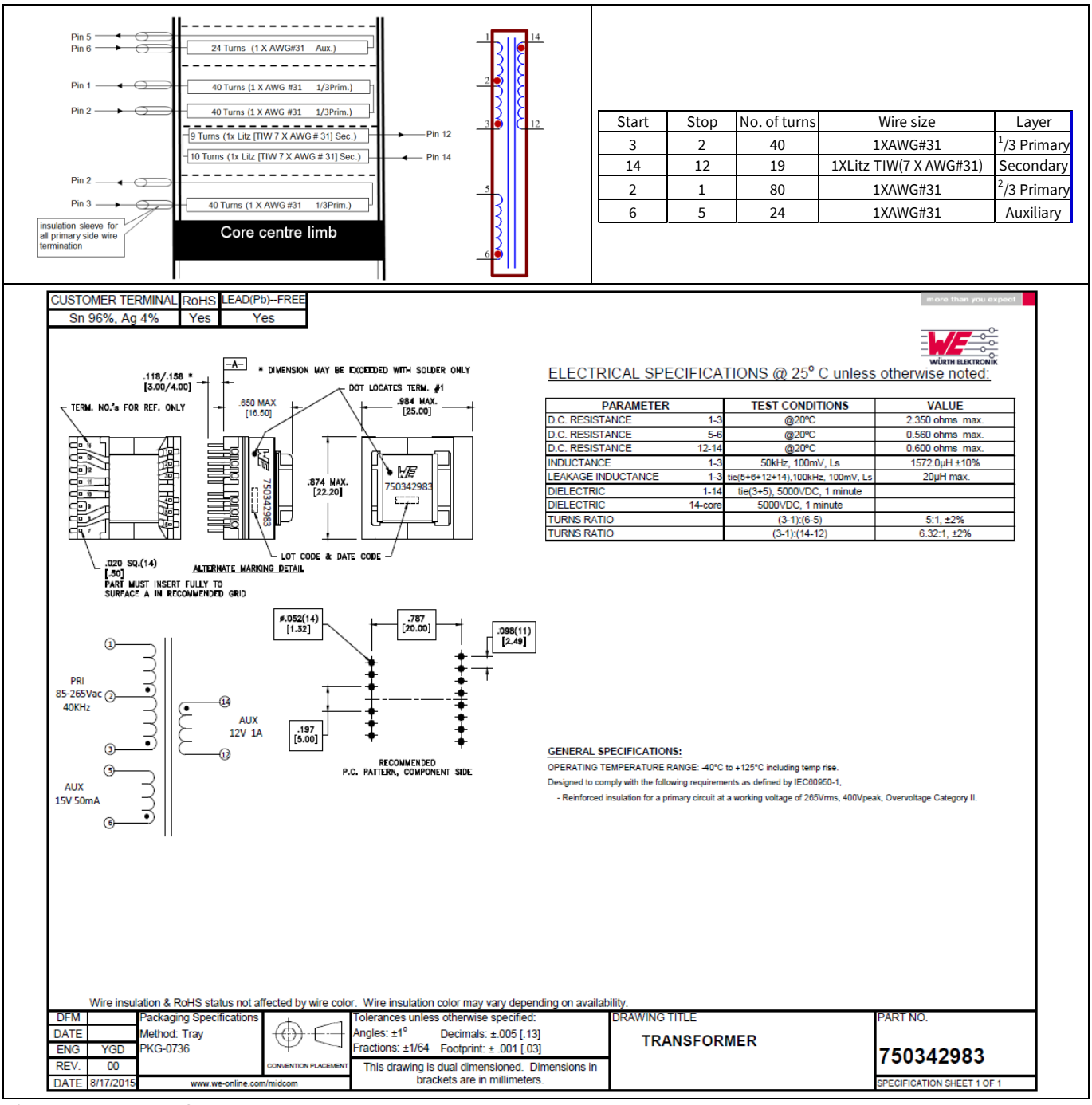
9 Transformer construction

Core and material: EE20/10/6(EF20), TP4A(TDG)

Bobbin: 070-5643 (14 Pin, THT, Horizontal Version)

Primary Inductance: Lp=1572 µH (±10%), measured between pin 3 and pin 1

Manufacturer and part number: Wurth Electronics Midcom (750342983)



Start	Stop	No. of turns	Wire size	Layer
3	2	40	1XAWG#31	[1]/3 Primary
14	12	19	1XLitz TIW(7 X AWG#31)	Secondary
2	1	80	1XAWG#31	[2]/3 Primary
6	5	24	1XAWG#31	Auxiliary

Figure 6 Transformer structure

10 Test results

10.1 Efficiency, regulation and output ripple

Table 4 Efficiency, regulation & output ripple

Input (V_{AC}/Hz)	P_{in} (W)	V_{out} (V_{DC})	I_{out} (A)	V_{OutRPP} (mV)	P_{out} (W)	Efficiency (η) (%)	Average η (%)	OLP P_{in} (W)	OLP I_{out} (A)
85 V_{AC}/60 Hz	0.0333	12.07	0.00	40.13				17.10	1.18
	1.4500	12.07	0.10	47.64	1.21	83.24			
	3.5300	12.07	0.25	12.62	3.02	85.48	85.07		
	7.0300	12.07	0.50	15.47	6.04	85.85			
	10.5500	12.07	0.75	17.33	9.05	85.81			
	14.5200	12.07	1.00	28.36	12.07	83.13			
115 V_{AC}/60 Hz	0.0334	12.07	0.00	39.96				16.70	1.19
	1.4500	12.07	0.10	48.93	1.21	83.24			
	3.5200	12.07	0.25	12.44	3.02	85.72	86.41		
	6.9600	12.07	0.50	14.44	6.04	86.71			
	10.4000	12.07	0.75	14.62	9.05	87.04			
	14.0100	12.07	1.00	17.60	12.07	86.15			
230 V_{AC}/50 Hz	0.0363	12.07	0.00	41.91				16.80	1.21
	1.4700	12.07	0.10	51.24	1.21	82.11			
	3.6100	12.07	0.25	11.96	3.02	83.59	85.93		
	7.0000	12.07	0.50	13.38	6.04	86.21			
	10.4200	12.07	0.75	12.18	9.05	86.88			
	13.8700	12.07	1.00	12.36	12.07	87.02			
265V_{AC}/50 Hz	0.0383	12.07	0.00	43.82				17.20	1.24
	1.4900	12.07	0.10	53.42	1.21	81.01			
	3.6700	12.07	0.25	11.73	3.02	82.22	85.16		
	7.0500	12.07	0.50	13.20	6.04	85.60			
	10.4900	12.07	0.75	12.27	9.05	86.30			
	13.9500	12.07	1.00	12.09	12.07	86.52			

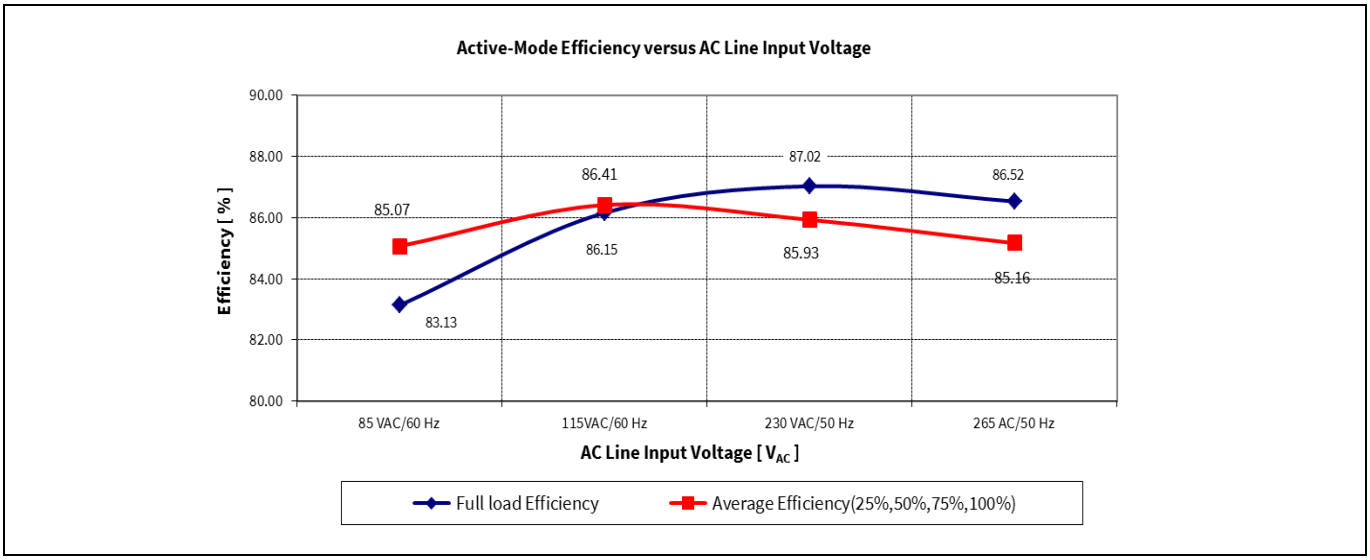


Figure 7 Efficiency vs AC line input voltage

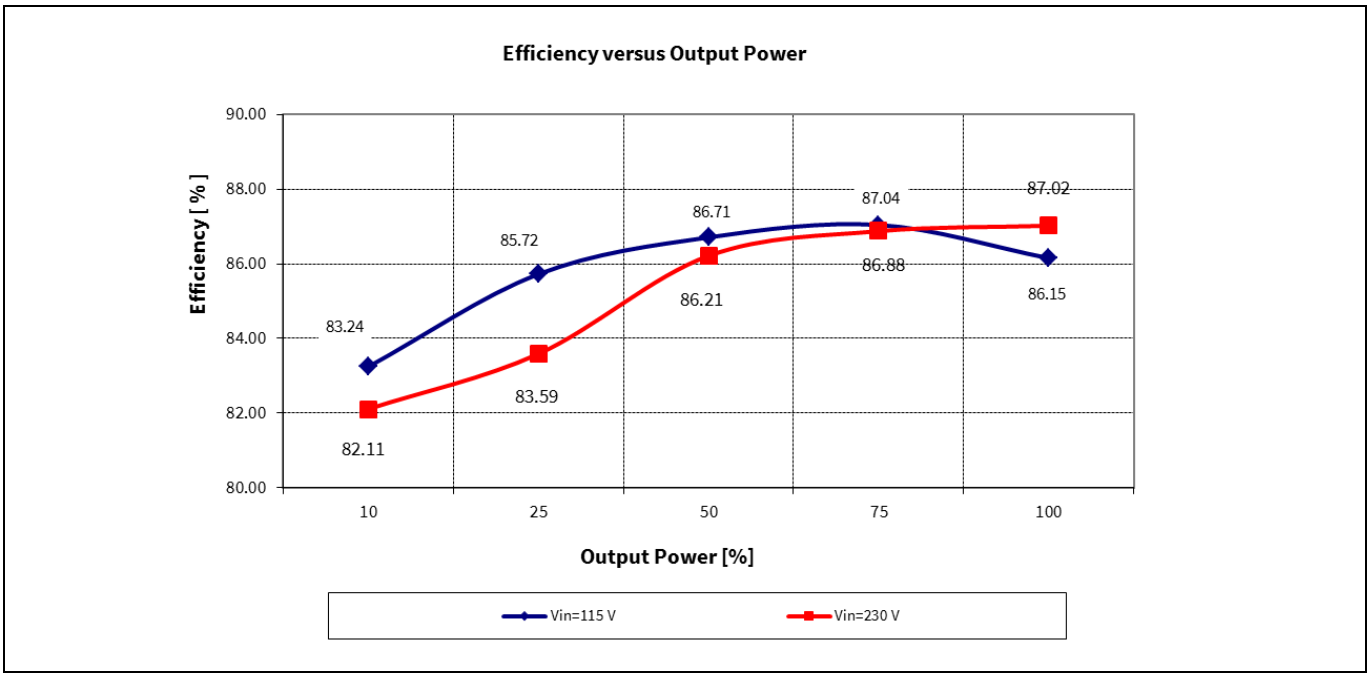


Figure 8 Efficiency vs output power at 115 V_{AC} and 230 V_{AC} line

10.2 Standby power

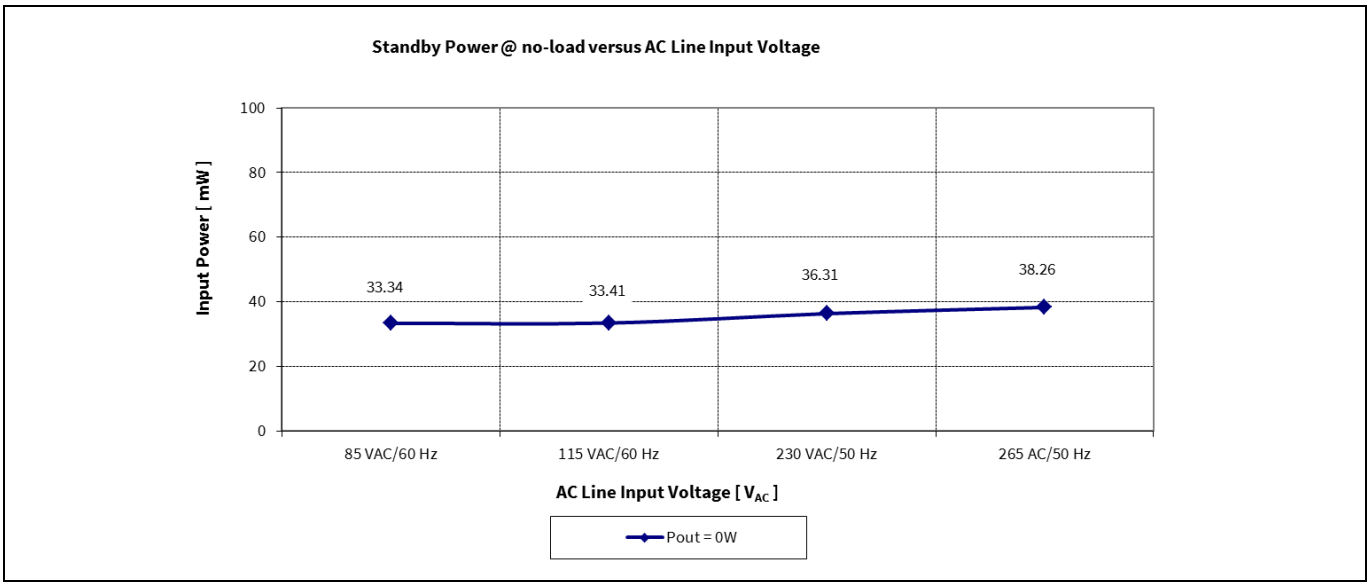


Figure 9 Standby power at no load vs AC line input voltage (measured by Yokogawa WT210 power meter - integration mode)

10.3 Line regulation

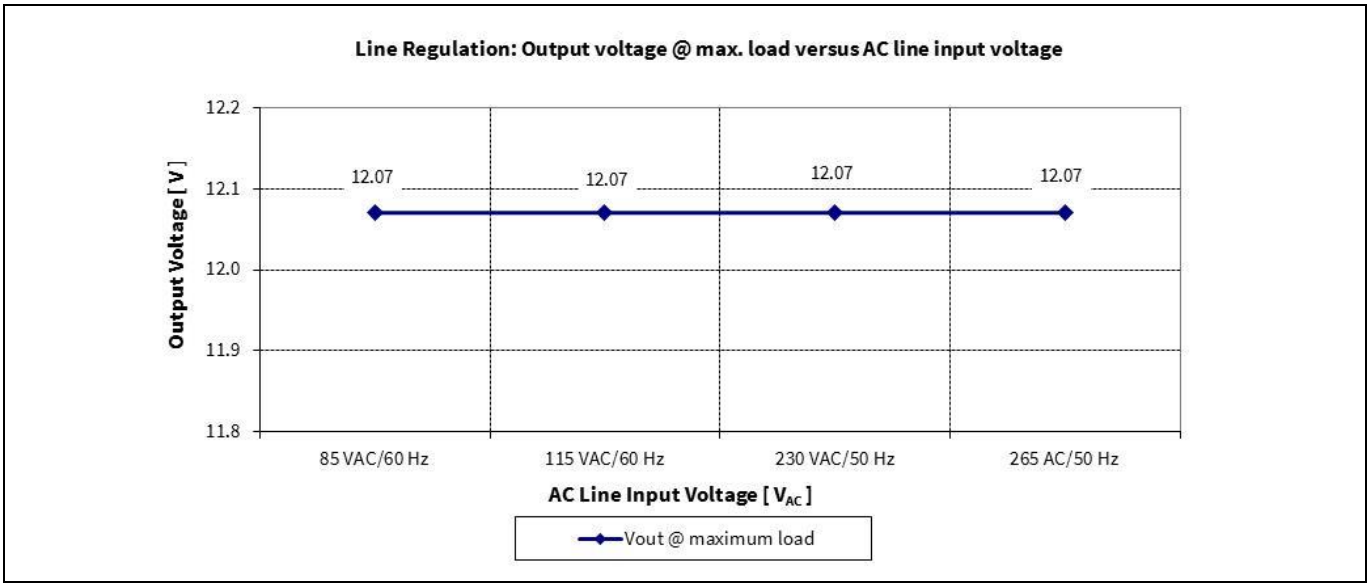


Figure 10 Line regulation Vout at full load vs AC line input voltage

10.4 Load regulation

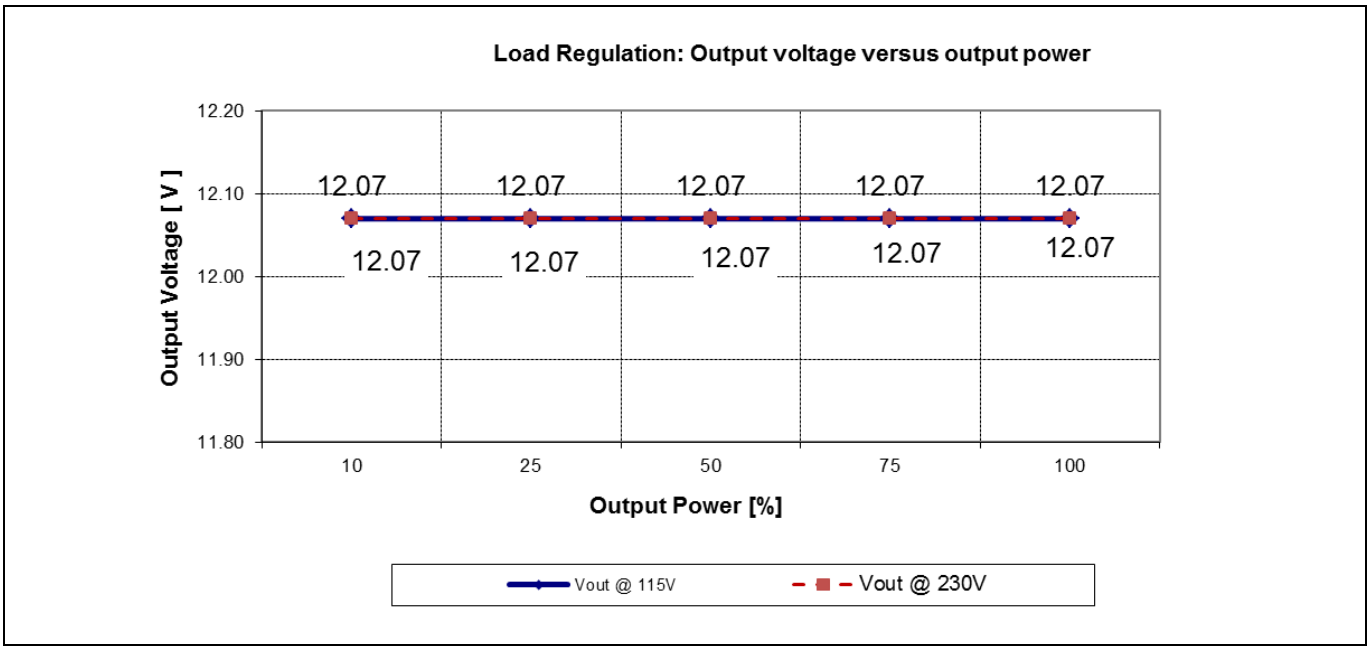


Figure 11 Load regulation V_{out} vs output power

10.5 Maximum input power

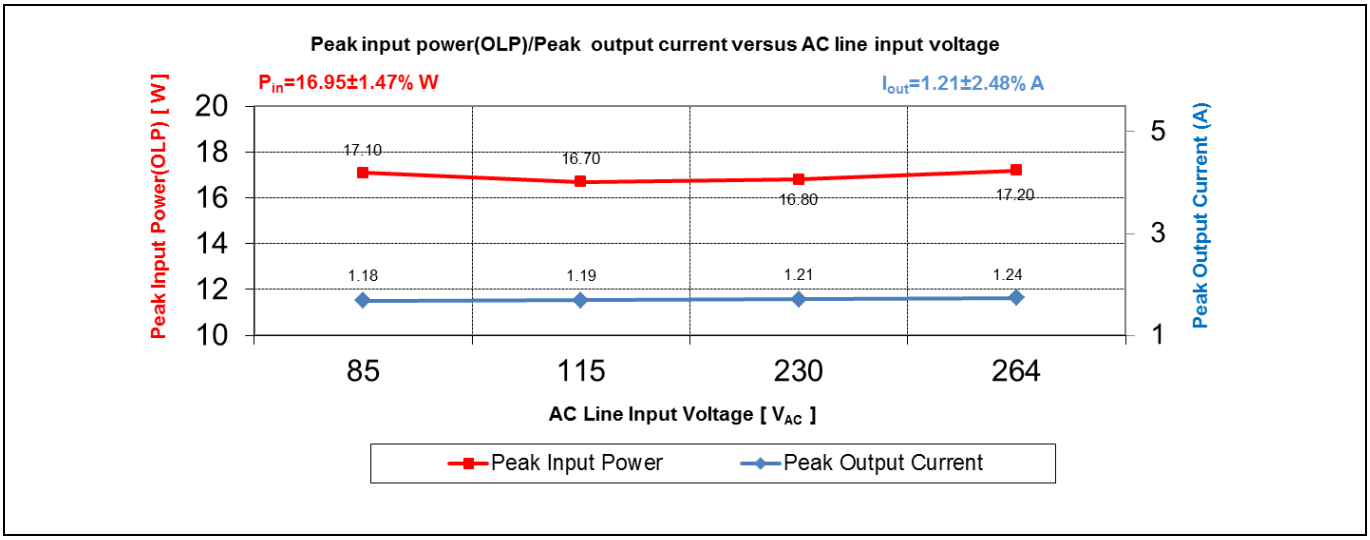


Figure 12 Maximum input power (before over-load protection) vs AC line input voltage

10.6 ESD immunity (EN61000-4-2)

Pass EN61000-4-2 Special Level (±16 kV for both contact and air discharge).

10.7 Surge immunity (EN61000-4-5)

Pass EN61000-4-5 Installation class 4 (±2 kV for line to line and ±4 kV for line to earth).

10.8 Conducted emissions (EN55022 class B)

The conducted EMI was measured by Schaffner (SMR4503) and followed the test standard of EN55022 (CISPR 22) class B. The demo board was set up at maximum load (12 W) with input voltage of 115 V_{AC} and 230 V_{AC}.

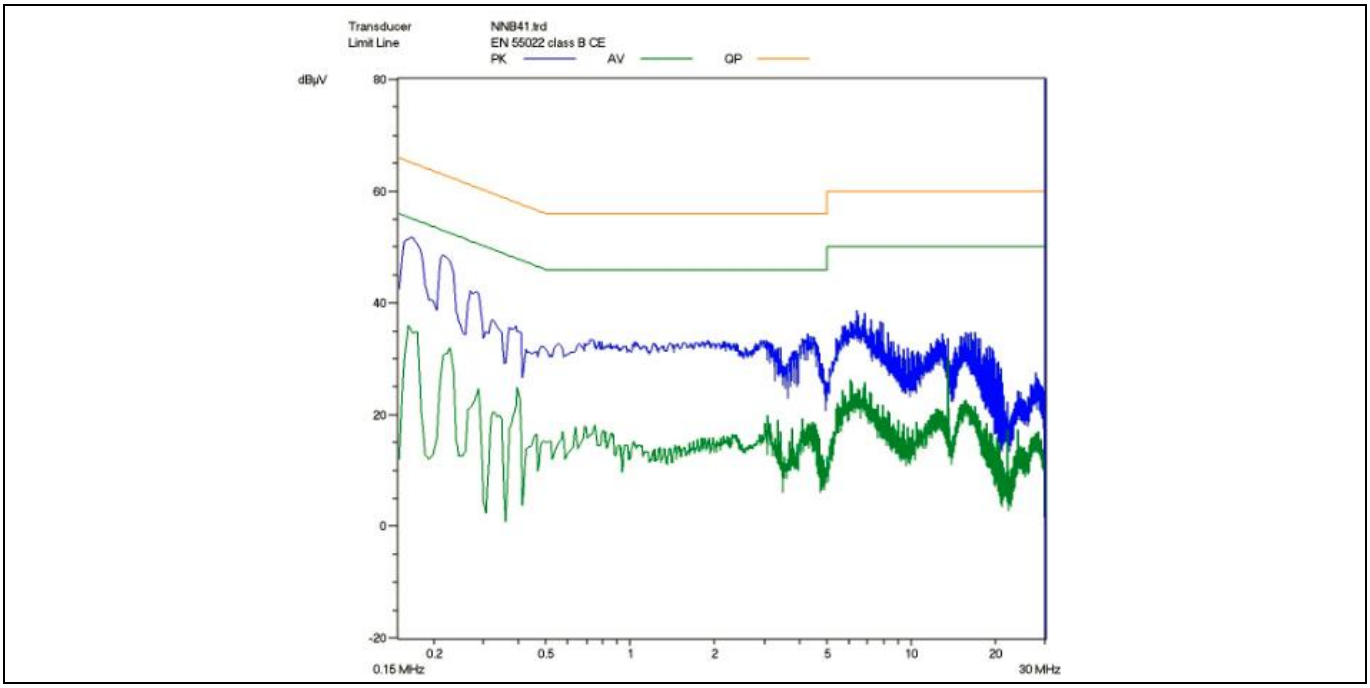


Figure 13 Conducted emissions(Line) at 115 V_{AC} and maximum Load

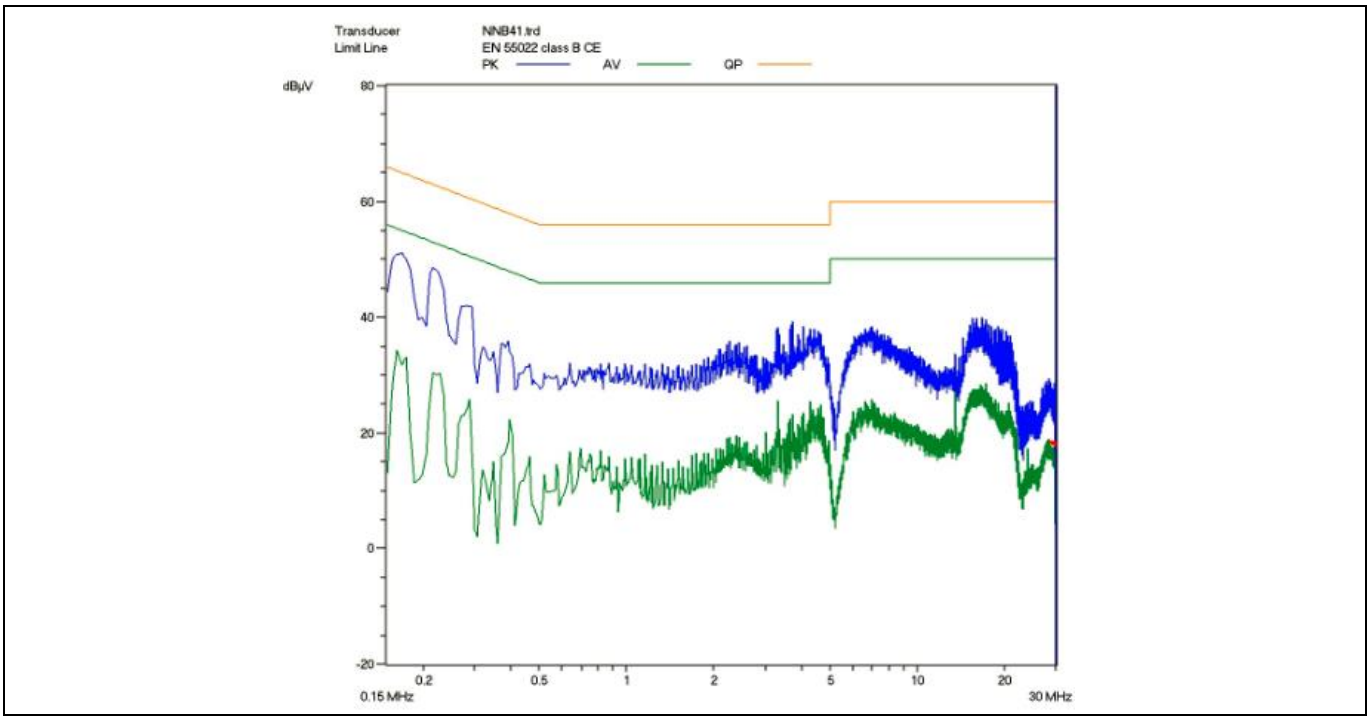


Figure 14 Conducted emissions(Neutral) at 115 V_{AC} and maximum Load

Pass conducted emissions EN55022 (CISPR 22) class B with 10 dB margin for quasi peak limit at low line (115 V_{AC}).

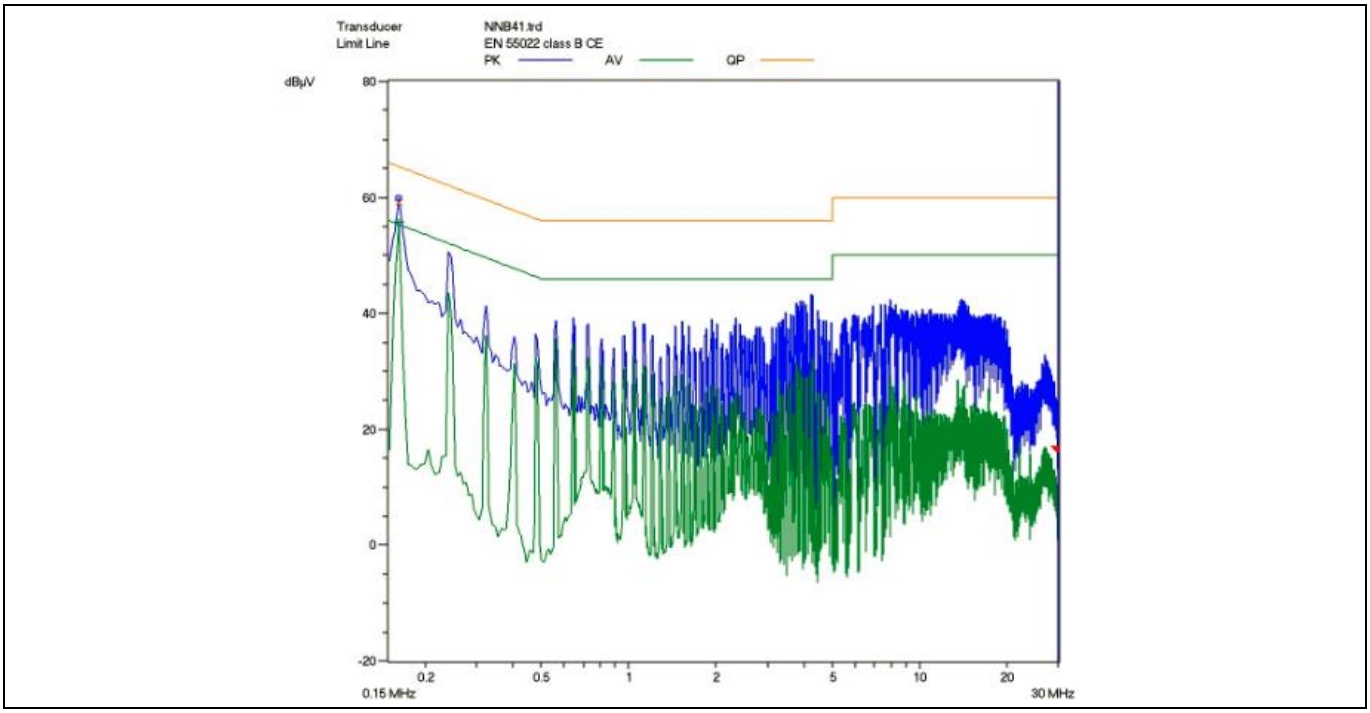


Figure 15 Conducted emissions(line) at 230 V_{AC} and maximum Load

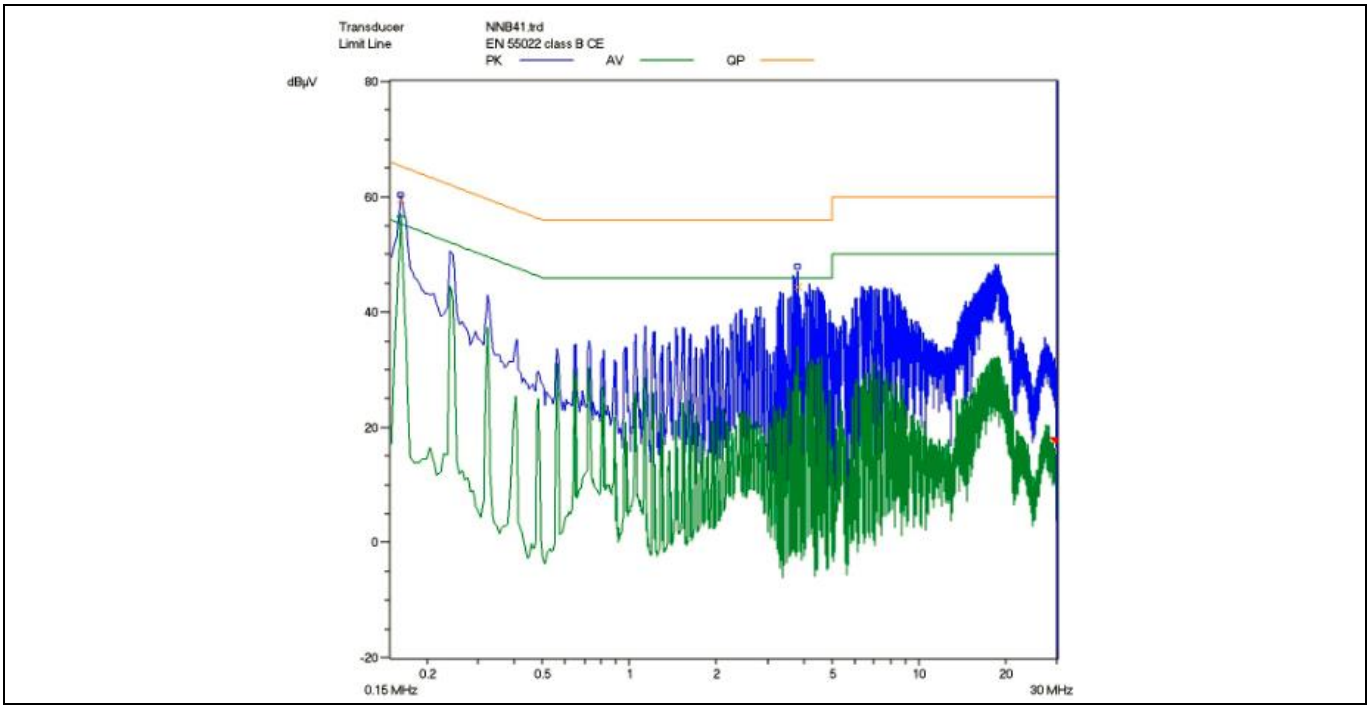


Figure 16 Conducted emissions(Neutral) at 230 V_{AC} and maximum Load

Pass conducted emissions EN55022 (CISPR 22) class B with 6 dB margin for quasi peak limit at high line (230 V_{AC}).

10.9 Thermal measurement

The thermal test of open frame demo board was done using an infrared thermography camera (TVS-500EX) at ambient temperature 25°C. The measurements were taken after two hours running at full load.

Table 5 Hottest temperature of demo board

No.	Major component	85 V_{AC} (°C)	265 V_{AC} (°C)
1	IC11 (ICE2QR4780G)	53.8	50.1
2	R14 (current sense resistor)	44.7	37.5
3	TR1 (transformer)	52.6	56.0
4	BR1 (bridge diode)	40.9	33.4
5	R11(clamper resistor)	43.0	41.3
6	L11 (choke)	40.1	29.3
7	D21 (Secondary diode)	42.4	42.7
8	Ambient	25	25

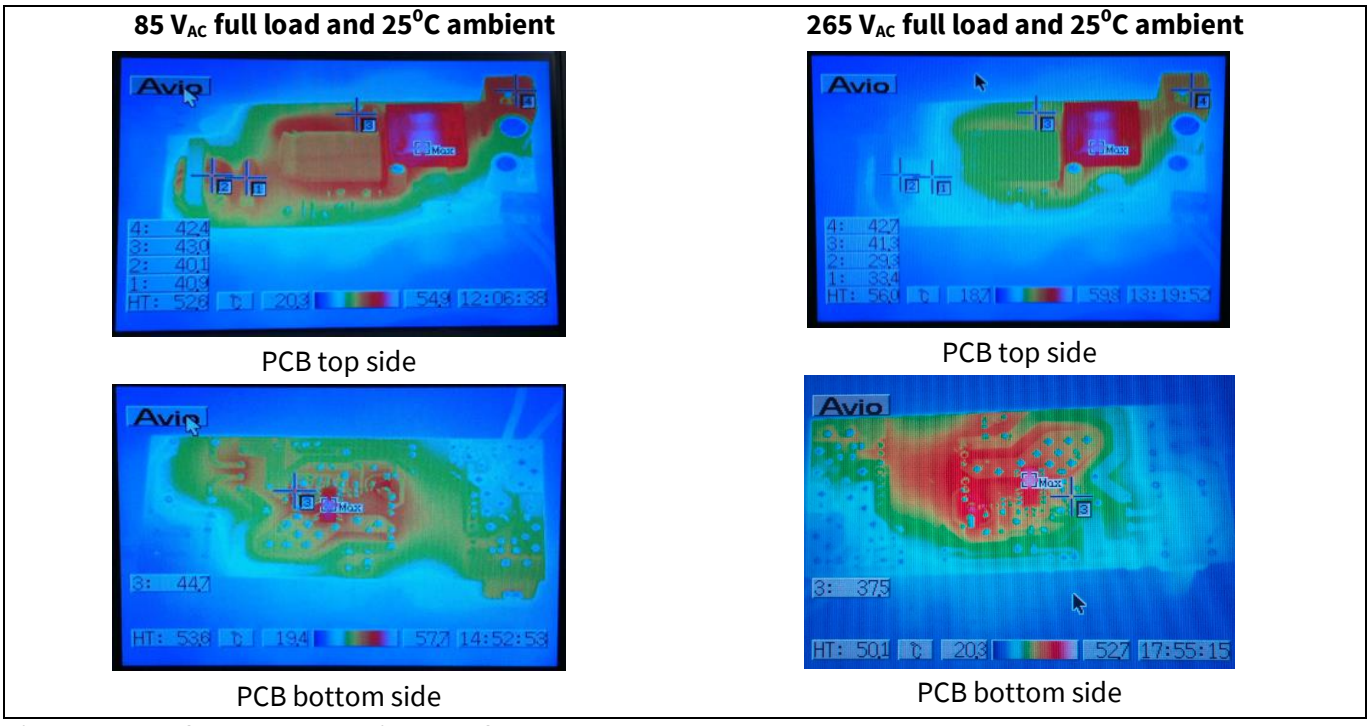


Figure 17 Infrared thermal image of DEMO-2QR4780G

11 Waveforms and scope plots

All waveforms and scope plots were recorded with a TELEDYNELECROY 606Zi oscilloscope.

11.1 Startup at low/high AC line input voltage with maximum load

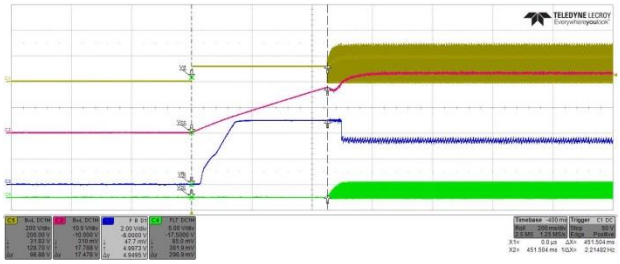
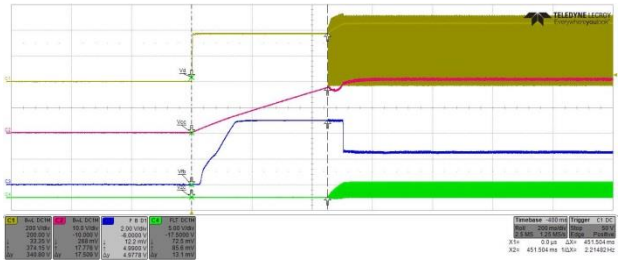
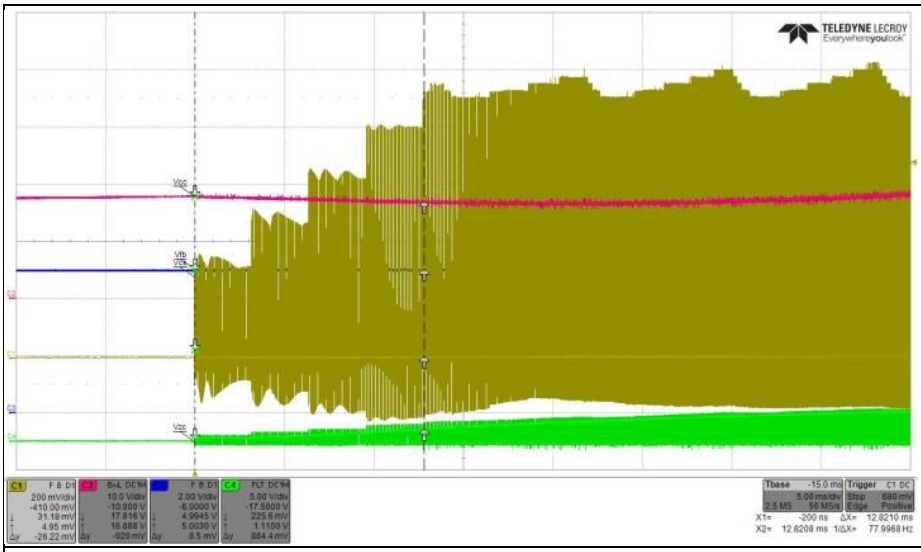
	
C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : Supply voltage (V_{VCC}) C2 (Blue) : Feedback voltage (V_{FB}) C2 (Green) : Zero crossing voltage (V_{ZC})	C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : Supply voltage (V_{VCC}) C2 (Blue) : Feedback voltage (V_{FB}) C2 (Green) : Zero crossing voltage (V_{ZC})
Startup time at 85 V_{AC} and maximum load ≈ 450 ms	Startup time at 265 V_{AC} and maximum load ≈ 450 ms

Figure 18 Startup

11.2 Soft start



C1 (Yellow) : Current sense voltage (V_{CS})
C2 (Purple) : Supply voltage (V_{VCC})
C2 (Blue) : Feedback voltage (V_{FB})
C2 (Green) : Zero crossing voltage (V_{ZC})

Soft start time at 85 V_{AC} and maximum load ≈ 12 ms

Figure 19 Soft start

11.3 Drain and current sense voltage at maximum load

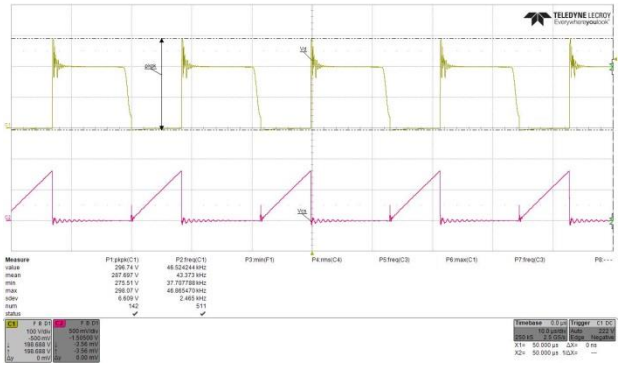
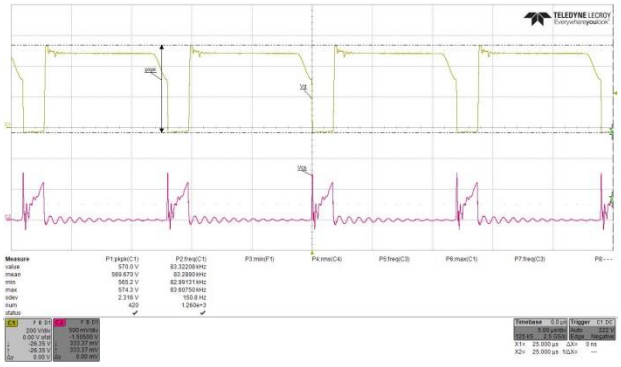
	
C1 (Yellow) : Drain voltage (V_{Drain}) C2 (Purple) : Current sense voltage (V_{CS})	C1 (Yellow) : Drain voltage (V_{Drain}) C2 (Purple) : Current sense voltage (V_{CS})
V_{Drain_peak} at 85 V_{AC} ≈ 290 V	V_{Drain_peak} at 265 V_{AC} ≈ 574 V

Figure 20 Drain and current sense voltage at maximum load

11.4 Zero crossing point during normal operation

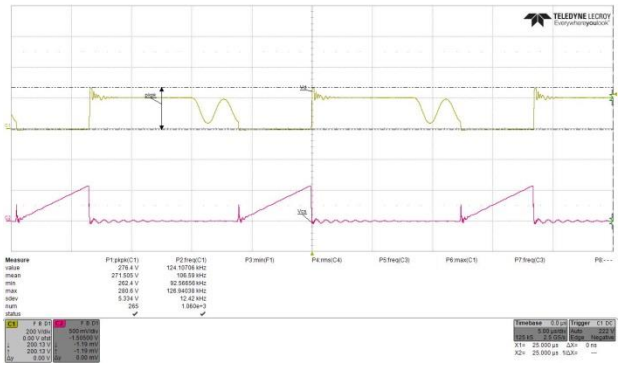
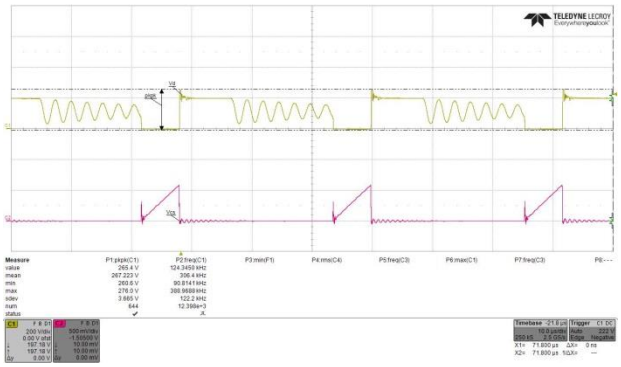
	
C1 (Yellow) : Drain voltage (V_{Drain}) C2 (Purple) : Current sense voltage (V_{CS})	C1 (Yellow) : Drain voltage (V_{Drain}) C2 (Purple) : Current sense voltage (V_{CS})
2nd zero crossing at 85 V_{AC}	7th zero crossing at 85 V_{AC}

Figure 1 Zero crossing

11.5 Load transient response (Dynamic load from 10% to 100%)

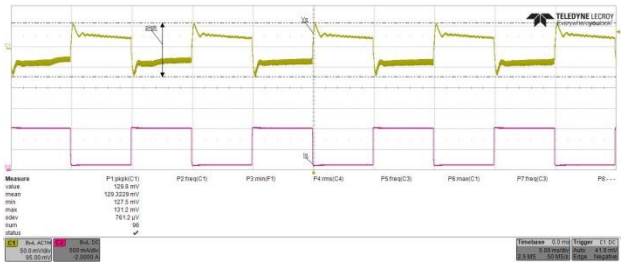
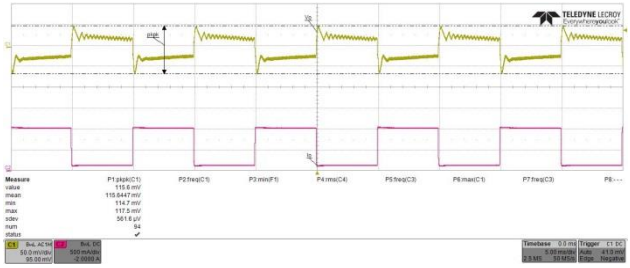
	
C1 (Yellow) : Output ripple voltage (V_{out}) C2 (Purple) : Output current (I_{out})	C1 (Yellow) : Output ripple voltage (V_{out}) C2 (Purple) : Output current (I_{out})
$V_{ripple\_pk\_pk}$ at 85 V_{AC} ≈ 131 mV (Load change from 10% to 100% at 85 V_{AC},100 Hz,1.5 A/µs slew rate) Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter	$V_{ripple\_pk\_pk}$ at 265 V_{AC} ≈ 117 mV (Load change from10% to 100% at 2100 V_{AC},100 Hz,1.5 A/µs slew rate) Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter

Figure 2 Load transient response

11.6 Output ripple voltage at maximum load

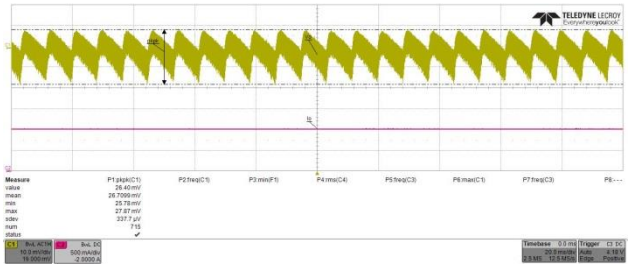
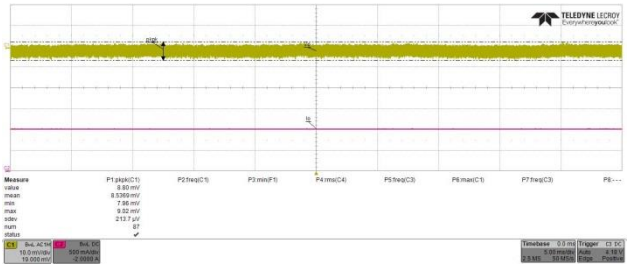
	
C1 (Yellow) : Output ripple voltage (V_{out}) C2 (Purple) : Output current (I_{out})	C1 (Yellow) : Output ripple voltage (V_{out}) C2 (Purple) : Output current (I_{out})
$V_{ripple\_pk\_pk}$ at 85 V_{AC} ≈ 28 mV Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter	$V_{ripple\_pk\_pk}$ at 265 V_{AC} ≈ 9 mV Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter

Figure 3 Output ripple voltage at maximum load

11.7 Output ripple voltage at burst mode 1 W load

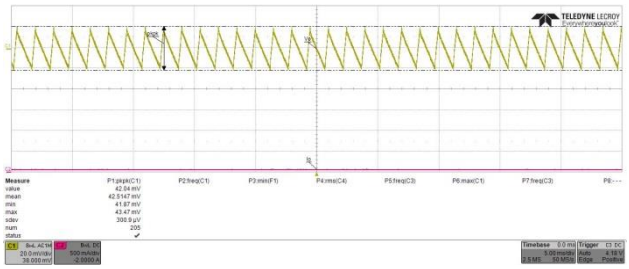
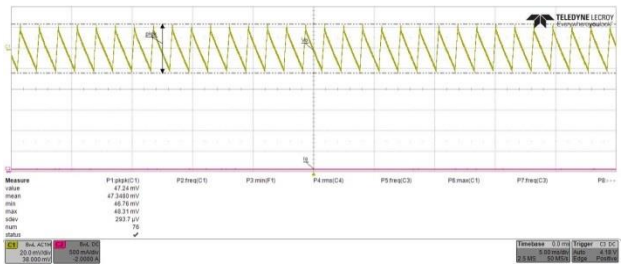
	
C1 (Yellow) : Output ripple voltage (V_{out}) C2 (Purple) : Output current (I_{out})	C1 (Yellow) : Output ripple voltage (V_{out}) C2 (Purple) : Output current (I_{out})
$V_{ripple\_pk\_pk}$ at 85 V_{AC} ≈ 44 mV Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter	$V_{ripple\_pk\_pk}$ at 265 V_{AC} ≈ 49 mV Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter

Figure 4 Output ripple voltage at burst mode 1 W load

11.8 Active burst mode

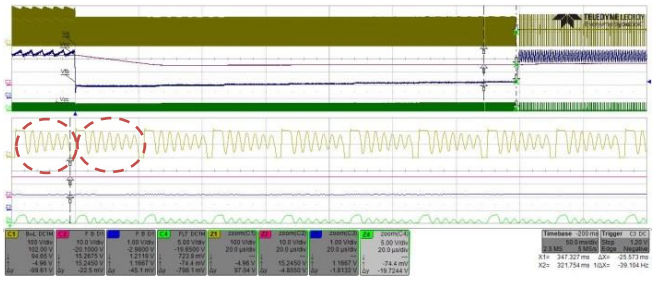
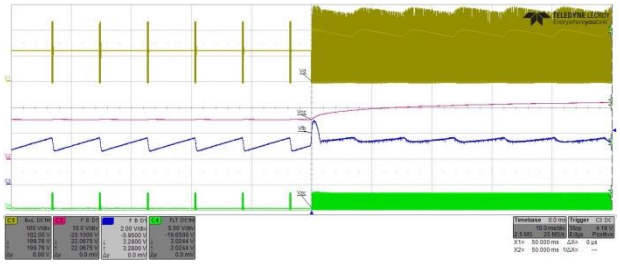
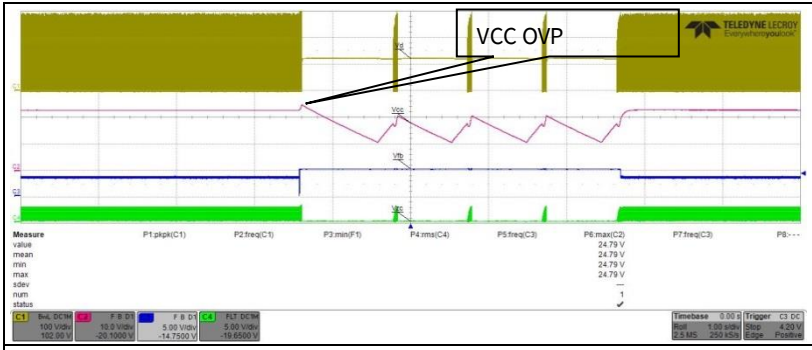
	
C1 (Yellow) : Current sense voltage (V_{CS}) C2 (Purple) : Supply voltage (V_{VCC}) C2 (Blue) : Feedback voltage (V_{FB}) C2 (Green) : Zero crossing voltage (V_{ZC})	C1 (Yellow) : Current sense voltage (V_{CS}) C2 (Purple) : Supply voltage (V_{VCC}) C2 (Blue) : Feedback voltage (V_{FB}) C2 (Green) : Zero crossing voltage (V_{ZC})
Condition to enter burst: V_{FB}<1.2 V, N_{ZC}=7 and $t_{blanking}$ =24 ms (load change form full load to 1 W load at 85 V_{AC})	Condition to leave burst: V_{FB}>4.5 V (load change form full load to 1 W to full load at 85 V_{AC})

Figure 5 Active burst mode

11.9 VCC over voltage protection (Auto restart mode)

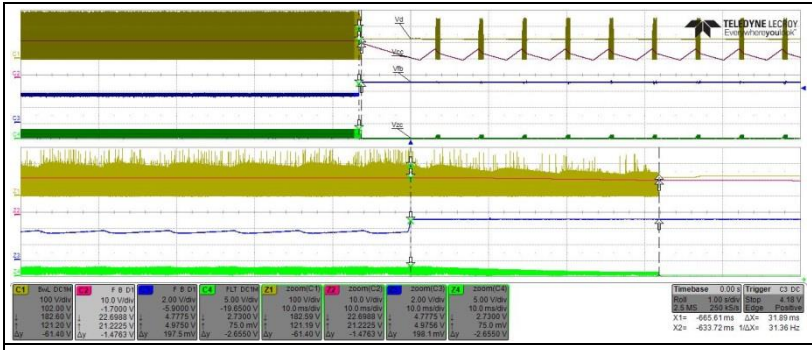


C1 (Yellow) : Drain voltage (V_D)
C2 (Purple) : Supply voltage (V_{VCC})
C2 (Blue) : Feedback voltage (V_{FB})
C2 (Green) : Zero crossing voltage (V_{ZC})

Condition to enter V_{VCC} over voltage protection: V_{VCC}>25 V
(85 V_{AC}, short the diode of optocoupler(Pin 1 and 2 of IC12) during system operating at light load and release)

Figure 6 Over load protection

11.10 Over load protection (Auto restart mode)

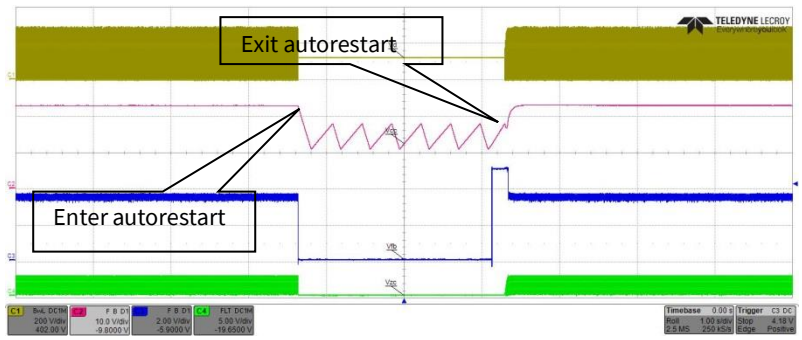


C1 (Yellow) : Drain voltage (V_D)
C2 (Purple) : Supply voltage (V_{VCC})
C2 (Blue) : Feedback voltage (V_{FB})
C2 (Green) : Zero crossing voltage (V_{ZC})

Condition to enter over load protection: V_{FB}>4.5 V & last for 40ms blanking time
(output load change from 2.33 A to 3.5 A at 85 V_{AC})

Figure 7 Over load protection

11.11 VCC under voltage/Short optocoupler protection (Auto restart mode)

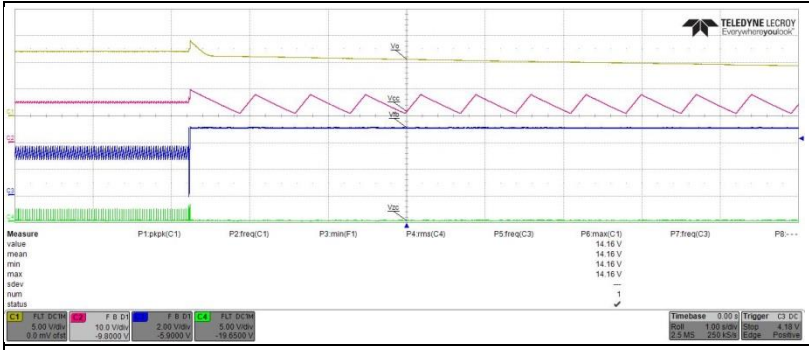


C1 (Yellow) : Drain voltage (V_D)
C2 (Purple) : Supply voltage (V_{VCC})
C2 (Blue) : Feedback voltage (V_{FB})
C2 (Green) : Zero crossing voltage (V_{ZC})

Condition to enter VCC under voltage protection: V_{CC} < 10.5 V
(short the transistor of optocoupler(Pin 3 and 4 of IC12) during system operating at full load and release at 85 V_{AC})

Figure 8 VCC under voltage/short optocoupler protection

11.12 Output overvoltage protection (Latch mode)



C1 (Yellow) : Output voltage (V_{out})
C2 (Purple) : Supply voltage (V_{VCC})
C2 (Blue) : Feedback voltage (V_{FB})
C2 (Green) : Zero crossing voltage (V_{ZC})

Condition to enter external protection enable: V_{out}>14 V (V_{ZC}>3.7 V)
(85 V_{AC}, short R26 during while system operation at no load)

Figure 9 External auto restart enableOutput overvoltage protection

12 References

[1] ICE2QR4780G datasheet, Infineon Technologies AG

[2] AN-PS0025-CoolSET F3R DIP-8, DIP-7, DSO-16/12 new jitter version design guide-V2.2

Revision History

Major changes since the last revision

Page or Reference	Description of change
--	First release.

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