EZ-USB™ FX3/FX3S/SX3 hardware design guidelines and schematic checklist

About this document

Scope and purpose

This application note discusses the recommended practices for EZ-USB™ FX3/FX3S/SX3 hardware design and the critical items that a developer must consider. EZ-USB™ FX3 is the next generation USB 3.0 peripheral controller. With its highly integrated and flexible features, developers can add USB 3.0 functionality to any system. All recommendations apply to FX3, FX3S, and SX3, unless specifically mentioned otherwise. For a complete list of USB SuperSpeed code examples, **click here**.

Table of contents

Table of contents

1 Introduction

Infineon' EZ-USB™ FX3 is a USB 3.0 peripheral controller, providing integrated and flexible features. EZ-USB™ FX3 has a fully-configurable, parallel, general programmable interface called GPIF II, which can connect to any processor, ASIC, or FPGA. It provides easy and glueless connectivity to popular interfaces, such as asynchronous SRAM, asynchronous and synchronous address data multiplexed interfaces, and parallel ATA. FX3 has an embedded 32-bit ARM926EJ-S microprocessor for powerful data processing and for building custom applications. It implements an architecture that enables 375 MBps data transfer from GPIF II to the USB interface.

An integrated USB 2.0 OTG controller enables applications in which FX3 may serve dual roles; for example, FX3 may function as an OTG Host to MSC as well as HID-class devices. FX3 contains 512 KB or 256 KB of on-chip SRAM for code and data. FX3 also provides interfaces to connect to serial peripherals such as UART, SPI, I^2C, and I2S. FX3 comes with application development tools. The software development kit comes with application examples for accelerating time to market.

In addition to these features, FX3S has an integrated storage controller and can support up to two independent mass storage devices. It can support SD 3.0 and eMMC 4.41 memory cards. It can also support SDIO on these ports. Feature differences between FX3 and FX3S are listed in **Table 1**. You should follow several guidelines for trace width, stack-up, and other layout considerations to make sure the system performs as expected.

A reference schematic for the SuperSpeed explorer kit is available at **CYUSB3KIT-003 EZ-USB™ FX3 SuperSpeed explorer kit**. A reference schematic for the EZ-USB™ FX3 DVK is available at **CYUSB3KIT-001 EZ-USB™ FX3**. Contact **Cypress Developer Community** for EZ-USB™ FX3S DVK schematics. Click **here** for SX3 kits.

Table 1 Feature differences between FX3 and FX3S

Feature	FX3	FX3S
GPIF	8/16/32-bit	8/16-bit
Storage ports	No	1 or 2 ports (SD3.0, eMMC4.41, SDIO3.0)
USB 3.0, USB 2.0 Device	Yes	Yes
HS-OTG	Yes	Yes
CPU	ARM9, 200 MHz	ARM9, 200 MHz
Embedded SRAM	256KB/512KB	256KB/512KB
Serial interfaces1	I^2C, SPI, I^2S, UART	I^2C, SPI, I^2S, UART
Boot options	I^2C, SPI, USB, GPIF-based	All FX3 boot options + eMMC-based boot options
Package	121-pin BGA, 10×10 mm	121-pin BGA, 10×10 mm

Note:

1. *If you are designing hardware using EZ-USB™ CX3, see **AN90369** for the guidelines on routing MIPI CSI-2 Signals.*
2. *If you are designing hardware using EZ-USB™ SX3, see **AN231295** for feature differences between FX3 and SX3.*

1 All serial interfaces might not be available under all configuration options. See the pin description section in the datasheet for details.

2 Related resources

Cypress provides a wealth of data at **Cypress developer community** to help you to select the right FX3 device for your design, and to help you to quickly and effectively integrate the device into your design.

- USB 3.0 product selectors: **FX3, FX3S, SD3, CX3, SX3**
- Application notes: Infineon offers a large number of USB application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with FX3 are:
  - **AN231295 - Getting started with EZ-USB™ SX3**
  - **AN75705 - Getting started with EZ-USB™ FX3**
  - **AN76405 - EZ-USB™ FX3 boot options**
  - **AN65974 - Designing with the EZ-USB™ FX3 slave FIFO interface**
  - **AN75779 - How to implement an image sensor interface with EZ-USB™ FX3 in a USB video class (UVC) framework**
  - **AN86947 - Optimizing USB 3.0 throughput with EZ-USB™ FX3**
  - **AN84868 - Configuring an FPGA over USB using EZ-USB™ FX3**
  - **AN68829 - Slave FIFO interface for EZ-USB™ FX3: 5-bit address mode**
  - **AN76348 - Differences in implementation of EZ-USB™ FX2LP and EZ-USB™ FX3 applications**
  - **AN89661 - USB RAID 1 disk design using EZ-USB™ FX3S**
  - **AN90369 - How to interface a MIPI CSI-2 image sensor with EZ-USB™ CX3**
  - **See more SX3 application notes in page 3 of SX3 datasheet.**
- Code examples:
  - **USB Hi-Speed**
  - **USB Full-Speed**
  - **USB SuperSpeed**
- Technical reference manual (TRM):
  - **EZ-USB™ FX3 technical reference manual**
  - **EZ-USB™ CX3 technical reference manual**
- Development kits:
  - **CYUSB3KIT-003, EZ-USB™ FX3 SuperSpeed explorer kit**
  - **CYUSB3KIT-001, EZ-USB™ FX3 development kit**
  - Visit the SX3 **website** to view the development kits available for SX3.
- Models: **IBIS**

2.1 EZ-USB™ FX3 software development kit

Cypress delivers the complete software and firmware stack for FX3, to easily integrate SuperSpeed USB into any embedded application. The **software development kit** (SDK) comes with tools, drivers and application examples, which help accelerate application development.

Note: *EZ-USB™ SX3 can be programmed using the **EZ-USB™ SX3 configuration utility**.*

2.2 GPIF II designer

The **GPIF II designer** is a graphical software that allows designers to configure the GPIF II interface of the EZ-USB™ FX3 USB 3.0 device controller.

The tool allows users to select from one of five Infineon-supplied interfaces or choose to create their own GPIF II interface from scratch. Infineon has supplied industry-standard interfaces such as asynchronous and synchronous slave FIFO, and asynchronous and synchronous SRAM. Designers who already have one of these pre-defined interfaces in their system can simply select the interface of choice, choose from a set of standard parameters such as bus width (x8, 16, x32) endianness, clock settings, and compile the interface. The tool has a streamlined three-step GPIF interface development process for users who need a customized interface. Users can first select their pin configuration and standard parameters. Secondly, they can design a virtual state machine using configurable actions. Finally, users can view the output timing to verify that it matches the expected timing. Once the three-step process is complete, the interface can be compiled and integrated with FX3.

3 Power system

3.1 Overview

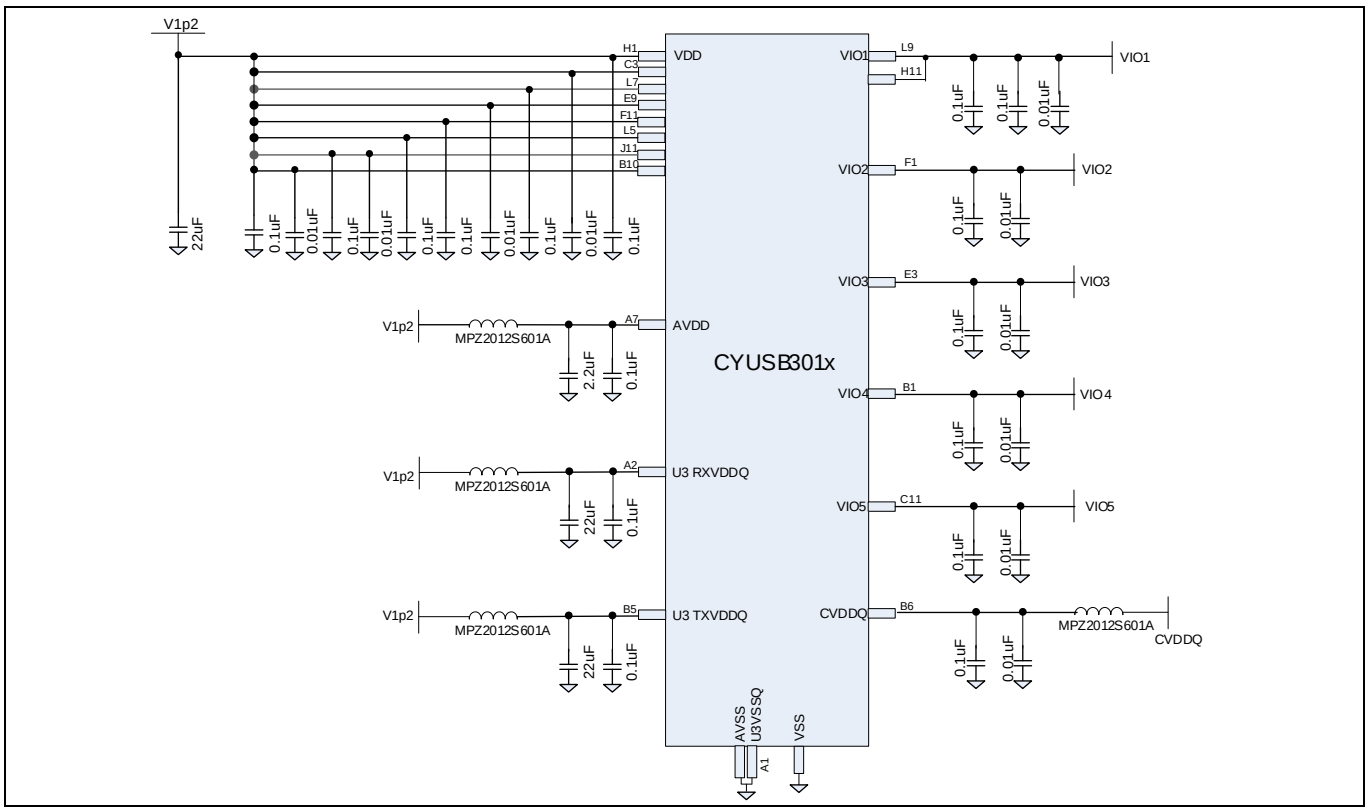

Figure 1 EZ-USB™ FX3/FX3S/SX3 power domains

Table 2 EZ-USB™ FX3/FX3S/SX3 power domains

Parameter	Description	Min	Typical	Max	Unit
V_{DD}	Core voltage supply	1.15	1.2	1.25	V
A_{VDD}	Analog voltage supply	1.15	1.2	1.25	V
V_{IO1}	GPIF II I/O power domain	1.7	1.8, 2.5, and 3.3	3.6	V
V_{IO2}	IO2 power domain	1.7	1.8, 2.5, and 3.3	3.6	V
V_{IO3}	IO3 power domain	1.7	1.8, 2.5, and 3.3	3.6	V
V_{IO4}	UART/SPI/I^2S power domain	1.7	1.8, 2.5, and 3.3	3.6	V
V_{IO5}	I^2C and JTAG supply domain	1.15	1.2, 1.8, 2.5, and 3.3	3.6	V
V_{BATT}	USB voltage supply	3.2	3.7	6	V
V_{BUS}	USB voltage supply	4.0	5	6	V
C_{VDDQ}	Clock voltage supply	1.7	1.8, 3.3	3.6	V
$U3TX_{VDDQ}$	USB3.0 1.2-V supply	1.15	1.2	1.25	V
$U3RX_{VDDQ}$	USB3.0 1.2-V supply	1.15	1.2	1.25	V

4 Power modes

EZ-USB™ FX3/SX3 supports the following power modes:

- **Normal mode:** This is the full-functional operating mode. In this mode, the internal CPU clock and the internal PLLs are enabled.
  - The I/O power supplies VIO2, VIO3, VIO4, and VIO5 may be turned off when the corresponding interface is not in use. VIO1 may not be turned off at any time if the GPIF II/GPIO interface is used in the application.
  - The USB I/O requires a 3.3-V regulated power supply. This supply is internally driven from either the VBUS or VBATT external supplies. VBATT/VBUS can be turned OFF if USB is not used. If the USB port is used, one or both supplies must be present.
  - VBATT can be connected to the system battery or a stable 3.2 V–6 V voltage rail from the PMIC. If VBUS and VBATT are both present and in their specified ranges, VBUS becomes the primary supply to the USB I/O unless there is a software/firmware override. If VBUS is less than 4.1 V, then FX3/SX3 behaves as if no VBUS is connected to it. If this happens when the FX3/SX3 is powered, then FX3/SX3 does not enumerate at all. If this happens somewhere during the operation of FX3/SX3, then the FX3/SX3 firmware will turn off the USB PHY and disconnect from the host.
  - EZ-USB™ FX3 can withstand up to 6 V on the VBUS pin; in applications where this supply can see higher voltages, it is necessary to have an external overvoltage protection (OVP) device to protect the EZ-USB™ FX3/SX3 device. One example of such an application is a battery charging application, battery charging v1.2 spec. In this application, the charger (such as a wall/dedicated charger) can supply up to 9 V to the VBUS. We recommend the NCP360 USB overvoltage protection device for the VBUS pin.
  - The VBUS pin can be connected to an in-system supply rail that is switched on/off depending on VBUS detect by another processor. A typical scenario is a PMIC that detects VBUS and switches ON a regulated 3.3-V supply to EZ-USB™ FX3/SX3 as a result. In such a case, the system must use the software override to use VBATT as the primary supply.
  - EZ-USB™ FX3/SX3 does not contain a charge pump and therefore, cannot source the VBUS supply when used as an OTG-A device. When EZ-USB™ FX3/SX3 is used in an OTG-A mode, an external charge pump, either standalone or integrated in a PMIC, must be used to power VBUS.
- **Suspend mode with USB 3.0 PHY enabled (L1):** Power supply for the wakeup source and core power must be retained. All other power domains can be turned off/on individually.
- **Suspend mode with USB 3.0 PHY disabled (L2):** Power supply for the wakeup source and core power must be retained. All other power domains can be turned off/on individually.
- **Standby mode (L3):** Power supply for the wakeup source and core power must be retained. All other power domains can be turned off/on individually.
- **Core power down mode (L4):** Core power is turned off. All other power domains can be turned off/on individually.

4.1 Device supply decoupling

Power supply decoupling is critical in ensuring that system noise does not propagate into the device through the power supply. Improper decoupling can lead to jittery signaling, especially on the USB bus, which results in higher CRC error rate and more retries. Decoupling capacitors should be ceramic type of a stable dielectric. It is important to have the decoupling caps as close to the power pins as possible and short trace runs for the power and ground connections on the FX3/SX3 device to solid power and ground planes.

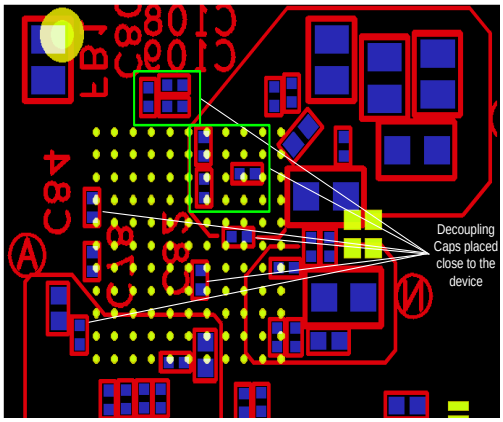

Figure 2 Placement of decoupling caps

The specific recommendation for the ceramic capacitor nearest to each FX3 power pin is given in **Table 3**.

Table 3 Power domain decoupling requirements

Power domain (pin numbers)	Capacitors for group	Capacitors per pin
VDD (B10, J11)	22 µF	0.01 µF and 0.1 µF
VDD (H1, L7, F11, L5)		0.1 µF
VDD (C3, E9)		0.01 µF
AVDD (A7)	2.2 µF	0.1 µF
U3RXVDDQ (A2)	22 µF	0.1 µF
U3TXVDDQ (B5)	22 µF	0.1 µF
CVDDQ (B6)	–	0.01 µF and 0.1 µF
VIO1 (L9, H11)	0.01 µF	0.1 µF
VIO2 (F1)	–	0.01 µF and 0.1 µF
VIO3 (E3)	–	0.01 µF and 0.1 µF
VIO4 (B1)	–	0.01 µF and 0.1 µF
VIO5 (C11)	–	0.01 µF and 0.1 µF
VBUS (E11)	–	0.1 µF

4.2 Inrush current and power supply design

When the USB3.0 SuperSpeed PHY is enabled for the first time, or a reset event; an initial inrush current is expected on the 1.2 V U3RXVDDQ and U3TXVDDQ supplies for ~10 µs. The magnitude of this current can be as high as 800 mA. In order that this inrush current does not cause the common 1.2-V supply to drop to unacceptable levels, care must be taken in the design of the power supply network for these supplies.

If the same 1.2-V supply is also used for the VDD core supply, ensure that the level on this supply does not fall too low, as this has the potential to trip the on-chip power-on reset (POR) circuit that will reset the entire chip. The POR circuit can fire if the 1.2-V core VDD voltage falls to less than 0.83 V for more than 200 ns. The 1.2-V power network must be designed such that the VDD does not drop below 0.83 V when an inrush event occurs. Proper combination of decoupling capacitors (as specified in the **datasheet**), inductor chokes, and regulator output impedance are required to make this possible.

Power modes

The following example waveforms show the inrush current (**Figure 4**) and resultant drop in VDD levels (**Figure 5**) when the current spike occurs. The results were obtained from a non-optimized power supply design using the TPS76801QD power regulator, 2.2-µF decoupling caps, and chokes as shown in **Figure 3**.

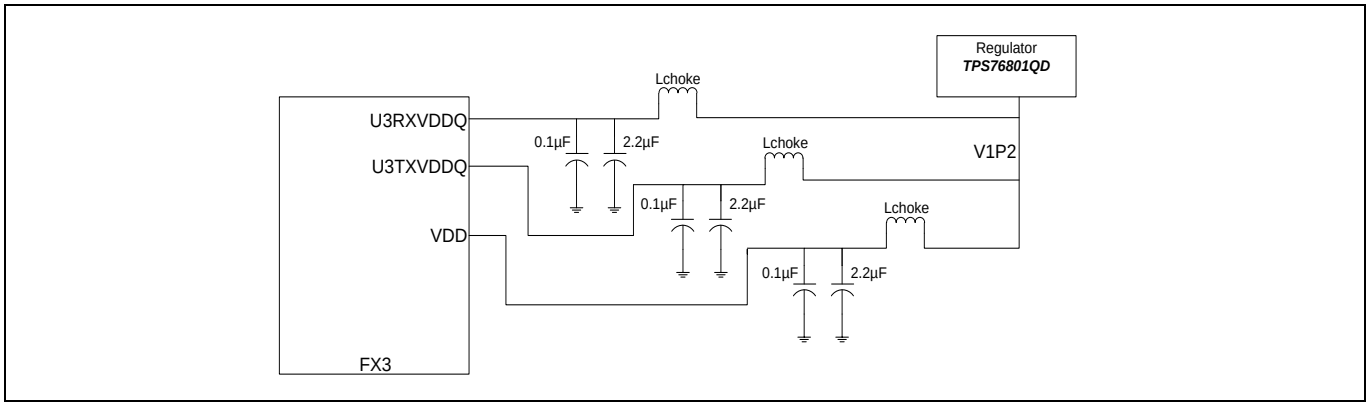

Figure 3 Non-optimized power supply design

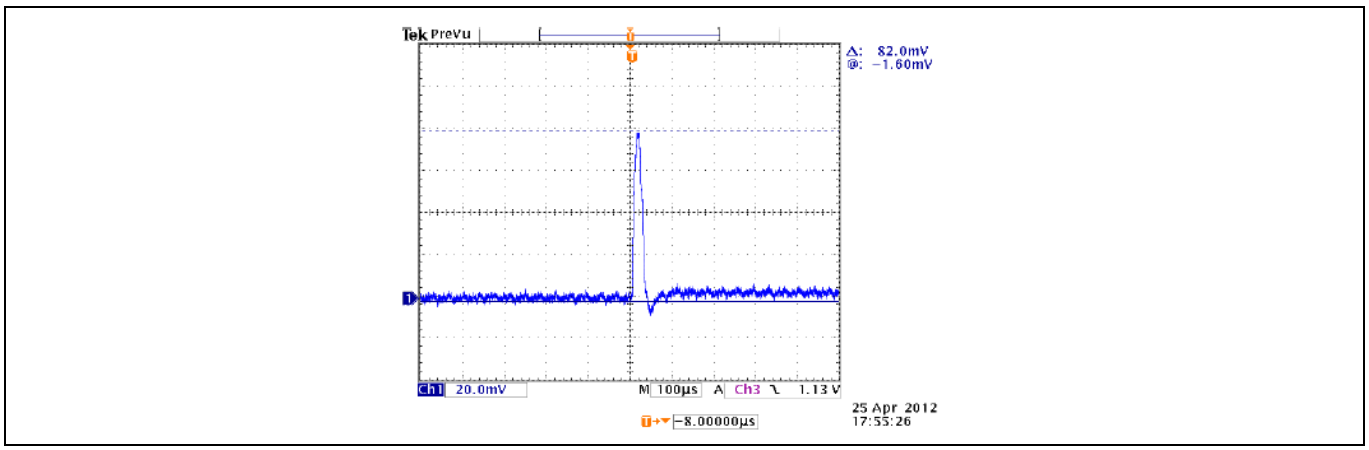

Figure 4 Inrush current (80 mV / 0.1 Ω = 800 mA)

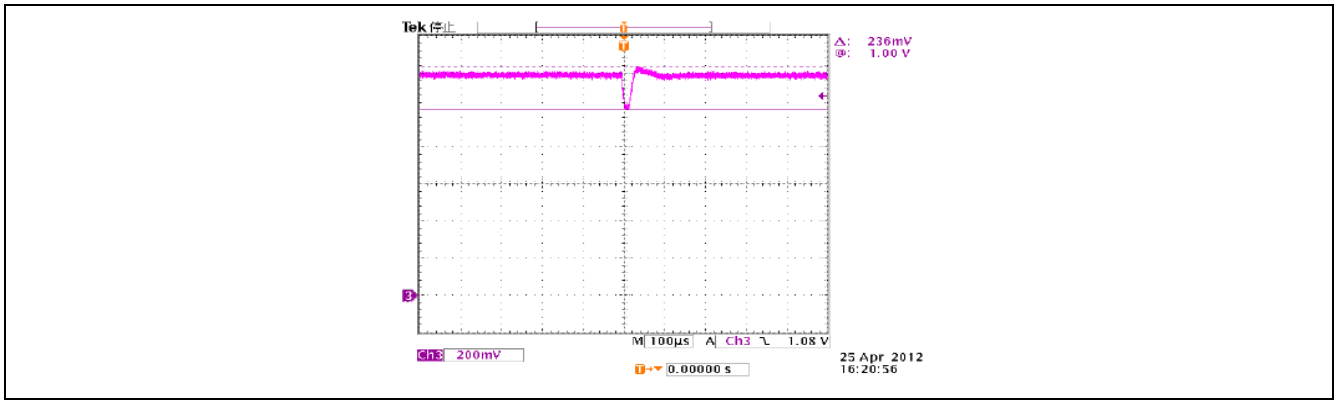

Figure 5 1.2-V power domain voltage drop (200 mV)

In contrast, an optimized power design shown in **Figure 6** designed using the same regulator (TPS76801QD), with the modification of using a 22-µF decoupling capacitor and removing the choke from the VDD supply, shows a reduction in the inrush (**Figure 7**) and an improvement in the power supply drop (**Figure 8**).

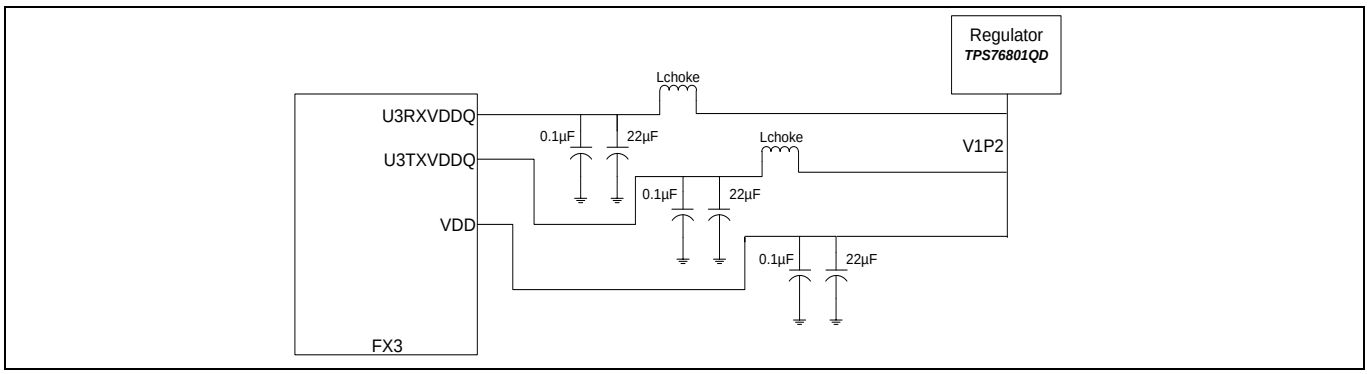

Figure 6 Optimized power supply design

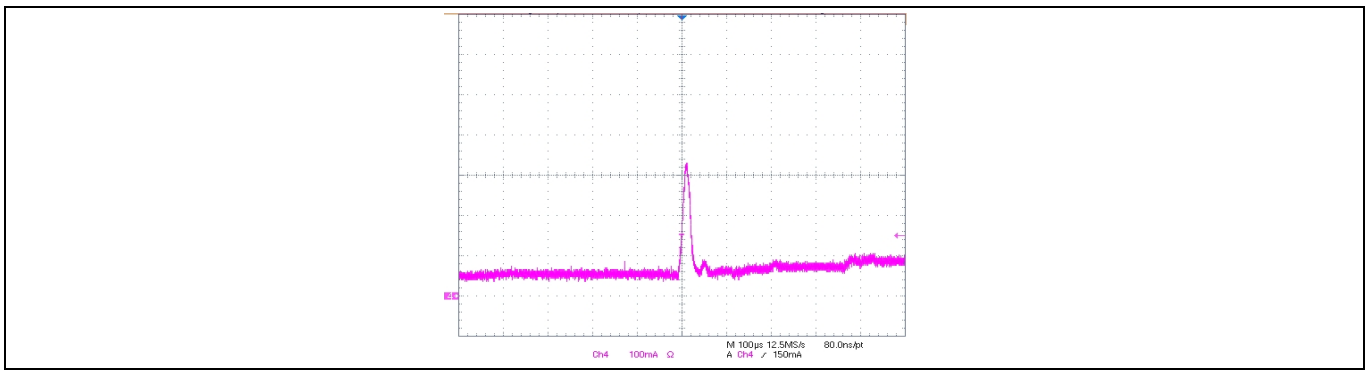

Figure 7 Inrush current (320 mA)

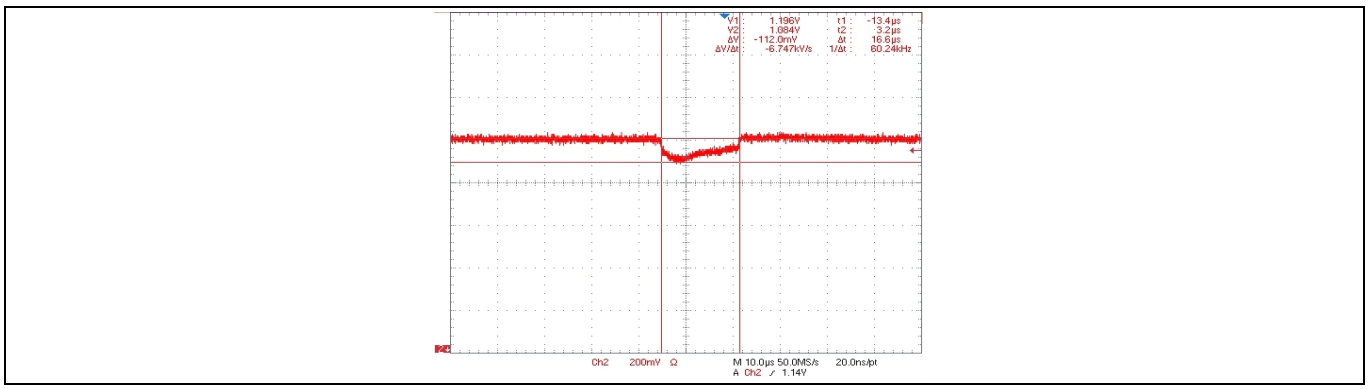

Figure 8 1.2-V power domain voltage drop (112 mV)

Customers can choose any regulator with similar specifications.

It is always a good practice to isolate different power supplies from each other. If you are shorting I/O power supplies (VIO1-5) to CVDDQ, it is always recommended to isolate CVDDQ using a choke (as shown in **Figure 1**). This will help in reducing the PHY errors. Also, operating VIO1 at lower voltages (1.8 V) helps in reducing the PHY errors.

5 Clocking

The EZ-USB™ FX3/SX3 device can use either of these options as the clocking source:

- 19.2-MHz crystal
- 19.2-MHz, 26-MHz, 38.4-MHz, or 52-MHz external clock

5.1 Crystal

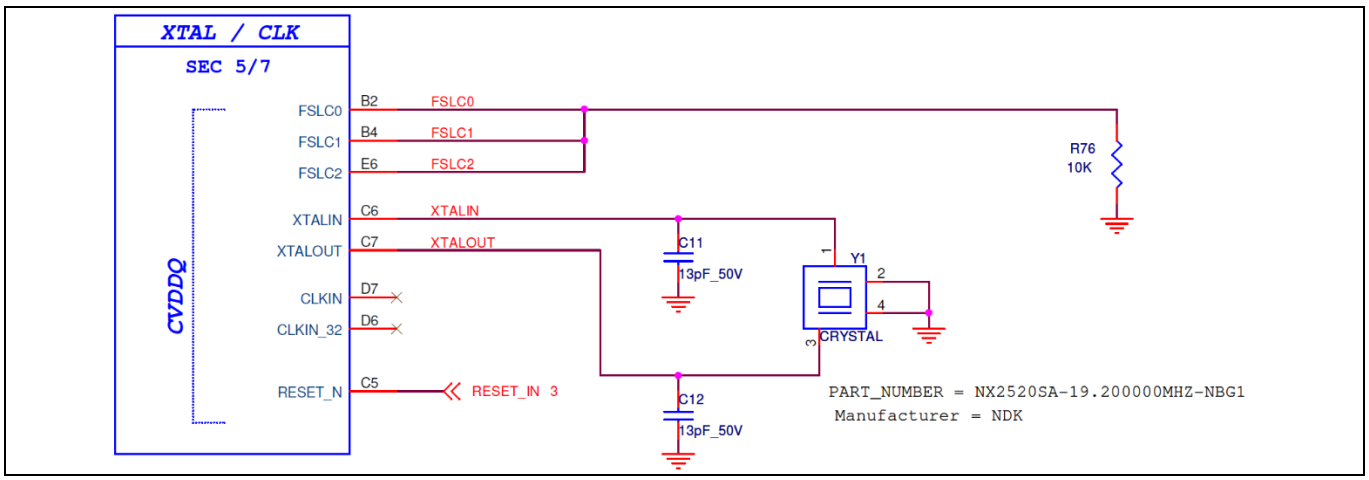

Figure 9 Crystal circuit

Table 4 19.2-MHz crystal requirements

Parameter	Specification	Unit
Tolerance	±100	Ppm
Temp range	–40 to 85	°F
Drive level	Use **Equation 1**	mW

The power dissipation of the crystal depends on the following:

- Drive level of the XTALOUT pin (for FX3/SX3, this is 1.32 V)
- Desired frequency (19.2 MHz)
- Equivalent resistance of the crystal.

Equation 1. Power dissipation of the crystal

$$P = I^2R = \left(\frac{V_x}{|Z|}\right)^2 R = 2[\pi f\ (C_0 + C_L)\ V_x]^2 R$$

Where:

f is the crystal frequency,

C_0 is the shunt capacitance of the crystal obtained from the crystal datasheet

C_L is the load capacitance, for C_L calculation, see the **next** section

R is the crystal ESR obtained from the datasheet of the crystal

V_x is the maximum voltage on XTALOUT pin – 1.32 V

Use of a crystal with a drive level less than the crystal's power dissipation may result in accelerated aging or even burnout of the crystal.

Examples of compatible crystals are shown in **Table 5**. Note that only the NX3225SA was characterized with the EZ-USB™ FX3/SX3, and the rest for the crystals are provided as examples using **Equation 1**.

Table 5 Crystal selection

Device	Max R1 (Ω) from datasheet	CL Eqv (pF)	C0 (pF) estimate	Drive level using equation 1 (µW)	Max drive level (spec) µW
NX2520SA-19.200000MHZ-NBG1	60	13	Nil	128	200
ECS-192-13-30B-AEM-TR	50	13	Nil	107	300
7V-19.200MDIQ-T	60	10	Nil	76	100
ECS-192.0-8-36-RWN-TR	80	8	Nil	65	100

Note: Do not connect any series resistor to the XTALOUT and XTALIN pins of the crystal. Placing a series resistor will add resistance to the crystal ESR, resulting in increased crystal power dissipation and startup time.

5.1.1 Crystal effective load capacitor calculation

Load capacitance C_L plays a critical role in providing an accurate clock source to FX3/SX3. The capacitors C_1 and C_2 (as shown in **Figure 9**) must be chosen carefully based on the load capacitance value of the crystal.

The load capacitance is calculated using the following equation:

Equation 2. Load capacitance of a crystal

$$C_L = \frac{C_1 * C_2}{C_1 + C_2} + C_S$$

C_S is the stray capacitance of XTALOUT and XTALIN traces on the PCB. Usually the value of C_S is around 2-8 pF if you follow good layout practice and keep the trace from the crystal to the pins on the FX3/SX3 as short as possible. It is better to assume the Cs of 5pF.

For the crystal used in FX3/SX3 development kit, C_L = 13 pF. FX3 PCB C_S = 7 pF. From equation 2, $C_1 = C_2$ = 12 pF.

5.1.2 Clock

Clock inputs to EZ-USB™ FX3/SX3 must meet the phase noise and jitter requirements specified in the following table.

Table 6 Clock requirements

Parameter	Description	Specification		Units
		Min	Max	
Phase noise	100-Hz Offset	–	–75	dB
	1-kHz Offset	–	–104	dB

	10-kHz Offset.	–	–120	dB
	100-kHz Offset	–	–128	dB
	1-MHz Offset	–	–130	dB
Maximum frequency deviation		–	150	ppm
Duty cycle		30	70	%
Overshoot		–	3	%
Undershoot		–	–3	%
Rise time/fall time		–	3	ns

Based on the clocking option that is used, the frequency select, FSLC[2:0], lines can be tied to power, through a weak pull-up resistor, or to ground.

Table 7 shows the values of FSLC[2:0] for the different clocking options.

ASEMB-19.200MHZ-LY-T is the recommended 19.2-MHz clock oscillator part. We recommend ECS-2530MV-260-BN-TR, SIT8008BI-71-33N-38.400000, SIT8008AC-73-33E-52.000000 are the part numbers for 26 MHz, 38.4 MHz, and 52 MHz respectively.

Table 7 Frequency select configuration

`	FSLC[1]	FSLC[0]	Crystal/clock frequency
0	0	0	19.2-MHz crystal
1	0	0	19.2-MHz input clock
1	0	1	26-MHz input clock
1	1	0	38.4-MHz input clock
1	1	1	52-MHz input clock

CVDDQ supply is the supply associated with the clock input. It should be set to the same voltage level as the external clock input (if any).

If only external clock input is used, the XTALIN and XTALOUT pins can be left unconnected. If only crystal clocking is used, the CLKIN pin can be left unconnected.

5.2 Watchdog timer

A 32.768-kHz clock input can be used for the watchdog timer operation during Standby mode. This may be optionally supplied by an external source.

Table 8 Watchdog timer requirements

Parameter	Min	Max	Unit
Duty cycle	40	60	%
Frequency deviation	–	±200	ppm

6 GPIF II interface

EZ-USB™ FX3 offers a high-performance general programmable interface, GPIF II. This interface enables functionality similar to, but more advanced than, **FX2LP**'s GPIF and Slave FIFO interfaces. See the application note **AN75779 – Interfacing an image sensor to EZ-USB™ FX3 in a USB video class (UVC) framework**, for more details on the GPIF interface.

The following are some general design guidelines for the EZ-USB™ FX3's GPIF II interface.

- The maximum frequency of the GPIF II interface is 100 MHz. It is recommended that all lines on the GPIF II bus are length-matched within 500 mils. The 500-mil requirement ensures that the delay between the signals lie within 1% of the total period considering the typical propagation delays for stripline and microstrip traces in PCBs (150 to 200 ps/inch). The reflection phenomenon occurs due to impedance mismatch of GPIF lines and also due to the PCB stackup. Therefore, you must use 22-Ω series termination resistors to avoid reflection on these lines.
- If the GPIF lines are to be routed for more than 5 inches or routed through a medium that can cause impedance mismatch, we recommend doing signal integrity simulation using the **EZ-USB™ FX3 IBIS model**, and come up with a termination.
- GPIO[16] (PCLK) should be used as the GPIF II clock signal in all synchronous interfaces.
- GPIO[32:30] (PMODE[2:0]) signals should be configured appropriately at FX3 boot-up. After boot-up, these signals can be used as GPIOs.
- INT# signal cannot be used as a GPIO. This pin can be either left floating or pulled up to VIO1 if it is not used.

Note: *SPI interface lines are not available when GPIF II is configured in 32-bit mode. However, it is still possible to use the SPI interface for booting and then configure GPIF II to 32-bit mode.*

7 USB

The OTG_ID pin can be left unconnected if FX3/SX3 is used as a USB device only. This pin must be connected to ground if you are using FX3 as a dual role device.

8 Low-performance peripherals (LPP)

8.1 I²C interface

EZ-USB™ FX3/SX3 has an I²C interface compatible with the I²C bus specification revision 3. EZ-USB™ FX3/SX3's I²C interface is capable of operating as I²C master only. For example, EZ-USB™ FX3/SX3 may boot from an EEPROM connected to the I²C interface, as a selectable boot option. EZ-USB™ FX3's I²C master controller also supports the multi-master mode functionality.

The power supply for the I²C interface is VIO5, which is a separate power domain from the other serial peripherals. This is to allow the I²C interface the flexibility to operate at a different voltage than the other serial interfaces.

The bus frequencies supported by the I²C controller are 100 kHz, 400 kHz, and 1 MHz. When VIO5 is 1.2 V, the maximum operating frequency supported is 100 kHz. When VIO5 is 1.8 V, 2.5 V, or 3.3 V; the operating frequencies supported are 400 kHz and 1 MHz.

If an external EEPROM is used on the I²C bus for firmware image booting, 2-kΩ pull-up resistors should be placed on the SCL and SDA lines for proper operation.

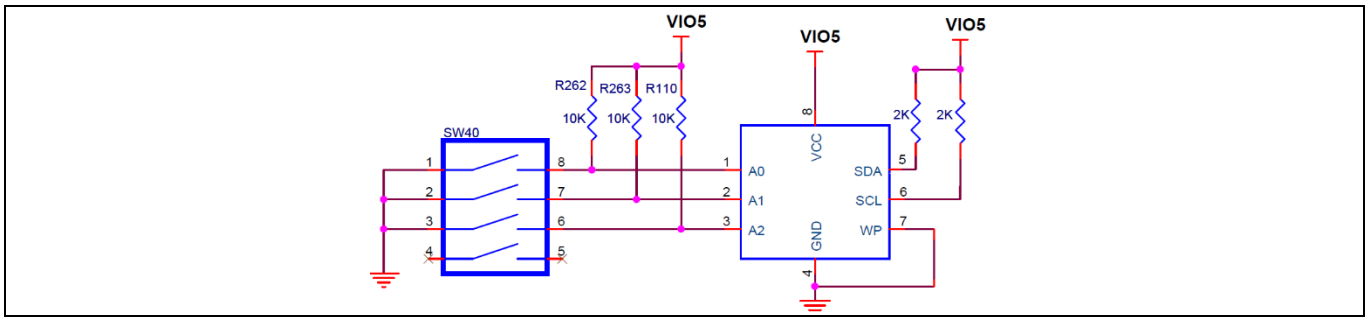

Figure 10 I²C configuration

Note: Address pins A0, A1, and A2 of the EEPROM should be connected per the recommendations in the EEPROM datasheet.

8.2 JTAG

EZ-USB™ FX3/SX3 has a JTAG interface to provide a standard five-pin interface for connecting to a JTAG debugger. This feature enables firmware debugging through the CPU core's on-chip debug circuitry.

There is no need for external pull-up/down on the JTAG signals as the JTAG signals TDI, TMC, TRST# have fixed 50 kΩ internal pull-ups and the TCK signal has a fixed 10 kΩ pull-down resistor.

Note that the FX3/SX3/FX3S does not support boundary scan. The JTAG interface available in these devices is for debugging purpose only.

8.3 I²S

EZ-USB™ FX3 has an I²S port to support external audio codec devices. EZ-USB™ FX3 functions as an I²S master (**transmitter only**). EZ-USB™ FX3 can generate the system clock as an output on the I2S_MCLK line or accept an external system clock input on the same line.

8.4 SPI and UART

EZ-USB™ FX3/SX3 supports an SPI master interface on the serial peripherals port. The SPI GPIOs are shared with the UART GPIOs. There should be no pull-up on SPI MISO/MOSI lines to allow FX3/SX3 to boot from SPI flash. It is recommended to include a pull-down resistor (2K) on the MISO line. **Figure 11** shows the correct SPI signal connection using the M25P40-VMN6TPB SPI device.

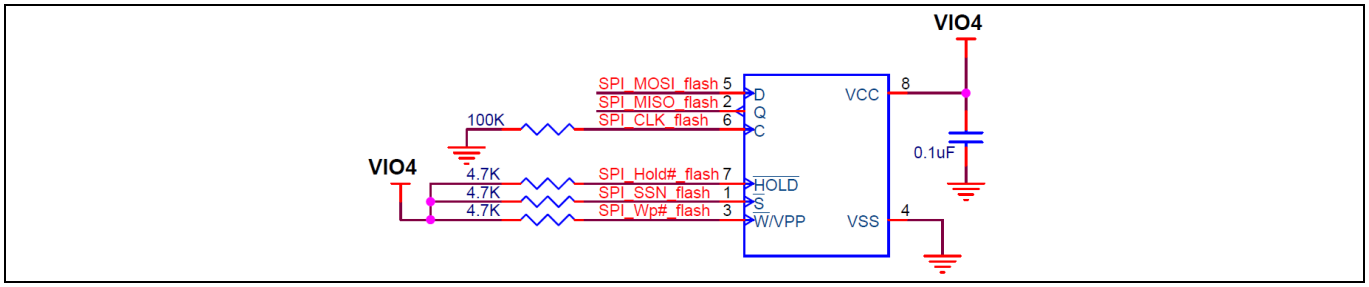

Figure 11 SPI configuration

8.5 Selection of SPI flash

Use the following guidelines while selecting the SPI flash:

- Flash size: 1 Kbit–128 Mbit are supported.
- Voltage: 1.7 V–3.6 V are supported.
- Command set: SPI flash should support the following commands to support FX3/SX3 boot.
  - Read data: 03h with 3-byte addressing
  - Read status register: 05h
  - Write enable: 06h
  - Write data (Page Program): 02h
  - Sector erase: D8h

An SPI flash can be used for FX3 boot if the read commands match. If there are any differences in the write commands, then programming of that SPI flash will not be successful with the default Infineon-provided programmer utility (USB control center utility). It requires rebuilding the firmware binary file used by the utility with the modified write commands for successful programming of the SPI flash. Hence, we recommend using a SPI flash compatible with the above read/write command set.

The following are the supported SPI flash parts:

- Infineon parts: S25FS064S(64-Mbit), S25FS128S(128-Mbit), and S25FL064L(64-Mbit)
- Winbond part: W25Q32FW (32-Mbit), W25Q80BW (8-Mbit), W25X20 (2-Mbit)
- Micron Technology part: M25P40 (4-Mbit)

8.6 Hybrid SPI flash usage

Some flash devices come with hybrid sectors (the first sector of 64KB divided into 9 sectors (8 sectors of 4KB and one 32KB sector). All remaining sectors are uniform (64KB each). When you use the Control Center application from the FX3 SDK, the internal programming utility (*CyBootProgrammer.img*) assumes uniform sector size for the flash device; this leads to corrupted data in the first sector, which is a hybrid sector. To prevent this, configure the flash device to use uniform sectors of 64KB each by modifying the appropriate configuration register. See **KBA231163** to learn more about using hybrid SPI flash devices.

9 Booting

EZ-USB™ FX3 can be either the main processor in a system or a co-processor to another main processor. The booting option you use depends on the specific system implementation. PMODE[2:0] configures the boot option and can be connected directly to the main processor or hardwired on the board depending on the booting option that will be used. The following table shows the levels of the PMODE[2:0] signals required for the different booting options.

Table 9 PMODE signals setting

PMODE[2:0]	Boot from
Z00	Sync ADMUX (16-bit)
Z01	Async ADMUX (16-bit)
Z11	USB boot
Z1Z	I^2C, on failure, USB boot is enabled
1ZZ	I^2C only
0Z1	SPI, on failure, USB boot is enabled

*Note: Z = High-Z, Open drain, No connect, *Applies to FX3S only*

We recommend adding pull-up and pull-down options (using 10 KΩ) on the PMODE[2:0] signals and load the combination needed for preferred booting option. This will give the flexibility to debug the system during early development.

SX3 operates only on two boot modes; USB boot (Z11) and SPI boot (0Z1).

10 EMI and ESD considerations

You must consider EMI and ESD on a case-by-case basis relative to the product enclosure, deployment environment, and regulatory statutes. This application note does not give specific recommendations regarding EMI, EZ-USB™ FX3 meets EMI requirements outlined by FCC 15B (USA) and EN55022 (Europe) for consumer electronics. EZ-USB™ FX3 can tolerate reasonable EMI, which is conducted by the aggressor, outlined by these specifications and continue to function as expected. However, this application note gives general EMI and ESD considerations. See **Appendix A – PCB layout tips** for general information on PCB layout techniques. You can also see 'Appendix A: PCB layout tips of **AN61290 - PSoC™ 3 and PSoC™ 5LP hardware design considerations**, which has a list of layout tips to improve EMI/EMC.

EZ-USB™ FX3/SX3 has built-in ESD protection on the D+, D-, and GND pins on the USB interface. The ESD protection levels provided on these ports are:

- ±2.2-kV human body model (HBM) based on ±6-kV contact discharge and ±8-kV air gap discharge based on IEC61000-4-2 level 3A
- ±8-kV contact discharge and ±15-kV air gap discharge based on IEC61000-4-2 level 4C.

This protection ensures the device will continue to function after ESD events up to the levels stated.

The SSRX+, SSRX-, SSTX+, SSTX- pins have only up to ±2.2-kV human body model (HBM) internal ESD protection.

You can include additional protection to these pins by using high-performance, low-capacitance external ESD devices (SP3010-04UTG), as shown in **Figure 12**. To prevent an effect on the performance of this bus, the added capacitance should not exceed 0.5 pF.

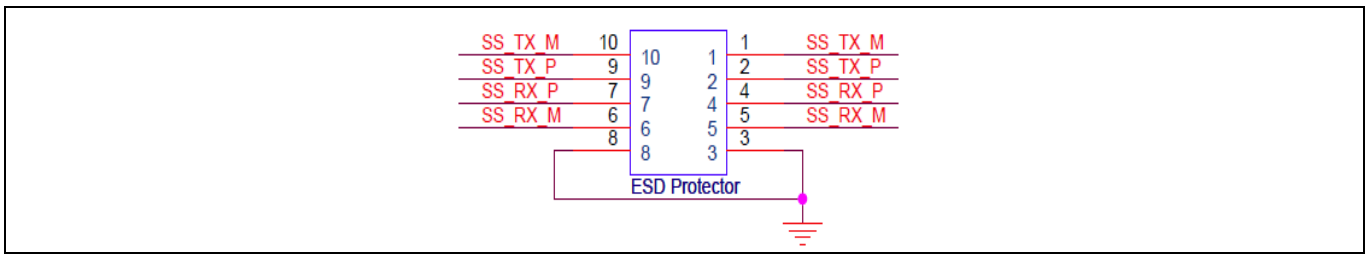

Figure 12 Low-capacitance external USB SuperSpeed (SS) ESD protection

In terms of EMI, all signal and clock traces emit electromagnetic (EM) radiation when they switch from one level to another. To meet the various standards in different countries, these emissions must be minimized. You can use several techniques to lower EM emissions:

- Consider putting the power and ground planes as the outside layers with signal layers underneath.
- Always have solid copper fills beneath integrated circuits and clocks.
- Ensure an adequate ground return path for all signals.
- Minimize the trace length of high speed and high current traces.

11 FX3/SX3 device package dimensions

EZ-USB™ FX3/SX3 is packaged on a 10 × 10 mm, 0.8-mm pitch ball grid array (BGA). We recommend the following:

- BGA pad size: 11 mils
- Solder mask size: 11 mils
- Solder paste size: 11 mils

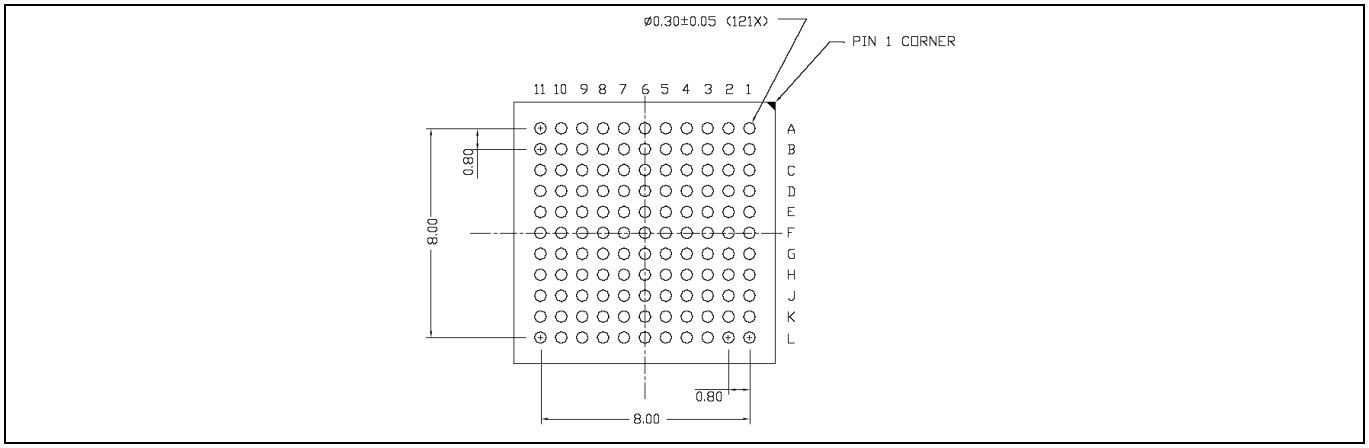

Figure 13 EZ-USB™ FX3/SX3 package dimensions

12 Electrical design considerations

USB 3.0 protocol enhances USB speed up to 5 Gbps. By including SuperSpeed (SS) lines along with High Speed (HS) lines, it is backward compatible with the USB 2.0 specification. Both buses require a greater level of attention to electrical design. Careful attention to component selection, supply decoupling, signal line impedance, and noise are required when designing for SuperSpeed USB. These physical issues are mostly affected by the PCB design. See **Appendix A – PCB layout tips** for general information on PCB layout techniques.

12.1 USB 3.0 SuperSpeed design guidelines

EZ-USB™ FX3/SX3 has SuperSpeed USB lines and Hi-Speed USB lines. Use the following best practices when designing with these buses:

- Minimize the trace length of USB lines as much as possible (<3 inches). These should be routed first to make sure certain recommendations on this list are achievable. Long traces affect the transmitter quality and introduce intersymbol interference (ISI) on the receive side.
- The polarity can be swapped on the USB 3.0 differential pairs. Polarity detection is done automatically by the USB 3.0 PHY during link training, as defined in the USB3.0 specification section 6.4.2, and does not require any additional changes to device firmware. Given the different USB connectors pinouts, the polarity inversion mechanism can be used to ensure that USB traces do not cross each other.
- Tie the R_USB2 pin to ground through a 1% 6.04-kΩ precision resistor. The R_USB3 pin should be tied to ground through a 1% 200-Ω precision resistor. See **Figure 14**.

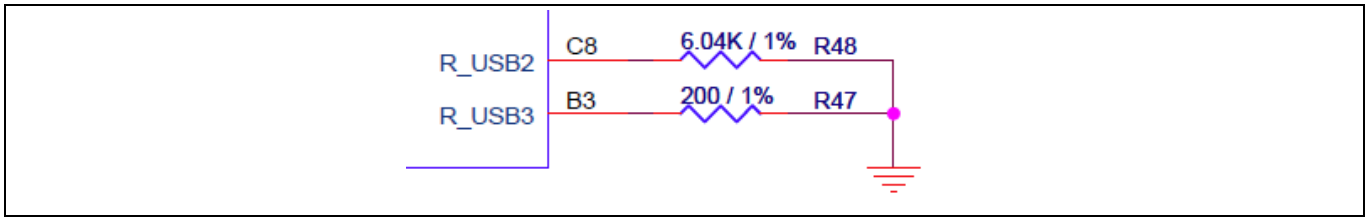

Figure 14 USB2 and USB3 reference resistors

- USB 3.0 traces require additional AC coupling capacitors (0.1 µF) placed on the SS_TX lines. Place these capacitors symmetrically and close to the EZ-USB™ FX3 device. See **Figure 15**.

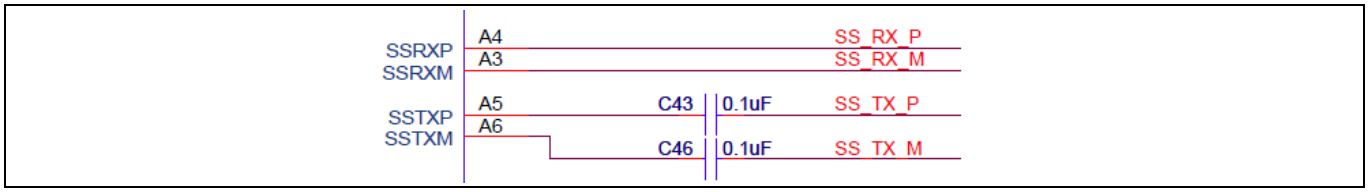

Figure 15 SuperSpeed TX line decoupling caps

- AC coupling capacitors should have a cut-out in the shape of these capacitors on the immediate solid GND layer to reduce reflection on the super speed signals. It is mandatory to provide the ground reference on layer, which is immediate to solid GND layer. **Figure 16** shows the proper layout of the decoupling caps; **Figure 17** shows the AC capacitor/ESD cutout. AC caps should be placed near to USB connector only for Host and device implementation which helps to avoid the cable noise reaching to FX3 device. AC caps should be placed near to FX3 device only if FX3 connected to HUB or other emdedded controller.

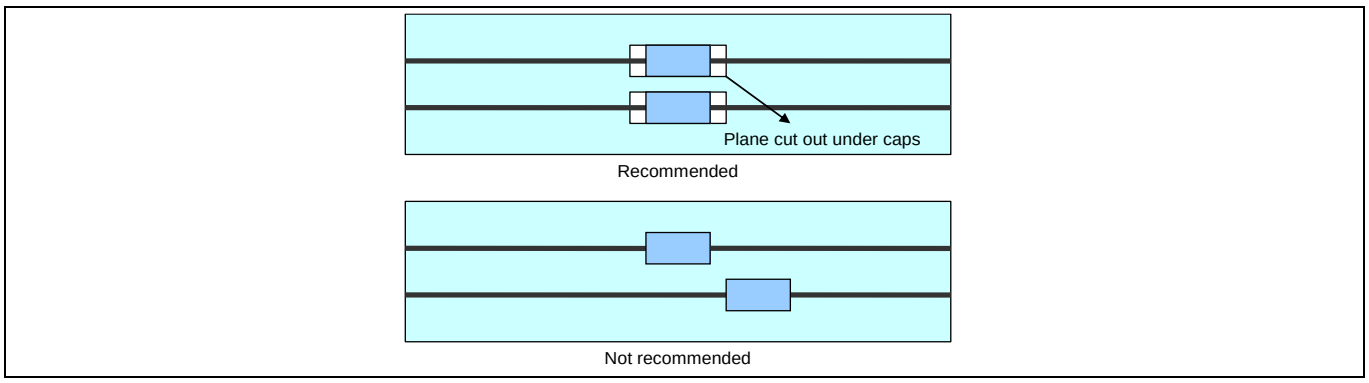

Figure 16 SuperSpeed TX AC coupling caps layout

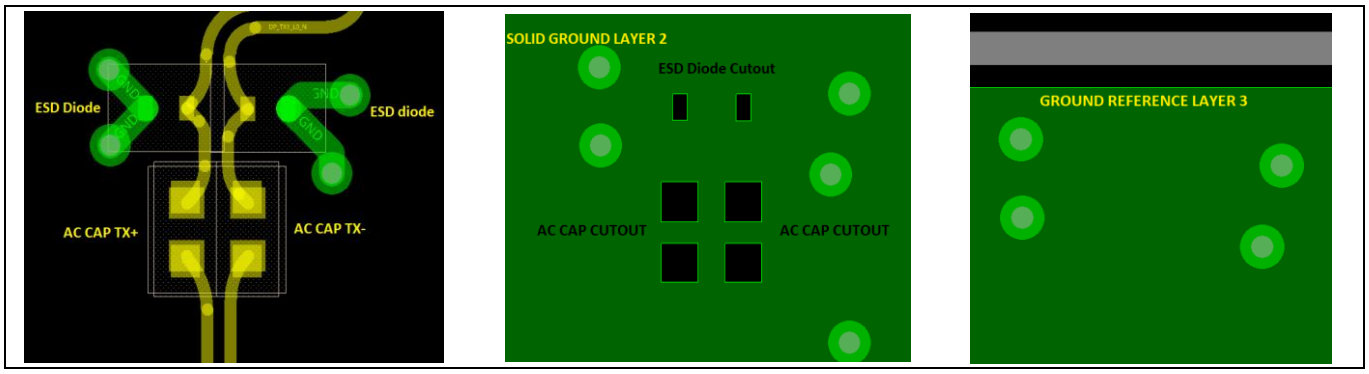

Figure 17 AC capacitor /ESD cutout

- Keep the USB signal line impedance at 90 Ω differential (±7%).
- Fill the space between the two differential pairs with ground. Maintain a minimum of 2W space between the ground and the differential pairs, where W = trace width.
- Keep the crystal trace as short as possible. Place the crystal within 2 cm from FX3/SX3.
- We recommend not to have vias on XTAL IN and XTAL OUT traces.
- Do not place any Hi-Speed signal and reset signal trace near to the crystal. If needed due to space constraints, fill the space with ground.
- Place the capacitor used in the RC reset circuitry as close as possible to the reset pin of FX3/SX3.
- Use split planes on the power layer for different power domains.
- Keep the power traces away from Hi-Speed data and clock lines.
- Power trace widths should be ≥25 mils to reduce inductance.
- Keep power traces as short as possible. Use larger vias (at least 30-mil pad, 15-mil hole) on power traces.
- Avoid any split in the immediate plane under the USB lines. The presence of split under the USB trace will result in variation of characteristic impedance at that point.
- Keep trace spacing between differential pairs consistent to avoid impedance mismatches as shown in the **Figure 18**.

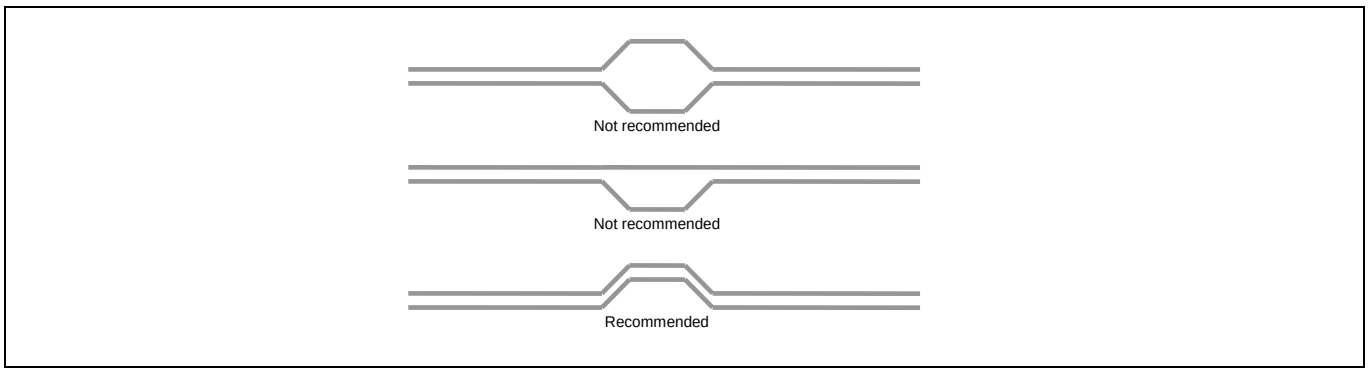

Figure 18 Differential pairs impedance matching techniques

- All SS signal lines should be routed entirely over a solid ground plane on an adjacent layer. Splitting the ground plane underneath the SS signals increases loop inductance introduces impedance mismatches and increases electrical emissions. See **Figure 19**.

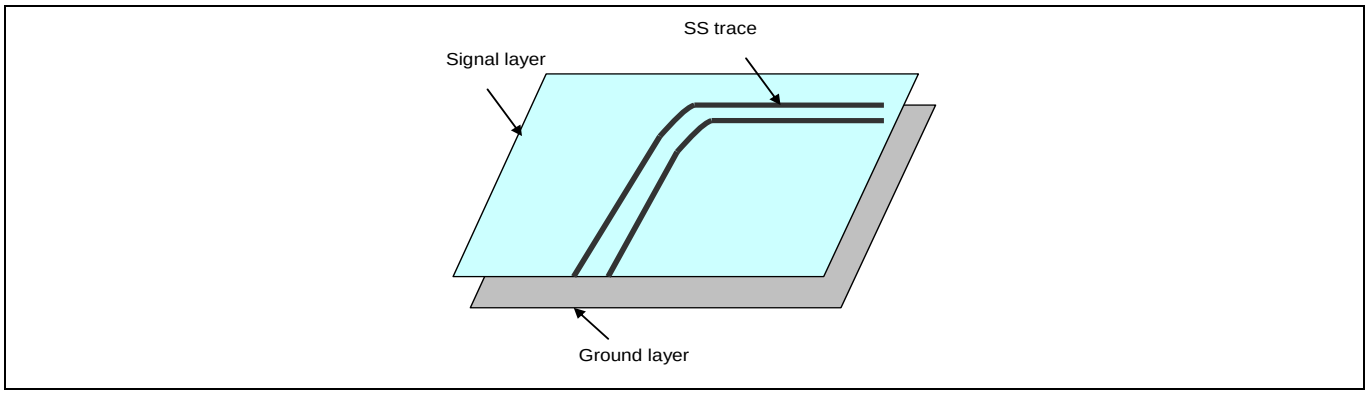

Figure 19 Solid ground plain under the SuperSpeed signal

- Whenever two pairs of USB traces cross each other in different layers, a ground layer should run all the way between the two USB signal layers. See **Figure 20**.

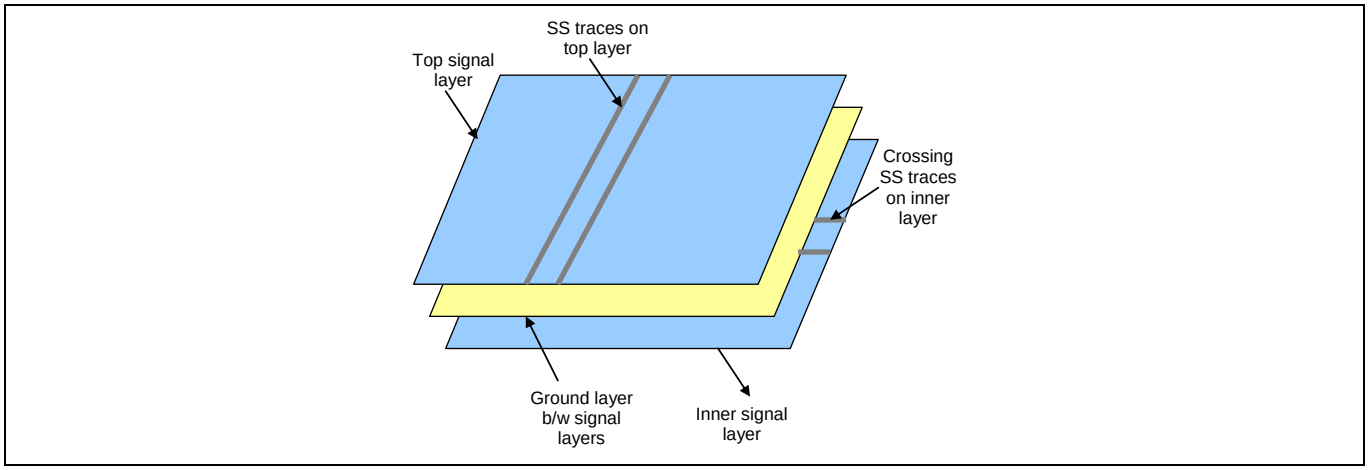

Figure 20 Ground insertion

- On the SuperSpeed/HS USB signal lines, use as few bends as possible. Do not use a 90-degree bends. Use 45-degree or rounded (curved) bends if necessary. See **Figure 21**.

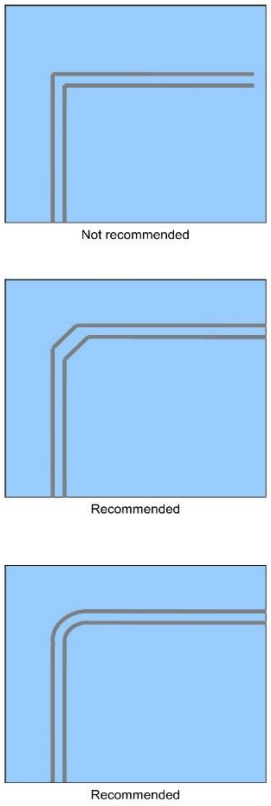

Figure 21 USB signal bends

- Differential SS pair trace lengths should be matched within 0.12 mm (5 mils). The HS D+ and D– signal trace lengths should be matched within 1.25 mm (20 mils). Always make adjustments (by putting loops as shown in **Figure 21**) for SuperSpeed USB/HS signal trace lengths near the USB receptacle and not near the device. The figure shows the matched and mismatched ends near the receptacle. Always adjust the length at the mismatched ends. An example for length matching for the SuperSpeed signal. See **Figure 22**.

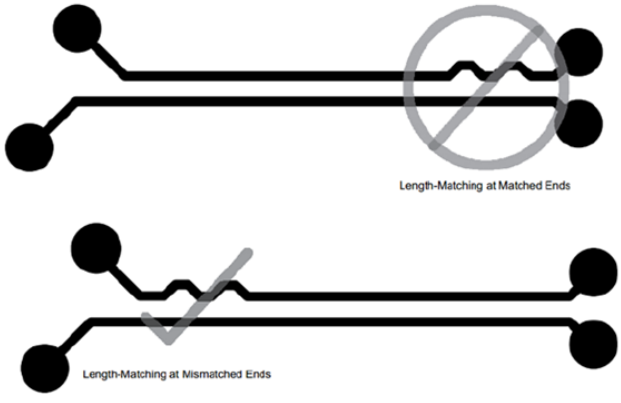

Figure 22 SuperSpeed/HS signal length matching

- There are different routing methods for length matching: single arc routing and serpentine routing methods. See **Figure 23** and **Figure 24** for single arc routing and serpentine routing respectively.

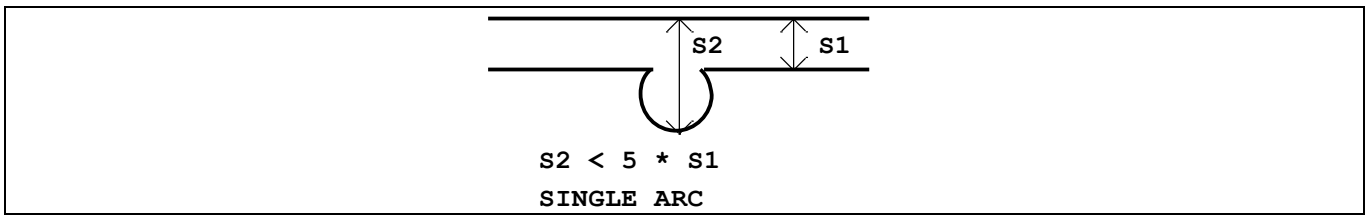

Figure 23 Single arc routing

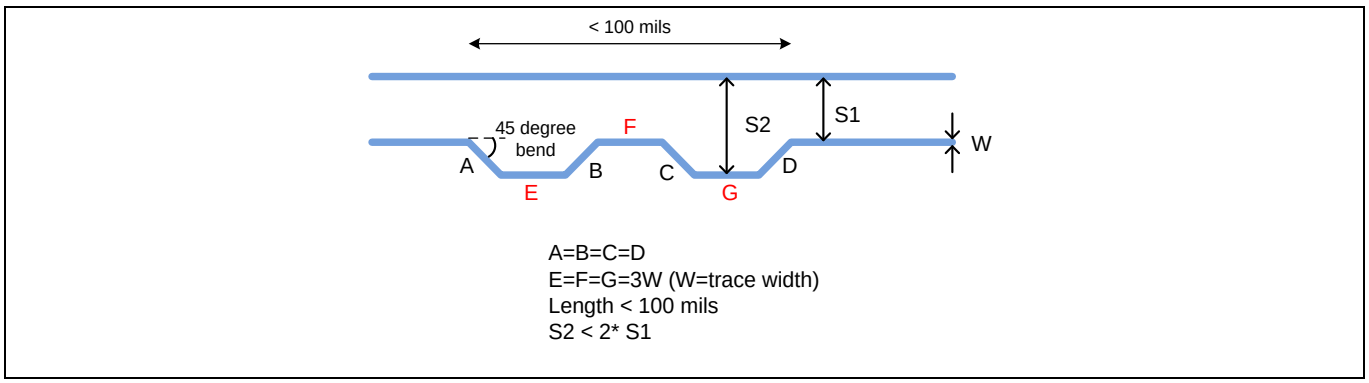

Figure 24 Serpentine routing

- The number of layers on the PCB should at least be four. To maintain a 90-Ω differential impedance, use a solid reference power plane.
- If signal routing has to be changed to another layer, continuous grounding has to be maintained to ensure uniform impedance throughout. To achieve this, ground vias should be placed next to signal vias. The distance between the signal and ground vias should be at least 40 mils. See **Figure 25**.

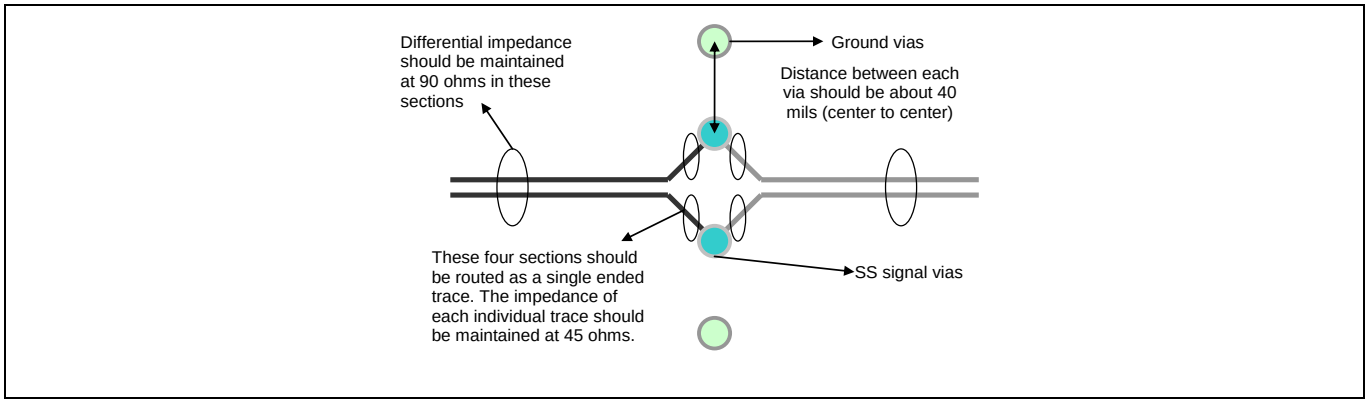

Figure 25 Ground vias

- Maintain constant trace width in differential pairs to avoid impedance mismatches:

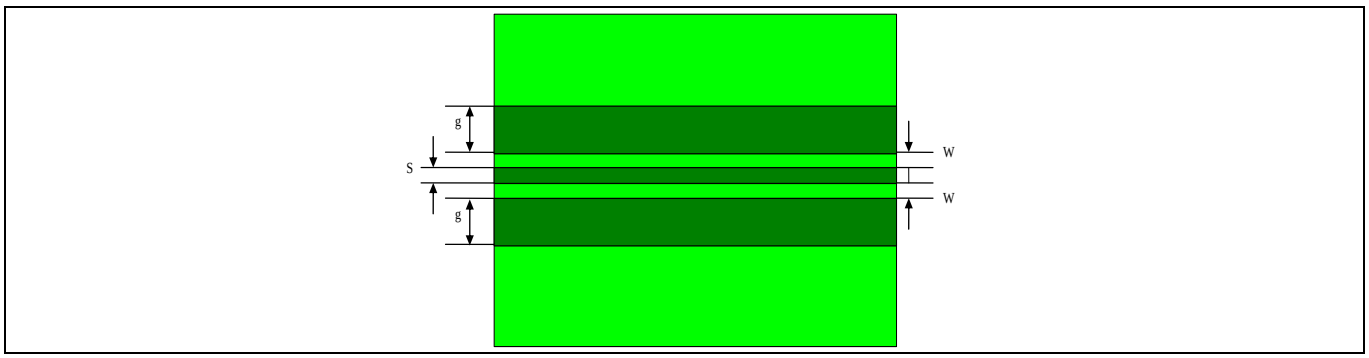

Figure 26 Differential pairs placements

Table 10 defines the recommended parameters mentioned in the **Figure 26**.

Table 10 USB traces specification

Dimension	Description	Value
S	Intra pair spacing	8 mils
W	Trace width	11 mils
G	Minimum gap b/w trace and other planes	8 mils

However, variation in the above values can be ignored if the lines have a characteristic impedance of 90 Ω.

- Avoid stubs on all USB lines. If pads are needed on the lines for probing purposes, they should not extend out of the trace in the form of a stub. See **Figure 27**.

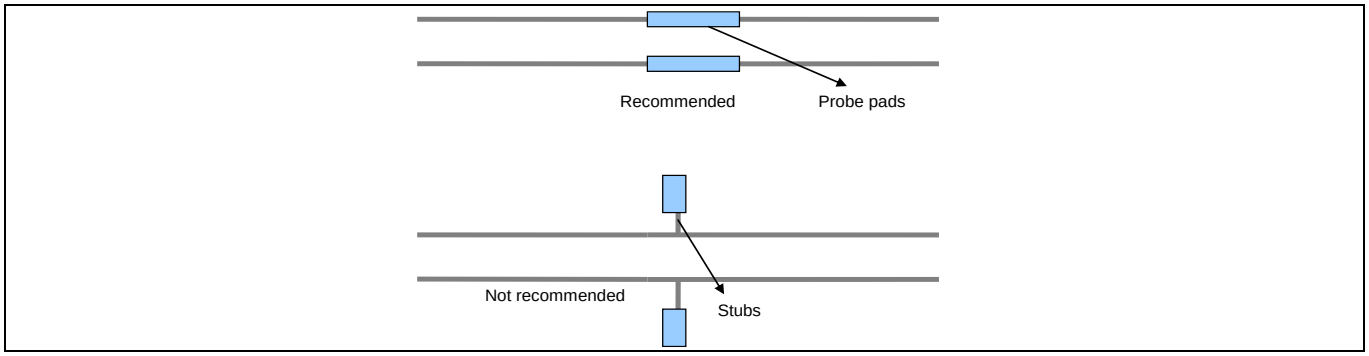

Figure 27 Probing pads placement

- Because the Micro-B receptacle is a surface mount receptacle, the USB signals can be routed entirely on the same layer as the EZ-USB™ FX3 device and the USB 3.0 Micro B receptacle. See **Figure 28** and **Figure 29** for the Micro-B receptable placement and Micro-B receptable layout respectively.

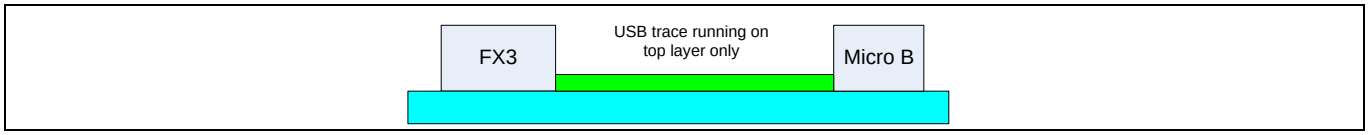

Figure 28 Micro-B receptacle placement

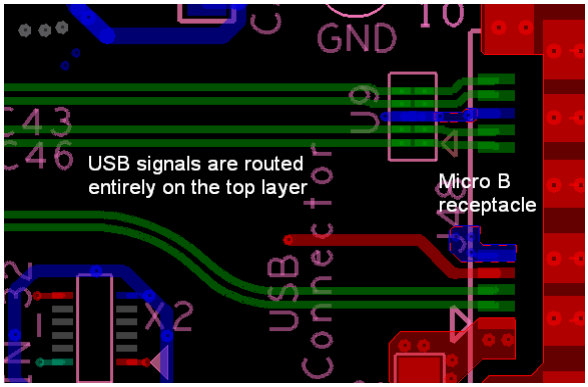

Figure 29 Micro-B receptacle layout

- It is highly recommended that, when using a standard B receptacle (through-hole receptacle), the USB signal lines are connected to the receptacle pins on the opposite layer of where the receptacle is placed as shown in **Figure 30** and **Figure 31**. For example, if the standard B receptacle is placed on the top layer, the signal lines should connect to the receptacle pins on the bottom layer. This prevents the unnecessary stubs due to the USB receptacle pins. A diagram of the recommended layout versus the stub producing layout is illustrated in detail in **Figure 32** and **Figure 33** respectively. To avoid introduction of vias, the EZ-USB™ FX3 device can be placed on the opposite layer of the standard B receptacle. In this case, the USB traces can be routed entirely on the same layer.

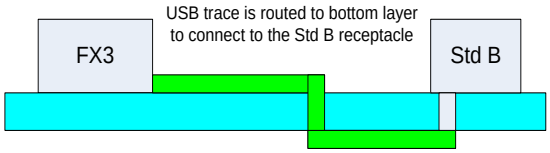

Figure 30 Standard-B receptacle placement

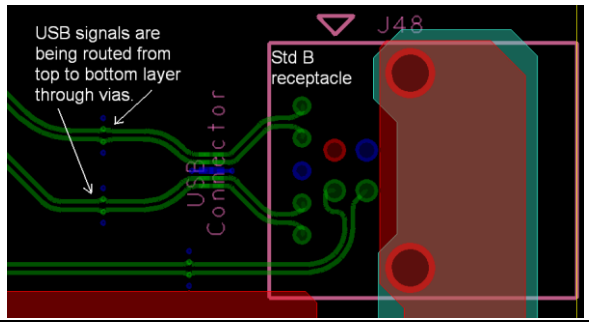

Figure 31 Standard-B receptacle layout

Both routing schemes mentioned earlier are tested to work at SS trace length of up to three inches.

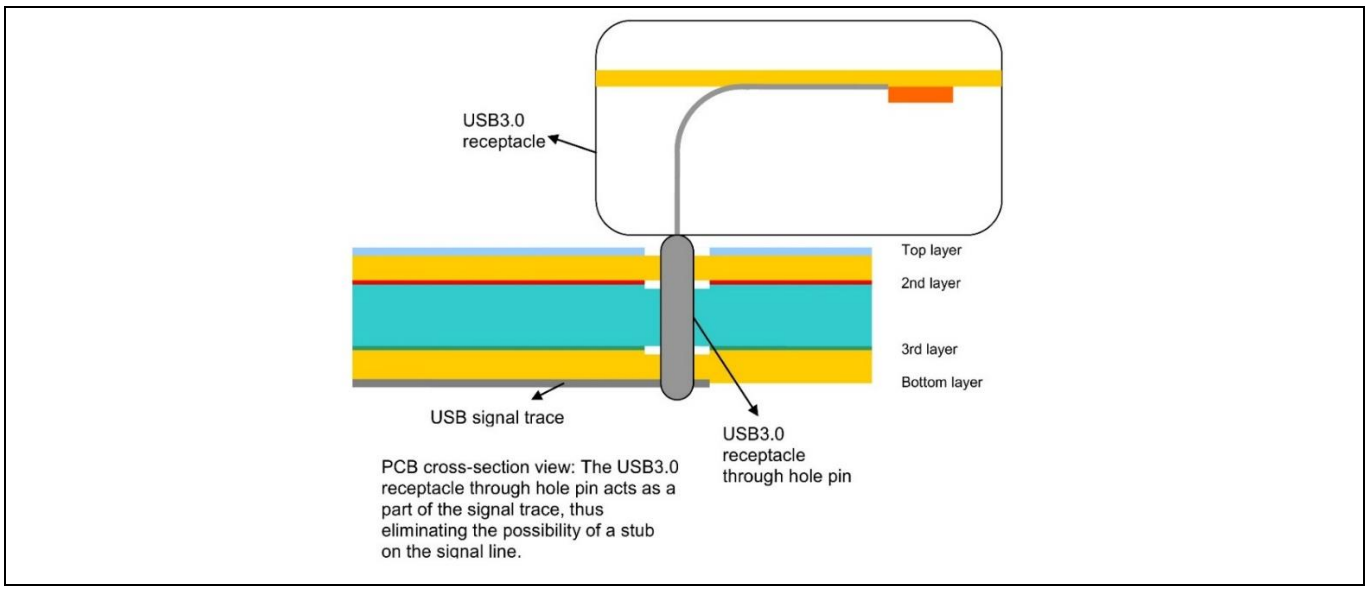

Figure 32 USB signals connected on the opposite side of the standard Type-B USB receptacle (recommended layout)

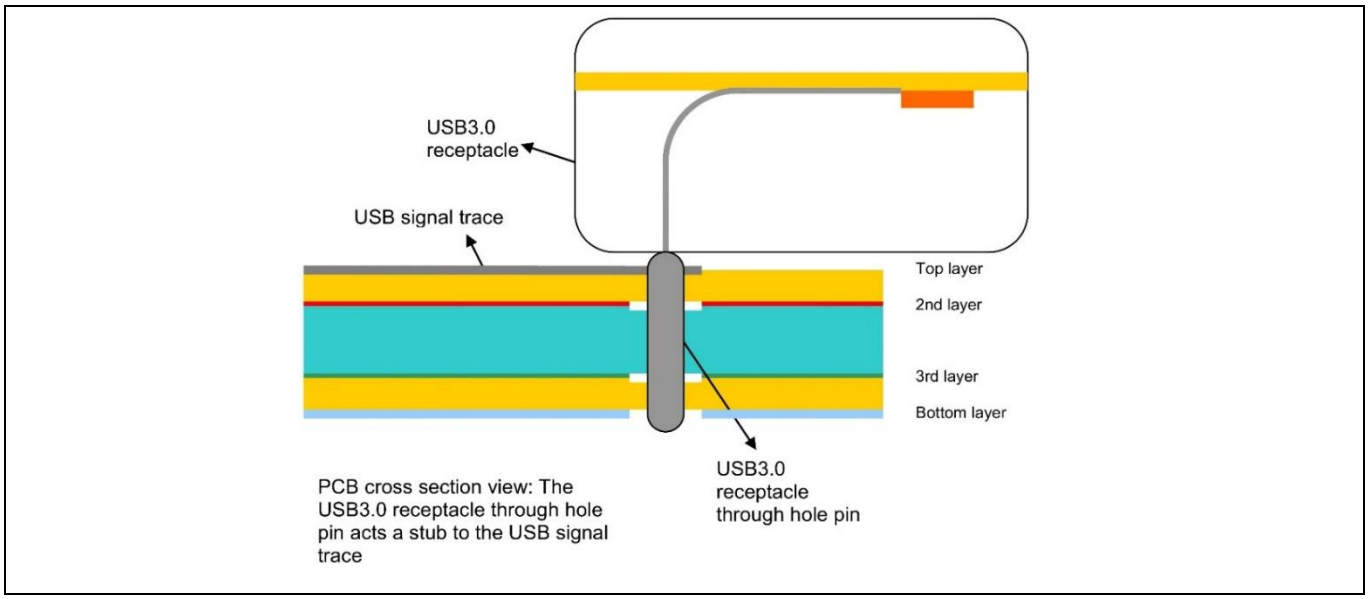

Figure 33 USB signals connected on the same side of the standard Type-B USB receptacle (not recommended)

- Void for vias on the SS signal lines should be common for the differential pair. Having a common void, as shown in **Figure 34**, maintains better impedance matching in comparison to separate vias.

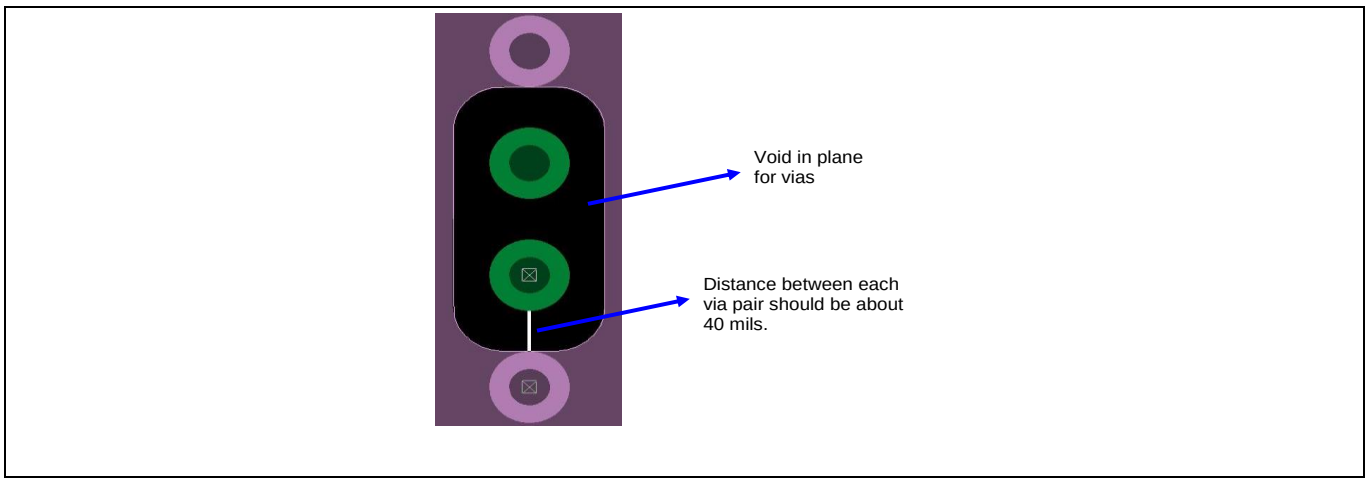

Figure 34 Void vias placement for SS traces

- Shield pins on the USB 3.0 receptacle should be terminated to ground with a parallel LC (or) RC circuit to avoid EMI/EMC issues. We recommend to use an RC circuit as shown in the **Figure 35**.

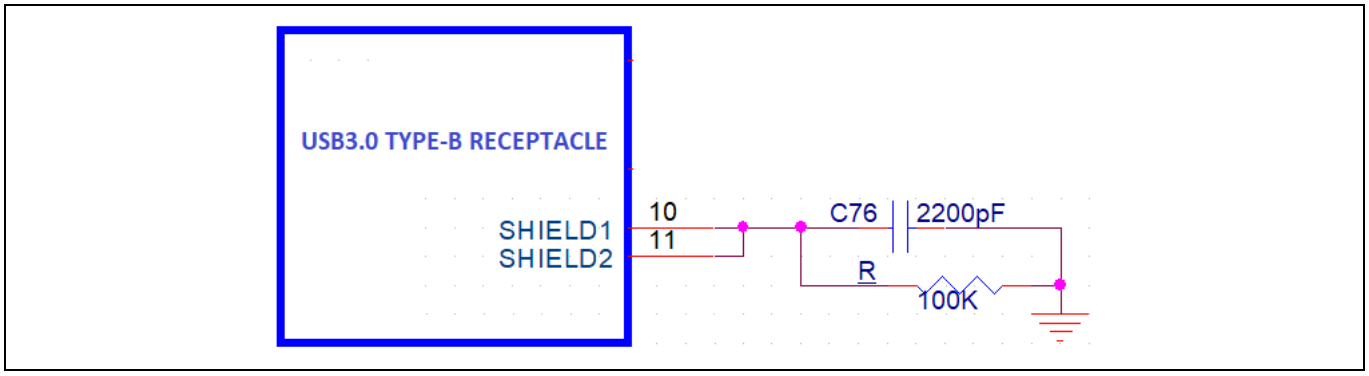

Figure 35 Standard-B receptacle layout

- To avoid cross talk, do not place the differential pairs close to other differential pairs, clock signals, or any other high-speed signals. We recommend to maintain 3x distance with other differential pair and other signals where ‘x’ is the width of the signal trace.

- **Figure 36** shows an example of routing the USB signals from the EZ-USB™ FX3 device to the USB 3.0 Micro B receptacle. Each differential pair should be kept uniform throughout the trace. Place AC coupling caps as close to the device as possible. ESD devices should be placed as close to the receptacle as possible.

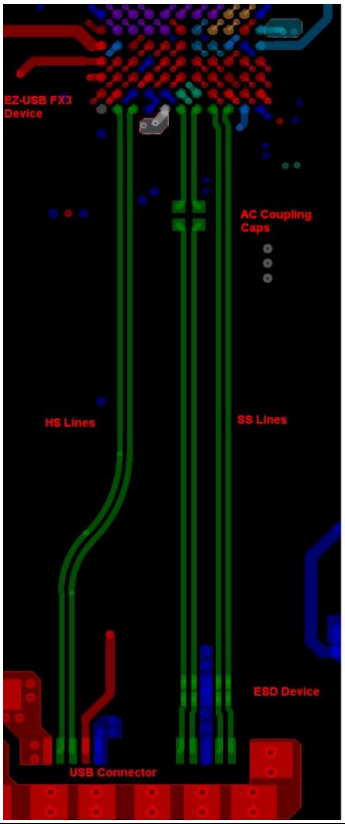

Figure 36 USB signals layout example

12.1.1 8-layer PCB example

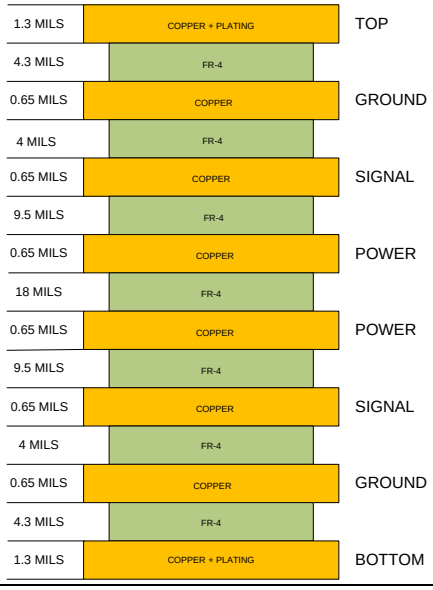

Figure 37 Stackup details for SuperSpeed explorer development kit

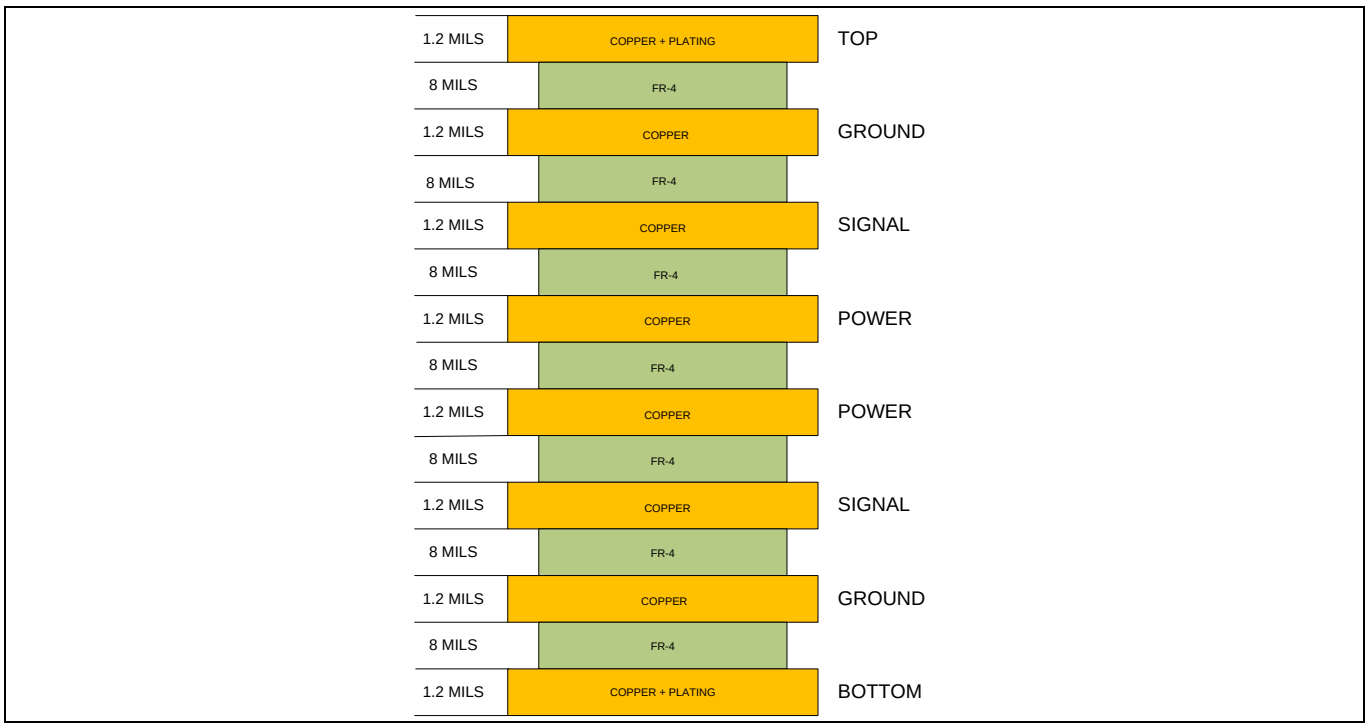

Figure 38 Stackup details for FX3 development kit

13 FX3S hardware design considerations

This section is specific only to EZ-USB™ FX3S. Consider the following guidelines in addition to the FX3 hardware design guidelines.

13.1 S-port interface

EZ-USB™ FX3S has two independent storage ports (S0-port and S1-port). Both storage ports support the following:

- MMC-system specification, MMCA technical committee, version 4.4
- SD specification Version, 3.0
- SDIO host controller compliant with SDIO specification version 2.00 (Jan 30, 2007)

To satisfy the requirements of these specifications, the following guidelines should be followed while designing the storage port circuitry on an EZ-USB™ FX3S system PCB.

- All data lines, command, and clock lines should be length-matched.
- The trace lengths should not be more than 5 inches. These numbers are calculated based on the worst-case timing parameters for SD cards, eMMC devices, and the EZ-USB™ FX3S device and should be taken only as a recommendation.
- In the case of SD card, V_{DD} should be tied to 3.3 V regardless of the I/O voltage used on the other SD lines, as illustrated in **Figure 39**.
- In case of an eMMC device, V_{CC} should be tied to 3.3 V and V_{CC} should be tied to the port I/O voltage supply (VIO2 or VIO3). **Figure 40** shows an eMMC device circuit.
- Add a 10-kΩ pull-up resistor to the SD data signals, except for SD_D3, which is used as one of the card insertion's detect mechanism. A 470 kΩ resistor is used to pull down SD_DQ3. SD_CLK is pulled up using only a 1-kΩ resistor.
- It is recommended to have 22E series termination on all the Data lines, CMD and CLK lines to reduce the reflection on these lines. If the CLK line voltage is less than recommended VIOx domain as per the **Table 2**, then 22E should be replaced by 0E resistor.
- SD card voltage supply (VIO2 or VIO3) should be changed to 1.8 V dynamically when UHS-I memory card is used.
- Card insertion and removal detection is provided using the following mechanisms:
  - SD-D3 data line: SD cards have an internal 10-kΩ pull-up resistor. When you insert or remove the card from the SD/MMC connector, the voltage level at the SD_D3 pin changes and triggers an interrupt to the CPU. Note that older generations of MMC cards do not support this card detection mechanism.
  - S0/S1_INS pin: Some SD/MMC connectors facilitate a micro switch for card insertion and removal detection. This micro switch can be connected to S0/S1_INS. When you insert or remove the card from the SD/MMC connector, it turns the micro switch on and off. This changes the voltage level at the pin that triggers the interrupt to the CPU. Note that this S0/S1_INS pin is shared between the two S-Ports. The register configuration determines which port gets to use this pin. This pin is mapped to the VIO3 power domain; if VIO2 and VIO3 are at different voltage levels, this pin cannot be used as S1_INS. The insertion/removal detection mechanism is not used for eMMC devices because the devices are usually soldered on the board and do not involve insertion/removal detection.

Figure 39 and **Figure 40** show different implementation of the SD/MMC cards and eMMC devices.

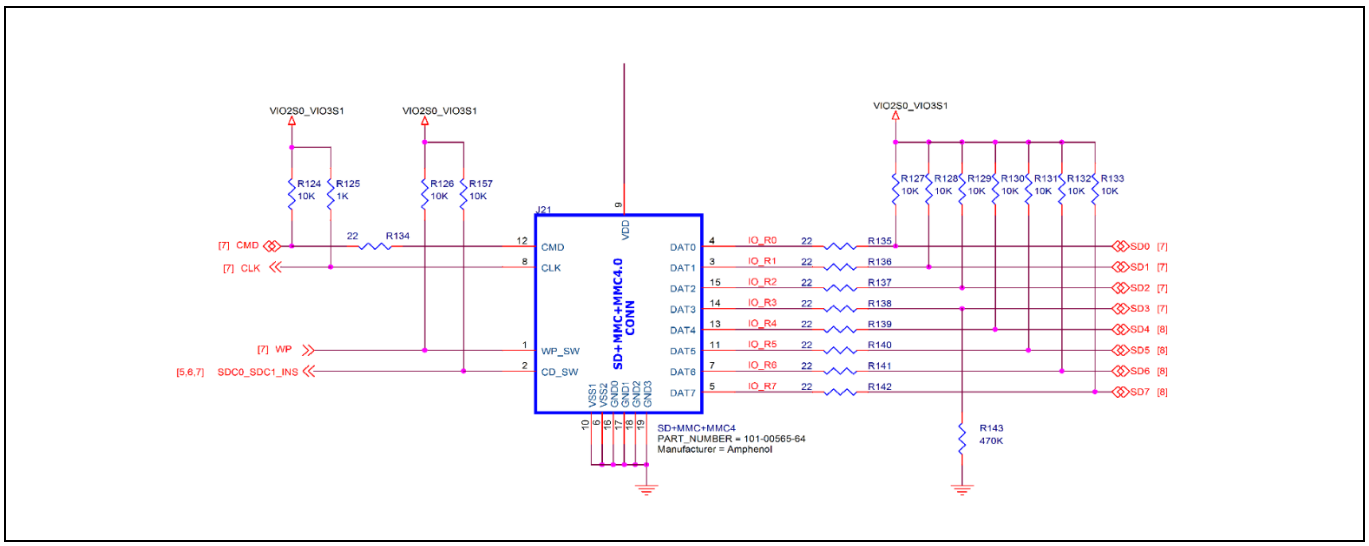

Figure 39 SD/MMC card circuit

Note:

1. *VIO2S0_VIO3S1 – VIO2S0 or VIO3S1*
2. *This voltage supply can be either VIO2 or VIO3 based on the place where you connect the storage daughter card. It will be VIO2 if you are connecting the storage daughter card to the S0 port and VIO3 if you are connecting the storage daughter card to the S1 port.*
3. *When the SD card is connected to the S1 port, then some of the serial interfaces are not available. See the pin description section in the FX3S **datasheet** for details.*

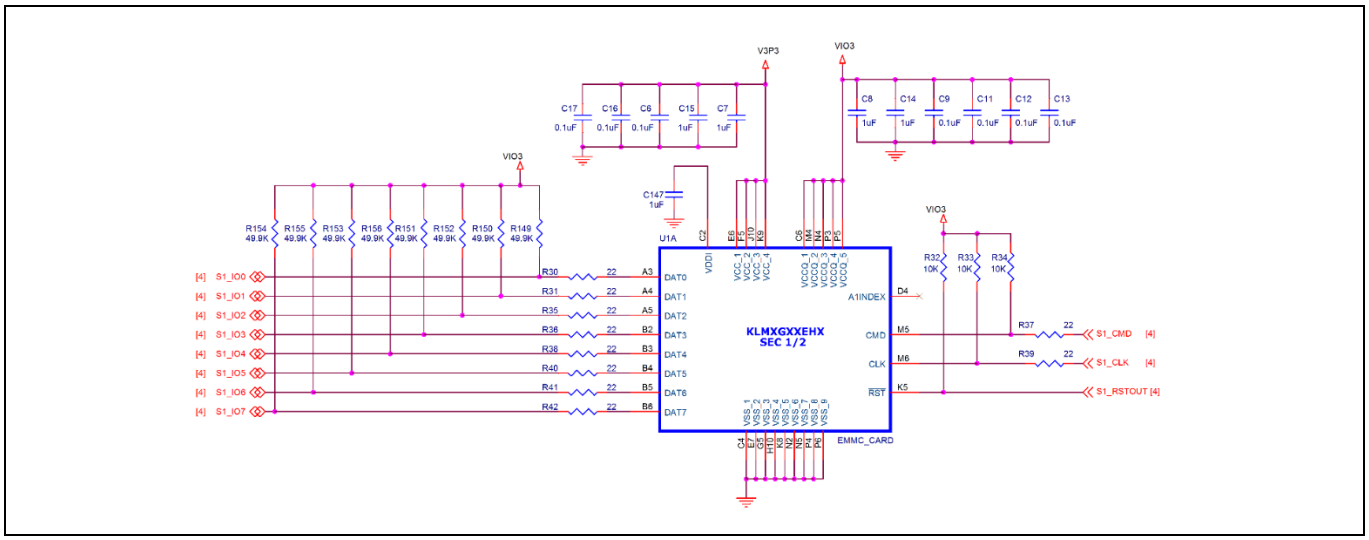

Figure 40 eMMC device

14 Schematics and layout review checklist

Table 11 is a checklist for all the important guidelines. Provide an answer to each checklist item to find out the extent to which your hardware design meets these guidelines. A design which satisfies all the schematic & Layout checklist will work definitely without any system level hardware issues.

Table 11 Schematics checklist

Sl. No	Schematic checklist	Answer (Yes/No/NA)
1	Are the decoupling capacitors and bulk capacitors connected according to Table 3?	
2	Does the crystal meet the specification in this application note according to Table 4 ?	
3	Are the ferrite beads connected on AVDD, U3TXVDD, U3RXVDD, and CVDD?	
4	Do the power-on-reset RC components meet the minimum reset time (1 ms)?	
5	Do the USB precision resistors have 1% tolerance?	
6	Are the I^2C lines provided with pull-up resistors to the VIO5 domain?	
7	Does the USB port shield terminate with RC circuit ?	
8	Do the SuperSpeed USB lines have ESD device connected?	
9	Do the GPIF lines have 22-Ω series resistor connected?	
10	Are the PMODE lines connected per Table 9?	
11	Does the SPI flash meet the specification in this application note according to Section 8.4 and Section 8.5 ?	
12	Did you make sure that the JTAG lines don't have pull up resistors?	
13	Does the VBUS pin of FX3 device has overvoltage protection?	
14	Does the VBUS pin of FX3 has 1uF capacitor?	
15	Does the TX pins of FX3 has AC (0.1uF) capacitor?	

Sl. No	Layout checklist	Answer (Yes/No/NA)
1	Is the crystal placed close to the chip (less than 2 cm)?	
2	Are the decoupling capacitors and bulk capacitors placed close to the FX3 power pins?	
3	Are the clock traces routed away from the high-speed data lines and the power lines?	
4	Are the power traces routed away from the high-speed data lines and the clock lines?	
5	Is the capacitor in the RC reset circuitry placed close to the reset pin of FX3?	
6	Are the USB SS and HS signal lines having 90 Ω differential impedance?	
7	Are the USB SS and HS signal lines matched in length?	

Schematics and layout review checklist

Sl. No	Layout checklist	Answer (Yes/No/NA)
8	Are the USB data lines provided with solid ground plane underneath?	
9	Are the SS traces provided with the guard traces along the USB data trace with stitching vias?	
10	Are the SS traces provided with the AC decoupling capacitors (0.1 µF) on the TX lines?	
11	Is the AC caps (0.1uF) on TX lines having the cut-out on immediate layer and reference GND split plane on immediate third layer?	
12	Are the AC caps (0.1uF) placed according to information provided below the **Figure 15** ?	
13	Are the USB traces kept less than 3 inches?	
14	Is it ensured that there are no stubs on all the USB traces?	
15	Is it ensured that there are no vias on the SS traces?	
16	Do the USB traces have few bends and no 90-degree bends?	
17	Do the two planes underneath the AC coupling capacitors have cut in shape of the capacitor?	
18	Is it ensured that SS and HS USB traces are routed with consistent trace spacing?	

15 Summary

The recommended practices for EZ-USB™ FX3/FX3S/SX3 hardware design and the critical items that a developer must consider have been discussed in this document.

16 Appendix A – PCB layout tips

There are many classic techniques for designing PCBs for low noise and EMC. Some of these techniques include:

- **Multiple layers:** Although they are more expensive, it is best to use a multi-layer PCB with separate layers dedicated to the V_{SS} and V_{DD} supplies. This gives good decoupling and shielding effects. Separate fills on these layers should be provided for V_{SSA}, V_{SSD}, V_{DDA}, and V_{DDD}.
- To reduce cost, a 2-layer or even a single-layer PCB can be used. In that case, you must have a good layout for all V_{SS} and V_{DD}.
- **Component position:** You should separate the different circuits on the PCB according to their electromagnetic interference (EMI) contribution. This will help reduce cross-coupling on the PCB. For example, you should separate noisy high-current circuits, low-voltage circuits, and digital components.
- **Ground and power supply:** There should be a single point for gathering all ground returns. Avoid ground loops, or minimize their surface area. All component-free surfaces of the PCB should be filled with additional grounding to create a shield, especially when using 2-layer or single-layer PCBs.
- The power supply should be close to the ground line to minimize the area of the supply loop. The supply loop can act as an antenna and can be a major emitter or receiver of EMI.
- **Decoupling:** The standard decoupler for external power is a 100-µF capacitor. Supplementary 0.1-µF capacitors should be placed as close as possible to the V_{SS} and V_{DD} pins of the device, to reduce high-frequency power supply ripple.

Generally, you should decouple all sensitive or noisy signals to improve electromagnetic compatibility (EMC) performance. Decoupling can be both capacitive and inductive.

- **Signal routing:** When designing an application, the following areas should be closely studied to improve EMC performance:
  - Noisy signals, for example signals with fast edge times
  - Sensitive and high-impedance signals
  - Signals that capture events, such as interrupts and strobe signals

To increase EMC performance, keep the trace lengths as short as possible and isolate the traces with V_{SS} traces. To avoid crosstalk, do not route them near to or parallel to other noisy and sensitive traces.

17 Appendix B – Troubleshooting

17.1 FX3/FX3S/SX3 device not enumerating

There are many factors which contributes to the FX3 enumeration issue. Some of these points include:

- **PMODE pins:** Many boot modes are supported by FX3/FX3S/SX3. Hence PMODE pins should be properly configured according to the application.
- **FSLC pins:** FSLC pins must be properly configured according to the source of the clock input (crystal or external clock).
- **USB3.0 Type-B receptacle to FX3/SX3 device connections:** TX pins of the FX3/SX3 device should be connected to TX pins of the USB3.0 Type-B receptacle. Rx pins of the FX3/SX3 device should be connected to RX pin of the USB receptacle. Use a USB3.0 cable which connects the host TX to FX3/SX3 device RX pins and host RX to FX3 device TX pins.

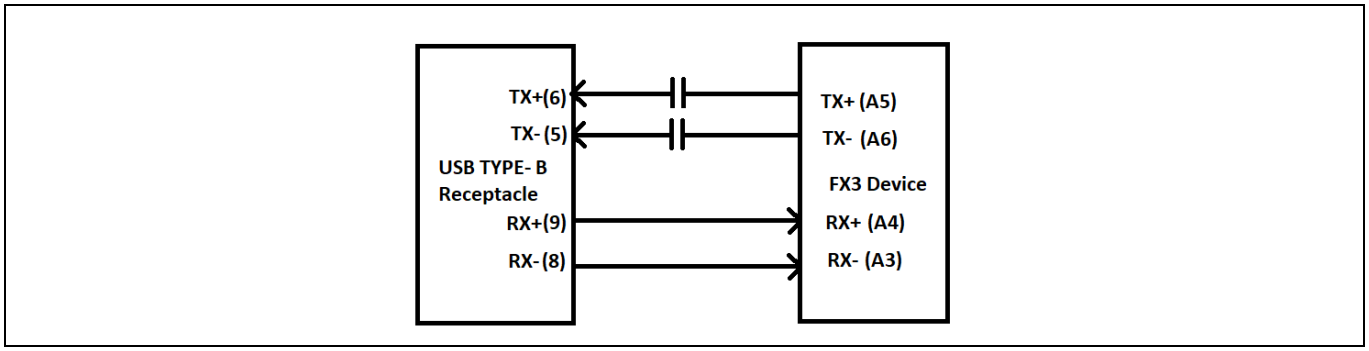

Figure 41 USB3.0 Type-B receptacle to FX3/SX3 device connections

- **Hub/embedded controller to FX3/SX3 device connections:** Some applications require the FX3/SX3 device to be connected to downstream ports of the hub (or) embedded controller in the same PCB. In these cases, FX3/SX3 device TX pins should be connected to RX pins of the downstream ports (or) Rx pins of the embedded controller. FX3/SX3 device RX pins should be connected to the TX pins of the downstream ports (or) Rx pins of the embedded controller.

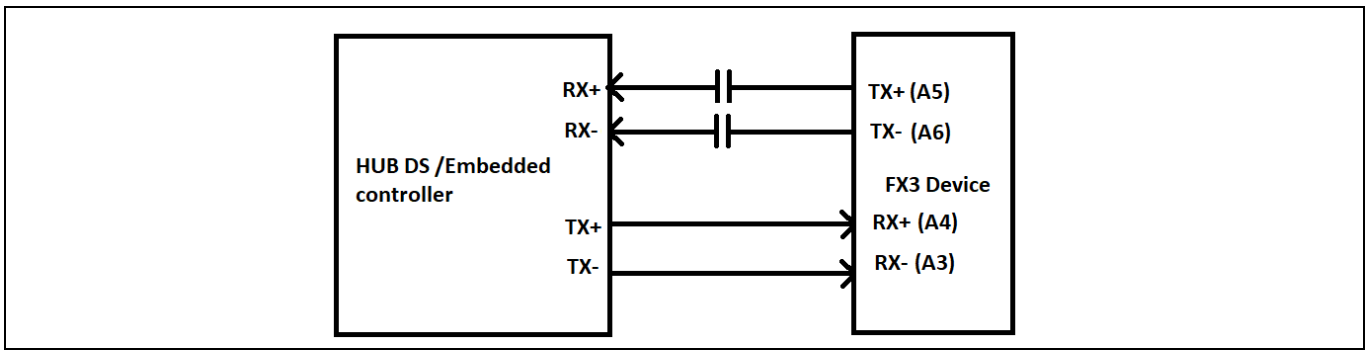

Figure 42 Hub/embedded controller to FX3/SX3 device connections

- **Power domain isolation:** Make sure that AVDD, CVDD, U3TXVDDQ, and U3RXVDDQ are isolated and connected with ferrite beads. Also, the source of these supplies should have noise/ ripple less than 70mV.

- **USB reference resistor:** Make sure that the USB3 reference pin (B3) is connected to a resistor (200E) with +/-1% tolerance. Make sure that the USB2 reference pin (C8) is connected to a resistor (6.04k) with +/-1% tolerance.
- **TX A/C capacitor:** A/C capacitor should be connected on TX lines of the FX3/SX3 device. This will prevent the common-mode noise from the cable/host entering FX3/SX3 device TX lines. The AC capacitor should be near to the type-B receptacle for the application which uses the type-B receptacle; the AC capacitor should be near to the FX3S/SX3 TX pins for the application which uses the hub/embedded controller.
- **USB3.0/USB2.0 layout guidelines:** Make sure that the high-speed layout guidelines are followed per Section **12.1**. High-speed signals should be differential with a solid ground plane underneath.

18 Appendix C – FX3/SX3 device connections to USB 2.0-only host

- FX3/SX3 SuperSpeed pins TX+/- pins (A5 and A6) and RX+/- pins (A3 and A4) can be left open.
- Both USB3.0 power pins (U3TXVDDQ and U3RXVDDQ) should be connected to 1.2V with a ferrite bead.
- The USB3 reference pin (B3) can be left open.
- Make sure that layout guidelines are followed per Section **12.1**.

19 Appendix D – FX3/SX3 device connections to USB 3.0-only host

- USB 3.0 consists of both SuperSpeed lines (SS_TX_P, SS_TX_M, SS_RX_P, and SS_RX_M) and High-Speed lines (DM and DP). Some designs may use the FX3 device in USB 3.0 mode alone; that is, only SuperSpeed lines are used by the FX3 and High-Speed lines are used by another controller. For example, Infineon USB 3.0 hub controllers, CYUSB3328 and CYUSB3326, have a “shared link” feature, which enables the USB 3.0 port to be split into an embedded SuperSpeed port and a standard USB 2.0 port. To connect the FX3 to the embedded USB 3.0 port, it should be programmed such that it operates only in USB 3.0 and does not fall back to USB 2.0. There can be other applications besides shared link where this may be useful. See **KBA219491** for USB 3.0-only application.
- FX3/SX3 High-Speed pins DP/DM pins (A9 and A10) can be left open (or) it can be connected to other embedded controllers.
- Both USB3.0 power pins (U3TXVDDQ and U3RXVDDQ) should be connected to 1.2V with a ferrite bead.
- The USB2 reference pin (C8) can be left open.
- Make sure that the layout guidelines are followed per Section **12.1**.

20 Appendix E – FX3/SX3/CX3 device with type-C applications

- See **KBA218640** for the following type-C based applications:
- FX3/SX3/CX3 with type-C plug implementation
- FX3/SX3/CX3 with type-C receptacle implementation
- FX3/SX3/CX3 with type-C receptacle with PD controller implementation

References

For more information, several references are available:

- The Circuit Designer's Companion, Second Edition, (EDN Series for Design Engineers) by Tim Williams
- PCB Design for Real-World EMI Control (The Springer International Series in Engineering and Computer Science), by Bruce R. Archambeault and James Drewniak
- Printed Circuits Handbook (McGraw Hill Handbooks), by Clyde Coombs
- EMC and the Printed Circuit Board: Design, Theory, and Layout Made Simple, by Mark I. Montrose
- Signal Integrity Issues and Printed Circuit Board Design, by Douglas Brooks

Revision history

Revision	Date of release	Description of changes
**	2011-07-14	New application note.
*A	2011-09-23	Updated trace adjustment diagram. Updated via void diagram. Updated AC coupling capacitors diagram.
*B	2011-01-11	Added ‘Schematic design checklist’ before the recommendations Added GPIF II Interface section Updated decoupling capacitor recommendation table Changed heading of the package detail section to ‘FX3 Package Dimensions’ Updated USB signal routing schemes using standard and micro B receptacles
*C	2012-09-18	Replaced the “F” symbol in the Booting section with High-Z Added Crystal and Clock specification and added a list of compatible crystals Added Inrush Consideration and Power Supply Design section Added decoupling cap placement sample Added values for termination resistors Added ESD part number and placement example Updated the loading capacitance requirements for the external USB 3.0 ESD Added Links to schematic and IBIS model Added the location of USB3.0 Polarity Inversion section in the USB 3.0 Spec Added GPIF example Application Notes numbers Added I2C, SPI /UART, I2S Consideration Added Images and tables numbers Added table of Content section Changed the VBUS min to 4.0 V Changed to standby mode support for the 32.768 kHz clock input Added Appendix A
*D	2012-10-03	Updated Figure 21 Title
*E	2012-11-28	Updated cap value column in Table 2 Updated VBUS/VBATT description
*F	2013-01-28	Modified to cover details of FX3S Changed title to include FX3S Added Table 1 Figure 12 is modified Added FX3S hardware design considerations section

Revision history

Revision	Date of release	Description of changes
*G	2014-04-11	Figure 1 is modified to show the decoupling capacitors connected to each pin Table 3 is modified Crystal section is modified Section for selecting SPI flash for FX3 boot is added Figure 33 is added to show the stackup details of FX3 DVK Schematics and Layout Review Checklist is added
*H	2014-08-26	Updated the value of bulk capacitors connected to U3TXVDDQ and U3RXVDDQ to 22 µF Added schematic guidelines for the OTG_ID pin.
*I	2015-01-23	Removed minimum trace length requirement for SD lines in **S-port interface**. Changed VIO pin name to H11 in **Figure 1**. Added recommended part for Crystal oscillator in **Crystal effective load capacitor calculation**. Updated the length matching requirement for GPIF II lines in **GPIF II interface**.
*J	2015-02-17	Updated **Table 3**. Added a hyperlink to refer the list of USB SuperSpeed Code Examples, in the Abstract (page 1).
*K	2015-07-23	Added **Related resources**. Added **Summary**. Updated to new template. Completing Sunset Review.
*L	2015-10-05	Updated **Figure 1** in **Overview**. Updated description in **GPIF II interface**. Updated description in **Selection of SPI flash** under **Low-performance peripherals (LPP)**. Updated description in **EMI and ESD considerations**. Updated **Figure 35** and **Figure 36** in **S-port interface** under **FX3S hardware design considerations**.
*M	2017-04-20	Updated logo and copyright
*N	2018-08-22	Updated flash size in Section **8.5**. Updated **Figure 1**. Updated the Epson FA-20H link in **Table 5**.
*O	2019-10-04	Added MISO pin pull-down recommendation
*P	2021-09-27	Updated with SX3 & CX3 reference. Updated Obsolete Part Numbers in Table 5. Added MISO line (2K) pull down value in Section 8.4. Added Hybrid SPI Flash Usage Updated Layout guidelines with AC/ ESD Capacitor Cut-out Updated Schematic & Layout checklist

Revision history

Revision	Date of release	Description of changes
		Updated package information with Solder mask opening and Solder paste details Added Appendix B, C & D Migrated to Infineon template
*Q	2021-10-26	Updated the document number as AN70707 in page 1

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2021-10-26

Published by

Infineon Technologies AG

81726 München, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference

001-70707 Rev.*Q

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie") .

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (**www.infineon.com**).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.