EZ-PD™ PMG1 MCU hardware design guidelines and checklist

About this document

Scope and purpose

This application note provides the hardware design and PCB layout guidelines for EZ-PD™ Power Delivery Microcontroller Gen1 (PMG1) family of high-voltage USB-C power delivery (PD) microcontrollers. This application note provides detailed hardware design aspects of EZ-PD™ PMG1 MCU-based system design. The document uses EZ-PD™ PMG1 MCU family prototyping kits as the design reference. This application note includes a schematics and layout review checklist, which consolidates the important points to be considered while designing with EZ-PD™ PMG1 MCU.

Intended audience

This application note is intended to familiarize engineers with the hardware design guidelines for EZ-PD™ PMG1 MCU-based designs.

Associated part family

CYPM1011, CYPM1111, CYPM1211, and CYPM1311/22

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1 Introduction

EZ-PD™ PMG1 MCU is a family of high-voltage USB PD MCUs with Arm® Cortex®-M0/Cortex-M0+ CPU. The EZ-PD™ PMG1 MCU family includes different MCUs with integrated USB PD controller, analog, and digital peripherals. You can choose the controller based on the design requirement. EZ-PD™ PMG1 MCU is targeted at embedded systems that provide or consume power to or from a high-voltage USB-C PD port and leverage the MCU to provide additional control capability.

2 Device selection

This section describes the basic features of the EZ-PD™ PMG1 MCU family. **Table 1** compares the basic features of various MCUs in the EZ-PD™ PMG1 MCU family.

Table 1 Comparison of features of different MCUs of EZ-PD™PMG1 MCU family

Subsystem or range	Item	EZ-PD™ PMG1-S0 MCU	EZ-PD™ PMG1-S1 MCU	EZ-PD™ PMG1-S2 MCU	EZ-PD™ PMG1-S3 MCU
CPU and Memory Sub-system	Core	Arm® Cortex®-M0	Arm® Cortex®-M0	Arm® Cortex®-M0	Arm® Cortex®-M0+
	Max freq (MHz)	48	48	48	48
	Flash (KB)	64	128	128	256
	SRAM (KB)	8	12	8	32
Power Delivery	Power Delivery ports	1	1	1	1 port for 48-QFN 2 port for 97-BGA
	Role	Sink	DRP	DRP	DRP
	MOSFET gate drivers	1x PFET	2x PFET	2x PFET/NFET	Flexible 2x NFET
	Fault protections	VBUS OVP[1] and UVP[2]	VBUS OVP, UVP, and OCP[3]	VBUS OVP, UVP and OCP	VBUS OVP, UVP, and OCP
USB	Integrated Full Speed USB 2.0 device with Billboard Class support	No	No	Yes	Yes
Voltage range	Supply (V)	VDDD (2.7 -5.5) VBUS (4 - 21.5)	VSYS (2.75 - 5.5) VBUS (4 - 21.5)	VSYS (2.7 - 5.5) VBUS (4 - 21.5)	VSYS (2.5 - 5.5) VBUS (4 - 28)
	IO (V)	1.71 - 5.5	1.71 - 5.5	1.71 - 5.5	1.71 - 5.5
Digital	Serial communication block (configurable as I2C/UART/SPI)	2	4	4	7 for 48-QFN (out of which only 5 can be configured as SPI and UART) and 8 for 97- BGA
	TCPWM block	4	2	4	7 for 48-QFN 8 for 97-BGA

[1] OVP stands for overvoltage protection

[2] UVP stands for undervoltage protection

[3] OCP stands for overcurrent protection

Device selection

Subsystem or range	Item	EZ-PD™ PMG1-S0 MCU	EZ-PD™ PMG1-S1 MCU	EZ-PD™ PMG1-S2 MCU	EZ-PD™ PMG1-S3 MCU
	Hardware Authentication Block (Crypto)	No	No	Yes	Yes
Analog	ADC	2x 8-bit SAR	1x 8-bit SAR	2x 8-bit SAR	2x 8-bit SAR 1x 12-bit SAR
	On-chip Temperature Sensor	Yes	Yes	Yes	Yes
GPIO	Max # of I/O	12(10+2 OVT[4])	17(15+2 OVT)	20(18+2 OVT)	26 (24+2 OVT) for 48-QFN 50 (48+2 OVT) for 97-BGA
Charging Standards	Charging Source	-	BC 1.2, AC	BC 1.2, AC	BC 1.2, AC, AFC and Quick Charge 3.0
	Charging Sink	BC 1.2, Apple Charging (AC)	BC 1.2, AC	BC 1.2, AC	BC 1.2, AC
ESD Protection	See **ESD and EMI/EMC protection** for details on in-built ESD thresholds				
Packages	Package Options	24 QFN (4x4mm, 0.5mm pitch)	40 QFN (6×6mm, 0.5mm pitch)	40 QFN (6×6mm, 0.5mm pitch)	48-QFN (6 x 6 mm, 0.5 mm pitch) 97BGA (6 x 6 mm, 0.5 mm and 0.65 mm pitch)

2.1 Ordering information

Table 2 Ordering information

MCU	MPN	Type-C port	Termination resistor	Package type	Si ID
PMG1-S0	CYPM1011-24LQXI CYPM1011-24LQXIT	1	R_D, $R_{D\text{-}DB}$	24-Pin QFN	0x2020
PMG1-S1	CYPM1111-40LQXI CYPM1111-40LQXIT	1	R_P, R_D, $R_{D\text{-}DB}$	40-Pin QFN	0x2A20
PMG1-S2	CYPM1211-40LQXI CYPM1211-40LQXIT	1	R_P, R_D, $R_{D\text{-}DB}$	40-Pin QFN	0x1D20
PMG1-S3	CYPM1311-48LQXI CYPM1311-48LQXIT	1	R_P, R_D, $R_{D\text{-}DB}$	48-Pin QFN	0x3501

[4] OVT stands for Over-Voltage Tolerant

Device selection

MCU	MPN	Type-C port	Termination resistor	Package type	Si ID
	CYPM1322-97BZXI CYPM1322-97BZXIT	2	R_P, R_D	96-Pin BGA	0x3500

3 System architecture

3.1 USB PD sink-only applications

The USB PD sink systems or applications are powered directly through the USB PD port on the design and requires no separate power input. In the USB PD Sink role, the EZ-PD™ PMG1 S0/S1/S2 MCUs are capable of handling a PD contract of up to 20 V, 5 A (100 W) and S3 MCU is capable of handling a PD contract of up to 28 V, 5 A (140 W).

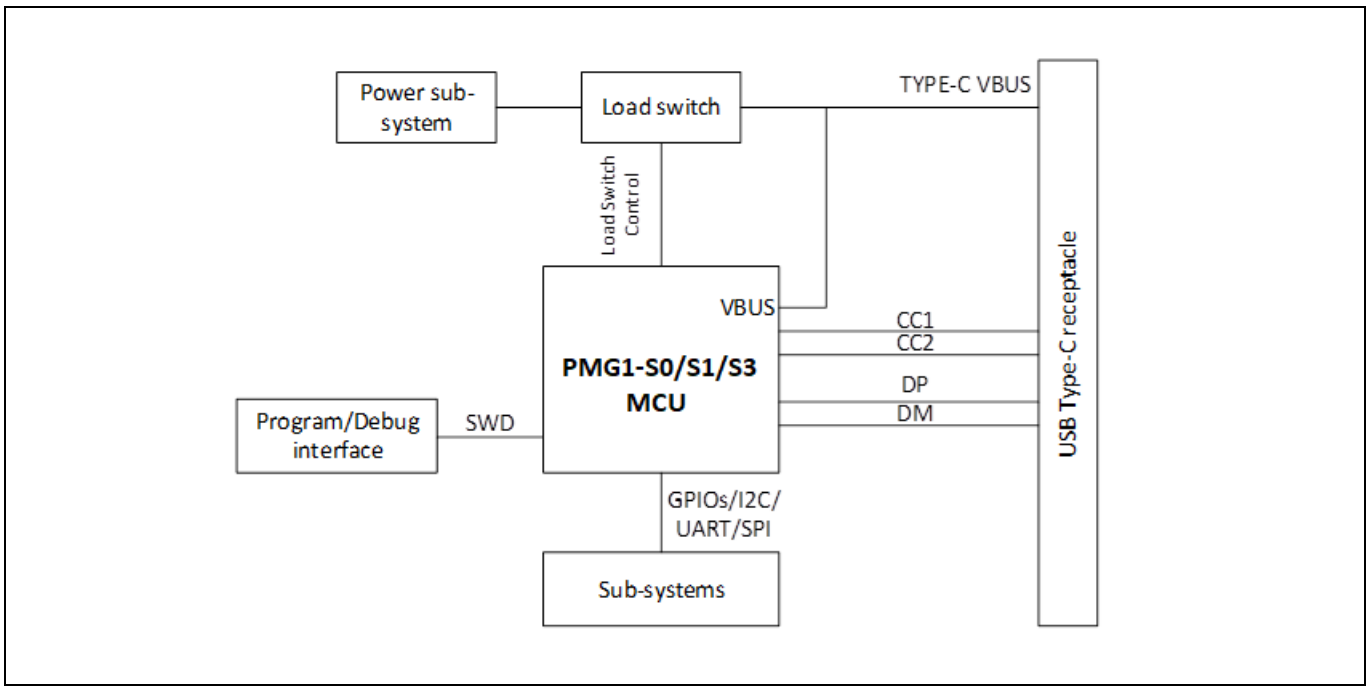

Figure 1 USB PD sink-only application using EZ-PD™ PMG1-S0/PMG1-S1/PMG1-S3 MCUs

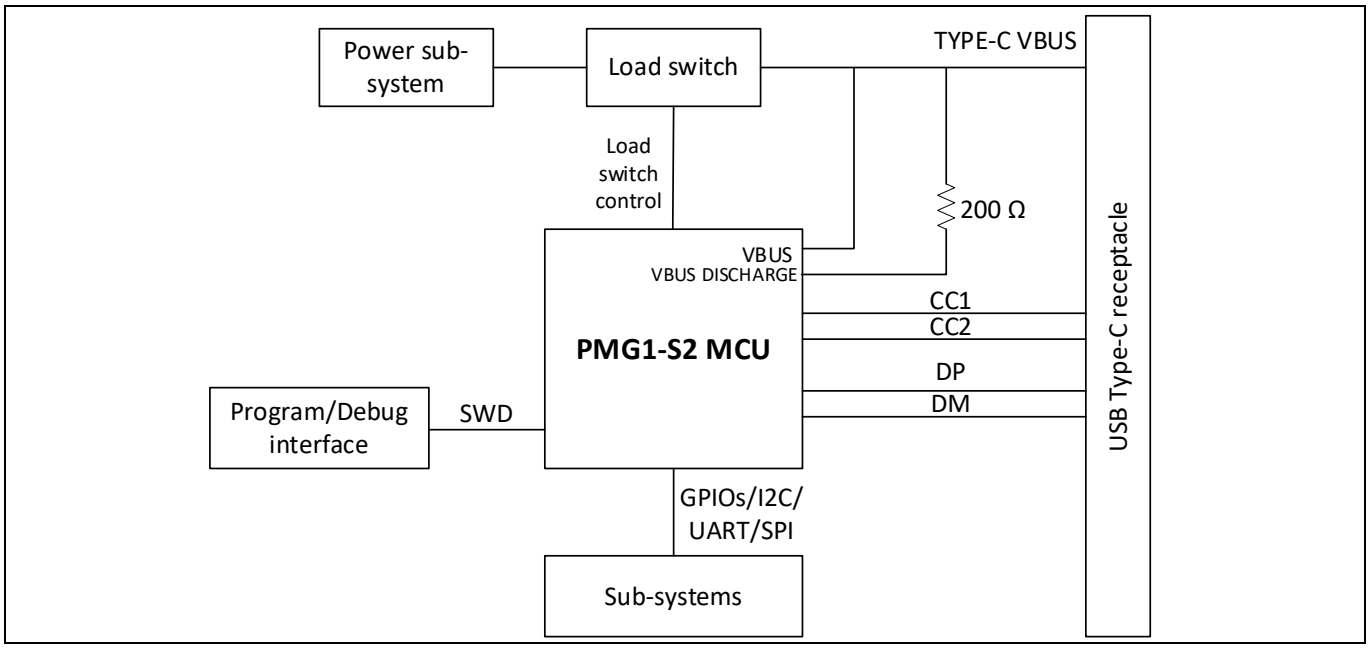

Figure 2 USB PD sink-only application using EZ-PD™ PMG1-S2 MCU

4 Schematic design requirements

This section explains the schematic design requirements and considerations for a EZ-PD™ PMG1 MCU-based system. CY711X PMG1-SX prototyping kits are used as the reference for design. See the following kit pages for details:

- **CY7110 EZ-PD™ PMG1-S0 prototyping kit**
- **CY7111 EZ-PD™ PMG1-S1 prototyping kit**
- **CY7112 EZ-PD™ PMG1-S2 prototyping kit**
- **CY7113 EZ-PD™ PMG1-S3 prototyping kit**

4.1 Power system

PMG1 MCUs support powering of the chip directly from the Type-C PD port through the VBUS pin on the MCU. The USB PD sink, dead battery, and other bus-powered applications use the VBUS pin as the power input for the MCU. When powered through VBUS, the internal regulator generates VDDD of 3.3 V for chip operation and further regulated VCCD (1.8 V) for core operation. PMG1 MCUs, except PMG1-S0, have a dedicated power input pin for any USB PD DRP/source-only application and all general MCU applications.

In PMG1-S0, the VDDD voltage can be supplied directly to power the MCU. EZ-PD™ PMG1-S1 and EZ-PD™ PMG1-S2 MCUs have a dedicated power input pin (VSYS), and do not support VDDD as the power input pin. The VSYS power pin is connected to VDDD internally through a switch. The core regulator regulates the VDDD voltage to 1.8 V for core operation and the output of the 1.8-V regulator denoted as VCCD.

A separate power domain, VDDIO, is provided for powering the GPIOs in EZ-PD™ PMG1-S1 and EZ-PD™ PMG1-S2 MCUs. The VDDD and VDDIO pins can be shorted if required. These devices support VCONN functionality; additional input supply option is available in the silicon for powering VCONN FETs.

Table 3 summarizes the power inputs in EZ-PD™ PMG1 MCUs.

Table 3 EZ-PD™ PMG1 MCU power pins and operating voltages

MCU	Power pin	Power pin description	Valid input voltage level
EZ-PD™ PMG1-S0 MCU	VBUS	Bus power	4.0 V – 21.5 V
	VDDD	MCU power input, internal LDO output	2.7 V – 5.5 V
	VCCD	The core voltage of the device is brought out to the pin. This pin cannot be used as a voltage source and is intended to connect only a decoupling capacitor.	
EZ_PD™ PMG1-S1 MCU	VBUS	Bus power	4.0 V - 21.5 V
	VSYS	Device power input	2.75 V – 5.5 V
	VDDIO	Supply for I/Os	1.8 V – VDDD
	VCONN_ Source	Supply to VCONN FETs	
	VCCD	The core voltage of the device is brought out to the pin. This pin cannot be used as a voltage source and is intended to connect only a decoupling capacitor.	
EZ-PD™ PMG1-S2 MCU	VBUS	Bus power	4.0 V - 21.5 V
	VSYS	Device power input	2.75 V – 5.5 V
	VDDIO	Supply for I/Os	1.8 V – VDDD

MCU	Power pin	Power pin description	Valid input voltage level
	VCONN_ Source	Supply to VCONN FETs	
	VCCD	The core voltage of the device is brought out to the pin. This pin cannot be used as a voltage source and is intended to connect only a decoupling capacitor.	
EZ-PD™ PMG1-S3 MCU	VBUS	Bus power	4.0 V - 28 V
	VSYS	Device power input	2.8 V – 5.5 V
	VDDIO	Supply for I/Os	1.8 V – VDDD
	VDDA	Supply for analog blocks	1.8 V – VDDD
	VCONN_ Source	Supply to VCONN FETs	
	VCCD	The core voltage of the device is brought out to the pin. This pin cannot be used as a voltage source and is intended to connect only a decoupling capacitor.	

Use the Following power system design considerations for USB PD sink application using EZ-PD™ PMG1 MCUs:

- Ensure that the VBUS pin of the MCU is the power input pin. Connect the power pin of the Type-C connector to the VBUS pin as shown in **Figure 3** and **Figure 4**.
- Do not connect the other input pin (VDDD in EZ-PD™ PMG1-S0 and EZ-PD™ PMG1-S3, and VSYS in EZ-PD™ PMG1-S1/S2 MCUs) to any power rail. Connect decoupling capacitors to those pins (see **Table 3** for the decoupling capacitor value).
- Short VDDD and VDDIO pins in EZ-PD™ PMG1-S1 MCU and EZ-PD™ PMG1-S2 MCU.
- Short VDDD, VDDA, and VDDIO in EZ-PD™ PMG1-S3 MCU.
- Do not connect any signal or power rail to VCCD; add only the decoupling capacitor.

4.1.1 Decoupling and bypass capacitors

Add decoupling and bypass capacitors to all power input pins and internal regulator output pins to filter out AC noise/voltage spikes and decouple the device power domains. **Table 4** lists the recommended values of decoupling and bypass capacitors for each power domain signal in the EZ-PD™ PMG1 family MCUs.

For VDDD, VBUS, and VSYS, it is recommended to use multiple capacitor decoupling circuit to improve filtering and reduce the effect of ESR of the capacitor. Along with recommended values, you can place one or two low-ESR 100-nF capacitors as the decoupling capacitor.

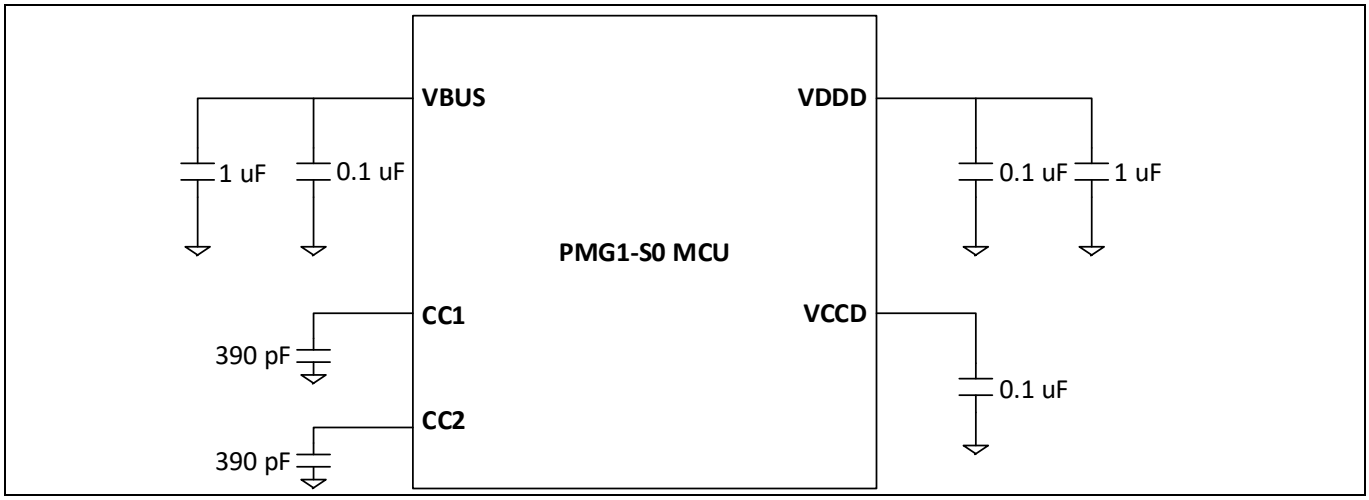

Figure 3 EZ-PD™ PMG1-S0 MCU decoupling capacitor

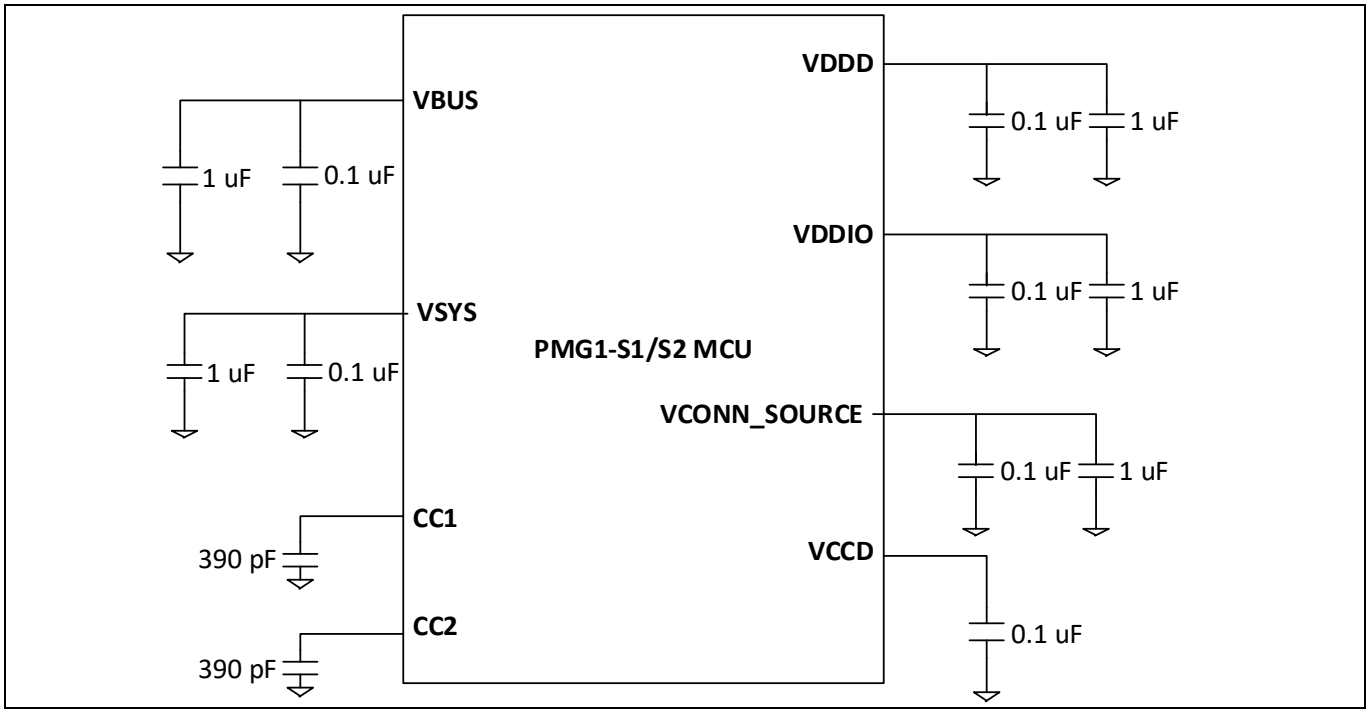

Figure 4 EZ-PD™ PMG1-S1, EZ-PD™ PMG-S2 MCUs decoupling capacitors

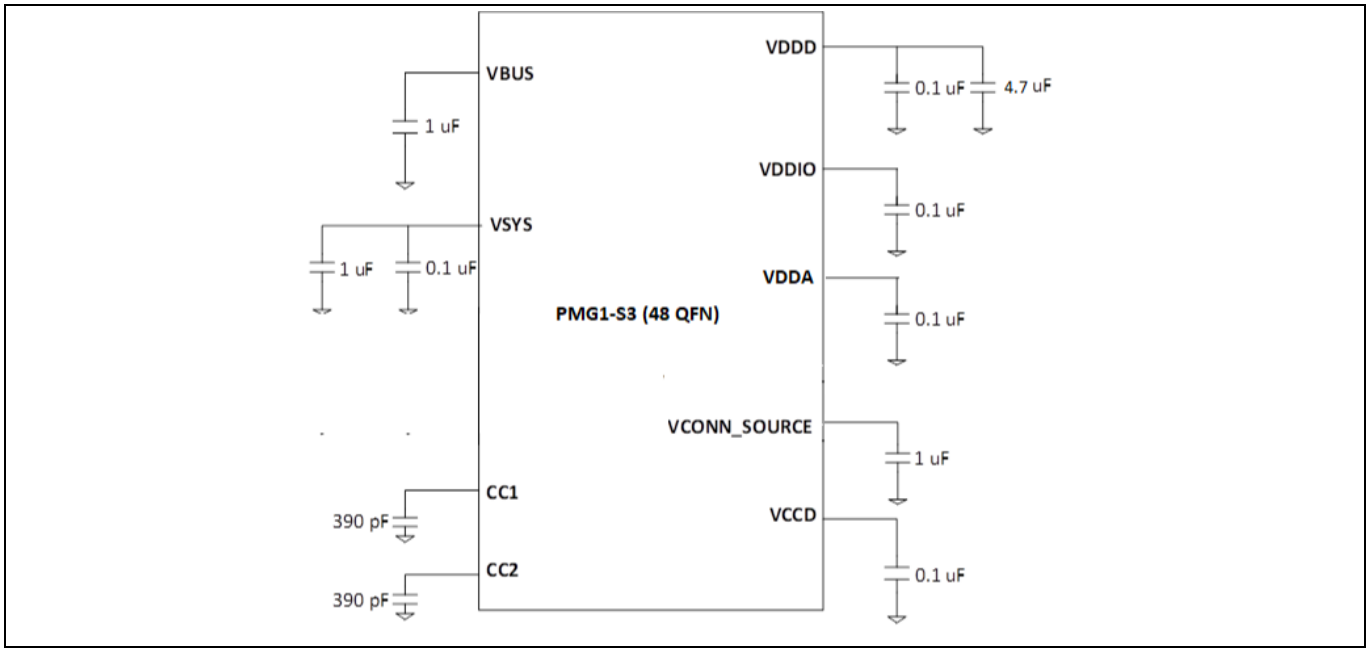

Figure 5 EZ-PD™ PMG1-S3 (48-QFN) MCU decoupling capacitors

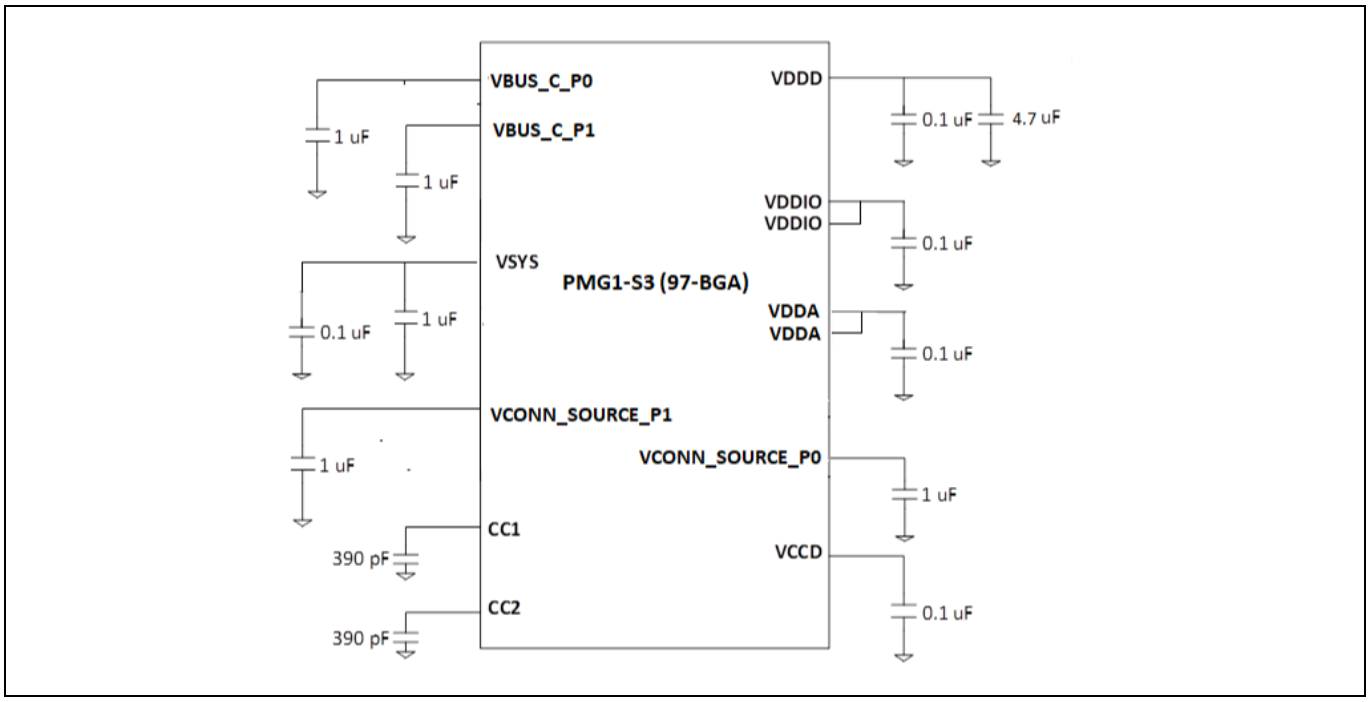

Figure 6 EZ-PD™ PMG1-S3 (97-BGA) MCU decoupling capacitors

Table 4 Power supply pins and decoupling capacitors

MCU	Power supply pin	Decoupling capacitor
EZ-PD™ PMG1-S0 MCU	VBUS	1 µF
	VDDD	1 µF
	VCCD	1 µF
EZ-PD™ PMG1-S1 MCU	VBUS	1 µF
	VSYS	1 µF

MCU	Power supply pin	Decoupling capacitor
	VDDIO	0.1 µF
	VCONN_ Source	1 µF
	VCCD	1 µF
EZ-PD™ PMG1-S2 MCU	VBUS	1 µF
	VSYS	1 µF
	VDDIO	0.1 µF
	VCONN_ Source	1 µF
	VCCD	1 µF
EZ-PD™ PMG1-S3 MCU (48-QFN)	VBUS	1 µF
	VSYS	0.1 µF and 1 µF
	VDDD	4.7 uF & 1uF
	VDDIO	0.1 µF
	VCONN_ Source	1 µF
	VCCD	0.1 µF
	VDDA	0.1 µF
EZ-PD™ PMG1-S3 MCU (97-BGA)	VBUS_C_P0	1 µF
	VBUS_C_P1	1 µF
	VSYS	0.1 µF and 1 µF
	VDDD	4.7 uF and 1uF
	VDDIO	0.1 µF
	VCONN_ Source_P0	1 µF
	VCONN_ Source_P1	1 µF
	VCCD	0.1 µF
	VDDA	0.1 µF

4.2 External voltage regulators

External voltage regulators are required in the application when an external module has higher current requirement than the EZ-PD™ PMG1 MCU GPIOs can supply. The GPIOs can source or sink a maximum current of 25 mA (per GPIO).

Linear dropout (LDO) regulators are required in the EZ-PD™ PMG1 MCU designs to power various sub-systems, such as LEDs, sensor modules, extension, adapter board, and so on, in the solution or design. Select the LDO by considering the required output voltage, maximum load current, and power ratings.

Table 5 lists the recommended LDOs.

Table 5 Recommended LDO regulators

MPN	Manufacturer	Input voltage max	Output voltage	Output current	Application
IFX25001	Infineon	45 V	2.5 V, 3.3 V, 5.0 V, 8.5 V, or 10.0 V	400 mA	Standard
TLE42744	Infineon	40 V	5 V and 3.3 V ±2%	400 mA	Automotive

MPN	Manufacturer	Input voltage max	Output voltage	Output current	Application
IFX27001	Infineon	40 V	1.5 V, 1.8 V, 2.6 V, 3.3 V, 5.0 V, or Adjustable output voltage	1 A	Standard

4.3 Reset circuit and clock

EZ-PD™ PMG1 MCUs, except EZ-PD™ PMG1-S0, have an external reset control pin, XRES, to manually reset the MCU. These MCUs have active LOW reset, and should be held LOW for a minimum of 5 µs to reset the chip. All PMG1 MCUs support the power-on-reset (POR) mechanism.

- In EZ-PD™ PMG1-S1 MCU, the reset pin should be pulled up to VDDIO/VDDD using a 4.7 k resistor. This will make sure that the XRES pin is not left floating in the design and the device can function properly.

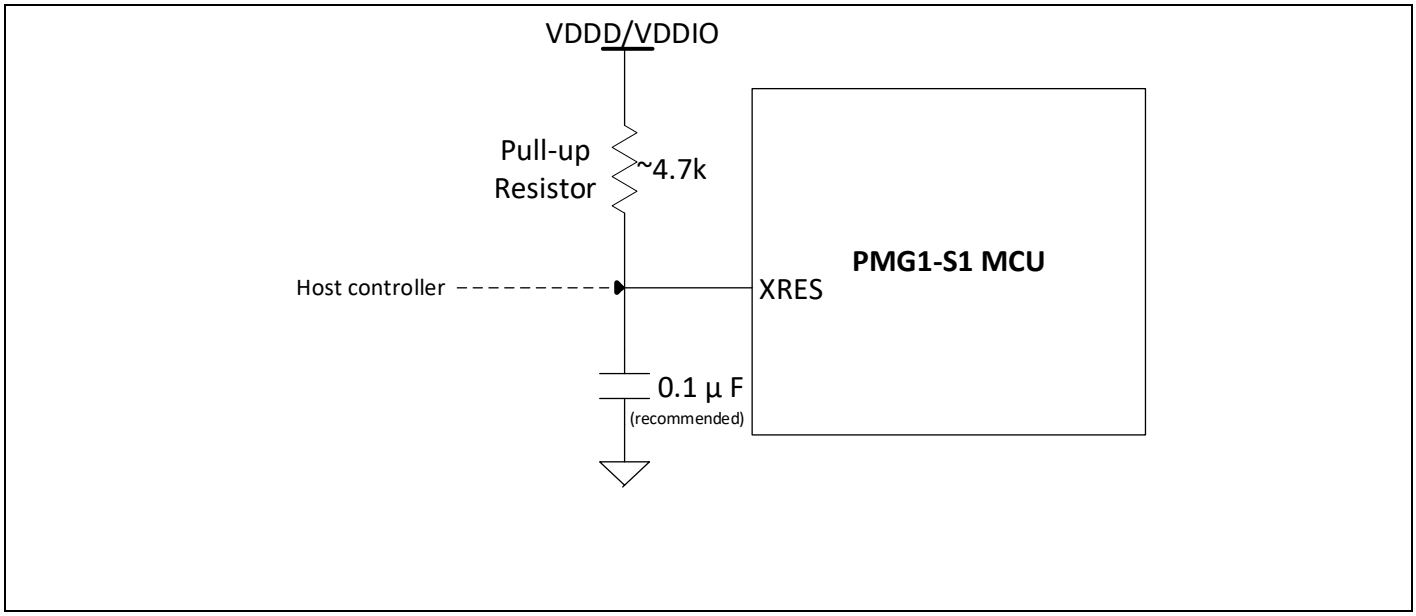

Figure 7 EZ-PD™ PMG1-S1 MCU XRES pin connection

- EZ-PD™ PMG1-S2 MCU has an internal pull-up on the XRES pin; this means that an external pull-up resistor is not required.

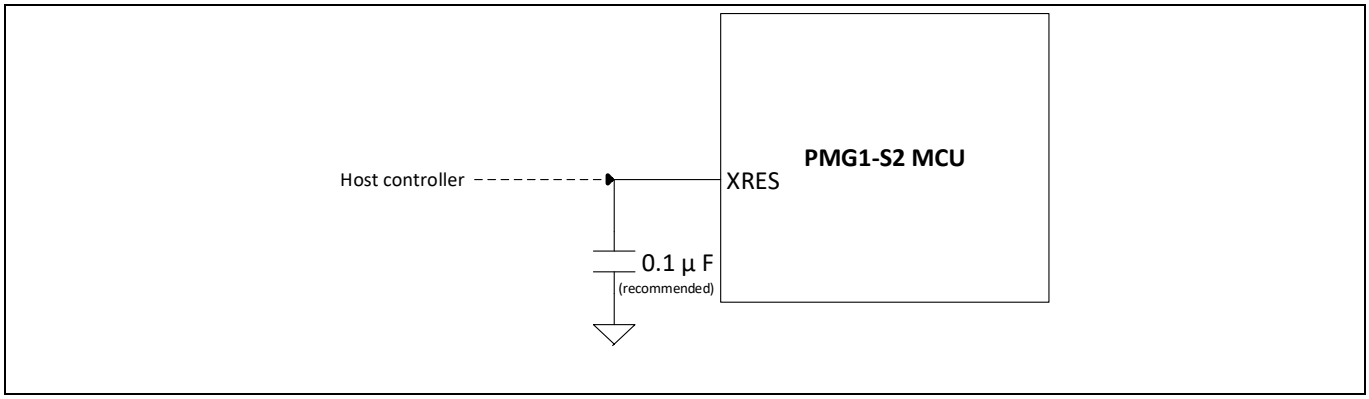

Figure 8 EZ-PD™ PMG1-S2 MCU XRES pin connection

- It is recommended to connect a capacitor (typically 0.1 µF) to the XRES pin to filter out glitches and to give the reset signal better noise immunity.
- In EZ-PD™ PMG1-S3 MCU, the reset pin should be pulled up to VDDIO/VDDD using a 4.7 k resistor. This will ensure that the XRES pin is not left floating in the design and the device can function properly.

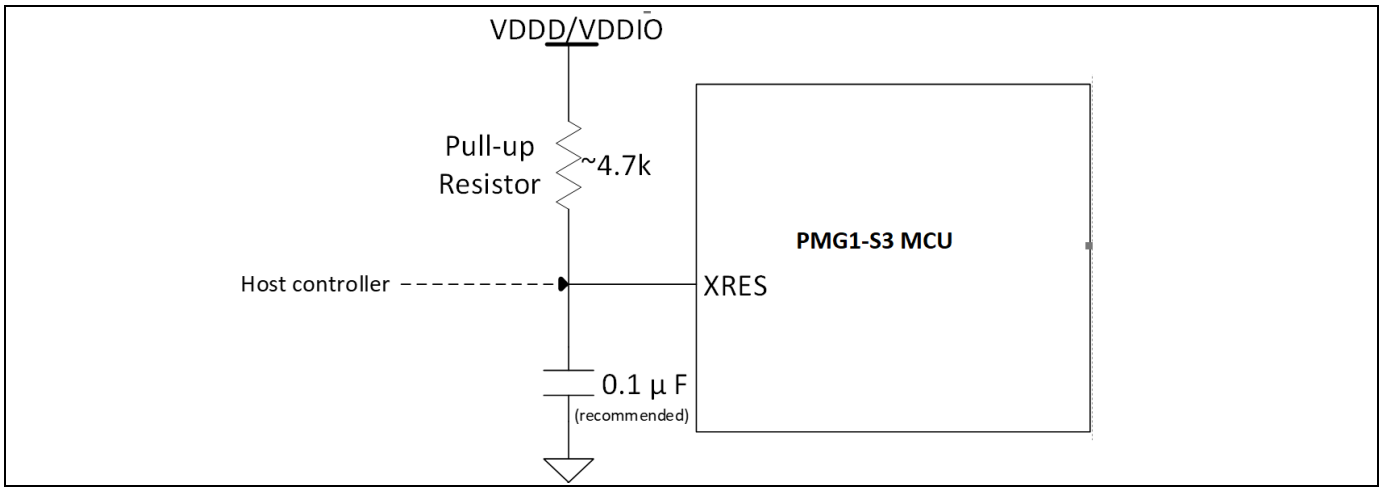

Figure 9 EZ-PD™ PMG1-S3 MCU XRES pin connection

- Optionally, if EZ-PD™ PMG1 MCU is controlled by an external controller, the XRES pin can be directly driven by the host.

EZ-PD™ PMG1 MCUs have an integrated clock circuitry; external components such as a crystal or oscillator are not required.

4.4 GPIO

EZ-PD™ PMG1 MCUs provide flexible GPIOs with alterative connection to digital and analog peripherals. Different peripherals have different dedicated or fixed pins for their terminals. The USB PD pins are fixed signals connected to USB PD subsystem.

4.4.1 I/O pin selection

Table 6 lists the MCU pins assigned for digital block, analog block, and USB sub-system.

Table 6 EZ-PD™ PMG1 MCU pin assignment

Block	Pin name	Pin #			Remarks
		EZ-PD™ PMG1-S0 MCU	EZ-PD™ PMG1-S1 MCU	EZ-PD™ PMG1-S2 MCU	
System function pins					
Reset	XRES	N/A	10	26	Reset input
USB and USB PD					
USB PD Sub system	CC1	15	9	5	Configuration Channel
	CC2	14	7	3	
	CSN	N/A	40	39	Current Sense

Schematic design requirements

Block	Pin name	Pin #			Remarks
		EZ-PD™ PMG1-S0 MCU	EZ-PD™ PMG1-S1 MCU	EZ-PD™ PMG1-S2 MCU	
	CSP	N/A	1	40	
	DP	17	N/A	21	USB D+/D- signals
	DM	16	N/A	22	
	DP_SYS	N/A	23	N/A	
	DM_SYS	N/A	24	N/A	
	DP_TOP	N/A	28	N/A	
	DM_TOP	N/A	27	N/A	
	DP_BOT	N/A	26	N/A	
	DM_BOT	N/A	25	N/A	
	FET control pins				Load switch control pins
Digital pins					
Serial communication block (SCB)	SCB Pins	See **Table 10**			PMG1-S0 MCU has two SCBs and PMG1-S1 and PMG1-S2 MCUs have four SCBs. The SCBs can be configured as SPI, I2C, or UART.
TCPWM	TCPWM pins	See **Table 12**			PMG1-S0 and PMG1-S2 MCUs have four TCPWM, while PMG1-S1 MCU has two TCPWM. All these signals are routed to dedicated GPIO pins.
Analog Pins					
SAR ADC	ADC	See the datasheet **[4]**			PMG1-S0 and PMG1-S2 MCUs have 2x 8-bit ADC and PMG1-S1 has one 8-bit ADC.

Table 7 EZ-PD™PMG1-S3 MCU pin assignment

Block	Pin Name	Pin #		Remarks
		EZ-PD™ PMG1-S3 MCU 48-QFN	EZ-PD™ PMG1-S3 MCU 97-BGA	
System function pins				
Reset	XRES	33	E14	Reset input
USB and USB PD				
USB PD Sub system	CC1/P0	28	N14 & N15	Configuration Channel P0

Block	Pin Name	Pin #		Remarks
		EZ-PD™ PMG1-S3 MCU 48-QFN	EZ-PD™ PMG1-S3 MCU 97-BGA	
	CC2/P0	30	J14 & J15	
	CC1_P1	N/A	N1 & N2	Configuration Channel P1
	CC2_P1	N/A	J1 & J2	
	CSN/P0	37	A15	Current Sense for P0
	CSP/P0	38	B15	
	CSN_P1	N/A	C14	Current Sense for P1
	CSP_P1	N/A	C15	
	DP	39	A13	USB D+/D- signals
	DM	40	A11	
	VBUS_IN_NGDO/P0	24	R14	Load switch control pins For Port0
	VBUS_IN_CTRL/P0	27	P14	
	VBUS_OUT_CTRL/P0	26	P15	
	VBUS_OUT_NGDO/P0	25	R15	
	VBUS_IN_NGDO_P1	N/A	R2	Load switch control pins For Port1
	VBUS_IN_CTRL_P1	N/A	P2	
	VBUS_OUT_CTRL_P1	N/A	P1	
	VBUS_OUT_NGDO_P1	N/A	R1	
Digital pins				
Serial communication block (SCB)	SCB Pins	See **Table 10**		PMG1-S3 QFN has seven SCBs and PMG1-S3 BGA has eight SCBs. The SCBs can be configured as SPI, I2C, or UART
TCPWM	TCPWM pins	See **Table 12**		PMG1-S3 QFN has seven TCPWM and PMG1-S1 has eight TCPWM. All these signals are routed to dedicated GPIO pins.
Analog pins				
SAR ADC	ADC	See the datasheet **[4]**		PMG1-S3 QFN and PMG1-S3 BGA have 2x 8-bit ADC and one 12-bit ADC.

4.4.2 Overvoltage-tolerant GPIO

All EZ-PD™ PMG1-MCUs have two overvoltage-tolerant (OVT) pins; I^2C signal pins (I2C SDA and I2C SCL) from SCB0 are the OVT pins. These GPIOs are capable of handling an absolute maximum voltage of 6 V. The pins are similar to regular GPIOs with additional features such as overvoltage tolerance, and better pull-down drive strength. When SCB0 is configured as an I^2C component, it meets the following I^2C specifications:

- Fast Mode hot-swap

- Fast Mode Plus specification
- Fast Mode and Fast Mode Plus hysteresis and minimum fall time specifications

Table 8 lists the OVT-GPIOs for each MCU in the EZ-PD™ PMG1 MCU family.

Table 8 OVT-GPIOs

	EZ-PD™ PMG1-S0 MCU	EZ-PD™ PMG1-S1 MCU	EZ-PD™ PMG1-S2 MCU	EZ-PD™ PMG1-S3 MCU 48-QFN	EZ-PD™ PMG1-S3 MCU 97-BGA
OVT-GPIO (GPIO [MCU pin#])	P0.0 [7]	P5.0 [16]	P0.0 [27]	P4.0 [34]	P4.0 [E15]
	P0.1 [8]	P5.1 [17]	P0.1 [28]	P4.1 [35]	P4.1 [D12]

4.5 Programming and debugging interfaces

EZ-PD™ PMG1 MCU supports the serial wire debug (SWD) protocol for programming and debugging. The SWD data and SWD clock signals are available on specific GPIOs of the MCU. **Table 9** lists the SWD pin mapped GPIOs in all devices. EZ-PD™ PMG1-S1 and EZ-PD™ PMG1-S2 devices support reset mode for acquiring the device for programming or debugging. In reset mode, the programmer/debugger applies reset signal over the XRES pin on the MCU. The device should be powered externally while using this mode, or the programmer should be able to power the chip.

Table 9 SWD signal pin assignment

	GPIO port [MCU pin#]				
	EZ-PD™ PMG1-S0 MCU	EZ-PD™ PMG1-S1 MCU	EZ-PD™ PMG1-S2 MCU	EZ-PD™ PMG1-S3 MCU 48-QFN	EZ-PD™ PMG1-S3 MCU 97-BGA
SWD IO (SWD Data)	P0.0 [7]	P1.4 [6]	P2.0 [15]	P1.2[13]	P1.1 [P3]
SWD CLK (SWD Clock)	P0.1 [8]	P1.0 [2]	P2.1 [16]	P1.1[12]	P1.2 [R3]

EZ-PD™ PMG1-S0 MCU does not have a reset signal; the device is acquired in power cycle mode. In power cycle mode, the target MCU is acquired by toggling the device power; the device should not be externally powered in this mode.

SWD signals can be routed to 5-pin or 10-pin standard SWD connector so that it can be used as programming/debugging connector. **Figure 10** and **Figure 11** show the standard 5-pin and 10-pin SWD connector pinout, respectively. In PMG1-S0 MCU, the reset pin of the header should be left unconnected.

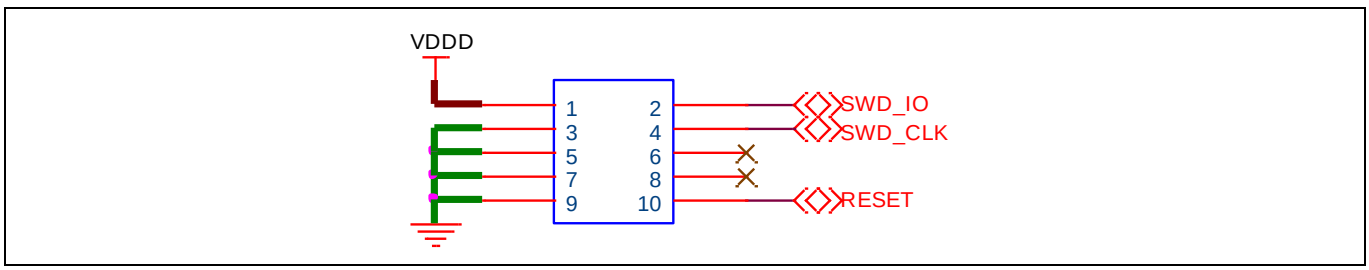

Figure 10 10-pin SWD header

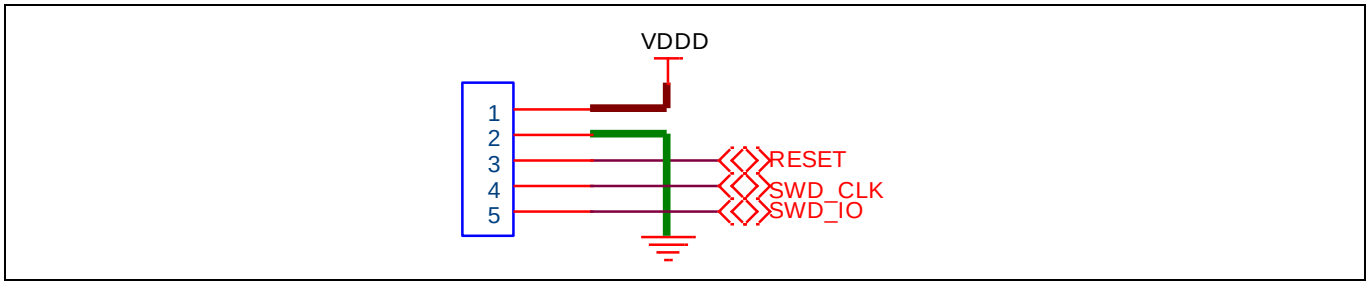

Figure 11 5-pin SWD header

4.6 Digital blocks

4.6.1 Serial communication block (SCB)

SCBs are multifunctional hardware blocks that implement UART, I2C, and SPI communication components. You can use any available SCB and configure it as the desired communication block in Eclipse IDE for ModusToolbox™ software. The communication signals, in SCB, are routed to specific GPIOs. See **Table 10** for the details of assignment.

4.6.1.1 Serial peripheral interface (SPI)

EZ-PD™ PMG1 MCUs can operate in SPI master and slave modes. The SCB supports single master-multiple slave topology for SPI. Use SPI master mode when PMG1 has to communicate with one or more SPI slave devices; use slave mode when EZ-PD™ PMG1 MCU has to communicate with an SPI master. The SCB offers different protocol types, data frame size, and configurable parameters as SPI peripheral.

4.6.1.2 I2C

The EZ-PD™ PMG1 MCU supports master and slave modes of operation for I2C. The I2C peripheral offers configurability to multiple I2C parameters. The I2C signals does not have any internal pull-ups in the MCU. You have to pull-up the signals to VDDIO/VDDD using 2.2 k resistor.

4.6.1.3 UART

UART communication is typically point-to-point communication protocol through Tx and Rx signals. Tx or transmitter output transmits the data, and Rx or receiver input receives data from the other module. Rx of the EZ-PD™ PMG1 MCU should be connected to Tx of the other module and Tx of the EZ-PD™ PMG1 MCU should connect to Rx of the module.

Table 10 lists the GPIO pin assignment for SCBs in EZ-PD™ PMG1 MCUs.

Table 10 EZ-PD™ PMG1 MCU SCBs and pin assignment

Component	Signal	Port and pin assignment (Port [MCU pin])			
		SCB0	SCB1	SCB2	SCB3
EZ-PD™ PMG1-S0 MCU					
UART	UART_RX	P2.3 [13] or P2.1 [10]	P1.3 [6] or P3.1 [16]		
	UART_TX	P2.2 [12] or P2.0 [9]	P1.2 [5] or P3.0 [17]		

Component	Signal	Port and pin assignment (Port [MCU pin])			
		SCB0	SCB1	SCB2	SCB3
	UART_CTS	P0.0 [7]	P1.0 [1]		
	UART_RTS	P0.1 [8]	P1.1 [2]		
I2C	I2C_SDA	P0.0 [7]	P1.0 [1] or P2.2 [12]		
	I2C_SCL	P0.1 [8]	P1.1 [2] or P2.3 [13]		
SPI	SPI_MOSI	P1.2 [5]	P0.0 [7]		
	SPI_MISO	P1.1 [2]	P0.1 [8]		
	SPI_SEL	P1.0 [1]	P2.0 [9]		
	SPI_CLK	P1.3 [6]	P2.1 [10]		
EZ-PD™ PMG1-S1 MCU					
UART	UART_RX	P3.0 [18]	P1.0 [2]	P4.1 [30]	P0.1 [39]
	UART_TX	P5.1 [17]	P1.1 [3]	P4.0 [29]	P0.0 [38]
	UART_CTS	P2.2 [15]	P1.2 [4]	P3.1 [20]	P2.0 [13]
	UART_RTS	P5.0 [16]	P1.3 [5]	P3.2 [21]	P2.1 [14]
I2C	I2C_SDA	P5.0 [16]	P1.1 [3]	P3.1 [20]	P2.1 [14]
	I2C_SCL	P5.1 [17]	P1.2 [4]	P3.2 [21]	P2.0 [13]
SPI	SPI_MOSI	P5.0 [16]	P1.1 [3]	P3.2 [21]	P2.1 [14]
	SPI_MISO	P5.1 [17]	P1.2 [4]	P4.0 [29]	P0.0 [38]
	SPI_SEL	P2.2 [15]	P1.0 [2]	P3.1 [20]	P2.0 [13]
	SPI_CLK	P3.0 [18]	P1.3 [5]	P4.1 [30]	P0.1 [39]
EZ-PD™ PMG1-S2 MCU					
UART	UART_RX	P2.6 [25] or P1.2 [9]	P1.7 [14]	P1.1 [8]	P1.5 [13]
	UART_TX	P2.5 [24] or P1.3 [10]	P1.6 [11]	P1.0 [7]	P1.4 [12]
	UART_CTS	P0.0 [27]	P2.0 [15]	P3.4 [36]	P1.2 [9]
	UART_RTS	P0.1 [28]	P2.1 [16]	P3.5 [37]	P1.3 [10]
I2C	I2C_SDA	P0.0 [27]	P2.1 [16]	P3.4 [36]	P1.3 [10]
	I2C_SCL	P0.1 [28]	P2.0 [15]	P3.5 [37]	P1.2 [9]
SPI	SPI_MOSI	P2.5 [24]	P2.1 [16]	P3.4 [36]	P1.2 [9]
	SPI_MISO	P0.1 [28]	P1.6 [11]	P1.0 [7]	P1.4 [12]
	SPI_SEL	P0.0 [27]	P1.7 [14]	P1.1 [8]	P1.5 [13]
	SPI_CLK	P2.6 [25]	P2.0 [15]	P3.5 [37]	P1.3 [10]

Table 11 EZ-PD™ PMG1-S3 SCBs and pin assignment

Component	Signal	Port and pin assignment (Port [MCU pin])							
		SCB0	SCB1	SCB2	SCB3	SCB4	SCB5	SCB6	SCB7
EZ-PD™ PMG1-S3 MCU 97-BGA									

Schematic design requirements

Component	Signal	Port and pin assignment (Port [MCU pin])							
		SCB0	**SCB1**	**SCB2**	**SCB3**	**SCB4**	**SCB5**	**SCB6**	**SCB7**
UART	UART_RX	P4.0 [E15]	P7.0 [G15]	P5.0 [G2]	P1.1 [P3]	P3.5 [F4]	P2.2 [A3]	P6.1 [P5]	P7.4 [B11]
	UART_TX	P4.1 [D12]	P1.5 [M12]	P5.1 [E1]	P1.2 [R3]	P3.6 [E2]	P2.3 [B5]	P6.0 [R5]	P7.3 [B13]
	UART_CTS	P2.4 [A7]	P2.7 [A8]	P5.2 [H6]	P1.3 [K4]	P3.0 [A1]	P2.5 [A5]	P6.3 [R13]	P7.5 [A9]
	UART_RTS	P2.1 [B2]	P2.6 [B7]	P5.3 [H1]	P1.4 [M10]	P3.3 [B1]	P2.0 [A2]	P6.2 [P13]	P7.6 [B9]
I2C	I2C_SDA	P4.1 [D12]	P1.5 [M12]	P5.1 [E1]	P1.2 [R3]	P3.6 [E2]	P2.2 [A3]	P6.0 [R5]	P7.3 [B13]
	I2C_SCL	P4.0 [E15]	P1.6 [K12]	P5.0 [G2]	P1.1 [P3]	P3.5 [F4]	P2.3 [B5]	P6.1 [P5]	P7.4 [B11]
SPI	SPI_MOSI	P4.1 [D12]	P2.6 [B7]	P5.1 [E1]	P1.3 [K4]	P3.0 [A1]	P2.2 [A3]	P6.3 [R13]	P7.5 [A9]
	SPI_MISO	P2.4 [A7]	P1.5 [M12]	P5.2 [H6]	P1.2 [R3]	P3.6 [E2]	P2.3 [B5]	P6.0 [R5]	P7.3 [B13]
	SPI_SEL	P2.1 [B2]	P2.7 [A8]	P5.3 [H1]	P1.4 [M10]	P3.3 [B1]	P2.0 [A2]	P6.2 [P13]	P7.6 [B9]
	SPI_CLK	P4.0 [E15]	P1.6 [K12]	P5.0 [G2]	P1.1 [P3]	P3.5 [F4]	P2.3 [B5]	P6.1 [P5]	P7.4 [B11]
EZ-PD™ PMG1-S3 MCU 48-QFN									
UART	UART_RX	P4.0 [34]	N/A	P5.0 [7]	P1.1 [12]	P3.5 [3]	N/A	P6.1 [16]	N/A
	UART_TX	P4.1 [35]	N/A	P5.1 [8]	P1.2 [13]	P3.6 [4]	N/A	P6.0 [15]	N/A
	UART_CTS	P2.4 [45]	N/A	P5.2 [9]	P1.3 [14]	P3.0 [1]	N/A	P6.3 [19]	N/A
	UART_RTS	P2.1 [48]	N/A	P5.3 [10]	P1.4 [20]	P3.3 [2]	N/A	P6.2 [18]	N/A
I2C	I2C_SDA	P4.1 [35]	P1.5 [21]	P5.1 [8]	P1.2 [13]	P3.6 [4]	P2.3 [47]	P6.0 [15]	N/A
	I2C_SCL	P4.0 [34]	P1.5 [22]	P5.0 [7]	P1.1 [12]	P3.5 [3]	P2.3 [46]	P6.1 [16]	N/A
SPI	SPI_MOSI	P4.1 [35]	N/A	P5.1 [8]	P1.3 [14]	P3.6 [4]	N/A	P6.3 [19]	N/A
	SPI_MISO	P2.4 [45]	N/A	P5.2 [9]	P1.2 [13]	P3.0 [1]	N/A	P6.0 [15]	N/A
	SPI_SEL	P2.1 [48]	N/A	P5.3 [10]	P1.4 [20]	P3.3 [2]	N/A	P6.2 [18]	N/A
	SPI_CLK	P4.0 [34]	N/A	P5.0 [7]	P1.1 [12]	P3.5 [3]	N/A	P6.1 [16]	N/A

4.6.2 Timer, counter, and pulse width modulator (TCPWM)

TCPWM is a multifunctional component that implements core microcontroller functionality. EZ-PD™ PMG1-S0 and EZ-PD™ PMG1-S2 MCUs have four TCPWM blocks and EZ-PD™ PMG1-S1 has two TCPWM blocks. TCWM block in EZ-PD™ PMG1 MCU implements the 16-bit timer, counter, pulse width modulator, and quadrature decoder functionality. The block can be used to measure the period and pulse width of an input signal (timer), find the number of times a particular event occurs (counter), generate PWM signals, or decode quadrature signals. **Table 12** lists the line output pin of TCPWM blocks in PMG1 MCUs. See the datasheet **[4]** for more details.

Table 12 List of TCPWM output pins

TCPWM signal	GPIO port [MCU Pin#]					Description
	EZ-PD™ PMG1-S0 MCU	EZ-PD™ PMG1-S1 MCU	EZ-PD™ PMG1-S2 MCU	EZ-PD™ PMG1-S3 MCU 48QFN	EZ-PD™ PMG1-S3 MCU 97-BGA	
TCPWM_line_0	P0.0 [7] P2.2 [12]	P1.2 [4]	P3.2 [34] P0.0 [27]	P6.2[18]	P6.2[P13]	Output of TCPWM-0
TCPWM_line_1	P0.1 [8] P2.3 [13]	P1.4 [6]	P3.3 [35] P0.1 [28]	N/A	P0.2[P8]	Output of TCPWM-1
TCPWM_line_2	P2.0 [9] P1.0 [1]	N/A	P3.4 [36]	P2.1[48]	P2.1[B2]	Output of TCPWM-2
TCPWM_line_3	P2.1 [10] P1.1 [2]	N/A	P3.5 [37]	P2.4[45]	P2.4[A7]	Output of TCPWM-3
TCPWM_line_4	N/A	N/A	N/A	P1.3[14]	P1.3[K4]	Output of TCPWM-4
TCPWM_line_5	N/A	N/A	N/A	P1.4[20]	P1.4[M10]	Output of TCPWM-5
TCPWM_line_6	N/A	N/A	N/A	P3.0[1]	P3.0[A1]	Output of TCPWM-6
TCPWM_line_7	N/A	N/A	N/A	P3.3[2]	P3.3[B1]	Output of TCPWM-7
TCPWM_line_4	N/A	N/A	N/A	P1.3[14]	P1.3[K4]	Output of TCPWM-4
TCPWM_line_5	N/A	N/A	N/A	P1.4[20]	P1.4[M10]	Output of TCPWM-5
TCPWM_line_6	N/A	N/A	N/A	P3.0[1]	P3.0[A1]	Output of TCPWM-6
TCPWM_line_7	N/A	N/A	N/A	P3.3[2]	P3.3[B1]	Output of TCPWM-7

4.7 USB PD block

This section explains the recommended hardware design considerations for USB- data and USB PD designs.

4.7.1 VBUS discharge

Integrated VBUS discharge circuitry discharges VBUS during detach condition or negative voltage transition. EZ-PD™ PMG1-S0 /S1/S3 MCUs have integrated VBUS discharge circuit. The EZ-PD™ PMG1-S2 MCU requires external resistor for discharging VBUS. The VBUS_C discharge switch allows discharging of VBUS through the external resistor. In EZ-PD™ PMG1-S2 MCU based designs, VBUS_DISCHARGE pin of the MCU should be connected to the VBUS pin through an external resistor of 200 Ohm (100 Ohm).

4.7.2 CC and VCONN

EZ-PD™ PMG1 MCUs support USB PD contract of up to 20 V, 5 A (100 W) in sink, source, and DRP roles. CC1 and CC2 pins on the EZ-PD™ PMG1 MCU device should be connected CC1 and CC2 pins on the Type-C PD connector. A 390-pF decoupling capacitor should be connected to CC lines (CC1, CC2) to maintain the signal quality at the signaling rate of 300 kHz. The CC pin decoupling capacitor should be placed as close as possible to the MCU pins.

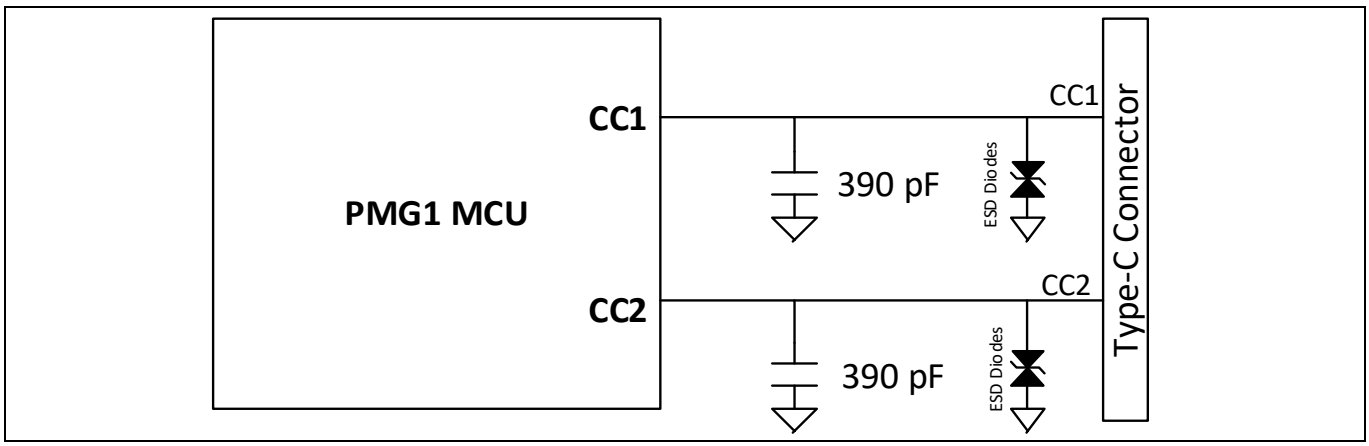

Figure 12 CC1, CC2 signals

If the application supports VCONN functionality in the USB PD port, VCONN_Source should be connected to the voltage source to power internal VCONN FETs. The power source should be capable of handling VCONN power requirement and decoupling capacitors should be placed on the MCU VCONN_Source pin as mentioned in Decoupling and bypass capacitors. VCONN FETs have an associated over current protection (OCP) circuit to protect the chip from VCONN OCP fault. EZ-PD™ PMG1-S0 MCU does not support VCONN functionality.

4.7.3 EZ-PD™ PMG1-S1/S2 MCU gate driver or load switch control signals

The EZ-PD™ PMG1 MCUs have an integrated N-Channel FET, P-Channel FET (PFET), or both Gate drivers to drive FET-based load switches on the provider and consumer path.

EZ-PD™ PMG1-S0 MCU has two P-channel FET gate drivers to drive two external PFETs on the VBUS consumer path. VBUS_FET_CTRL_0 gate driver has an active pull-up, and thus can drive HIGH, LOW, or High-Z. But VBUS_FET_CTRL_1 gate driver can drive only LOW or High-Z thus requires external pull-up. The gate driver signals are VBUS voltage-tolerant.

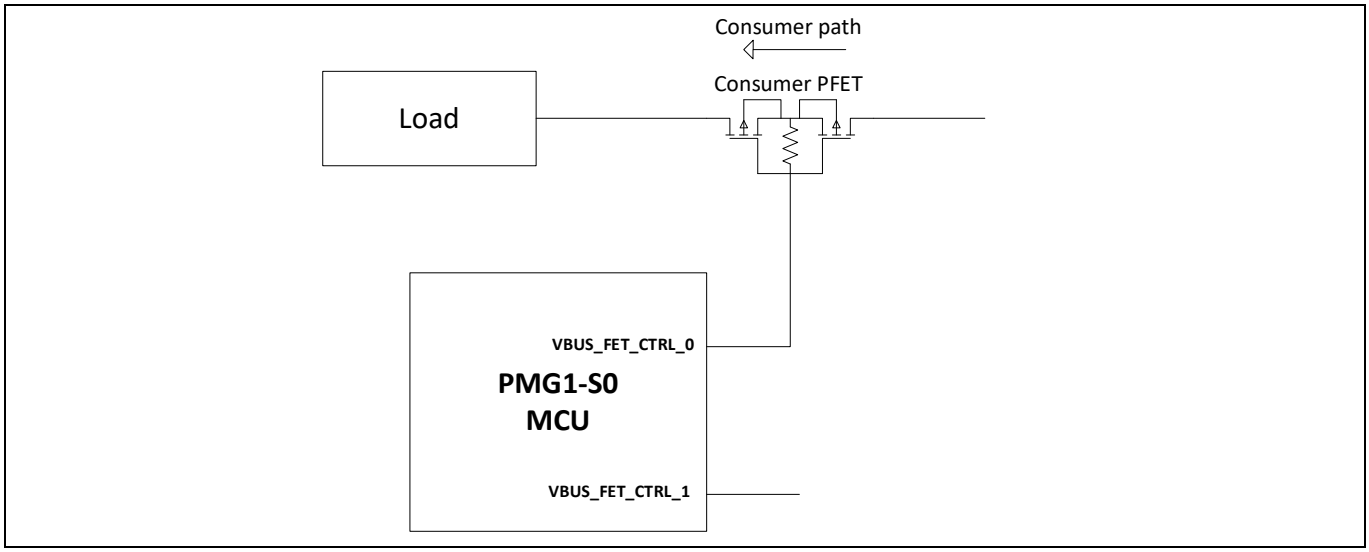

Figure 13 EZ-PD™ PMG1-S0 MCU external FET control

EZ-PD™ PMG1-S1 MCU has an integrated load switch controller with PFET driver to drive external PFETs on the consumer path in DRP and sink only designs. The gate diver requires an external pull-up. The load switch controller also has slew rate-controlled gate driver to drive external PFETs on provider path. The integrated load switch controller has more features compared to normal gate driver. See the EZ-PD™ PMG1-S1 MCU datasheet [4] for details on the load switch controller.

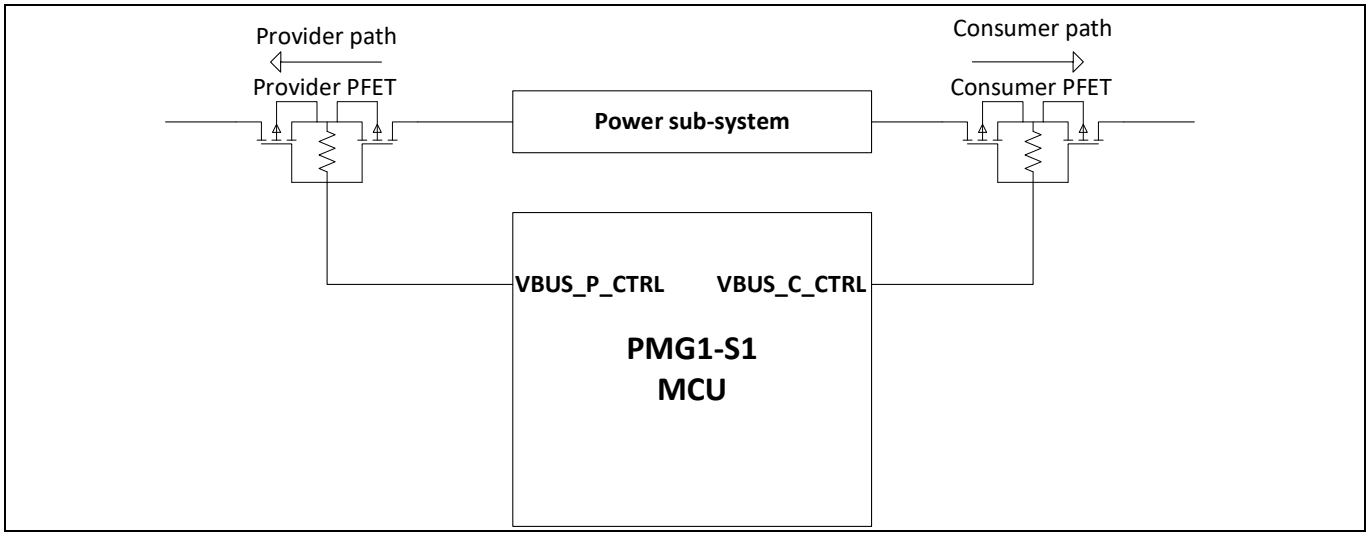

Figure 14 EZ-PD™ PMG1-S1 MCU external FET control

In the EZ-PD™ PMG1-S2 MCU device, N-Channel FET (NFET) and PFET gate drivers are integrated with the MCU. The type of gate driver can be configured in hardware using the P1.0 GPIO pin, to support P and N type external FETs. Floating P1.0 indicates NFET driver and to configure as PFET driver, the pin should be connected to ground. EZ-PD™ PMG1-S2 has two pins, VBUS_P_CTRL0 and VBUS_P_CTRL1, for driving provider path FET and two pins (VBUS_C_CTRL0 and VBUS_C_CTRL1) for driving consumer path FET.

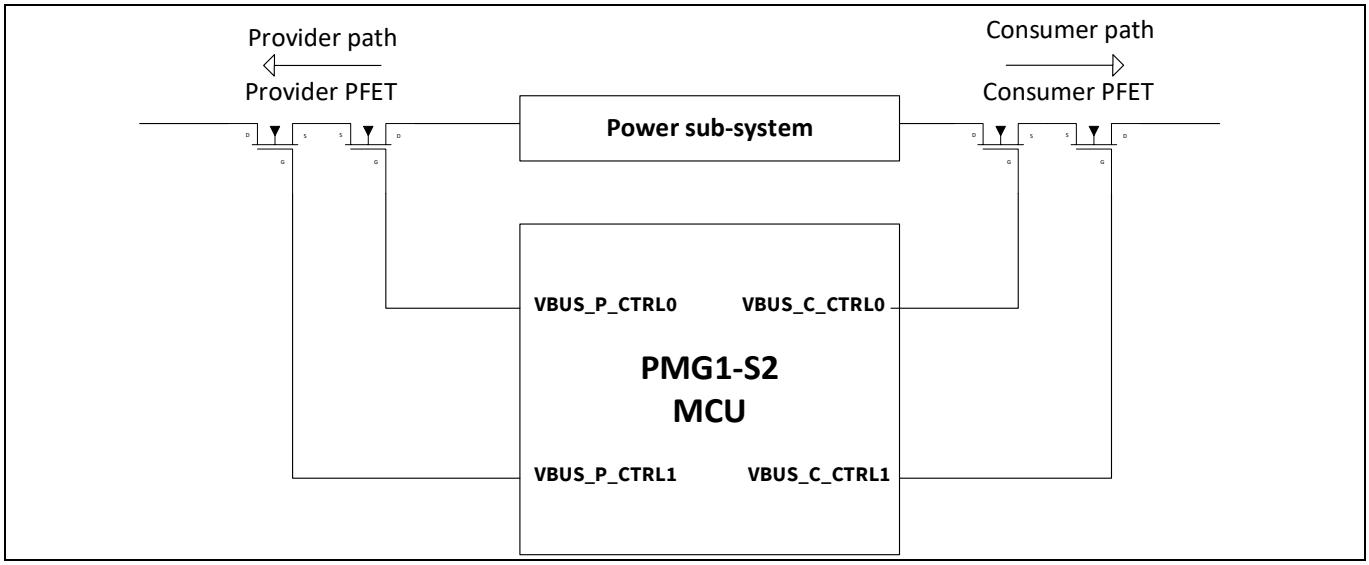

Figure 15 EZ-PD™ PMG1-S2 MCU external FET control

Table 13 lists the EZ-PD™ PMG1 MCU pins assigned to the gate driver/load switch control.

4.7.4 EZ-PD™ PMG1-S3 MCU gate driver or load switch control signals

In the EZ-PD™ PMG1-S3 MCU 48-QFN device, one N-Channel FET (NFET) gate driver is integrated with the MCU. In the EZ-PD™ PMG1-S3 MCU 97-BGA device, two N-Channel FET (NFET) gate drivers are integrated with the MCU. Each gate driver has four pins (VBUS_IN_NGDO, VBUS_IN_CTRL, VBUS_OUT_NGDO and VBUS_OUT_CTRL).

We always mandate two NFET (common drain) solution for load switch implementation and they are referred as IN_NFET and OUT_NFET. The external NFET should have following characteristics:

- Gate source voltage (VGS) should have minimum +/- 20 V.
- Gate to source forward leakage current (IGSS) should be less than 2 µA.

IN_NFET is always connects to DC-DC output for Source only operation and connects to VBUS pin of the Type-C connector for sink only operation. VBUS_IN_NGDO and VBUS_IN_CTRL signals should map to IN_NFET.

- VBUS_IN_NDGO should be connected to Source pin of IN_NFET.
- VBUS_IN_NGDO should be connected to DC-DC output for source only operation.
- VBUS_IN_NGDO should be connected to VBUS pin of the Type-C connector for sink only operation.
- VBUS_IN_NGDO should be connected to VBUS_C pin for sink only operation.
- VBUS_IN_CTRL should to be connected to gate pin of the IN)NFET.
- VBUS_IN_CTRL can source the maximum of current of 4 µA only.

OUT_NFET is always connects to VBUS pin of the Type-C connector for Source only operation and connects to load circuit for sink only operation. VBUS_OUT_NGDO and VBUS_OUT_CTRL signals should map to OUT_NFET.

- VBUS_OUT_NDGO should be connected to Source pin of OUT_NFET.
- VBUS_OUT_NGDO should be connected to VBUS pin of the Type-C connector for source only operation.
- VBUS_OUT_NGDO should be connected to VBUS_C pin for source only operation.
- VBUS_OUT_NGDO should be connected to load circuit for sink only operation.
- VBUS_OUT_CTRL should to be connected to gate pin of the OUT_NFET.

Schematic design requirements

- VBUS_IN_CTRL can source the maximum of current of 4 µA only.

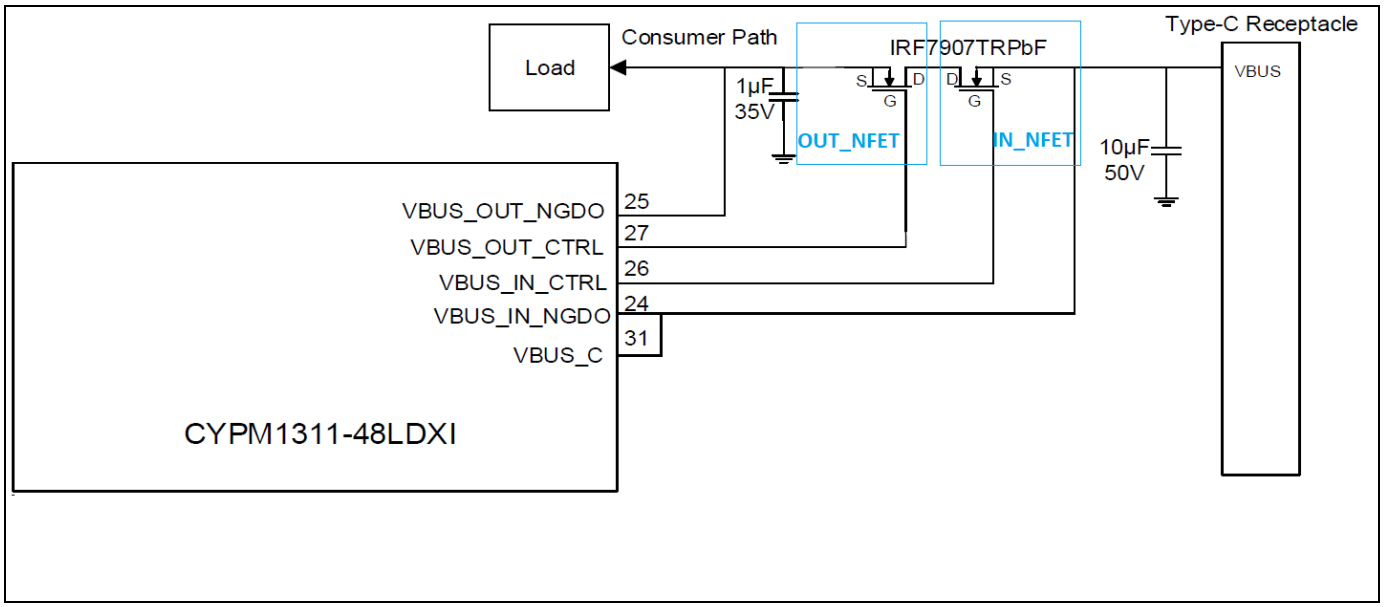

Figure 16 EZ-PD™ PMG1-S3 MCU(48-QFN) external NFET control (sink-only operation)

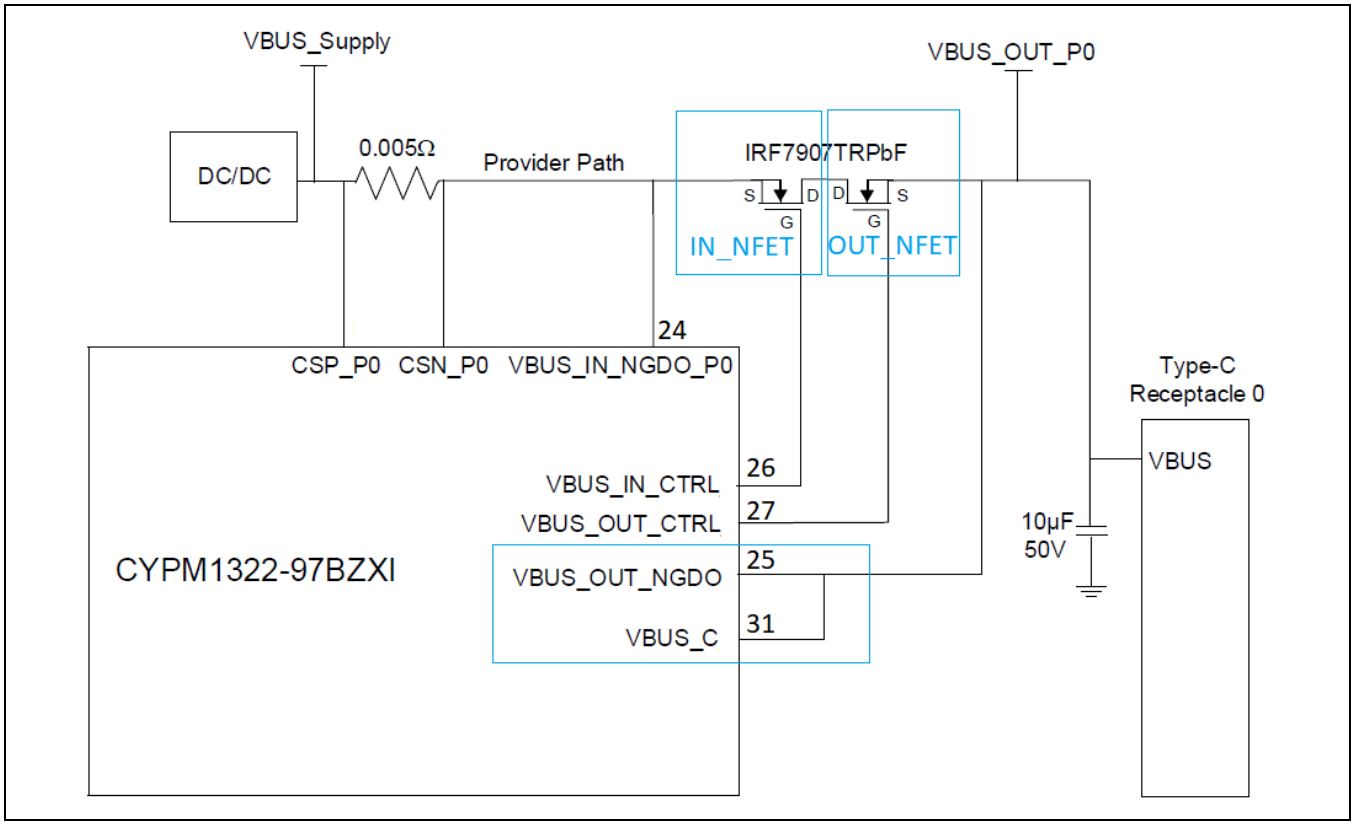

Figure 17 EZ-PD™ PMG1-S3 MCU (48-QFN) external NFET control (source-only operation)

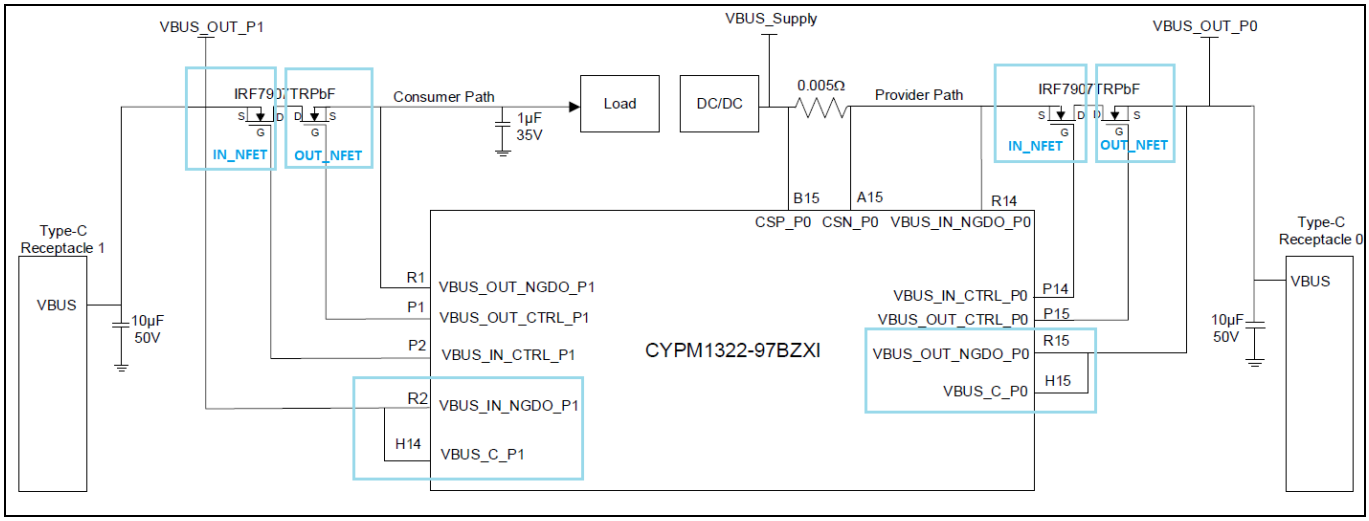

Figure 18 EZ-PD™ PMG1-S3 MCU (97-BGA) external NFET control (2-port source-only operation)

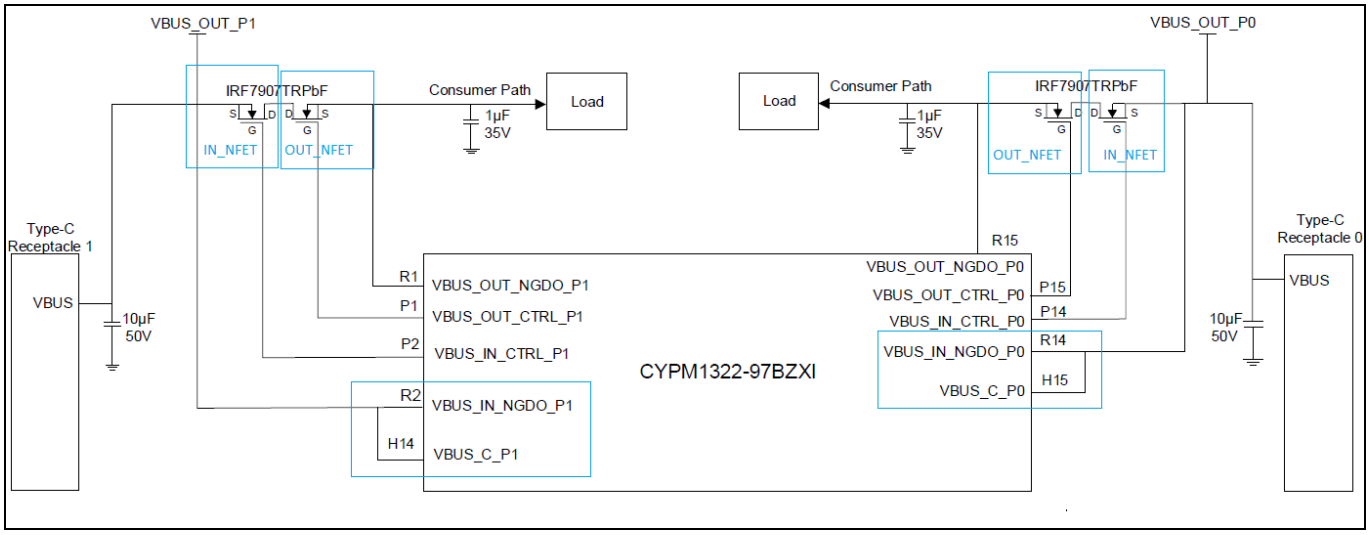

Figure 19 EZ-PD™ PMG1-S3 MCU (97-BGA) external NFET control (2-port sink-only operation)

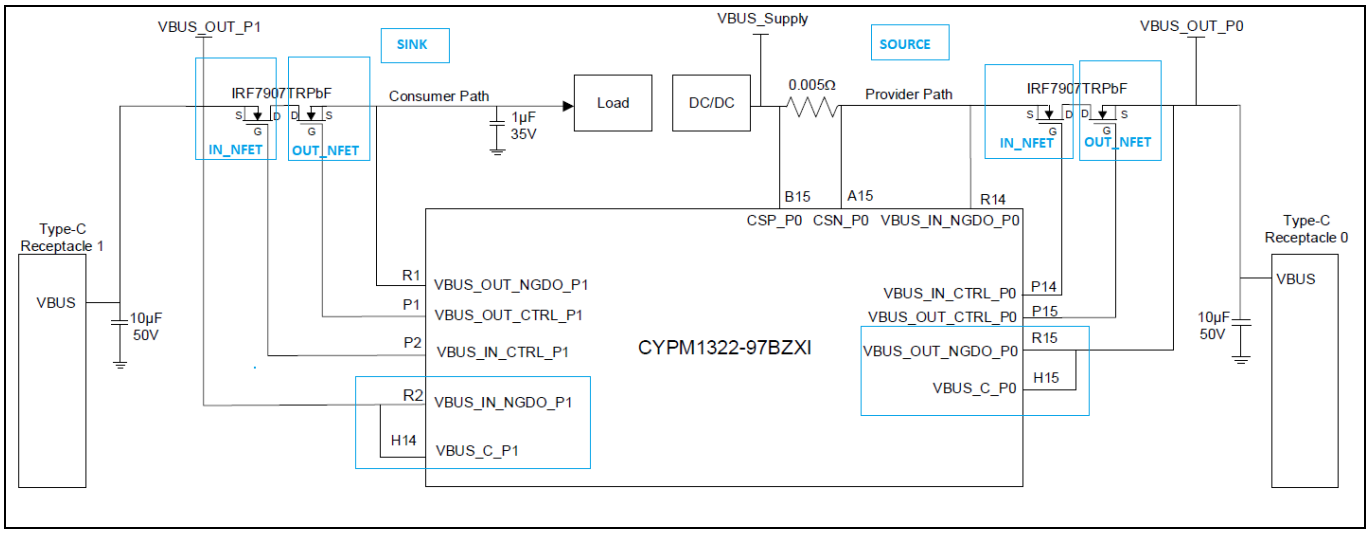

Figure 20 EZ-PD™ PMG1-S3 MCU (97-BGA) external NFET control (port 0 as source and port 1 as sink-only operation)

Schematic design requirements

EZ-PD™PMG1-S3 MCU allows to use an external load switch with a built-in gate driver. The following guidelines must be followed:

- Connect VBUS_IN_NDGO to the input pin of the load switch.
- Connect VBUS_IN_CTRL to the enable pin of the load switch through a potential divider circuit. VBUS_IN_CTRL can source the maximum current of 4 uA only. Current drawn from these resistors must be less than 4 uA; otherwise gate drive will collapse.
- Use GPIO (P2.0) to drive the external gate driver. VBUS_IN_CTRL or GPIO(P2.0) can be used to control the external gate driver and external load switch with the built-in gate driver.
- Connect VBUS_OUT_NGDO to the VBUS_C pin for source-only operation.
- Connect VBUS_OUT_NGDO to the load circuit for sink-only operation.

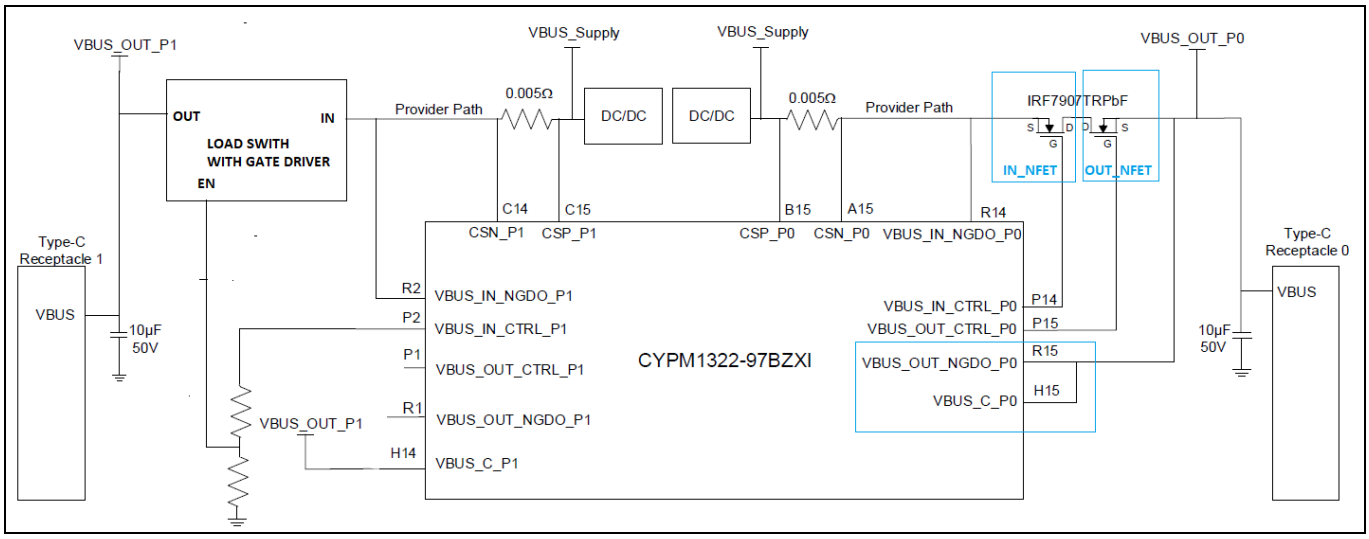

Figure 21 EZ-PD™ PMG1-S3 MCU (97-BGA) external load switch with built-in gate driver control using VBUS_IN CRTL (source-only operation)

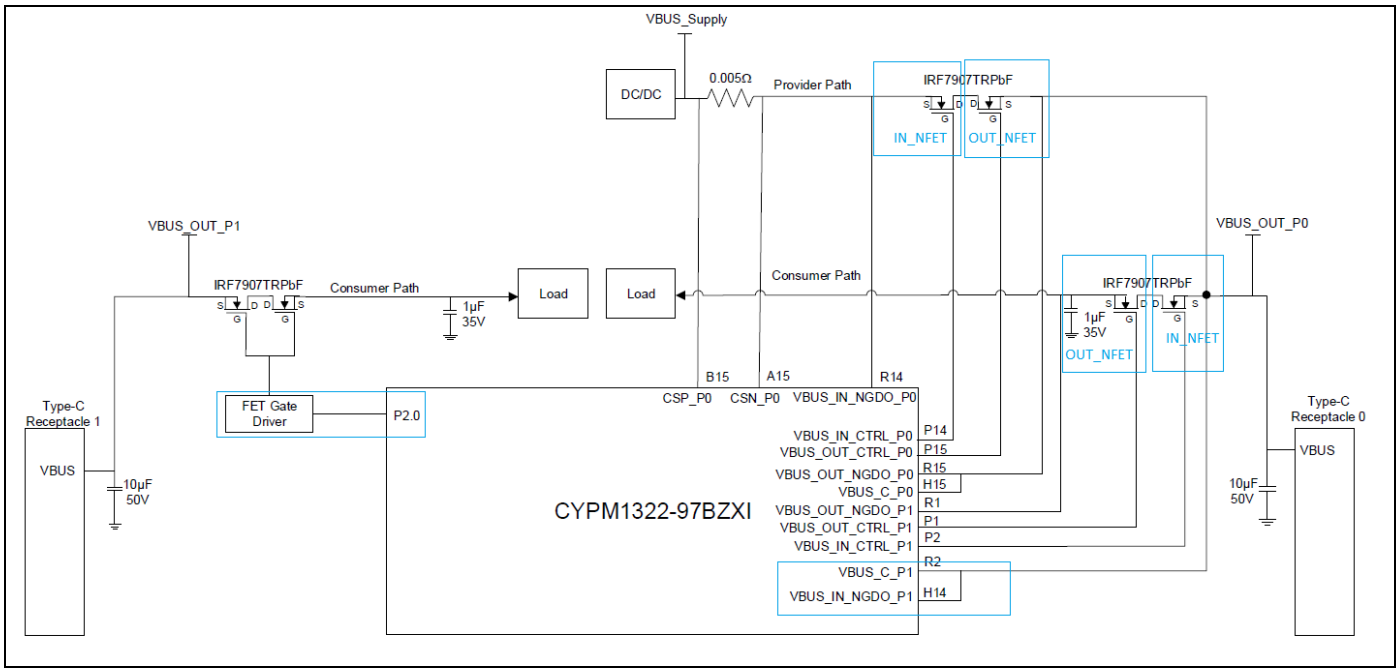

Figure 22 DRP on one port and sink operation on other port with external load switch and external gate driver control through GPIO

Table 13 lists the EZ-PD™ PMG1 MCU pins assigned to the gate driver/load switch control.

Table 13 Load switch/gate driver signals

Load switch control signal	MCU pin #	Description
EZ-PD™ PMG1-S0 MCU		
VBUS_FET_CTRL_0	3	External PMOS FET (PFET) control (30-V Tolerant) with internal pull-up 0: Path ON 1: Path OFF
VBUS_FET_CTRL_1	4	External PFET Control (30-V Tolerant) 0: Path ON High-Z: Path OFF To use this pin, provide external pull-up
EZ-PD™ PMG1-S1 MCU		
VBUS_P_CTRL	11	Slew Rate controlled I/O for enabling/disabling Provider side PFET 0: Path ON High Z: Path OFF
VBUS_C_CTRL	12	Pin for enabling/disabling Consumer side PFET 0: Path ON High Z: Path OFF
EZ-PD™ PMG1-S2 MCU		
VBUS_P_CTRL1	1	VBUS Gate Driver Control 1 for Provider Switch
VBUS_P_CTRL0	2	VBUS Gate Driver Control 0 for Provider Switch
VBUS_C_CTRL1	29	VBUS Gate Driver Control 1 for Consumer Switch
VBUS_C_CTRL0	30	VBUS Gate Driver Control 0 for Consumer Switch
EZ-PD™ PMG1-S3 MCU 48-QFN		
VBUS_IN_NGDO	1	Source pin of IN_FET
VBUS_IN_CTRL_NDGO	2	Gate driver Control for IN_FET
VBUS_OUT_CTRL_NGDO	29	Gate driver Control for OUT_FET
VBUS_OUT_NGDO	30	Source pin of OUT_FET
EZ-PD™ PMG1-S3 MCU 97-BGA		
VBUS_IN_NGDO_P0	1	Source pin of IN_FET for Port 0
VBUS_IN_CTRL_NDGO_P0	2	Gate driver control for IN_FET for Port 0
VBUS_OUT_CTRL_NGDO_P0	29	Gate driver control for OUT_FET for Port 0
VBUS_OUT_NGDO_P0	30	Source pin of OUT_FET for Port 0
VBUS_IN_NGDO_P1	1	Source pin of IN_FET for Port 1
VBUS_IN_CTRL_NDGO_P1	2	Gate driver control for IN_FET for Port 1
VBUS_OUT_CTRL_NGDO_P1	29	Gate driver control for OUT_FET for Port 1
VBUS_OUT_NGDO_P1	30	Source pin of OUT_FET for Port 1

4.8 Charger detection

The EZ-PD™ PMG1 MCU family integrates battery charger emulation and detection for USB BC 1.2 and Apple charge terminations. The DP and DM pins of the MCU connected to charger detect block. In PMG1-S1 device, charger detection is part of the internal HS Mux.

Following are the hardware design considerations for connecting DP and DM signals:

- In EZ-PD™ PMG1-S0 MCU, EZ-PD™ PMG1-S2 MCU, and EZ-PD™ PMG1-S3 MCU, short the A6 and B6 (DP) of the Type-C connector and route to the USBDP pin of the MCU. Short A7 and B7 (DM) and route to the USBDM pin of the MCU (**Figure 23**).
- In EZ-PD™ PMG1-S1 MCU, do not short the pins. Route the Type-C connector pins directly to the High-Speed (HS) pins of the MCU (**Figure 24**).
- Follow the USB HS signal routing consideration explained in Power domain for optimum performance.

Table 14 lists the pin number for USB HS/Charger detection signals on EZ-PD™ PMG1 MCUs.

Table 14 USB HS/Charger detection signals

HS Signal	MCU Pin#				
	EZ-PD™ PMG1-S0 MCU	EZ-PD™ PMG1-S1 MCU	EZ-PD™ PMG1-S2 MCU	EZ-PD™ PMG1-S3 MCU (48-QFN)	EZ-PD™ PMG1-S3 (97-BGA)
USBDP	17	N/A	21	39	A13
USBDM	16	N/A	22	40	A11
USBDP_TOP	N/A	28	N/A	N/A	N/A
USBDP_BOT	N/A	26	N/A	N/A	N/A
USBDM_TOP	N/A	27	N/A	N/A	N/A
USBDM_BOT	N/A	25	N/A	N/A	N/A

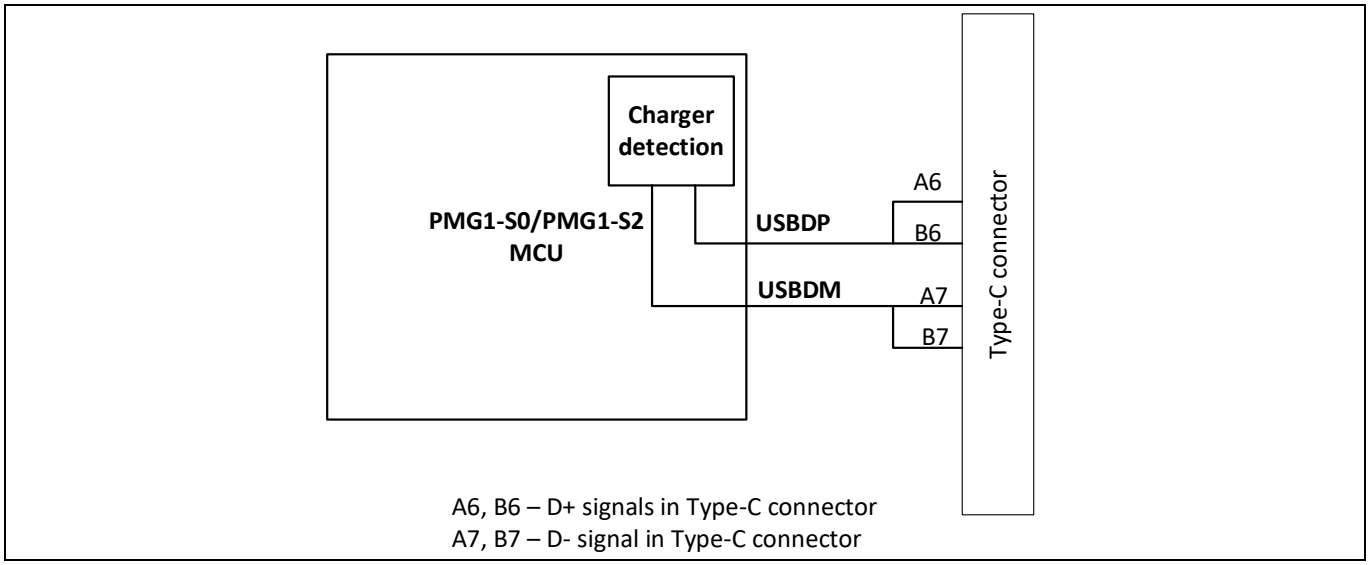

Figure 23 Charger detection in EZ-PD™ PMG1-S0 MCU, EZ-PD™ PMG1-S2 MCU, and EZ-PD™ PMG1-S3 MCU

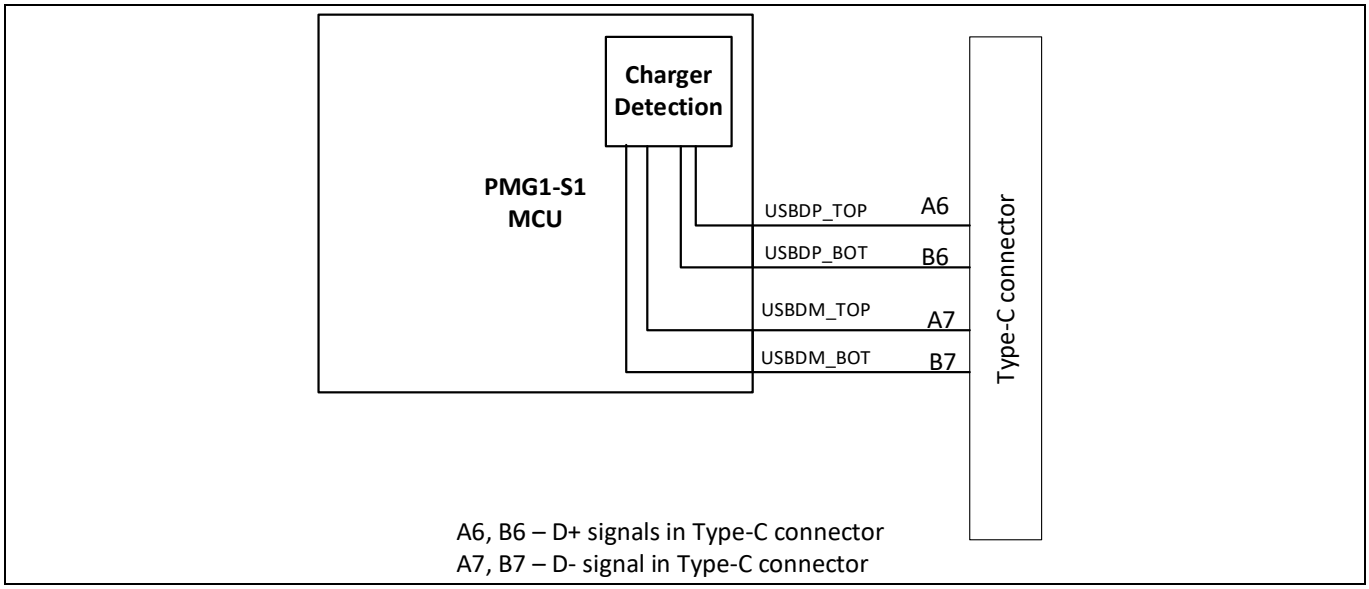

Figure 24 Charger detection in EZ-PD™ PMG1-S1 MCU

5 Electrical design consideration

5.1 ESD and EMI/EMC protection

EZ-PD™ PMG1 MCUs have built-in ESD protection on VBUS, OVT pin, and USB/USB PD lines. **Table 15** summarizes the built-in ESD protection of MCUs.

Table 15 Built-in ESD protection for EZ-PD™ PMG1 MCU

MCU	EZ-PD™ PMG1-S0 MCU	EZ-PD™ PMG1-S1 MCU	EZ-PD™ PMG1-S2 MCU	EZ-PD™ PMG1-S3 MCU (48-QFN and 97-BGA)
Contact Discharge	±8 kV on CC1, CC2, VBUS, P2.2, and P2.3 pins	No	±8 kV on CC1, CC2, VBUS, USBDP, USBDM, SBU1, and SBU2 pins	No
Air Discharge	±15 kV on CC1, CC2, VBUS, P2.2, and P2.3 pins	No	±15 kV on CC1, CC2, VBUS, USBDP, USBDM, SBU1, and SBU2 pins	No
HBM	± 2.2 kV	±2.2 kV	± 2.2 kV	± 2.2 kV
CDM	± 500 V	± 500 V	± 500 V	± 500 V

The guidelines recommend adding ESD diodes on USB signals and CC lines for extended protection beyond the rated limits. The ESD diodes meet the requirements of IEC61000-4-2, and low input capacitance. Ferrite beads are not mandatory for all Type-C applications using EZ-PD™ PMG1 MCU, but it is recommended to connect the beads between the Type-C connector's shield and the system GND pin.

5.2 General PCB layout tips

There are many classic techniques for designing PCBs for low noise and EMC. This section explains some of these general techniques. These techniques can be used to improve the overall design of the system, EMI/EMC performance, noise handling, and so on:

- **Multiple layers:** Although they are more expensive, it is best to use a multi-layer PCB with separate layers dedicated to the VSS and VDD supplies. This provides good decoupling and shielding effects. Separate fills on these layers should be provided for GND, VDDIO, VSYS, VBUS, and VDDD.

  To reduce cost, a two-layer or even a single-layer PCB can be used. In that case, you must have a good layout for all and power and ground trace. But for designing USB PD systems, two-layer PCBs are not recommended, since the system has to handle a maximum power of 100 W.
- **Ground and power supply:** There should be a single point for gathering all ground returns. Avoid ground loops, or minimize their surface area. All component-free surfaces of the PCB should be filled with additional grounding to create a shield, especially when using two-layer or single-layer PCBs.

  The power supply should be close to the ground line to minimize the area of the supply loop. The supply loop can act as an antenna and can be a major emitter or receiver of EMI.
- **Decoupling:** The standard decoupling circuit for external power is a 100-µF capacitor. Supplementary 0.1-µF capacitors should be placed as close as possible to the VSS and VDD pins of the device to reduce high-frequency power supply ripple.

  Generally, you should decouple all sensitive or noisy signals to improve the EMC performance. Decoupling can be both capacitive and inductive.
- **Component position:** Separate the circuits on the PCB according to their EMI contribution. This will help reduce cross-coupling on the PCB. For example, separate noisy high-current circuits, low-voltage circuits,

and digital components. The decoupling capacitors and the inductor (Buck Inductor) should be placed as close as possible to the device pins with minimum trace resistance.

- **Signal routing**: When designing an application, the following areas should be closely studied to improve the EMC performance:
  - Noisy signals, for example, signals with fast edge times
  - Sensitive and high-impedance signals
  - Signals that capture events, such as interrupts and strobe signals

  To improve the EMC performance, keep the trace lengths as short as possible and isolate the traces with VSS traces. To avoid crosstalk, do not route them near to or parallel to other noisy and sensitive traces.

5.3 PCB Selection and basic routing considerations

The PCB copper thickness should be 2oz minimum to handle a maximum current of 5 A.

5.3.1 Reference PCB stackup for EZ-PD™ PMG1 MCU designs

5.3.1.1 1.2 mm, four-layer PCB stackup

Figure 25 shows the recommended stackup for a 1.2-mm thick PCB. The values of width (W) and spacing (S) are based on CY7110 EZ-PD™ PMG1-S0 prototyping kit.

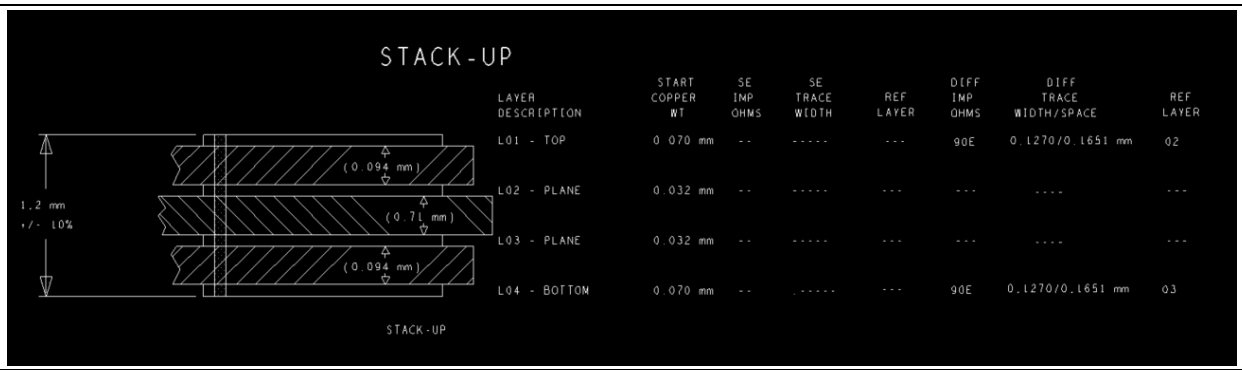

Figure 25 4-layer PCB stackup

5.3.1.2 1.2-mm, 6-layer PCB stackup

Figure 26 shows the recommended stackup for a 1.2-mm thick PCB. The values of width (W) and spacing (S) are based on CY7110 EZ-PD™ PMG1-S0 MCU prototyping kit.

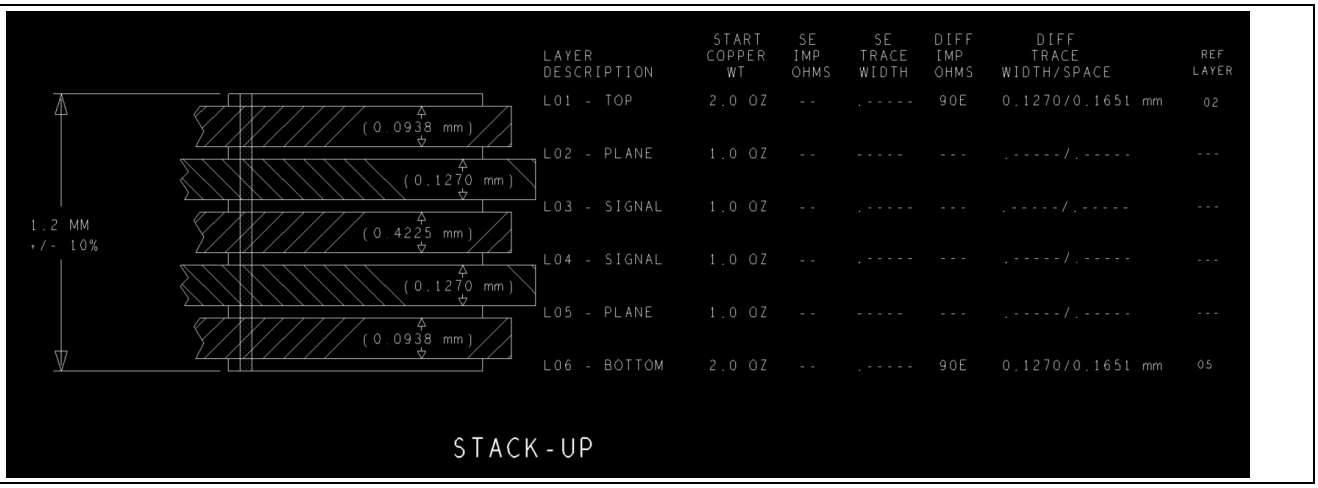

Figure 26 6-layer PCB stackup

5.4 Power domain

5.4.1 Placement of bulk and decoupling capacitors

- Place decoupling capacitors close to the power pins of the respective PMG controller for high- and low-frequency noise filtering as shown in **Figure 27**.
- Place the bulk capacitor, which acts as a local power supply, close to the power supply input and output headers and voltage regulators. Filter power inputs and outputs near the power headers to reduce the electrical noise. Ceramic or tantalum capacitors are recommended; electrolytic capacitors are not suitable for bulk capacitance.

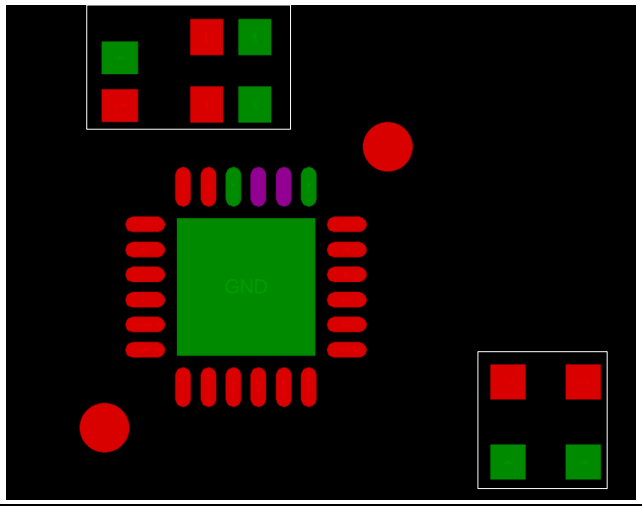

Figure 27 Placement of bulk and decoupling capacitors

5.4.2 Placement of power and ground planes

- There should be a single point for gathering all ground returns. Avoid ground loops, or minimize their surface area. All component-free surfaces of the PCB should be filled with additional grounding to create a shield, especially when using two-layer or single-layer PCBs.
- For design of system with USB PD functionality, use a high-performance substrate material for PCBs. According to the USB PD specification, the system may carry current up to 5 A. Thus, it is required to

construct PCBs with 2-ounce (oz) copper thickness. Minimum recommended space between copper elements is 8 mil (0.203 mm).

- Use dedicated planes for power and ground. Use of dedicated planes reduces jitter on USB signals and helps minimize the susceptibility to EMI and RFI.
- Use cutouts on the power plane if more than one voltage is required on the board. **Figure 28** shows the cutouts on power plane, and various power domains are marked in different colors.

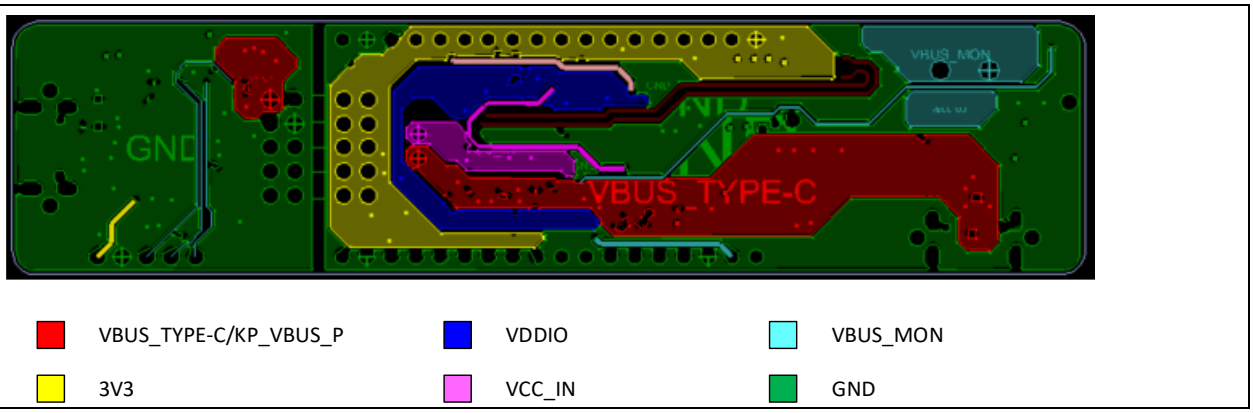

Figure 28 Power plane (Reference: EZ-PD™ PMG1-S1 MCU kit)

- Place the power plane near the ground plane for good planar capacitance. Planar capacitance that exists between the planes acts as a distributed decoupling capacitor for high-frequency noise filtering, thereby reducing the electromagnetic radiation.

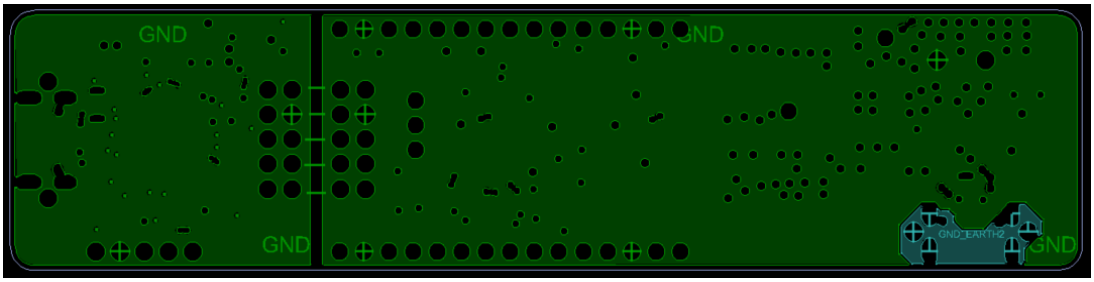

Figure 29 Ground plane (Reference: EZ-PD™ PMG1-S1 MCU kit)

- Do not split or cut the ground plane. Splitting it increases the electrical noise and jitter on USB signals. Ground planes should be continuous. A discontinuous ground plane leads to larger inductance due to longer return current paths, which can increase EMI radiation. Also, multiple split grounds can cause increased crosstalk.

5.4.3 Power domain routing

- Route the power traces with a minimum of 40 mils trace width to reduce inductance.
- Keep the power traces short.
- Use larger vias (at least 30-mil pad, 15-mil hole) on power traces.
- Make the power trace width the same as that of the power pad. To connect power pins to the power plane, keep the vias very close to the power pads. This helps in minimizing the stray inductance and IR drop on the line.
- Solder the Exposed PAD (EPAN) of PMG1 MCUs onto an exposed ground pad provided in the PCB.

- If a switched-mode power supply is used, make sure that the power traces are far away from signal traces to avoid addition of power noise on signal or keep ground traces in between the signal traces.

5.4.4 Voltage regulation

Consider the following points while selecting voltage regulators/LDO to reduce electrical emissions and prevent regulation problems during USB suspend:

- Select voltage regulators that have minimum load current that is less than the board's load current during USB suspend. If the current drawn on the regulator is less than the regulator's minimum load current, then the output voltage may change.
- Place voltage regulators so that they straddle split VCC planes; this reduces emissions.

5.5 Routing of USB PD and USB-Data signals (Type-C)

5.5.1 Guidelines for routing Type-C (VBUS, GND, and CC) lines

- Group the VBUS pins together (all VBUS pins are brought out to the same plane using vias).
- Similarly, group the GND pins together (all GND pins are brought out to the same plane using vias).
- Place GND plane adjacent and below CC (CC1, CC2) lines. Traces from CC pins must be routed with a minimum of 20 mils trace width for VCONN operation.
- Route the signals as differential pair to the external Rsense resistor.

5.5.2 Guidelines for routing USB data lines

- Match the High-Speed (DP and DM) signal trace lengths within 1.25 mm (50 mils) in EZ-PD™ PMG1 MCUs.
- In EZ-PD™ PMG1-S1 MCU, where USB High-Speed signals are routed through internal mux, ensure that the High-Speed signals are less than 3-inches (75 mm) between MCU and Type-C connector. Also, Htrace length, between the MCU and host connector, is less than three inches.
- Ensure that the differential pairs (USBDP, USBDM, USBDP_TOP, USBDP_BOT, USBDM_TOP, USBDM_BOT, USBDP_SYS and USBDM_SYS) have a minimum pair-to-pair separation of 0.5 mm.
- Minimize the use of vias.
- Select a grounded coplanar waveguide (CPWG) system as a transmission line method.
- Adjust the High-Speed signal trace lengths near the USB receptacle, if necessary.
- On USB signal lines, use as few bends as possible. Do not use a 90-degree bend. Use 45-degree or rounded (curved) bends if necessary (see **Figure 30**).

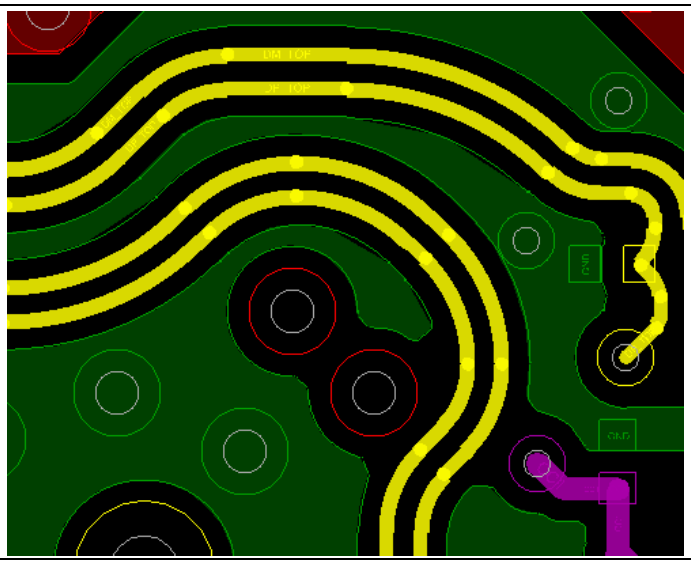

Figure 30 USB High-Speed signal routing - rounded bends

5.5.3 EZ_PD™ PMG1-S3 MCU 97-BGA and 48QFN layout guidelines

Figure 30 shows the PMG1-S3 97-BGA device footprint that is recommended. The footprint has oval-shaped pads in specific locations. It is recommended to use oval pads in order to reduce the manufacturing cost by eliminating a high-density interconnector (HDI) board processing. This method allows the PCB designer to route the inner perimeter balls through the top layer. This footprint is recommended for MDI (medium density) PCB designs that are generally less expensive to build.

You should ensure that the outer ball size is be 0.25 mm x 0.1778 mm and the inner ball size is 0.25 mm x 0.25 mm. EZ-PD™ PMG1-S3 MCU BGA package supports via size of 10 x 18 mils.

Perform differential routing for current sense pins.

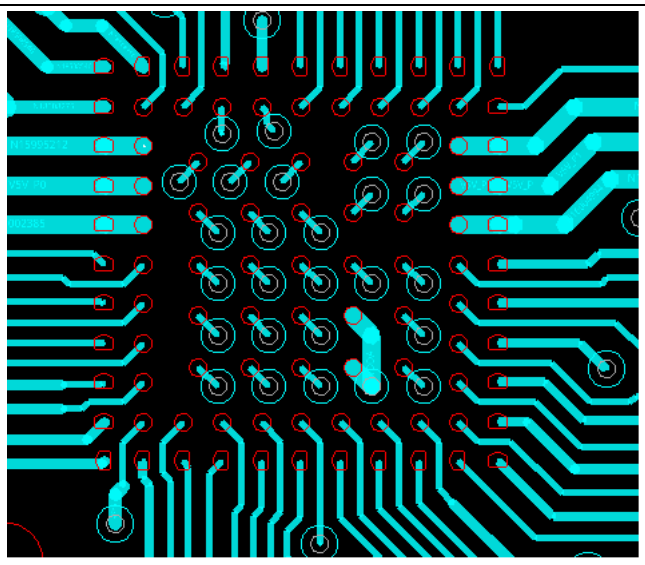

Figure 31 EZ-PD™ PMG1-S3 MCU 97-BGA fanout and via size (10x18)

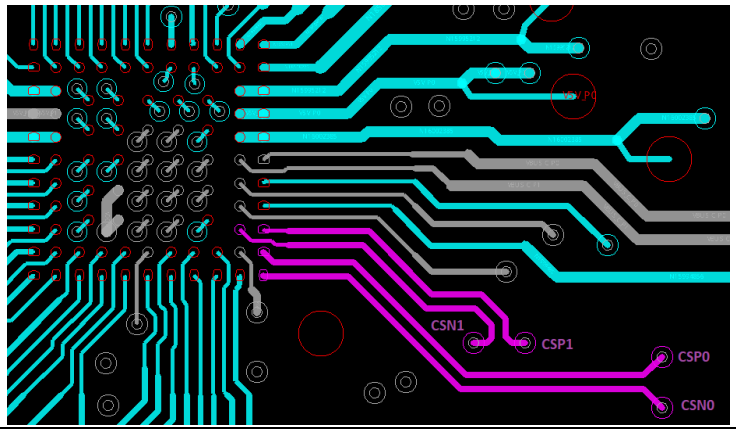

Figure 32 EZ-PD™ PMG1-S3 MCU 97-BGA current sense routing: Top side

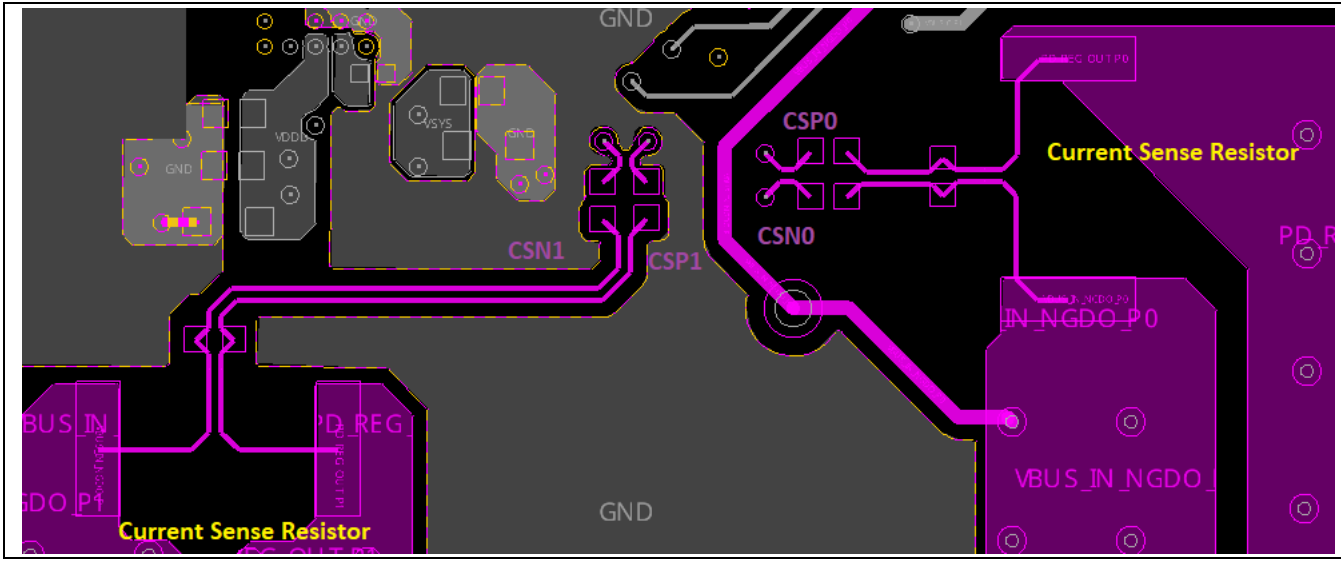

Figure 33 EZ-PD™ PMG1-S3 MCU 97-BGA current sense routing: Top side

As shown in **Figure 34**, the EZ-PD™ PMG1-S3 MCU 48-QFN device has a 5 × 5 via array (25 vias) on the thermal pads. It is recommended to have a 4 × 4 via array (16 vias) on the thermal pads to meet the thermal performance. Via array means the number of vias present on the rows and columns of the EPAD. Each via size should be minimum of 10-mil drill and 20-mil diameter.

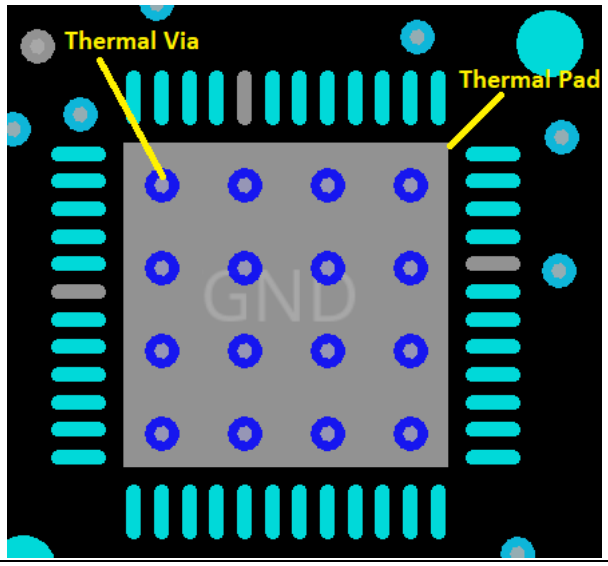

Figure 34 EZ-PD™ PMG1-S3 MCU 48-QFN thermal via

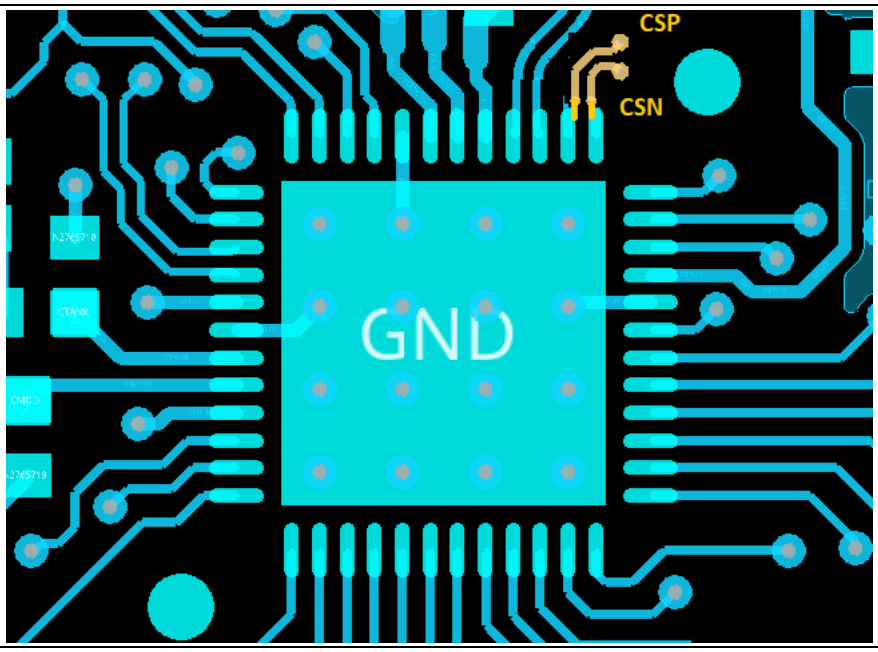

Figure 35 EZ-PD™ PMG1-S3 MCU 40-QFN fanout and current sensing: Top side

As shown in **Figure 36**, the EZ-PD™ PMG1-S3 MCU 48-QFN device has a 5 × 5 via array (25 vias) on the thermal pads. It is recommended to have a 4 × 4 via array (16 vias) on the thermal pads to meet the thermal performance. Via array means the number of vias present on the rows and columns of the EPAD. Each Via size should be minimum of 10-mil drill and 20-mil diameter.

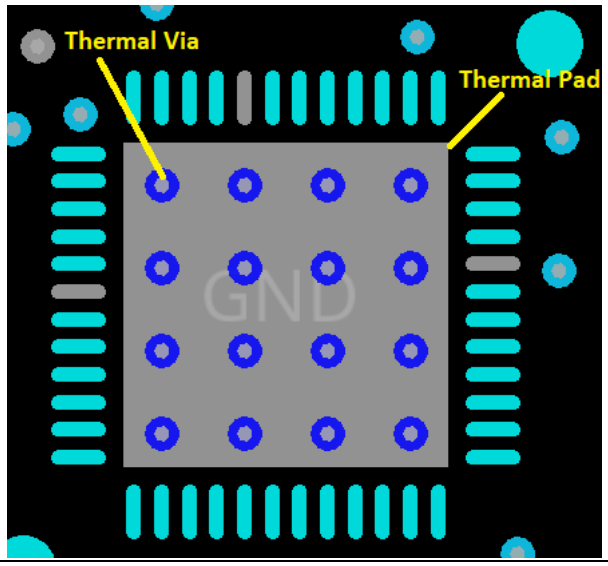

Figure 36 EZ-PD™ PMG1-S3 MCU 48-QFN thermal via

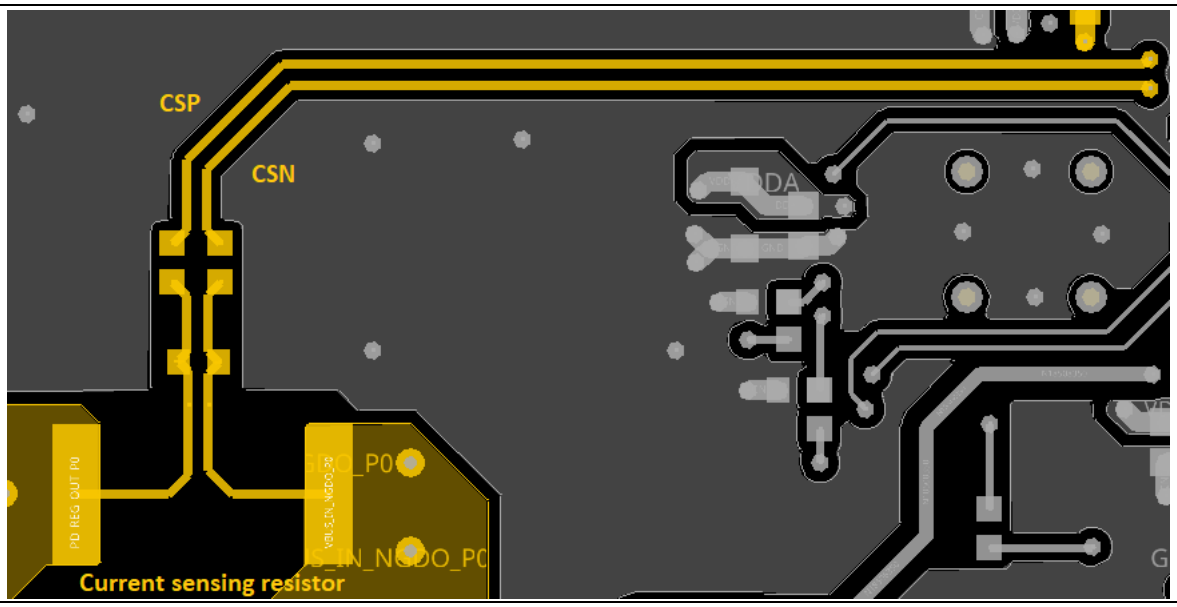

Figure 37 EZ-PD™ PMG1-S3 MCU 48-QFN current sensing: Bottom side

5.5.4 EZ-PD™ PMG1-S3 MCU 97 BGA/48 QFN CAPSENSE™ (CSD) pin assignment and layout guidelines

MCU pins are multiplexed with many functions like SCB, UART, SPI, TCPWM, and CAPSENSE™.

Table 6 lists the MCU pins which support CAPSENSE™. These pins must not be multiplexed with other functions during CAPSENSE™ operation. They can be multiplexed with other functions when CAPSENSE™ operation is Not in use. Use 0E resistor to isolate CAPSENSE™ and non-CAPSENSE™ operations.

See **AN85951** for CAPSENSE™ guidelines.

Table 16 EZ-PD™ PMG1-S3 MCU 97-BGA CSD pin assignment

Pin number	EZ-PD™ PMG1-S3 MCU 97-BGA pin name	CAPSENSE™ (CSD) support with other functions
A1	P3.0	GPIO, SCB4, CSD
A2	P2.0	GPIO, SCB5, CSD
A3	P2.2	GPIO, SCB5, CSD
A3	P2.2	GPIO, SCB5, CSD
A5	P2.5	GPIO, SCB5, CSD
A7	P2.4	GPIO, SCB0, CSD
A8	P2.7	GPIO, SCB1, CSD
B1	P3.3	GPIO, SCB4, CSD
B2	P2.1	GPIO, SCB0, CSD
B3	P3.1	GPIO, CSD
B5	P2.3	GPIO, SCB5, CSD
B7	P2.1	GPIO, SCB1, CSD
C1	P3.7	GPIO, CSD
D4	P3.4	GPIO, CSD
E1	P5.1	GPIO, SCB2, CSD (CMOD)
E2	P3.6	GPIO, SCB4, CSD
F4	P3.5	GPIO, SCB4, CSD
K12	P1.6	GPIO, SCB1, CSD
H2	P1.0	GPIO, CSD
H4	P5.5	GPIO, CSD
H6	P5.2	GPIO, CSD
M12	P1.5	GPIO, SCB1, CSD
C2	P3.2	GPIO, CSD
G1	P5.4	GPIO, CSD
G2	P5.0	GPIO, SCB2, CSD (CTANK)
H1	P5.3	GPIO, SCB2, CSD
P3	P1.1	GPIO, SCB3, CSD, Serial Wire Debug Clock
R3	P1.2	GPIO, SCB3, CSD, Serial Wire Debug Data
K4	P1.3	CSD, I2C_INT_TBT_P0
R5	P6.0	GPIO, SCB6, CSD
P5	P6.1	GPIO, SCB6, CSD
R8	P0.0	CSD, LXRX_P1
R7	P0.1	CSD, LXTX_P1
P7	P0.2	CSD, DGB1_P1
K6	P0.2	CSD, DGB2_P1
P8	P0.4	CSD, DGB2_P0

Pin number	EZ-PD™ PMG1-S3 MCU 97-BGA pin name	CAPSENSE™ (CSD) support with other functions
M8	P0.5	CSD, DGB1_P0
R9	P0.6	CSD, LXTX_P0
R11	P0.7	CSD, LXRX_P0
P13	P6.2	CSD, SBU2_P0
R13	P6.3	CSD, SBU1_P0
M10	P1.4	CSD, GPIO
M12	P1.5	GPIO, SCB1, CSD
K12	P1.6	GPIO, SCB1, CSD
G15	P7.0	GPIO, SCB1, CSD
G14	P7.0	GPIO, CSD
E15	P4.0	GPIO, SCB0, CSD
D12	P4.1	GPIO, SCB0, CSD
A14	P7.2	GPIO, CSD
B13	P7.3	GPIO, SCB7, CSD
B11	P7.4	GPIO, SCB7, CSD
A9	P7.5	GPIO, SCB7, CSD
B9	P7.6	GPIO, SCB7, CSD

Table 17 EZ-PD™ PMG1-S3 MCU 48 QFN CSD pin assignment

Pin number	EZ-PD™ PMG1-S3 MCU48 QFN pin name	CAPSENSE™ (CSD) support with other functions
1	P3.0	GPIO, SCB4, CSD
2	P3.3	GPIO, SCB4, CSD
3	P3.5	GPIO, SCB4, CSD
4	P3.6	GPIO, SCB4, CSD
7	P5.0	GPIO, SCB2, CSD
8	P5.1	GPIO, SCB2, CSD (CMOD)
9	P5.2	GPIO, SCB2, CSD
10	P5.3	GPIO, SCB2, CSD
11	P5.5	GPIO, CSD
12	P1.1	GPIO, SCB3, CSD, Serial Wire Debug Clock
13	P1.2	GPIO, SCB3, CSD, Serial Wire Debug Data
14	P1.3	GPIO, SCB3, CSD
15	P6.0	GPIO, SCB6, CSD
16	P6.1	GPIO, SCB6, CSD

Pin number	EZ-PD™ PMG1-S3 MCU48 QFN pin name	CAPSENSE™ (CSD) support with other functions
17	P0.0	GPIO, CSD
18	P6.2	GPIO, SCB6, CSD
19	P6.3	GPIO, SCB6, CSD
20	P1.4	GPIO, SCB3, CSD
21	P1.5	GPIO, SCB1, CSD
22	P1.6	GPIO, SCB1, CSD
34	P4.0	GPIO, SCB0, CSD
35	P4.1	GPIO, SCB0, CSD
45	P2.4	GPIO, SCB0, CSD
46	P2.3	GPIO, SCB5, CSD
47	P2.2	GPIO, SCB5, CSD
48	P2.1	GPIO, SCB0, CSD

6 Schematics and layout review checklist

Table 18 Schematics and layout review checklist

No.	Schematic checklist	Answer (Yes/No/NA)
1	Are the decoupling capacitors and bulk capacitors connected on power supplies and CC pins as shown in **Figure 7** and **Figure 10**?	
2	Are the I^2C lines provided with pull-up resistors (2.2 KΩ)? Is the GPIO for I2C interrupt pin the same in both bootloader and application firmware?	
3	Do the POR RC components meet the required reset times?	
4	Are the I^2C lines provided with pull-up resistors to the 3.3-V domain?	
5	Is the recommended arrangement of FETs present on VBUS to control power provider and consumer path as shown in **Figure 14**, **Figure 15**, and **Figure 23**?	
6	Are all USB connector shields terminated properly?	
7	Is the VBUS discharge circuitry present in the design as shown in **Figure 23** for EZ-PD™ PMG1-S2 MCU?	
8	Are the VBUS discharge resistors rated for 2-W of power dissipation for EZ-PD™ PMG1-S2 MCU?	
9	Are the EZ-PD™ PMG1-S3 MCU Gate driver pins are signed properly for sink and source application?	
10	Are the CAPSENSE™ signals are multiplexed with some function pins? If yes, Is the isolation resistor (0E) present?	
Layout checklist		
1	Are the decoupling capacitors and bulk capacitors placed close to the Type-C PD controller power pins?	
2	Is a 0.1-µF decoupling capacitor placed close to VCCD pin?	
3	Are the vias placed close to the Type-C PD controller power pins?	
4	Are the power traces routed away from the HS and Super-Speed (SS) data lines?	
5	Is the capacitor in the RC reset circuitry placed close to the reset pin of the Type-C PD controller?	
6	Has a dedicated and continuous GND plane been used?	
7	Are all VBUS pins on the Type-C connector brought on the same plane using vias?	
8	Are all GND pins on the Type-C connector brought on the same plane using vias?	
9	Is GND present adjacent to and below CC lines?	
10	Do the USB SS and HS signal lines match in length?	
11	Are the USB SS and HS signal lines provided with a solid ground plane underneath?	
12	Are the USB traces kept short?	

Schematics and layout review checklist

No.	Schematic checklist	Answer (Yes/No/NA)
13	Do the USB traces have minimum bends and no 90-degree bends?	
14	Are the SS and HS signal trace impedance matched 90E?	
15	Are the PMG1-S3 current sense pins routed as differential signals?	
16	Are the CAPSENSE™ signals follow the **AN85951** layout guidelines?	

References

[1] Overview: **Infineon USB PD Controller Roadmap**

[2] Product Webpage:

- **EZ-PD™ PMG1 MCU webpage**

[3] Kit webpages

- **CY7110 EZ-PD™ PMG1-S0 prototyping kit**
- **CY7111 EZ-PD™ PMG1-S1 prototyping kit**
- **CY7112 EZ-PD™ PMG1-S1 prototyping kit**
- **CY7113 EZ-PD™ PMG1-S3 prototyping kit**

[4] Datasheets

- **EZ-PD™ PMG1-S0 MCU datasheet**
- **EZ-PD™ PMG1-S1 MCU datasheet**
- **EZ-PD™ PMG1-S2 MCU datasheet**
- **EZ-PD™ PMG1-S3 MCU datasheet**

[5] Application note: **AN232553 - Getting started with EZ-PD™ PMG1 MCU on ModusToolbox™ software**

Acronyms and abbreviations

Acronyms	Expansion
AC	Apple Charging
ADC	Analog-to-Digital Converter
Arm®	Advance RISC machine, a CPU architecture
BC	Battery Charging
CC	Configuration Channel
CDM	Charged Device Model
CPU	Central Processing Unit
CS	Current Sense
CSN	Current Sense Negative
CSP	Current Sense Positive
CYP	Cypress Programmer
DFP	Downstream Facing Port
DRP	Dual Role Port
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
FS	Full-Speed
GPIO	General Purpose Input/ Output
HBM	Human Body Model
HS	High-Speed
IC	Integrated Circuit
IDE	Integrated Development Environment
I^2C	Inter-Integrated Circuit, a communication protocol
I/O	Input/Output
LDO	Low Dropout Regulator
MCU	Microcontroller Unit
NC	No Connect
OCP	Over Current Protection
OVP	Over Voltage Protection
PCB	Printed Circuit Board
PD	Power Delivery
POR	Power-On-Reset
PWM	Pulse-Width Modulator
QFN	Quad-Flat No-lead, a type of IC packaging
RCP	Reverse Current Protection
R_D	Pull-down resistor on the USB Type-C CC wire used to indicate that the Port is a Sink

Acronyms and abbreviations

Acronyms	Expansion
R_{D-DB}	Pull-down resistor on the USB Type-C CC wire used to indicate that the Port is a dead battery sink
R_P	Pull-up resistor on the USB Type-C CC wire used to indicate that the Port is a Source
RX	Receiver
SAR	Successive Approximation Register
SCB	Serial Communication Block
SCL	I2C Serial Clock
SCP	Short Circuit Protection
SDA	I2C Serial Data
SPI	Serial Peripheral Interface, a communication protocol
SRAM	Static Random Access Memory
SWD	Serial Wire Debug
TCPWM	Timer/Counter Pulse-Width Modulator
TX	Transmit
Type-C	Latest USB connector and cable standard
UART	Universal Asynchronous Transmitter Receiver, a communication protocol
USB	Universal Serial Bus
USB-PD/ USB PD	USB Power Delivery
USB-FS	USB Full-Speed
UVP	Under Voltage Protection
XRES	External Reset I/O pin

Revision history

Document version	Date of release	Description of changes
**	2021-03-15	Initial release
*A	2021-07-30	Added hardware design guidelines for EZ-PD™ PMG1-S3 MCU parts

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