Low output voltage configuration for fast COT POLs

About this document

Scope and purpose

This application note summarizes the application approaches for deriving the output voltage of a DC-DC buck converter that is less than the internal reference voltage of the converter using fast constant on-time (COT) architecture.

Intended audience

Customers, field application engineers and application engineers who design power conversion circuits with fast COT point-of-load products (POLs).

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1 Introduction

Among Infineon's POL product families, the proprietary fast COT is the most popular loop control. It achieves fast load transient as conventional COT control does, and at the same time, it maintains high DC accuracy in V_{OUT} as voltage mode and current mode control do. A quick introduction to fast COT control is available on Infineon's website [1].

This application note demonstrates a unique way of generating output voltage that is less than the reference voltage of the standard buck converter – one which has good efficiency, line regulation, load regulation, output ripple and stability, which are the essential performance parameters of a buck converter.

This document details the procedure for designing the circuit, and capturing the test results of the designed circuit. The procedure can be applied to the family of POLs.

The design example uses the IR3889 regulator [2] to demonstrate the design procedure. The **IR3889** is an easy-to-use, fully integrated DC-DC buck regulator. The onboard pulse-width modulation (PWM) controller and OptiMOS™ FETs with integrated bootstrap diode make IR3889 a small-footprint solution, providing highly efficient power delivery. Furthermore, it uses a fast COT control scheme, which simplifies the design efforts and achieves fast control response. The IR3889 is a versatile regulator, offering programmable switching frequency from 600 kHz to 2 MHz, four selectable current limits, four selectable soft-start times, forced continuous conduction mode (FCCM) and diode emulation mode (DEM) operation.

2 Design requirements

The circuit has been designed to meet the following requirements.

Table 1 Design requirements

Input voltage, V_{IN}	12 V
Output voltage, V_{OUT}	0.4 V
Output current	15 A
Switching frequency	600 kHz
Mode	FCCM

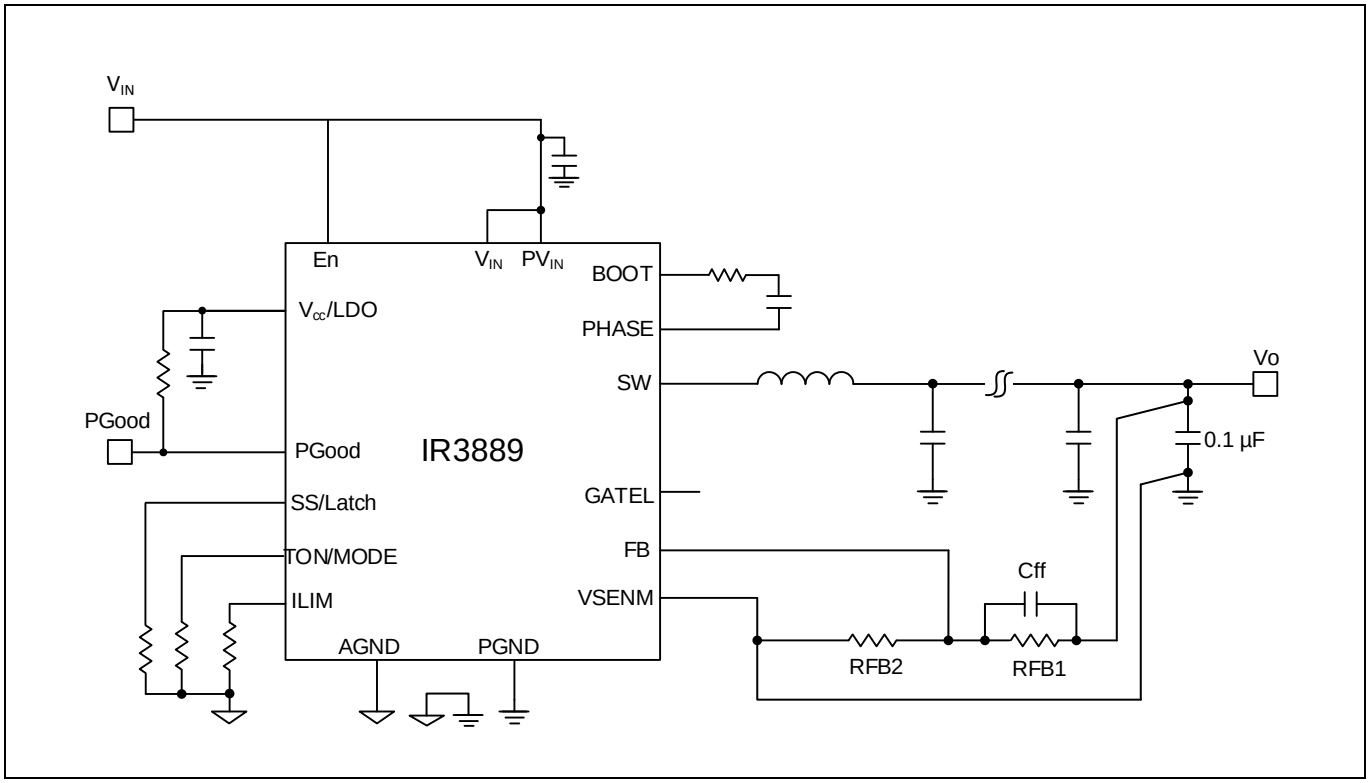

Figure 1 Typical application of IR3889

2.1 Output voltage configuration techniques

The IR3889 has an internal reference of 0.8 V. In order to design an application circuit with output voltage of 0.4 V, there are many techniques which can be used to configure an output voltage less than the reference voltage or to make the reference voltage equal to the output voltage

Method 1: One of them is to use the internal V_{CC} low dropout (LDO) supply to clamp the Zener diode and then configure RFB1 and RFB2 so that the feedback (FB) pin is 0.8 V and output is 0.4 V.

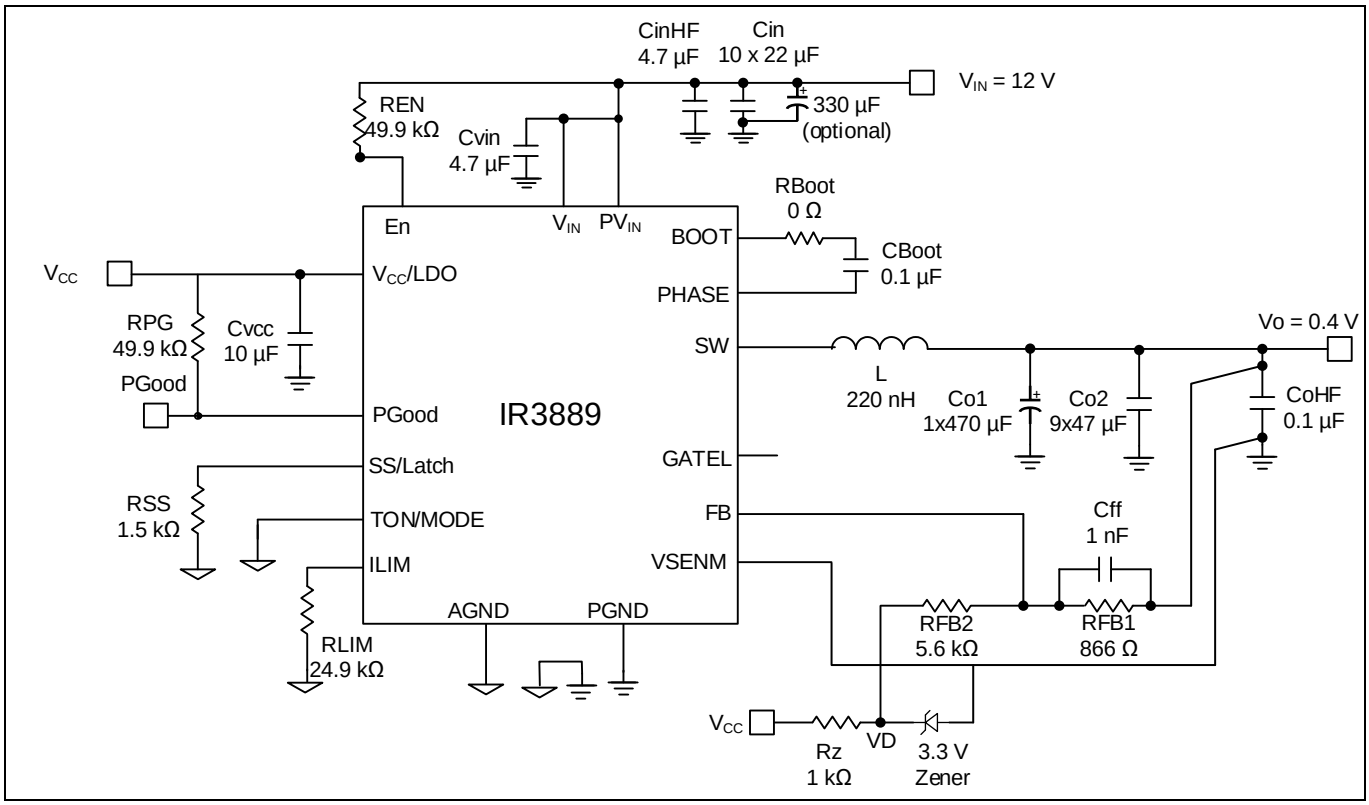

Figure 2 Configuring output using a Zener diode

Drawback: The V_{CC} has a lot of variation from 4.7 to 5.3 V, which results in inaccuracy of the output voltage.

Table 2 Accuracy of output voltage using a Zener diode

	V_{CC}	R1	R2	Vfb	Vfb1	Vfb2	V_{OUT}	Error in V_{OUT} %
PZU3.3B2L,315	3.3	5600	866	0.8	0.441973399	0.358027	0.413393	3.348
	3.25	5600	866	0.8	0.435276833	0.364723	0.421125	5.281
	3.5	5600	866	0.8	0.468759666	0.33124	0.382464	-4.384

Design requirements

Method 2: To save cost, since V_{CC}/LDO and internal LDO are already present on IR3889, we can connect a resistive divider accordingly so that the output voltage tracks the V_{CC} reduced voltage. The advantage of this method is that the reference rises linearly and so does the output.

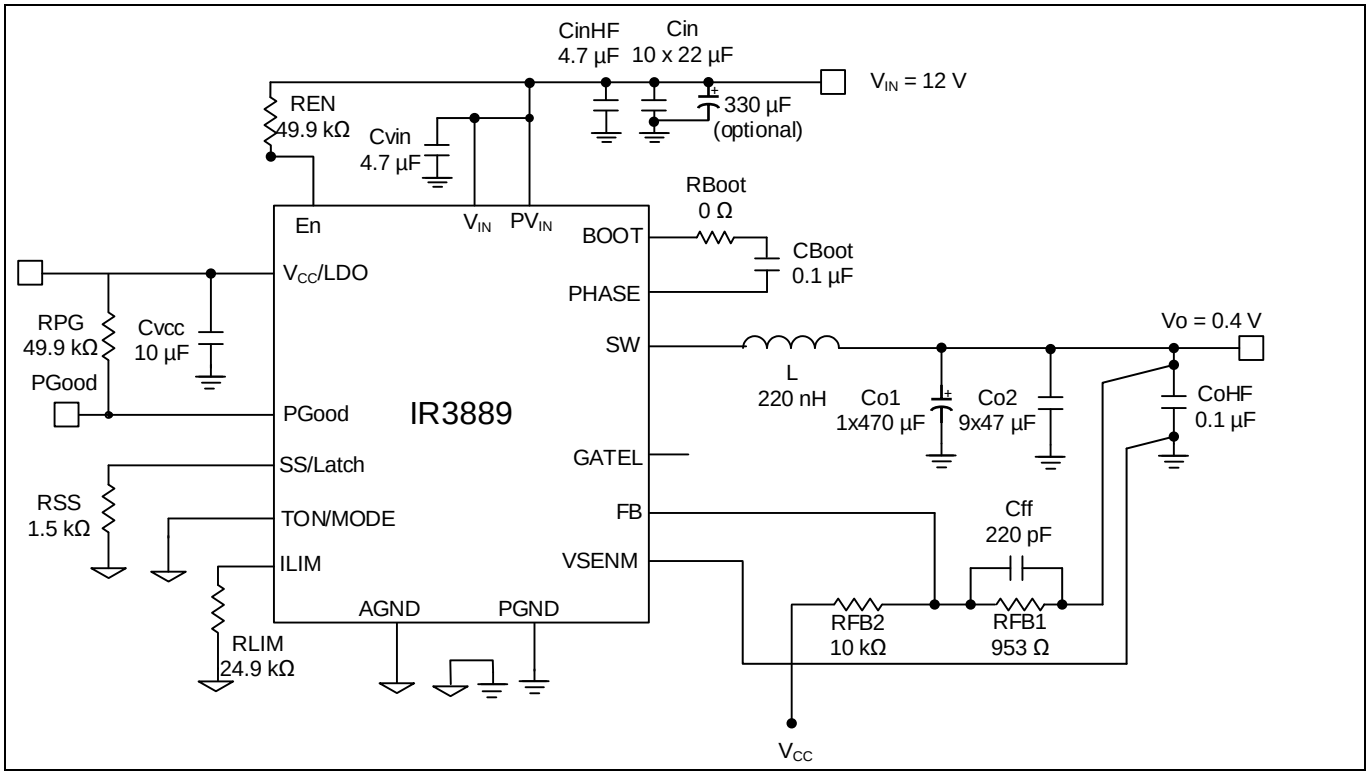

Figure 3 Configuring output using a resistive divider with internal V_{cc}

Output inaccuracy:

Table 3 Accuracy of output voltage using internal V_{cc}

	V_{CC}	R1	R2	Vfb	Vfb1	Vfb2	V_{OUT}	Error in V_{OUT} %
Using internal V_{CC}	5	10000	953	0.8	0.435040628	0.364959	0.39974	-0.065
	4.7	10000	953	0.8	0.40893819	0.391062	0.42833	7.083
	5.3	10000	953	0.8	0.461143066	0.338857	0.37115	-7.213

Both Method 1 and Method 2 are good in terms of cost-effectiveness and simplicity, but there are certain parameters to be considered, such as inacuuracy of the output voltage.

To overcome the following drawbacks, we propose a unique method where the above disadvantages are eliminated and the part works like a typical buck converter.

Design requirements

Method 3: In a buck conveter, the FB resistor network decides the output voltage of the buck converter. The FB voltage is compared to an internal reference voltage of 0.8 V. The divider ratio is set to provide 0.8 V at the FB pin when the output is at its desired value. The calculation of the FB resistor divider is shown below.

$$Vo = Vref * \left(1 + \frac{RFb1}{RFb2}\right)$$

In general the RFb2 is referenced to ground; instead of referring to ground we can refer to an another voltage so that the FB is still 0.8 V and we can achieve the reduced output voltage.

Applying superposition theorem:

$$VFb1 = Vo * \left(\frac{RFb2}{RFb1 + RFb2}\right)$$

VFb1 = voltage at FB pin due to output voltage:

$$VFb2 = Vext * \left(\frac{RFb1}{RFb1 + RFb2}\right)$$

VFb2 = voltage at FB pin due to external voltage:

$$VFb1 + VFb2 = 0.8V$$

Choosing an output voltage of 0.4 V and an external voltage of 2.5 V, RFb2 = 10k, RFb1 = 2.35k.

$$VFb1 = 0.4 * (\frac{10}{2.35 + 10}) = 0.3238$$

$$VFb2 = 2.5 * (\frac{2.35}{2.35 + 10}) = 0.4757$$

Adding VFb1 and VFb2 results in 0.8 V.

Note: The soft start configured will vary accordingly since the feedback is pre-biased.

Design requirements

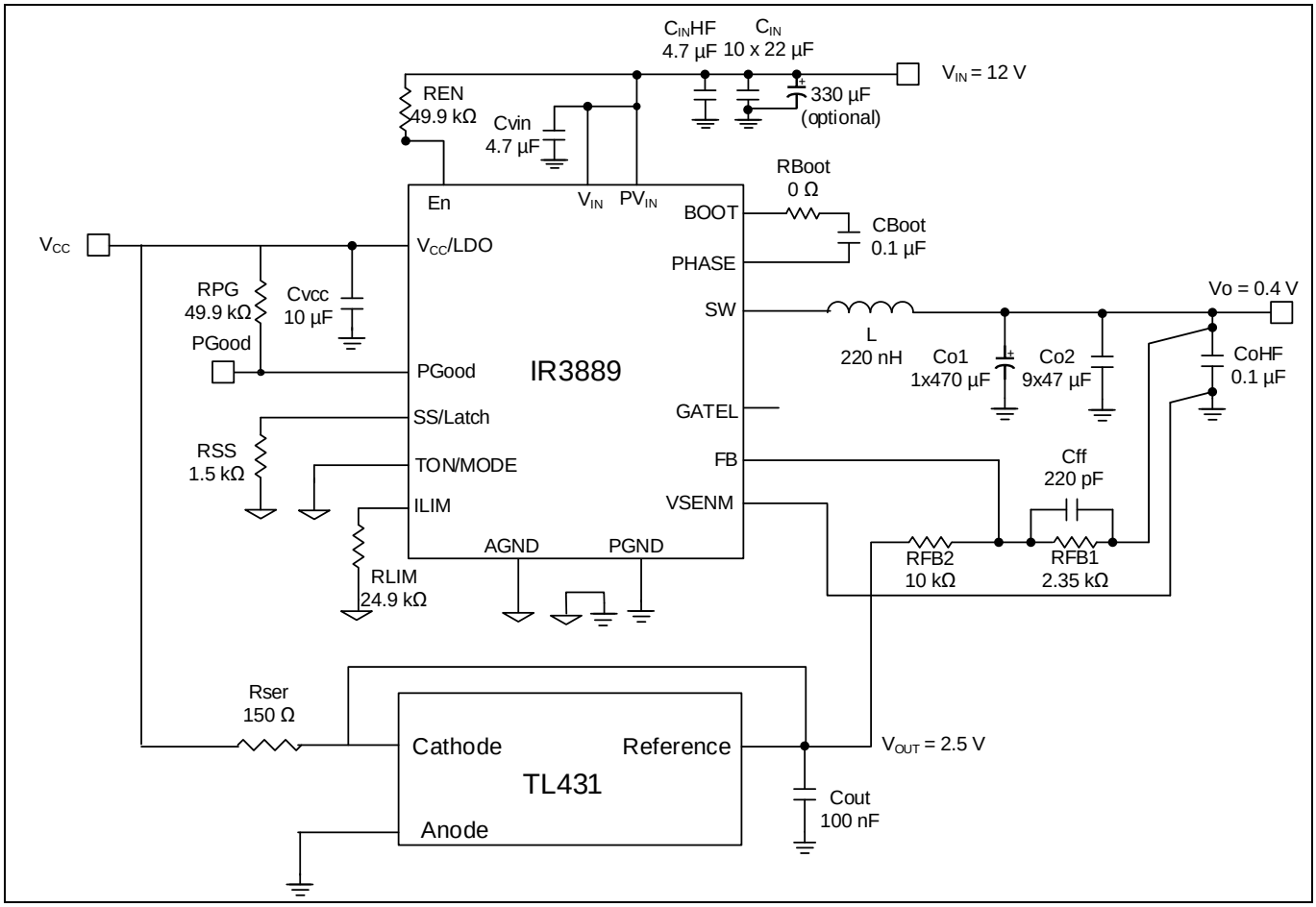

Figure 4 Suggested schematic for 0.4 V output configuration

Generating 2.5 V output: The external voltage reference can be generated by using any voltage regulators or low-noise LDOs. In this application note we have taken TL431, which can generate the stable 2.5 V output. Here, the enable pin of TL431 is tied to the the V_{IN} for ease of testing. Alternately, the enable pin of the regulator can be controlled based on the application requirements. The input of the regulator is connected to the V_{CC} LDO output of IR3889 so that the TL431 regulates 2.5 V from 3 V input supply, minimizing the losses.

Note: If using an external LDO to generate the 2.5 V and not the internal V_{CC} of IR3889, ensure that the output of the external LDO is generated and then the IR3889 is turned on so that the output increases linearly.

3 Selection of external components

3.1 Selection of inductor

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of MOSFET switching and gate charge losses. In addition to this basic trade-off, the effect of the inductor value on ripple current and low current operation must also be considered. The inductor value has a direct effect on ripple current.

The maximum average inductor current $IL_{(MAX)}$ is equal to the maximum output current. The peak current is equal to the average inductor current plus half of the inductor ripple current, ΔIL, which decreases with higher inductance or higher frequency and increases with higher V_{IN}.

$$Lo = \frac{Vout * (1 - \frac{Vout}{Vin})}{\Delta IL * Fsw}$$

$$IL(peak) = Iout + \Delta Il/2$$

3.2 Selection of output capacitor

Ordinarily, the output capacitor energy store of the regulator combined with the control loop response is prescribed to maintain the integrity of the output voltage within the dynamic (transient) tolerance specifications. The usual boundaries restricting the output capacitor in power management applications are driven by finite available PCB area, component footprint and profile, and cost. The capacitor parasitics – equivalent series resistance (ESR) and equivalent series inductance (ESL) – take greater precedence in shaping the load-transient response of the regulator as the load-step amplitude and slew rate increase. The output capacitor, C_{OUT}, filters the inductor ripple current and provides a reservoir of charge for step-load transient events. Typically, ceramic capacitors provide extremely low ESR to reduce the output voltage ripple and noise spikes, while tantalum and electrolytic capacitors provide a large bulk capacitance in a relatively compact footprint for transient loading events.

$$Cout \geq \frac{\Delta IL}{8 * Fsw * \sqrt{(\Delta Vout^2 - (RESR * \Delta IL)^2)}}$$

To meet the dynamic specification of output voltage overshoot during such a load-off transient (denoted as $\Delta V_{OVERSHOOT}$ with step reduction in output current given by ΔI_{OUT}), the output capacitance must be larger than:

$$Cout \geq \frac{Lo * \Delta Iout^2}{(Vout + \Delta Vovershoot)^2 - Vout^2}$$

The output-filter capacitor must have low enough ESR to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. When using high-capacitance, low-ESR capacitors, the filter capacitor's ESR dominates the output voltage ripple, so the output capacitor's size depends on the maximum ESR required to meet the output voltage ripple ($V_{RIPPLE(P-P)}$) specification.

3.3 Selection of input capacitors

The selection of C_{IN} is simplified by the two-phase architecture and its impact on the worst-case RMS current drawn through the input network (battery/fuse/capacitor). It can be shown that the worst-case capacitor RMS current occurs when only one controller is operating. The controller with the highest $V_{OUT} \cdot I_{OUT}$ product needs to be used in the equation below to determine the maximum RMS capacitor current requirement. Increasing the output current drawn from the other controller will actually decrease the input RMS ripple current from its maximum value. The out-of-phase technique typically reduces the input capacitor's RMS ripple current by a factor of 30 to 70 percent when compared to a single-phase power supply solution. In continuous mode, the source current of the top MOSFET is a square wave of duty-cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low-ESR capacitor sized for the maximum RMS current of one channel must be used. At maximum load current I_{MAX}, the maximum RMS capacitor current is given by:

$$Cin \geq \frac{D * (1 - D) * ILoad}{\Delta Vin(p - p) * Fsw}$$

Where:

$$D = \frac{Vout}{Vin * \eta}$$

3.4 Selection of feedforward capacitor

A small multilayer ceramic capacitor (MLCC), Cff, is preferred in parallel with the top FB resistor, RFB1, to provide extra phase boost and to improve the transient load response. The following formula can be used to help select Cff and RFB1. The value of Cff is recommended to be 100 pF or higher to minimize the impact of circuit parasitic capacitance, where L_{OUT} and C_{OUT} are the output LC filter of the buck regulator. The table lists the suggested k for some common outputs. Cff and RFB1 may be further optimized based on the transient load tests.

$$R_{FB1}C_{ff} = \frac{\sqrt{L_0 C_0}}{k \times 5.6}$$

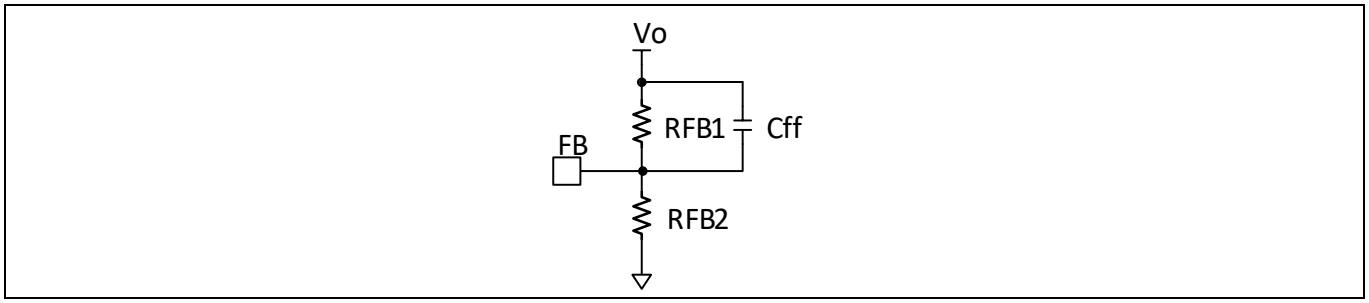

Figure 5 Output Voltage Setting

Table 4 Selection of k

V_{OUT}	k
3 V ≤ V_{OUT} ≤ 5 V	0.4
3 V < V_{OUT} < 1.2 V	0.6
V_{OUT} ≤ 1.2 V	0.8

4 Test results

4.1 Board features

V_{IN} = 12 V, V_{OUT} = 0.4 V, F_{SW} = 600 kHz, FCCM, 0 to 20 A

L = 150 nH (12.4 x 8.3 x 8 mm, DCR = 0.15 mΩ)

C_{IN} = 10 x 22 µF (25 V, ceramic 0805)

C_{OUT} = 10 x 22 µF (6.3 V, ceramic 0805) + 4 x 47 µF (6.3 V, ceramic 0805) + 1 x 470 µF (2 V, 6 mΩ, SP-cap)

4.2 Start-up

Oscilloscope:

Channel 1: Input voltage

Channel 2: Output voltage

Channel 3: SW node of IR3889

From the figure we can see that the output voltage is rising as the input rises to its set value.

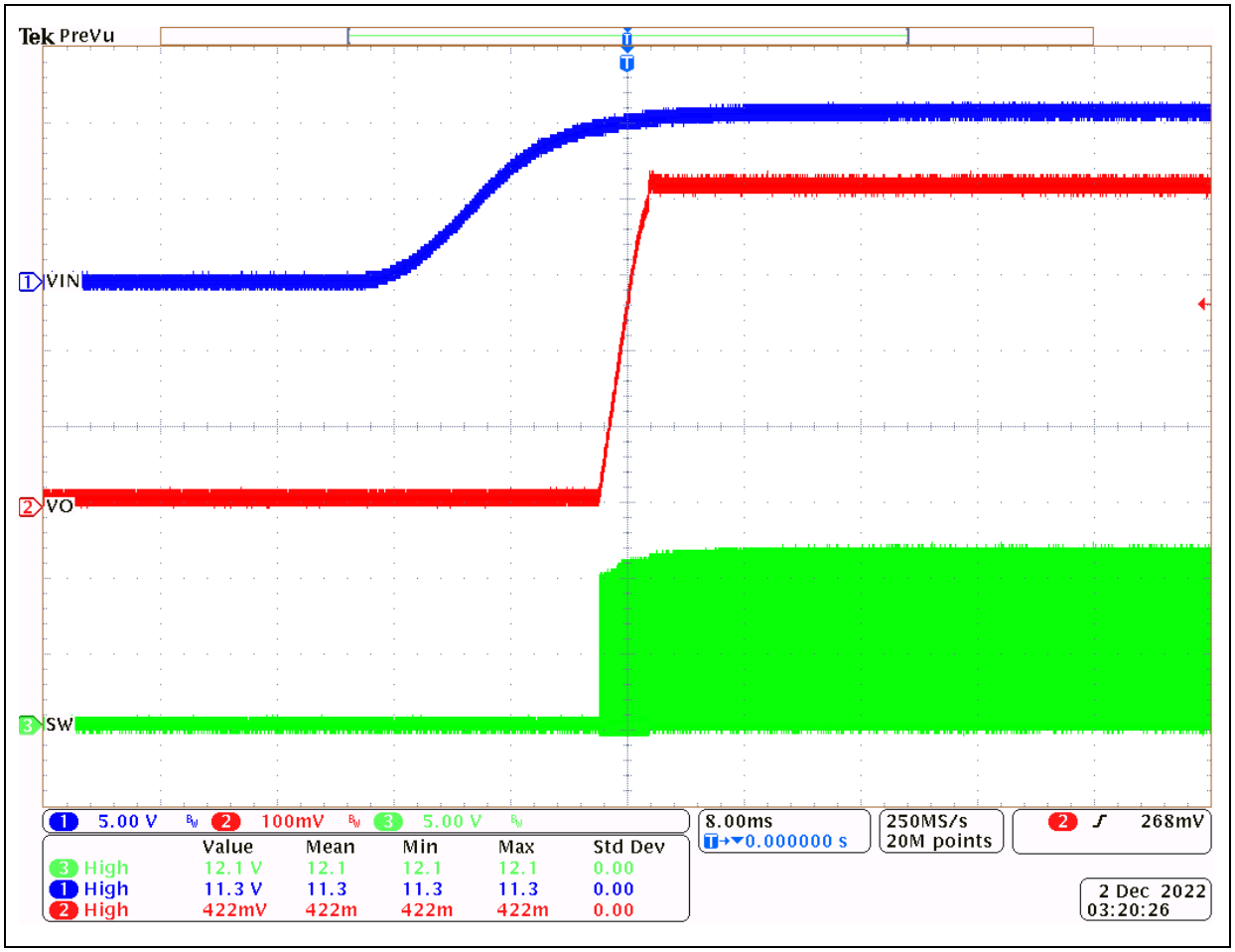

Figure 6 Start-up of IR3889 with proposed solution

Test results

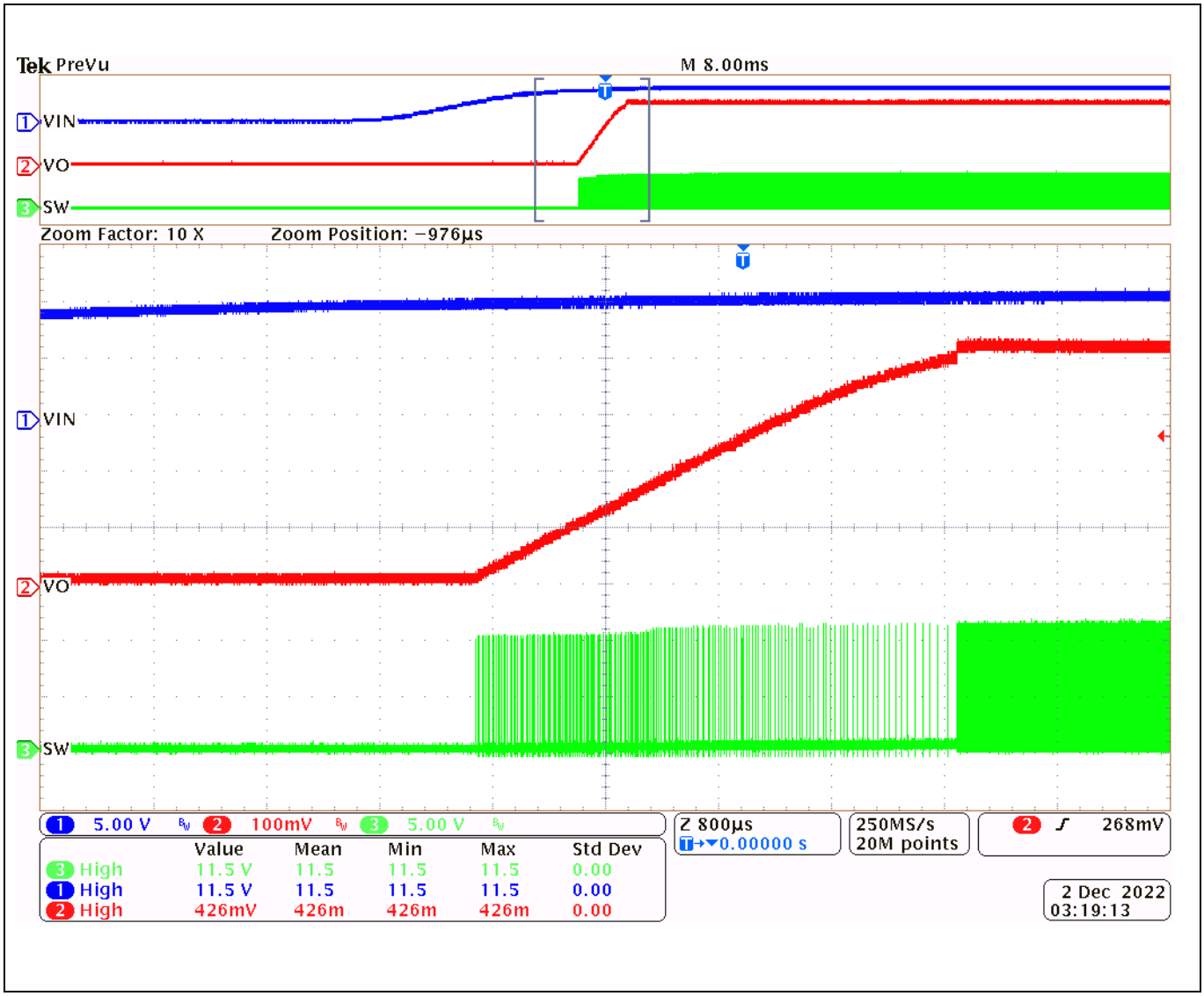

Figure 7 Switch node during start-up

The part starts in DEM as expected and goes into FCCM after the V_{OUT} is greater than 90 percent of the set value.

4.3 Shutdown

Oscilloscope:

Channel 1: Input voltage

Channel 2: Output voltage

Channel 3: SW node of IR3889

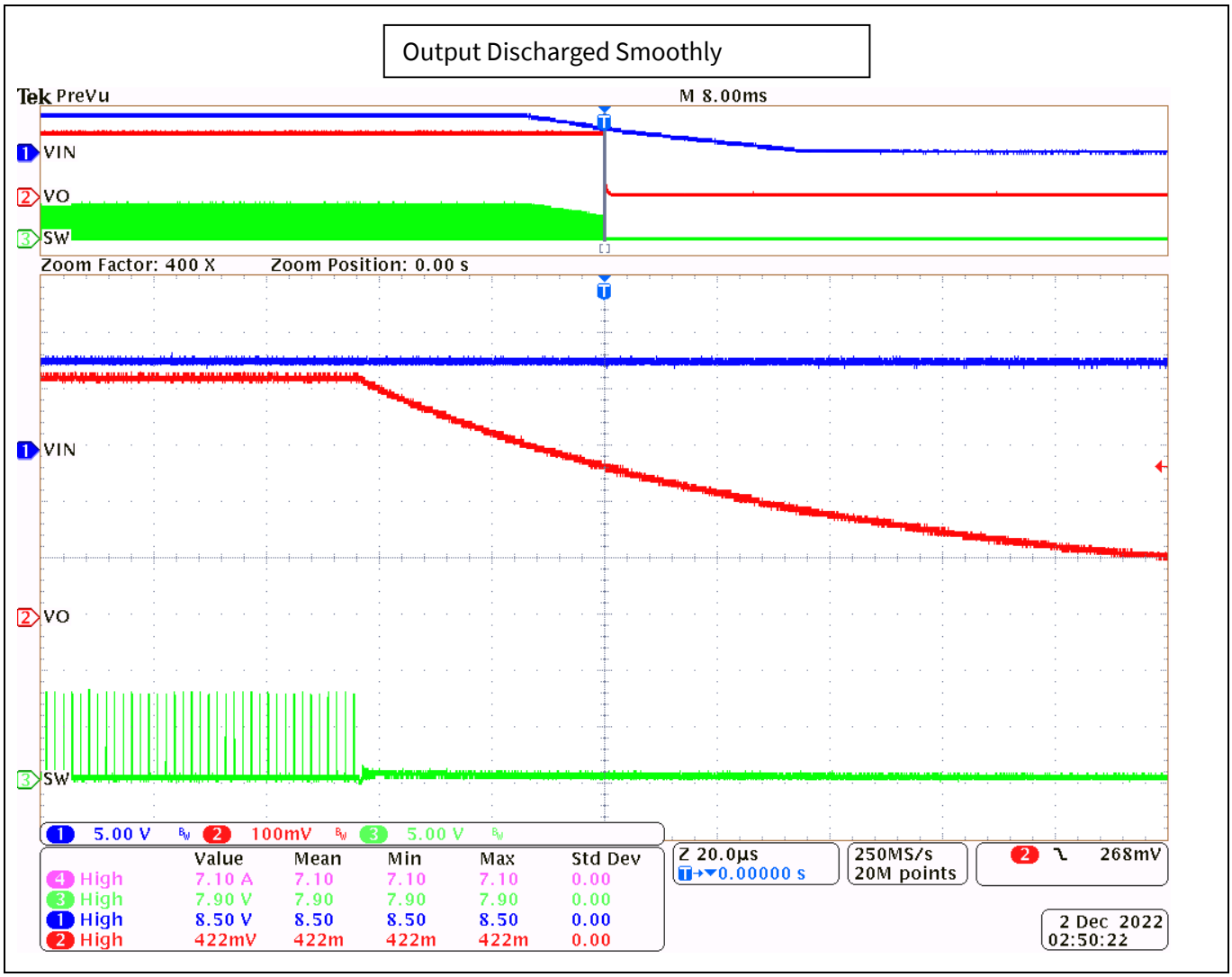

Figure 8 Shutdown of IR3889

The output discharges smoothly when the V_{IN} goes to 0 V when it is turned off.

4.4 Start-up with load

V_{IN} = 12 V, V_{OUT} = 0.4 V, F_{SW} = 600 kHz, 15 A, FCCM

Oscilloscope:

Channel 1: Input voltage

Channel 2: Output voltage

Channel 3: SW node of IR3889

Channel 4: Load current

A resistive load of 25 mΩ is connected across the V_{OUT} terminals and we can see that the current also increases linearly (shown in pink) with an increase in the output voltage as expected.

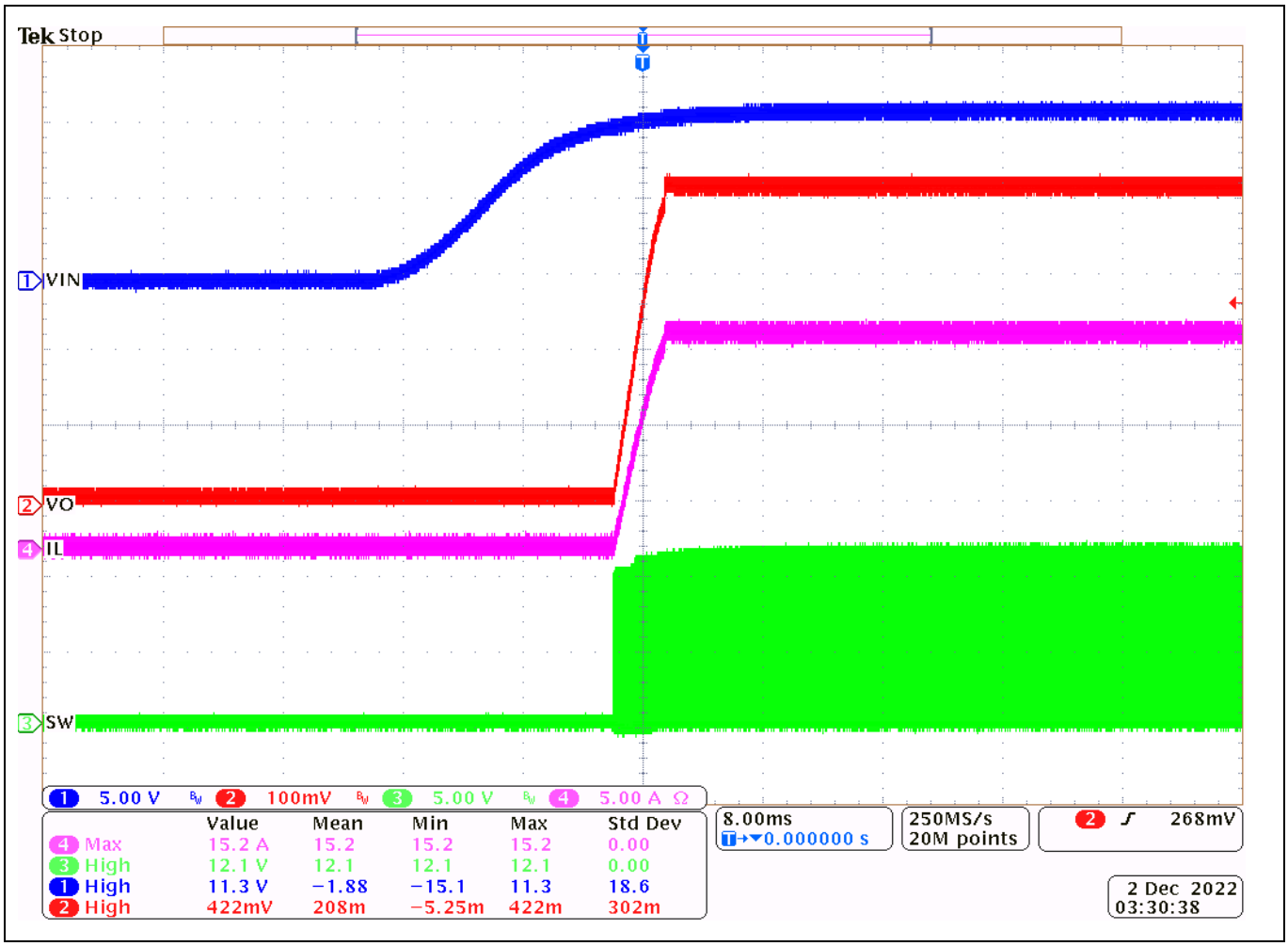

Figure 9 Start-up with load

4.5 Shutdown with load

Oscilloscope:

Channel 1: Input voltage

Channel 2: Output voltage

Channel 3: SW node of IR3889

Channel 4: Load current

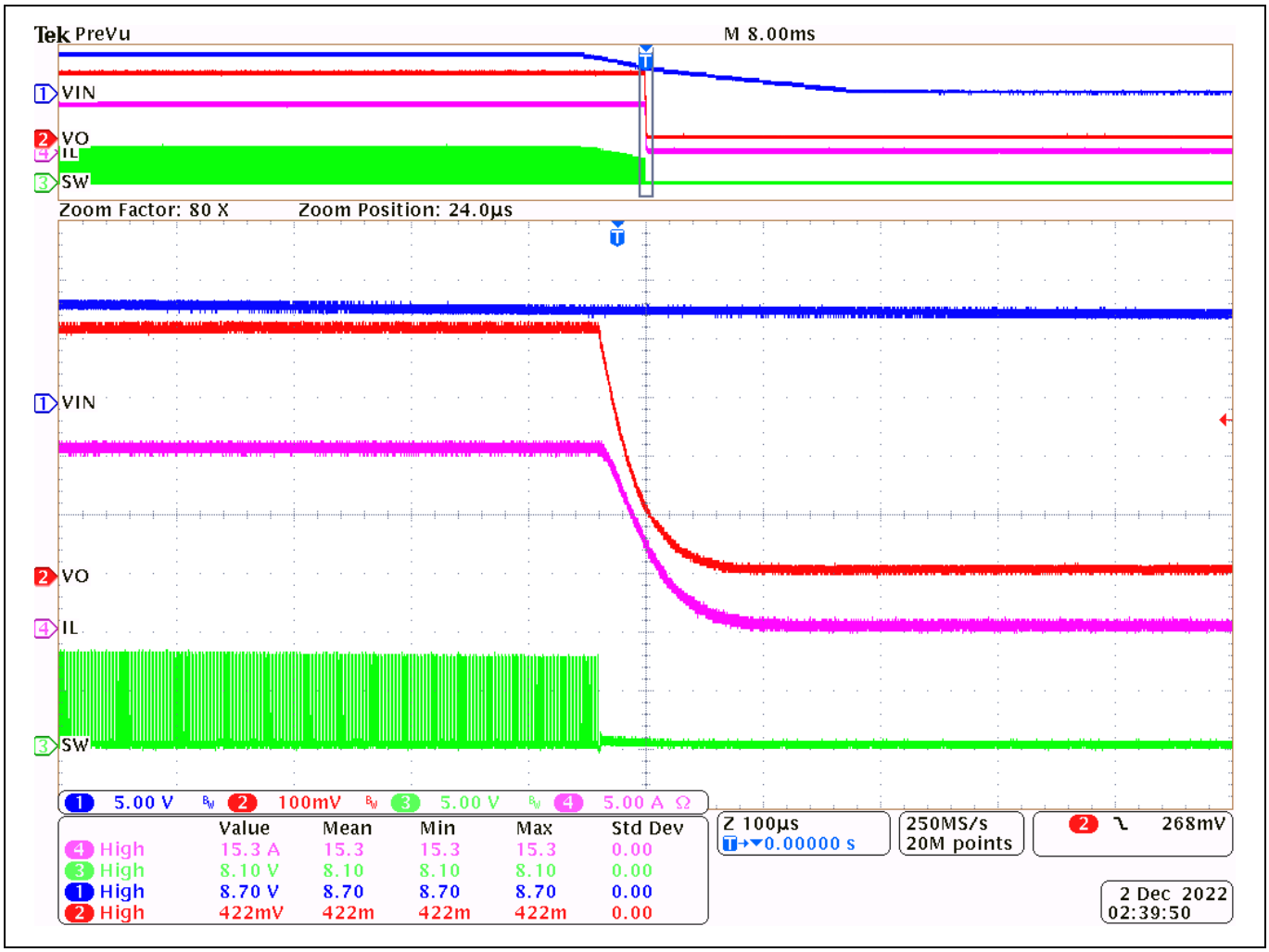

Figure 10 Shutdown with load

4.6 Transient test

Transient setup:

V_{IN} = 12 V, V_{OUT} = 0.4 V, F_{SW} = 600 kHz, 15 A, FCCM, 0 to 20 A load, 2.5 A/µs

Oscilloscope:

Channel 1: Control voltage of transient circuit

Channel 2 : Output voltage (AC mode)

Channel 4: Load current

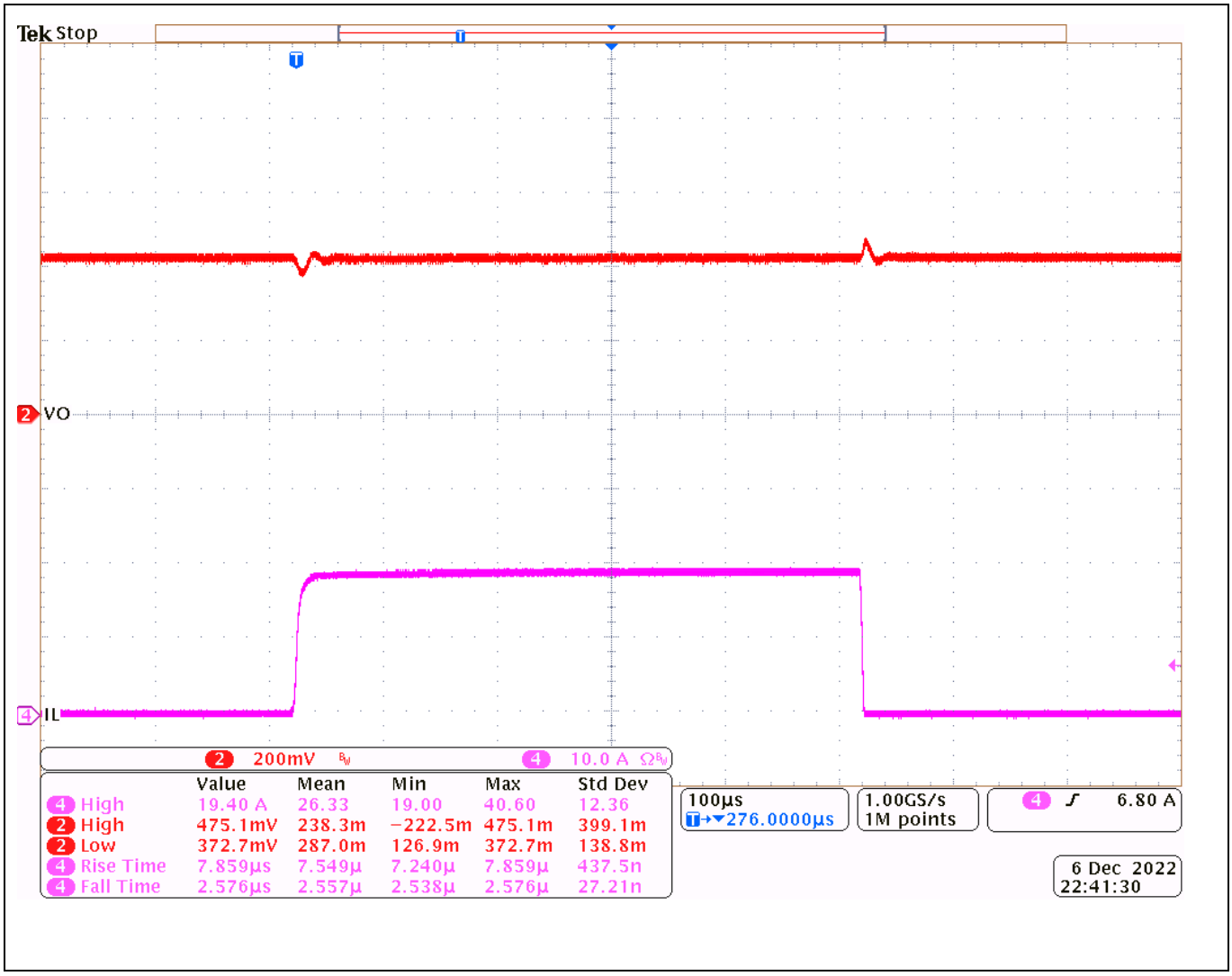

Figure 11 Transient behavior

Test results



Figure 12 Transient start-up behavior

4.7 Transient shutdown



Figure 13 Transient shutdown behavior

4.8 Ripple injection circuit

The jitter is captured for the circuit implemented, as shown in Method 3 at 8 A of load.

Conditions:
V_{IN} = 12 V
V_{OUT} = 0.4 V
F_{SW} = 600 kHz
I_{Load} = 8 A

We can see that the jitter is around 290 ns.

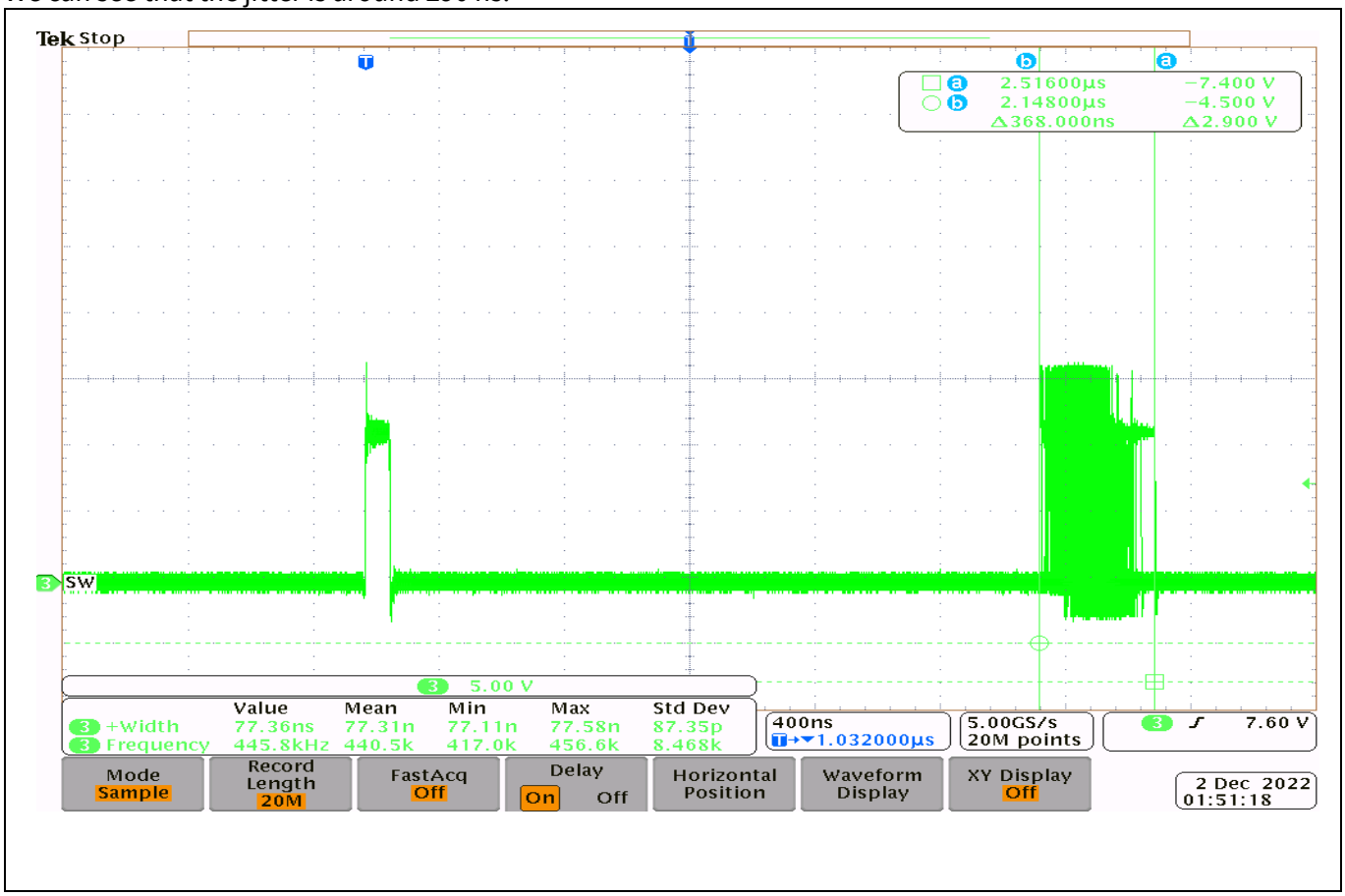

Figure 14 Jitter measurement without ripple injection circuit

As shown in the illustration below, the ripple injection circuit consists of the three components, R1, C1 and C2. The R1 and C1 cross the inductor, generating a triangular ripple waveform across the C1. The triangular ripple passes to V_{FB} via the C2 capacitor. The C2 capacitor, C2>>C1, blocks DC voltage to maintain the V_{OUT} DC accuracy.

Test results

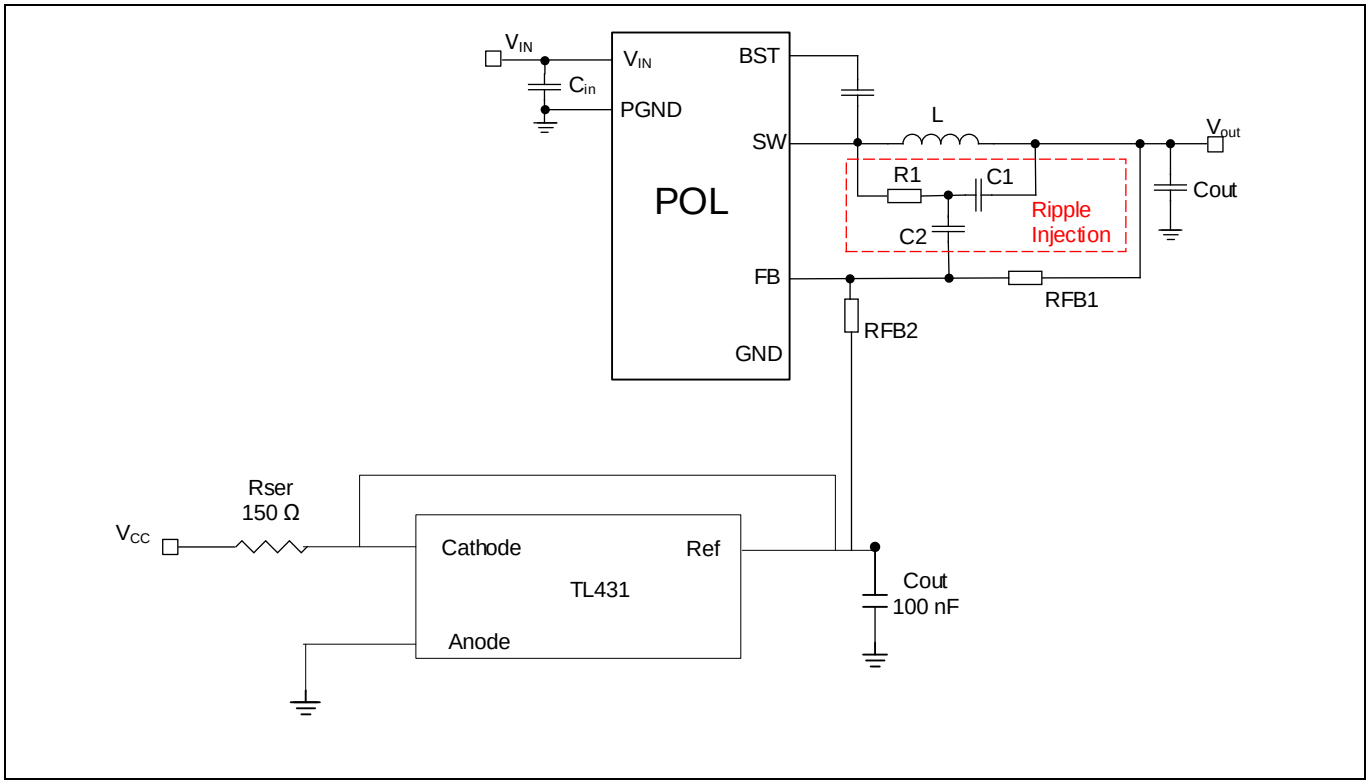

Figure 15 Ripple injection circuit

The selection of component value for ripple injection is a compromise between jitter reduction and transient performance. A recommended starting point of R1, C1 and C2 is shown below [2]:

$$R1 = \frac{40RFB1 \cdot V_0}{7 - \frac{V_0}{V_{ref}}}$$

$$C1 = \frac{\sqrt{LC_0}}{0.5 \times RFB1 \times \sqrt{\frac{40V_0}{7}}}$$

$$C2 \approx 10 \times C1$$

IR3889 analog POL with V_{OUT} = 0.4 V, which has:

- RFB1 = 10 kΩ
- V_{ref} = 0.8 V
- L = 0.12 µH
- C_{OUT} = 500 µF (a combination of bulk capacitor and MLCCs with derating)

$$\mathrm{R1} = \frac{40RFB1 \cdot V_0}{7 - \frac{V_0}{V_{ref}}} = \frac{40 \times 10k\Omega \cdot 0.4V}{7 - \frac{0.4V}{0.8V}} = 24.165k\Omega$$

R1 is further optimized to 10k so that the jitter is reduced.

Test results

$$C_1 = \frac{\sqrt{LC_0}}{0.5 \times RFB1 \times \sqrt{\frac{40V_0}{7}}} = \frac{\sqrt{0.12uH \times 500uF}}{0.5 \times 10k\Omega \times \sqrt{\frac{40 \times 0.4}{7}}} \approx 1nF$$

$$C2 \approx 10 \times C1 = 10 \times 1nF = 10nF$$

With the above values, the ripple injection circuit reduces jitter to 80 ns compared to 290 ns.

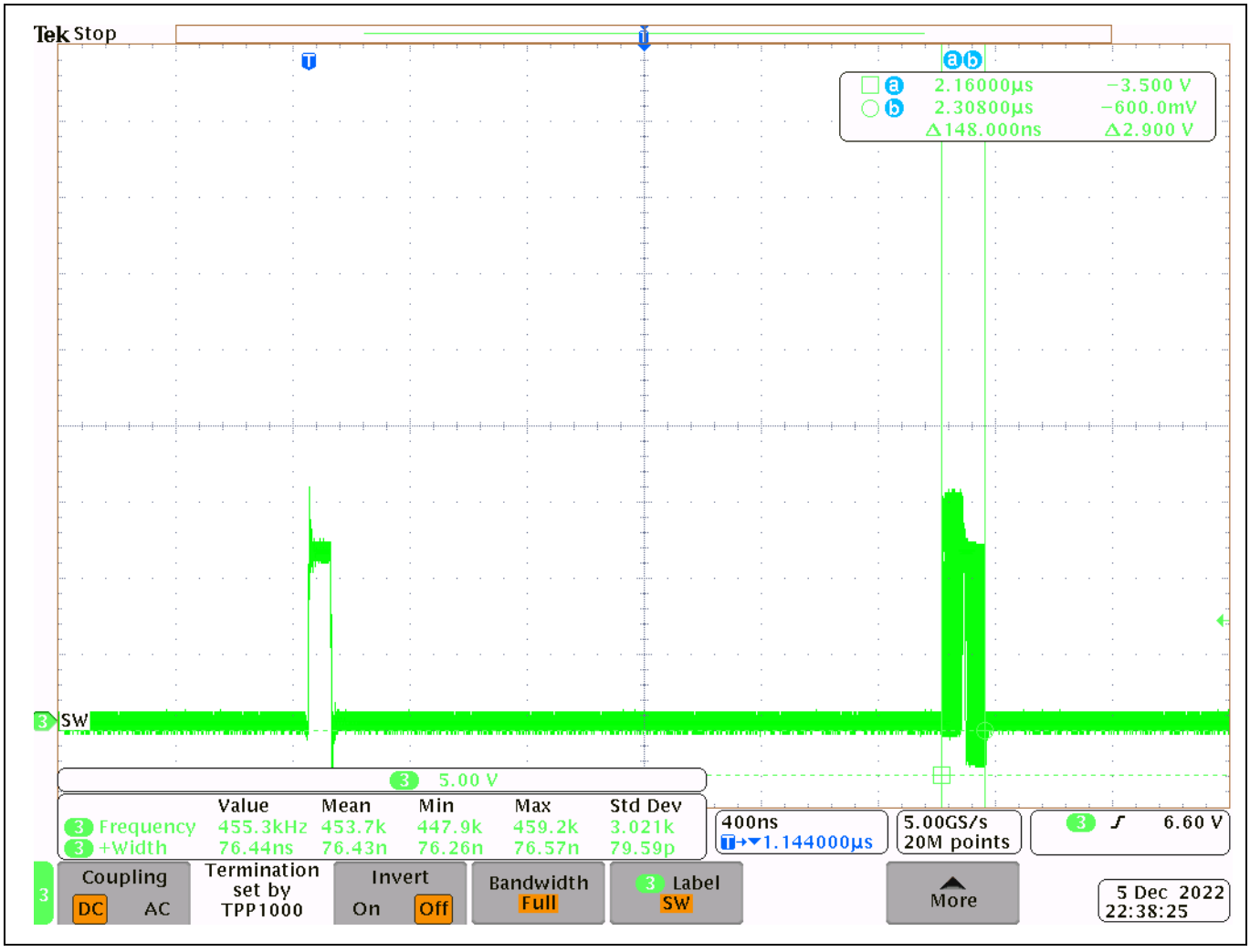

Figure 16 Jitter measurement with ripple injection circuit

Test results

As mentioned earlier, adding the ripple injection circuit will increase the phase margin, as shown in the plot below:

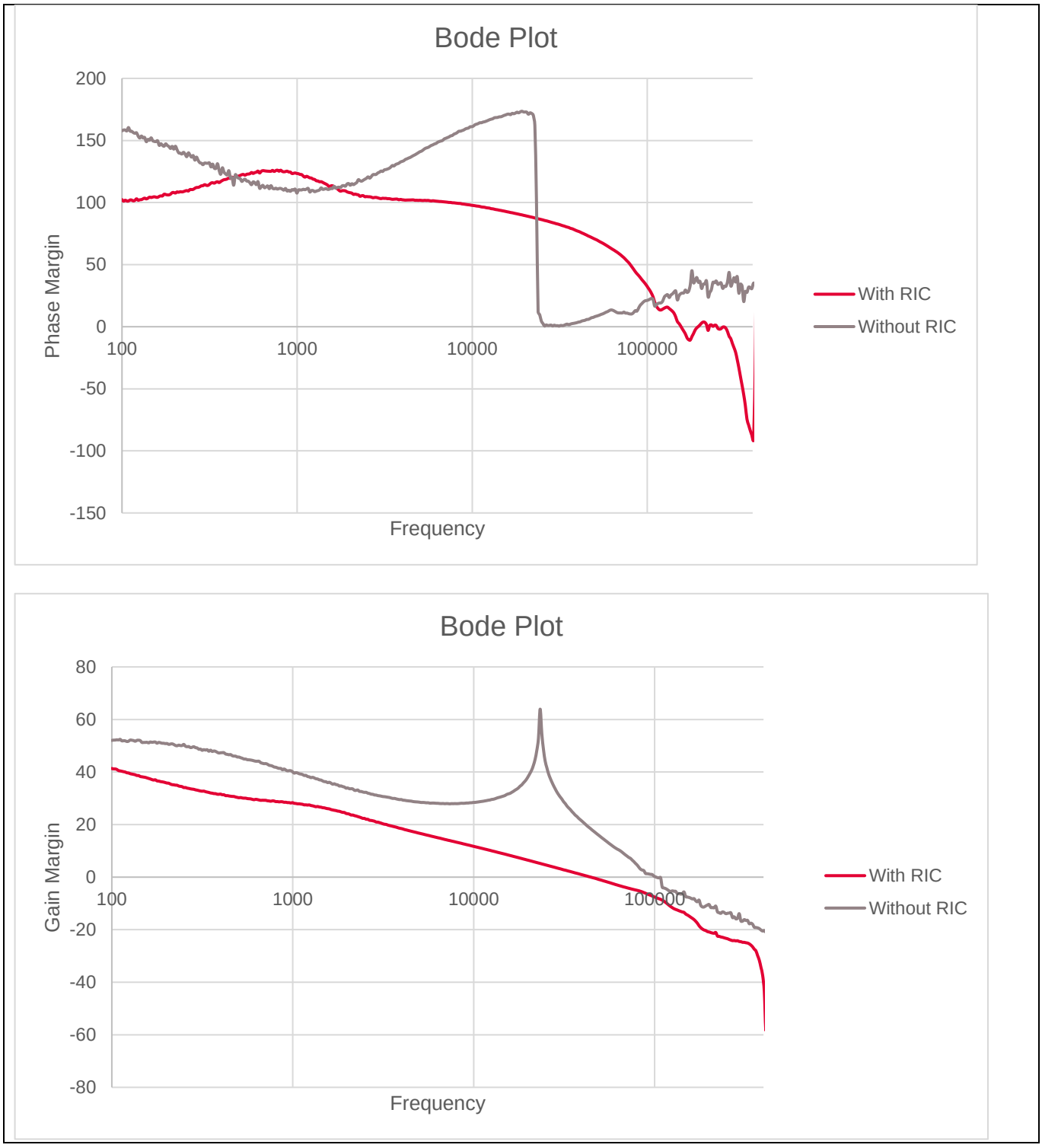

Figure 17 Gain margin and phase margin comparison

Test results

Transient response after adding the ripple injection circuit:

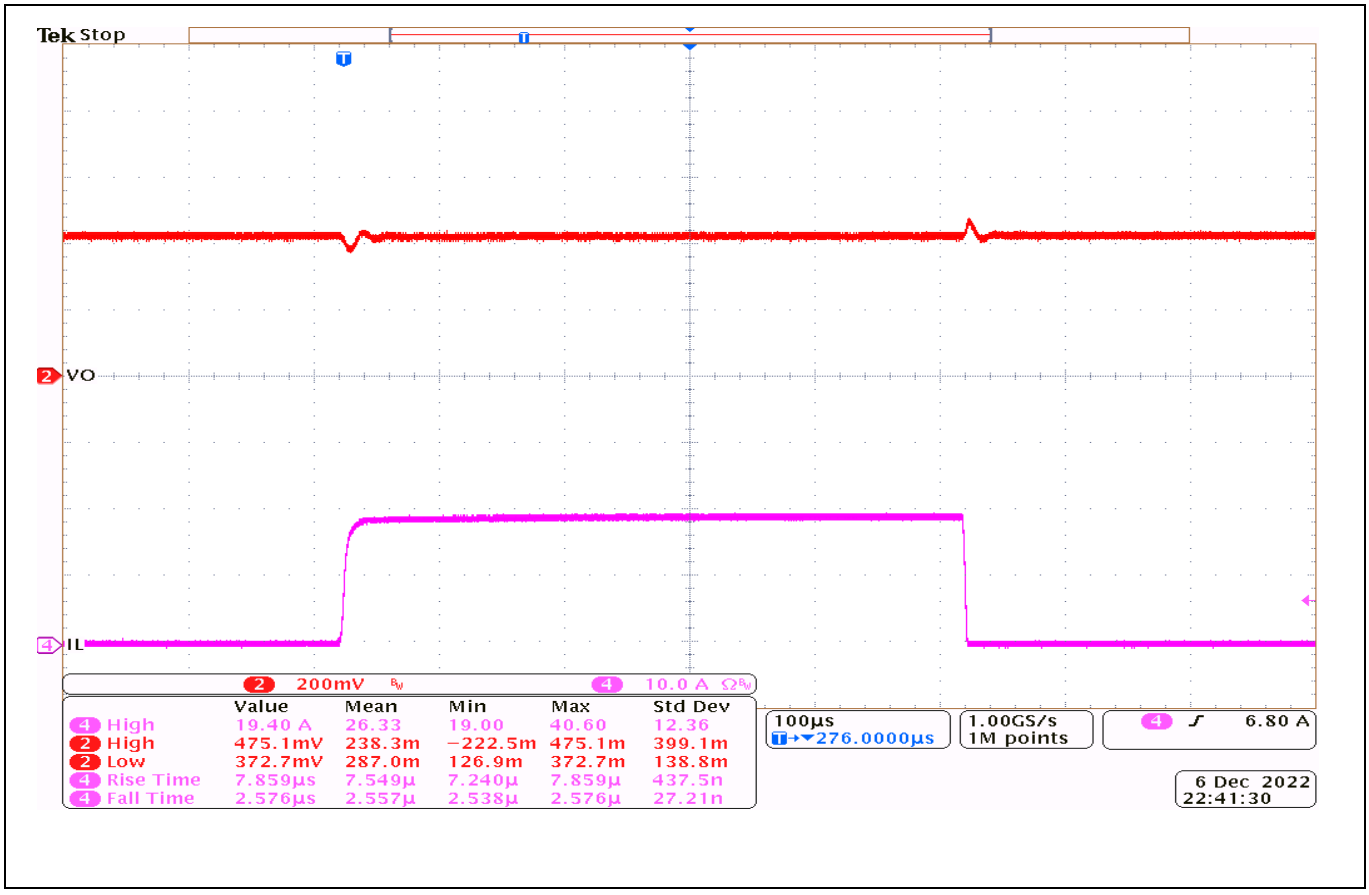

Figure 18 Transient response after adding the ripple injection circuit

Table 5 Overshoot and undershoot of output voltage during transient

Voltage ripple	Without ripple injection circuit	With ripple injection circuit
Positive side	46 mV	75.1 mV
Negative side	-14 mV	-27.3 mV

Summary

From the calculation we can observe that if we use the internal V_{CC} LDO, there is a variation of output. So, to avoid this we can use low-noise LDOs and voltage regulators so that the output will be within the requirements. For better accuracy the voltage difference between V_{SENM} and local GND may introduce some errors to the V_{OUT}, which can be compensated by adjusting the RFB1 and RFB2 if needed. The external voltage at the FB connection may introduce noise and affect the jitter content because of very low output voltage; to decrease the jitter content we should implement the ripple injection circuit, which is designed to achieve better jitter content for the configured output.

References

[1] Infineon Technologies AG: *Introduction of to fast COT for POL applications*; e-Learning Media; **Available online**

[2] Infineon Technologies AG: *IR38889 datasheet*; **Available online**

[3] Infineon Technologies AG: *Jitter reduction for fast COT POLs (V 1.0)*; 2022-10-28

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Document revision	Date	Description of changes
V 1.0	2023-02-22	Initial release

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