1200 V CIPOS™ Maxi IPM

1200 V CIPOS™ Maxi CoolSiC™ MOSFET IPM application note

About this document

Scope and purpose

The scope of this application note is to describe the 1200 V CIPOS™ Maxi CoolSiC™ MOSFET IPM family and the basic requirements for operating the products in a recommended mode. This is related to the integrated components, such as CoolSiC MOSFET or gate driver IC, as well as to the design of the necessary external circuitry, such as bootstrap or interfacing.

Intended audience

Power electronics engineers who want to design reliable and efficient 1200 V CIPOS Maxi IPM applications.

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1 Scope

The scope of this application note is to describe the product group of 1200 V CIPOS™ Maxi CoolSiC™ MOSFET IPM and the basic requirements for operating the products in a recommended mode. This is related to the integrated components, such as silicon carbide (SiC) MOSFET or gate driver ICs, as well as to the design of the necessary external circuitry, such as bootstrap or interfacing. Integrating discrete power semiconductors and gate driver ICs into one package allows design engineers to reduce the time and effort spent on design. To meet the strong demand for small size and higher power density, Infineon Technologies has developed a new family of highly integrated intelligent power modules that contain nearly all of the semiconductor components required to drive electronically controlled variable-speed electric motors. They incorporate a three-phase inverter power stage with an SOI gate driver and Infineon's leading-edge 1200 V CoolSiC Power MOSFETs.

The application note concerns the following products:

IM828-XCC

IM12S60EA2

IM12S90EA2

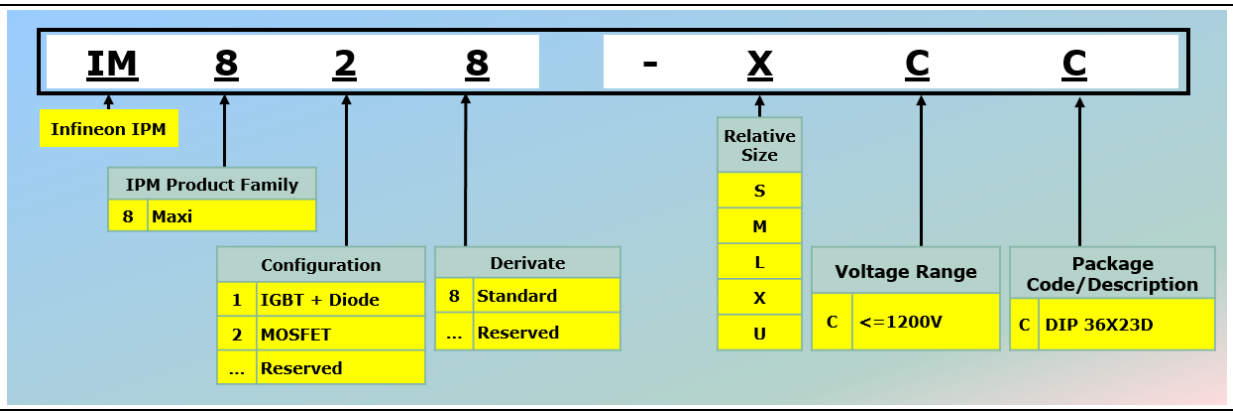
1200 V CoolSiC MOSFET IPM is a product group of CIPOS Maxi IPM family, which are designed for motor drives in commercial applications, such as fan drives, active harmonic filters, PWM rectifiers, and compressor drives for HVAC (heating, ventilating, and air-conditioning) systems, low power general purpose drives (GPD), pumps applications and as well as CAV (commercial, construction and agriculture vehicle) application.

1.1 Product line-up

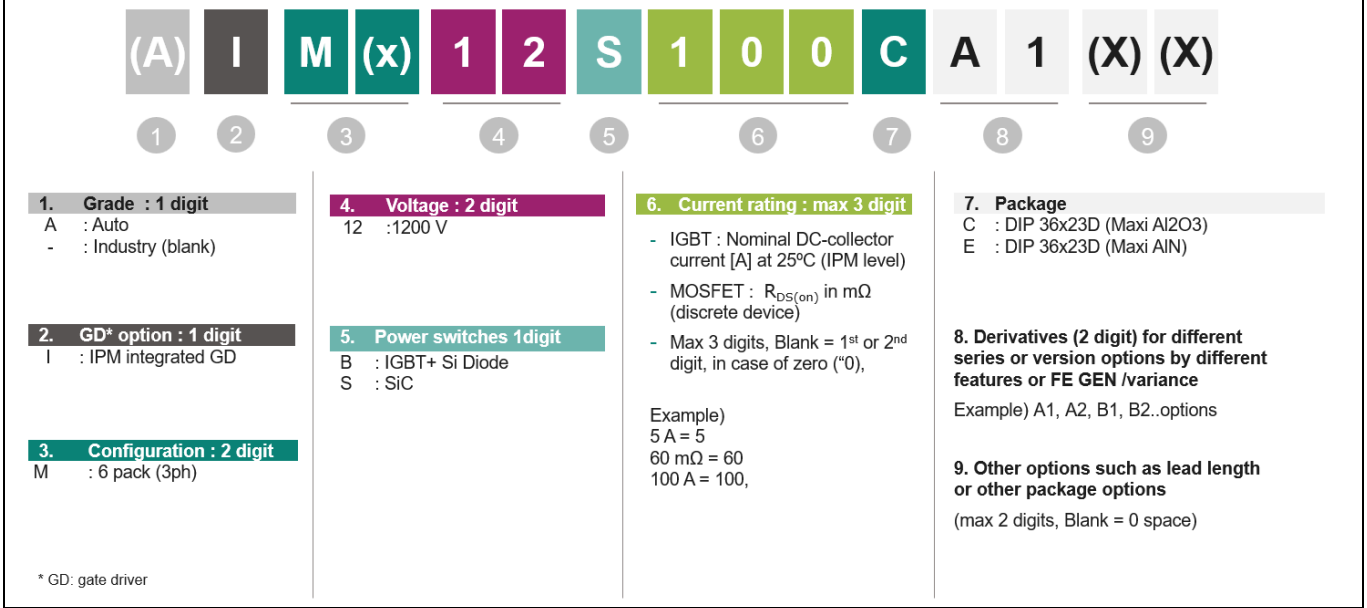
Table 1 Line-up of 1200 V CIPOS Maxi CoolSiC MOSFET IPM products (*Chip $R_{DS(on)}$, V_{GS} = 18 V, T_{vj} = 25°C)

Part Number	Rating		Topologies	Package	Isolation voltage [Vrms]	Main applications
	*$R_{DS(on)}$ [mΩ]	Voltage [V]				
IM828-XCC	30	1200	3ϕ bridge open source	Fully molded dual In-line module with Al_2O_3 DCB substrate	2500 Vrms/60 Hz (sinusoidal, 1 min. All pins shorted – heat sink)	Active harmonic filter for HVAC, Industrial motor drives, fans, and pumps as well as auxiliary inverter applications in CAV
IM12S60EA2	60	1200		Fully molded dual In-line module with AlN DCB substrate		
IM12S90EA2	90	1200				

1.2 Nomenclature



(a) Previous nomenclature (IM828-XCC)



(b) New nomenclature (IM12S60/90EA2)

Figure 1 1200 V CIPOS™ Maxi CoolSiC™ MOSFET IPM product group nomenclature

2 Internal components and package technology

2.1 1200 V CoolSiC™ MOSFET

Infineon Technologies introduced 1200 V CoolSiC MOSFET technology in 2017 [1]. Silicon carbide (SiC) opens up new degrees of flexibility for designers to harness never before seen levels of efficiency and reliability.
In comparison to traditional silicon (Si) based high voltage (> 600 V) switches like IGBTs and MOSFETs, the SiC MOSFET offers a series of advantages. These include the lowest gate charge and device capacitance levels seen in 1200 V switches, less reverse recovery losses of the body diode, temperature-independent low switching losses, and threshold-free on-state characteristics. Infineon's unique 1200 V SiC MOSFET adds additional advantages. Superior gate oxide reliability enabled by state-of-the-art trench design, best-in-class switching and conduction losses, highest transconductance level (gain), typical gate-source threshold voltage of $V_{GS(th)}$ = 4.5 V and short-circuit robustness. Delivering the highest-level efficiency at switching frequencies unreachable by Si-based switches allow for system size reduction, power density increases and high lifetime reliability.

2.2 Control IC - 1200 V 6-channel gate driver IC

The basic feature of this technology is the separation of the active silicon from the base material by means of a buried silicon oxide layer. The buried silicon oxide provides an insulation barrier between the active layer and silicon substrate, and hence reduces the parasitic capacitance tremendously. Moreover, this insulation barrier disables leakage or latch-up currents between adjacent devices. This also prevents the latch-up effect even in case of high dv/dt switching under elevated temperature, and hence provides improved robustness. Besides the thin-film SOI technology provides additional benefits like lower power consumption and higher immunity to radioactive radiation or cosmic rays.[3] A monolithic single control IC for all six MOSFETs provides further advantages, such as bootstrap circuitry, matched propagation delay times, built-in deadtime, anti-cross conduction, and all six MOSFETs turn-off under fault situations like undervoltage lockout or overcurrent.

2.3 Thermistor

In IPM, the thermistor is integrated in the internal PCB. It is connected between the VTH and VSS pins. A circuit proposal using the thermistor for over-temperature protection is discussed in Section 5.5.

Table 1 Raw data on the thermistor

T [°C]	R_{min} [kΩ]	R_{typ} [kΩ]	R_{max} [kΩ]	Tol [%]	T [°C]	R_{min} [kΩ]	R_{typ} [kΩ]	R_{max} [kΩ]	Tol [%]
-40.0	2809.57	2974.02	3146.14	6.0	45.0	35.43	36.69	37.97	3.4
-35.0	2011.21	2125.36	2244.59	5.9	50.0	29.15	30.16	31.18	3.3
-30.0	1458.73	1539.04	1622.76	5.7	55.0	24.10	24.91	25.73	3.2
-25.0	1070.96	1128.16	1187.68	5.5	60.0	20.02	20.67	21.33	3.1
-20.0	795.19	836.41	879.22	5.4	65.0	16.70	17.23	17.76	3.1
-15.0	596.67	626.70	657.83	5.2	70.0	13.99	14.42	14.86	3.0
-10.0	452.13	474.22	497.08	5.1	75.0	11.77	12.13	12.48	2.9
-5.0	345.77	362.18	379.13	4.9	80.0	9.95	10.23	10.52	2.8
0.0	266.72	279.02	291.69	4.8	85.0	8.43	8.67	8.91	2.7
5.0	207.43	216.71	226.27	4.7	90.0	7.18	7.37	7.57	2.7
10.0	162.55	169.62	176.89	4.5	95.0	6.13	6.29	6.45	2.6
15.0	128.31	133.73	139.29	4.4	100.0	5.25	5.39	5.52	2.5
20.0	101.98	106.17	110.45	4.3	105.0	4.51	4.63	4.75	2.6

25.0	81.58	84.83	88.16	4.2	110.0	3.88	3.99	4.10	2.7
30.0	65.66	68.21	70.81	4.1	115.0	3.36	3.45	3.54	2.7
35.0	53.17	55.17	57.21	3.9	120.0	2.91	2.99	3.08	2.8
40.0	43.29	44.87	46.48	3.8	125.0	2.53	2.60	2.68	2.8

2.4 Package technology

The 1200 V CoolSiC™ MOSFET IPM series offers the smallest size while providing high power density up to 1200 V 30 mΩ with V_{DD} = +18 V by employing CoolSiC MOSFETs with 6-channel gate driver ICs. It contains all the power components such as the SiC MOSFETs and isolates them from each other and from the heat sink. All low power components such as the gate driver IC and thermistor are assembled on a PCB.

The electric insulation is provided by the DCB itself, which is simultaneously the thermal contact to the heat sink. To further decrease the thermal impedance, the internal lead frame design is optimized [4]. Figure 2 shows the external view and internal structure of the CIPOS Maxi package.

The two dummy pins on the package side which fix the inner PCB, have no connection with the internal circuit, which means that the dummy pins have no electrical function and are isolated in the package.

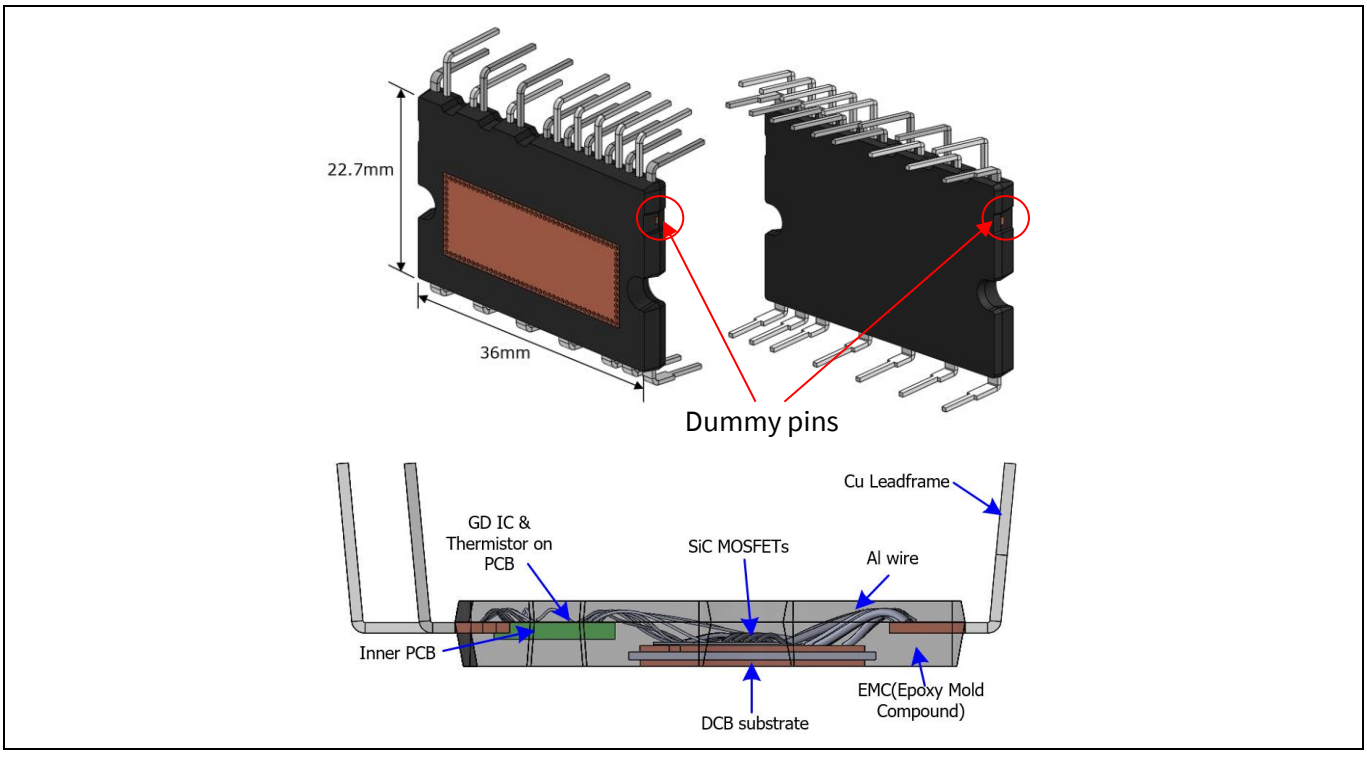


Figure 2 External view and internal structure of CIPOS™ Maxi package (DIP 36x23D)

3 Product overview

3.1 Internal circuit and features

Figure 3 illustrates the internal block diagram of the 1200 V CIPOS™ Maxi CoolSiC™ MOSFET IPM. It consists of a three-phase inverter circuit and a gate driver IC with control functions. The detailed features and integrated functions of IPM are described as follows.

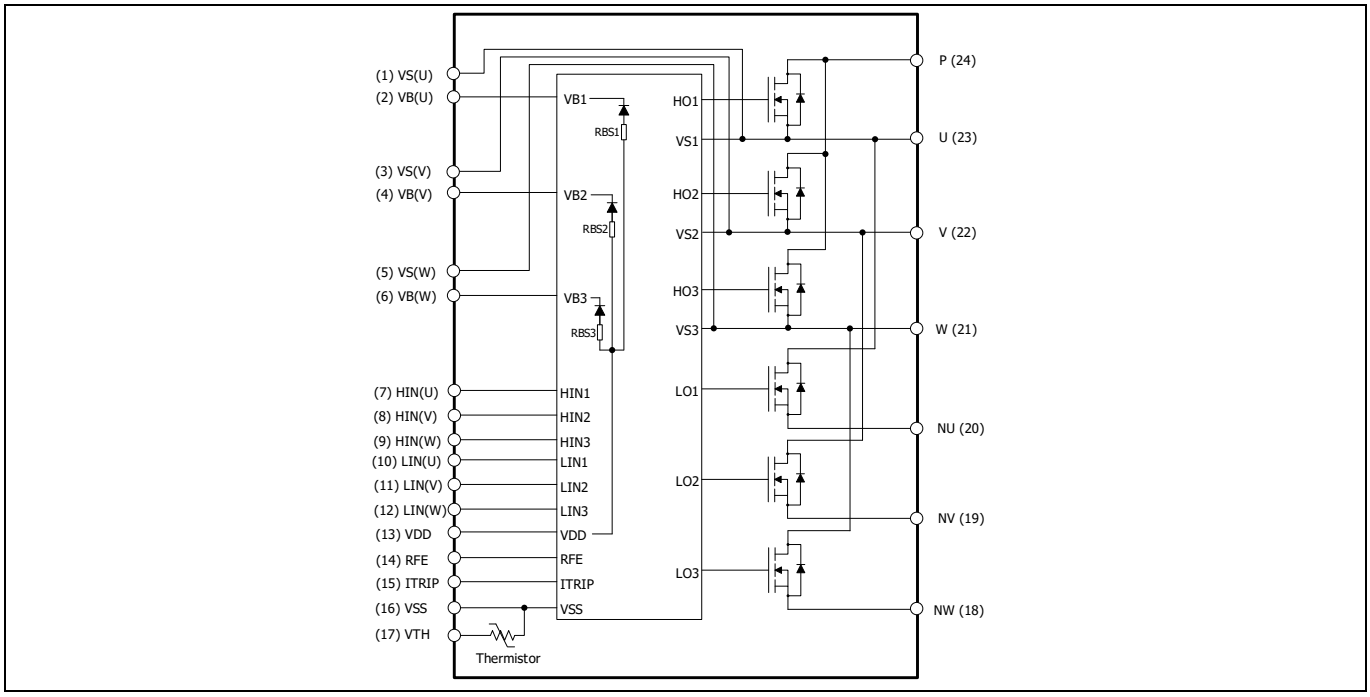


Figure 3 Internal circuit (3-phase inverter with open source)

Features

- Fully isolated DIL molded module with DCB substrate
- 1200 V CoolSiC™ MOSFETs 30, 60, and 90 mΩ at V_{DD} = +18 V (Based on chip $R_{DS(on)}$ only)
- Rugged 1200 V SOI gate driver technology with stability against transient and negative voltage
- Integrated bootstrap diode
- Matched delay times of all channels / built-in deadtime
- Lead-free terminal plating; RoHS compliant

Functions

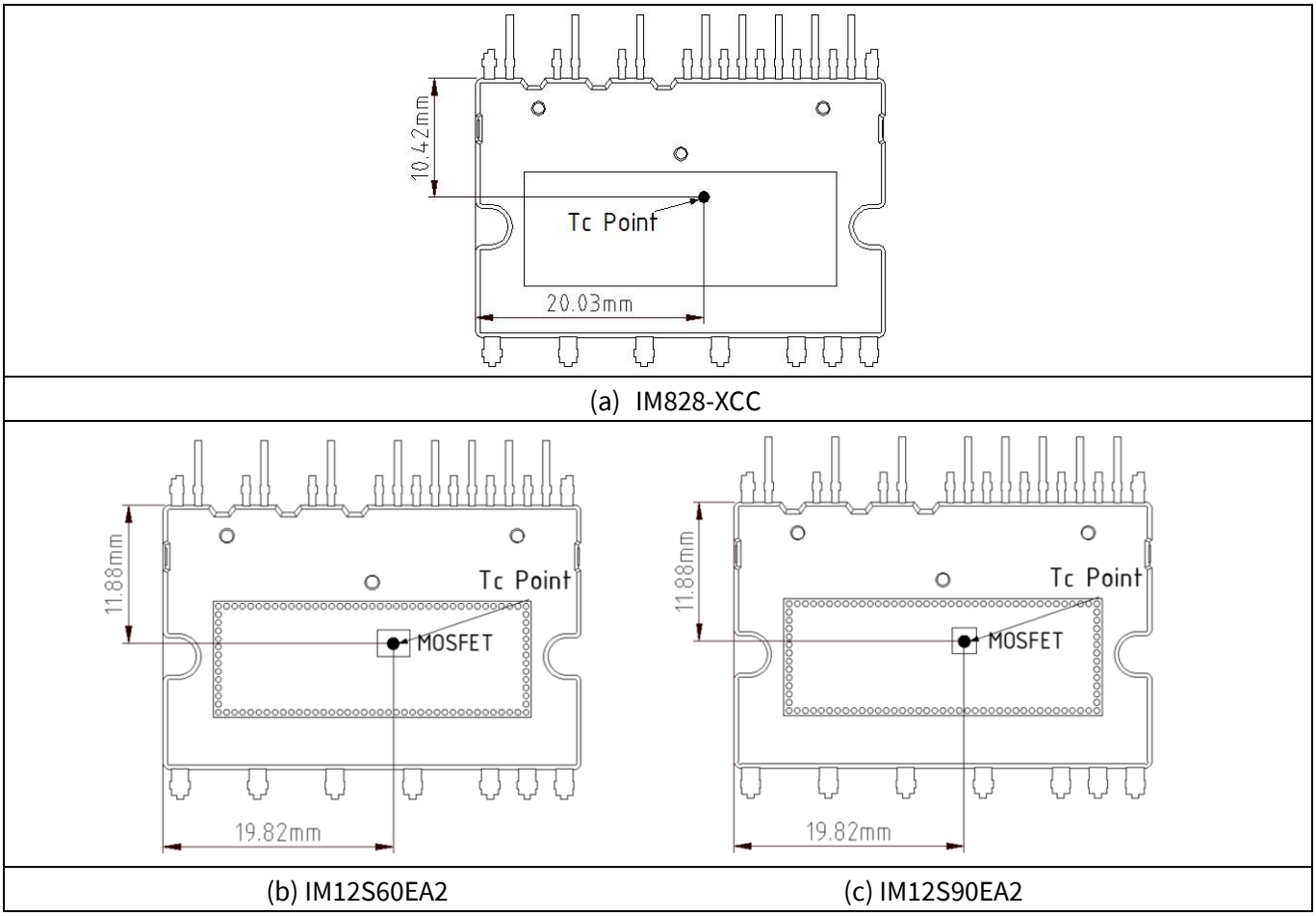
- Overcurrent shutdown
- Built-in NTC thermistor for temperature monitoring
- Under-voltage lockout at all channels
- Low-side source pins accessible for current monitoring
- Anti-cross conduction function
- All six switches turn off during protection
- Programmable fault clear timing and enable input

3.2 Maximum electrical ratings

Table 2 Detailed description of absolute maximum ratings (IM12S60EA2)

Item	Symbol	Rating	Description
Max. blocking voltage	V_{DSS}	1200 V	The sustained drain-source voltage of internal MOSFETs
*Output phase current	I_O	± 26.7 A_{rms}	The allowable IPM maximum output current
Operating junction temperature	T_{VJ}	-40 ~ 150°C	Considering temperature ripple on the power chips, the maximum junction temperature rating of the IPM is 150°C. (Maximum T_{VJ} of MOSFET itself can be 175°C, however IPM included not only MOSFET but also gate driver IC. Therefore, maximum T_{VJ} of IPM is just 150°C.)
Operating case temperature	T_C	-40 ~ 125°C	T_C (case temperature) is defined as the temperature of the package surface underneath the specified power chip. Please mount a temperature sensor on a heat sink surface at the defined position in Figure 4, to get accurate temperature information.

*Note: Pulse width and period are limited by junction temperature.



(a) IM828-XCC

(b) IM12S60EA2 (c) IM12S90EA2

Figure 4 T_C measurement point (unit [mm])

3.3 Electrical characteristics

3.3.1 Statics characteristics

The static characterization includes blocking capability, output characteristics, $R_{DS(on)}$ vs. T_J, and body diode I-V characteristics.

3.3.1.1 Blocking capability

The leakage current I_{DSS} of CoolSiC™ MOSFET is measured with increasing temperature at a blocking voltage 1200 V. This was done by V_{DD} = 0 V, and thus the device is off. At a blocking voltage of 1200 V, each device's leakage current I_{DSS} is typically at 2 µA at 25°C and 4 µA at 150°C.

3.3.1.2 Output characteristics

The I-V curves, or output characteristics, of each MOSFET on IM828-XCC are measured in pulse mode for different junction temperatures of 25°C and 150°C, respectively. Figure 6 (left) shows the drain current as a function of drain source voltage V_{DS} with different V_{DD}. The solid curves are typical results at 25°C and the dashed curves are the ones at the maximum junction temperature of 150°C. The device is designed for an on-state gate voltage of +15 V, which is common for Si IGBT. The typical on-resistance of the device is determined at V_{DD} = +15 V and a rated current of I_D = 20 A. It amounts $R_{DS(on)}$ = 55 mΩ at T_J = 25°C. (The $R_{DS(on)}$ of IM828-XCC included not only SiC MOSFET $R_{DS(on)}$ (typ. 45 mΩ) but also package parasitic resistance (approximately 10 mΩ, due to bonding wire and lead frame.)

As the SiC MOSFET is a voltage-controlled device, it turns on step by step with increasing gate source voltage V_{GS}. The higher gate source voltage is above threshold level, the higher drain current is at given drain voltage. The curves of Figure 6 are almost linear up to drain currents of about 30 A if the gate source voltage is above 13 V. For higher drain currents or lower gate source voltages, there is a significant curvature steadily lowering the current slope with increasing V_{DS}. This behaviour is a consequence of the built-in JFET which is formed by the deep p+ wells (see Figure 5). As the p+ wells are linked to source, the junction channel of the JFET is controlled by drain-source voltage drop. Hence, the JFET channel is narrowed down with increasing V_{DS}. This feature improves the short-circuit ruggedness by limiting the saturation current for very high drain voltages V_{DS}.

The temperature behaviour of the I-V characteristic depends also on temperature: above 13 V of control supply voltage V_{DD}, the drain current decreases with temperature. Below 13 V control supply voltage V_{DD}, the drain current increases with temperature, this is not recommended to have V_{DD} below +13 V for on-state. However, IM828-XCC have V_{DD} and V_{BS} undervoltage lock out UVLO functionality to prevent operation with low gate voltage. In general, the device could be driven with higher V_{DD} than 15 V, which further improves the on-state behaviour. However, the lifetime of the gate oxide will be reduced since the gate oxide stress is higher thus accelerating the aging of the device. Consequently, the failure rate can be increased by using a higher control supply voltage than 15 V. For on-state operating, Infineon recommends V_{DD} = +15 V of its IM828-XCC. The trade-off between long lifetime and low drain voltage V_{DS} is balanced in an optimum manner for this on-state operation voltage. For more information, refer to reference document. [9]

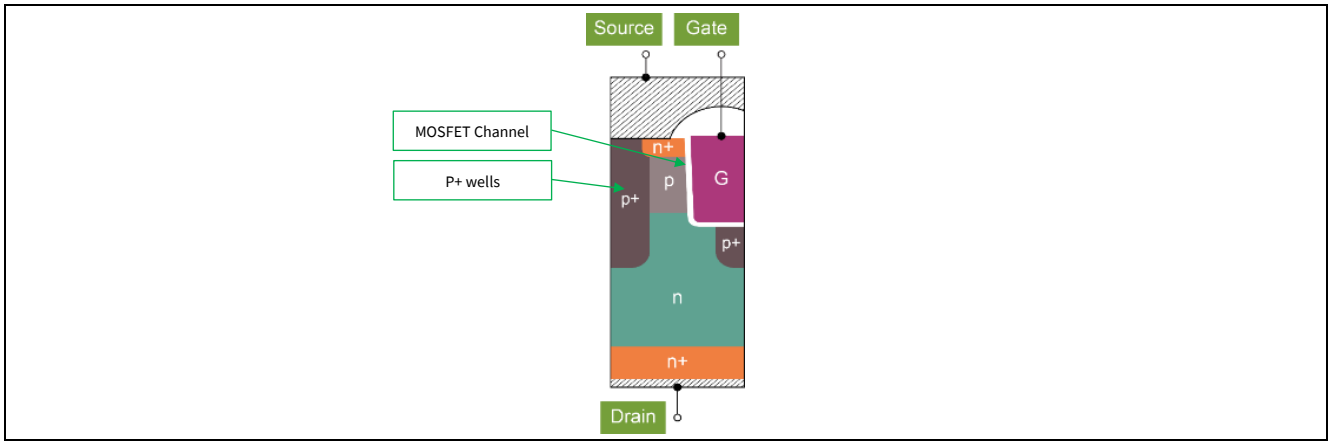


Figure 5 Sketch of the CoolSiC™ MOSFET cell

3.3.1.3 On-state resistance $R_{DS(on)}$ vs. junction temperature T_J

The on-state resistance $R_{DS(on)}$ is shown below in Figure 6 (right) as a function of junction temperature T_J with drain-to-source current I_D as a parameter. At 20 A and 25°C, the typical value of $R_{DS(on)}$ is 55 mΩ with V_{DD} = +15 V (included package resistance).
The $R_{DS(on)}$ of CoolSiC™ MOSFET is mainly determined by three parts: MOSFET's channel, intrinsic JFET and drift region in the device, which are all temperature dependent. The MOSFET's channel has a negative temperature characteristic due to the behaviour of the interface states, while drift region and intrinsic JFET have positive temperature characteristic. Because of the advantageous channel orientation along the preferred crystal plane with a low density of interface defects, the total $R_{DS(on)}$ of CoolSiC™ MOSFET is not dominated by the MOSFET's channel resistance, and it monotonously increases with temperature as the physics of MOSFETs with superior channel quality predict. This behaviour is beneficial to balance the current distribution of parallel devices. Moreover, with high temperature, the $R_{DS(on)}$ is increased to limit the highest saturation current, and thus improve the short circuit ruggedness of the device as well.

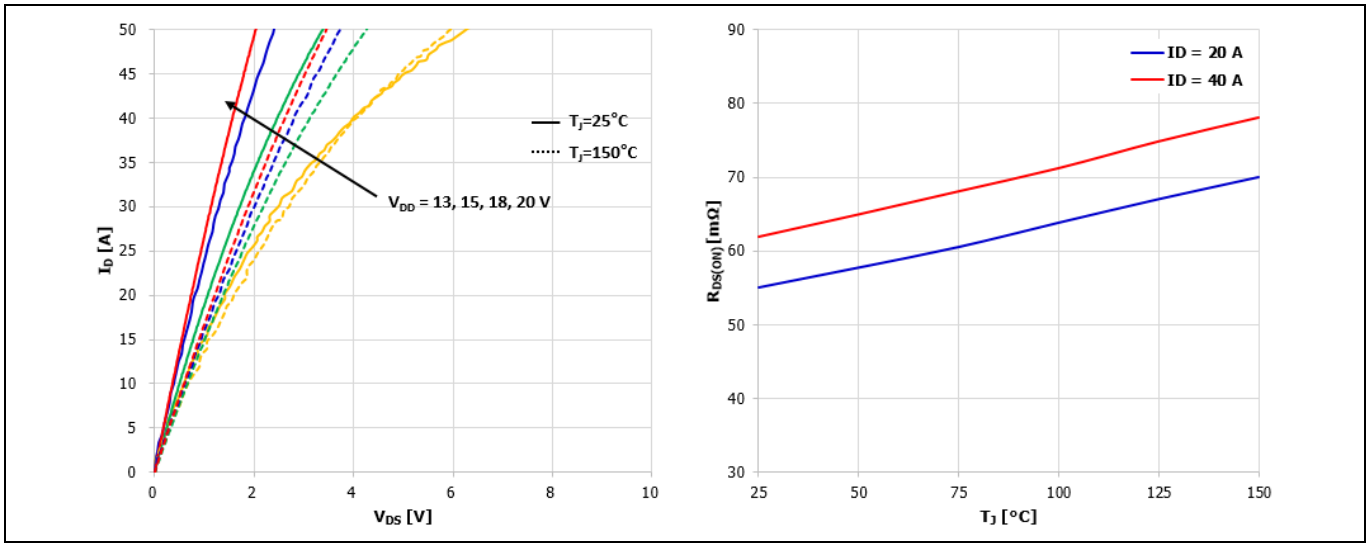


Figure 6 (Left) Typical output characteristic, V_{DD} as parameter, with T_J = 25°C and T_J = 150°C; (Right) Typical on-resistance vs. junction temperature, I_D as parameter (V_{DD} = 15 V)

3.3.1.4 3rd quadrant operating mode

Like other MOSFETs, the CoolSiC™ MOSFET also integrates an intrinsic body diode with p-n junction behaviour. As shown in Figure 7, the intrinsic bipolar body diode has high forward voltage V_{SD} (about 4.1 V at 20 A) if the control supply voltage is 0 V. This is due to the wide bandgap characteristics of the silicon carbide material. The forward voltage V_{SD} has a negative temperature coefficient as well as the standard Si p-n junction diode. So, it is not useful using its body diode to conduct current for long cycle periods. However, the body diode has to operate during the deadtime when both high-side and low-side MOSFETs are turned off for bridge topology, and to reduce the on-state conduction losses due to the body diode, it is necessary to design the deadtime as short as possible. The value of deadtime depends on the topologies and design circuit, for example, hard-switching or soft-switching, PCB layout, gate drive IC selection, and etc. It can range from one hundred nanoseconds to several hundred nanoseconds.
Fortunately, unlike an IGBT, the SiC MOSFET can conduct reverse current from source to drain through the channel, if a positive bias is applied to the gate. This mode of operation is called synchronous rectification (or 3rd quadrant operation) and is achieved with a positive voltage of typically +15 V on the gate. As shown in the figure below, this synchronous rectification mode is highly recommended to limit the conduction loss. Also, with synchronous rectification mode, another benefit is to have a positive temperature coefficient with the ease of the devices' paralleling operation, which is the same as the 1st quadrant output I-V operation mentioned in Section 3.3.2.1. Table 3 shows the static characteristics of IM828-XCC.

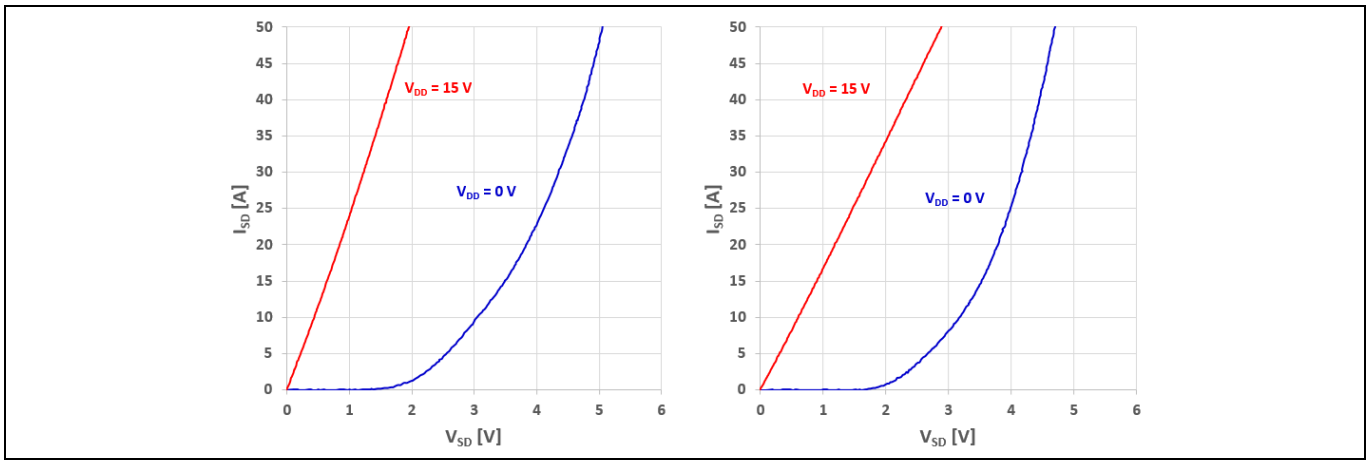


Figure 7 Reverse current I_{SD} as function of voltage at different V_{DD} and temperature: T_J = 25°C (left), T_J = 150°C (right)

Table 3 Static characteristics of IM828-XCC (at V_{DD} = V_{BS} = 15 V, *included package resistance)

Description	Symbol	Condition		Value			Unit
				Min.	Typ.	Max.	
Drain-source on-state resistance	*$R_{DS(on)}$	V_{IN} = 5 V I_D = 20 A	T_J = 25°C	-	55	87	mΩ
			T_J = 150°C	-	70	-	
Drain-source leakage current	I_{DSS}	V_{DS} = 1200 V		-	-	1	mA
Diode forward voltage	V_{SD}	V_{IN} = 0 V I_{SD} = 20 A	T_J = 25°C	-	3.9	5.8	V
			T_J = 150°C	-	3.8	-	

Table 5 Static characteristics of IM12S60EA2 (at V_{DD} = V_{BS} = 18 V, **without package resistance)

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Drain-source on-state resistance	**$R_{DS(on)}$	I_D = 13 A, V_{IN} = 5 V, V_{DD} = 18 V, T_{VJ} = 25°C 150°C	- -	60 100	83 -	mΩ
Drain-source leakage current	I_{DSS}	V_{DS} = 1200V	-	-	1	mA
Diode forward voltage	V_{SD}	I_{SD} = (13 A), V_{IN} = 0 V T_{VJ} = 25°C 150°C	- -	4.1 3.9	5.2 -	V

3.3.2 Dynamic characteristics

The dynamic characterization includes the switching characteristics, body diode reverse recovery characteristics, and short circuit ruggedness.

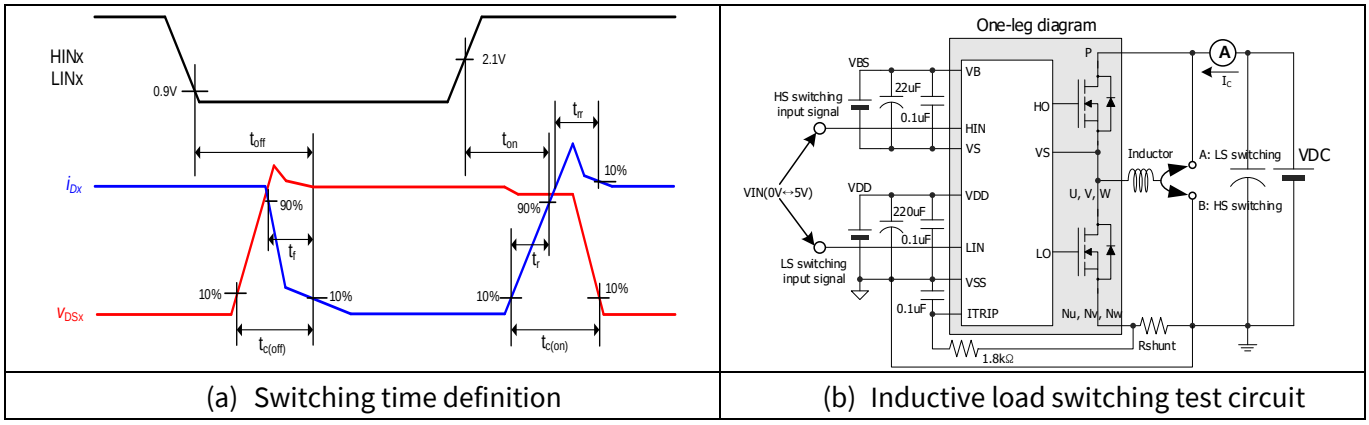
3.3.2.1 Switching characteristics

The CoolSiC™ MOSFET on IM828-XCC is needed to consider the on-state and off-state control supply voltage V_{DD} voltage at first. For the turn-on V_{DD} voltage of on-state operating, as mentioned in the previous section, +15 V is recommended to trade-off between long lifetime and low forward voltage, which is also a common turn-on voltage in common Si IGBTs. To ensure low conduction loss, the supply of the gate driver should be stabilized for maintaining the on-state V_{DD} at 15 V ideally. For the turn-off V_{DD} voltage of off-state operating, the SiC MOSFET itself is capable of switching at a very high speed and the voltage slew rate can range from tens to a hundred of volts per nanosecond. To improve the noise interference immunity, a negative gate-to-source turn-off voltage is normally recommended. However, the slew rate of IM828-XCC is designed to a few volts per nanosecond for three-phase inverter applications by the internal SOI gate driver IC. Therefore, IM828-XCC is allowed off-state operating with V_{GS} = 0 V because of the high robustness threshold voltage $V_{GS(th)}$ of the CoolSiC MOSFET.

The switching time definition and evaluation method are shown in Figure 8(a) and (b). The inductive load switching test circuit is used to measure the switching losses for V_{DD} = 15 V at 150°C as shown in Figure 9(left). The recommended control supply voltage V_{DD} (gate source voltage V_{GS}) of IM828-XCC is 15 V.

Under the same operating conditions, IM828-XCC shows much fewer switching losses compared to its conventional Si IGBT IPM as Figure 9 (right). In addition, IM828-XCC can achieve better switching performance (E_{on} by 18% and E_{off} by around 2% at drain current to 40 A) with higher control supply voltage V_{DD}(18V) without the SiC MOSFET degradation impact[9] as shown in Figure 9(left and center). Figure 10 shows a typical switching waveform of IM828-XCC at inductive load-switching test conditions as in Figure 8(b). However, it should also be considered that the short-circuit peak current is much higher compared to the 15 V turn-on voltage as shown in Figure 15. Therefore, the short-circuit capability of the IM828-XCC at 18 V turn-on voltage will be worse than at 15 V turn-on voltage.

New IM12SxxEA2 have more faster switching characteristics than IM828-XCC. Table 6 and Figure 12 shows switching speed (slew rate) and switching loss comparison between IM828-XCC and IM12S60/90EA2. This kind of faster switching characteristics can be maximizing 1200V CoolSiC MOSFET performance and IM12SxxEA2 will be more suitable product for fast switching applications such as active harmonic filter, PFC, and fans & pumps of CAV.



(a) Switching time definition | (b) Inductive load switching test circuit

Figure 8 Switching time definition and evaluation circuit for switching test

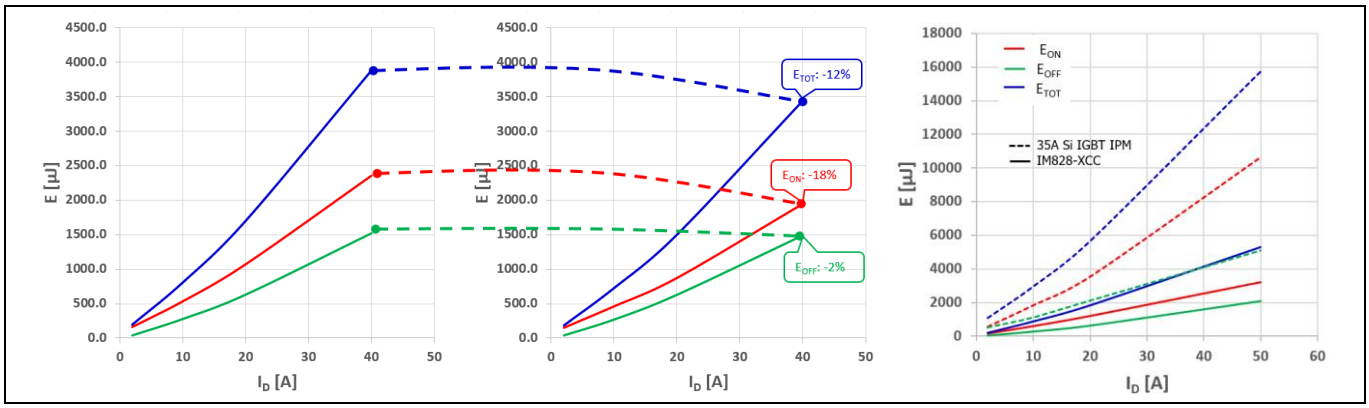


Figure 9 Typical switching energy losses at T_J=150°C; V_{DD} = 15 V (left) and V_{DD} = 18 V (center), and typical switching energy losses comparison between IM828-XCC and 35A Si IGBT IPM (right)

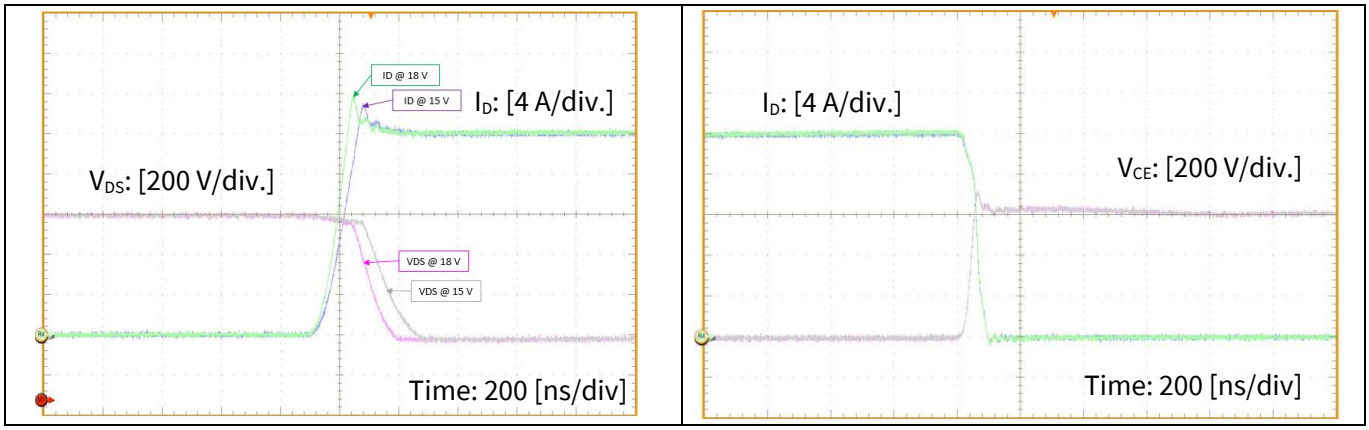


Figure 10 IM828-XCC typical switching waveform; turn-on(left) and turn-off(right) (V_{DC} = 600 V, V_{DD} = 15 / 18 V, I_D = 20 A, T_J = 150°C, inductive load = 3 mH)

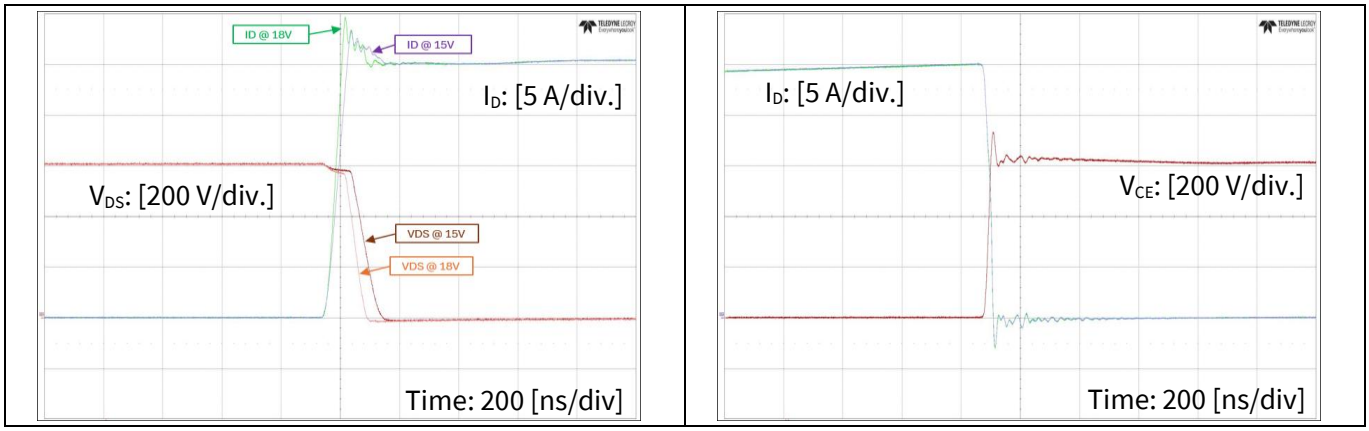


Figure 11 IM12S60EA2 typical switching waveform; turn-on(left) and turn-off(right) (V_{DC} = 600 V, V_{DD} = 15 / 18 V, I_D = 25 A, T_J = 150°C, inductive load = 1 mH)

Table 6 Typical switching characteristics comparison between IM828-XCC (2 / 20 A) and IM12S60EA2 (2.5 / 25 A) / IM12S90EA2 (1.5 / 15 A)

V_{DC} = 600 V, V_{DD} = 18 V T_{VJ} = 25°C, Inductive load switching	Turn-on (10% of rated current)				Turn-off (100% rated current)			
	High-side MOSFET		Low-side MOSFET		High-side MOSFET		Low-side MOSFET	
	dv/dt [kV/µs]	di/dt [A/µs]	dv/dt [kV/µs]	di/dt [A/µs]	dv/dt [kV/µs]	di/dt [A/µs]	dv/dt [kV/µs]	di/dt [A/µs]
IM828-XCC	7.5	150.0	5.2	95.0	7.0	350.0	4.50	10.50
IM12S60EA2	14.0	270.0	10.0	200.0	16.0	1270.0	26.0	1150.0
IM12S90EA2	23.0	250.0	16.5	200.0	21.0	380.0	30.0	480.0

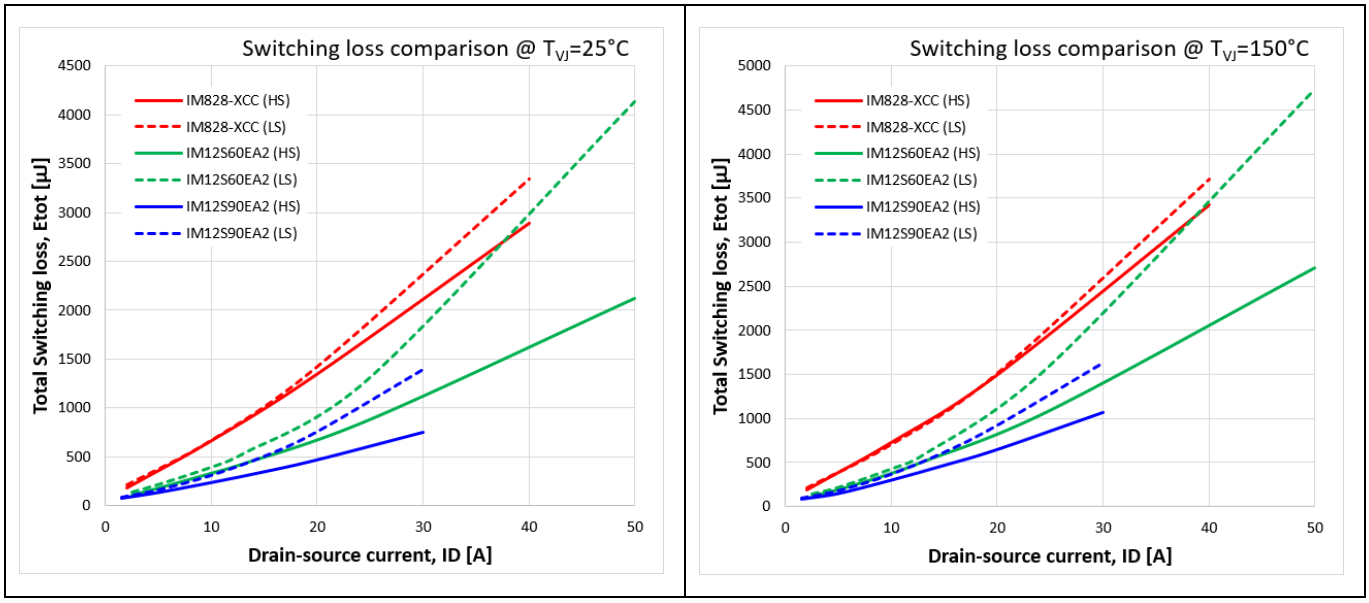


Figure 12 Typical switching loss comparison between IM828-XCC and IM12S60/90EA2 (V_{DC} = 600 V, V_{DD} = 18 V, T_J = 25 / 150°C, inductive load switching)

Table 7, Table 8, Table 9, and Table 10 shows dynamic characteristics and switching losses of IM828-XCC & IM12S60EA2.

Table 7 Dynamic characteristics of IM828-XCC (at V_{DD} = 15 V, T_{VJ} = 25°C)

Description		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
High side	Turn-on propagation delay time	t_{on}	V_{HIN} = 0 V ⟶ 5 V, I_D = 20 A, V_{DC} = 600 V	-	870	-	ns
	Turn-on rise time	t_r		-	45	-	ns
	Turn-on switching time	$t_{c(on)}$		-	140	-	ns
	Reverse recovery time	t_{rr}		-	60	-	ns
	Turn-off propagation delay time	t_{off}	V_{HIN} = 5 V ⟶ 0 V, I_D = 20 A, V_{DC} = 600 V	-	960	-	ns
	Turn-off fall time	t_f		-	70	-	ns
	Turn-off switching time	$t_{c(off)}$		-	100	-	ns
Low side	Turn-on propagation delay time	t_{on}	V_{LIN} = 0 V ⟶ 5 V, I_D = 20 A, V_{DC} = 600 V	-	960	-	ns
	Turn-on rise time	t_r		-	85	-	ns
	Turn-on switching time	$t_{c(on)}$		-	230	-	ns
	Reverse recovery time	t_{rr}		-	90	-	ns
	Turn-off propagation delay time	t_{off}	V_{LIN} = 5 V ⟶ 0 V, I_D = 20 A, V_{DC} = 600 V	-	880	-	ns
	Turn-off fall time	t_f		-	50	-	ns
	Turn-off switching time	$t_{c(off)}$		-	60	-	ns

Table 8 Switching loss of IM828-XCC (at V_{DC} = 600 V, V_{DD} = 15 V, I_D = 20 A)

Description		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
High side	MOSFET turn-on energy (includes reverse recovery of diode)	E_{on}	T_J = 25°C	-	0.90	-	mJ
			T_J = 150°C		1.04		mJ
	MOSFET turn-off energy	E_{off}	T_J = 25°C	-	0.48	-	mJ
			T_J = 150°C	-	0.66	-	mJ
	Body diode recovery energy	E_{rec}	T_J = 25°C	-	0.08	-	mJ
			T_J = 150°C		0.10		mJ
Low side	MOSFET turn-on energy (includes reverse recovery of diode)	E_{on}	T_J = 25°C	-	1.51	-	mJ
			T_J = 150°C		1.62		mJ
	MOSFET turn-off energy	E_{off}	T_J = 25°C	-	0.25	-	mJ
			T_J = 150°C	-	0.34	-	mJ
	Body diode recovery energy	E_{rec}	T_J = 25°C	-	0.07	-	mJ
			T_J = 150°C		0.07		mJ

Table 9 Dynamic characteristics of IM12S60EA2 (at V_{DD} = 18 V, T_{VJ} = 25°C)

Description		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
High side	Turn-on propagation delay time	t_{on}	V_{HIN} = 0 V ⟶ 5 V, I_D = 25 A, V_{DC} = 600 V	-	780	-	ns
	Turn-on rise time	t_r		-	30	-	ns
	Turn-on switching time	$t_{c(on)}$		-	60	-	ns
	Reverse recovery time	t_{rr}		-	40	-	ns
	Turn-off propagation delay time	t_{off}	V_{HIN} = 5 V ⟶ 0 V, I_D = 25 A, V_{DC} = 600 V	-	750	-	ns
	Turn-off fall time	t_f		-	20	-	ns
	Turn-off switching time	$t_{c(off)}$		-	40	-	ns
Low side	Turn-on propagation delay time	t_{on}	V_{LIN} = 0 V ⟶ 5 V, I_D = 25 A, V_{DC} = 600 V	-	870	-	ns
	Turn-on rise time	t_r		-	70	-	ns
	Turn-on switching time	$t_{c(on)}$		-	70	-	ns
	Reverse recovery time	t_{rr}		-	40	-	ns
	Turn-off propagation delay time	t_{off}	V_{LIN} = 5 V ⟶ 0 V, I_D = 25 A, V_{DC} = 600 V	-	700	-	ns
	Turn-off fall time	t_f		-	20	-	ns
	Turn-off switching time	$t_{c(off)}$		-	30	-	ns

Table 10 Switching loss of IM12S60EA2 (at V_{DC} = 600 V, V_{DD} = 18 V, I_D = 25 A)

Description		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
High side	MOSFET turn-on energy (includes reverse recovery of diode)	E_{on}	T_J = 25°C	-	0.55	-	mJ
			T_J = 150°C		0.72		mJ
	MOSFET turn-off energy	E_{off}	T_J = 25°C	-	0.35	-	mJ
			T_J = 150°C	-	0.48	-	mJ
	Body diode recovery energy	E_{rec}	T_J = 25°C	-	0.10	-	mJ
			T_J = 150°C		0.14		mJ
Low side	MOSFET turn-on energy (includes reverse recovery of diode)	E_{on}	T_J = 25°C	-	1.03	-	mJ
			T_J = 150°C		1.19		mJ
	MOSFET turn-off energy	E_{off}	T_J = 25°C	-	0.17	-	mJ
			T_J = 150°C	-	0.23	-	mJ
	Body diode recovery energy	E_{rec}	T_J = 25°C	-	0.03	-	mJ
			T_J = 150°C		0.06		mJ

3.3.2.2 Body diode reverse recovery characteristics

The intrinsic body diode switching performance of SiC MOSFET is measured with V_{DS}=600 V, V_{DD}=15 V and I_D = 20 A. Figure 13 is reverse recovery losses Err and reverse recovery current Irr as a function of diode current slope for IM828-XCC based on CoolSiC™ MOSFET body diode dynamic characteristics.
From Figure 13, unlike the SiC Schottky diode, the reverse recovery loss (E_{rr}) is temperature dependent; the higher the temperature, the higher the reverse recovery losses. Obviously, this is an effect due to minority carriers injected by the forward biased intrinsic pn-junction, which generates a reverse recovery charge. Fortunately, the absolute values at the rated current are still fairly low, meaning the CoolSiC MOSFET has negligible reverse recovery losses.

The body diode E_{rr} is an important parameter for bridge topology with hard switching. During the deadtime period of bridge topology, the body diode is freewheeling current before the corresponding switch is turned on, and when this corresponding switch is turned on, the body diode reverse recovery current will go through the corresponding switch in a short period. With the low E_{rr} of CoolSiC MOSFET, it can minimize the switching loss and increase the switching frequency.

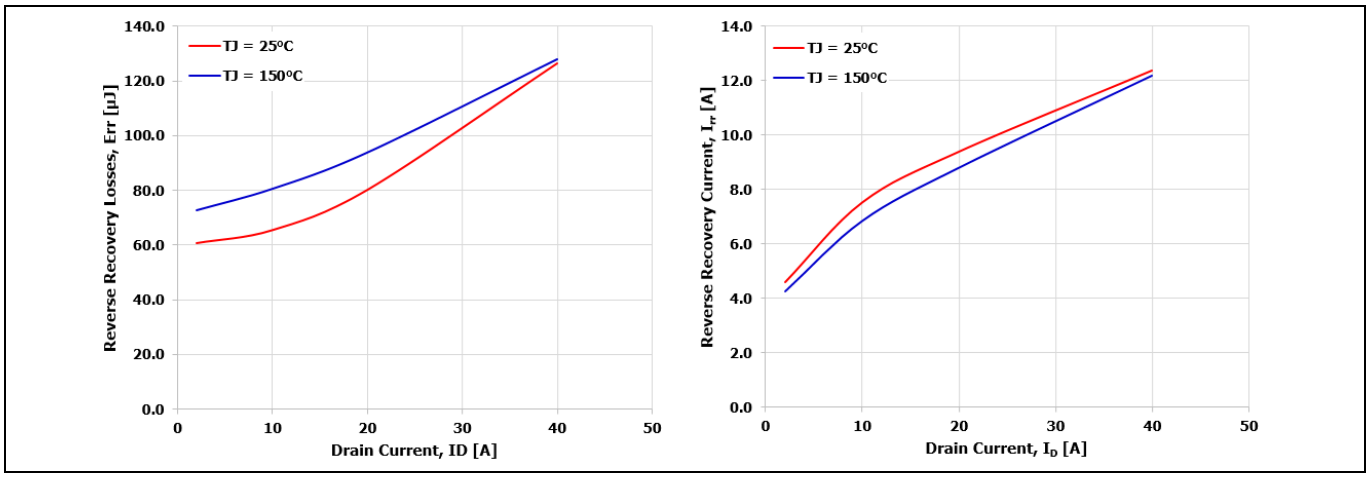
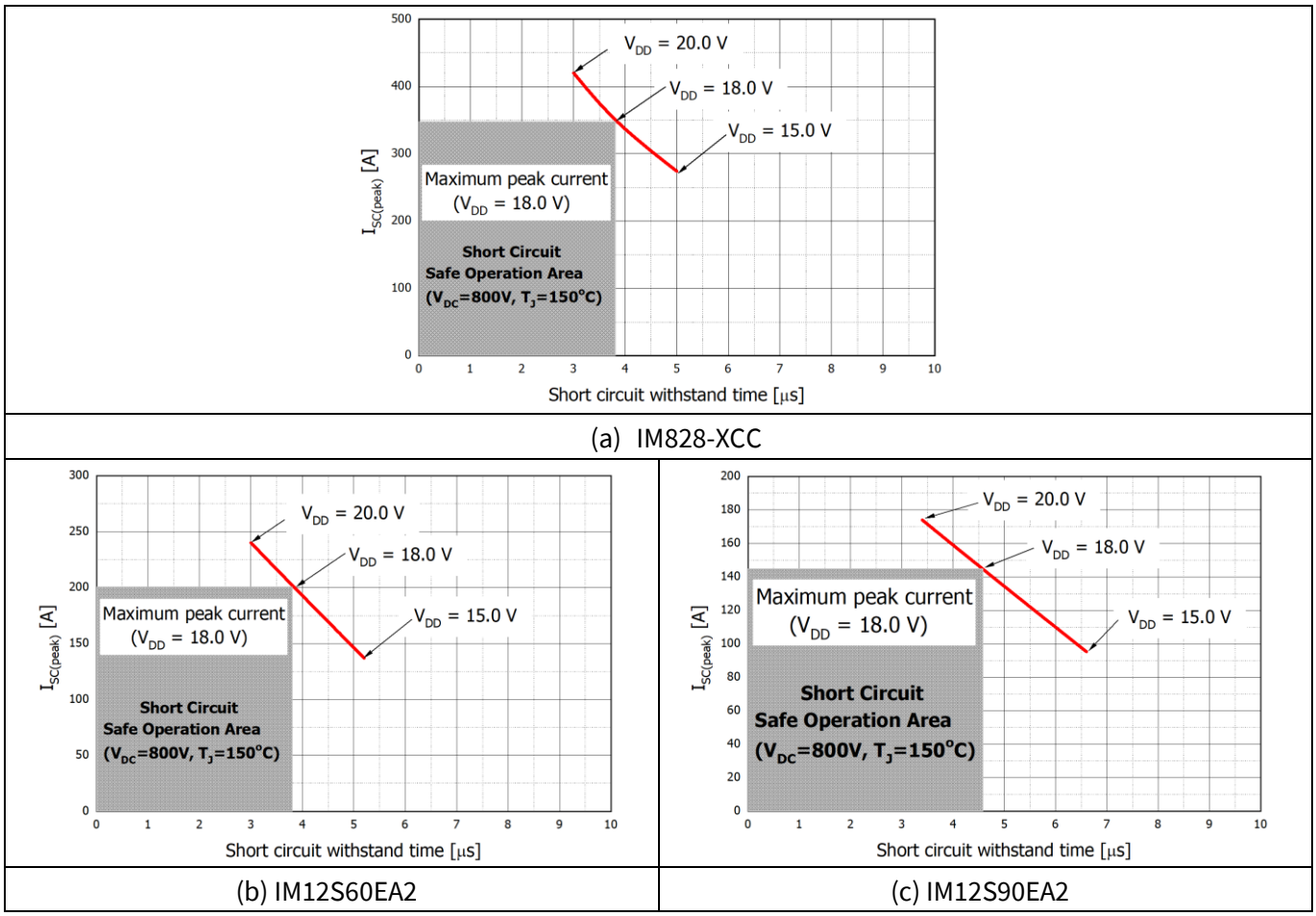


Figure 13 Typical reverse recovery losses (left) and reverse recovery current (right) as a function of diode current slope for IM828-XCC

3.3.2.3 Typical SCSOA(short-circuit safe operation area) characteristics

Figure 14 shows the typical (not guaranteed) SCSOA performance graph of 1200 V CIPOS™ Maxi CoolSiC™ MOSFET IPM products under the short circuit status with the following conditions. In the case of IM828-XCC, the graph illustrates that if the short circuit time is less than 3.8 µs, the SiC MOSFET has the ability to turn off safely. In this case, the SiC MOSFET can shut down an SC current (non-repetitive) about 346 A_{peak} under a control supply voltage of 18.0 V. Figure 15 shows typical SC (short circuit) waveform at DC link voltage V_{DC} = 800 V, control power supply voltage V_{DD} = 15 V / 18 V, and T_J = 150 °C.



(a) IM828-XCC

(b) IM12S60EA2

(c) IM12S90EA2

Figure 14 Typical SCSOA graph (at V_{DC} = 800 V, $V_{PN(surge)}$ < 1200 V, T_J = 150°C)

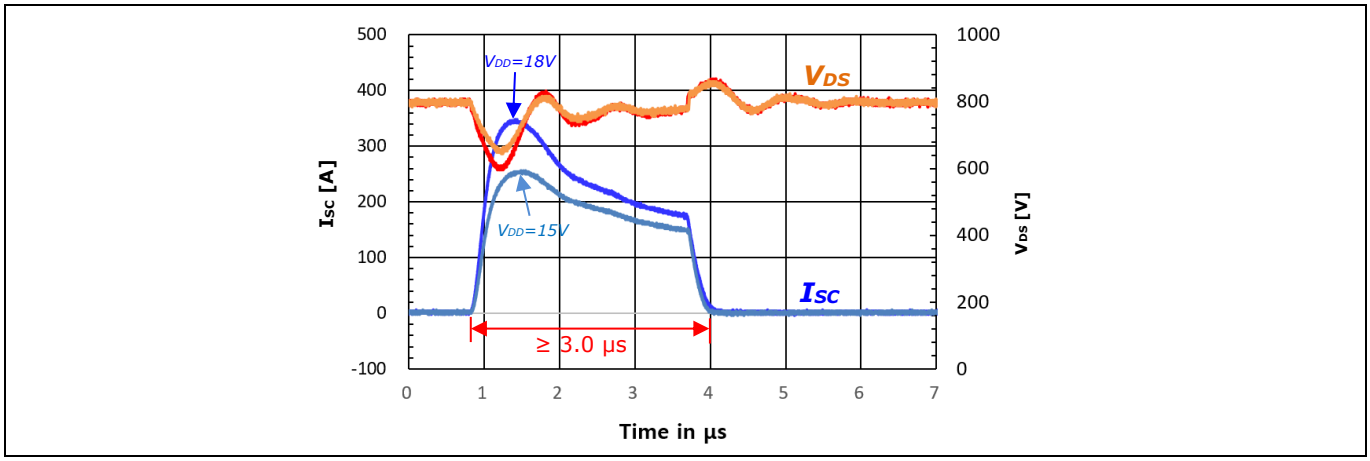


Figure 15 Typical short circuit (SC) waveform of IM828-XCC (V_{DC} = 800 V, V_{DD} = 15 V / 18 V, T_J = 150°C)

3.4 Description of the input and output pins

Table 11 defines the 1200 V CIPOS™ Maxi CoolSiC™ MOSFET IPM input and output pins. The detailed functional descriptions are as follows:

Table 11 Pin descriptions of IPM

Pin Number	Pin Name	Pin Description
1	VS(U)	U-phase high side floating IC supply offset voltage
2	VB(U)	U-phase high side floating IC supply voltage
3	VS(V)	V-phase high side floating IC supply offset voltage
4	VB(V)	V-phase high side floating IC supply voltage
5	VS(W)	W-phase high side floating IC supply offset voltage
6	VB(W)	W-phase high side floating IC supply voltage
7	HIN(U)	U-phase high side gate driver input
8	HIN(V)	V-phase high side gate driver input
9	HIN(W)	W-phase high side gate driver input
10	LIN(U)	U-phase low side gate driver input
11	LIN(V)	V-phase low side gate driver input
12	LIN(W)	W-phase low side gate driver input
13	VDD	Low side control supply
14	RFE	Programmable fault clear time, fault output, enable input
15	ITRIP	Overcurrent shutdown input
16	VSS	Low side control negative supply
17	VTH	NTC thermistor terminal
18	NW	W-phase low side source
19	NV	V-phase low side source
20	NU	U-phase low side source
21	W	Motor W-phase output
22	V	Motor V-phase output
23	U	Motor U-phase output
24	P	Positive bus input voltage

High-side bias voltage pins for driving the MOSFET

Pins: VB (U, V, W) – VS (U, V, W)

- These pins provide the gate-drive power to the high-side MOSFETs.
- The ability to utilize a bootstrap circuit scheme for the high-side MOSFETs eliminates the need for external power supplies.
- Each bootstrap capacitor is charged from the VDD supply during the ON-state of the corresponding low-side MOSFET or the freewheeling state of the low-side body diode.

- To prevent malfunctions caused by noise and ripple in the supply voltage, a good-quality (low ESR, low ESL) filter capacitor should be mounted very close to these pins.

Low side-bias voltage pin

Pin: VDD

- This is the control supply pin for the internal IC.
- To prevent malfunctions caused by noise and ripples in the supply voltage, a good-quality (low ESR, low ESL) filter capacitor should be mounted very close to this pin.

Low-side, common-supply ground pin

Pin: VSS

- This pin connects the control ground for the internal IC.

Signal input pins

Pins: HIN (U, V, W), LIN (U, V, W)

- These are pins used to control the operation of the internal MOSFETs.
- They are activated by voltage input signals. The terminals are internally connected to a Schmitt trigger circuit composed of 3.3 V/5 V-class CMOS.
- The signal logic of these pins is active-high. The MOSFET associated with each of these pins will be turned "ON" when a sufficient logic voltage is applied to these pins.
- The wiring of each input should be as short as possible to protect the IPM against noise influences.
- To prevent signal oscillations, an RC coupling is recommended as illustrated in Figure 19.

Overcurrent detection pin

Pin: ITRIP

- The current sensing shunt resistor should be connected between the N pin (source of low-side MOSFET) and the power ground to detect short-circuit current (refer to Figure 24). An RC filter should be connected between the shunt resistor and the ITRIP pin to eliminate noise.
- The integrated comparator is triggered if the voltage V_{ITRIP} is higher than 0.5 V. The shunt resistor should be selected to meet this level for the specific application. In case of a trigger event, the voltage at the RFE pin is pulled down to LOW.
- The connection length between the shunt resistor and ITRIP pin should be minimized.

Fault output, fault-clear time, and enable pin

Pin: RFE

- The fault-out indicates a module failure in case of undervoltage at pin VDD or in case of triggered overcurrent detection at ITRIP. The alarm conditions are overcurrent detection and low-side bias UV (undervoltage) operation.
- The programmable fault-clear time can be adjusted by the RC network, which is an external pull-up resistor and capacitor. For example, the typical value is about 1 ms at 1 MΩ and 2 nF.
- The microcontroller can pull this pin low to disable the IPM functionality. This is the enable function.

NTC thermistor terminal pin

Pin: VTH

- This is the NTC thermistor terminal pin
- This pin provides direct access to the NTC thermistor, which is referenced to VSS. An external pull-up resistor connected to +5 V ensures that the resulting voltage can be directly connected to the microcontroller.

Positive DC-link pin

Pin: P

- This is the DC-link positive-power supply pin.
- It is internally connected to the collectors of the high-side MOSFETs.
- To suppress the surge voltage caused by the DC-link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin. (Typically, metal film capacitors are used.)

Negative DC-link pins

Pins: NU, NV, NW

- These are the DC-link negative-power supply pins (power ground) of the inverter.
- These pins are connected to the low-side MOSFETs sources of each phase.

Inverter power output pins

Pins: U, V, W

- Inverter output pins for connecting to the inverter load (e. g. motor).

3.5 Outline drawing

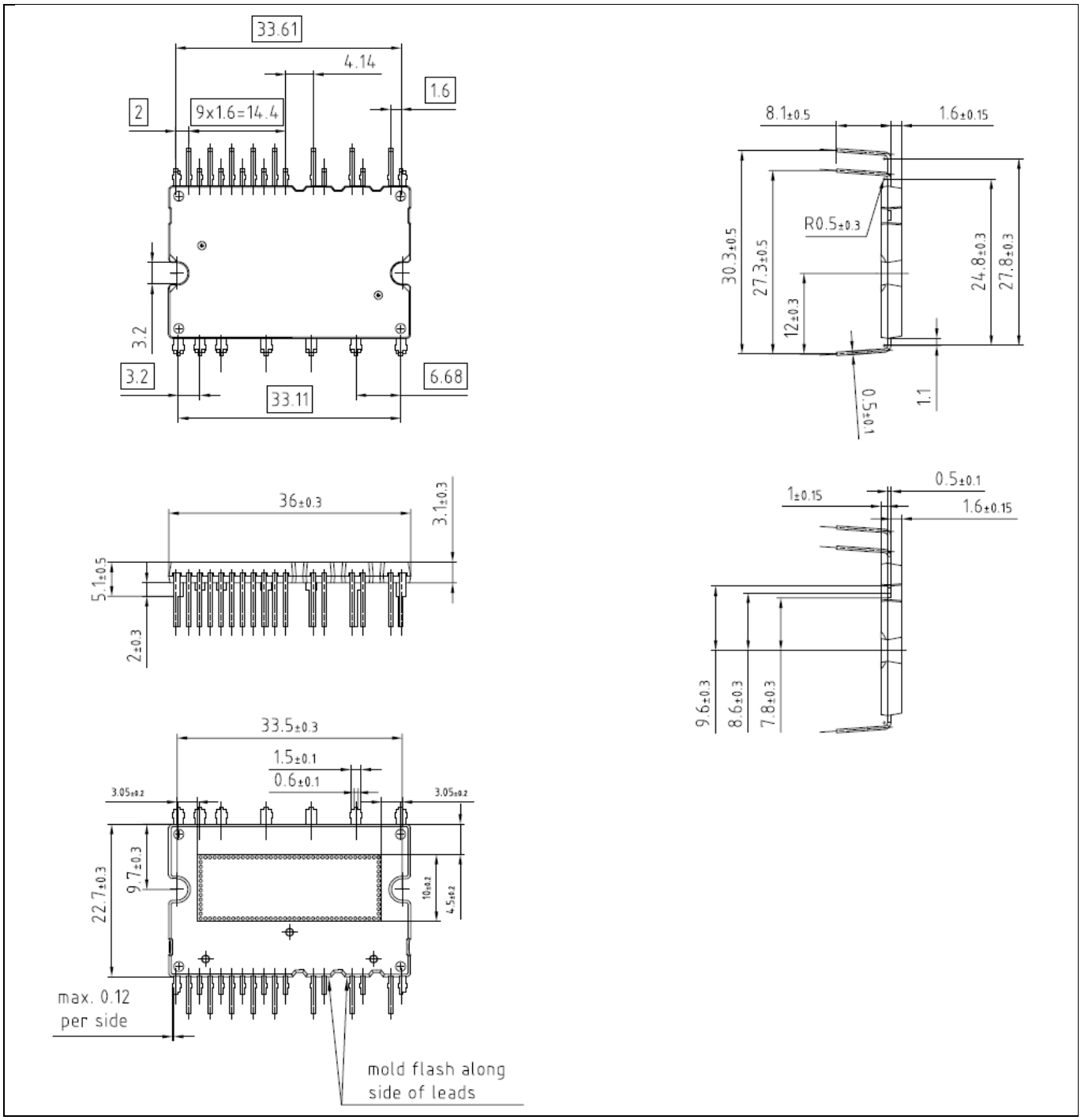
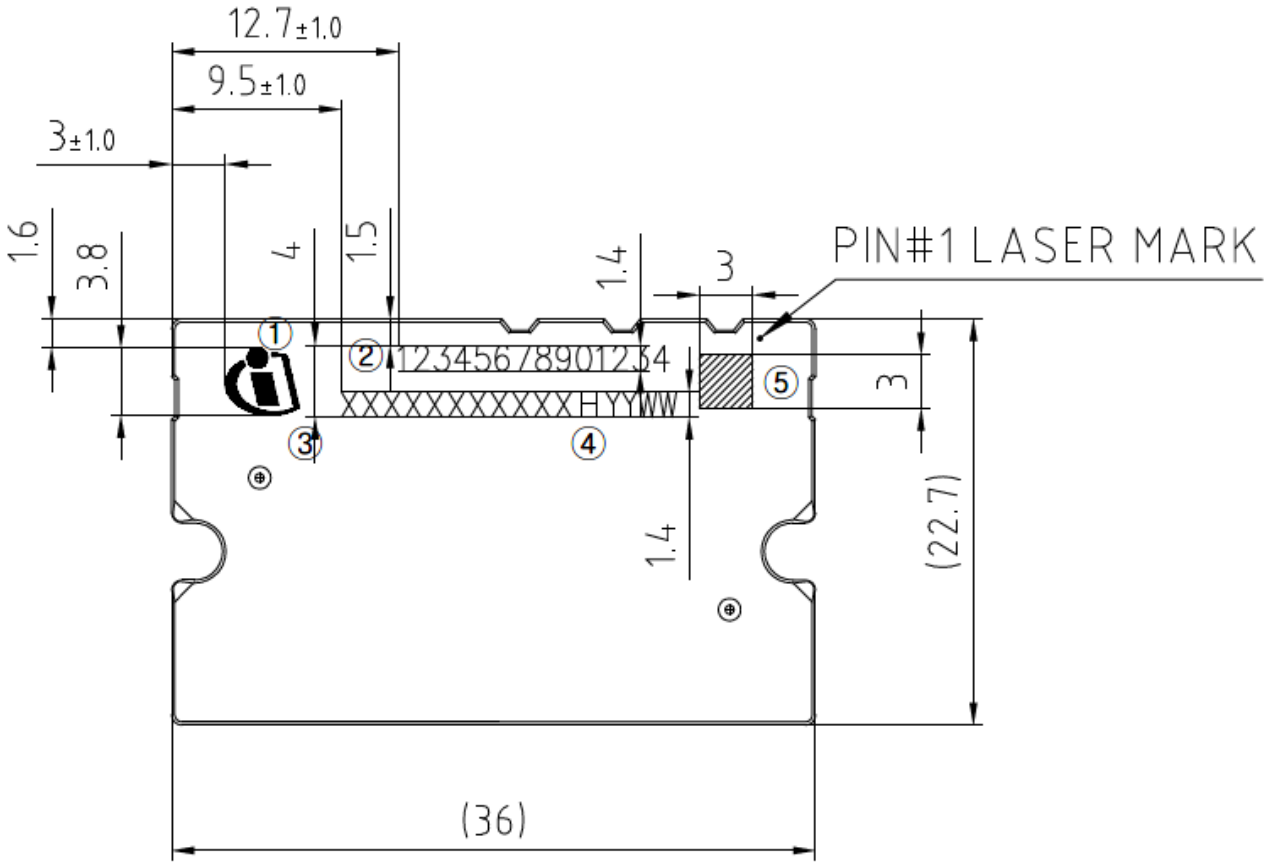


Figure 16 Package outline dimensions (Unit: [mm])

3.6 Marking Information

Figure 17 shows the laser marking specifications for CIPOS™ Maxi IPM. The company logo, the device type, the lot number, the date code, and the matrix code (2D) are marked on the upper side of the module.



<MARKING INFORMATION>

① : Company Logo

② : Product(Device) name

③ : Lot number

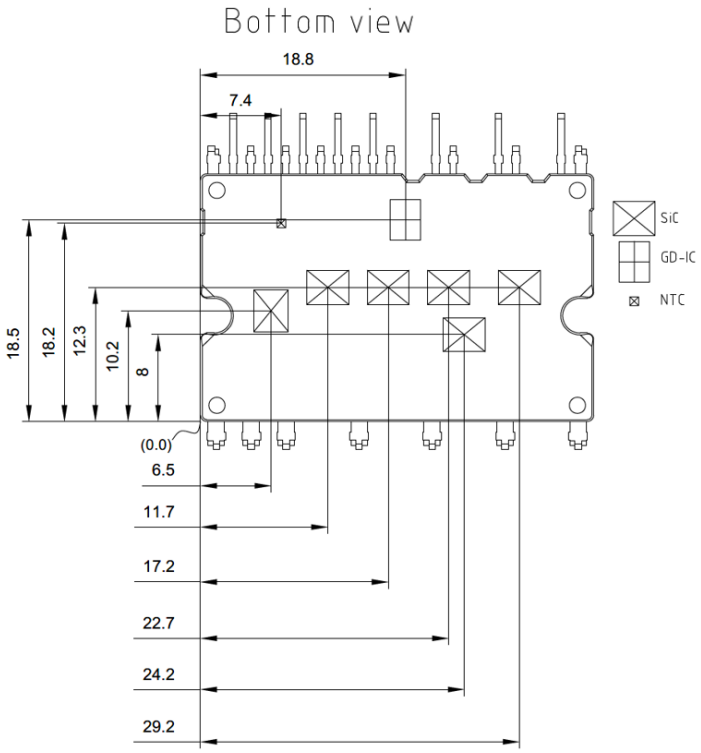
④ : Date code

⑤ : Data-matrix code

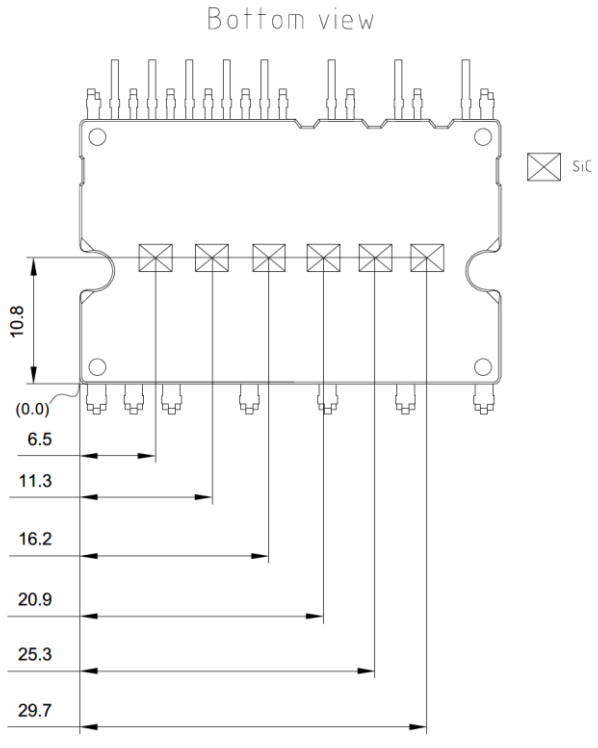
DATA MATRIX CODE 47x47 DOTS (3x3mm)
(DOT SIZE: 0.0638 mm)

Figure 17 Marking information

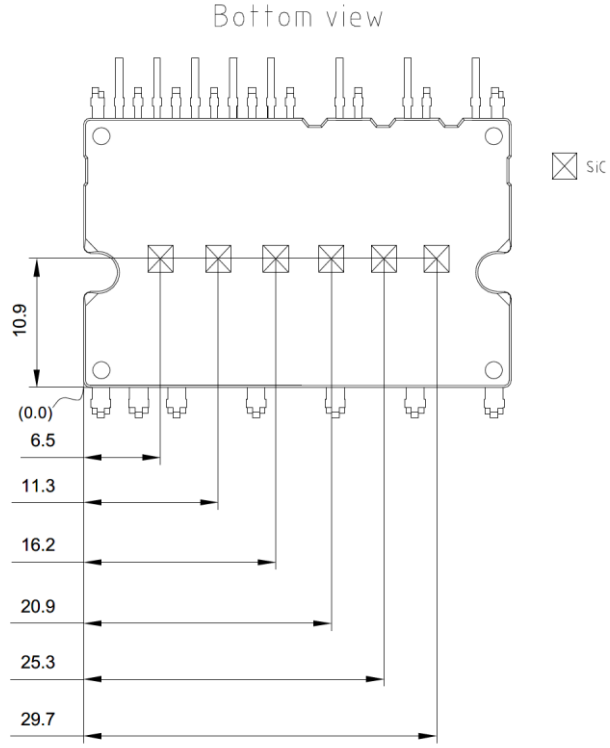
3.7 Chip Position



(a) IM828-XCC



(a) IM12S60EA2



(b) IM12S90EA2

Figure 18 Chip Position (Unit: [mm])

4 Interface circuit and layout guide

4.1 Input signal connection

Figure 19 shows the I/O interface circuit between micro-controller and IPM. The IPM input logic is active-high with internal pull-down resistors. External pull-down resistors are not needed.

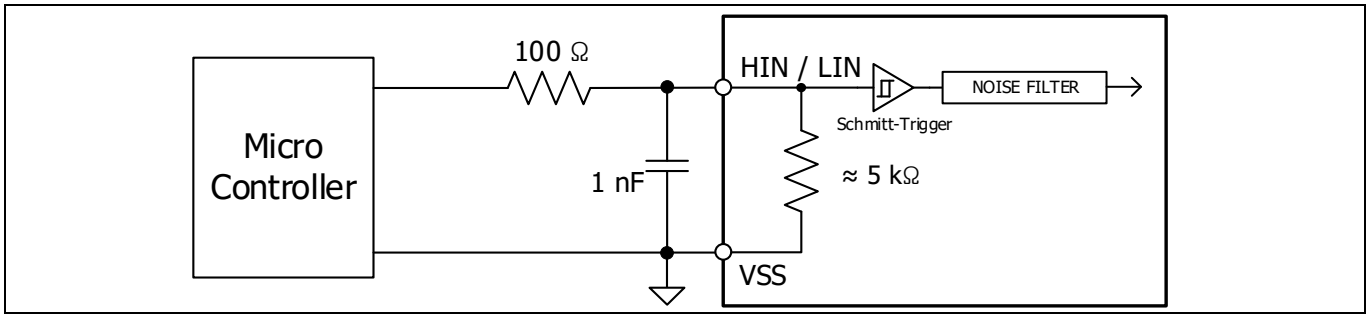


Figure 19 Recommended micro-controller I/O interface circuit

Table 12 Maximum ratings of inputs

Item	Symbol	Condition	Value	Unit
Module supply voltage	V_{DD}	Applied between VDD – VSS	-1 ~ 20	V
High- side floating supply voltage	V_{BS}	Applied between VB (U,V,W) – VS (U,V,W)	-1 ~ 20	V
Input voltage	V_{IN}	Applied between HIN (U,V,W) – VSS, LIN (U,V,W) – VSS	-1 ~ V_{DD}+0.3	V

The input maximum rating voltages are listed in Table 12. Since the input voltage rating is VDD + 0.3 V, a 15 V supply interface is possible. However, it is recommended that the input signal be configured with the 5 V or 3.3 V logic supply for direct connect with the micro-controller. It is recommended to place bypass capacitors as close as possible to the signal lines from the micro-controller as well as the IPM.

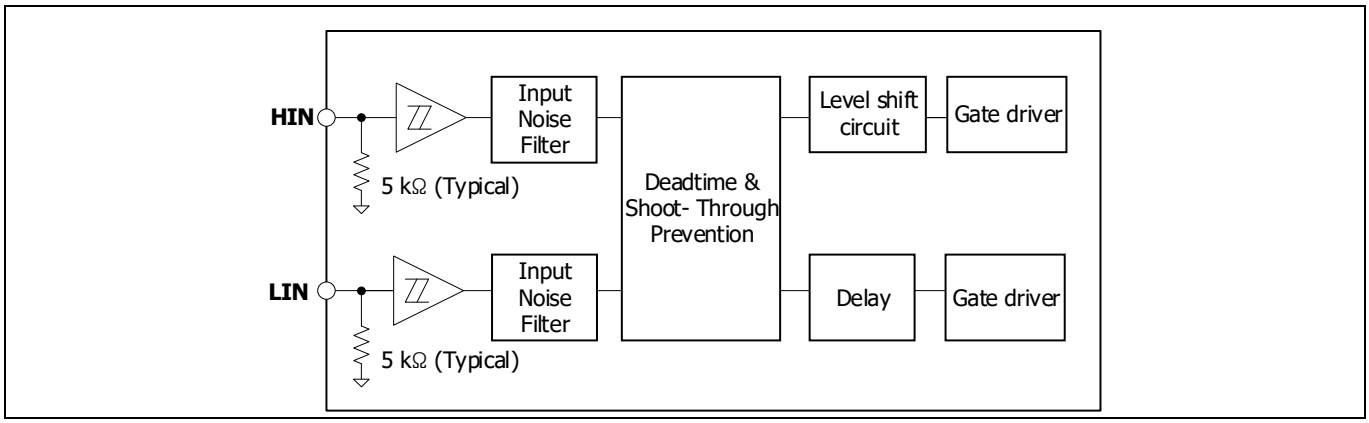


Figure 20 Simplified block diagram of IPM gate driver IC

Because IPM employ active-high input logic, the power sequence restriction between the control supply and the input signal during start-up or shut-down operation does not exist. Therefore, it makes the system fail-safe. In addition, pull-down resistors are built into each input circuit. Thus, external pull-down resistors are not needed. This reduces the required external component count. Input Schmitt-trigger, noise filter, deadtime and

shoot-through prevention functions provide beneficial noise rejection to short input pulses. Furthermore, the inputs of IPM are compatible with standard CMOS and TTL outputs. The gate driver IC of IPM has been designed to be compatible with 3.3 V and 5 V logic-level signals. Therefore, by lowering the turn-on and turn-off threshold voltage of the input signal as shown in Table 13, a direct connection to 3.3 V / 5 V-class micro-controller or DSP is possible.

Table 13 Input threshold voltage (at VDD = 15 V, T_J = 25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic "1" input voltage (LIN, HIN)	V_{IH}	HIN – VSS	-	1.9	2.3	V
Logic "0" input voltage (LIN, HIN)	V_{IL}	LIN – VSS	0.7	0.9	-	V

As shown in Figure 20, the IPM input signal section integrates a 5 kΩ (typical) pull-down resistor. Therefore, when using an external filtering resistor between micro-controller output and IPM input, pay attention to the signal voltage drop at the IPM input terminals. It should fulfill the logic "1" input voltage requirement. For instance, R = 100 Ω and C = 1 nF for the parts shown in Figure 19.

4.2 Internal deadtime

The gate driver IC of IPM features integrated deadtime protection circuitry. The deadtime for gate driver IC is fixed. The deadtime feature inserts a time period (a minimum deadtime) in which both the high- and low-side power switches are held off; this is done to ensure that the power switch being turned off has fully turned off before the second power switch is turned on.
This minimum deadtime is automatically inserted whenever the external deadtime is shorter than DT_{IC}; external deadtimes larger than DT_{IC} are not modified by the gate driver IC.

Table 14 Internal deadtime (at VDD = 15 V, T_J = 25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal deadtime	DT_{IC}	V_{IN} = 0 or V_{IN} = 5 V	300	-	-	ns

4.3 Anti-cross conduction circuitry

The gate driver IC of IPM is equipped with shoot-through protection circuitry (also known as anti-cross conduction circuitry or interlock circuitry). Figure 21 shows how this protection circuitry prevents both the high- and low-side switches from conducting at the same time.

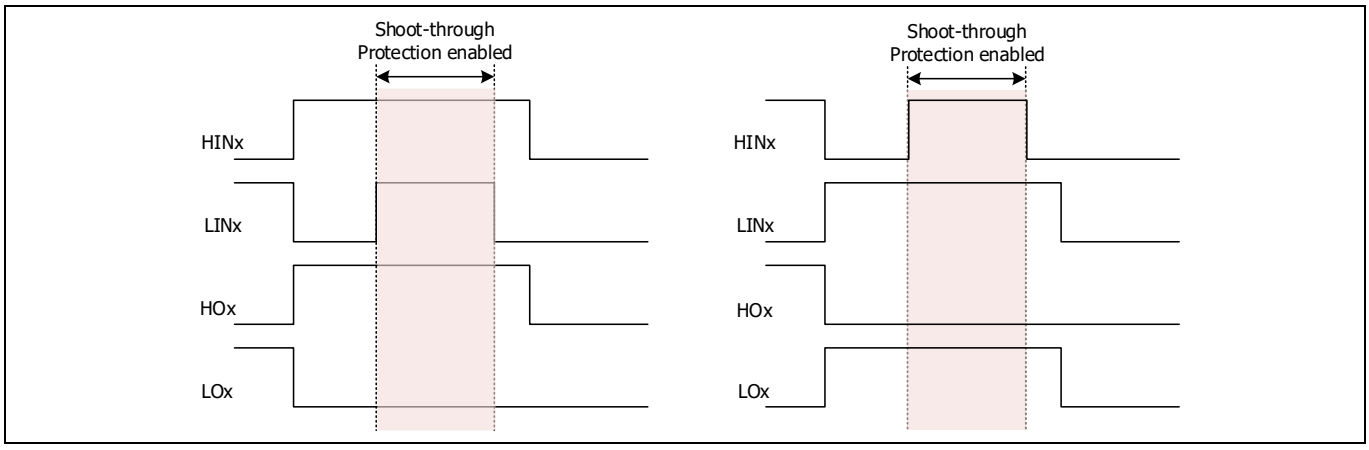


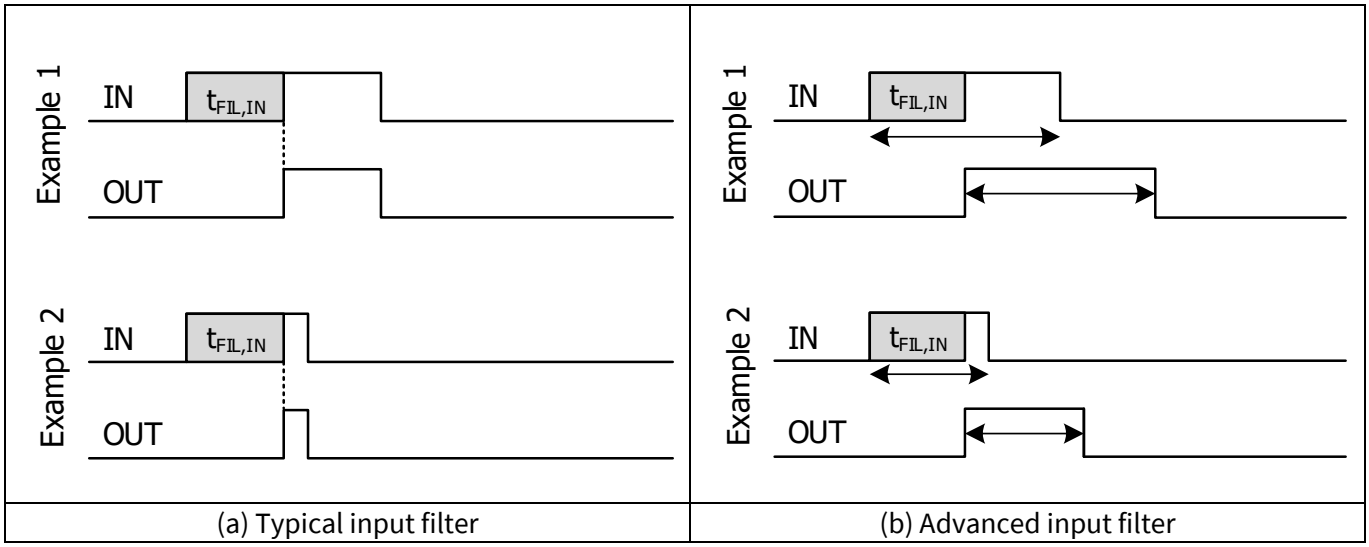
Figure 21 Illustration of shoot-through protection circuity

4.4 Advanced input filter

The advanced input filter allows an improvement in the input/output pulse symmetry of the gate driver IC and helps to reject noise spikes and short pulses. This input filter has been applied to the HIN and LIN inputs. The working principle of the new filter is shown in Figure 22 (a), (b).
Figure 22 (a) shows a typical input filter and the asymmetry of the input and output. The upper pair of waveforms (Example 1) show an input signal width with a duration much longer then $t_{FIL,IN}$; the resulting output is approximately the difference between the input signal and $t_{FIL,IN}$. The lower pair of waveforms (Example 2) show an input signal with a duration slightly longer then $t_{FIL,IN}$; the resulting output is approximately the difference between the input signal and $t_{FIL,IN}$.
Figure 22 (b) shows the advanced input filter of IPM and the symmetry between the input and output. The upper pair of waveforms (Example 1) show an input signal with a duration much longer then $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal. The lower pair of waveforms (Example 2) show an input signal with a duration slightly longer then $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal.

Table 15 Input filter time (at VDD = 15 V, T_J = 25 ℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input filter time at LIN, HIN for turn-on and off	$t_{FIL,IN}$	$V_{LIN, HIN}$ = 0 V or 5 V	-	350	-	ns



(a) Typical input filter (b) Advanced input filter

Figure 22 Internal Input filter characteristics

4.5 Matched propagation delay

The gate driver IC of IPM is designed with propagation-delay matching circuitry. With this feature the internal gate driver IC's response at the output to a signal at the input requires approximately the same time duration (i.e., t_{ON}, t_{OFF}) for both the low-side channels and the high-side channels; the maximum difference is specified by the delay-matching parameter (M_T). The propagation turn-on delay (t_{ON}) of the IPM is matched to the propagation turn-off delay (t_{OFF}). In other words, delay-matching turn-on/off between high-side and low-side means there is the time difference between the LO and HO outputs, when each output has reached 10% of its maximum (during turn-on), or when each output has decreased to 90% of its maximum (during turn-off), assuming that HINx and LINx are simultaneously applied. The shorter the delay-matching time, the better the circuit performance.

Table 16 Matching propagation delay time (at VDD = 15 V, T_J = 25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Matching propagation delay time (On & Off) all channels	M_T	External deadtime > 500 ns	-	-	130	ns

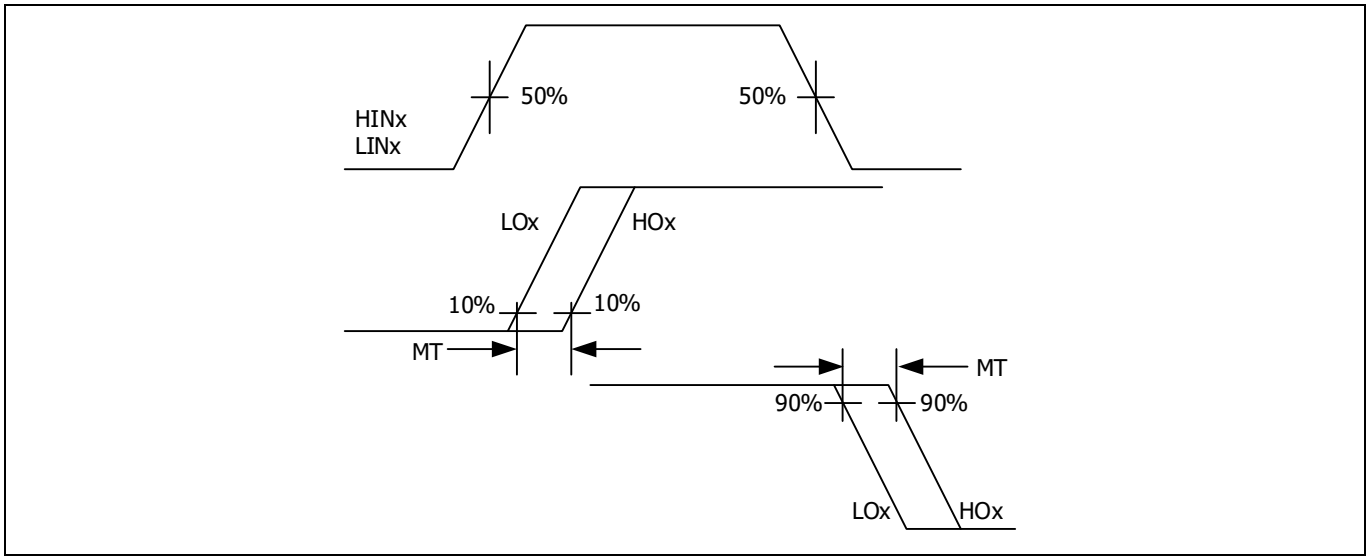


Figure 23 Delay-matching waveform definition

4.6 General interface circuit example

Figure 24 shows a typical application circuit of IPM for interface schematic with control signals connected directly to a micro-controller.

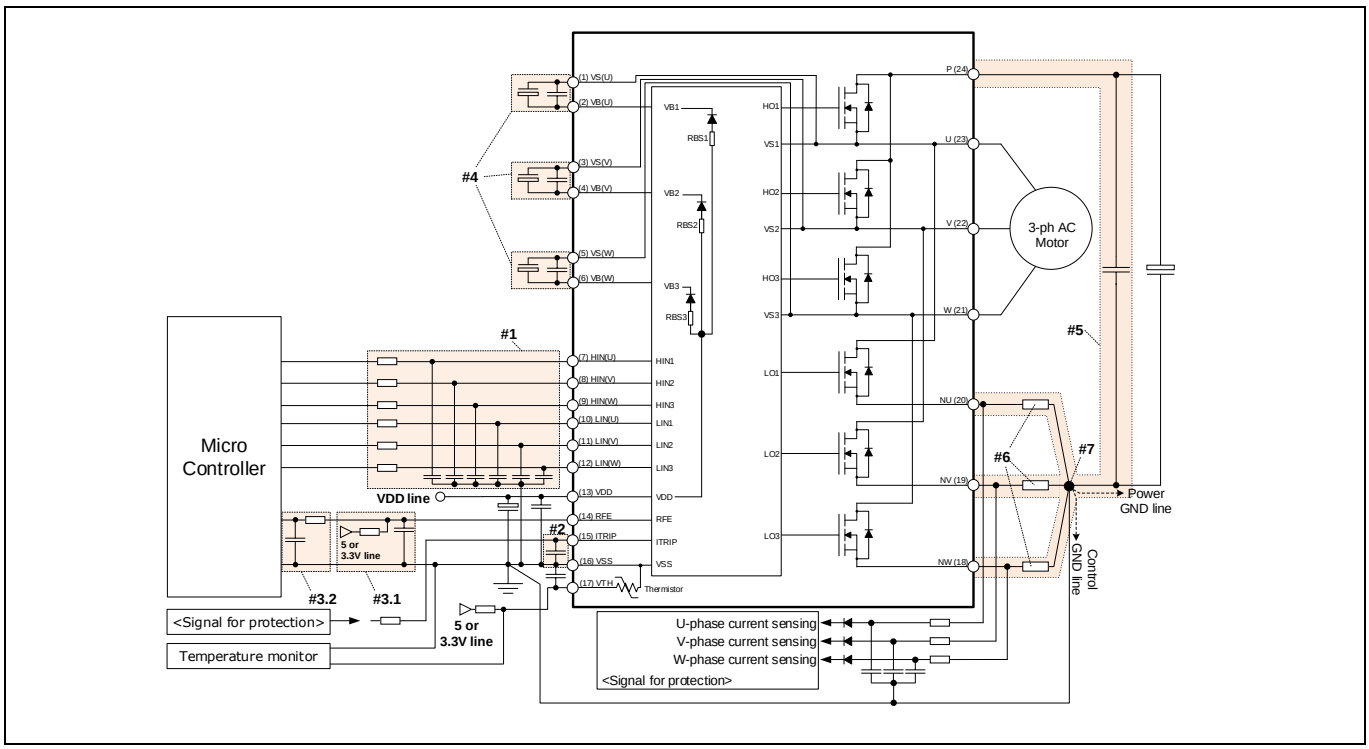


Figure 24 Application circuit example

Note:

1. Input circuit
   - To reduce input signal noise by high-speed switching, the R_{IN} and C_{IN} filter circuit should be mounted. (100 Ω, 1 nF)
   - C_{IN} should be placed as close to VSS pin as possible.
2. Itrip circuit
   - To prevent protection function errors, C_{ITRIP} should be placed as close to ITRIP and VSS pins as possible.
3. RFE circuit

   3.1 Pull-up resistor (R_{RFE}) and pull-down capacitor (C_{RFE})
   - RFE output is an open-drain output. This signal line should be pulled up to the positive side of the 5 V / 3.3 V logic power supply (V_{CTR}) with a proper resistor R_{RFE}.
   - The fault-clear time is adjusted by RC network of a R_{RFE}, a C_{RFE} and V_{CTR}.
     - $t_{FLTCLR} = -R_{RFE} \cdot C_{RFE} \cdot \ln(1 - V_{RFE,TH+} / V_{CTR}) +$ internal fault-clear time 160 µs
     - $t_{FLTCLR} = -2\ M\Omega \times 1\ nF \times \ln(1 - 1.9 / 5\ V) + 160\ \mu s \cong 1.1$ ms at R = 2 MΩ, C = 1 nF and $V_{pull\text{-}up} = 5$ V
     - A pull-up resistor is limited to max. 2 MΩ
     - In case of V_{CTR} is higher than 5 V, the R_{RFE} needs to be at least 200 kΩ to limit the IC power dissipation

   3.2 RC filter
   - It is recommended that the RC filter be placed as close to the controller as possible.
4. VB-VS circuit
   - Capacitor for high-side floating supply voltage should be placed as close to VB and VS pins as possible.
5. Snubber capacitor
   - The wiring between IPM and snubber capacitor including shunt resistor should be as short as possible.
6. Shunt resistor
   - The shunt resistor of SMD type should be used for reducing its stray inductance. (non-inductive resistance)
7. Ground pattern
   - Ground pattern should be separated at only one point of shunt resistor as short as possible.

4.7 Recommended rated output current of power supply

Control and gate drive power for the IPM is normally provided by a single 15 V supply that is connected to the module VDD and VSS terminal. The circuit current of VDD control supply of IM828-XCC is shown in below Table 17.

Table 17 The circuit current of control power supply of IM828-XCC (Unit: [mA])

Item		Static (typ.)	Dynamic (typ.)	Total (typ.)
VDD = 15 V	FSW = 5 kHz	1.45	3.08	4.53
	FSW = 10 kHz	1.45	3.81	5.26
	FSW = 20 kHz	1.45	5.28	6.73
	FSW = 40 kHz	1.45	8.20	9.65
VDD = 20 V	FSW = 60 kHz	2.53	15.77	18.30

And the circuit current of the 5 V logic power supply (RFE & input terminals) is about 5 mA.

Finally, the recommended minimum circuit currents of power supply are shown in Table 18 which takes into consideration ripple current and sufficient margins at the worst conditions, e.g. 5 times higher than the calculated value.

Table 18 The recommended minimum circuit current of power supply (Unit: [mA])

Item	The circuit current of +15 V control supply	The circuit current of +5 V logic supply
VDD ≤ 20 V, FSW ≤ 20 kHz	98.0	25.0

4.8 Recommended layout pattern

4.8.1 OCP & SCP function

It is recommended that the ITRIP filter capacitor connections to the IPM pins be as short as possible. The ITRIP filter capacitor should be connected to the VSS pin directly without overlapped ground pattern. The signal ground and power ground should be as short as possible and connected at only one point via the filter capacitor of VDD line.

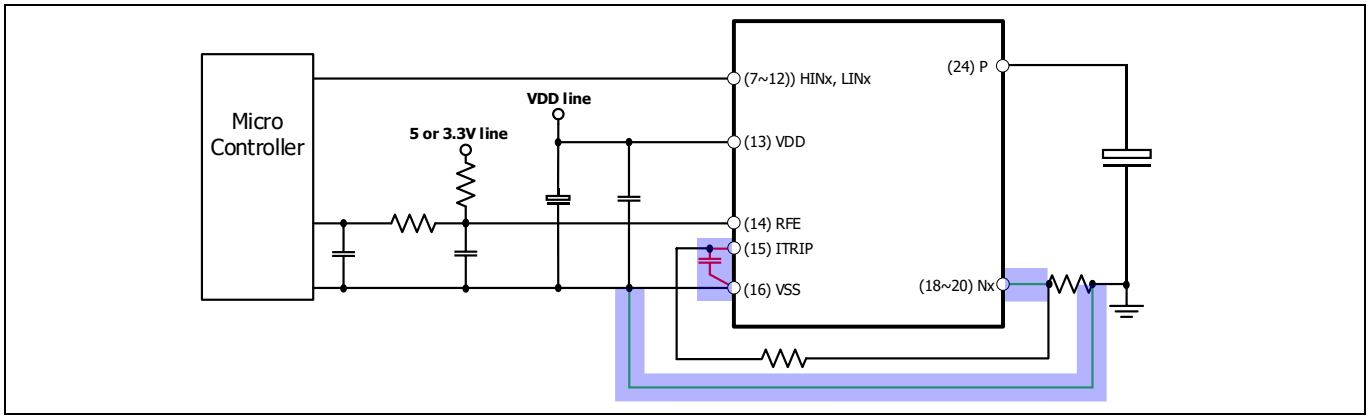


Figure 25 Recommended layout pattern for OCP & SCP function

4.8.2 Power line

Probably the most important parasitic components which must be considered for the development of a power electronic application are the stray inductance. A stray inductance is a consequence of internal and external connections between the semiconductor devices and the power electronic system. Figure 26 shows internal stray inductance of IPM (left figure) by bonding wire, DCB pattern, and lead frame and example of external stray inductance between IPM and system board (right figure).

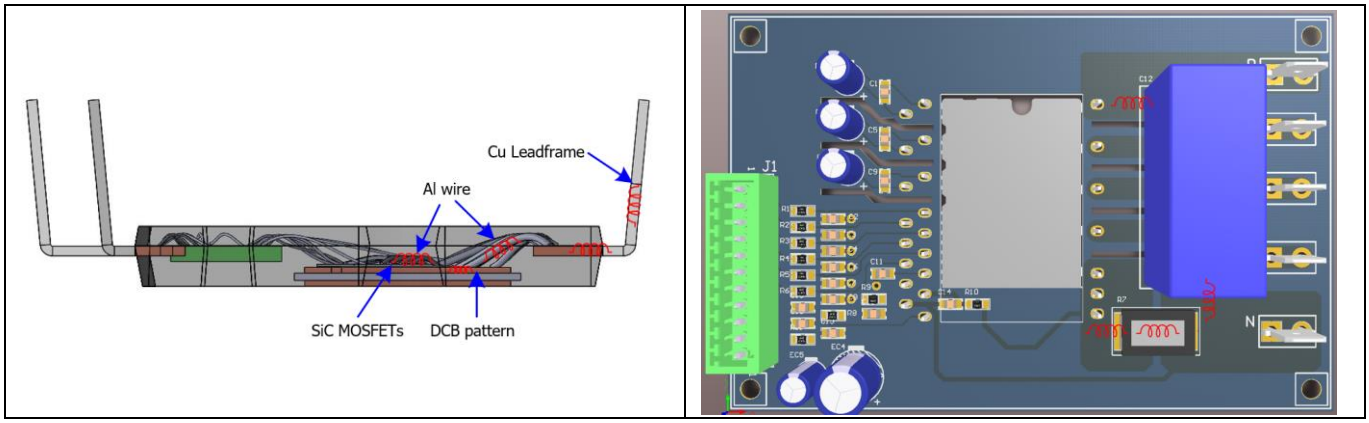


Figure 26 Internal stray inductance parameter (left) and possible external stray inductance parameters (right)

During a switching event a voltage drop across an inductor is calculated by the following equation.

$$\Delta V = L \times di/dt.$$

This voltage drop has influence on the turn-on and turn-off behavior of IM828-XCC. Figure 27 shows the turn-on and turn-off switching waveforms according to the stray inductance. The voltage drop during turn-on leads to a drop of V_{DS} leading to a reduction of the turn-on energy. During the turn-off of the device, the voltage leads to an increase of the voltage spike. If this voltage increase is larger than the device breakdown voltage the device will fail and the IPM will be destructed. Consequently, the turn-off of a power device is the critical event to look at with respect to an IM828-XCC stray inductance. Table 19 shows switching characteristics with different stay inductance.

As 1200 V CoolSiC™ MOSFET is much faster than Si IGBT within the same voltage class, SiC MOSFET with large stray inductance is limiting the use of SiC MOSFET with respect to the maximum allowed switching speed and/or applied voltages. However, IM828-XCC have relatively lower switching speeds (di/dt and dv/dt) for motor drive applications via optimized gate driver IC design. Therefore, IM828-XCC is relatively less affected by stray inductance. However, the turn-off switching speed of IM828-XCC is still much faster than Si IGBT IPM. So, larger stray inductance is able to induce larger voltage spikes as shown in Figure 27, which might cause device destruction. That is why users must reduce the stray inductance as much as possible.

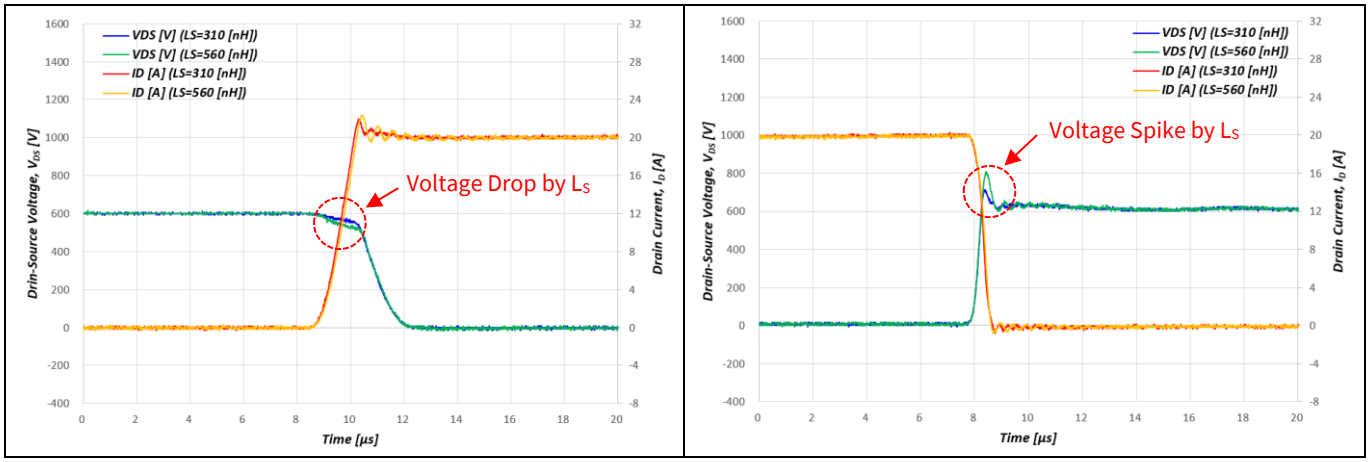


Figure 27 Turn-on(left) and Turn-off(right): Switching waveform comparison with different stray inductance, L_S (V_{DC} = 600 V, V_{DD} = 15 V, I_D = 20 A, T_J = 25 °C, inductive load = 3 mH)

Table 19 Switching characteristics with external stray inductance

	Total stray inductance, L_S [nH]	Slew rate, di/dt [A/µs]	Voltage drop, V_D [V]	Switching loss, E_{ON} [µJ]
Turn-on	310	152.4	47.6	1673.0
	560	142.9	80.0	1580.0
	Total stray inductance, L_S [nH]	**Slew rate, di/dt [A/µs]**	**Voltage spike, V_S [V]**	**Switching loss, E_{OFF} [µJ]**
Turn-off	310	333.2	112.0	296.0
	560	333.3	198.0	342.0

4.9 Recommended wiring of shunt resistor and snubber capacitor

External current sensing resistors are applied to detect overcurrent of phase currents. A long wiring pattern between the shunt resistors and IPM will cause excessive surges that might damage the IPM's internal IC and current detection components. This may also distort the sensing signals. To decrease the pattern inductance, the wiring between the shunt resistors and IPM should be as short as possible.

As shown in Figure 28 snubber capacitors should be installed in the right location to suppress surge voltages effectively. Generally, a high frequency non-inductive capacitor of around 0.1 ~ 0.22 µF is recommended. If the snubber capacitor is installed in the wrong location '1' as shown in Figure 28, it cannot suppress the surge voltage effectively. If the capacitor is installed in location '2', the charging and discharging currents generated by wiring inductance and the snubber capacitor will appear on the shunt resistor. This will impact the current sensing signal and the SC protection level will be a little lower than the calculated design value. The "2" position surge suppression effect is greater than the location '1' or '3'. The '3' position is a reasonable compromise with better suppression than in location '1' without impacting the current sensing signal accuracy. For this reason, location '3' is generally used.

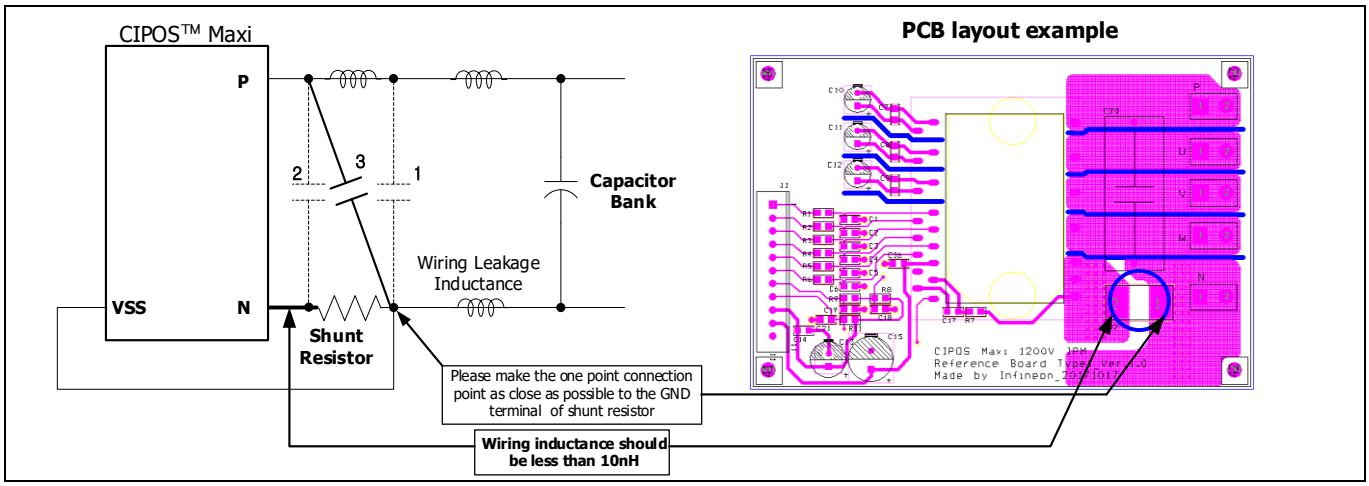


Figure 28 Recommended wiring of shunt resistor and snubber capacitor

4.10 Pin and screw hole coordinates for CIPOS™ Maxi IPM footprint

Figure 29 shows the IPM position on the PCB to indicate center coordinates of each pin and screw hole in Table 20.

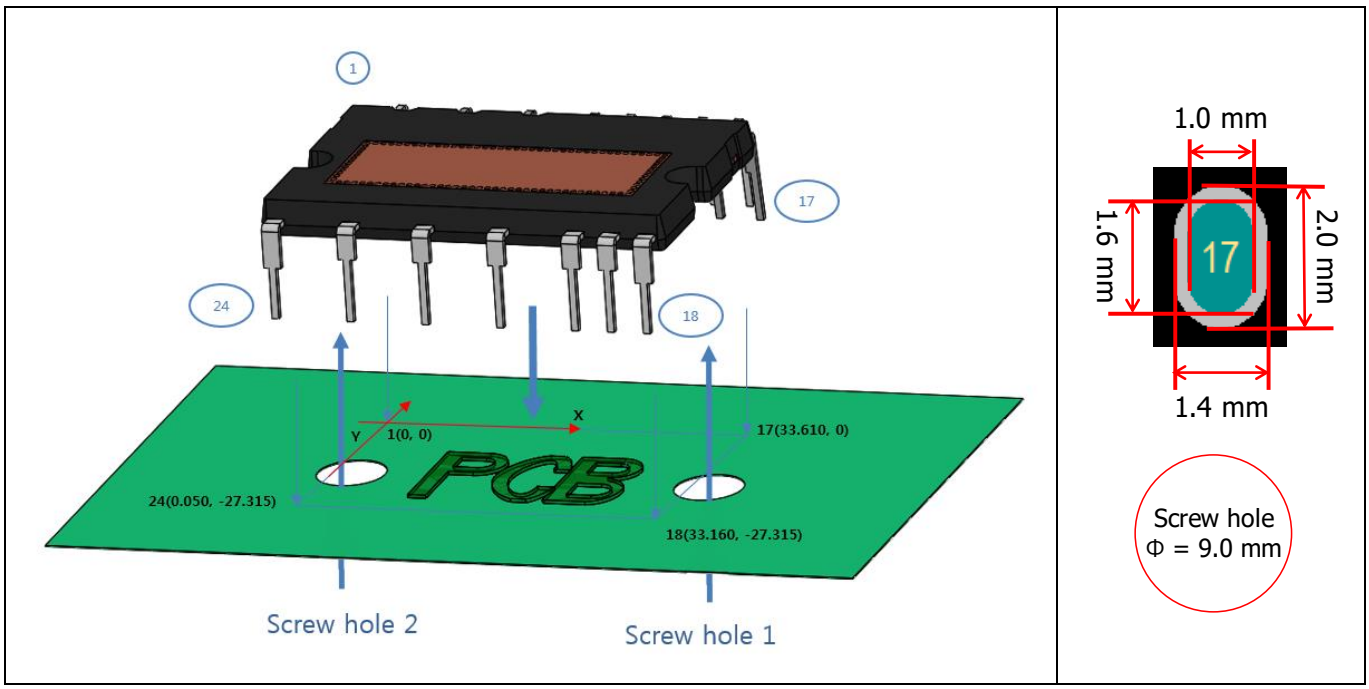


Figure 29 CIPOS Maxi IPM position on PCB (Unit: [mm]) and example of pad design(1~24pin)

Table 20 Pin & screw holes coordinates for IPM footprint (Unit: [mm])

Pin Number		X	Y	Pin Number		X	Y
Signal Pin	1	0.000	0.000	Signal Pin	14	28.410	2.997
	2	1.600	2.997		15	30.010	0.000
	3	5.737	0.000		16	31.610	2.997
	4	7.337	2.997		17	33.610	0.000
	5	11.473	0.000	Power Pin	18	33.160	-27.315
	6	13.073	2.997		19	29.960	-27.315
	7	17.210	0.000		20	26.760	-27.315
	8	18.810	2.997		21	20.083	-27.315
	9	20.410	0.000		22	13.405	-27.315
	10	22.010	2.997		23	6.728	-27.315
	11	23.610	0.000		24	0.050	-27.315
	12	25.210	2.997	Screw Hole	1	33.355	-15.308
	13	26.810	0.000		2	-0.145	-15.308

5 Protection features

5.1 Undervoltage protection

Control and gate drive power for the IPM is normally provided by a single 15 V supply that is connected to the module VDD and VSS terminals. For proper operation this voltage should be regulated to 15 V ± 10%. Table 21 describes the behavior of the IPM for various control supply voltages. The control supply should be well filtered with a low-impedance electrolytic capacitor and a high-frequency decoupling capacitor connected at the IPM's pins.

High-frequency noise on the supply might cause the internal control IC to malfunction and generate erroneous fault signals. To avoid these problems, the maximum ripple on the supply should be less than ± 1 V/µs.

The potential at the module's VSS terminal is different from that at the N power terminal by the voltage drop across the sensing resistor. It is very important that all control circuits and power supplies be referred to this point and not to the N terminal. If circuits are improperly connected, the additional current flowing through the sense resistor might cause improper operation of the short-circuit protection function. In general, it is best practice to make the common reference (V_{SS}) a ground plane in the PCB layout.

The main control power supply is also connected to the bootstrap circuits to generate the floating supplies for the high-side gate drives.

When control supply voltage (V_{DD} and V_{BS}) falls under UVLO (undervoltage lockout) level, MOSFETs will turn off while ignoring the input signal.

Table 21 The IPM functions versus control power supply voltage

Control Voltage Range [V]	Function operations
0 ~ 4	Control IC does not operate. Undervoltage lockout and fault output do not operate.
4 ~ 12.5	When the undervoltage lockout function is activated, control input signals are blocked, and a fault-out signal (V_{RFE}) is generated.
12.5 ~ 13.5	MOSFETs will be operated in accordance with the control gate input. Driving voltage is below the recommended range, so the $V_{DS(on)}$ and the switching losses will be larger than under normal conditions. And high-side MOSFETs cannot operate after V_{BS} initial charging, because V_{BS} cannot reach V_{BSUV+}.
13.5 ~ 18.0 for V_{DD} 12.5 ~ 18.0 for V_{BS}	Normal operation. This is the recommended operating condition. V_{DD} of 15 V is recommended when only integrated bootstrap circuitry is used.
18.0~ 20 for V_{DD}, V_{BS}	MOSFETs are still operated. Because driving voltage is above the recommended range, MOSFETs' switching is faster. It causes increasing system noise. And peak short-circuit current might be too large for proper operation of the short-circuit protection.
Over 20	Control circuit in the IPM might be damaged.

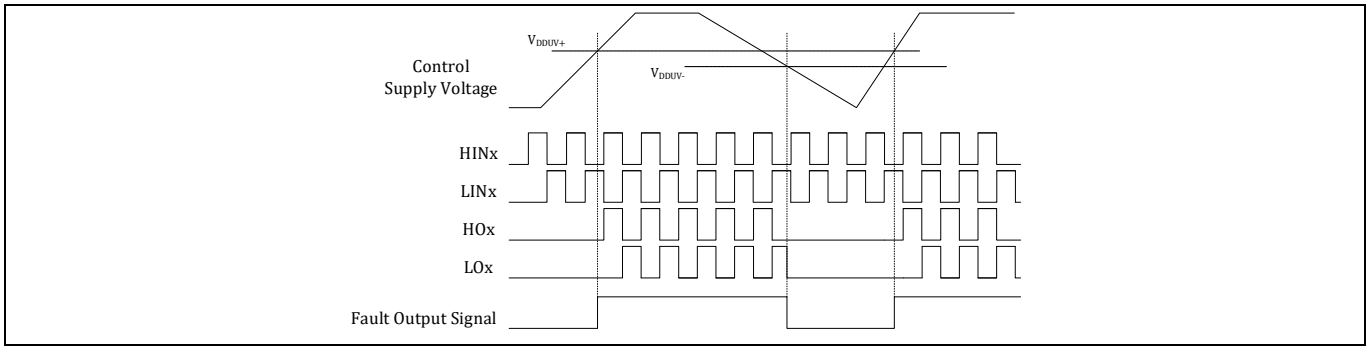


Figure 30 Timing chart of low-side undervoltage protection function

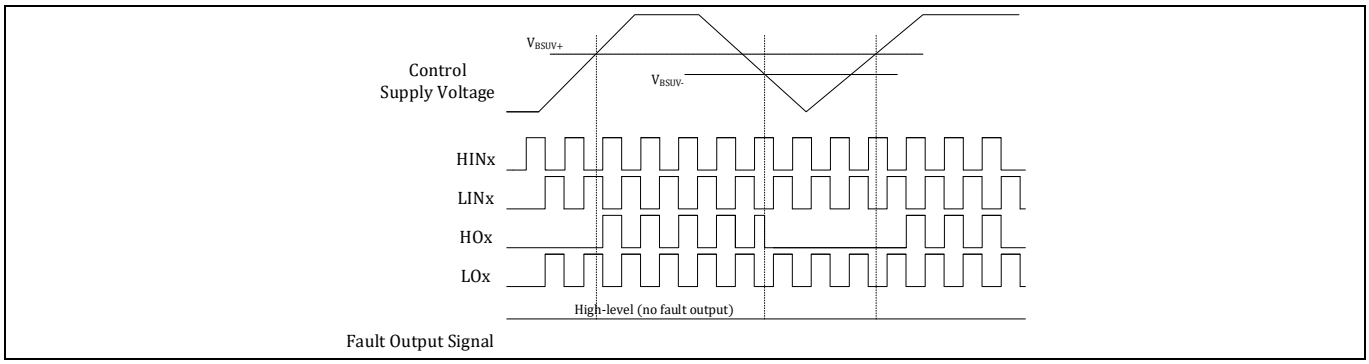


Figure 31 Timing chart of high-side undervoltage protection function

5.2 Overcurrent protection

5.2.1 Timing chart of overcurrent (OC) protection

The IPM has an overcurrent shutdown function. Its internal IC monitors the voltage of the ITRIP pin, and if this voltage exceeds the $V_{IT,TH+}$, which is specified in the device's datasheets, a fault signal is activated and all MOSFETs are turned off. Typically, the maximum short-circuit current magnitude is gate-voltage dependent. A higher gate voltage results in a larger short-circuit current. To avoid this potential problem, the maximum overcurrent trip level is usually set to below 2 times the nominal rated collector current. The overcurrent protection-timing chart is shown in Figure 32.

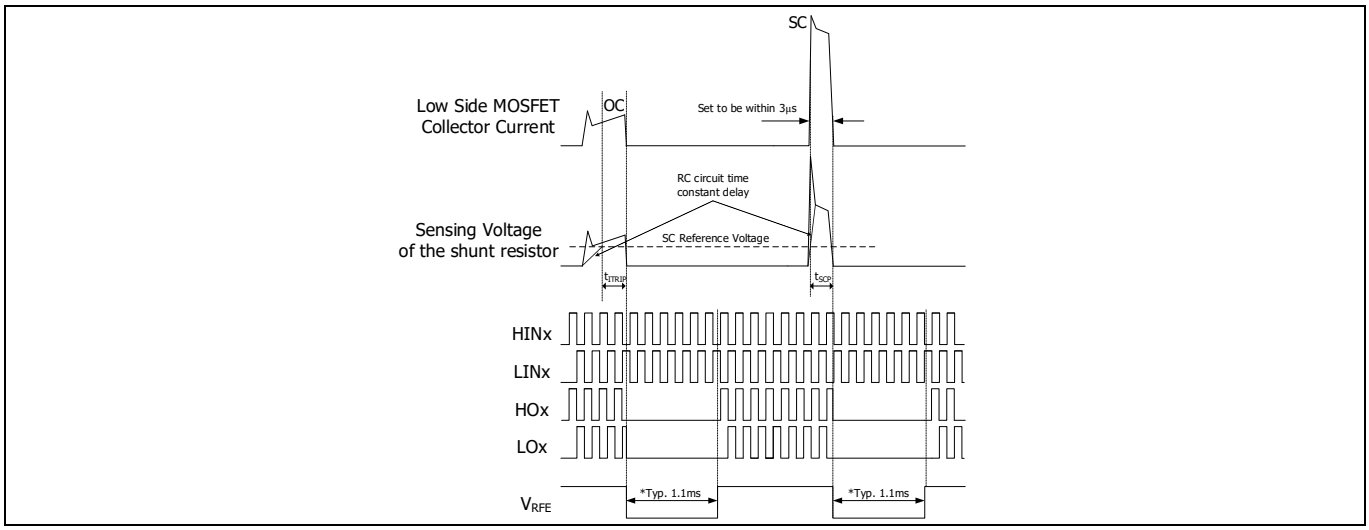


Figure 32 Timing chart of overcurrent protection function

(*$t_{FLT,CLR}$ is defined by R_{RCIN}, C_{RCIN}, please refer to Section 5.3)

5.2.2 Selecting current sensing shunt resistor

The value of the current sensing resistor is calculated by the following expression:

$$R_{SH} = \frac{V_{IT,TH+}}{I_{OC}} \quad (1)$$

Where $V_{IT,TH+}$ is the ITRIP positive-going threshold voltage of IPM. It is typically 0.5 V. I_{OC} is the current of OC detection level.

The maximum value of OC protection level should be set lower than the repetitive peak collector current in the datasheet taking into consideration the tolerance of the shunt resistor. For example, the current of OC detection level of IM828-XCC is 50 A_{peak}, and thus, the recommended value of the shunt resistor is calculated as

$$R_{SH(\min)} = \frac{0.5}{50} = 0.01\ \Omega$$

For the power rating of the shunt resistor, the following list should be considered:

- Maximum load current of inverter (I_{rms})
- Shunt resistor value at Tc = 25°C (R_{SH})
- Power derating ratio of shunt resistor at T_{SH}=100°C according to the manufacturer's datasheet
- Safety margin

The shunt resistor power rating is calculated by the following equation.

$$P_{SH} = \frac{I_{rms}^2 \times R_{SH} \times margin}{derating\ ratio} \quad (2)$$

For example, in the case of IM828-XCC and R_{SH} = 10 mΩ (WSR5R0100F: Vishay)

- Max. load current of the inverter: 14 A_{rms}
- Power derating ratio of shunt resistor at T_{SH} = 100°C: 80%
- Safety margin: 30%

$$P_{SH} = \frac{14^2 \times 0.01 \times 1.3}{0.80} \approx 3.2\ W$$

A proper power rating of shunt resistor exceeds 3.2 W, e.g. 5 W. In addition, we recommend an SMD-type shunt resistor to minimize surge voltage by stray inductance of shunt resistor.

Model	Power rating [W]	Short time overload	Inductance [nH]	TCR [ppm/°C]	Operating temp. range [°C]
WSR5	5.0 at 70°C	3x rated power for 5 s	0.5 ~ 5.0	< 20	-55 ~ 150

Based on the previous equations, conditions, and calculation method, the minimum shunt resistance and resistor power of the IPM have been introduced and are listed in Table 22. It is noted that a proper resistance and power rating higher than the minimum value should be chosen considering the overcurrent protection level required in the application.

Table 22 Minimum R_{SH} and P_{SH}

Product	Max. peak current	Min. shunt resistance, R_{SH}	Min. shunt resistor power, P_{SH}
IM828-XCC	50 A	10 mΩ	5.0 W
IM12S60EA2	50 A	10 mΩ	5.0 W

IM12S90EA2	33 A	15 mΩ	3.0 W

5.2.3 Delay time

The RC filter is necessary in the overcurrent sensing circuit to prevent malfunction of OC protection caused by noise. The RC time constant is determined by considering the noise duration and the short-circuit withstand time capability of the MOSFET.

When the sensing voltage on the shunt resistor exceeds the ITRIP positive-going threshold ($V_{IT,TH+}$), this voltage is applied to the ITRIP pin of the IPM via the RC filter. Table 23 shows the specification of the OC protection reference level. The filter delay time (t_{Filter}) until that the input voltage of ITRIP pin rises to the ITRIP positive threshold voltage is defined by the following equation (3), (4).

$$V_{IT,TH+} = R_{SH} \cdot I_C \cdot (1 - \frac{1}{e^{\frac{t_{Filter}}{\tau}}}) \quad (3)$$

$$t_{Filter} = -\tau \cdot \ln(1 - \frac{V_{IT,TH+}}{R_{SH} \cdot I_C}) \quad (4)$$

Where, $V_{IT,TH+}$ is the ITRIP pin input voltage, I_C is the peak current, R_{SH} is the shunt resistor value and τ is the RC time constant. In addition, there is a short-circuit propagation delay time of Itrip (t_{SCP}) which is defined by the propagation delay time from $V_{IT,TH+}$ to 10% of I_{SC}. Please refer to Table 24.

Table 23 Specification of OC protection reference level $V_{IT,TH+}$

Item	Symbol	Min.	Typ.	Max.	Unit
ITRIP positive-going threshold	VIT,TH+	0.475	0.500	0.525	V

Table 24 Shut-down propagation delay

Item		Condition	Min.	Typ.	Max.	Unit
Short-circuit propagation delay time (t_{SCP})	IM828-XCC	From $V_{IT,TH+}$ to 10% I_{SC}	-	1200	-	ns
	IM12S60EA2		-	1000	-	
	IM12S90EA2		-	900	-	

Therefore, the total time from ITRIP positive-going threshold ($V_{IT,TH+}$) to the shut-down of the MOSFET becomes:

$$t_{total} = t_{Filter} + t_{SCP}$$

The short-circuit propagation delay can be changed by operating conditions such as operating temperature and V_{DD}, V_{DC}. The total delay must be less than the 3 µs of short-circuit withstand time (t_{SC}) in the datasheet.

5.3 RFE circuit

The RFE pin combines three functions in one pin: fault output, enable input, and RC-network-based programmable fault clear timing.

The RFE pin is normally connected to an RC network on the application circuit in Figure 33. Under normal operating conditions, R_{RCIN} pulls the RFE pin to 5 V, thus enabling all the functions in the IPM. The micro-controller can pull this pin low to disable the IPM functionality. This is the Enable function.

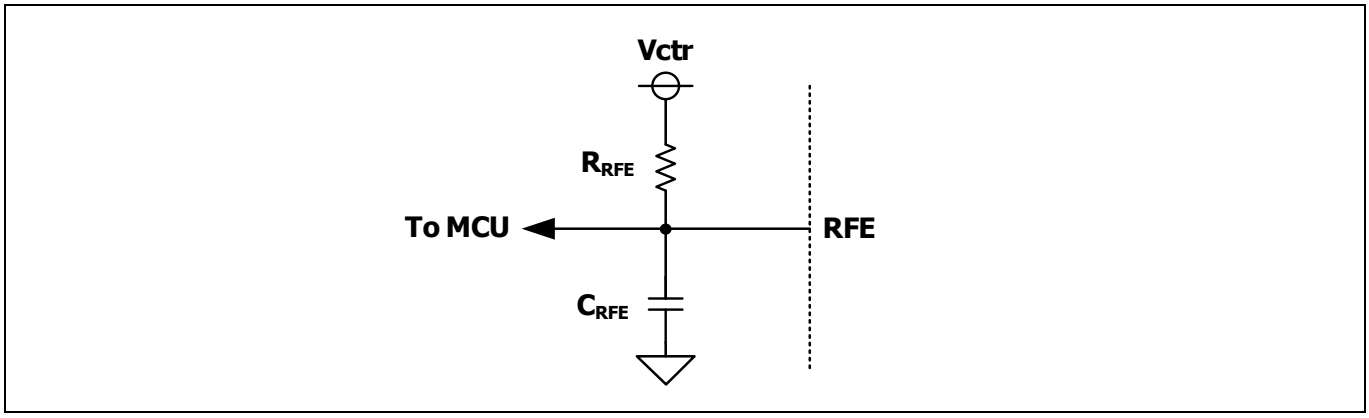


Figure 33 Typical application circuit for RFE pin

The fault-out function allows the IPM to report a fault event to the MCU by pulling the RFE pin low in one of two situations. The first is an undervoltage condition on V_{DD} and the second is when the ITRIP pin detects a voltage rising above $V_{RFE,TH+}$.

The programmable fault-clear timing function provides a means of automatically re-enabling the IPM operation a preset amount of time ($T_{FLT,CLR}$) after the fault event has disappeared. Figure 34 shows the RFE-related circuit block diagram inside the IPM.

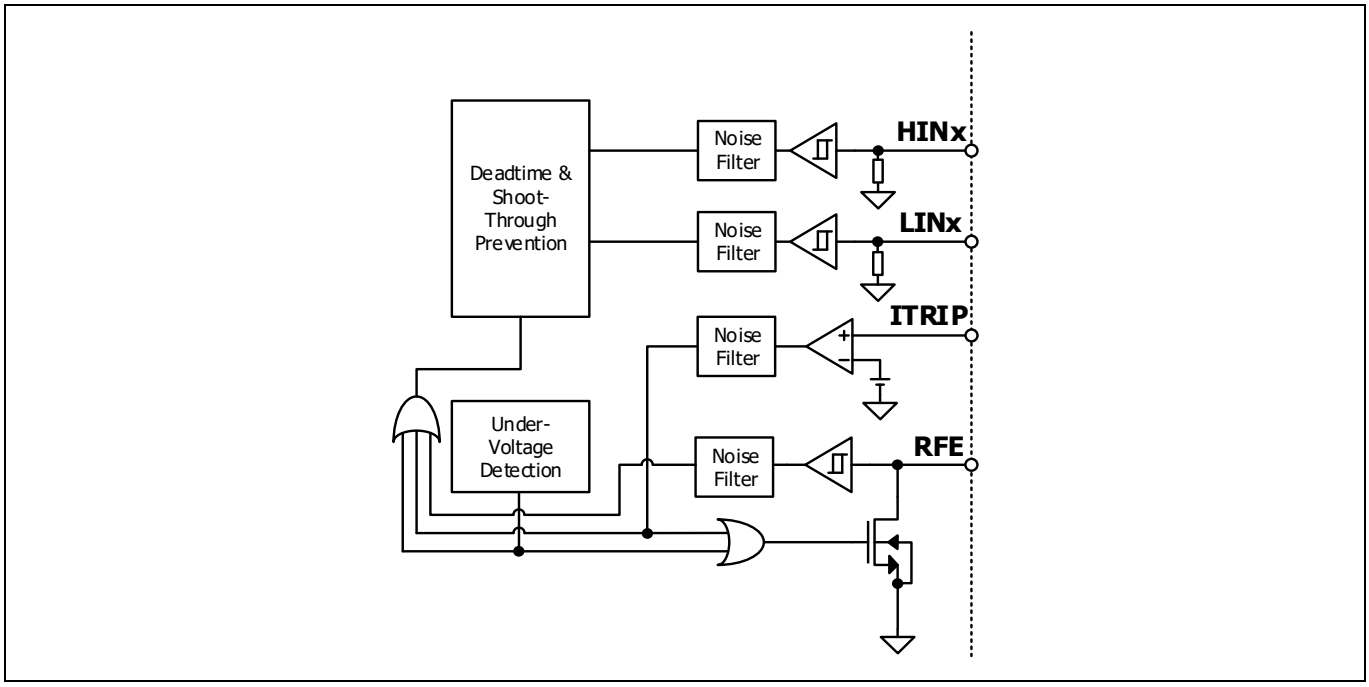


Figure 34 RFE internal circuit diagram

The length of total $T_{FLT,CLR}$ can be determined by using the formula below.

$$RFE(t) = Vctr \times \left(1 - e^{-\frac{t}{RC}}\right)$$

$$Total\ T_{FLT,CLR} = -R_{RFE} \times C_{RFE} \times \ln\left(1 - \frac{V_{RFE,TH+}}{V_{ctr}}\right) + \text{Internal fault-clear time } (T_{FLT,CLR})$$

For example, if V_{ctr} is 5.0 V, R_{RFE} is 2 MΩ , and C_{RFE} is 1 nF,

$$Total\ T_{FLT,CLR} = -2\ M\Omega \times 1\ nF \times \ln\left(1 - \frac{1.9\ V}{5.0\ V}\right) + 160\ \mu s\ \cong 1.1\ ms$$

Table 25 Examples of total $t_{FLT,CLR}$

V_{CTR} [V]	R_{RFE} [MΩ]	C_{RFE} [nF]	Total $T_{FLT,CLR}$ [ms]	V_{CTR} [V]	R_{RFE} [MΩ]	C_{RFE} [nF]	Total $T_{FLT,CLR}$ [ms]
3.3	2.0	1.0	1.9	**5.0**	2.0	1.0	1.1
	1.0	1.0	1.0		1.0	1.0	0.6
	0.5	1.0	0.6		0.5	1.0	0.4
	2.0	2.0	3.6		2.0	2.0	2.1
	1.0	2.0	1.9		1.0	2.0	1.1
	0.5	2.0	1.0		0.5	2.0	0.6

Table 26 RFE maximum rating

Item	Symbol	Condition	Rating	Unit
RFE voltage	V_{RFE}	Applied between RFE-VSS	-1~ V_{DD} + 0.3	V

Table 27 Electric characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
RFE output voltage	V_{RFE}	I_{RFE} = 10 mA, V_{ITRIP} = 1 V	-	0.7	-	V
RFE MOSFET Resistance	$R_{ON,RFE}$	-	-	40	70	Ω
RFE positive-going threshold	$V_{RFE,TH+}$	-	-	1.9	2.3	V
RFE negative-going threshold	$V_{RFE,TH-}$	-	0.7	0.9	-	V

Because the RFE terminal is an open-drain type, it must be pulled up to the high level via a pull-up resistor. The resistor has to be calculated according to the above specifications. In case of V_{CTR} is higher than 5V, the R_{RFE} needs to be minimum 200 kΩ.

5.4 Sleep function

The sleep function is activated after each trigger of ITRIP or undervoltage lockout. A new edge of each individual control signal LINx and HINx for activation of the outputs LOx or HOx is mandatory after release of signal RFE (fault out function). Please refer to Figure 35 for the description of the timing diagram.

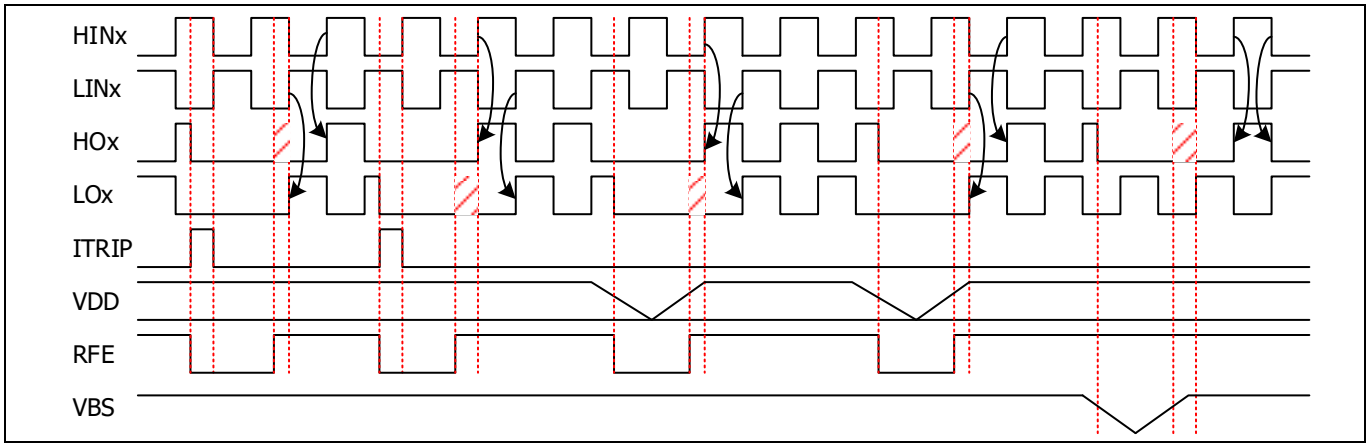


Figure 35 Sleep-function timing diagram ITRIP and UVLO

5.5 Temperature monitor and thermal protection

The IPM have independent pins for internal thermistors (85 kΩ at 25°C). The built-in thermistor is directly connected to the VSS internally. The typical application circuit looks like Figure 37. An external pull-up resistor connected to V_{ctr} ensures that the resulting voltage can be directly connected to the MCU.

In this reference board, the pull-up resistor is set to 18 kΩ so that the VTH voltage becomes 1.15 V and 0.75 V respectively for 5 V and 3.3 V control voltage (V_{ctr}) when the thermistor temperature is 100°C, as shown in Figure 38.

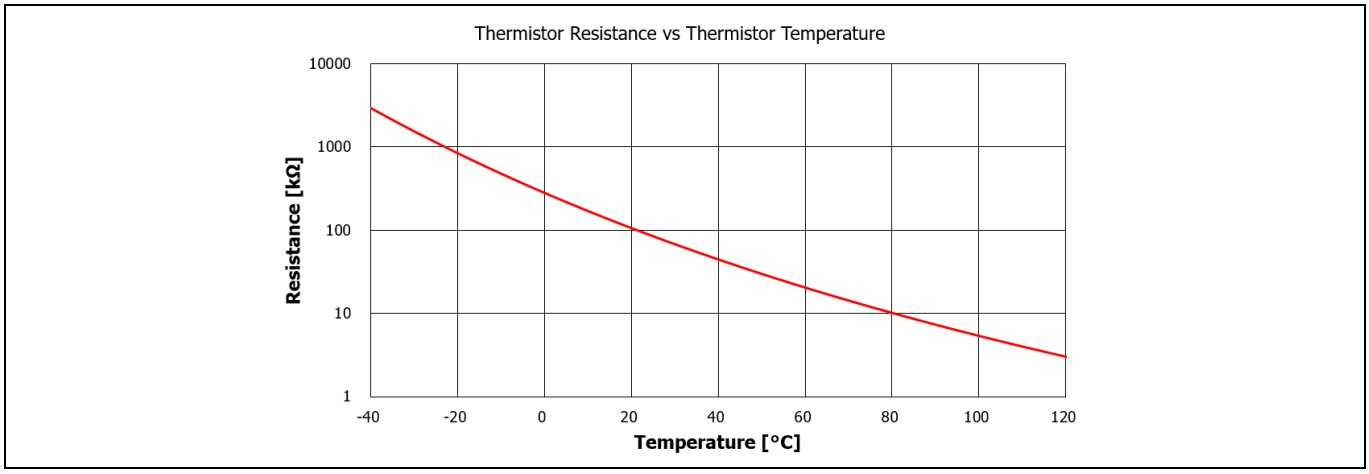


Figure 36 Internal thermistor resistance characteristics as a function of thermistor temperature

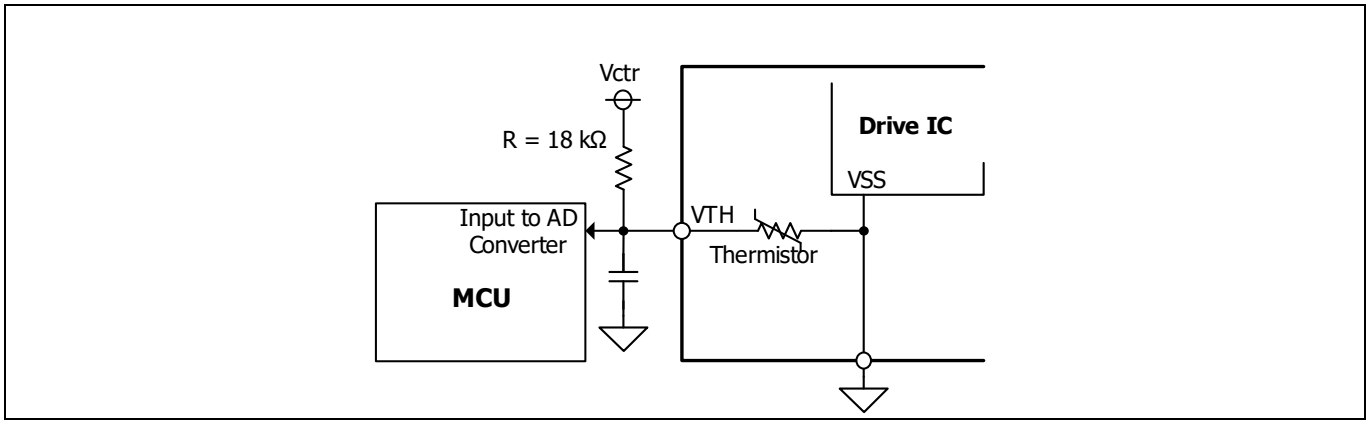


Figure 37 Circuit proposals for overtemperature protection

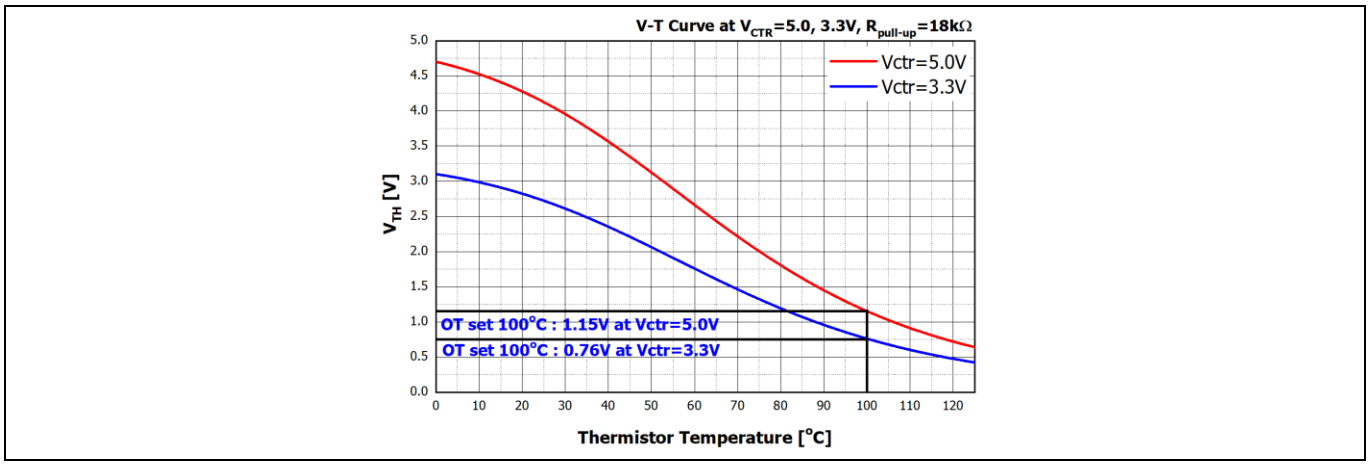
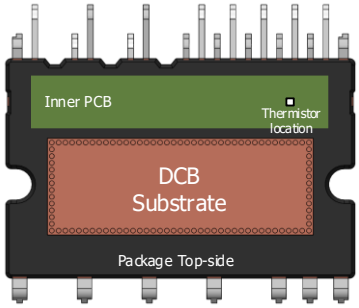


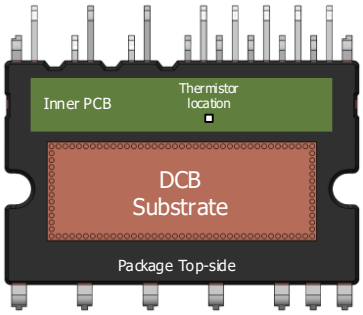
Figure 38 Voltage of VTH pin according to thermistor temperature

The NTC thermistor is located on the inner PCB of the IPM as in Figure 39(a) and (b). So, thermistor temperature cannot reflect power chip temperature directly. When the IPM is operated, the heat of power devices is transferred to the thermistor through the heat sink and package as seen in Figure 39(c). Also, Figure 39(d) and (e) describes temperature measurement point.

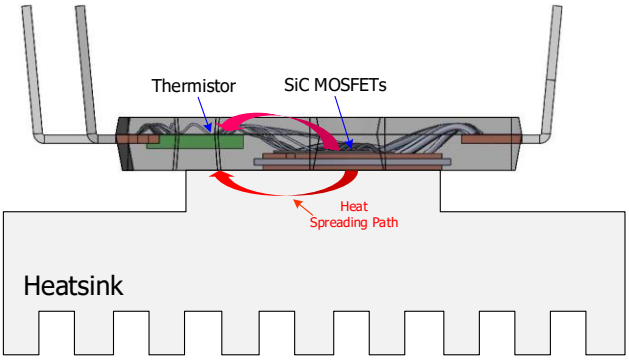
Figure 40 and Figure 41 shows the relationship between $T_{VJ(avg)}$(SiC MOSFET's maximum junction temperature), T_C (IPM case temperature), T_H(IPM heat sink temperature) and T_{NTC}(thermistor temperature) under given conditions. However, this relationship is just one of example, as the relationship depends on the system conditions such as heat sink size, cooling system, control scheme, etc. Therefore, if the user would like to know the relationship between T_{VJ}, T_H, and T_{NTC} on their system, we strongly recommend that they define the relationship by themselves with their own system.



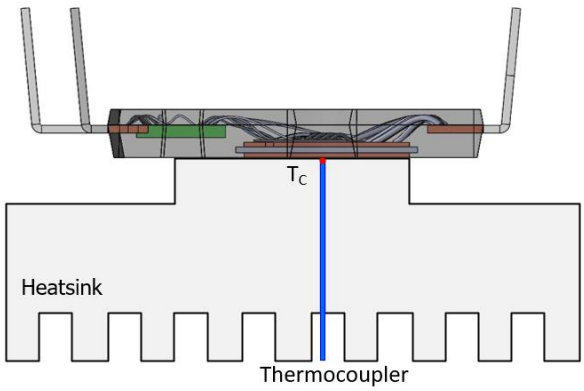
(a) Thermistor location (IM828-XCC)



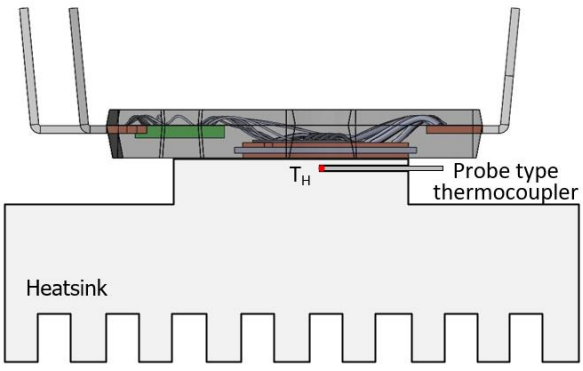
(b) Thermistor location (IM12S60/90EA2)



(c) Heat spreading from power devices



(d) Case temperature measurement point



(e) Heat sink temperature measurement point

Figure 39 Thermistor location, heat spreading from power devices, and temperature measurement point

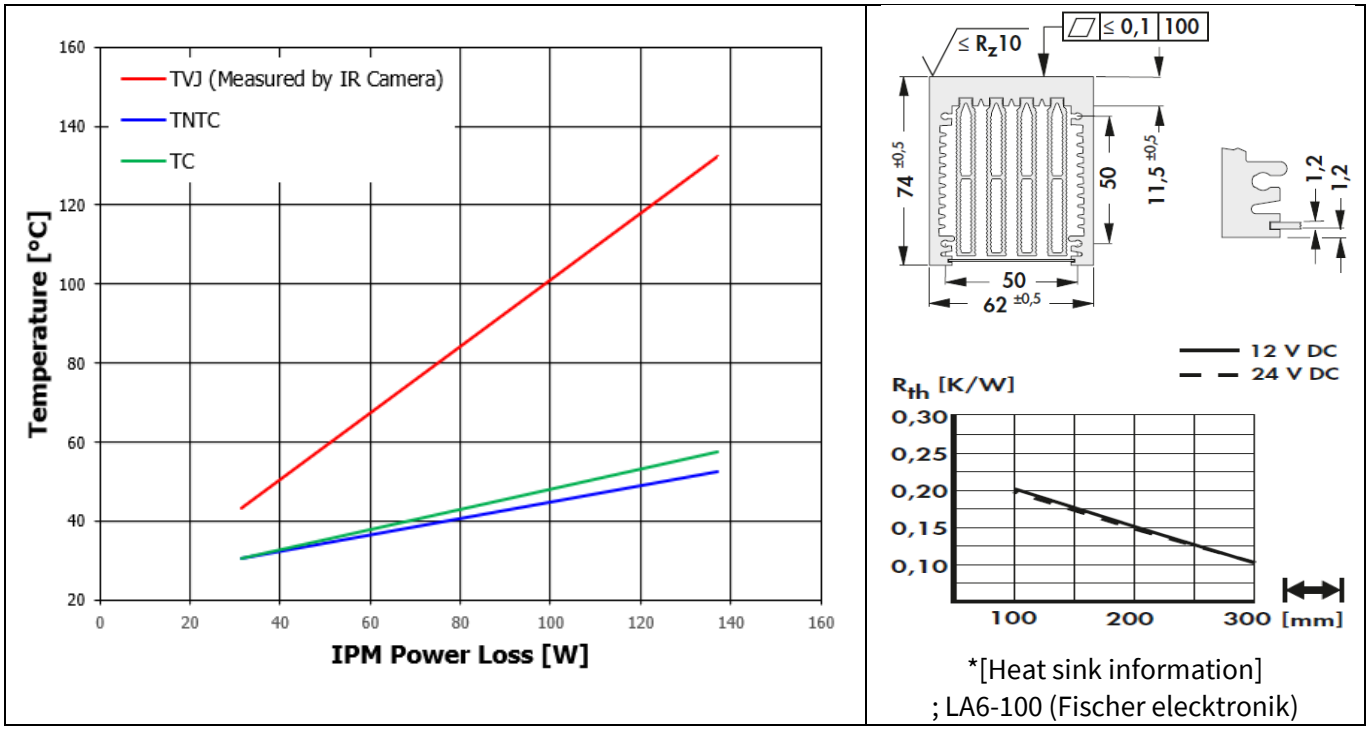


Figure 40 Example of relationship between $T_{J(MEA)}$, T_C, and T_{NTC} (Test conditions: IM828-XCC, V_{DC} = 600 V, V_{DD} = 15 V, I_O = 5 ~ 20 Apeak, F_{SW} = 20 kHz, F_O = 3 Hz, SVPWM, force cooling with *heat sink and fan, T_J is measured by Infrared camera, T_C measurement point refer to Figure 4 (a))

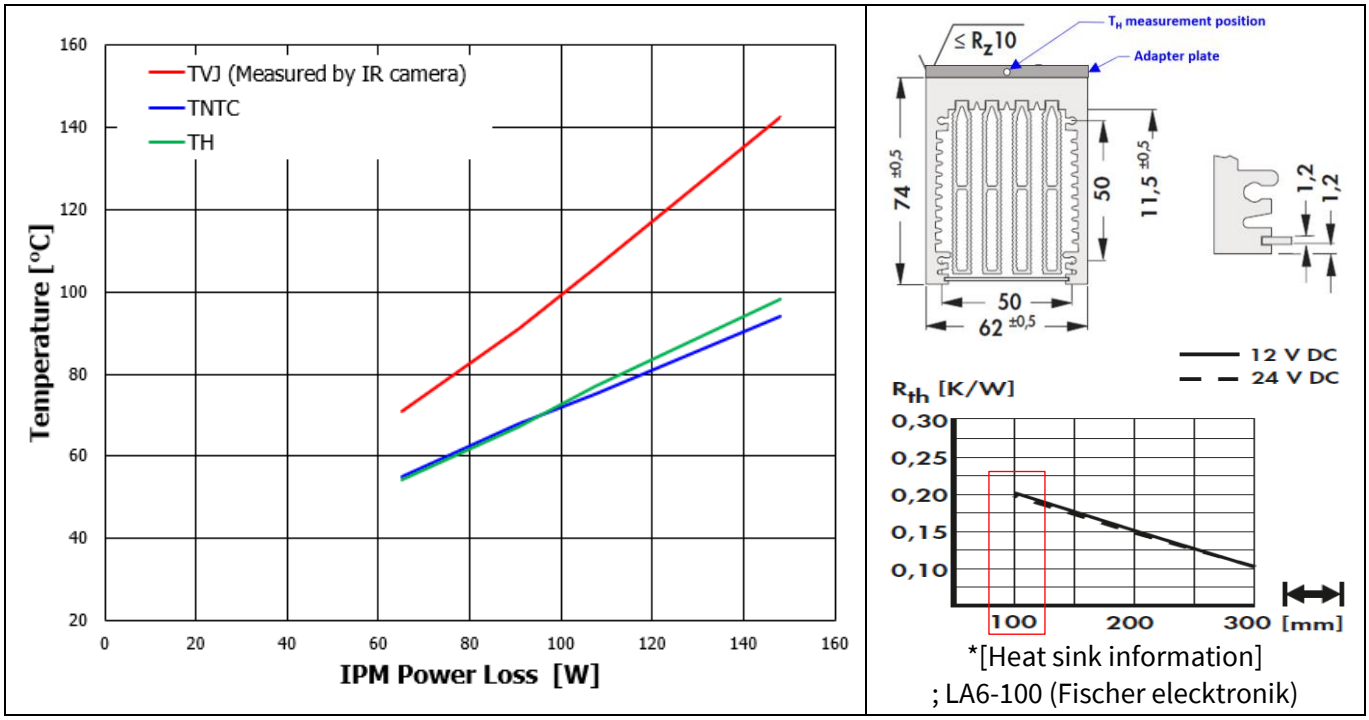


Figure 41 Example of relationship between $T_{VJ(avg)}$, T_C, and T_{NTC} (Test conditions: IM12S60EA2, V_{DC} = 660 ~ 850 V, V_{DD} = 18 V, I_O = 15 ~ 20 Apeak, F_{SW} = 20, 40 kHz, F_O = 60 Hz, SVPWM, force cooling with *heat sink and fan, $T_{VJ(avg)}$ is measured by Infrared camera

6 Bootstrap circuit

6.1 Bootstrap circuit operation

The V_{BS} voltage, which is the voltage difference between $V_{B\,(U,V,W)}$ and $V_{S\,(U,V,W)}$, provides the supply to the high-side gate driver IC within the IPM. This supply voltage (V_{BS}) is recommended to be in the range of 12.5 ~ 18.5 V to ensure that the gate driver IC can fully drive the high-side MOSFET. The IPM includes an undervoltage detection function for the V_{BS} to ensure that the IC does not drive the high-side MOSFET if the V_{BS} voltage drops below a specified voltage (refer to the datasheet). This function prevents the MOSFET from operating in a high dissipation mode. Please note here that the undervoltage lockout function of any high-side section acts only on the triggered channel without any feedback to the control level.

There are a number of ways in which the V_{BS} floating supply can be generated. One of them is the bootstrap method described here. This method has the advantage of being simple and cheap. However, the duty cycle and on-time are limited by the requirement to refresh the charge in the bootstrap capacitor. The bootstrap supply is formed by a combination of a diode (D_{BS}), resistor (R_{BS}) and capacitor (C_{BS}) as shown in Figure 44 (a). The current flow path of the bootstrap circuit is shown in Figure 44 (a). When V_S is pulled down to ground (either through the low side or the load), the bootstrap capacitor (C_{BS}) is charged through the bootstrap diode (D_{BS}) and the resistor (R_{BS}) from the V_{DD} supply.

6.2 Internal bootstrap functionality characteristics

The IPM includes three bootstrap functionalities in the internal gate driver IC, which consist of three diodes and three resistors, as shown in Figure 3. A typical value of the internal bootstrap resistor is 120 Ω at room temperature. For more information, please refer to Figure 42 and Table 28.

V_{DD} of 15 V is recommended when only the integrated bootstrap circuitry is used.

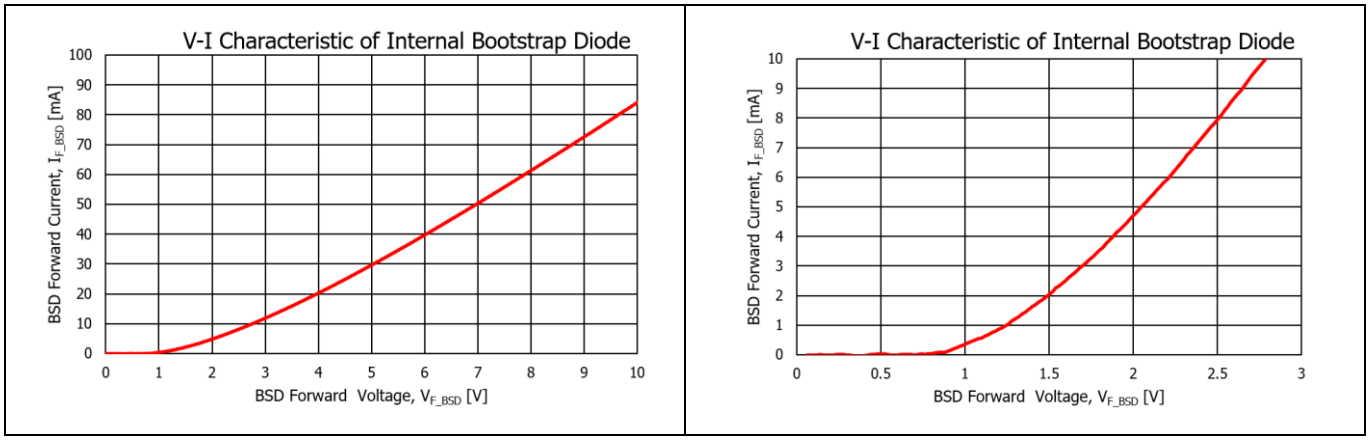


Figure 42 Internal bootstrap diode I_F - V_F characteristics

Table 28 Electrical characteristics of internal bootstrap parameters

Description	Condition	Symbol	Value			Unit
			Min.	Typ.	Max.	
Repetitive peak-reverse voltage		V_{RRM}	1200	-	-	V
Diode resistance	Between V_F = 4 V and V_F = 5 V	R_{BSD}	-	120	-	Ω
Diode forward voltage	I_F = 0.3 mA	V_{F_BSD}	-	0.9	-	V

6.3 Initial charging of bootstrap capacitor

Once we assume that the use one-pulse charging method is used, the time required for initial charge depends on capacitance of C_{BS}, forward voltage of bootstrap diode (V_{F_BSD}) and resistance of R_{BS}. Charge is performed with a time constant that is roughly calculated from capacitance of C_{BS} and resistance of R_{BS}.

Example of calculation charging waveform is shown in Figure 43.

Conditions: IM828-XCC (1200 V / 20 A, D_{BS} and R_{BS} (120 Ω) are embedded on gate driver IC), C_{BS} = 22 µF / 100 µF, V_{DD} = 15 V and R_{SHUNT} = 10 mΩ.

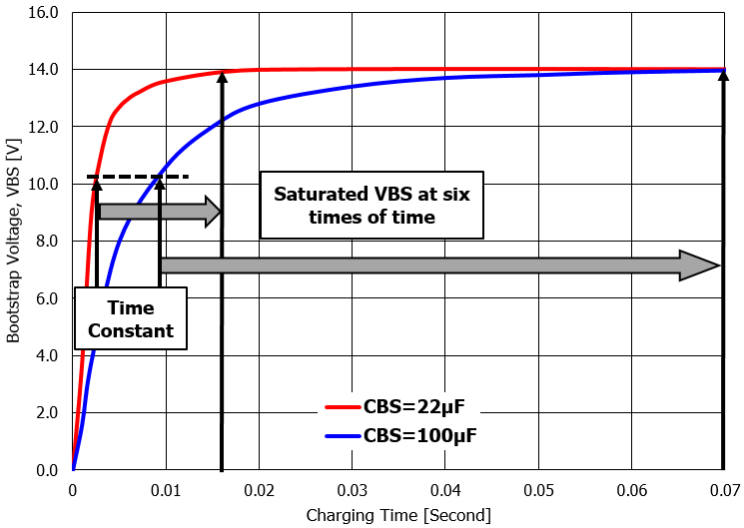
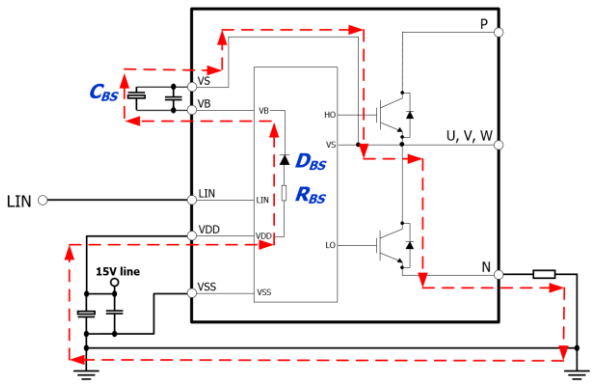


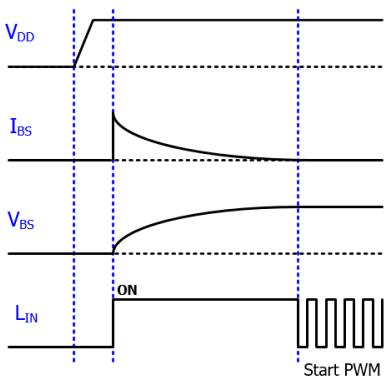
Figure 43 Bootstrap circuit operation and initial changing

Asin the above figure, V_{BS} does no reach target voltage (about 70%) by charging up to time constant (e.g. = C x R = 22 µF x 120 Ω = 2.64 ms). To reach target voltage, approximately six times the time constant will be needed. Target voltage does not reach the V_{DD}. It will become 1.0 V lower than the control supply voltage due to voltage drop of low-side MOSFET ($V_{DS(ON)}$) and D_{BS} (V_F) which are in charging path. Refer to Figure 44(a).

Initial charging needs to be performed until V_{BS} (voltage of C_{BS}) exceeds recommended minimum bootstrap voltage (V_{BS_min}) 12.5 V. (It is recommended to charge as high as possible with consideration for voltage drop between the end of charging and start of inverter operation.)



(a) Bootstrap circuit



(b) Timing chart of initial bootstrap charging

Figure 44 Bootstrap circuit operation and initial changing

6.4 Bootstrap supply circuit current at switching mode

Bootstrap supply circuit current at steady state, I_{QBS} (quiescent V_{BS} supply current) is typical 175 µA. But at switching mode, because gate charge and discharge are repeated by switching event, the circuit current (I_{BS}) can exceed I_{QBS} and increases proportional to switching frequency (F_{SW}). For reference, Figure 45 shows typical I_{BS} vs F_{SW} characteristics for IM828-XCC. (Conditions: V_{DD} = V_{BS} = 15V, T_J = 150°C, MOSFET ON duty = 50%)

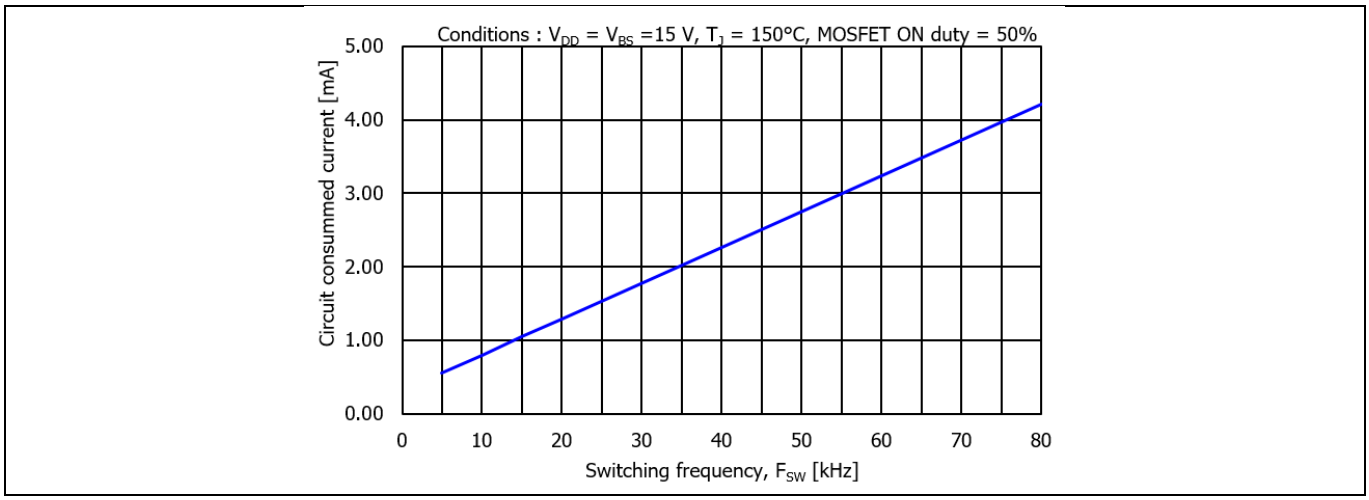


Figure 45 Bootstrap circuit consumed current (I_{BS}) vs. switching frequency (F_{SW}) for IM828-XCC

6.5 Bootstrap circuit design

When IM828-XCC for bootstrap circuit is designed, it is necessary to consider various conditions such as temperature characteristics, change by lifetime, variation and so on. Notes for designing these devices are listed as below. For more detailed information about driving via the bootstrap circuit, please refer to the application note “AN2020-14_Bootstrap circuit design for CIPOS™ IPM”.

6.5.1 Bootstrap capacitor

Electrolytic capacitors are used for C_{BS} generally. And recently MLCC (multilayer ceramic capacitor) with large capacitance are also applied. But the DC bias characteristics of the MLCC when applying DC voltage are considerably different from that of the electrolytic capacitor, especially the large capacitance type. Some differences in capacitance characteristics between electrolytic and ceramic capacitors are listed in Table 29.

Table 29 Difference of capacitance characteristics between electrolytic and ceramic capacitors

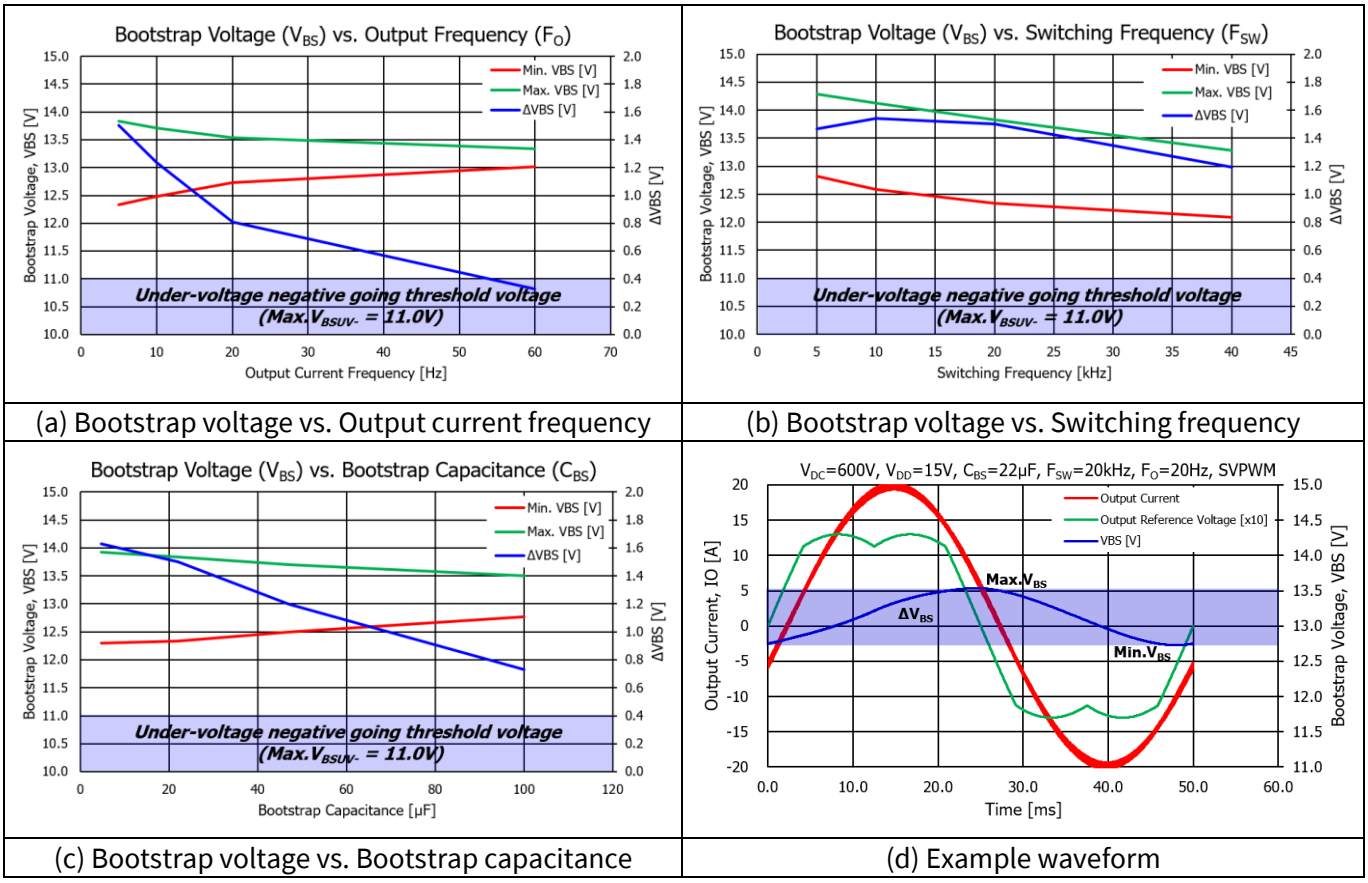
	Electrolytic capacitor	MLCC
Temperature characteristics (T_A : -20 ~ 85°C)	- Aluminum type: Low temp.: -10%, High temp.: +10% - Conductive polymer aluminum solid type: Low temp.: -5%, High temp.: +10%	- Difference due to temp. characteristics: Low temp.: -5% ~ 0% High temp.: -5% ~ -10% (with X5R, X7R)
DC bias characteristics (applying DC15V)	Nothing within rating voltage	Difference due to temp. characteristics, rating voltage, package size and so on -50% ~ -15% (with X7R, 50 VDC rating)

6.5.2 Bootstrap voltage variance under inverter operating conditions

When a bootstrap circuit is designed, bootstrap voltage (V_{BS}) variance needs to be considered at inverter operating conditions such as output current & frequency, switching frequency, modulation scheme, voltage ripple of V_{BS} and so on. Because lower bootstrap voltage can lead to high dissipation of high-side MOSFET or undervoltage lockout (UVLO) protection mode. Figure 46 shows trend of bootstrap voltage variance under given conditions based on simulation.

• Conditions: DUT = IM828-XCC, V_{DC} = 600 V, V_{DD} = 15 V, I_O = 20 Apeak, SVPWM, ΔV_{BS} (Voltage ripple) < 2.0 V, T_C = 25°C,

(a) C_{BS} = 22 µF, F_{SW} = 20 kHz, (b) C_{BS} = 22 µF, F_O = 5 Hz, (c) F_{SW} = 20 kHz, F_O = 5 Hz



(a) Bootstrap voltage vs. Output current frequency

(b) Bootstrap voltage vs. Switching frequency

(c) Bootstrap voltage vs. Bootstrap capacitance

(d) Example waveform

Figure 46 Bootstrap voltage (V_{BS}) variance under inverter operating conditions (IM828-XCC)

According to Figure 46, except bootstrap capacitance (C_{BS}), major affected operating conditions to bootstrap voltage (V_{BS}) are

• Output current frequency, F_O

• Switching frequency, F_{SW}

Note that these results are only an example. It is necessary to consider enough confirmation and evaluation at the system design. Because bootstrap voltage is also affected by other operating conditions such as PWM scheme (e.g. discontinuous space vector PWM), power factor, modulation index, power switches (IGBT and MOSFET), and so on.

7 Thermal system design

7.1 Introduction

The thermal design of a system is a key issue of IPM included in electronic systems such as drives. To avoid overheating and/or to increase the reliability, two design criteria are of importance:

- Low power losses
- Low thermal resistance from junction to ambient

The first criterion is already fulfilled when choosing IPM as an intelligent power module for the application. To get the most out of the system, a proper heat sink choice is necessary. A good thermal design either allows the designer to maximize the power or to increase the reliability of the system (by reducing the maximum temperature). This application note will give a short introduction on power losses and the heat sink, helping to understand the mode of operation and to find the right heat sink for a specific application.

For the thermal design, one needs:

- The maximum power losses $P_{sw,i}$ of each power switch
- The maximum junction temperature $T_{J,max}$ of the power semiconductors
- The junction to ambient thermal resistance impedance $Z_{th,J-A}$. For stationary considerations the static thermal resistance $R_{th,J-A}$ is sufficient. This thermal resistance comprises the junction-to-case thermal resistance $R_{th,J-C}$ as provided in the datasheets, the case to heat sink thermal resistance $R_{th,C-HS}$ accounting for the heat flow through the thermal interface material between heat sink and the power module, and the heat sink-to-ambient thermal resistance $R_{th,HS-A}$. Each thermal resistance can be extended to its corresponding thermal impedance by adding the thermal capacitances.
- The maximum allowed ambient temperature is $T_{A,max}$

Furthermore, all heat flow paths need to be identified. Figure 47 presents a typical simplified equivalent circuit for the thermal network. This circuit is simplified, as it omits thermal capacitance, and typically negligible heat paths such as the heat transfer from the module surface directly to the ambient via convection and radiation.

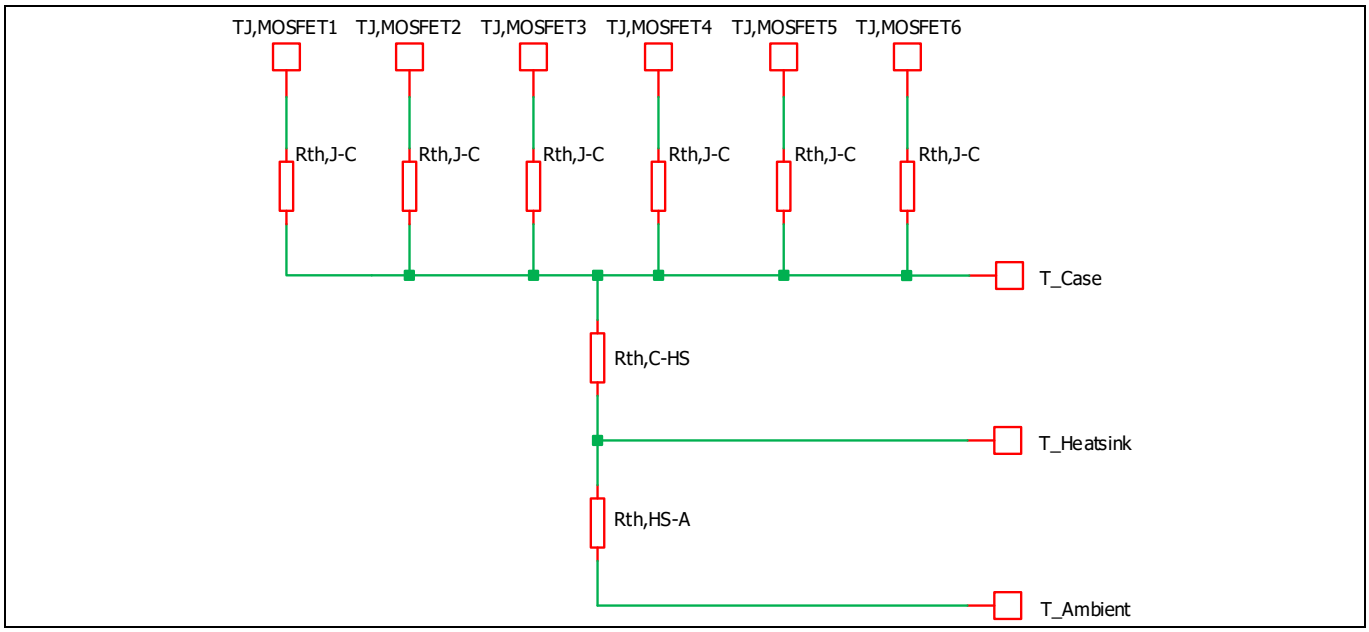


Figure 47 Simplified thermal equivalent circuit

7.2 Power loss

The total power losses in the IPM are composed of conduction and switching losses in the MOSFETs and body diodes. The loss during the turn-off steady state can be ignored because it is very small and has little effect on increasing the temperature in the device. The conduction loss depends on the DC electrical characteristics of the device, i.e. saturation voltage. Therefore, it is a function of the conduction current and the device's junction temperature. On the other hand, the switching loss is determined by the dynamic characteristics like turn-on/off time and overvoltage/current. Hence, to obtain the accurate switching loss, the DC-link voltage of the system, the applied switching frequency and the power circuit layout in addition to the current and temperature should be considered. In this chapter, based on a PWM inverter system for motor control applications, detailed equations are shown to calculate both losses of the IPM for a 3-phase continuous sinusoidal PWM. For other cases like 3-phase discontinuous PWMs, please refer to [5].

7.2.1 Conduction losses

The typical characteristics of forward drop voltage are approximated by the following linear equation for the IGBT and the diode, respectively.

$$V_{IGBT} = V_I + R_I \cdot i$$
$$V_{DIODE} = V_D + R_D \cdot i \quad (6)$$

- V_I = threshold voltage of IGBT
- V_D = threshold voltage of diode
- R_I = on-state slope resistance of IGBT
- R_D = on-state slope resistance of diode

Assuming that the switching frequency is high, the output current of the PWM inverter can be assumed to be sinusoidal. That is,

$$i = I_{peak}\cos(\theta - \varphi) \quad (7)$$

Where, φ is the phase-angle difference between output voltage and current. Using equations (6) and (7), the conduction loss of one IGBT and its diode can be obtained as follows.

$$P_{con.I} = \frac{1}{2\pi}\int_0^{\pi} \xi(V_{IGBT} \times i)d\theta = \frac{I_{peak}}{2\pi}V_I + \frac{I_{peak}}{8}V_I MI\cos\varphi + \frac{I_{peak}^2}{8}R_I + \frac{I_{peak}^2}{3\pi}R_I MI\cos\varphi \quad (8)$$

$$P_{con.D} = \frac{1}{2\pi}\int_0^{\pi} (1-\xi)(V_{DIODE} \times i)d\theta = \frac{I_{peak}}{2\pi}V_D - \frac{I_{peak}}{8}V_D MI\cos\varphi + \frac{I_{peak}^2}{8}R_D - \frac{I_{peak}^2}{3\pi}R_D MI\cos\varphi \quad (9)$$

$$P_{con} = P_{con.I} + P_{con.D} \quad (10)$$

Where ξ is the duty cycle in the given PWM method

$$\xi = \frac{1 + MI\cos\theta}{2} \quad (11)$$

Where, MI is the PWM modulation index (MI is defined as the peak-phase voltage divided by the half of DC- link voltage).

It should be noted that the total inverter conduction losses are six times the P_{con}.

7.2.2 Switching losses

Different devices have different switching characteristics, which also vary according to the handled voltage/current and the operating temperature/frequency. However, the turn-on/off loss energy (joule) can be experimentally measured indirectly by multiplying the current and voltage and integrating over time, under a given circumstance. Therefore, the linear dependency of the switching energy loss on the switched current is expressed during one switching period as follows.

$$Swtitching \quad energy \quad loss = (E_I + E_D) \times i \ [joule] \tag{12}$$

$$E_I = E_{I.ON} + E_{I.OFF} \tag{13}$$

$$E_D = E_{D.ON} + E_{D.OFF} \tag{14}$$

Where, E_I i is the switching loss energy of the IGBT and E_D i is for its anti-parallel diode. E_I and E_D can be considered approximately as a constant.

As mentioned in the equation (7), the output current can be considered as a sinusoidal waveform; and the switching loss occurs every PWM period for the continuous PWM schemes. Therefore, depending on the switching frequency f_{sw}, the switching loss of one device is represented in the following equation (15).

$$P_{sw} = \frac{1}{2\pi}\int_0^{\pi}(E_I + E_D)\ i\ f_{sw}d\varphi = \frac{(E_I + E_D)f_{sw}I_{peak}}{\pi} \tag{15}$$

Where, E_I is a unique constant of IGBT related to the switching energy, and different IGBTs have different E_I values. E_D is one for diode. These should be derived by experimental measurement. From the equation (15), it should be noted that the switching losses are a linear function of current, and directly proportional to the switching frequency.

7.3 Thermal impedance

In practical operation, the power loss P_D is cyclic and therefore the transient impedance needs to be considered. The thermal impedance is typically represented by a RC equivalent circuit (Foster model) as shown in Figure 48. For pulsed power loss, the thermal capacitance effect delays the rise in junction temperature, and thus permits a heavier loading of the IPM. Figure 49 shows thermal impedance from the junction-to-case curves of each IPMs. The thermal resistance in Table 30 goes into saturation in about 10 seconds.

Table 30 Thermal resistance of IM828-XCC

Product	Description	Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
IM828-XCC	Single-MOSFET thermal resistance, junction-case	R_{thJC}	Low-side U-phase MOSFET (See Figure 4 for T_C measurement point)	-	-	1.45	K/W
IM12S60EA2				-	-	0.88	
IM12S90EA2				-	-	1.10	

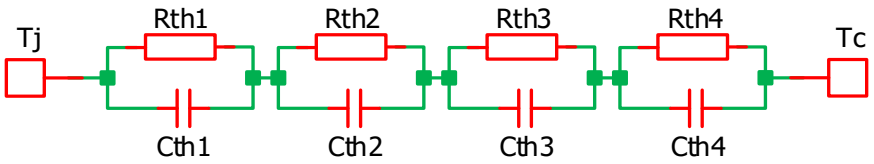


Figure 48 Thermal impedance RC equivalent circuit

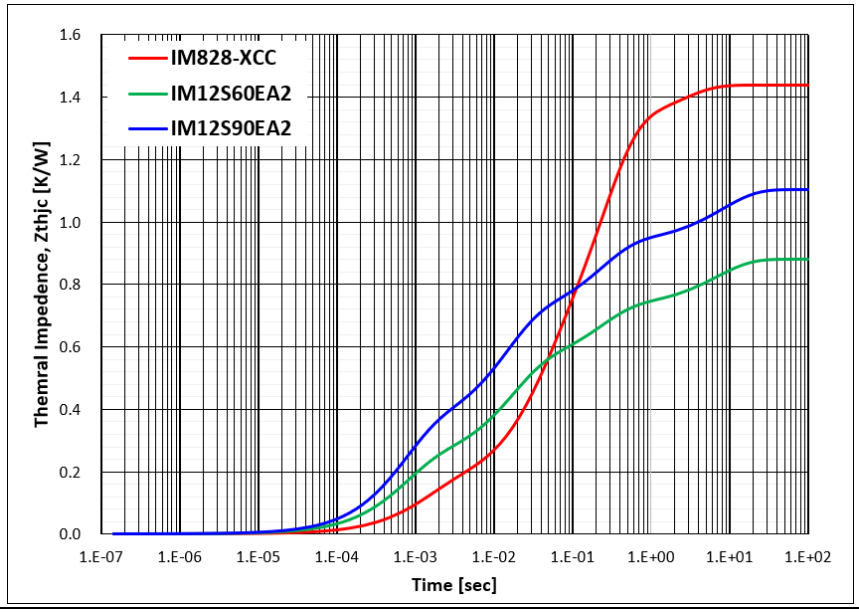
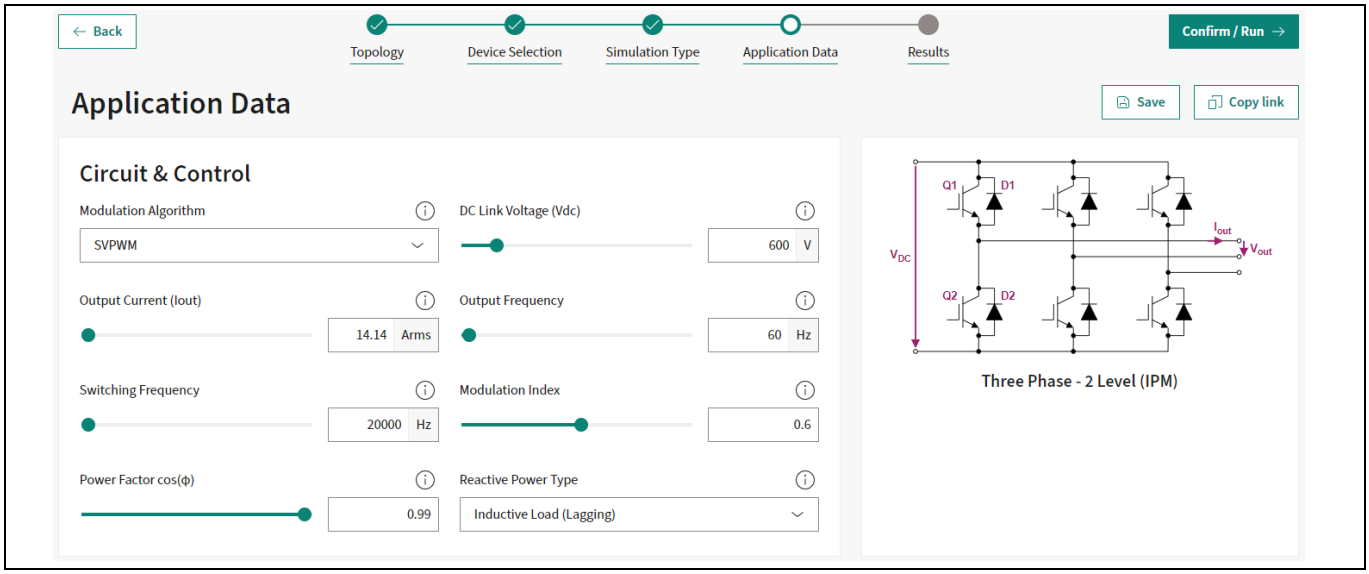


Figure 49 Thermal impedance curves (based on single-chip heating)

7.4 Temperature rise considerations and calculation example

The IPOSIM – Infineon Power Simulation [6] allows users to calculate power losses and temperature profiles with two heat sink mounting options (fixed reference, user defined heat sink). The result of loss & temperature calculation using the typical characteristics is shown in Figure 50 as simulation example (for V_{PN} = 600 V, V_{DD} = 15 V, $V_{DS(ON)}$ = typical, switching losses = typical, T_J = 150°C, F_{SW} = 20 kHz, $R_{th(J-C)}$ = Max., P.F = 0.99, MI = 0.60, I_O = 14.14 A_{rms}, T_C = 100°C (fixed reference), SVPWM modulation, 60 Hz sine waveform output).



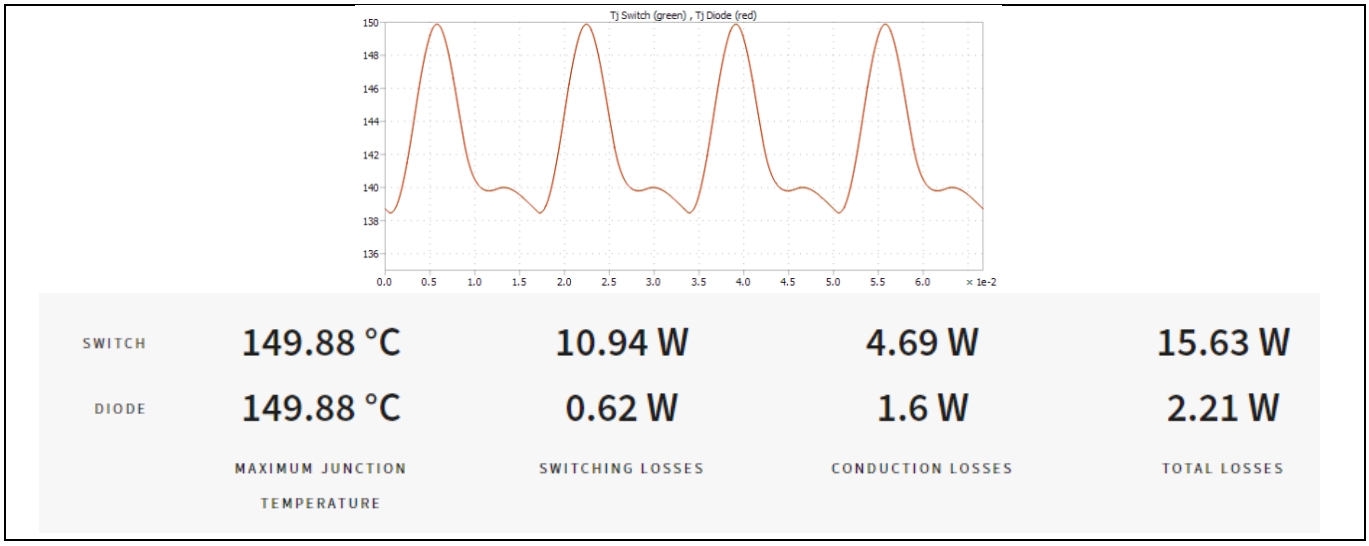


Figure 50 IPOSIM – Infineon Power Simulation results for IM828-XCC [6]

7.5 Heat sink selection guide

7.5.1 Required heat sink performance

If the power losses $P_{sw,i}$, $R_{th(J-C)}$ and the maximum ambient temperature are known, the required thermal resistance of the heat sink and the thermal interface material can be calculated according to 0 from,

$$T_{J,max} = T_{A,max} + \sum_i P_{sw,i} \cdot R_{th,HS-A} + \sum_i P_{sw,i} \cdot R_{th,C-HS} + Max(P_{sw,i} \cdot R_{th,JC,i}) \quad (16)$$

For three- phase bridges, one can simply assume that all power switches dissipate the same power and all have the same $R_{th,J-C}$. This leads to the required thermal resistance from case to ambient.

$$R_{th,C-A} = R_{th,C-HS} + R_{th,HS-A} = \frac{T_{J,max} - P_{sw} \cdot R_{th,JC} - T_{A,max}}{\sum P_{sw}} \quad (17)$$

For example, the power switches of a washing machine drive dissipate 3.5 W maximum each, the maximum ambient temperature is 50°C, the maximum junction temperature is 150°C and $R_{th(J-C)}$ is 3 K/W. It results in:

$$R_{th,C-A} \leq \frac{150°C - 3.5W \cdot 3\frac{K}{W} - 50°C}{6 \cdot 3.5W} = 4.3\frac{K}{W}$$

If the heat sink temperature shall be limited to 100°C, an even lower thermal resistance is required:

$$R_{th,C-A} \leq \frac{100\,°C - 50\,°C}{6 \cdot 3.5W} = 2.4\frac{K}{W}$$

Smaller heat sinks with higher thermal resistance may be acceptable if the maximum power is only required for a short time (times below the time constant of the thermal resistance and the thermal capacitance). However, this requires a detailed analysis of the transient power and temperature profiles. The larger the heat sink, the larger the thermal capacitance and the longer it takes to heat up the heat sink.

7.5.2 Heat sink characteristics

Heat sinks are characterized by three parameters:

- Heat transfer from the power source to heat sink
- Heat transfer within the heat sink (to all the surfaces of the heat sink)
- Heat transfer from heat sink surfaces to ambient

7.5.2.1 Heat transfer from heat source to heat sink

There are two factors which need to be considered in order to provide a good thermal contact between power source and heat sink:

- **Flatness of the contact area**

  Due to the unevenness of surfaces, a thermal interface material needs to be supplied between heat source and heat sink. However, such materials have a rather low thermal conductivity (< 10 K/W). Hence these materials should be as thin as possible. On the other hand, they need to fill out the space between heat source and heat sink. Therefore, the unevenness of the heat sink should be as low as possible. In addition, the particle size of the interface material must fit to the roughness of the module and the heat sink surfaces. Particles that are too large will unnecessarily increase the thickness of the interface layer, and hence increase the thermal resistance. Particles that are too small will not provide a good contact between the two surfaces and will lead to a higher thermal resistance as well.
- **Mounting pressure**

  The higher the mounting pressure, the better the interface material disperses. Also excessive interface material is squeezed out resulting in a thinner interface layer with a lower thermal resistance.

7.5.2.2 Heat transfer within the heat sink

The heat transfer within the heat sink is mainly determined by:

- **Heat sink material**

  The material needs to be a good thermal conductor. Most heat sinks are made of aluminum ($\lambda \approx 200$ W/(m*K)). Copper is heavier and more expensive but also nearly twice as efficient ($\lambda \approx 400$ W/(m*K)).
- **Fin thickness**

  If the fins are too thin, the thermal resistance from heat source to fin is too high, and the efficiency of the fin decreases. Hence it does not make sense to make the fins as thin as possible in order to make more fins and therefore to increase the surface area.

7.5.2.3 Heat transfer from heat sink surface to ambient

The heat transfers to the ambient mainly by convection. The corresponding thermal resistance is defined as

$$R_{th,conv} = \frac{1}{\alpha \cdot A} \qquad (18)$$

Where α is the heat transfer coefficient and A is the surface area.

Hence there are two important parameters:

- **Surface area:** Heat sinks require a huge surface area in order to easily transfer the heat to the ambient. However, as the heat source is assumed to be concentrated at one point and not uniformly distributed, the total thermal resistance of a heat sink does not change linearly with length. Also, increasing the surface area

by increasing the number of fins does not necessarily reduce the thermal resistance as discussed in Section 7.5.2.2.

- **Heat transfer coefficient (aerodynamics):** This coefficient strongly depends on the air flow velocity as shown in Figure 51. If there is no externally induced flow, one speaks of natural convection. Otherwise, it is forced convection. Heat sinks with very small fin spacing do not allow a good air flow. If a fan is used, the fin gap may be lower than for natural convection, as the fan forces the air through the space between the fins.

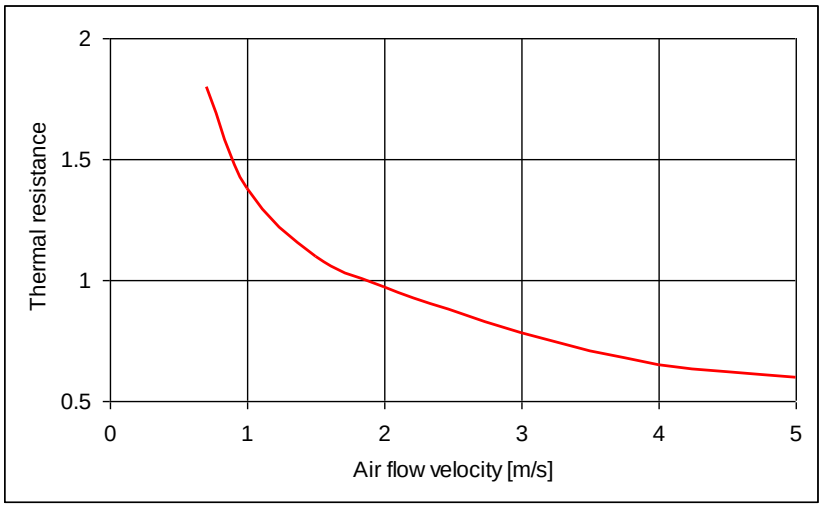


Figure 51 Thermal resistance as a function of the air flow velocity

Furthermore, in the case of natural convection, the heat sink efficiency depends on the temperature difference of heat sink and ambient, i.e. on the dissipated power. Some manufacturers, like Aavid Thermalloy, provide a correction table which allows the user to calculate the thermal resistance depending on the temperature difference. Figure 52 shows the heat sink efficiency degradation for natural convection as provided in [7]. Please note that the thermal resistance is 25% higher at 30 W than at 75 W.

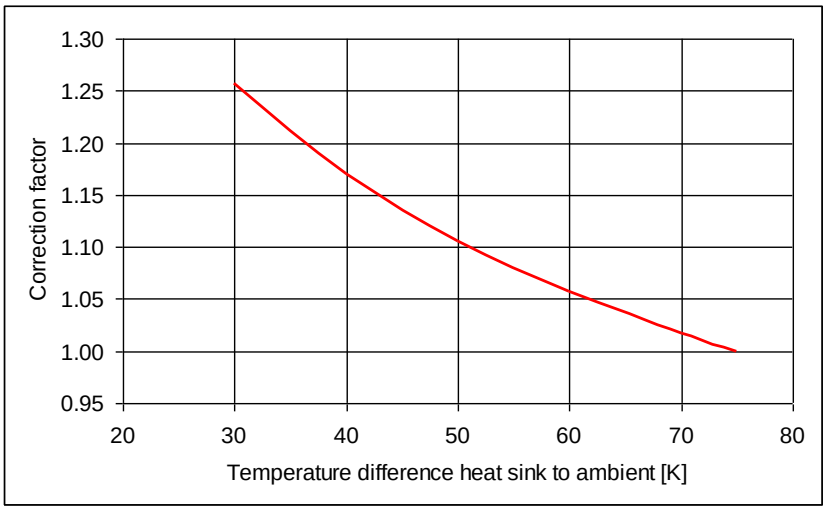


Figure 52 Correction factors for temperature

The positioning of the heat sink also plays an important role in the aerodynamics. In the case of natural convection, the best mounting is done with vertical fins, as the heated air tends to move upwards due to buoyancy. Furthermore, one should make sure that there are no significant obstructions impeding the air flow.

Radiation occurs as well supporting the heat transfer from heat sink to ambient. In order to increase radiated heat, one can use anodized heat sinks with a black surface. However, this decreases the thermal resistance of

the heat sink only by a few percentages in the case of natural convection. Radiated heat is negligible in the case of forced convection. Hence blank heat sinks can be used if no fan is used with the heat sink.

The discussions in this section clearly show that there cannot be a single thermal resistance value assigned to a certain heat sink.

7.5.3 Selecting a heat sink

Unfortunately, there are no straightforward formulas for selecting heat sinks. Finding an appropriate heat sink will include an iterative process of choosing and testing heat sinks. In order to get a first rough estimation of the required volume of the heat sink, one can start with estimated volumetric thermal resistances as given in Table 31 (taken from [8]). This table gives only a first clue, as the actual resistance may vary depending on many parameters like actual dimensions, type and orientation, etc.

Table 31 Volumetric thermal resistance

Flow conditions [m/s]	Volumetric resistance [cm³ °C/W]
Natural convection	500 ~ 800
1.0	150 ~ 250
2.5	80 ~ 150
5.0	50 ~ 80

One can roughly assume that the volume of a heat sink needs to be quadrupled in order to halve its thermal resistance. This gives a hint whether natural convection is sufficient for the available space, or whether forced convection is required.

In order to get an optimized heat sink for a given application, one needs to contact heat sink manufacturers or consultants. Further hints and references can be found in [7].

When contacting heat sink manufacturers in order to find a suitable heat sink, please note the conditions under which the given thermal resistance values are valid. They might be given either for a point source or for a heat source which is evenly distributed over the entire base area of the heat sink. Also take care that the fin spacing is optimized for the corresponding flow conditions.

8 Heat sink mounting and handling guidelines

8.1 Electrical spacing

The electric spacing specifications of IPM for MHA & industrial applications are shown in Table 32. The CIPOS™ Maxi package (DIP 36X23D) does not satisfy the clearance and creepage distance between pins and heat sink (earthed) and the creepage distance on the PCB between signal pins such as (2) to (3), (4) to (5), (6) to (7). Based on IEC and UL standards, to secure a clearance and creepage distance between the pins and the heat sink (earthed), a convex-shaped heat sink is necessary as shown in Figure 53, and the PCB slot is required to keep 4.0 mm creepage on the PCB between the signal pins.

Table 32 Electrical spacing (*not compliant to IEC)

Standard & CIPOS™ Maxi	IPM Unit				PCB		Remark
	Basic insulation pin to heat sink(earthed) [mm]		Functional insulation between pin and pin [mm]		PWB (solder to solder) [mm]		
	Clearance	Creepage	Clearance	Creepage	Clearance	Creepage	
IEC60335-1 IEC60664-1 IEC67800-5-1 UL840	5.5	4.0	3.0	4.0	3.0	4.0	Refer to Table 21
CIPOS™ Maxi Package	*1.6	*1.62	Power pins: 4.97 Signal pins: 3.33	Power pins: 5.17 Signal pins: 4.12	Power pins: 4.94 Signal pins: 3.53	Power pins: 4.94 Signal pins: *3.53	PCB slot is necessary.

Table 33 Boundary conditions

Isolation	Rated voltage	Overvoltage category	Impulse voltage	Working voltage	Working voltage	Pollution degree	IPM CTI
Pin to heat sink (earthed)	480 V_{ac}	III	6000 V	679 V_{dc}	Max. 800 V_{dc}	II	> 600
Pin to pin	480 V_{ac}	II	4000 V	679 V_{dc}	Max. 800 V_{dc}	II	> 600

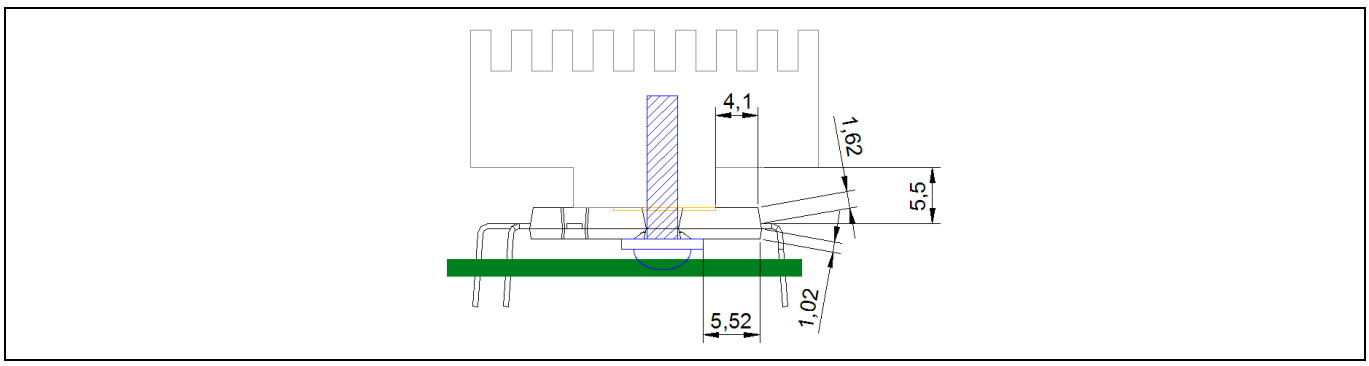


Figure 53 Recommended heat sink shape to get creepage and clearance distance between pins and heat sink (Dimension is symmetric)

8.2 Heat sink mounting

8.2.1 General guidelines

An adequate heat-sinking capability of the IPM is only achievable if the heat sink is suitably mounted. This is the fundamental requirement to meet the electrical and thermal performance criteria of the module. The following general points should be observed when mounting the IPM on a heat sink. Verify the following points related to the heat sink:

a) There must be no burrs on aluminum or copper heat sinks.
b) Screw holes must be countersunk.
c) There must be no unevenness or scratches in the heat sink.
d) The surface of the module must be completely in contact with the heat sink.
e) There must be no oxidation, stain, or burrs on the heat sink surface.

To improve the thermal conductivity, apply silicone grease to the contact surface between the IPM and heat sink. Spread a homogenous layer of silicone grease with a thickness of 100 µm over the IPM substrate surface. Non-planar surfaces of the heat sink may require a thicker layer of thermal grease. Please refer here to the specifications of the heat sink manufacturer. It is important to note here that the heat sink covers the complete backside of the module. There may be different functional behavior if there is a portion of the backside of the module which is not in contact with the heat sink.

To prevent a loss of heat dissipation effect due to warping of the substrate, tighten down the mounting screws gradually and sequentially while maintaining a left/right balance in pressure applied.

It must be assured by design of the application PCB, that the plane of the back side of the module and the plane of the heat sink are parallel to achieve minimal tension of the package and an optimal contact of the module with the heat sink. Please refer to the mechanical specifications of the module given in the datasheets.

It is the basics of good engineering to verify the function and thermal conditions by means of detailed measurements. It is best to use a final application inverter system, which is assembled with the final production process. This helps to achieve high-quality applications.

8.2.1.1 Recommended tightening torque

As shown in Table 34, the tightening torque of M3 screws is specified for a minimum MS = 0.49 N·m and a maximum MS = 0.78 N·m. The screw holes must be centered to the screw openings of the mold compound, so that the screws do not contact the mold compound. If an insulating sheet is used, use a sheet larger than the IPM, which should be aligned accurately when attached. It is important to ensure that no air is enclosed by the insulating sheet. Generally speaking, insulation sheets are used in the following cases:

- When the ability of withstanding primary and secondary voltages is required to achieve required safety standard against a hazardous situation.
- When the IPM must be insulated from the heat sink.
- When measuring the module, to reduce radiated noise or eliminate other signal-related problems.

Table 34 Mechanical characteristics and ratings

Item	Condition	Value			Unit
		Min.	Typ.	Max.	
Mounting torque	Mounting screw: M3	0.49	-	0.78	N·m
Backside curvature	(Note Figure 54)	0	-	+150	µm
Heat sink flatness	(Note Figure 55)	0	-	+100	µm
Weight		-	7.1	-	g

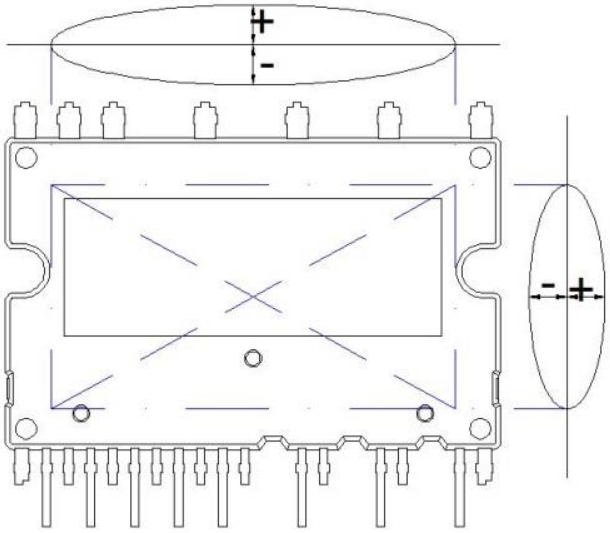


Figure 54 Backside curvature measurement position

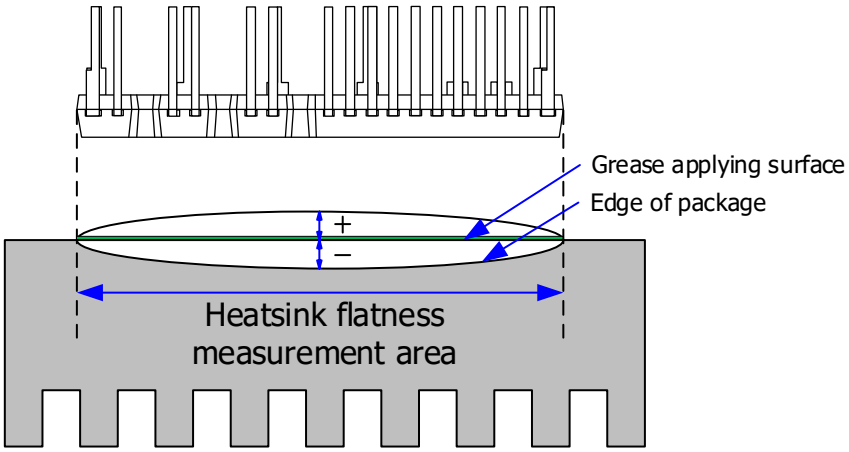


Figure 55 Heat sink flatness measurement position

8.2.1.2 Screw-tightening to heat sink

The tightening of the screws is the main process of attaching the module to the heat sink. It is assumed that an interface pad is attached to the heat sink surface, which extends to the edge of the module and is located for the fixing holes. It is recommended that M3 fixing screws are used in conjunction with a spring washer and a plain washer. The spring washer must be assembled between the plain washer and the screw head. The screw torque must be monitored by the fixing tool.

Tightening process:

- Align module with the fixing holes.
- Insert screw A with washers to touch only position (pre-screwing).
- Insert screw B with washers (pre-screwing).
- Tighten screw A to final torque.
- Tighten screw B to final torque.

Note: The pre-screwing torque is set to 20~30% of maximum torque rating.

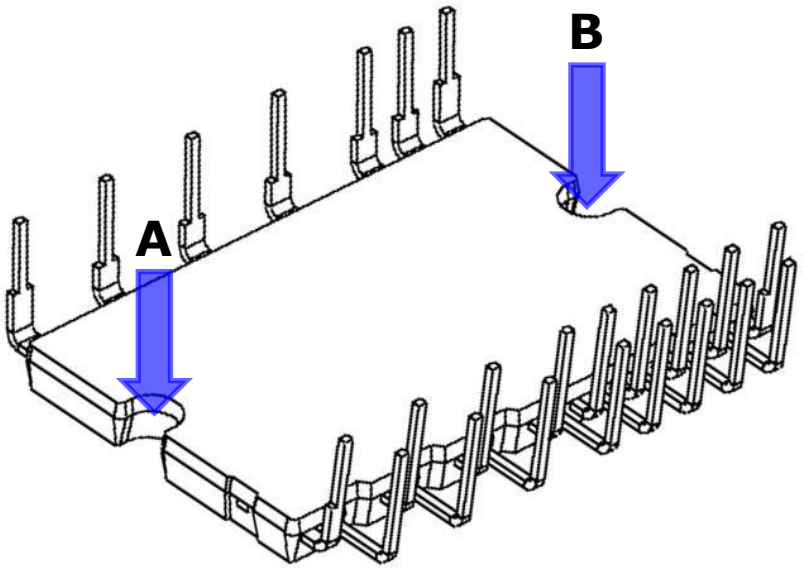


Figure 56 Recommended screw-tightening order: Pre-screwing A → B, Final screwing A → B

When installing a module to the heat sink, using excessive and uneven tightening force might stress the chips inside. This can break or degrade the device.

Some basic guidelines to follow are:

- Do not over torque when mounting the screws. Excessive mounting torque may damage the module holes, the screws, and the heatsink
- Avoid one-sided tightening stress. Uneven mounting can damage the module holes
- For effective heat dissipation, enlarge the contact area as much as possible. This also minimizes the contact thermal resistance
- Ensure that the thermal conductive grease is applied properly over the contact surface between the module and the heatsink. This also protects the contact surface from corrosion. The grease should be of stable quality and have long-term durability over a wide range of operating temperatures

- Use a torque wrench to tighten till the specified torque rating. Exceeding the maximum torque limitation may damage or degrade the module
- Make sure that there is no dirt on the contact surface between the module and the heatsink
- All equipment used to handle or mount the IPM must comply with the relevant ESD standards. This includes transportation, storage, and assembly. The module itself is an ESD-sensitive device. It may, therefore, get damaged in case of ESD shocks

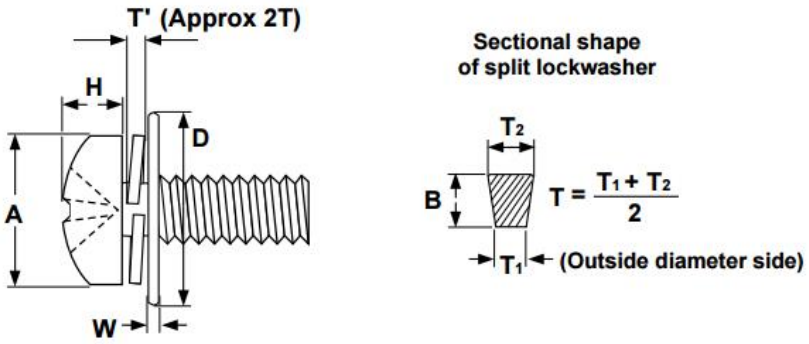
Do not shake or grasp the heatsink. Avoid any shock to the PCB by grasping only the heatsink. This can create cracks or break the package

8.2.1.3 Mounting screw

When we attach module to heat sink, we recommend M3 SEMS screws (JIS B1256/JIS B1188) as shown in Table 35.

Table 35 Recommended screw specifications (Typical)

Screw dimensions				Flat washer		Spring washer	
Size	Thread pitch	A	H	D	W	D1	B x T
		Head diameter	Head height	Outer diameter	Thickness	Outside diameter	
M3	0.5	5.2	2.0	7.8	0.58	5	1.1 x 0.7



8.3 Handling guidelines

When installing a module to a heat sink, excessive uneven tightening force might apply stress to inside chips, which will lead to breaking or degradation of the device. An example of recommended fastening order is shown in Figure 56.

- Do not over-torque when mounting the screws. Excessive mounting torque may cause damage to module holes as well as to the screws and heat sink.
- Avoid one-side tightening stress. Uneven mounting can cause the module holes to be damaged.

To get effective heat dissipation, it is necessary to enlarge the contact area as much as possible, which minimizes the contact thermal resistance.

Properly apply thermal conductive grease over the contact surface between the module and the heat sink, which is also useful for preventing the contact surface from corrosion. Furthermore, the grease should be of stable quality and long-term durability within a wide operating-temperature range. Use a torque wrench to tighten to the specified torque rating. Exceeding the maximum torque limitation might cause a module to be damaged or degraded. Make sure there is no dirt remaining on the contact surface between the module and the heat sink. All equipment used to handle or mount the IPM must comply with the relevant ESD standards. This

includes transportation, storage and assembly. The module itself is an ESD-sensitive device. It may therefore be damaged in case of ESD shocks.

Do not shake or grasp the heat sink; in particular, avoid any chocks to the PCB by grasping only the heat sink. This could cause package cracking or breaking.

8.4 Storage guidelines

8.4.1 Recommended storage conditions

Temperature: 5 ~ 35℃

Relative humidity: 45 ~ 75%

- Avoid leaving the IPM exposed to moisture or direct sunlight. In particular be careful during periods of rain or snow.
- Use storage areas where there is minimal temperature fluctuation.

Rapid temperature changes can cause moisture condensation on the stored IPM, resulting in lead oxidation or corrosion as a result, leading to degraded solderability.

- Do not allow the IM828-XCC to be exposed to corrosive gasses or dusty conditions.
- Do not allow excessive external forces or loads to be applied to the IPM while they are in storage.

8.5 Soldering conditions

8.5.1 Wave soldering

Wave soldering is a large-scale soldering process through which electronic components are soldered onto a PCB to form an electronic assembly. The name is derived from the soldering process — a tank is used to hold a quantity of molten solder, the components are inserted into or placed on the PCB and then the loaded PCB is passed across a pumped wave or cascade of the solder. The solder wets the exposed metallic areas of the board (those not protected with solder mask) creating a reliable mechanical and electrical connection.

The leads of trough-hole devices (THD) are long and straight at the end. Therefore, they can be inserted into the drill holes in the PCBs and be attached by wave soldering. Only the leads that extend through the drill holes in the PCB meet the hot solder. The body of the package is heated by the hot leads [8].

This method has two consequences:

- The package body stays cooler than in the case of reflow soldering
- The temperature gradient between the leads and the body and inside the package is greater than in the case of reflow soldering

Therefore, in a wave-solderable THD the heat resistance is tested according to JESD22-B106 and IEC668 2-20 (typically 260°C, 10 s).

Immersing the entire package body into the molten solder is not recommended because THDs are generally not suited for such harsh temperature shocks.
Dual-wave soldering is the most used wave-soldering method (see Figure 57). The peak temperatures, ramp rates, and time used depend on the material and the wave-soldering equipment.

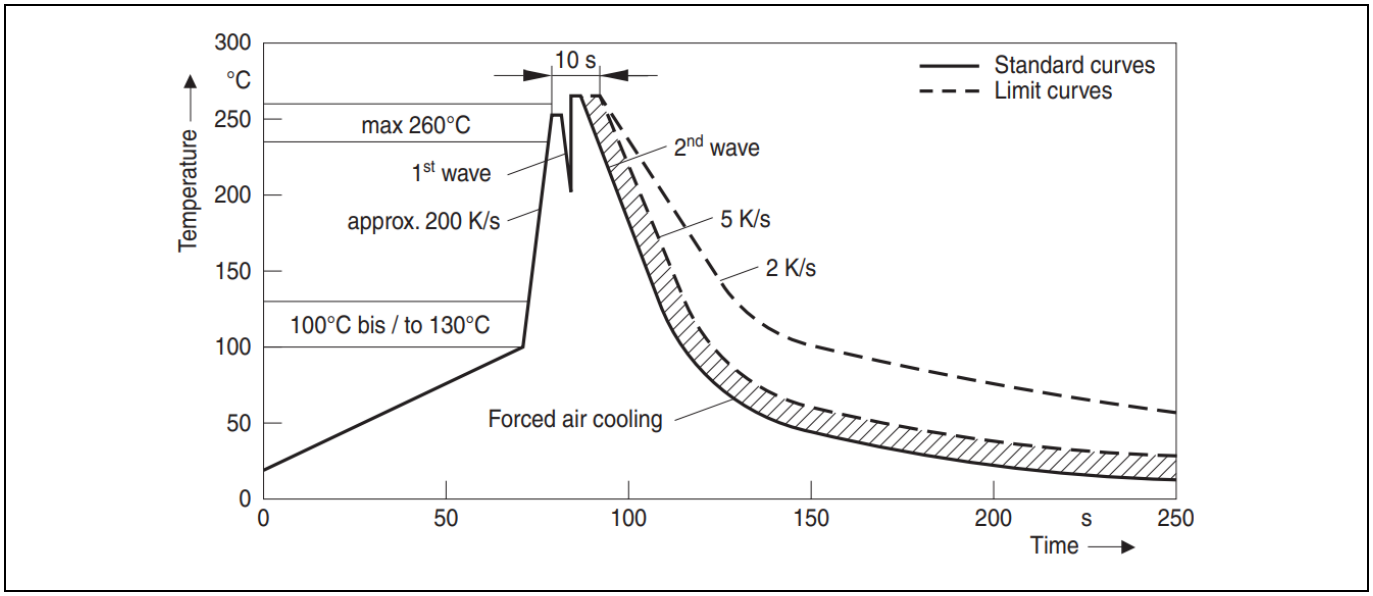


Figure 57 Typical dual wave soldering profile

8.5.2 Manual soldering

Considering the glass-transition temperature (T_g) of the package mold resin and the thermal-withstand capability of the internal chips and assembly, the temperature of the lead root should be kept below 150°C. The iron tip should touch the lead only at its tip, away from the package mold body. It is recommended that the soldering time be as short as possible.

Testing method with a manual solder iron: ATC-2450-3 (ARIM), 50 W:

- Put the soldering tip of the 50 W iron (temperature set to upper conditions) on the terminal (within 1 mm of the terminal end point) and measure the temperature rise in the root part of the terminal using the thermocouple installed on the terminal root

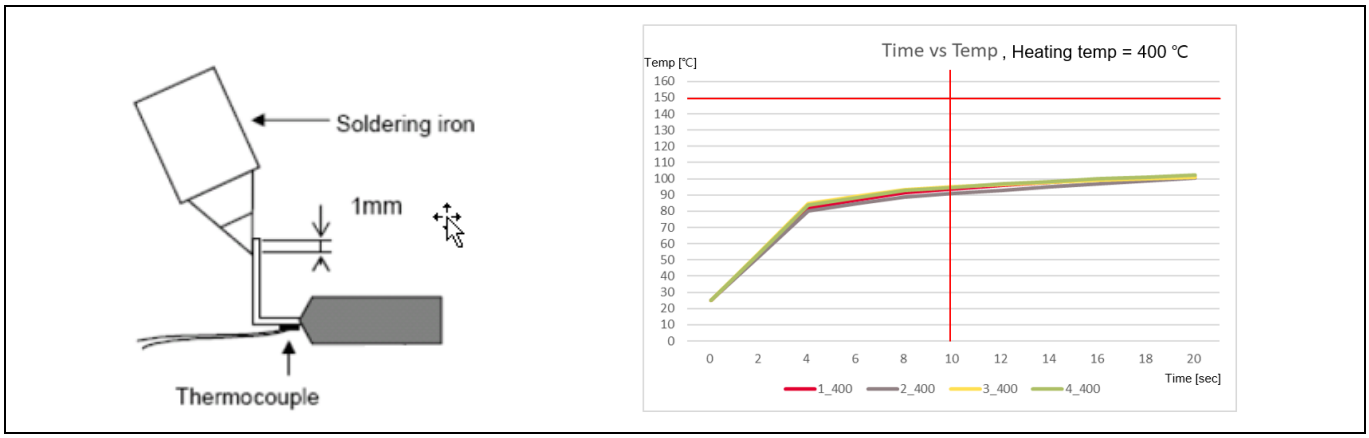


Figure 58 Heating and measuring point, temperature alteration of the terminal root (example)

Recommendations for manual soldering of the CIPOS™ IPM series:

- The available range of temperature is 350 – 400°C (for 10 seconds)
- A temperature over 400°C is not recommended as it can delaminate the lead after soldering
- Mass production is not recommended as it may be difficult to control the amount of solder applied

9 Package handling guidelines

9.1 Recommended storage conditions

Temperature: 5 – 40°C

Relative humidity:-10 – 75%

- Avoid leaving the CIPOS™ IPM exposed to moisture or direct sunlight. Be particularly careful during rainfall or snowfall
- Use storage areas that have minimal temperature fluctuation. Rapid temperature changes can create condensation on the stored CIPOS IPM, resulting in lead oxidation or corrosion and degraded soldering ability.
- DCB substrates are designed with a copper layer that is directly exposed to air, leading to natal oxidation process, but oxidized copper layers have no impact on the thermal performance [10].
- Do not allow the CIPOS IPM to be exposed to corrosive gasses or dusty conditions
- While storing, ensure that no excessive external forces or load is applied on the CIPOS IPM
- If storing the modules for a long time (more than one year), ensure they are kept dry
- Before using a module that has been in storage for a long time, ensure that there are no visible flaws, stains, or rust on the exterior

9.2 Packing specification

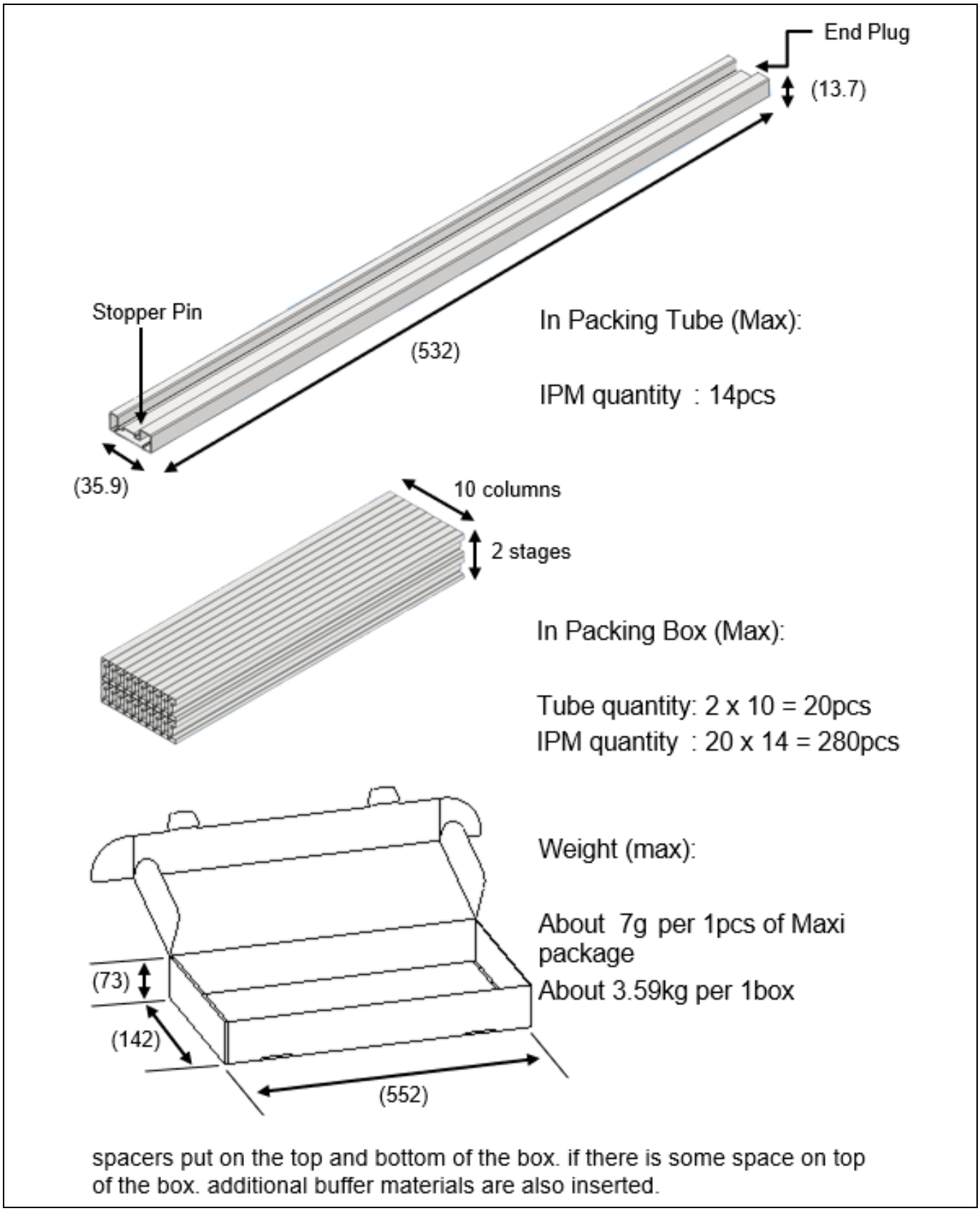


Figure 59 Packing information

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Revision History

Major changes since the last revision

Version Number	Revision date	Description of change
1.00	2020-09-22	Initial release
1.01	2021-09-06	Changed Figure 5 Corrected data in Table 32 (Clearance for signal pin: 4.12mm → 3.33mm)
2.0	2025-07-21	Adding a new product information

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