EiceDRIVER™ 1ED34x1 and 1ED38x0 Enhanced family

Technical description

1ED34x1Mc12M (1ED-X3 Analog), 1ED38x0Mc12M (1ED-X3 Digital)
Single-channel 5.7 kV (rms) isolated gate driver IC with adjustable DESAT and soft-off or I2C configurability

About this document

The Infineon EiceDRIVER™ 1ED34x1 and 1ED38x0 Enhanced products are single-channel high-voltage gate driver ICs with integrated coreless transformer (CLT) technology. The ICs are designed for use with 650 V, 1200 V, 1700 V, and 2300 V IGBTs, silicon and silicon-carbide MOSFETs.

Scope and purpose

The scope of this application note includes an explanation of general gate driver input and output features, and a description of how to use them in an application.

Intended audience

This document is intended for application circuit designers and concept engineers in power electronics.

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1 Introduction

The Infineon EiceDRIVER™ 1ED34x1 and 1ED38x0 Enhanced products are available in a fine pitch 300 mil package. All variants have UL 1577 certification with either resistor programmable or I2C configurable product and safety features.

1ED34x1 Enhanced (1ED-X3 Analog) with resistor programmable features

There are six variants in the wide body PG-DSO-16 (300 mil) package. 3 A current variants have a direct Miller clamp output and the higher output current variants have a Miller clamp pre-driver and require an external MOSFET for clamping.

Product type	Output current	CLAMP type[1)]	Isolation class	Marking	OPN
1ED3431MC12M	3 A (typ)	CLAMP	reinforced	3431MC12	1ED3431MC12MXUMA1
1ED3461MC12M	6 A (typ)	CLAMPDRV	reinforced	3461MC12	1ED3461MC12MXUMA1
1ED3491MC12M	9 A (typ)	CLAMPDRV	reinforced	3491MC12	1ED3491MC12MXUMA1
1ED3431MU12M	3 A (typ)	CLAMP	UL 1577	3431MU12	1ED3431MU12MXUMA1
1ED3461MU12M	6 A (typ)	CLAMPDRV	UL 1577	3461MU12	1ED3461MU12MXUMA1
1ED3491MU12M	9 A (typ)	CLAMPDRV	UL 1577	3491MU12	1ED3491MU12MXUMA1

1ED38x0 Enhanced (1ED-X3 Digital) with I2C configurable features

There are six variants in the wide body PG-DSO-16 (300 mil) package. The Miller clamp type is always configurable via I2C independent of the output current strength.

Product type	Output current	Isolation class	Marking	OPN
1ED3830MC12M	3 A (typ)	reinforced	3830MC12	1ED3830MC12MXUMA1
1ED3860MC12M	6 A (typ)	reinforced	3860MC12	1ED3860MC12MXUMA1
1ED3890MC12M	9 A (typ)	reinforced	3890MC12	1ED3890MC12MXUMA1
1ED3830MU12M	3 A (typ)	UL 1577	3830MU12	1ED3830MU12MXUMA1
1ED3860MU12M	6 A (typ)	UL 1577	3860MU12	1ED3860MU12MXUMA1
1ED3890MU12M	9 A (typ)	UL 1577	3890MU12	1ED3890MU12MXUMA1

Nomenclature

1ED3vivMc12M: Lower case letters in the product name are placeholders for a single digit of the original product name.

- Product type (v_v): 4i1 = resistor programmable, 8i0 = I2C configurable
- Product variant (i): single digit typical output current (3/6/9 A)
- Type of insulation certification (c): C = IEC 60747-17 and UL 1577 certified insulation, U = UL 1577 certified insulation

[1] Please refer to CLAMP output types for circuit connection to avoid damage to the gate driver IC

2 1ED34x1 specific feature description

2.1 Power-up and resistor programmable feature configuration

The input side of the gate driver IC requires up to 200 µs to be ready for configuration resistor sampling after the *VCC1* pin voltage reaches its UVLO threshold level.

To ensure stable resistor sampling the gate driver IC requires sufficient capacitive buffering at the input supply pins *VCC1* to *GND1* of at least $C_{VCC1} \geq 100$ nF. Always use low ESR type capacitors and place them close to the supply pins (< 1 cm).

Each resistor programmable input pin (*ADJA*, *ADJB*) differentiates between 16 specific resistor values from the E96-series having 1% tolerance. A value from another resistor series and outside of the specified tolerance will fall back to one of the specified resistor values and results in their associated configuration. However the flipping point outside of the tolerance band is not specified and therefore the resulting configuration will either be the one from the lower or higher specified configuration resistor step.

The resistor value will only be evaluated once during start-up and again after each power supply loss. It is not possible to change the configuration during operation by swapping resistor values since the gate driver IC requires a power cycle for each change.

The input side selected configuration can only be transferred after a successful output side power-up. The IC signals this readiness by releasing the pin *RDYC* to high.

2.2 Analog DESAT adjustment

The 1ED34x1 (1ED-X3 Analog) has a comfortable method to adjust the DESAT detection from the input side of the gate driver IC. The *ADJB* pin requires a simple resistor to influence the leading edge blanking time and DESAT filter time without any additional components on the output side.

This simplifies the application circuit and also minimizes the influence of external component tolerances on the DESAT detection timings.

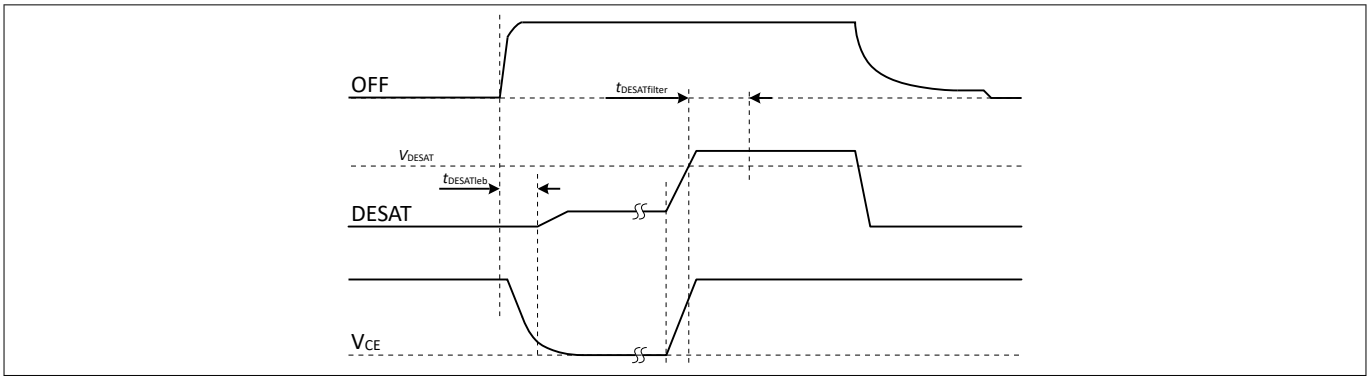

Figure 1 *ADJB* influence on DESAT parameter $t_{DESATleb}$ and $t_{DESATfilter}$

This diagram shows the starting point of the leading edge blanking time $t_{DESATleb}$ and the DESAT filter time $t_{DESATfilter}$ in correlation to signals available to the gate driver IC. The leading edge blanking starts as soon as the output turns on. The IC monitors this at the *OFF* pin. The rising *DESAT* pin voltage starts the DESAT filter after the voltage went over the DESAT threshold voltage V_{DESAT}.

The DESAT filter time uses a so called up-reset digital filter implementation. As soon as the DESAT pin voltage is above the DESAT threshold voltage the filter time elapses. However if the DESAT pin voltage drops even briefly below the DESAT threshold voltage, the filter resets and starts again. Noisy environments can therefore rely on a shorter filter time and still get a robust detection.

The configuration at the *ADJB* pin is as described in the datasheet:

- A resistor from *ADJB* to *GND1* sets the DESAT leading edge blanking time and the DESAT filter time used during DESAT detection
- Use resistors from the E96 resistor-series with 1% tolerance values to achieve accurate parameter configuration

- The gate driver IC reads the resistor value once during start-up
- Connecting *ADJB* to *GND1* inhibits the gate driver operation and stops the start-up sequence
- Connecting *ADJB* to *VCC1* disables the filtering resulting in minimum response times

Table 1 DESAT filter timing ADJB adjustment

DESAT filter time set up	**stopped**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
Resistance at *ADJB* to *GND1*	< 1.05 kΩ or tied to *GND1*	1.33 kΩ	1.58 kΩ	1.91 kΩ	2.26 kΩ	2.74 kΩ	3.32 kΩ	4.02 kΩ	4.87 kΩ
typ. $t_{DESATleb}$	inhibit gate driver operation	650 ns	650 ns	650 ns	650 ns	650 ns	650 ns	650 ns	650 ns
typ. $t_{DESATfilter}$		1575 ns	1775 ns	1975 ns	2375 ns	2775 ns	3175 ns	3575 ns	3975 ns
DESAT filter time set up	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**default**
Resistance at *ADJB* to *GND1*	5.90 kΩ	7.15 kΩ	8.66 kΩ	10.7 kΩ	13.7 kΩ	17.4 kΩ	23.2 kΩ	28.0 kΩ	>45.3 kΩ or tied to *VCC1*
typ. $t_{DESATleb}$	1150 ns	1150 ns	1150 ns	1150 ns	1150 ns	1150 ns	1150 ns	1150 ns	400 ns
typ. $t_{DESATfilter}$	3975 ns	3575 ns	3175 ns	2775 ns	2375 ns	1975 ns	1775 ns	1575 ns	*225* ns

In some cases the application needs to implement a solution with an external DESAT filter. The gate driver IC supports this classic DESAT structure, even though the accuracy of the overall DESAT detection depends then mainly on the external components.

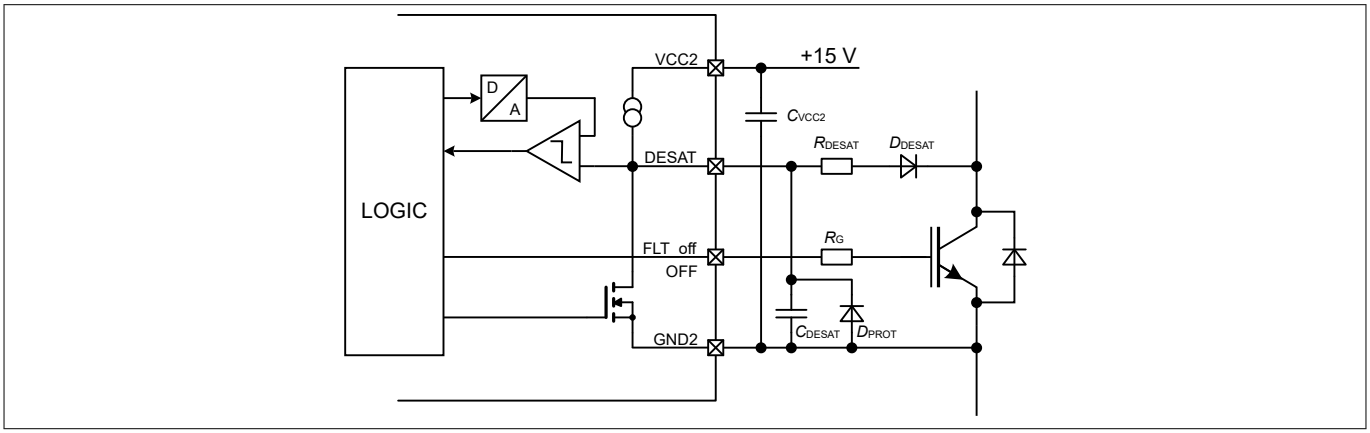

Figure 2 Circuit example for DESAT with external capacitor

This diagram only shows relevant pins and connection points to the external capacitor C_{DESAT}. The additional diode D_{PROT} is required in application cases where the *DESAT* pin voltage drops below the absolute minimum pin rating.

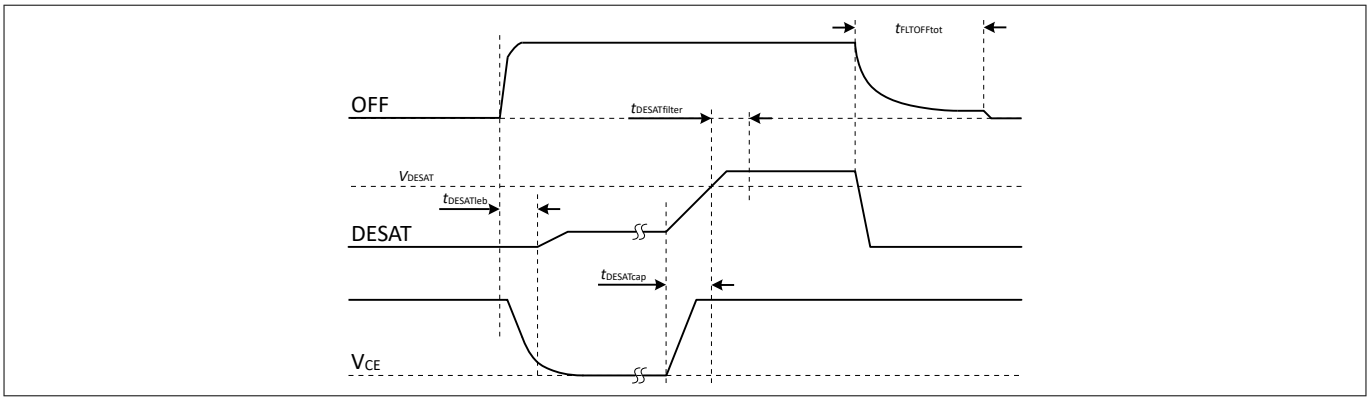

Figure 3 Timing influence of external DESAT capacitor on overall filtering

In case of a short circuit, the external DESAT capacitor C_{DESAT} slows down the rising voltage at the *DESAT* pin. It therefore increases the total filter time until DESAT detection.

In a short circuit situation, the DESAT diode D_{DESAT} blocks the current path of the internal current source I_{DESAT}. Instead this current charges the DESAT capacitor C_{DESAT}. This additional filter time $t_{DESATcap}$ can be estimated as follows:

$$t_{DESATcap} = C_{DESAT} \cdot \frac{V_{DESAT}}{I_{DESAT}}$$

Equation 1

For more accurate calculations also include the tolerances of the capacitor, the range of the DESAT current source, and the DESAT threshold voltage with respect to the collector-emitter saturation voltage and the DESAT diode forward voltage.

3 1ED38x1 specific feature description

3.1 Power-up and I2C readiness

The input side of the gate driver IC requires up to 200 µs to be ready for I2C operation after the *VCC1* pin voltage reaches its UVLO threshold level.

To ensure uninterrupted I2C operation the gate driver IC requires sufficient capacitive buffering at the input supply pins *VCC1* to *GND1* of at least $C_{VCC1} \geq 100$ nF. Always use low ESR type capacitors and place them close to the supply pins (< 1 cm).

After an initial power-up, the gate driver IC expects the address configuration followed by the remaining register configuration before signaling IC readiness. These steps are always required after an input side supply loss unless the configuration includes a configuration recovery from output side and the supply loss was limited to the input side. If the register bit **RECOVER**.RECOVER is set, the input side tries to recover the address and register configuration from the output side and signals the IC readiness immediately after. In this case, the gate driver IC will be addressable by the previously set I2C addresses. However if the recovery fails, the gate driver IC resets to its default I2C address. The controlling microcontroller should therefore be prepared to handle this address mismatch for various power-up sequences.

3.2 Short input pulses at two-level turn-off operation

The 1ED38x0 gate driver IC two-level turn-off behavior for short input pulses is depending on the gate load conditions as well as internal register configurations.

In a normal two-level turn-off operation mode, the gate driver IC additionally delays the turn-on by the same duration as the configured two-level turn-off time to achieve pulse matching. This also results in an increase of the minimum input pulse length to longer pulses than the previously mentioned two-level turn-off time. Input ON pulses shorter than this time will be suppressed by the gate driver IC. After that, the gate driver IC activates its output and starts charging the gate. Depending on the gate load, the gate driver IC needs a certain time to charge the gate up to the two-level turn-off level and later to *VCC2* level.

The gate driver IC monitors the actual gate voltage via the *ON* and *OFF* pins and has a comparator for the TLTOff plateau voltage. The IC filters all pin voltage comparator signals before applying the result to internal processing. This filter time is the CLAMP and pin monitoring filter configured in register **CLCFG**.

The turn-off behavior of the gate driver IC for such short pulses therefore depends on the ON pulse length $t_{ONpulse}$ compared to

- the actual two-level turn-off time t_{TLTOff},
- the gate load dependent rise time until the TLTOff plateau voltage is reached $t_{RISE,load}$,
- the selected pin monitoring filter time $t_{CLFILT,x}$, and
- an internal processing time $t_{IntProc}$ of 25 ns (max).

To ensure a full and uninterrupted two-level turn-off switching make sure to limit the minimum turn-on pulse length by software to a value larger than the above mentioned timings:

$$t_{ON,\,min} \geq t_{TLTOff} + t_{RISE,\,load} + t_{CLFILT,\,x} + t_{IntProc}$$

Turn-on pulses in between $t_{TLTOff} < t_{ONpulse} < t_{ON,min}$ can have incomplete and undetermined pulse forms ranging from

- short turn-on peaks ($t_{TLTOff} < t_{ONpulse} < t_{TLTOff} + t_{RISE,load}$), not shown
- short turn-on with ramp B turn-off ($t_{TLTOff} + t_{RISE,load} < t_{ONpulse} < t_{TLTOff} + t_{RISE,load} + t_{CLFILT,x}$), see Figure 4: top waveforms
- jitter between ramp B turn-off and full TLTOff sequence ($t_{TLTOff} + t_{RISE,load} + t_{CLFILT,x} < t_{ONpulse} < t_{ON,min}$), see Figure 4: middle waveforms, and
- complete TLTOff sequence ($t_{ONpulse} > t_{ON,min}$), see Figure 4: bottom waveforms

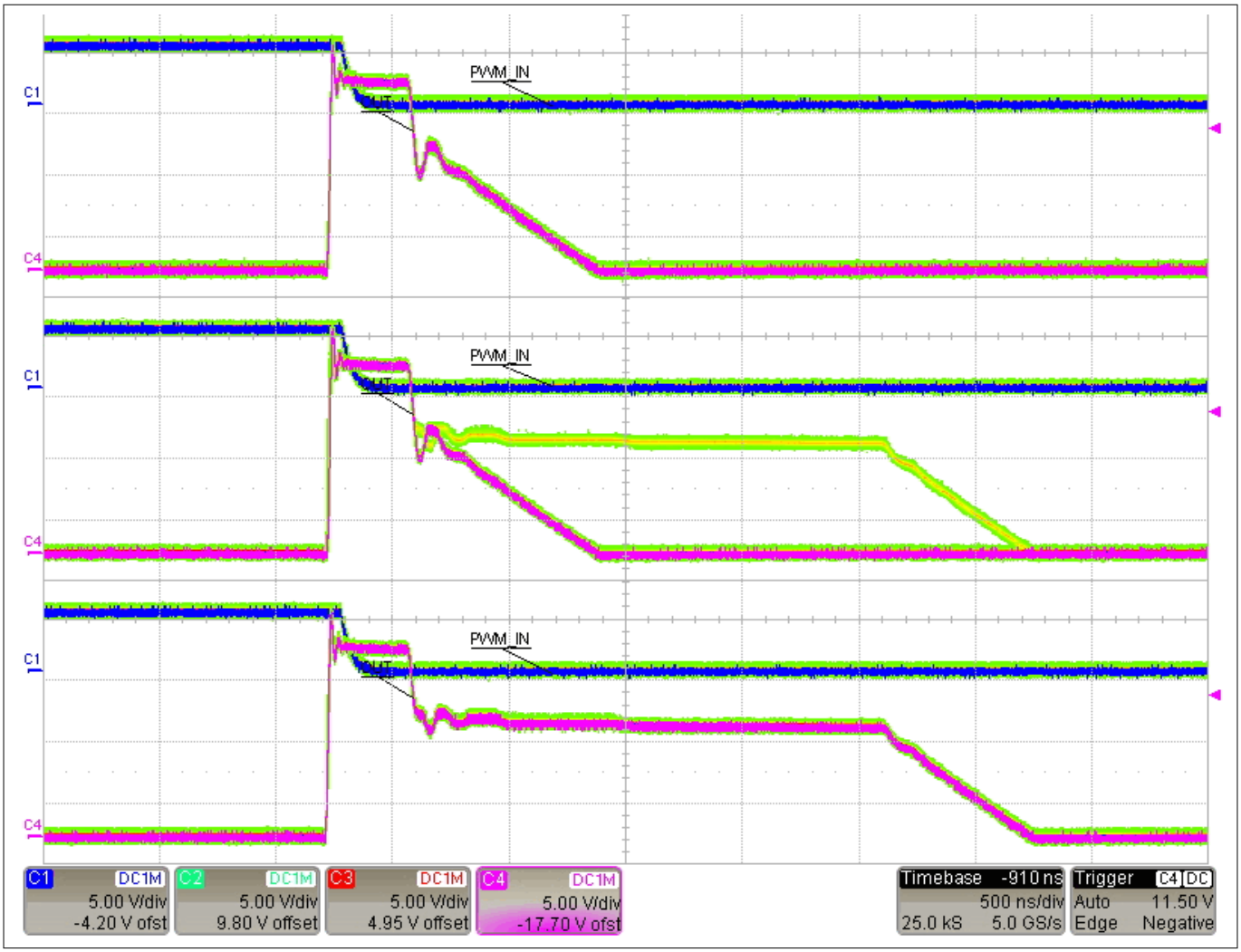

Figure 4 Combined image of two-level turn-off short pulse operation with minimal gate load

Gate driver IC configuration:

- TLTOff level: 9 V, TLTOff RA: 60 V/µs, TLTOff duration: 2 µs, TLTOff RB: 15 V/µs
- Filter for CLAMP and pin status monitoring: 370 ns

3.3 Switch-off time-out behavior with fault latching

The gate driver IC monitors the switch-off duration. However only with the 1ED38x0 is this feature configurable in both timing and fault latching behavior. This section describes the behavior when the configuration option with *FLT_N* latching to low after a timeout detection is enabled.

The whole timeout monitoring only becomes interesting for the application in case a weak connection along the regular discharge path via gate, gate turn-off resistor ($R_{G,OFF}$), and *OFF* pin. This weak connection prohibits the gate driver to lower the monitored gate voltage below the OFF detection threshold of *VEE2* + 2 V. In all other cases where the gate voltage fall time ($t_{gate,fall}$) is shorter than the configured switch-off time-out time (t_{CTT}) the PWM operation is not influenced by the timeout monitoring feature. This is still independent of the configuration of the fault latching behavior.

To enable the fault reporting of a switch-off timeout detection, the application needs to configure the register bit **SOTOUT**.SOTOUT_F to 1_B.

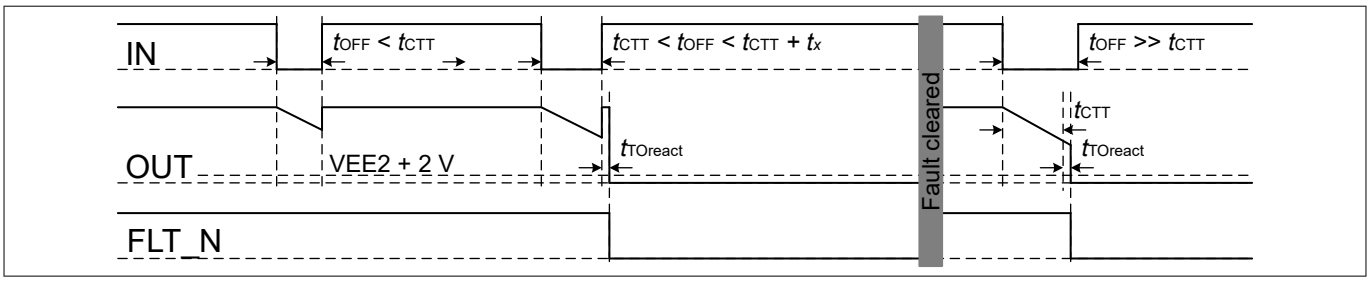

Figure 5 Switch-off timeout monitoring with fault latching

Parameters used in diagram:

- t_{OFF}: duration of OFF pulse
- t_{CTT}: configured timeout time according to register bits **SOTOUT**.SOTOUT_T
- t_x: timeout tolerance including gate driver internal processing time ($t_{x,max}$ = 100 ns)
- $t_{TOreact}$: reaction time of gate driver to activate all turn-off paths and reporting of fault condition

The switch-off timeout behavior with long gate voltage fall times can be divided into three time segments:

- $t_{OFF} < t_{CTT}$: The OFF pulse is too short to trigger the switch-off timeout, the gate driver simply turns the output on with the rising edge of the *IN* signal.
- $t_{CTT} < t_{OFF} < (t_{CTT} + t_x)$: The OFF pulse is slightly longer than the switch-off timeout time. However the output has already started to turn-on again before the timeout condition is propagated through the internal gate driver logic to shutdown and report the fault.
- $t_{OFF} >> t_{CTT}$: The OFF pulse is much longer than the switch-off timeout time. The output will be forced to shutdown by all available means (hard switch-off and *CLAMP*) and the gate driver IC pulls the *FLT_N* pin to low.

Please note, that the slow turn-off of the output can also result in a shoot-through event at the inverter stage which could trigger a secondary fault detected by the DESAT protection.

4 Implementation specific feature behavior

4.1 High inductance connection to gate load using soft turn-off

It is always good practice to keep the gate loop inductance to a minimum while designing the gate driver circuit. However not all application circuits allow for the gate driver IC to be placed close to the power switch. These cases require extra care for soft turn-off operation.

The gate driver IC implements the soft turn-off function using an internal control loop to limit the maximum sink current during a fault-off event. Therefore the application does not need an additional external high ohmic resistor connected to a separate pin of the gate driver IC. Instead the *OFF* pin itself acts as soft-off pin and uses the configured soft-off current to discharge the gate during fault-off. In circuits having a long wire track between gate driver IC and gate of the power switch, the soft-off control loop can cause a current ringing at the gate driver IC when operated with a low soft-off current setting.

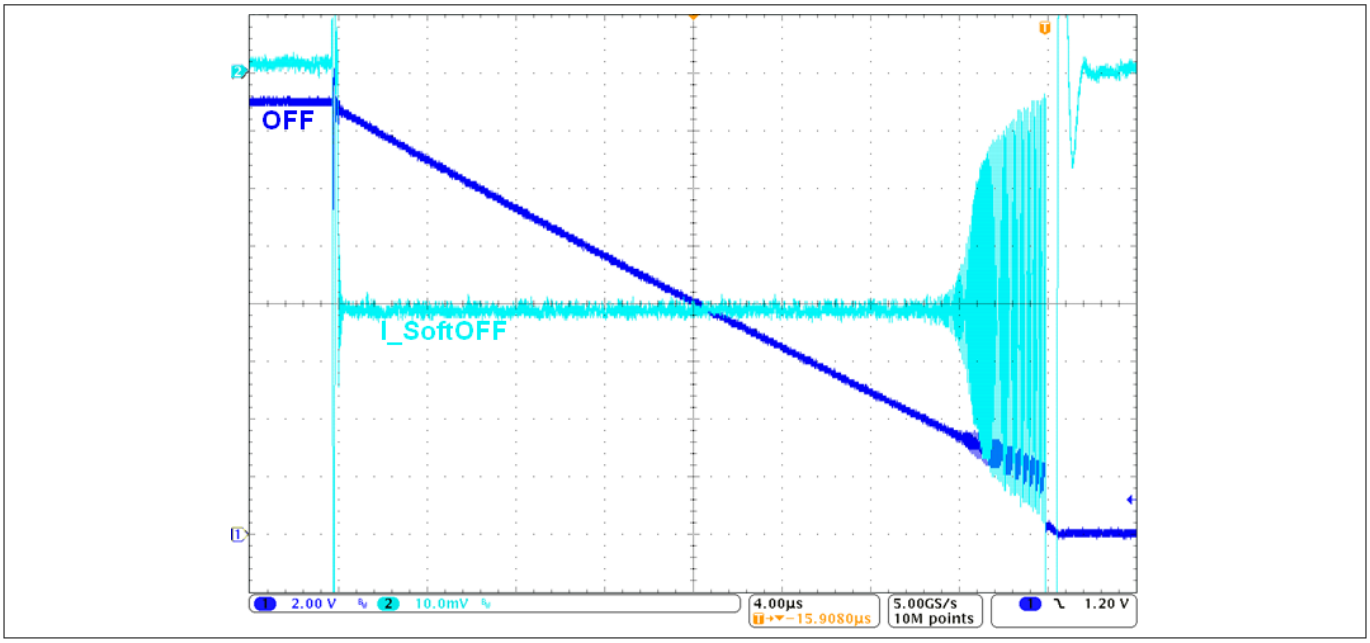

Figure 6 Soft-off behavior at high load, long gate loop and low soft-off current

Measurement setup:

- 1 Ω gate resistor used as shunt for $I_{SoftOFF}$ current measurement on channel 2
- 100 nF capacitor as gate load
- 200 mm wire loop connecting the *OFF* pin to the load and monitoring on channel 1
- < 50 mA soft turn-off current setting

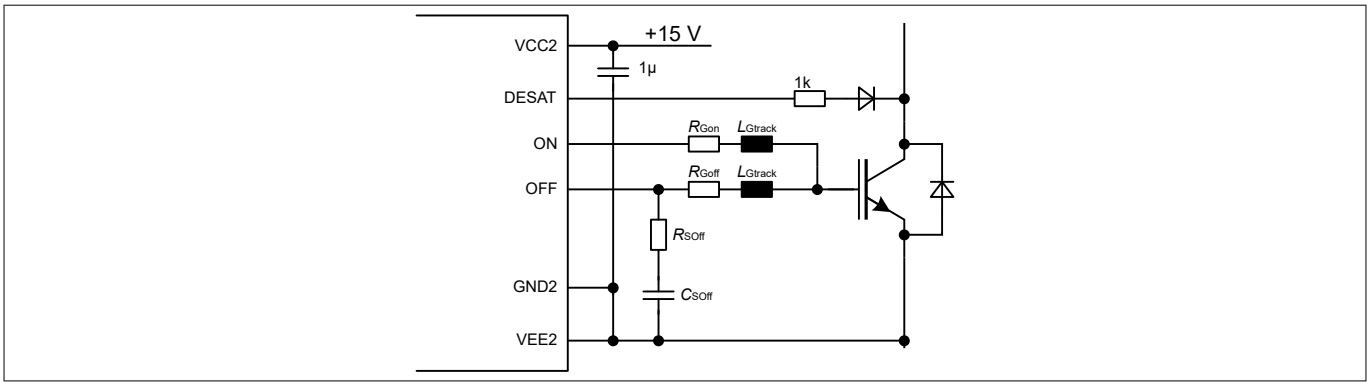

Figure 7 Optimize circuit for stable high load, long gate loop and low soft-off current situations

To overcome this ringing, a small capacitor and series resistor directly at the *OFF* pin stabilizes the soft-off control loop. This example schematic indicates the long but unintended gate loop as L_{Gtrack}. Depending on the gate resistor R_{Goff} and the equivalent gate charge C_{Gate} the following guidelines give good starting values for the additional components to stabilize the loop:

- $R_{SOff} \leq 10 \times R_{Goff}$
- $C_{SOff} = 0.01 \times C_{Gate}$

The additional resistor should be big enough and the capacitor small enough not to influence the normal switching behavior and also not influence the thermal behavior of the gate driver IC. And even with the ringing of the soft-off current, the safety of the application is not at risk and can operate as intended.

4.2 Overall supply UVLO of output side responsible for IC reset

The gate driver ICs have fast UVLO detection for the *VCC2* to *GND2* supply to ensure low on-state losses at the IGBT. The remaining overall supply voltage between *VCC2* and *VEE2* defines if the gate driver IC stays internally operational or transitions into reset.

This internal *VCC2 - VEE2* UVLO threshold is at approximately 7 V. An overall voltage drop at the output side supply pins will not result in an output side reset as long as the remaining voltage stays above this value.

The following conditions occur in applications with unipolar supply (*VEE2 = GND2*):

- *VCC2 - GND2* > V_{UVLO2H}: The gate driver IC supply is ready for operation.
- V_{UVLO2L} > *VCC2 - GND2* > *VCC2 - VEE2* UVLO: The gate driver IC is internally ready but does not allow PWM operation.
- *VCC2 - VEE2* UVLO > *VCC2 - GND2*: The gate driver IC is in output side reset state and requires the product specific power-up sequence for a restart.

The following conditions occur in applications with bipolar supply (*VEE2 < GND2*) assuming there is no additional *VEE2* UVLO configured:

- *VCC2 - GND2* > V_{UVLO2H}: The gate driver IC supply is ready for operation.
- *VCC2 - VEE2* > *VCC2-VEE2* UVLO: The gate driver IC is internally ready but does not allow PWM operation.
- *VCC2 - VEE2* UVLO > *VCC2 - VEE2*: The gate driver IC is in output side reset state and requires the product specific power-up sequence for a restart.
- *VEE2* > *GND2*: The gate driver IC is also in output side reset state and requires the product specific power-up sequence for a restart.

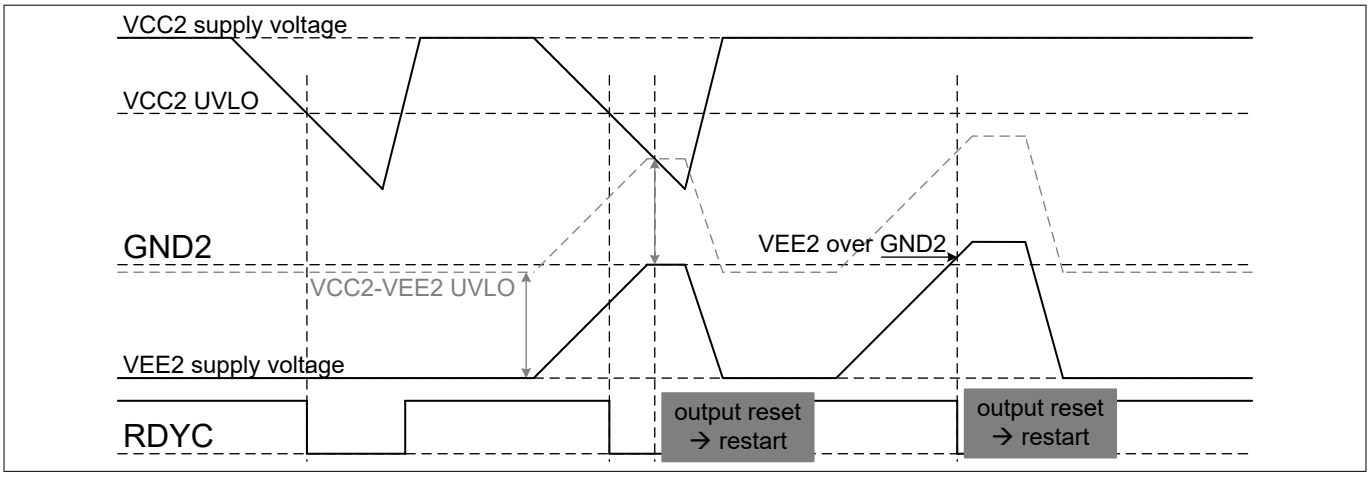

Figure 8 Overall supply UVLO of output side with output reset conditions

The restart after an output side reset requires apart from the product specific power-up action also that the supply voltages are in their respective operational ranges. The actions for supply recovery and restart are not shown in this diagram.

5 Design aspects

The design aspects describe gate resistor and output supply capacitor selection as well as the power dissipation estimation for a selected design.

5.1 External Components

The gate driver ICs are designed to require as few external components as possible. This section shows some of these components and their usable application range and limits.

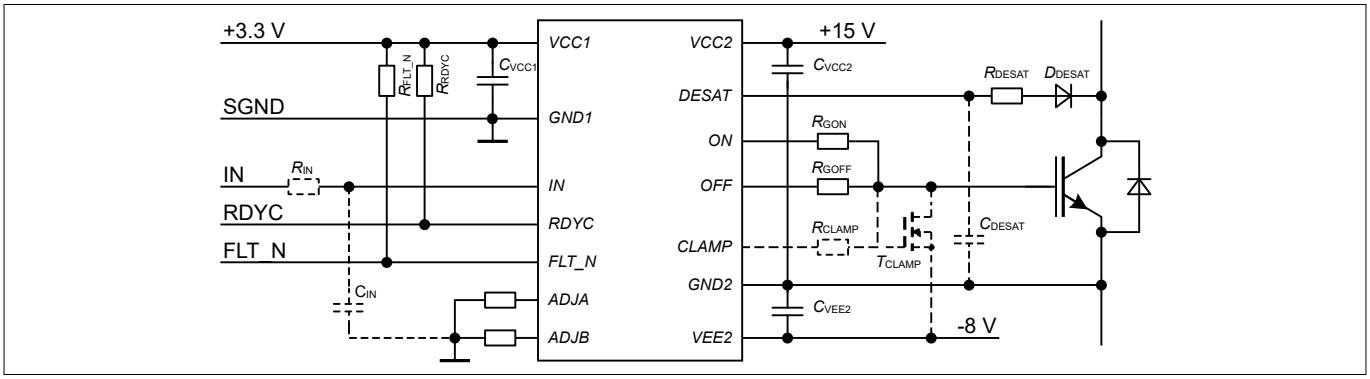

Figure 9 1ED34x1 (1ED-X3 Analog) application example with bipolar power supply

Dashed components at the input side are optional and depend on the application requirements to protect the circuit against EMI. Additional filters at the *FLT_N* and *RDYC* pins are possible in a similar way to the shown *IN* pin filter. The *CLAMP* pin connection at the output side depends on the gate driver IC output current class and its impact on the pin configuration as regular clamp or clamp pre-driver output. The optional DESAT capacitor C_{DESAT} simply enlarges the DESAT filter options.

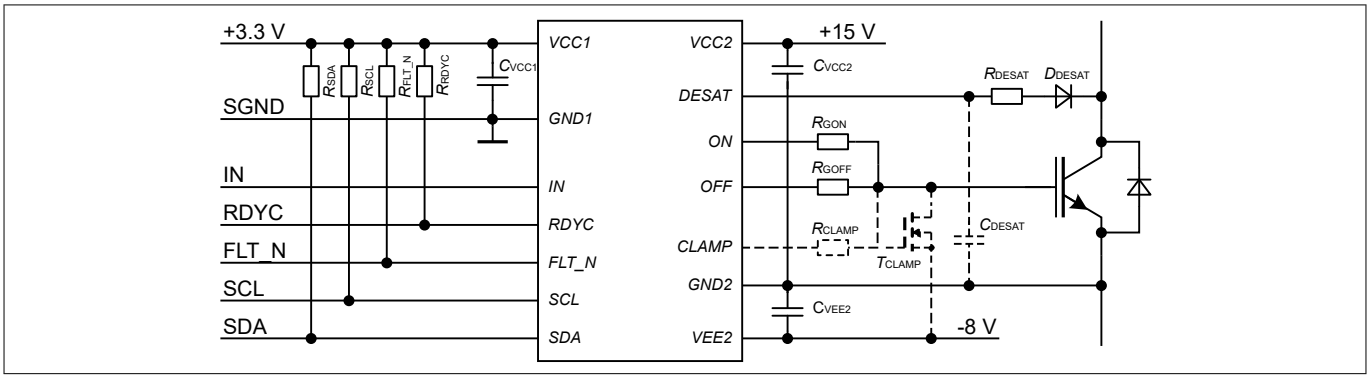

Figure 10 1ED38x0 (1ED-X3 Digital) application example with bipolar power supply

The input side can implement filters at the *IN*, *FLT_N*, and *RDYC* pins to protect the circuit against EMI. The filters are not shown. The *CLAMP* pin connection at the output side depends on the gate driver IC register configuration of this pin. Appropriate components for the operation as regular clamp or clamp pre-driver output need to be selected. The optional DESAT capacitor C_{DESAT} simply enlarges the DESAT filter options.

In a bipolar supply configuration, it is also recommended to add a capacitor between the pins *VCC2* and *VEE2* even though it is not shown here. All capacitors should be of X7R or similar type with low ESR. The capacitors should be placed as close to the individual supply pins as possible.

Table 2 External components

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Decoupling input side	C_{VCC1}	0.1	1	–	µF	–
SDA, *SCL* pull up against input supply	R_{SDA}, R_{SCL}	150	–	–	Ω	according to I2C-bus specification
SDA, *SCL* pull up current	I_{SDA}, I_{SCL}	–	–	20	mA	according to I2C-bus specification
FLT_N, *RDYC* pull up against input supply	R_{FLT_N}, R_{RDYC}	1	–	–	kΩ	total value of all parallel resistors
FLT_N, *RDYC* filter capacitor typ. at µC side	C_{FLT_N}, C_{RDYC}	–	–	22	nF	total value of all parallel capacitors
Decoupling capacitor output side positive rail	C_{VCC2}	0.1	1	–	µF	VCC2 ripple <1 V
Decoupling capacitor output side negative rail	C_{VEE2}	0.1	1	–	µF	VEE2 ripple <1 V
Decoupling capacitor output side overall supply pins	$C_{VCC2,VEE2}$	0.1	–	–	µF	supply ripple <1 V
DESAT protection resistor	R_{DESAT}	1	–	10	kΩ	–
DESAT external timing capacitor	C_{DESAT}	0	–	1000	pF	optional
Total *ON* gate resistance 1ED3x3xM	R_{GON}	2	–	–	Ω	–
Total *OFF* gate resistance 1ED3x3xM	R_{GOFF}	2	–	–	Ω	–
Total *ON* gate resistance 1ED3x6xM, 1ED3x9xM	R_{GON}	1	–	–	Ω	–
Total *OFF* gate resistance 1ED3x6xM, 1ED3x9xM	R_{GOFF}	1	–	–	Ω	–

Gate driver ICs with reinforced rated isolation capability need to be protected against electrical overstress. E.g. against a maximum output current or maximum power dissipation. A higher gate resistor value might be required to fulfill these requirements.

5.1.1 Output supply capacitor selection

A general design rule for the location of the driver output supply capacitor is always as close to the IC's supply pins *VCC2* and *VEE2* as possible.

Additionally, the value of the capacitor needs to be big enough to limit the voltage drop during the power switch turn-on. The following equation helps to calculate a first approximation for this capacitor.

$$C_2 = \frac{I_{Q2} \cdot t_p + Q_G}{\Delta V_{CC}} \cdot 1.2$$

Equation 2

I_{Q2} is the gate driver supply current, t_P the period of the switching frequency, Q_G the total gate charge at the selected operating condition, and ΔV_{CC} the maximum allowable voltage variation. The additional margin of 20% covers typical tolerances of capacitor and gate charge parameters.

Calculating this for the 100 A module FP100R12KT4 with Q_G = 800 nC, a switching frequency of f_{sw} = 15 kHz and an acceptable voltage variation of ΔV_{CC} = 0.2 V results in

$$C_2 = \frac{4\,\text{mA} \cdot 67\,\mu\text{s} + 800\,\text{nC}}{200\,\text{mV}} \cdot 1.2$$

$$C_2 = 5.6\,\mu\text{F}$$

Equation 3

5.1.2 Gate resistor selection

To optimize the gate resistor, it is recommended to have the appropriate gate charge diagram of the IGBT used and the output characteristic of the gate driver available. Both diagrams depend on operation conditions such as DC-link voltage (V_{DC}), collector current (I_C) and operating temperature.

The following representative diagrams show typical behaviors of an IGBT and the gate driver IC output without scale.

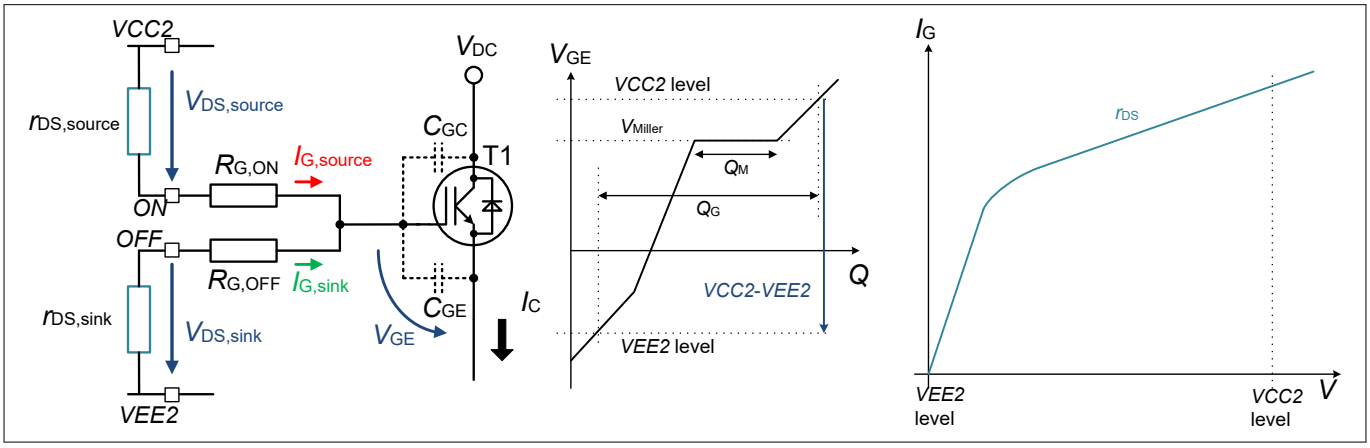

Figure 11 Simplified gate circuit, IGBT gate charge diagram and driver output characteristics

The MOSFET-based gate driver outputs can be simplified as dynamic resistors ($r_{DS,source}$; $r_{DS,sink}$) with a voltage drop ($V_{DS,source}$; $V_{DS,sink}$) during switching. The total gate charge (Q_G) and the Miller charge (Q_M) can be extracted from the gate charge diagram using the given gate driver supply V_{CC2} and DC-link voltage.

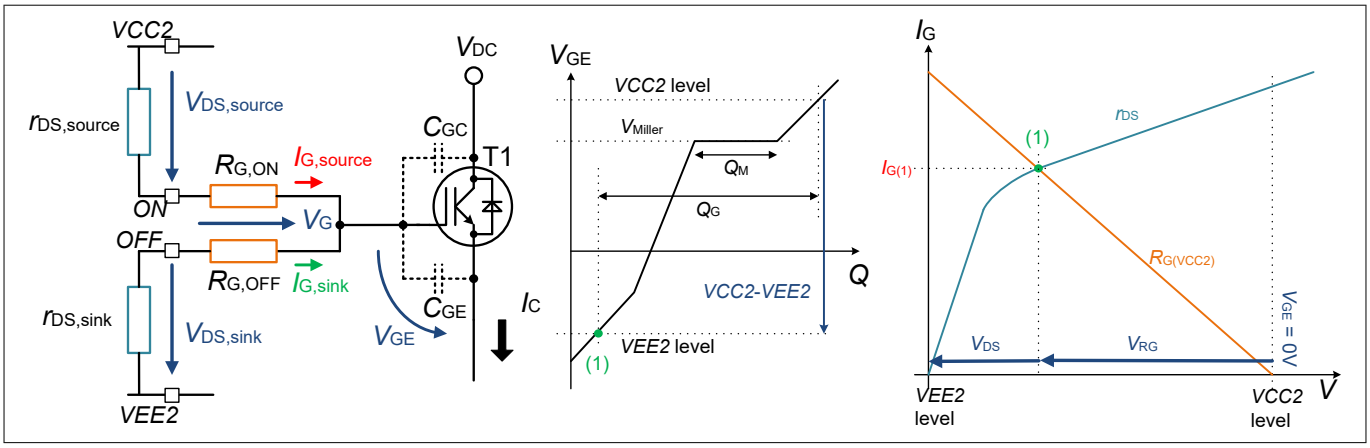

Figure 12 Simplified gate circuit turn-on event: Initial phase

In the initial phase of an IGBT turn-on event the gate is discharged and at the level of the *VEE2* pin. In the diagram this is marked with (1). Therefore the total gate supply voltage is split between the inner gate driver resistance ($r_{DS,source}$) and the turn-on gate resistor ($R_{G,ON}$). The graphical solution shows the initial gate current ($I_{G(1)}$) which can be located in the linear or in the saturated region of the gate driver output characteristic. This maximum current can also be used to select the appropriate pulse current class for the gate resistor.

Immediately after the initial phase, the gate current starts to fall, following the crossing point of the output characteristic curve and the parallel translated gate resistor line while the gate-emitter voltage (V_{GE}) charges up.

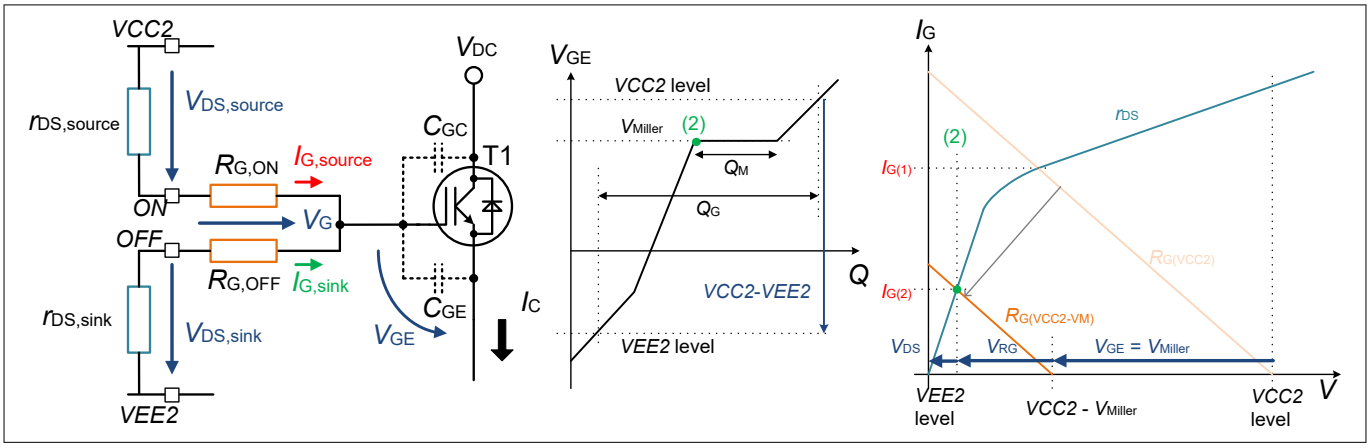

Figure 13 Simplified gate circuit turn-on event at Miller plateau

Beginning with the Miller plateau, marked with (2) above, the gate-emitter voltage remains nearly constant while the transistor is reducing the collector-emitter voltage to its saturation level.

Given the condition at that phase, the resulting gate current is constant allowing a collector-emitter voltage transition time (t_{ON}) calculation with the following formula:

$$t_{ON} = \frac{(R_{G,ON} + r_{DS,source(2)})}{(V_{CC2} - V_M)} \cdot Q_M$$

$$t_{ON} = \frac{1}{I_{G(2)}} \cdot Q_M$$

Equation 4

Tuning the value of a gate resistor requires extensive knowledge of all the parasitics in the gate circuit. It is therefore an iterative process of adjusting between switching losses and EMI.

5.1.3 DESAT diode selection

A fitting DESAT diode is an integral part of a robust desaturation protection. This section describes the important parameters and how to select a fitting component.

The DESAT diode has to fulfill similar requirement as a bootstrap diode. The diode needs

- a fast reverse recovery time,
- a low reverse recovery current, and
- a low pn-junction capacitance.

In addition and depending on the application operating conditions, the diode needs to fulfill the requirement for the reverse blocking voltage, operating temperatures and mechanical parameters. To fulfill the higher creepage and clearance requirements, the diodes are often placed in a serial connection. The following table shows a selection of often used diodes for DESAT operation.

Table 3 Discrete DESAT diodes

Part No.	Vendor	V_R	I_F	t_{rr}	C_J @ 1 V	V_f	Comment
STTH1L06	ST	600 V	1 A	60 ns	22 pF	1.3 V	–
STTH1R06	ST	600 V	1 A	25 ns	20 pF	1.7 V	–
STTH112	ST	1200 V	1 A	75 ns	–	1.9 V	good HV diode
DA2JF8100L	Panasonic	800 V	0.2 A	45 ns	0.4 pF	2.5 V	high dV/dt capable
RS07K	Vishay	800 V	1 A	300 ns	6 pF	1.3 V	–
US1M	Vishay	1000 V	1 A	75 ns	22 pF	1.7 V	good HV diode

5.1.4 MOSFET for *CLAMP* pre-driver output

A gate driver IC configured with a *CLAMP* pre-driver output require a suitable n-channel MOSFET to keep the IGBT gate low during a switched off gate driver output.

For low overall supply voltages, e.g.

- unipolar +15 V or
- bipolar +15 V / -5 V,

the 30 V MOSFET BSL306N is a good choice.

For higher overall supply voltages, e.g.

- bipolar +15 V / -8 V,
- bipolar +15 V / -15 V, or higher,

the 60 V MOSFET BSR606N for currents up 9.1 A or BSL606SN for currents up to 18.1 A are preferred. These MOSFETS allow higher margins especially at abnormal operating conditions.

Table 4 Discrete MOSFET devices

Part No.	Vendor	$V_{DS,max}$	$I_{D,peak}$	$Q_{G,total}$	Comment
BSD316SN	Infineon	30 V	5.6 A	0.6 nC	smallest part
BSL306N	Infineon	30 V	9.0 A	1.5 nC	strongest part
BSR606N	Infineon	60 V	9.1 A	3.7 nC	standard
BSL606SN	Infineon	60 V	18.1 A	4.1 nC	strongest part

5.1.5 Booster selection using discrete bipolar device

The gate driver IC with lower output current rating are designed to support bipolar transistors to boost the output current of a driving solution. The bipolar devices are used in emitter follower configuration. Various devices from different vendors could be used. The following tables shows a brief selection of typical parts used as booster:

Table 5 Discrete bipolar devices

Part No.	Vendor	Polarity	$I_{CE,typ.Peak}$	Comment
ZXTP2012Z	Zetex	PNP	10 A	Industry standard
ZXTN2010Z	Zetex	NPN	10 A	Industry standard
PBSS304NX	NXP	NPN	10 A	–
PBSS304PX	NXP	PNP	10 A	–
2SA2016	ON	PNP	10 A	–
2SC5569	ON	NPN	10 A	–
ECH8502	ON	NPN/PNP	10 A	complementary BJT

5.2 Power dissipation estimation

Apart from the power losses in the gate resistor during switching of any power switch, there is also considerable power loss inside the driver IC.

Every package can achieve a maximum power dissipation at a certain operating condition without exceeding the maximum junction temperature. The internal power loss of the output section (P_{OUT}) of the gate driver IC can be estimated as follows:

$$P_{\mathrm{OUT}} = P_Q + P_{\mathrm{source}} + P_{\mathrm{sink}}$$

Equation 5

P_Q is the operating power loss of the driver output stage. It is easily calculated by the operating supply current (I_{Q2}) and the supply voltage V_{CC2}between *VCC2* and *VEE2* pins:

$$P_Q = I_{\mathrm{Q2}} \cdot V_{\mathrm{CC2}}$$

Equation 6

The turn-on (P_{source}) and turn-off (P_{sink}) losses can be estimated using the resistive voltage divider between inner gate driver resistance (R_{DS}) and outer gate resistor (R_G) with the total gate charge (Q_G) and switching frequency (f_{sw}):

$$P_{\mathrm{source}} = \frac{1}{2} Q_G \cdot f_{\mathrm{sw}} \cdot V_{\mathrm{CC2}} \cdot \frac{R_{\mathrm{DS,source}}}{R_{\mathrm{DS,source}} + R_{\mathrm{G,ON}}}$$

$$P_{\mathrm{sink}} = \frac{1}{2} Q_G \cdot f_{\mathrm{sw}} \cdot V_{\mathrm{CC2}} \cdot \frac{R_{\mathrm{DS,sink}}}{R_{\mathrm{DS,sink}} + R_{\mathrm{G,OFF}}}$$

Equation 7

Table 6 Gate driver output resistance

The lower case letter c in the product name is a placeholder for either U or C of the original product name.

- U: UL 1577 certified product
- C: VDE 0884-11 and UL 1577 certified product

The maximum values refer to the saturated MOSFET resistance as it might appear at the initial turn-on or turn-off.

Driver type	$R_{DS,source}$ output resistance		$R_{DS,sink}$ output resistance	
	typ [Ω]	max [Ω]	typ [Ω]	max [Ω]
1ED3431Mc12M, 1ED3830Mc12M	1.12	4.0	0.82	6.0
1ED3461Mc12M, 1ED3860Mc12M	0.56	2.0	0.41	3.0
1ED3491Mc12M, 1ED3890Mc12M	0.38	1.4	0.28	2.0

Revision history

Document version	Date of release	Description of changes
1.00	2020-07-07	• Initial version
1.10	2021-02-15	• Added links to reinforced certified driver IC variants
1.20	2026-04-10	• Product page links update

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Edition 2026-04-10

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about any aspect of this document?

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Document reference
IFX-oix1578558291492

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