# CIPOS™ Nano IPM Application Note

## For IM111-X6Q1B and IM111-X3Q1B

## About this document

### Scope and purpose

This application note describes the IM111 portfolio of CIPOS™ Nano Intelligent Power Modules (IPM) and should be used in parallel with each part's data sheet. This document first gives an overview of the product lineups and data sheet information. It details the functionality of the modules and then provides recommendations for designing the external circuitry that interfaces with the modules. The application note ends with thermal-design considerations.

### Intended Audience

Power electronics engineers who want to design reliable and efficient motor drive applications with IM111.

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# 1 Introduction

With the global emphasis on energy efficiency, there is an ever stricter requirement on the efficiency of motor drive systems. CIPOS™ IPMs are becoming more popular in home appliance and industrial motor drive applications, because they enable increased system efficiencies, smaller designs, easier assembly methods and shorter system development cycles.

Our next generation of CIPOS™ Nano IPM has been developed with a focus on providing added features, higher module efficiency and better long-term reliability. Integrating Infineon's low $R_{DS(ON)}$ CoolMOS ™ and OptiMOS ™ technology and latest gate driver technologies in one package allows for the shrinking of the package size, and hence increased power densities.

The IM111 H-bridge IPMs are designed for high-efficiency appliance motor drives such as linear refrigerator compressor, high-efficiency single-phase motor drives, and DC-AC inverters rated between 80 and 200 W. These advanced IPMs, available in the same QFN 12x10 mm package, have several protection features including precise overcurrent protection and a UL-certified temperature sensor.

The application note concerns the following products:

IM111-X6Q1B

IM111-X3Q1B

## 1.1 Product portfolio

**Table 1 IM111 Product line**

| Part number | Rating | | Topology | Package | Isolation Voltage ($V_{rms}$) |
|---|---|---|---|---|---|
| | $R_{dson}$ (Ω) | Voltage (V) | | | |
| IM111-X6Q1B | 0.28 | 600 | H-bridge with open sources | QFN 12x10 mm | 1500 Vrms sinusoidal, 1 min. |
| IM111-X3Q1B | 0.063 | 250 | | | |

## 1.2 Nomenclature

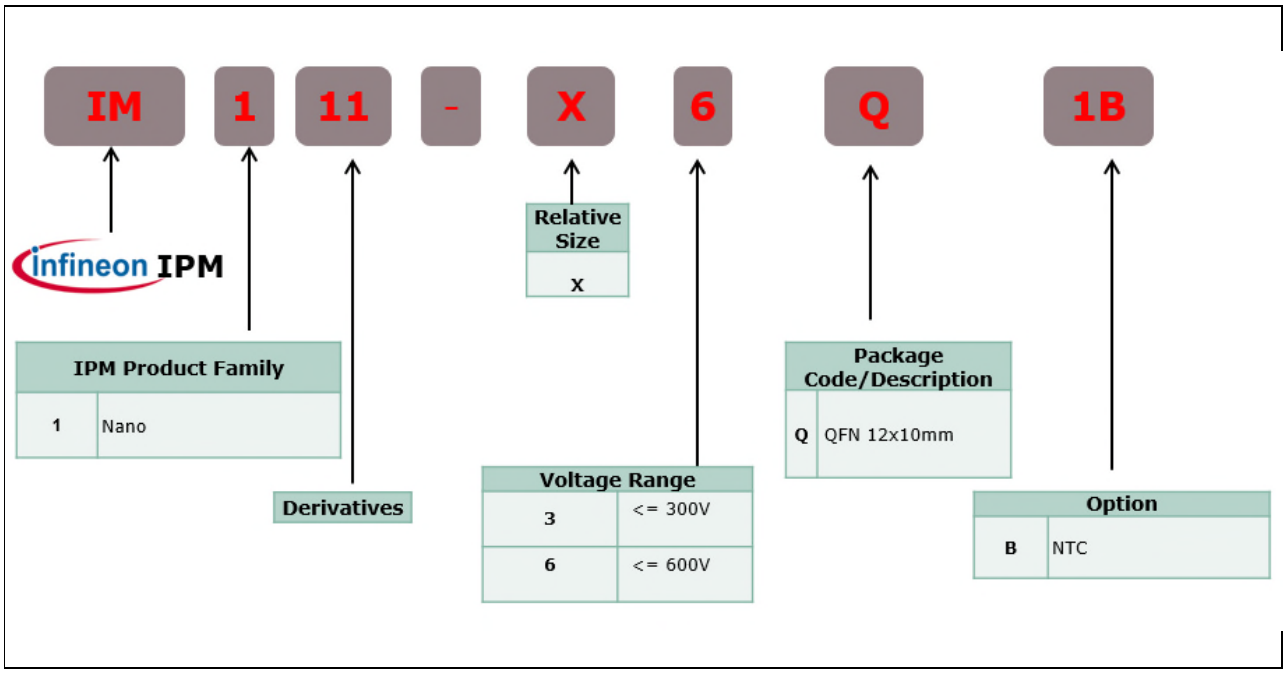



**Figure 1** Nomenclature for CIPOS™ Nano IPM's IM111 series

# 2 Product overview and pin description

## 2.1 Internal circuit and features

Figure 2 illustrates the internal block diagram of the IM111. These products consist of an H-bridge MOSFET inverter circuit and two half-bridge driver ICs with protection features.

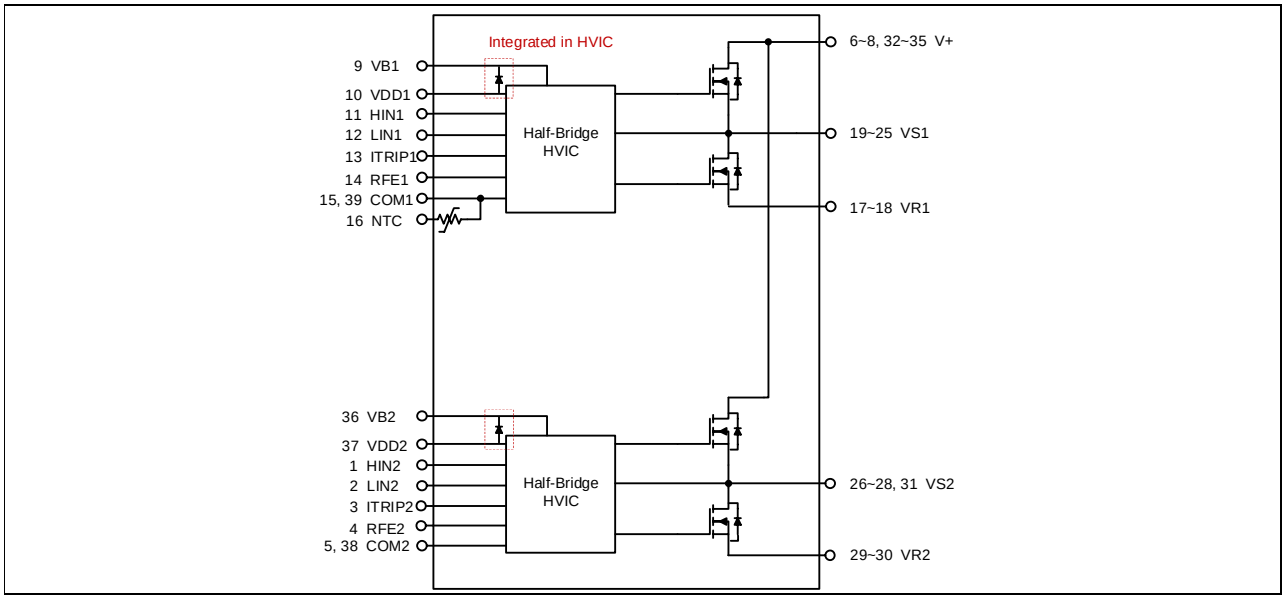



**Figure 2** Internal block diagram

The detailed features and integrated functions of IM111 are described as follows:

Key features:

- 600 V/0.28 Ω to 250 V/0.063 Ω rating in one physical package size (mechanical layouts are identical)
- Motor power range from 80 W to 200 W
- Infineon $R_{DS(ON)}$ CoolMOS ™ (600V) and OptiMOS ™ (250V) technology
- Undervoltage lockout for all channels
- Rugged gate driver technology with stability against transient and negative voltage
- Integrated bootstrap functionality
- Matched delay times of all channels / Built in dead time
- Overcurrent protection
- Lead-free terminal plating; RoHS-compliant
- 3.3 V Schmitt-triggered input logic
- Cross-conduction preventing logic
- Low-side source pins accessible for current monitoring
- Active high input signal logic
- Isolation 1500 Vrms min
- High operating case temperature, $T_{cmax}$ = 125 °C
- UL-certified temperature monitor
-
-

Product **overview and pin description**

Key benefits:

- Ease of design and short time-to-market
- Compact package with minimized PCB space requirement
- Simplified design and manufacturing
- Lower EMI emissions due to very tuned dv/dt
- Heat sink-less operation

## 2.2 Input and output pins

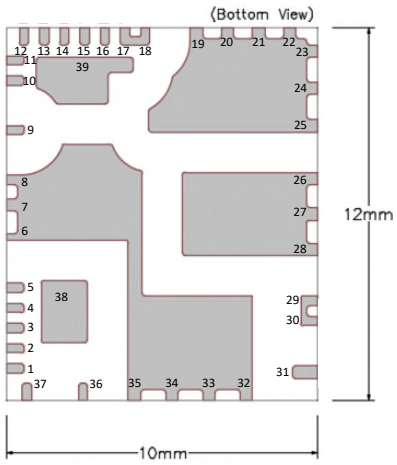



**Figure 3** Module pinout

**Table 2 Pin Assignment**

| Pin | Name | Description |
|---|---|---|
| 1 | $HIN_2$ | Logic Input for High Side Gate Driver (Active High) |
| 2 | $LIN_2$ | Logic Input for Low Side Gate Driver (Active High) |
| 3 | $I_{TRIP2}$ | Over Current Protection |
| 4 | $RFE_2$ | Fault Clear, Fault Reporting & Enable |
| 5 | $COM_2$ | Logic Ground |
| 6-8 | V+ | DC Bus Voltage Positive |
| 9 | $V_{B1}$ | High Side Floating Supply (Bootstrap Cap Connection +) |
| 10 | $V_{DD1}$ | Low Side Control Supply |
| 11 | $HIN_1$ | Logic Input for High Side Gate Driver (Active High) |
| 12 | $LIN_1$ | Logic Input for Low Side Gate Driver (Active High) |
| 13 | $I_{TRIP1}$ | Over Current Protection |
| 14 | $RFE_1$ | Fault Clear, Fault Reporting & Enable |
| 15 | $COM_1$ | Logic Ground |
| 16 | NTC | Negative Temperature Coeffient Thermistor |
| 17-18 | $V_{R1}$ | Low Side Source |
| 19-25 | $V_{S1}$ | Phase Output |
| 26-28 | $V_{S2}$ | Phase Output |

Product **overview and pin description**

| Pin | Name | Description |
|---|---|---|
| 29-30 | $V_{R2}$ | Low Side Source |
| 31 | $V_{S2}$ | Phase Output (Bootstrap Cap Connection -) |
| 32-35 | V+ | DC Bus Voltage Positive |
| 36 | $V_{B2}$ | High Side Floating Supply (Bootstrap Cap Connection +) |
| 37 | $V_{DD2}$ | Low Side Control Supply |
| 38 | $COM_2$ | Logic Ground |
| 39 | $COM_1$ | Logic Ground |

## 2.3 Pin descriptions

### HIN(1,2) and LIN(1,2) (Low-side and high-side control pins)

These pins are positive logic and they are responsible for the control of the integrated MOSFETs. The internal structure of these pins is depicted in Figure 5. The Schmitt-trigger input thresholds are designed to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. A pull-down resistor of about 800 kΩ is internally provided to pre-bias inputs during supply start-up, and an ESD diode is provided for pin protection purposes. The input Schmitt trigger and a noise filter provide beneficial noise rejection to short input pulses. See Section 3.5 for more details about the advanced input filter.

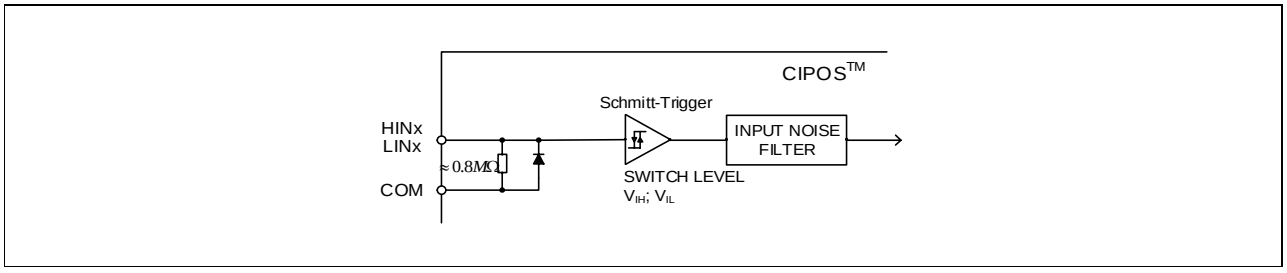



**Figure 4** Input pin structure

The integrated gate drive also provides a shoot-through inhibiting capability, which prevents the simultaneous on-state of the high-side and low-side switch of the same inverter phase. A dead time of 300 ns (typical) is also inserted between the corresponding HIN and LIN signals by the gate driver IC in order to reduce cross-conduction of the MOSFETs.

### $V_{DD}$, COM (Low-side control supply and reference)

$V_{DD}$ is the control supply, which provides power both to input logic and to output power stage. Input logic is referenced to COM ground.

The undervoltage circuit enables the device to operate at power on when a supply voltage of at least a typical voltage of $V_{DDUV+}$ = 8.9 V is present.

The IC shuts down all the gate drivers' power outputs, when the $V_{DD}$ supply voltage is below $V_{DDUV-}$ = 7.7 V. This prevents the external power switches from critically low gate voltage levels during the on state, and therefore from excessive power dissipation.

### $V_{B(1,2)}$ and $V_{S(1,2)}$ (High-side supplies)

$V_B$ to $V_S$ is the high-side supply voltage. The high-side circuit can float with respect to COM following the external high-side power device source voltage.

Due to the low power consumption, the floating driver stage is supplied by an integrated bootstrap circuit.

The undervoltage detection operates with a rising supply threshold of typically $V_{BSUV+}$ = 8.9 V and a falling threshold of $V_{BSUV-}$ = 7.7 V.

$V_{S(1,2)}$ provide a high robustness against negative voltage in respect of COM. This ensures very stable designs even under rough conditions.

### $V_{R(1,2)}$ (Low-side sources)

The low-side sources are available for current measurements of each phase leg. It is recommended to keep the connection to the COM pin as short as possible in order to avoid unnecessary inductive voltage drops.

### NTC (Thermistor output)

A UL-certified NTC is integrated in the module with one terminal of the chip connected to COM and the other to NTC pin. When pulled up to a rail voltage such as $V_{DD}$ or 3.3 V by a resistor, the NTC pin provides an analog voltage signal corresponding to the temperature of the thermistor.

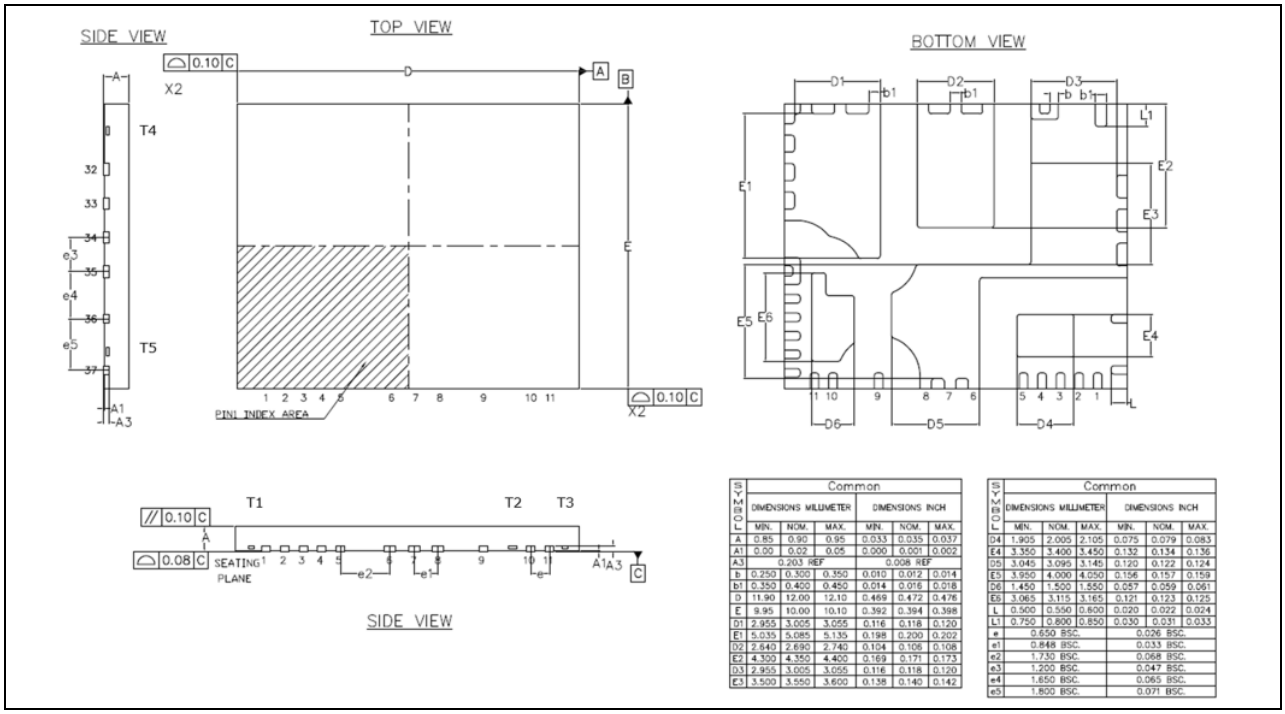
### RFE (Fault clear / Fault reporting / Enable)

The RFE pin combines three functions in one pin: RCIN or RC-network-based programmable fault clear timer, fault output and enable input. This pin has negative logic and an open-drain output. See Section 3.2 for more details.

### V+ (Positive bus input voltage)

The high-side MOSFETs are connected to the bus voltage. Note that the bus voltage does not exceed 450 V for X6 and 200 V for X3.

## 2.4 Outline drawings




| SYMBOL | Common DIMENSIONS MILLIMETER MIN. | NOM. | MAX. | DIMENSIONS INCH MIN. | NOM. | MAX. |
|---|---|---|---|---|---|---|
| A | 0.85 | 0.90 | 0.95 | 0.033 | 0.035 | 0.037 |
| A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| A3 | | 0.203 REF | | | 0.008 REF | |
| b | 0.250 | 0.300 | 0.350 | 0.010 | 0.012 | 0.014 |
| b1 | 0.350 | 0.400 | 0.450 | 0.014 | 0.016 | 0.018 |
| D | 11.90 | 12.00 | 12.10 | 0.469 | 0.472 | 0.476 |
| E | 9.95 | 10.00 | 10.10 | 0.392 | 0.394 | 0.398 |
| D1 | 2.955 | 3.005 | 3.055 | 0.116 | 0.118 | 0.120 |
| E1 | 5.035 | 5.085 | 5.135 | 0.198 | 0.200 | 0.202 |
| D2 | 2.640 | 2.690 | 2.740 | 0.104 | 0.106 | 0.108 |
| E2 | 4.300 | 4.350 | 4.400 | 0.169 | 0.171 | 0.173 |
| D3 | 2.955 | 3.005 | 3.055 | 0.116 | 0.118 | 0.120 |
| E3 | 3.500 | 3.550 | 3.600 | 0.138 | 0.140 | 0.142 |

| SYMBOL | Common DIMENSIONS MILLIMETER MIN. | NOM. | MAX. | DIMENSIONS INCH MIN. | NOM. | MAX. |
|---|---|---|---|---|---|---|
| D4 | 1.905 | 2.005 | 2.105 | 0.075 | 0.079 | 0.083 |
| E4 | 3.350 | 3.400 | 3.450 | 0.132 | 0.134 | 0.136 |
| D5 | 3.045 | 3.095 | 3.145 | 0.120 | 0.122 | 0.124 |
| E5 | 3.950 | 4.000 | 4.050 | 0.156 | 0.157 | 0.159 |
| D6 | 1.450 | 1.500 | 1.550 | 0.057 | 0.059 | 0.061 |
| E6 | 3.065 | 3.115 | 3.165 | 0.121 | 0.123 | 0.125 |
| L | 0.500 | 0.550 | 0.600 | 0.020 | 0.022 | 0.024 |
| L1 | 0.750 | 0.800 | 0.850 | 0.030 | 0.031 | 0.033 |
| e | | 0.650 BSC. | | | 0.026 BSC. | |
| e1 | | 0.848 BSC. | | | 0.033 BSC. | |
| e2 | | 1.730 BSC. | | | 0.068 BSC. | |
| e3 | | 1.200 BSC. | | | 0.047 BSC. | |
| e4 | | 1.650 BSC. | | | 0.065 BSC. | |
| e5 | | 1.800 BSC. | | | 0.071 BSC. | |

**Figure 5** QFN 12x10mm (dimensions in mm)

## 2.5 Maximum electrical rating

Absolute maximum ratings indicate sustained limits beyond which damage to the module may occur. These are not tested in production. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the tables. These values can be viewed in the specific part's data sheet. Appropriate design margins should be implemented to ensure that all absolute maximum ratings are observed at all times during operation. This includes abnormal conditions like start-up, shut-down, overload, short-circuit, and system failures. Section 6 provides detailed instructions to help assess the temperatures of the device based on operating conditions. Please see references below for more in-depth descriptions of these ratings.

**Table 3 Module**

| Parameter | Symbol | Description |
|---|---|---|
| Storage temperature | $T_{STG}$ | Storage temperature range for reliable performance over life of device |
| Operating case temperature | $T_C$ | Temperature range of package top surface (surface with part marking) |
| Operating junction temperature | $T_J$ | Temperature range of the internal junction of power switches and gate drivers. |
| Isolation test voltage | $V_{ISO}$ | 60 Hz voltage that can be applied for one minute between all pins and top surface of the module. |

**Table 4 Inverter**

| Parameter | Symbol | Description |
|---|---|---|
| Max. blocking voltage | $V_{DSS}/V_{RRM}$ | Voltage that can be applied across each MOSFET. |
| Output current | $I_O$ | Current class to aid in selection of right part number. It is based on $Rth_{(J-C)B}$. |
| Peak output current | $I_{OP}$ | Pulsed output current capability from single switch at specified temperature and $t_P$ (duration of time at peak). |
| Peak power dissipation per IGBT | P | Peak power dissipation per switch |
| Output current | $I_{OA}$ | Current class to aid in selection of right part number. It is based on $Rth_{(J-A)}$. |

**Table 5 Control**

| Parameter | Symbol | Description |
|---|---|---|
| Low-side control supply voltage | $V_{DD}$ | Voltage range of input supply voltage |
| Input voltage LIN, HIN | $V_{IN}$ | Voltage range in reference to $V_{DD}$ |
| High-side floating supply voltage ($V_B$ reference to $V_S$) | $V_{BS}$ | Voltage range of input supply voltage |

# 3 Protection features

## 3.1 Overcurrent protection

IM111 is equipped with an ITRIP input pin. Together with one or more external shunt resistors, this functionality can be used to detect overcurrent events. The internal high-voltage gate driver will continuously monitor the voltage on the ITRIP pin. Whenever this voltage exceeds the reference voltage ($V_{IT,TH+}$ = 0.5 V with a ±5% variation), a fault signal will be generated on the RFE pin, and all MOSFETs will be turned OFF.

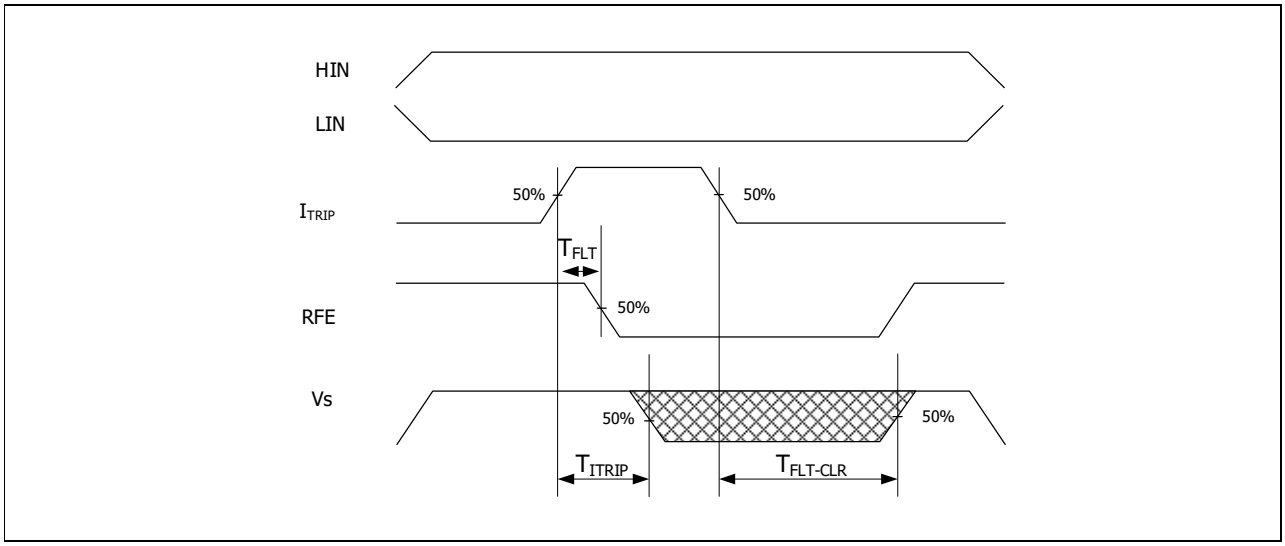



**Figure 6** Timing chart for the overcurrent protection function

The threshold of overcurrent protection can be determined by $V_{IT,TH+}$ / $R_{SHUNT}$, if a single bus shunt is used and is directly connected to the ITRIP pin without any voltage-dividing circuit.

### 3.1.1 Selecting the current-sensing shunt resistor

The value of the current-sensing resistor is calculated by the following expression:

$$R_{SH} = \frac{V_{IT,TH+}}{I_{OC}} \quad (1)$$

Where $V_{IT,TH+}$ is the ITRIP positive-going threshold voltage of IM111, typically 0.50 V. $I_{OC}$ is the trip current level.

$I_{OC}$ should be lower than the pulsed peak drain current in the data sheet. In real applications, it is typically chosen at 2 to 3 times of peak operating current of the system to avoid unnecessary shut-down due to coupled noises.

The following should be considered to determine the power rating of a single shunt resistor:

- Maximum load current of inverter ($I_{rms}$)
- Shunt resistor value at $T_C$=25°C ($R_{SH}$)
- Power derating ratio of shunt resistor at $T_{SH}$=100°C according to the manufacturer's data sheet
- Safety margin

The shunt resistor power rating is calculated by the following equation:

$$P_{SH} = \frac{I_{rms}^2 \times R_{SH} \times margin}{deratingratio} \quad (2)$$

For example, in case of $R_{SH}$=100 mΩ:

- Max. load current of the inverter : 1 $A_{rms}$
- Power derating ratio of shunt resistor at $T_{SH}$=100°C : 80%
- Safety margin : 30%

$P_{SH}$=0.1625 W

A proper power rating of a single shunt resistor should then be over 0.1625 W. A strategy to reduce the power dissipation requirement for one single shunt resistor is to use two or more shunt resistors in parallel.

### 3.1.2 Delay time

When an overcurrent event occurs in the inverter, there is a delay between the occurrence of this event and the IPM turning off all its MOSFETs. This delay arises from circuit-design choices made external to the IPM, and from intrinsic delays within the IPM.

Let us examine the delay due to circuit design choices external to the IPM first. An RC circuit is typically placed between the shunt resistor and the ITRIP pin. This low pass filter is necessary to prevent spurious triggering of the overcurrent protection feature due to noise. Assuming no voltage-dividing circuit is present, when the sensing voltage on the shunt resistor exceeds ITRIP positive-going threshold ($V_{IT,TH+}$), this voltage is filtered by the RC network and then applied to the ITRIP pin with a delay determined by the RC time constant, $t_{RC}$.

Next let us examine the intrinsic delays within the IPM. The IPM has a built-in filter of $t_{FIL,ITRIP}$ =300 ns (typical) to reject pulses on the ITRIP pin that are shorter than $t_{FIL,ITIRP}$. In addition there is the shutdown propagation delay of ITRIP ($t_{ITRIP}$) shown in the data sheet. With no capacitor on RFE, the IPM requires a typical 900s to shut down all the MOSFETs after ITRIP crosses $V_{IT,TH+}$. If a capacitor is placed on RFE, this delay will increase by the time required to discharge the capacitor to a voltage below $V_{RFE-}$. To minimize the overall delay, keep the capacitance connected to RFE low (~1nF), and pull up RFE to 3.3V or 5V rather than $V_{DD}$. Refer to Section 3.2 for more information on RFE.

Therefore, the total time from the ITRIP positive-going threshold ($V_{IT,TH+}$) to shut down all MOSFETs becomes:

$t_{TOTAL} = t_{RC} + t_{ITRIP}$ (with no capacitor on RFE).

## 3.2 RFE functions

The RFE pin is normally connected to an RC network on the PCB as per the schematic in Figure 7. Under normal operating conditions, $R_{RCIN}$ pulls the RFE pin to 3.3 V, thus enabling all the functions in the IPM. The microcontroller can pull this pin low to disable the IPM functionality. This is the Enable function.

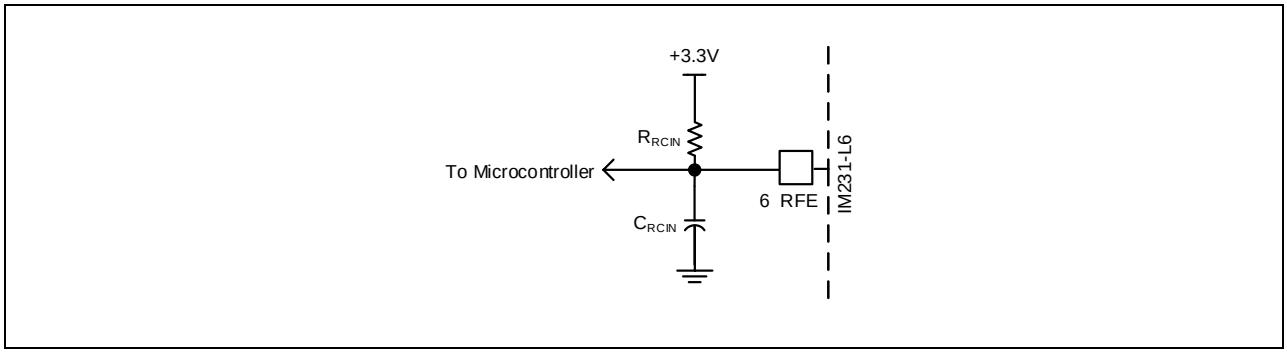



**Figure 7** Typical PCB circuit connected to the RFE pin

The Fault function allows the IPM to report a Fault condition to the microcontroller by pulling the RFE pin low in one of two situations. The first is an undervoltage condition on $V_{DD,}$ and the second is when the ITRIP pin detects a voltage rise above $V_{IT,TH+}$.

The programmable fault-clear timer function provides a means of automatically re-enabling the module operation to a preset amount of time ($t_{FLT-CLR}$) after the fault condition has disappeared. Figure 8 shows the RFE-related circuit block diagram inside the IPM.

The length of $T_{FLT-CLR}$ can be determined by using the formula below.

$V_{RFE}(t) = 3.3\ V * (1 - e^{-t/RC})$

$t_{FLT-CLR} = -R_{RCIN} * C_{RCIN} * \ln(1-V_{IN,TH+}/3.3\ V)$

For example, if $R_{RCIN}$ is 1.2 MΩ and $C_{RCIN}$ is 1 nF, the $t_{FLT-CLR}$ is about 1.7 ms with $V_{IN,TH+}$ of 2.5 V. It is also important to note that $C_{RCIN}$ needs to be minimized in order to make sure it is fully discharged in case of an overcurrent event.

Since the ITRIP pin has a 300 ns input filter, it is appropriate to ensure that $C_{RCIN}$ will be discharged below $V_{IN,TH-}$ by the open-drain MOSFET, after 200 ns. Therefore, the max $C_{RCIN}$ can be calculated as follows:

$V_{RFE}(t) = 3.3\ V * e^{-t/RC} < V_{IN,TH-}$

$C_{RCIN} < 300\ ns / ( - \ln (V_{IN,TH-} / 3.3\ V) * R_{RFE_ON})$

Considering a $V_{IN,TH-}$ of 0.8 V and $R_{RFE_ON}$ of 50 Ω, $C_{RCIN}$ should be less than 4 nF. It is also suggested to use a $R_{RCIN}$ of between 0.5 MΩ and 2 MΩ.

Finally, to minimize the delay in the overcurrent protection circuit, we recommend pulling up RFE with $R_{RCIN}$ to 3.3 V or 5 V instead of $V_{DD}$.

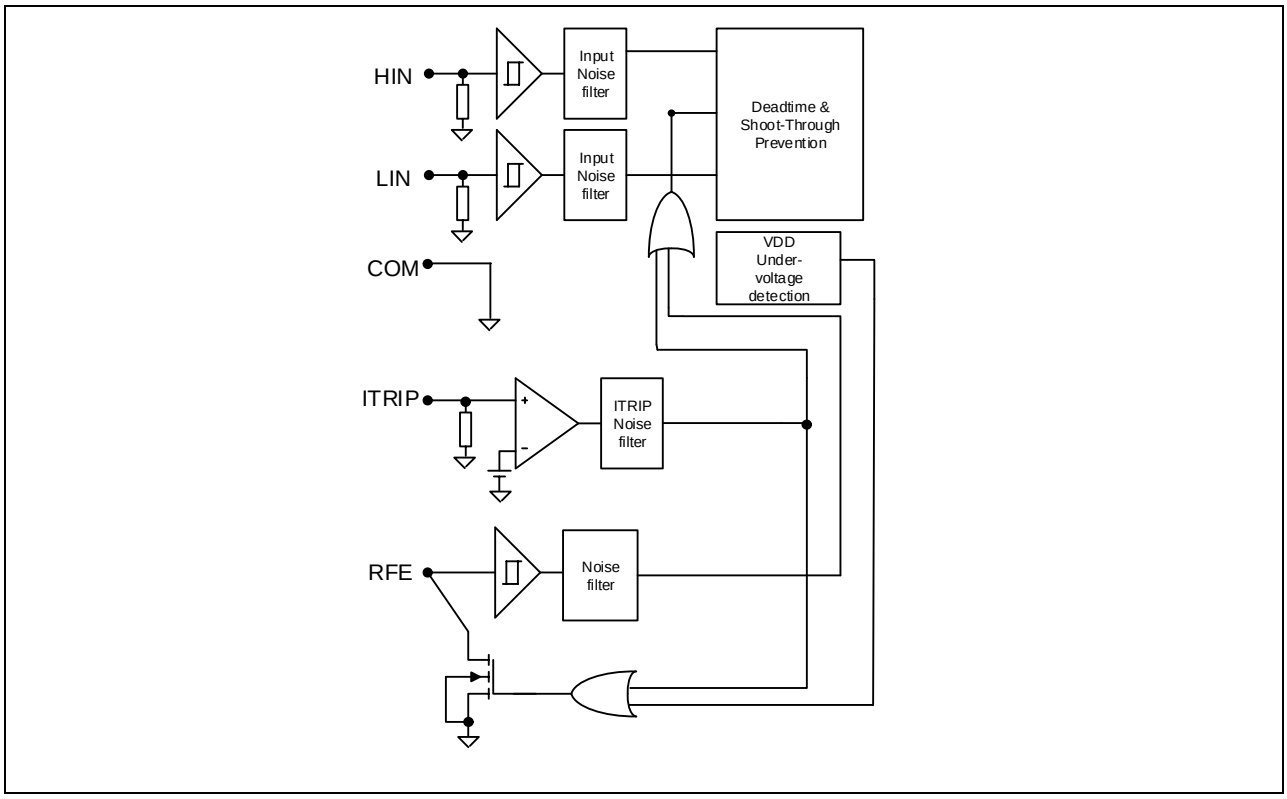



**Figure 8** RFE internal circuit structure

## 3.3 Undervoltage lockout

The gate drivers inside IM111 provide undervoltage lockout (UVLO) on both the $V_{DD(1-2)}$ (logic and low-side circuitry) power supplies, and also $V_{BS(1-2)}$ (high-side circuitry power supplies). UVLO's threshold, labeled as $V_{DDUV+/-}$ (or $V_{BSUV+/-}$) in Figure 9 below, is the voltage level of $V_{DD(1-2)}$ or $V_{BS(1-2)}$ where UVLO is enabled or disabled depending on whether the power supply voltage is rising or falling.

Upon power-up, should the $V_{DD(1-2)}$ voltage fail to reach the $V_{DDUV+}$ threshold, the driver will not turn ON. Additionally during operation, if the $V_{DD(1-2)}$ voltage decreases below the $V_{DDUV-}$ threshold during operation, the UVLO circuitry will recognize a fault condition and shut down the high and low-side gate drive outputs.

Upon power-up, should the $V_{BS(1-2)}$ voltage fail to reach the $V_{BSUV+}$ threshold, the driver will not turn ON. Additionally during operation, if the $V_{BS(1-2)}$ voltage decreases below the $V_{BSUV-}$ threshold, the UVLO circuitry will recognize a fault condition, and shut down the high-side gate outputs of the driver.

UVLO ensures that the drivers will turn on the corresponding MOSFETs only when the gate supply voltage is sufficient enough to fully enhance the MOSFETs. Without this feature, the gates of the MOSFET could be driven with a low voltage causing the MOSFETs to conduct current with a high saturation voltage. This could result in very high conduction losses within the power device, and could lead to IPM failure.

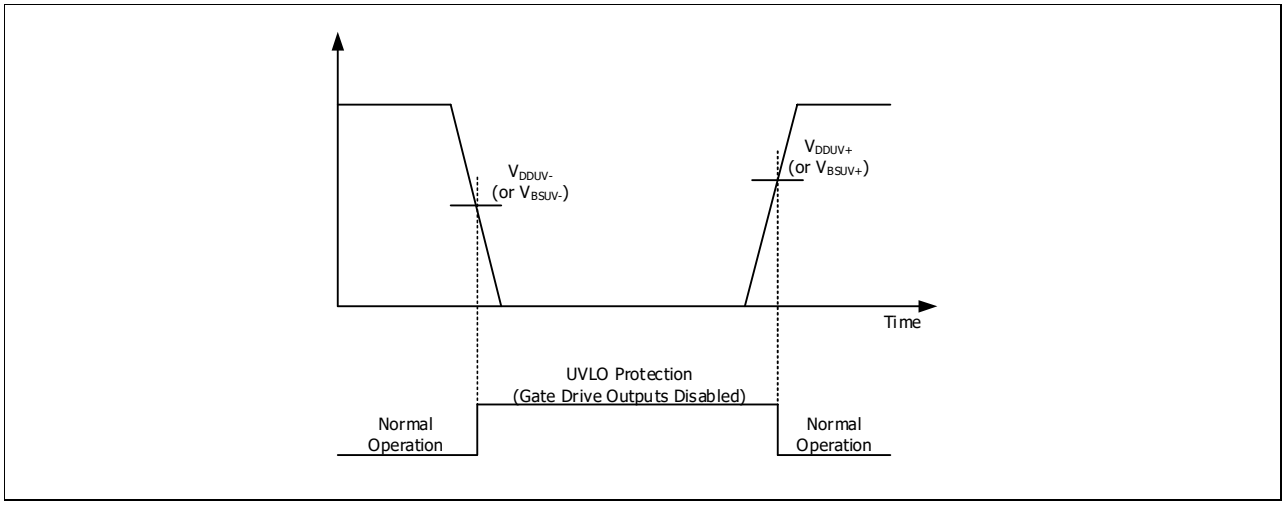



**Figure 9** UVLO protection

Table 6 describes the functionality of the IPM over a range of control power supply voltages. We recommend connecting a low-impedance (low ESR, low ESL) electrolytic capacitor and high-frequency decoupling capacitors as close to the $V_{DD}$ pins of the IPM as possible. Maximum ripple of the supply should not exceed ± 1 V/µs to prevent the internal drivers from malfunctioning.

The potential at the module's COM terminal is different from that at the $V_{R(1-2)}$ power terminals by the voltage drop across the shunt resistor(s). All control circuits and power supplies should refer to COM and not to the $V_{R(1-2)}$ nodes.

**Table 6 CIPOS™ IPM versus control power supply voltage**

| Control voltage [V] | Functionality |
|---|---|
| 0-2.5 V | IPM gate drivers are not functional, supply is not sufficient to have working active devices. |
| 2.5-8.9 V (positive going)<br>2.5-7.7 V(negative going) | Gate driver logic circuits are working, the gate drivers are in UVLO, MOSFETs are kept off. |
| 11.2-13.5 V | Conduction and switching losses will be higher than under normal conditions. High-side transistors may not operate after $V_{B(1-2)}$ initial charging, as the $V_{B(1-2)}$ voltage level may not reach $V_{BSUV+}$. |
| 13.5-16.5 V for $V_{DD(1-2)}$<br>12.5-17.5 V for $V_{B(1-2)}$ | Normal operation. |
| 16.5-20 V for $V_{DD(1-2)}$<br>17.5~20 V for $V_{B(1-2)}$ | Because the control supply voltage is above the recommended range, the transistor's switching will be faster, which will cause an increase in system noise. Peak short-circuit current might be too large for proper operation of short-circuit protection. |
| Over 20 V | Damage of module may occur. |

## 3.4 Over-temperature protection

All IM111 IPMs have an internal negative-temperature coefficient (NTC) thermistor to sense the module temperature. The NTC thermistor is integrated in the module with one terminal of the chip connected to COM,

and the other to the NTC, which can be used to monitor the temperature of the IPM. The resistance of the NTC can be calculated at any temperature as follows:

$$R_{TH} = R_{25} \cdot e^{\left[B\left(\frac{1}{T_{TH}} - \frac{1}{T_{25}}\right)\right]}$$

B (B-constant), $R_{25}$ (resistance at 25°C), and $R_{125}$ (resistance at 125°C) are given in the specific data sheet where an NTC is implemented. Characterization of the thermistor's resistance depending on temperature is shown in Table 7 below.

**Table 7 Raw data of the thermistor used in IM111**

| T [°C] | $R_{min}$ [kΩ] | $R_{typ}$ [kΩ] | $R_{max}$ [kΩ] | Tol [%] | T [°C] | $R_{min}$ [kΩ] | $R_{typ}$ [kΩ] | $R_{max}$ [kΩ] | Tol [%] |
|---|---|---|---|---|---|---|---|---|---|
| -40 | 1438.40 | 1568.15 | 1705.34 | 8.7% | 45 | 18.930 | 20.097 | 21.282 | 5.9% |
| -35 | 1040.65 | 1130.82 | 1225.73 | 8.4% | 50 | 15.448 | 16.432 | 17.436 | 6.1% |
| -30 | 761.64 | 825.03 | 891.47 | 8.1% | 55 | 12.695 | 13.531 | 14.385 | 6.3% |
| -25 | 563.53 | 608.58 | 655.58 | 7.7% | 60 | 10.4830 | 11.1942 | 11.9238 | 6.5% |
| -20 | 421.23 | 453.57 | 487.16 | 7.4% | 65 | 8.6961 | 9.3033 | 9.9279 | 6.7% |
| -15 | 317.53 | 340.93 | 365.14 | 7.1% | 70 | 7.2454 | 7.7652 | 8.3016 | 6.9% |
| -10 | 241.62 | 258.72 | 276.33 | 6.8% | 75 | 6.0619 | 6.5084 | 6.9703 | 7.1% |
| -5 | 185.51 | 198.10 | 211.02 | 6.5% | 80 | 5.0922 | 5.4767 | 5.8755 | 7.3% |
| 0 | 143.62 | 152.98 | 162.53 | 6.2% | 85 | 4.3017 | 4.6342 | 4.9800 | 7.5% |
| 5 | 112.35 | 119.37 | 126.51 | 6.0% | 90 | 3.6482 | 3.9366 | 4.2372 | 7.6% |
| 10 | 88.440 | 93.740 | 99.109 | 5.7% | 95 | 3.1056 | 3.3565 | 3.6186 | 7.8% |
| 15 | 70.033 | 74.055 | 78.112 | 5.5% | 100 | 2.6533 | 2.8721 | 3.1012 | 8.0% |
| 20 | 55.770 | 58.837 | 61.918 | 5.2% | 105 | 2.2748 | 2.4661 | 2.6669 | 8.1% |
| 25 | 44.650 | 47.000 | 49.350 | 5.0% | 110 | 1.9567 | 2.1245 | 2.3009 | 8.3% |
| 30 | 35.772 | 37.737 | 39.711 | 5.2% | 115 | 1.6886 | 1.8360 | 1.9913 | 8.5% |
| 35 | 28.801 | 30.449 | 32.110 | 5.5% | 120 | 1.4616 | 1.5915 | 1.7287 | 8.6% |
| 40 | 23.298 | 24.682 | 26.084 | 5.7% | 125 | 1.2690 | 1.3837 | 1.5050 | 8.8% |

An external resistor network should be connected to the NTC to provide temperature readings. When pulled up to a rail voltage such as $V_{DD}$ or 3.3 V by a resistor, the NTC pin provides an analog voltage signal corresponding to the temperature of the thermistor. This circuit can be connected to the ADC terminal of the microcontroller to shut down the module if the temperature reading is too high. An example of this circuit is shown below in Figure 10.

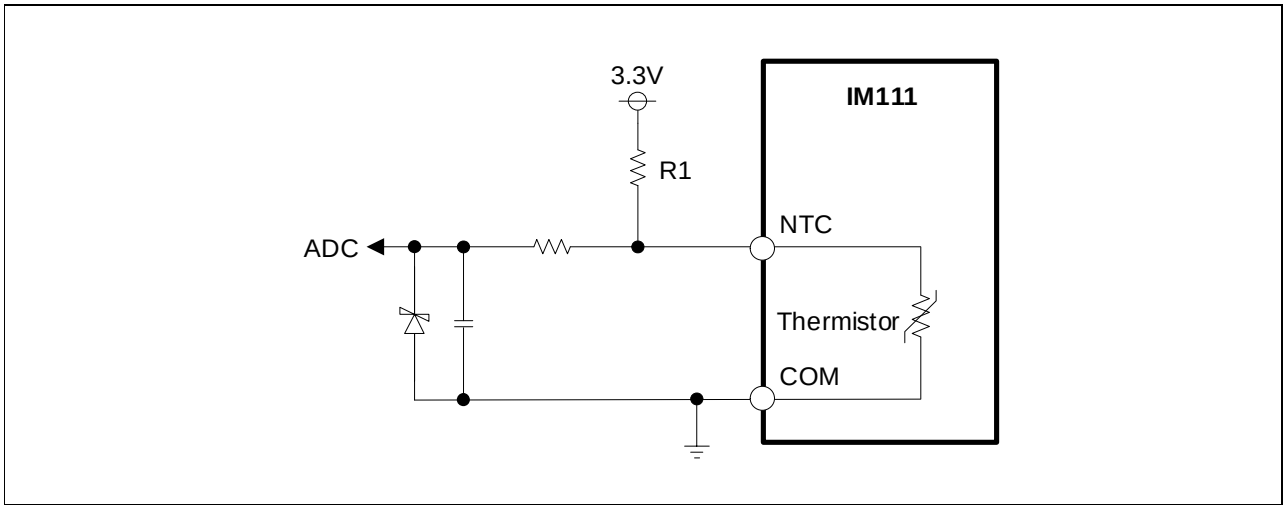



**Figure 10** Example of over-temperature protection circuit

Please note that it remains the responsibility of the system designer to implement protection strategies against overheating that are appropriate for the system operating conditions. While the NTC provides temperature-reading outputs, it is remote from the power switches, which are the major heat source inside the IPM. Because of this, the NTC does not necessarily reflect the temperature of all internal components, as there will always be a timing and temperature difference. The actual NTC reading is affected by the thermal system design specified by the system designer, so some calibration of readings and actual temperature may be required depending on the application.

## 3.5 Advanced input filter

IM111 includes an advanced noise filter providing beneficial noise rejection to short input pulses applied to LIN and HIN. The noise filter suppresses control pulses which are below the filter time $T_{FILIN}$. The filter acts according to Figure 11.

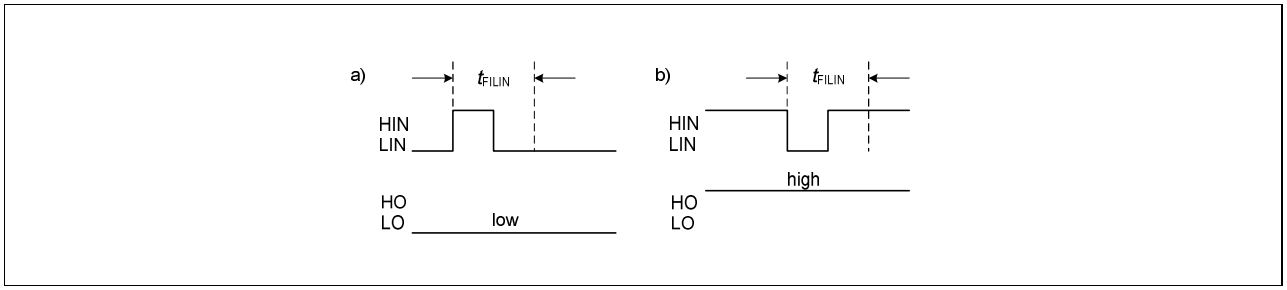



**Figure 11** Input filter timing diagram

Compared to noise filters in competitor products, the advanced input filter also allows for an improvement in the input/output pulse symmetry of the gate driver. The working principle of the filter as compared with the standard competitor input filter is shown in Figure 12.

The figure shows the advanced input filter of the gate driver in IM111, and the symmetry between the input and output. The upper pair of waveforms (Example 1) show an input signal with a duration much longer then $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal. The lower pair of waveforms

(Example 2) show an input signal with a duration slightly longer then $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal.

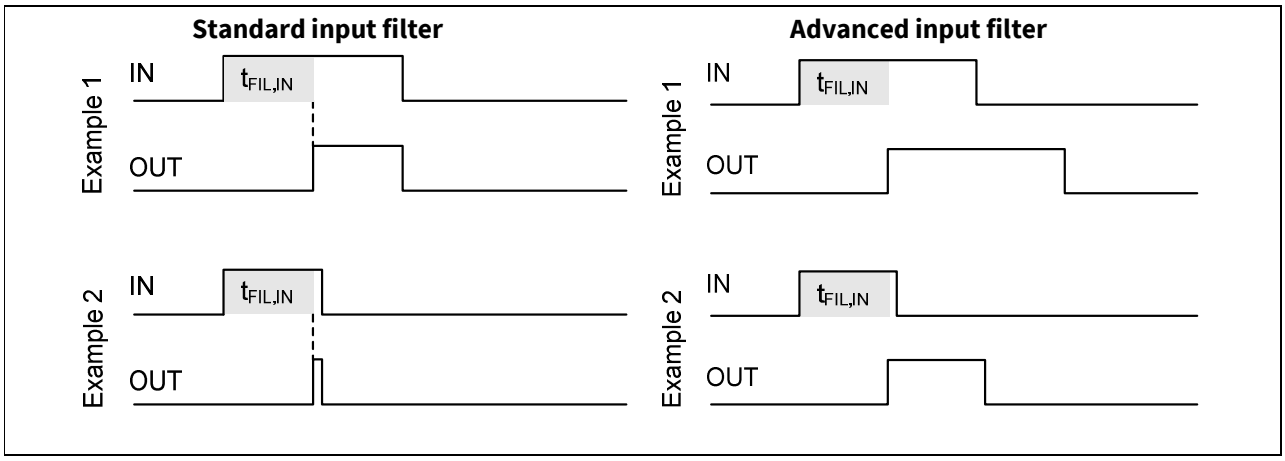



**Figure 12** Standard input filter found in competitor products (left) and the advanced input filter in IM111 (right)

# 4 Interface circuits and layout guide

## 4.1 Input/output signal connection

The following shows the I/O interface circuit between microcontroller and IM111. The IPM input logic is active-high with weak 800 kΩ internal pull-down resistors. It is recommended to use external pull-down resistors on each PWM input pin in the range of 10 kΩ to 100 kΩ. The RFE output is configured as an open-drain MOSFET. This signal should thus be pulled up to 5 V or 3.3 V external logic power supply with a resistor. The resistor should be carefully chosen as per Section 3.2.

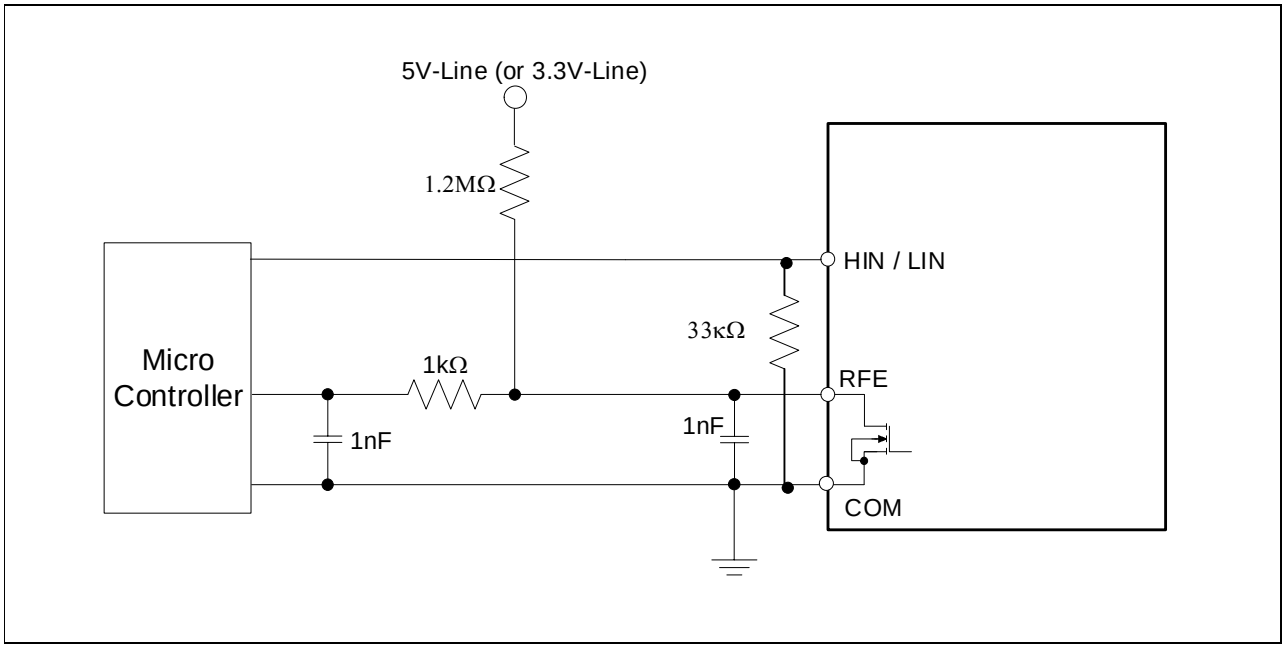



**Figure 13** Recommended microcontroller I/O interface circuit

**Table 8 Maximum rating of input and RFE pin**

| Item | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Module supply voltage | $V_{DD}$ | Applied between $V_{DD}$ – COM | -0.3 ~ 20 | V |
| Input voltage | $V_{IN}$ | Applied between HIN(1,2)– COM, LIN(1,2) – COM, ITRIP to COM | -0.3 ~ 20 | V |
| Fault output supply voltage | RFE | Applied between RFE – COM | -0.3 ~ 20 | V |

The input and fault output maximum rating voltages are listed in Table 8. The fault output is open-drain configured and is rated up to 20 V. However, it is recommended that the fault output be pulled up to 5 V or 3.3 V logic supply used for the inputs. We recommend connecting bypass capacitors as close as possible to the RFE pin to avoid any noise that might turn on the open-drain MOSFET.

## 4.2 General interface circuit example

Figure 14 shows a typical application circuit interface schematic with control signals connected directly to the microcontroller.

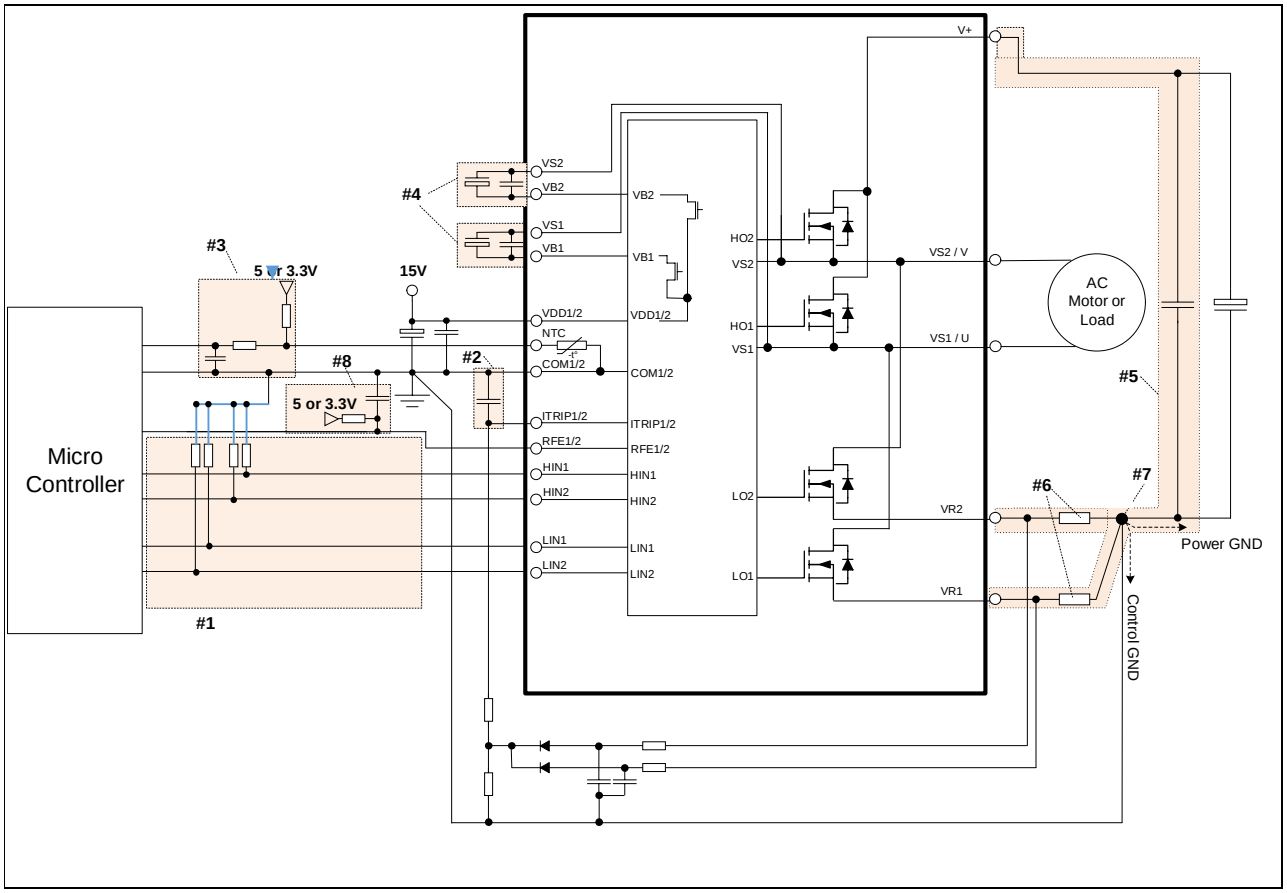



**Figure 14** Example of application circuit

1. **Input circuit**
   - Pull-down resistors on each PWM input (~30 kΩ).
2. **Itrip circuit**
   - To prevent faulty operation of the protection function, an RC filter is recommended.
   - The capacitor must be located close to Itrip and COM terminals.
3. **NTC circuit**
   - To define suitable voltage for temperature monitoring, this terminal should be pulled up to the bias voltage of 5 V/3.3 V by a proper resistor.
   - It is recommended that the RC filter be placed close to the controller.
4. **VB-VS circuit**
   - Capacitors for high-side floating supply voltage should be placed close to VB and VS terminals.
   - Additional high-frequency capacitors, typically 0.1 uF, are strongly recommended.
   - Overlap of pattern-to-motor and pattern-to-bootstrap capacitors should be minimized.
5. **Snubber capacitor**
   - The snubber capacitor and shunt resistors should be as short as possible.
6. **Shunt resistor**
   - SMD type shunt resistors are strongly recommended to minimize internal stray inductance.

7. **Ground pattern**
   - Pattern overlap of power ground and signal ground should be minimized. The patterns should be connected at the common end of shunt resistors only for the same potential.
8. **RFE circuit**
   - To set up R and C parameters for fault-clear time.
   - RFE is active-low. The pin should always be pulled up to 3.3 V or 5 V.
   - This R is also mandatory for the fault-reporting function because it is an open-drain structure.
   - Please refer to Section 3.2 for additional details.

## 4.3 Recommended circuit current of power supply

The recommended minimum current of the power supply is shown in Table 9 below. This value considers ripple and sufficient margins.

**Table 9 The recommended minimum circuit current of power supply [mA]**

| Item | The circuit current of +15 V control supply | The circuit current of +5 V logic supply |
|---|---|---|
| $V_{DD} \leq 20$ V, $F_{SW} \leq 20$ KHz | 90 | 45 |

## 4.4 Recommended layout pattern for ITRIP functions

It is recommended that the ITRIP filter capacitor connections to the IM111 pins be as short as possible. The ITRIP filter capacitor should be connected to the COM pin directly without an overlapped ground pattern. The signal ground and power ground should be as short as possible, and connected at only one point via the filter capacitor of $V_{DD}$ line. The ITRIP function combined with the external shunt resistor can be used to detect overcurrent events in the ground path that will result in the damaging of the IPM. The internal gate driver will continuously monitor the voltage on the ITRIP pin. If this voltage exceeds the reference voltage (typ. 0.5 V) a fault signal will be generated on the RFE pin, and all MOSFETs will be turned OFF.

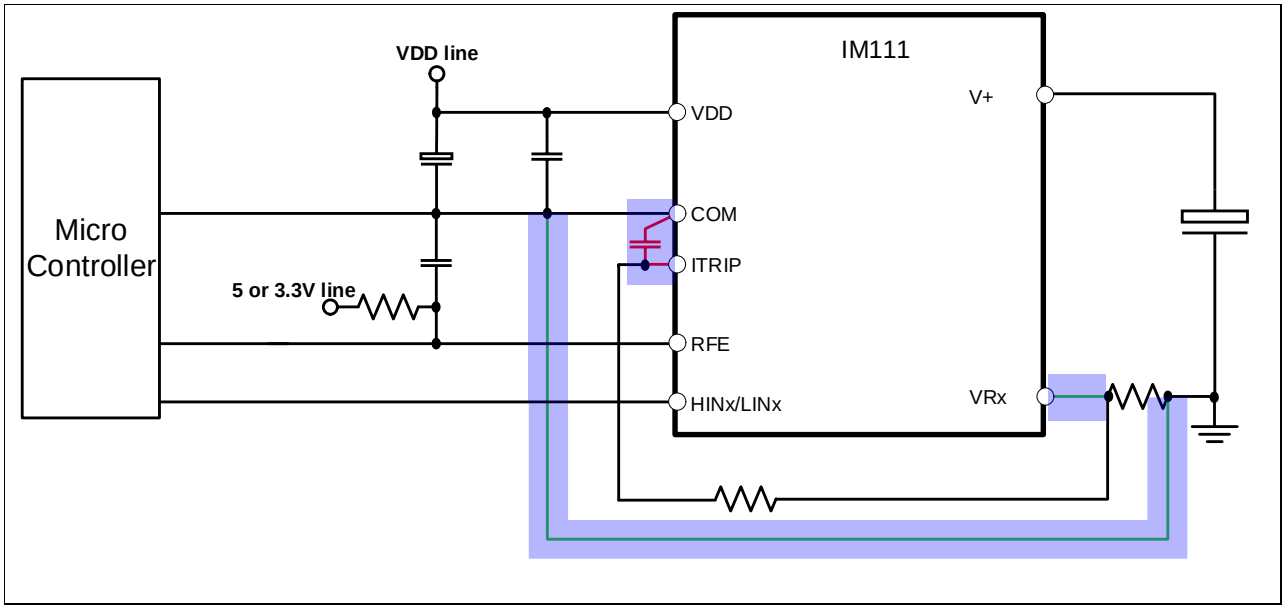



**Figure 15** Recommended layout for ground and overcurrent protection traces

## 4.5 Recommended wiring of shunt resistor and snubber capacitor

External current-sensing resistors are applied to detect the overcurrent of phase currents. A long wiring pattern between the shunt resistors and IM111 will cause excessive surges that might damage the IPM's internal gate drivers and current-detection components. This may also distort the sensing signals that may lead to loss of control when driving a motor. To decrease the pattern inductance, the wiring between the shunt resistors and IPM should be as short as possible, and any loop should be avoided.

As shown in Figure 16, snubber capacitors should be installed in the right location so as to suppress surge voltages effectively. Generally, a high-frequency non-inductive capacitor of around 0.1 ~ 0.22 µF is recommended. If the snubber capacitor is installed in the wrong location ('1' as shown in Figure 16), the snubber capacitor cannot suppress the surge voltage effectively. If the capacitor is installed in location '2', the charging and discharging currents generated by the wiring inductance and the snubber capacitor will appear on the shunt resistor. This will impact the current-sensing signal, and the SC protection level will be a bit lower than the calculated design value. The '2' position surge suppression effect is greater than in location '1' or '3'. The '3' position is a reasonable compromise with better suppression than location '1' without impacting the current-sensing signal accuracy. For this reason, the location '3' is generally used.

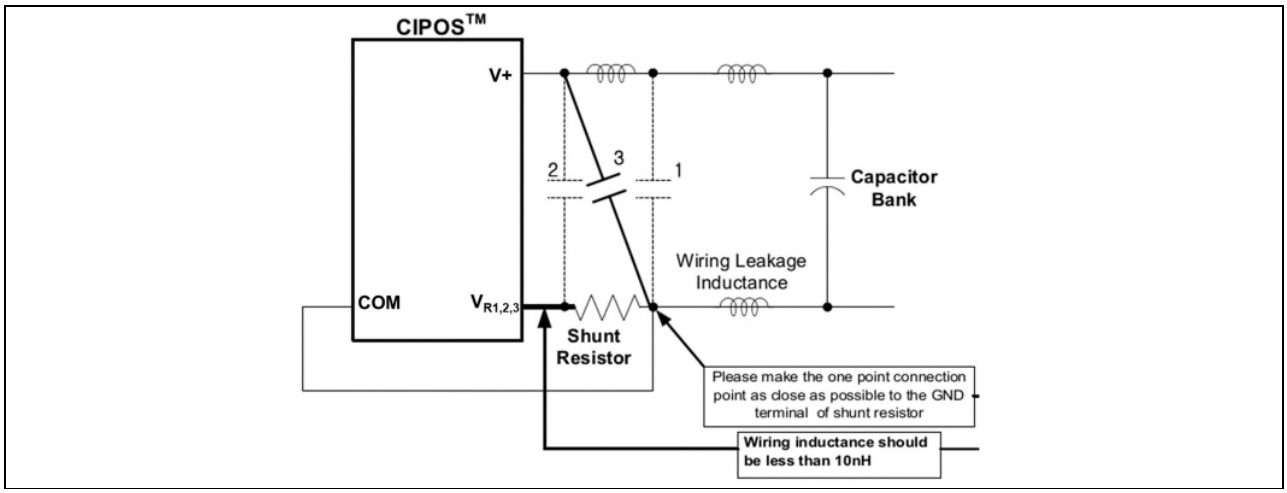



**Figure 16** Proper snubber capacitor use

General suggestions and summary:

- PCB traces should be designed as short as possible and the area of the circuit (power or signal) should be minimized to avoid any noise.
- Make sure there is a good distance between switching lines with high dI/dt and dV/dt and the signal lines, as they are very sensitive to electrical noise. Specifically, the trace of each OUT phase carrying significant fast current and voltage transition should be separated from the logic lines and analog sensing circuits (ITRIP, RFE).
- Place shunt resistors as close as possible to the low-side emitter pins of the IPM. Parasitic inductance should be as low as possible. Use of low inductance SMD resistors is recommended.
- Avoid any ground loop. Only a single path must connect to COM.
- Place each RC filter as close as possible to the IPM pins to increase their efficiency.
- Fixed voltage tracks such as GND and high-voltage lines can be used to shield the logic and analog lines from electrical noise produced by the switching lines.

# 5 Bootstrap circuit

## 5.1 Bootstrap-circuit operation

The $V_{BS}$ voltage, which is the voltage difference between $V_B$ (1-2) and $V_S$ (1-2), supplies voltage to the high-side circuitry of the gate driver, and must be in the range of 12.5~17.5 V. As described in Section 3.3, all IM111 have an undervoltage protection function for $V_{BS}$.

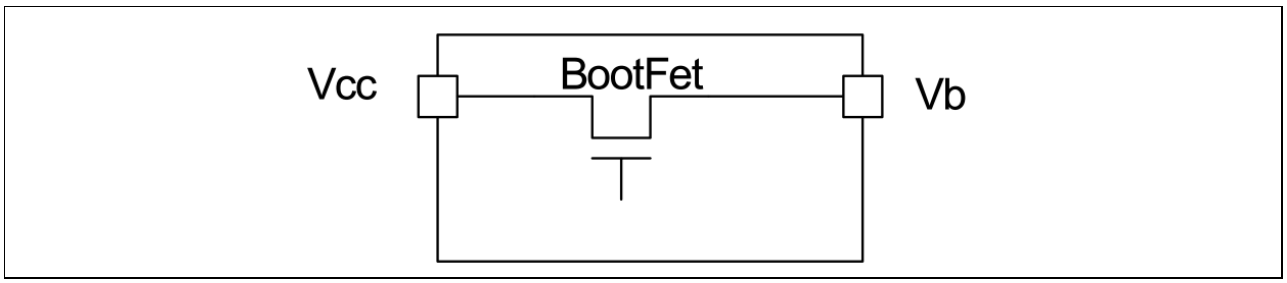



**Figure 17** Simplified BootFET internal connection

Internal bootstrap circuitry consists of three high-voltage bootFETs that eliminate the need for any external high-voltage diodes and resistors. One bootFET is integrated for each high-side output channel, and is connected between $V_{DD}$ supply and its respective floating supply ($V_{B1}$, $V_{B2}$) as shown in Figure 21. The integrated bootFET is turned ON during the time when LO is 'high', and has a limited source current due to intrinsic $R_{BS}$. $V_{BS}$ will increase each cycle depending on the duration of LO, value of the $C_{BS}$ capacitor, the collector-emitter drop of the corresponding low-side IGBT, and the low-side, free-wheeling diode drop.

The bootFET of each channel follows the state of low-side output stage, i.e. the bootFET is ON when LO is 'high', unless the $V_B$ voltage is higher than $V_{DD}$. In that case, the bootstrap FET is designed to remain off until $V_B$ returns below that threshold. This concept is illustrated in Figure 18.

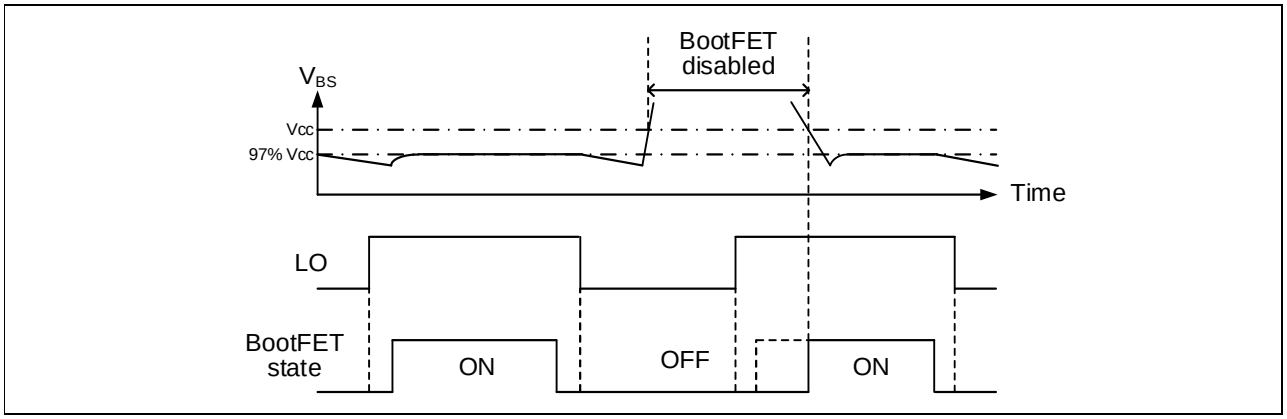



**Figure 18** BootFET timing diagram

A bootFET is suitable for most PWM modulation schemes, and can be used either in parallel with an external bootstrap network (diode + resistor) or as replacement of it. The use of the integrated bootstrap as a replacement of the external bootstrap network may, however, have some limitations. An example of this limitation may arise when this functionality is used in non-complementary PWM schemes and at very high PWM duty cycles. In these cases, superior performance can be achieved by using an external bootstrap diode and resistor in parallel with the internal bootstrap network.

## 5.2 Initial charging of bootstrap capacitor

To charge the bootstrap capacitor, a sufficient on-time duration of the low-side MOSFET is required for initial bootstrap charging. The initial charging time ($t_{charge}$) can be calculated from the following equation:

$$t_{charge} \geq \frac{C_{BS} \cdot R_{BS}}{\delta} \cdot \ln\left(\frac{V_{DD}}{V_{DD} - V_{BS(\min)} - V_{LS}}\right)$$

Where,

- $V_{BS(min)}$ = The minimum value of the bootstrap capacitor voltage
- $V_{LS}$ = Voltage drop across the low-side MOSFET
- δ = Duty ratio of PWM
-

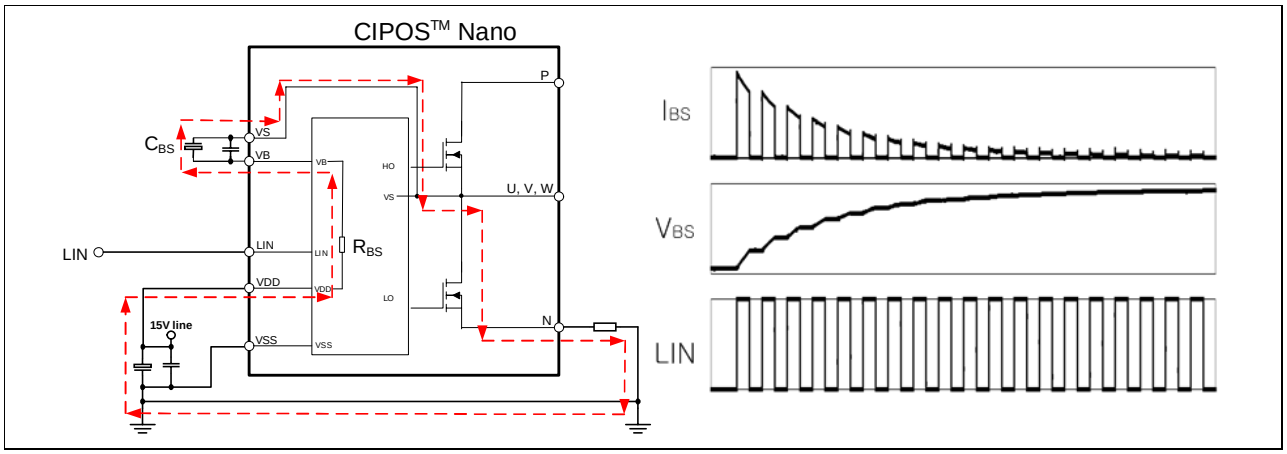



**Figure 19** BootFET circuit operation and timing chart of initial FET charging

## 5.3 Bootstrap capacitor selection

The bootstrap capacitance can be calculated by:

$$C_{BS} = \frac{I_{leak} \cdot \Delta t}{\Delta V_{BS}}$$

Where,

- Δt = maximum ON pulse width of high-side MOSFET
- $\Delta V_{BS}$ = the allowable discharge voltage of the $C_{BS}$
- $I_{leak}$= maximum discharge current of the $C_{BS}$ mainly via the following mechanisms:
  - Gate charge for turning on the high-side MOSFET
  - Quiescent current to the high-side circuit in the IC
  - Level-shift charge required by level shifters in the IC
  - Leakage current in the bootstrap diode
  - $C_{BS}$ capacitor leakage current (ignored for non-electrolytic capacitors)
  - Bootstrap-diode reverse-recovery charge

In practice, a leakage current of 1 mA is recommended as a calculation basis. By taking into consideration dispersion and reliability, the capacitance is generally selected to be 2~3 times higher than the calculated one.

The $C_{BS}$ is only charged when the high-side MOSFET is off and the VS voltage is pulled down to ground. Therefore, the ON-time of the low-side MOSFET must be sufficient to ensure that the charge drawn from the $C_{BS}$ capacitor can be fully replenished. Hence, inherently there is a minimum ON-time of the low-side MOSFET (or OFF-time of the high-side MOSFET).

The bootstrap capacitor should always be placed as close to the module pins as possible. At least one low ESR capacitor should be used to provide good local de-coupling. For example, a separate ceramic capacitor close to the IPM is essential if an electrolytic capacitor is used for the bootstrap capacitor. If the bootstrap capacitor is either a ceramic or tantalum type, it should be adequate for local decoupling.

## 5.4 Charging/ discharging of bootstrap capacitor during operation

The bootstrap capacitor $C_{BS}$ charges through the bootFET from the $V_{DD}$ supply when the high-side MOSFET is off, and the VS voltage is pulled down to ground. It discharges when the high-side MOSFET or diode are on.

### 5.4.1 Example 1: Selection of initial charging time

An example calculation of the minimum value of the initial charging time:

Conditions:

- $C_{BS}$=4. 7 µF, $R_{BS}$ = 200 Ω, Duty Ratio (δ)= 0.5, $V_{DD}$ = 15 V
- $V_{BS\,(min)}$ = 12.5 V
- $V_{LS}$ = 0.1 V
- $t_{charge} \geq 4.7\mu F \times 200\Omega \times \frac{1}{0.5} \times \ln(\frac{15V}{15V-12.5V-0.1V})$

In order to ensure safety, it is recommended that the charging time must be at least three times longer than the calculated value.

### 5.4.2 Example 2: Minimum value of bootstrap capacitor

Based on the conditions given above, a minimum value of bootstrap capacitor can be chosen based on switching frequency.

Conditions:

- $\Delta V_{BS}$=0.1 V, $I_{leak}$= 1 mA

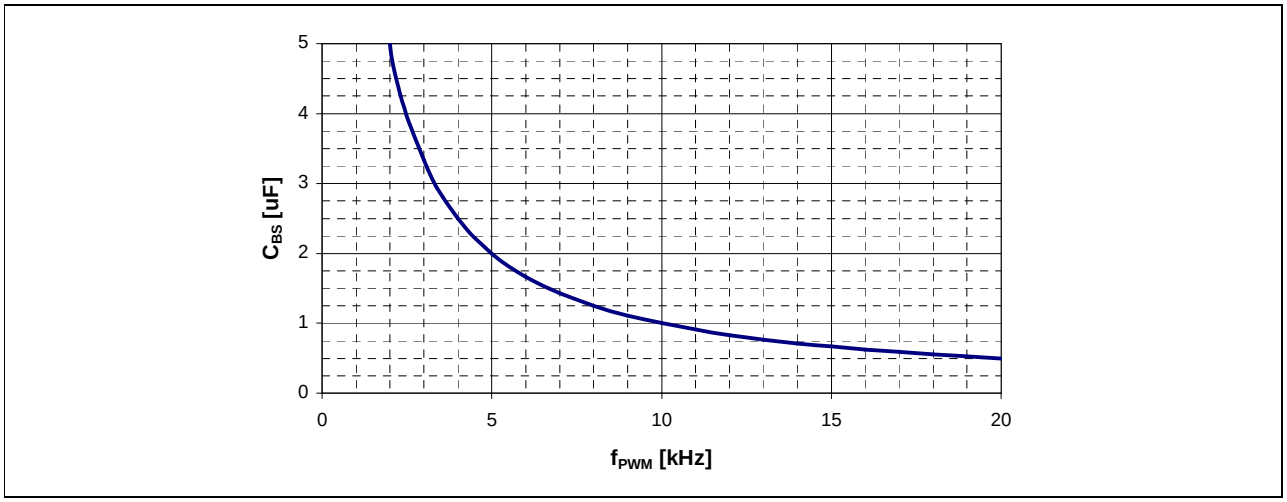



**Figure 20** Bootstrap capacitance as a function of switching frequency

Figure 20 shows the curve for a continuous sinusoidal modulation if the voltage ripple ($\Delta V_{BS}$) is 0.1 V. The recommended bootstrap capacitance for a continuous sinusoidal modulation method is therefore in the range of up to 2.2 µF for most common switching frequencies.

It is recommended that the system design considers the actual control pattern when designing the bootstrap circuit.

# 6 Thermal system design

The thermal design of a system is a key issue included in electronic systems such as drives. In order to avoid overheating and/or to increase the reliability, two design criteria are of importance:

- Low power losses
- Low thermal resistance from junction to ambient

The first criterion is already fulfilled when choosing CIPOS™ Nano as an intelligent power module for the application. A good thermal design allows the user to either maximize the power or to increase the reliability of the system (by reducing the maximum temperature).

For the thermal design, the following is required:

- The maximum power losses $P_{sw,i}$ of each power switch
- The maximum junction temperature $T_{J,\ max}$ of the power semiconductors
- The maximum allowable ambient temperature $T_{A,\ max}$
- The junction-to-ambient thermal resistance impedance $Z_{th,\ J\text{-}A}$. For steady-state considerations, the static thermal resistance $R_{th,J\text{-}A}$ is sufficient. This thermal resistance comprises the junction-to-case thermal resistance $Rth_{,J\text{-}C}$ as provided in datasheets, and the heat case-to-ambient thermal resistance $R_{th,C\text{-}A}$.
- For detailed thermal design of CIPOS™ Nano, please refer to the following application note AN2018-24: https://www.infineon.com/dgdl/Infineon-CIPOS_Nano_QFN-based_IPM-ApplicationNotes-v02_00-EN.pdf?fileId=5546d462584d1d4a0158bf28a6ac5856

## 6.1 Online motor-drive-simulation tool

The CIPOS™ IPM Motor Drive Simulation Tool, which is available on Infineon's website (www.infineon.com/plex-ipm), offers help to users for part selection and design decisions. This tool allows the user to simulate and compare IPM parts to determine which module best suits their needs. The tool shows the expected temperature of the selected IPM, the approximate losses of the system, and also generates output voltage, current, junction temperature and loss waveforms. It is recommended to test parts with planned motor conditions in the simulation tool prior to physical design. A user manual and video tutorial to aid in tool use is provided on the webpage.

This tool provides a breakdown of losses, and can provide a glimpse of the tradeoff between switching and conduction losses in the module for given conditions and design. Alternatively, these losses can be calculated based on the formulas discussed in the next sections.

## 6.2 Power loss

Total power losses in the module are composed of conduction and switching losses in the power switch.

Detailed equations are provided below to calculate both conduction and switching losses of the module for a three-phase continuous sinusoidal modulation scheme. For other cases, like three-phase discontinuous modulation, please see [1].

### 6.2.1 Conduction loss

Conduction losses depend on the DC electrical characteristics of the device, i.e., saturation voltage. Therefore, it is a function of the conduction current and the device's junction temperature.

The typical characteristics of forward drop voltage are approximated by the following linear equation for the MOSFET and the diode, respectively:

$$V_{MOSFET} = R_{ds} \cdot i$$
$$V_{DIODE} = V_D + R_D \cdot i$$

Where,

- $V_D$= Threshold voltage of body diode
- $R_{ds}$= ON-state resistance of MOSFET
- $R_D$=ON-state slope resistance of body diode
- Assuming that the switching frequency is high, the output current of the PWM inverter can be assumed to be sinusoidal and can be calculated by:
- $i = I_{Peak} \cdot \cos(\theta - \varphi)$

Where,

- $\varphi$ = phase angle difference between output voltage and current.
- Using the equations above, the conduction loss of one MOSFET and its body diode can be obtained as follows:
- $$P_{con.M} = \frac{1}{2\pi}\int_0^{\pi} \xi(V_{MOSFET} \times i)d\theta = \frac{I_{peak}^{\ 2}}{8}R_{ds} + \frac{I_{peak}^{\ 2}}{3\pi}R_{ds}MIcos\varphi$$
- $$P_{con.D} = \frac{1}{2\pi}\int_0^{\pi} (1-\xi)(V_{DIODE} \times i)d\theta = \frac{I_{peak}}{2\pi}V_D - \frac{I_{peak}}{8}V_D MIcos\varphi + \frac{I_{peak}^{\ 2}}{8}R_D - \frac{I_{peak}^{\ 2}}{3\pi}R_D MIcos\varphi$$
- $P_{con} = P_{con.M} + P_{con.D}$
- Where,
- $\delta$= duty cycle given in PWM method.
- This can be calculated by:
- $\delta = \frac{1+MI\cos(\theta)}{2}$
- Where,
- MI = PWM modulation index (MI, defined as the peak phase voltage divided by half of DC link voltage).
- It should be noted that the total inverter conduction losses are six times that of $P_{con}$.

### 6.2.2 Switching loss

Switching losses are determined by dynamic characteristics like turn-on and off time as well as the presence of overvoltage and overcurrent transients. Hence, in order to obtain the accurate switching loss, the DC-link voltage of the system, the applied switching frequency and the power circuit layout, operating current and operating temperature should be considered.

Therefore the linear dependency of the switching energy loss on the switched current is expressed during one switching period as follows:

$$E_M = E_{M.on} + E_{M.off}$$
$$E_D = E_{D.on} + E_{D.off}$$

Where,

- $E_M$= switching loss energy of the MOSFET
- $E_D$= switching loss energy of body diode
- $E_M$ and $E_D$ can be considered a constant.

As mentioned in the conduction-loss explanation, the output current can be considered a sinusoidal waveform, and the switching loss occurs every PWM period for the continuous PWM schemes. Therefore depending on the switching frequency, $f_{sw}$, the switching loss of one device is the following equation:

$$P_{sw} = \frac{1}{2\pi}\int_0^{\pi}(E_M + E_D)\cdot i \cdot f_{sw}\,d\varphi = \frac{(E_M + E_D)\cdot f_{sw}\cdot I_{peak}}{\pi}$$

- These constants should be derived by experimental measurement. From the above equation, it should be noted that the switching losses are a linear function of current, and directly proportional to switching frequency.

# 7 References

[1] D. Chung, S. Sul, "Minimum-Loss Strategy for three-Phase PWM Rectifier", IEEE Transactions on Industrial Electronics, Vol. 46, No. 3, June 1999

## Revision history

| Document version | **Date of release** | **Description of changes** |
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