CIPOS™ Micro IPM Application Note

For IRSM5xx and IM240 Only

About this document

Scope and purpose

This application note describes the part portfolio of IRSM5xx and IM240 of the product family CIPOS™ Micro Intelligent Power Modules (IPM) and should be used in parallel with each part's datasheet. This document first gives an overview of the product line-up and datasheet information. It details the functionality of the modules and then provides recommendations for designing the external circuitry that interfaces with the modules. The application note ends with thermal-design considerations and heat-sinking guidelines.

Intended audience

Power electronics engineers who want to design reliable and efficient motor drive applications for part line-up IRSM5xx and IM240 of the product family CIPOS™ Micro IPM.

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1 Introduction

The CIPOS™ Micro IPM is a family of compact, three-phase, intelligent power modules (IPM) for low-power motor drive applications including fans, pumps, air purifiers and refrigerator compressor drives. It offers a cost-effective and fast time-to-market power solution by leveraging industry-standard footprints compatible with various PCB substrates such as FRx and CEMx.

CIPOS™ Micro IPMs are comprised of 600 V IGBT, 250 V MOSFET and 500 V FREDFET- based parts. All CIPOS™ Micro IPMs contain three half-bridge driver ICs with an optional UL-certified Negative Temperature Coefficient (NTC) thermistor as a temperature sensor. The MOSFET-based parts feature rugged and efficient high-voltage Fast Recovery Diode MOSFETs (FREDFETs) specifically optimized for variable frequency drives with voltage ratings of 250 V and 500 V. Reverse-conducting RC-DF IGBT-based IPMs were developed specifically to increase the power range of the CIPOS™ Micro IPM family to approximately 200 W.

These IPMs feature high-voltage gate drivers tuned to achieve an optimal balance between EMI and switching losses. CIPOS™ Micro IPM family offers DC current ratings ranging from up to 6 A to drive motors up to 100 W without heatsink and up to 300 W with a heatsink. IPMs in this family are available in both through-hole and surface-mount package options.

This application note concerns the following products:

1.1 Product line-up

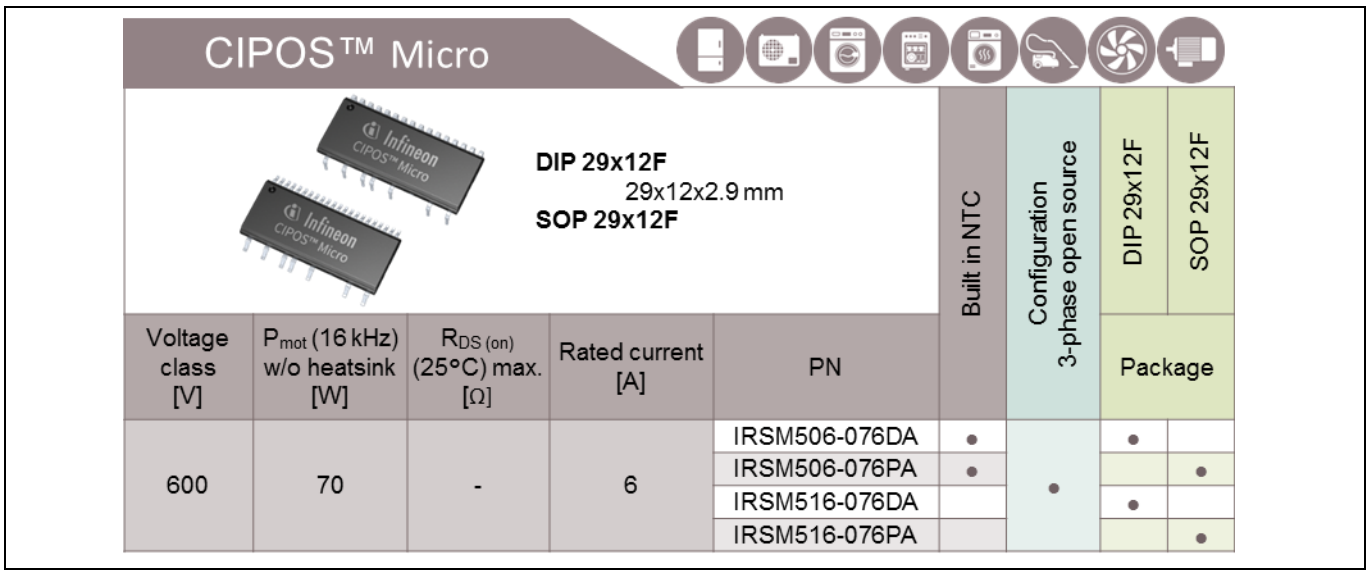
CIPOS™ Micro



DIP 29x12F
29x12x2.9 mm
SOP 29x12F

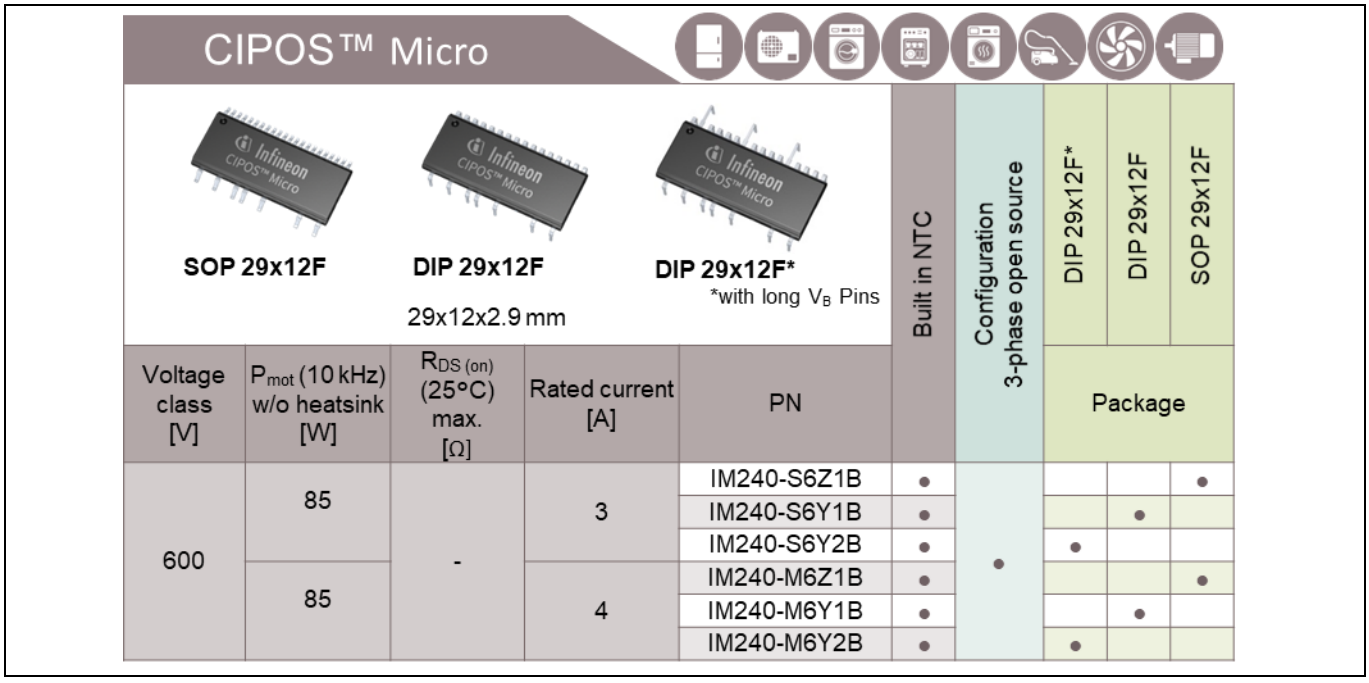
Voltage class [V]	P_{mot} (16 kHz) w/o heatsink [W]	$R_{DS\ (on)}$ (25°C) max. [Ω]	Rated current [A]	PN	Built in NTC	Configuration 3-phase open source	Package: DIP 29x12F	Package: SOP 29x12F
250	35	2.2	-	IRSM505-024DA	•	•	•	
				IRSM505-024PA	•			•
				IRSM515-024DA			•	
				IRSM515-024PA				•
	50	1.05	-	IRSM505-044DA	•		•	
				IRSM505-044PA	•			•
				IRSM515-044DA			•	
				IRSM515-044PA				•
	70	0.45	-	IRSM505-084DA	•		•	
				IRSM505-084PA	•			•
				IRSM515-084DA			•	
				IRSM515-084PA				•
500	40	6.0	-	IRSM505-015DA	•		•	
				IRSM505-015PA	•			•
				IRSM515-015DA			•	
				IRSM515-015PA				•
	45	4.0	-	IRSM505-025DA	•		•	
				IRSM505-025PA	•			•
				IRSM515-025DA			•	
				IRSM515-025DA				•
	50	2.2	-	IRSM505-035DA	•		•	
				IRSM505-035PA	•			•
				IRSM515-035DA			•	
				IRSM515-035PA				•
	55	1.7	-	IRSM505-055DA	•		•	
				IRSM505-055PA	•			•
				IRSM515-055DA			•	
				IRSM515-055PA				•
		1.3	-	IRSM505-065DA	•		•	
				IRSM505-065PA	•			•
				IRSM515-065DA			•	
				IRSM515-065PA				•

Figure 1 MOSFET CIPOS™ Micro IPM line-up



Voltage class [V]	P_{mot} (16 kHz) w/o heatsink [W]	$R_{DS\ (on)}$ (25°C) max. [Ω]	Rated current [A]	PN	Built in NTC	Configuration 3-phase open source	Package: DIP 29x12F	Package: SOP 29x12F
600	70	-	6	IRSM506-076DA	•	•	•	
				IRSM506-076PA	•			•
				IRSM516-076DA			•	
				IRSM516-076PA				•

Figure 2 IGBT CIPOS™ Micro IPM line-up



Voltage class [V]	P_{mot} (10 kHz) w/o heatsink [W]	$R_{DS\ (on)}$ (25°C) max. [Ω]	Rated current [A]	PN	Built in NTC	Configuration 3-phase open source	Package: DIP 29x12F*	Package: DIP 29x12F	Package: SOP 29x12F
600	85	-	3	IM240-S6Z1B	•	•			•
				IM240-S6Y1B	•			•	
				IM240-S6Y2B	•		•		
	85		4	IM240-M6Z1B	•				•
				IM240-M6Y1B	•			•	
				IM240-M6Y2B	•		•		

Figure 3 RC-DF IGBT CIPOS™ Micro IPM line-up

1.2 Nomenclature

The charts below show the nomenclature used within CIPOS™ Micro IPMs. The first chart explains the historical nomenclature beginning with IRSM. The second is the current nomenclature beginning with IM.

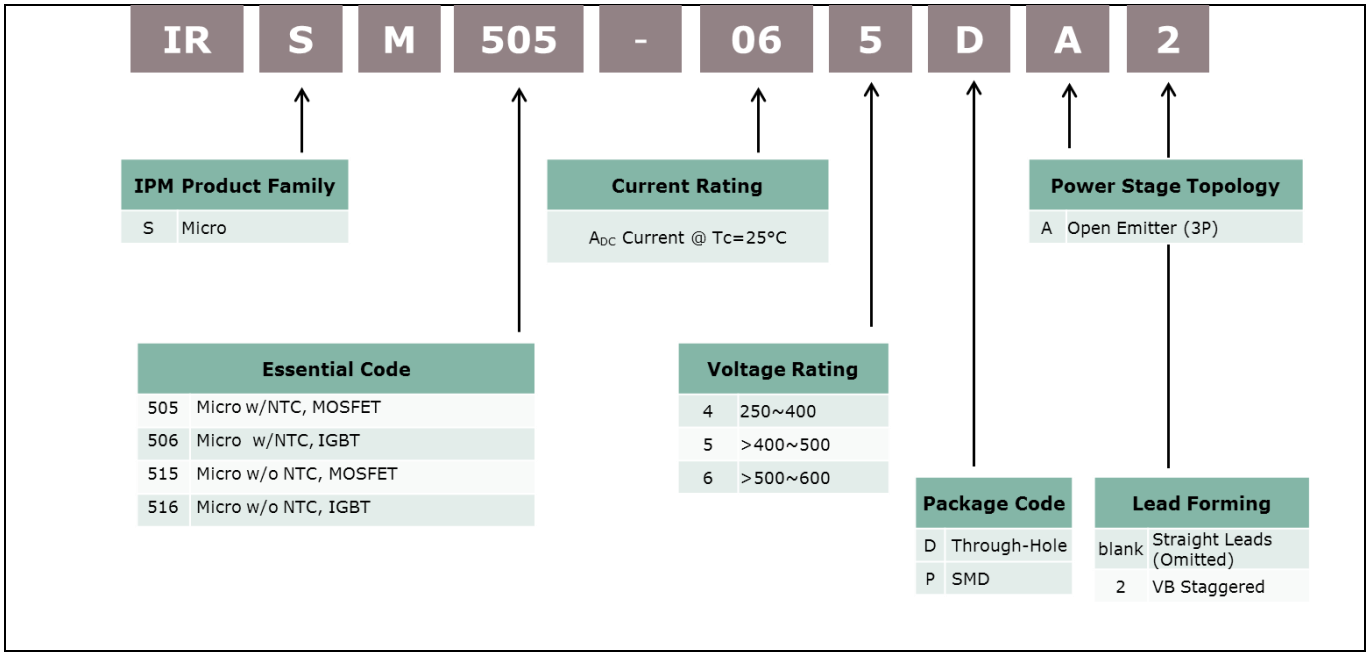


Figure 4 Nomenclature for CIPOS Micro IRSM

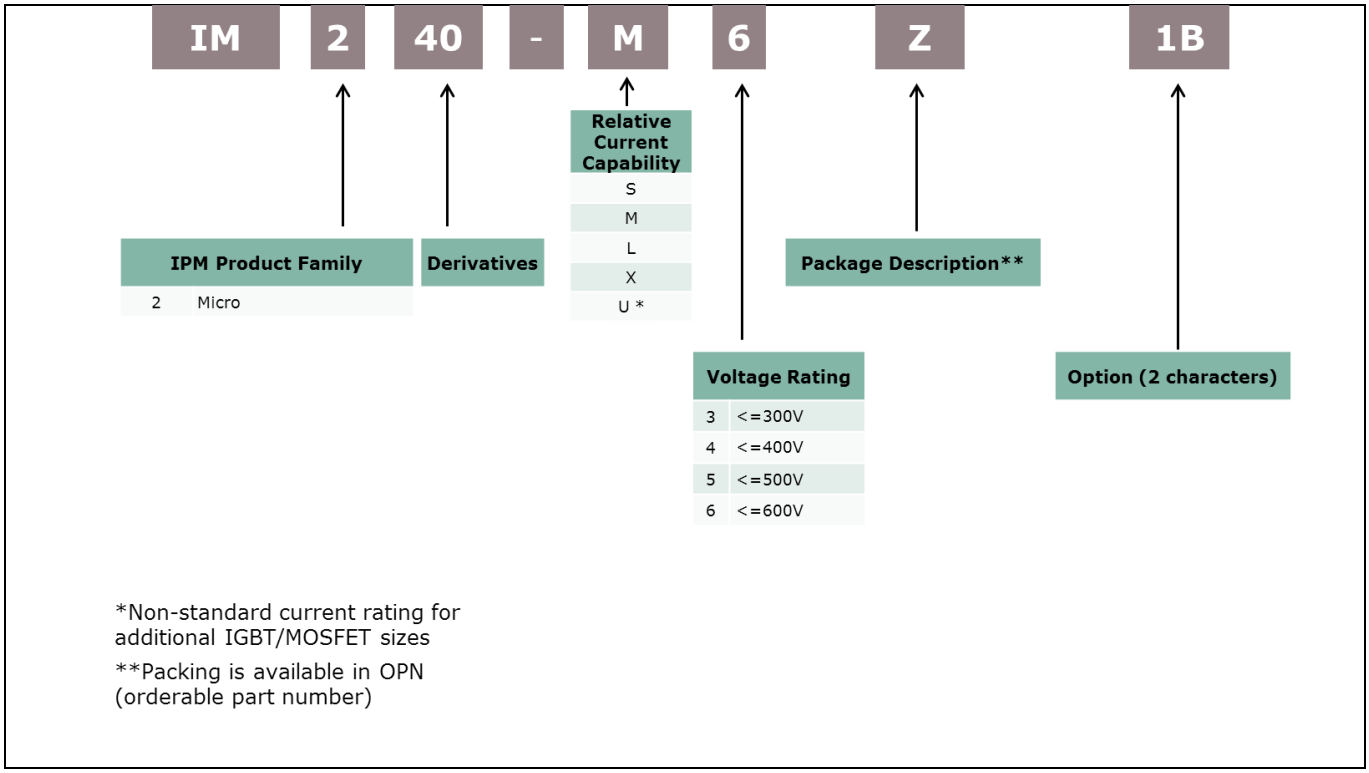


Figure 5 Nomenclature for next generation CIPOS Micro IPMs

1.3 Application positioning

Major applications for line-up, IRSM5xx and IM240 of the CIPOS™ Micro IPM product family, include:

- Fridge
- Air-conditioning fans
- Ventilation fans
- Dishwasher pumps
- Laundry dryer fans
- Small servo drives
- Window shutters

2 Product overview

2.1 Internal circuit and features

Figure 6 illustrates the internal block diagram of the CIPOS™ Micro IRSM5xx and IM240 series. These products consist of a three-phase IGBT, RC-DF IGBT or MOSFET inverter, and three half-bridge driver IC's with an optional NTC thermistor. The detailed features and integrated functions are described as follows:

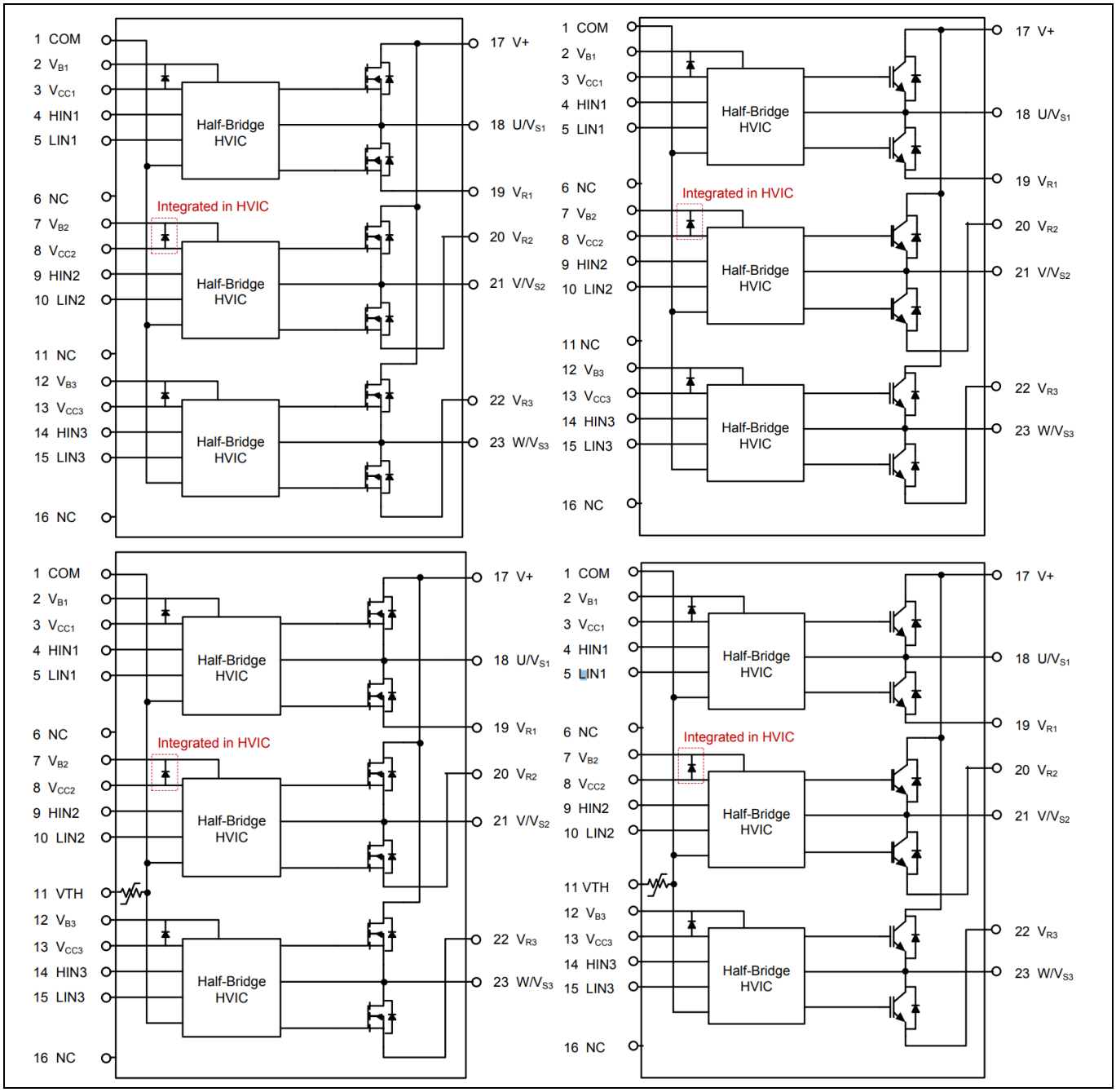


Figure 6 MOSFET and IGBT CIPOS™ Micro IPMs with and without NTC

Key features:

- 250 V to 600 V rating in one physical package size (mechanical layouts are identical)
- Fully isolated Dual In-line Package (DIP) and surface-mount Small Outline Package (SOP)-molded module

Product overview

- Incorporated Infineon Low $V_{CE(sat)}$ RC-DF IGBTs for the IM240 series, Trench IGBTs for the IRSM5x6 series, and TRENCH FREDFETs for the IRSM5x5 series
- Undervoltage lockout for all channels
- Integrated bootstrap functionality
- 3.3 V logic compatible
- Drive tolerant to negative voltage ($-V_s$)
- Matched propagation delay for all channels
- Optimized dV/dt for loss and EMI tradeoffs
- Separate low-side emitter pins for single or leg-shunt current sensing
- Advanced input filter with shoot-through protection
- UL-certified Temperature Sense (NTC)
- Up to Isolation 1900 V_{RMS}, 1 min

Key benefits:

- Ease of design and short time to market
- Compact package with three lead-form options available
- Wide range of current and voltage ratings in the same package
- Wide range of modules for 110 V_{AC} or 230 V_{AC} applications in the same footprint
- Simplified design and manufacturing
- Lower losses than similar modules in the market
- Heatsink-less operation possible

2.2 Input and output pins

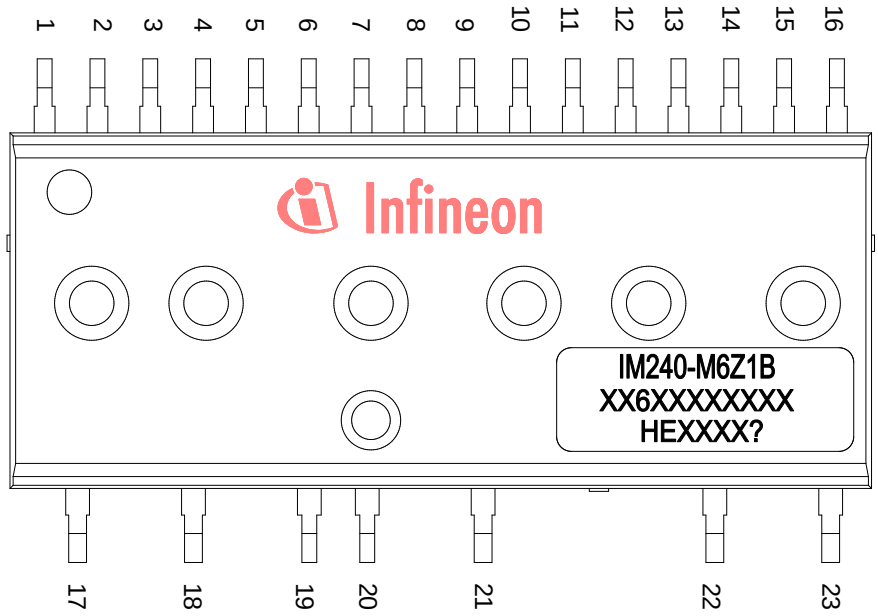


Figure 7 Module pinout

Product overview

Table 1 Pin assignment

Pin	Name	Description
1	COM	Logic ground
2	V_{B1}	High-side floating supply voltage 1
3	V_{DD1}	Low-side control supply 1
4	HIN1	Logic input for high-dide gate driver - Phase 1
5	LIN1	Logic input for low-side gate driver - Phase 1
6	NC	Not connected
7	V_{B2}	High-side floating supply voltage 2
8	V_{DD2}	Low-side control supply 2
9	HIN2	Logic input for high-side gate driver - Phase 2
10	LIN2	Logic input for low-side gate driver - Phase 2
11	VTH	Thermistor output
	NC	Not connected for non-thermistor parts
12	V_{B3}	High-side floating supply voltage 3
13	V_{DD3}	Low-side control supply 3
14	HIN3	Logic input for high-side gate driver - Phase 3
15	LIN3	Logic input for low-side gate driver - Phase 3
16	NC	Not connected
17	V+	Dc bus voltage positive
18	U/V_{S1}	Output - phase 1, high-side floating supply offset 1
19	V_{R1}	Phase 1 low-side emitter
20	V_{R2}	Phase 2 low-side emitter
21	V/V_{S2}	Output - phase 2, high-side floating supply offset 2
22	V_{R3}	Phase 3 low-side emitter
23	W/V_{S3}	Output – phase 3, high-side floating supply offset 3

2.2.1 Pin descriptions

HIN (1,2,3) and LIN (1,2,3) (High-side and low-side control pins)

These pins are positive-logic, and are responsible for the control of the integrated IGBT/MOSFET. The Schmitt-trigger input thresholds are such to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. Pull-down resistor of about 800 kΩ is internally provided to pre-bias inputs during supply start-up, and an ESD diode is provided for pin-protection purposes. The input Schmitt trigger and noise filter provide beneficial noise rejection to short input pulses.

The noise filter suppresses control pulses which are below the filter time T_{FILIN}. The filter acts as according to Figure 8.

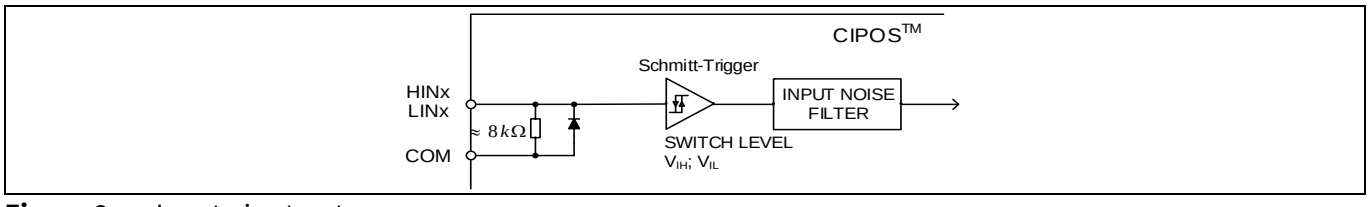


Figure 8 Input pin structure

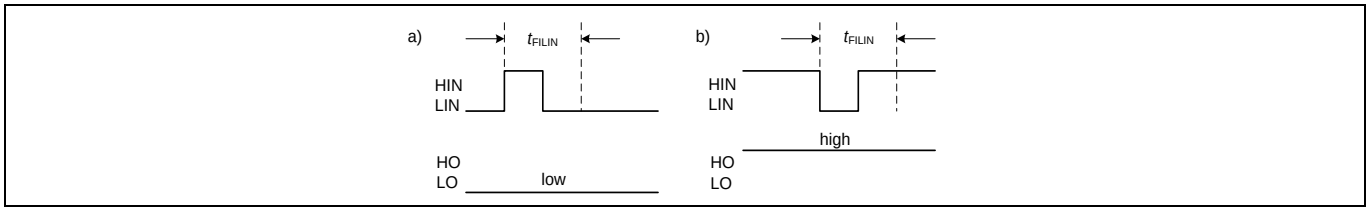


Figure 9 Input filter timing diagram

The integrated gate drive provides additionally a shoot-through prevention capability which avoids the simultaneous on-state of the high-side and low-side switch of the same inverter phase. A minimum dead time insertion of typically 300 ns is also provided by the driver IC in order to reduce cross-conduction of the external power switches.

V_{DD} (V_{CC}), COM (Low-side control supply and reference)

V_{DD} is the control supply providing power both to the input logic and to the output power stage. Input logic is referenced to COM ground. For the IRSM5xx product line-up, the control supply is labeled as V_{CC}. This application note will only refer to the control supply as $V_{DD,}$ however, it also applies to the IRSM5xx line-up.

The undervoltage circuit enables the device to operate at power 'on' when a supply voltage of at least a typical voltage of V_{DDUV+} is present.

The IC shuts down all the gate driver's power outputs, when the V_{DD} supply voltage is below V_{DDUV-}. This prevents the external power switches from critically low gate-voltage levels during on-state, and therefore from excessive power dissipation.

$V_{B(1,2,3)}$ and $V_{S(1,2,3)}$ (High-side supplies)

V_B to V_S is the high-side supply voltage. The high-side circuit can float with respect to COM following the external high-side power device emitter voltage.

Due to the low power consumption, the floating driver stage is supplied by an integrated bootstrap circuit.

The undervoltage detection operates with a rising supply threshold of typically V_{BSUV+} = 11.1 V and a falling threshold of V_{BSUV-} = 10.9 V.

$V_{S(1,2,3)}$ provides a high robustness against negative voltage with respect to COM. This ensures very stable designs even under rough conditions.

$V_{R(1,2,3)}$ (Low-side emitters)

The low-side emitters are available for current measurements of each phase leg. It is recommended to keep the connection to pin COM as short as possible in order to avoid unnecessary inductive voltage drops.

VTH (Thermistor output)

A UL-certified NTC is integrated in the module with one terminal of the chip connected to COM and the other to VTH. When pulled up to a rail voltage such as V_{DD} or 3.3 V by a resistor, the VTH pin provides an analog voltage signal corresponding to the temperature of the thermistor.

U/V_{S1}, V/V_{S2}, W/V_{S3} (High-side emitter and low-side collector)

These pins are motor U, V, W input pins.

V+ (Positive bus input voltage, Pin 23)

The high-side IGBTs are connected to the bus voltage. It is noted that the bus voltage does not exceed 450 V.

2.3 Package variations

Most CIPOS™ Micro IPM parts are available in three package variations: surface-mount (SOP 29x12F), standard through-hole (DIP29x12F) and through-hole with long V_B pins. These package variations are illustrated in Figure 10.

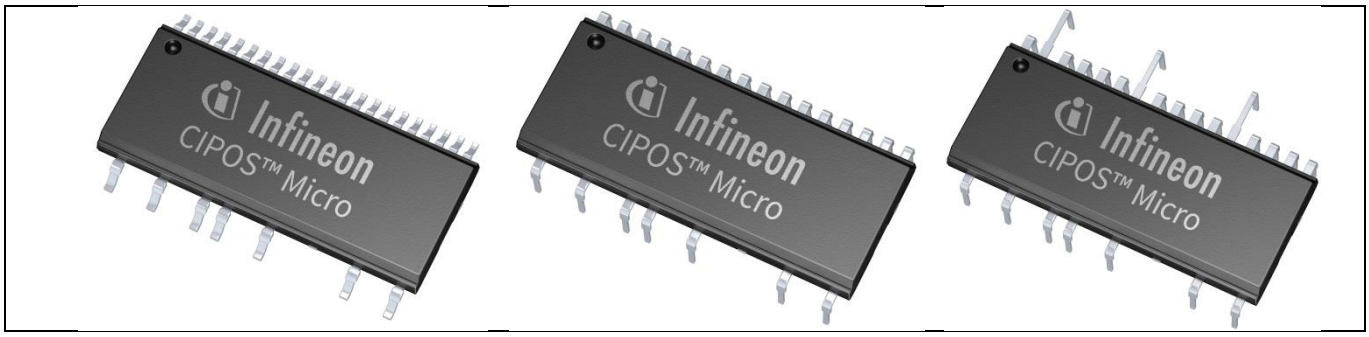


Figure 10 SOP 29x12F (left), and DIP29x12F (middle and right) package types

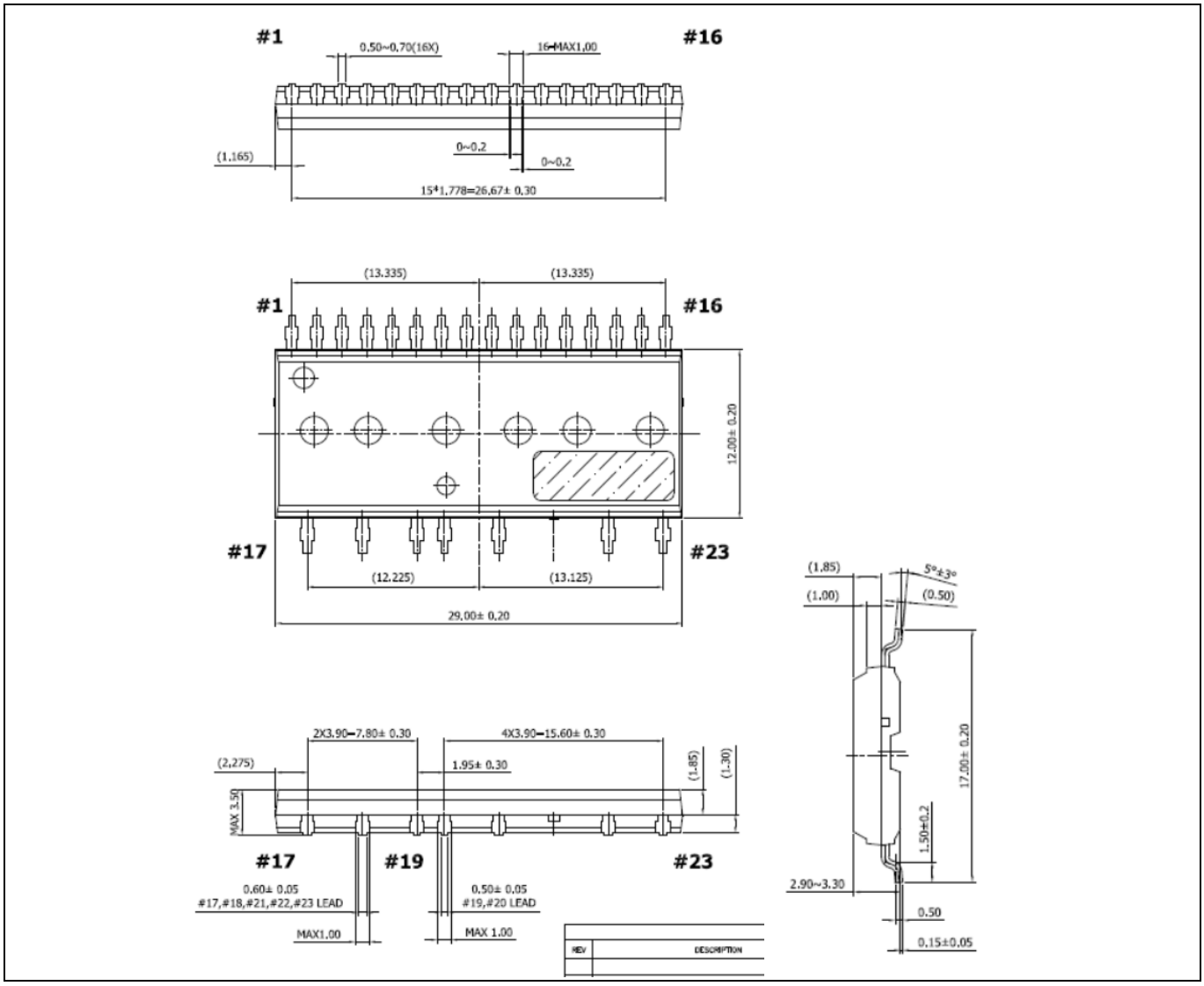


Figure 11 SOP 29x12F (dimensions in mm)

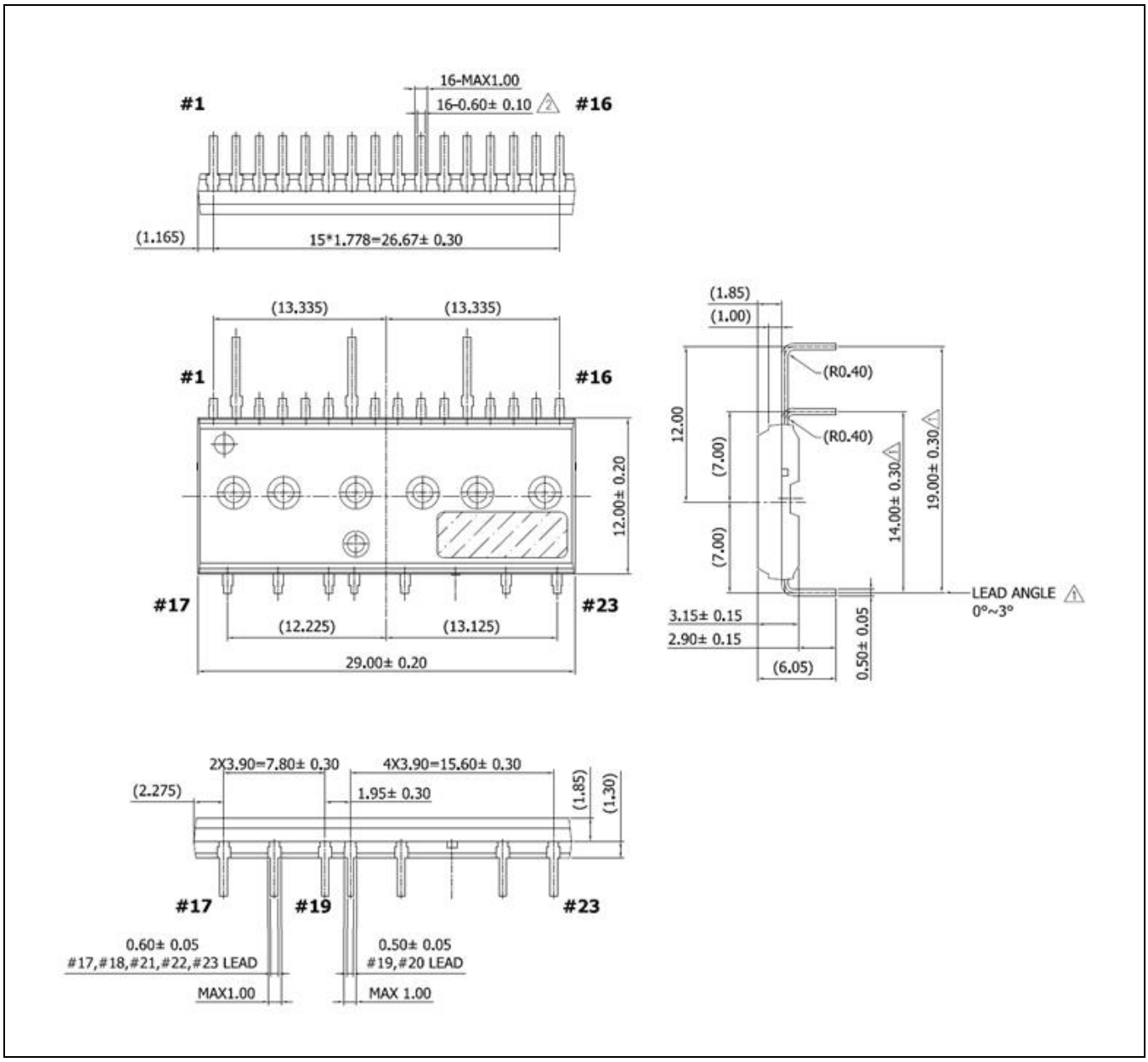


Figure 12 DIP29x12F w/ long V_B pins (dimensions in mm)

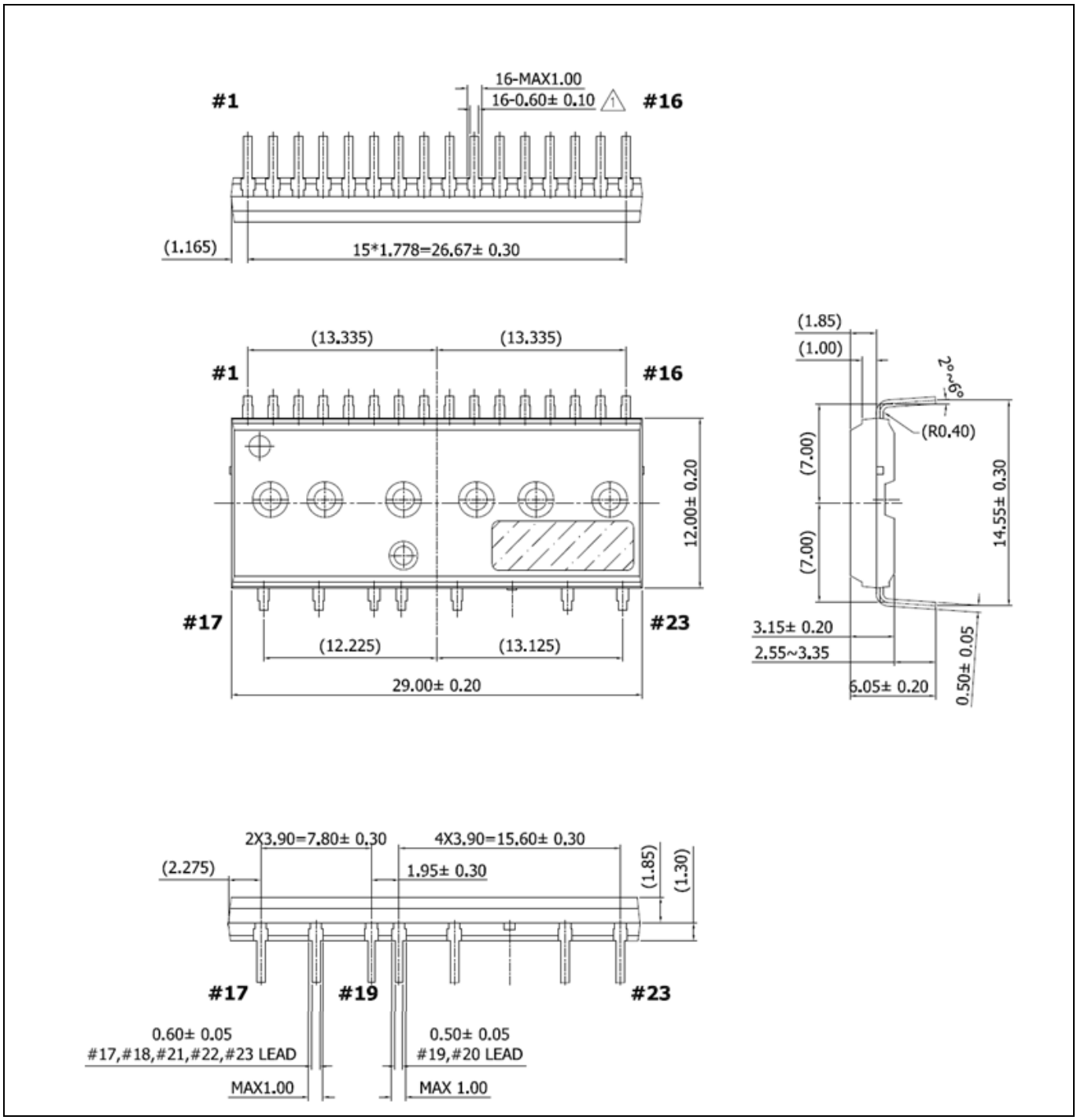


Figure 13 DIP29x12F (Dimensions in mm)

2.4 Maximum rating descriptions

Absolute maximum ratings indicate sustained limits beyond which damage to the module may occur. These are not tested in production. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the tables. These values can be viewed in the specific part's datasheet. Appropriate design margins should be implemented to ensure that all absolute maximum ratings are observed at all times during operation. This includes abnormal conditions like start-up, shut-down, overload, short-circuit, and system failure. Section 6 provides detailed instructions to help assess the temperatures of the device based on operating conditions. Please reference below for more in-depth descriptions of these ratings.

2.4.1 IM240 series

Table 2 Module

Parameter	Symbol	Description
Storage temperature	T_{STG}	Storage temperature range for reliable performance over life of device
Operating case temperature	T_C	Temperature range of package top surface (surface with part marking)
Operating junction temperature	T_J	Temperature range of the internal junction of power switches and gate drivers
Isolation test voltage	V_{ISO}	60 Hz voltage that can be applied for one minute between all pins and top surface of the module. This is a UL-certified rating (E252584).

Table 3 Inverter

Parameter	Symbol	Description
Max. blocking voltage	V_{CES}/V_{RRM}	Maximum voltage that can be applied across each IGBT
Output current	I_O	Current class to aid in selection of right part number
Peak output current	I_{OP}	Pulsed output current capability from single switch at specified temperature and t_P (duration of time at peak)
Peak power dissipation per IGBT	P_{tot}	Total peak power dissipation per switch
Short-circuit withstand time	T_{SC}	At specified conditions

Table 4 Control

Parameter	Symbol	Description
Low-side control supply voltage	V_{DD}	Maximum voltage range of input supply voltage
Input voltage LIN, HIN	V_{IN}	Maximum voltage range in reference to V_{DD}
High-side floating supply voltage (V_B reference to V_S)	V_{BS}	Maximum voltage range of input supply voltage

2.4.2 IRSM5xx series

Table 5 Absolute maximum ratings

Symbol	Parameter	Description
BV_{DSS}	Drain-to-source breakdown voltage	(MOSFET IPMs only) Maximum voltage that can be applied across each MOSFET before reverse conduction exceeds a threshold of typically 250 µA
V_{CES}/V_{RRM}	IGBT/ FW diode-blocking voltage	(IGBT IPMs only) Maximum voltage that can be applied across each IGBT before reverse conduction exceeds a threshold of typically 250 µA.
I_O @ T_C=25 °C	DC output current per MOSFET/IGBT	DC output current at maximum junction temperature considering typical thermal resistance
I_{OP} @ T_C =25 °C	Pulsed output current per MOSFET/ IGBT (Note 1)	Pulsed output current rating at $T_J \leq 150$ and t_P (duration of time at peak)
P_d @ T_C=25 °C	Maximum power dissipation per MOSFET/ IGBT	Total max power dissipation per switch
V_{ISO}	Isolation voltage (1 min)	60 Hz voltage that can be applied for one minute between all pins and top surface of the module. This is a UL-certified rating (E252584).
T_J	Operating junction temperature	Temperature range of the internal junction of power switches and gate drivers
T_C	Operating case temperature	Temperature range of package top surface (surface with part marking)
T_S	Storage temperature	Storage temperature range for reliable performance over life of device
$V_{S1,2,3}$	High-side floating supply offset voltage	Maximum voltage range of input offset voltage in reference to COM
$V_{B1,2,3}$	High-side floating supply voltage	Maximum voltage range of input supply voltage
V_{CC}	Low-side and logic supply voltage	Maximum voltage range of input supply voltage
V_{IN}	Input voltage of LIN, HIN	Maximum voltage range in reference to COM and V_{cc}

3 Key parameters: protection features

3.1 Undervoltage Lockout (UVLO)

IRSM5xx and IM240 of product family CIPOS™ Micro provide Undervoltage Lockout (UVLO) on both the $V_{DD(1-3)}$ (logic and low-side circuitry) power supplies, and also $V_{BS(1-3)}$ (high-side circuitry power supplies). UVLO's threshold, labeled as $V_{DDUV+/-}$ (or $V_{BSUV+/-}$) in Figure 14 below, is the voltage level of $V_{DD(1-3)}$ or $V_{BS(1-3)}$ where UVLO is enabled or disabled depending on the increasing or decreasing of voltage level.

Upon power-up, should the $V_{DD(1-3)}$ voltage fail to reach the V_{DDUV+} threshold, the driver will not turn ON. Additionally during operation, if the $V_{DD(1-3)}$ voltage decreases below the V_{DDUV-} threshold during operation, the UVLO circuitry will recognize a fault condition and shut down the high and low-side gate drive outputs.

Upon power-up, should the $V_{B(1-3)}$ voltage fail to reach the V_{BSUV+} threshold, the driver will not turn ON. Additionally during operation, if the $V_{BS(1-3)}$ voltage decreases below the V_{BSUV+} threshold, the UVLO circuitry will recognize a fault condition, and shut down the high-side gate outputs of the driver.

UVLO ensures that the driver will drive external power devices only when the gate supply voltage is sufficient to fully enhance the power devices. Without this feature, the gates of the external power switch could be driven at a low voltage, resulting in the power switch conducting current while the channel impedance is high. This could result in very high conduction losses within the power device, and could lead to power device failure.

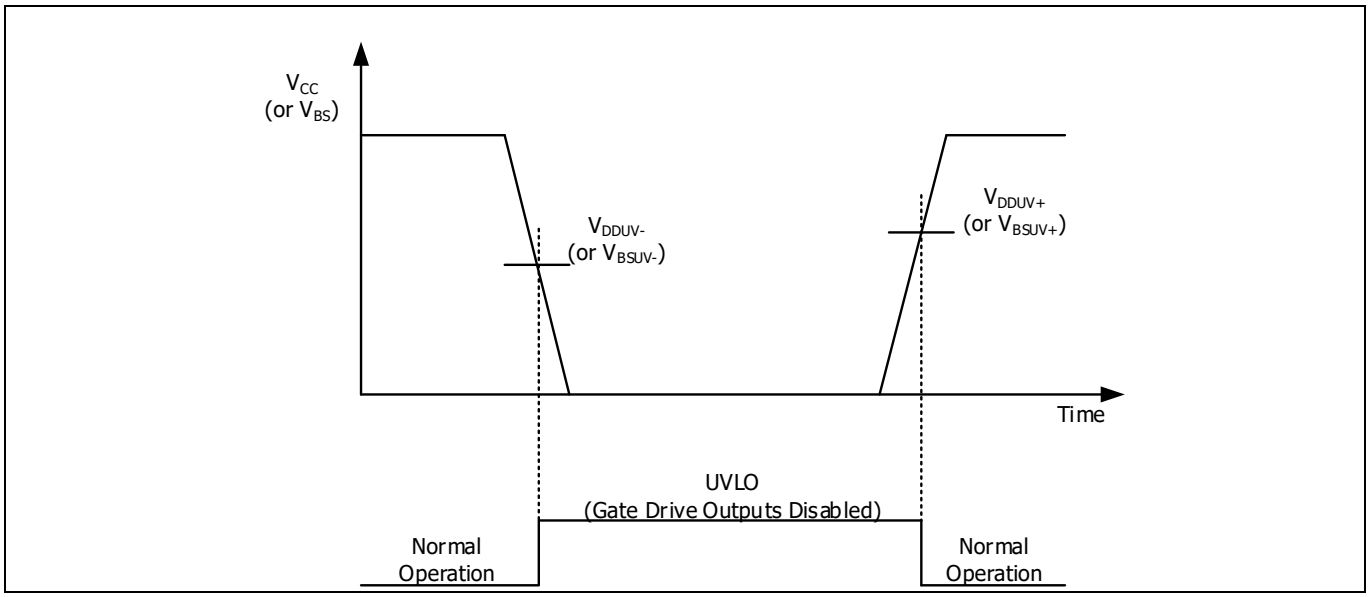


Figure 14 Undervoltage Lockout Function

For correct functionality, $V_{DD(1-3)}$ should be 15 V +/- 10%. Table 6 describes the functionality of the IPM over a range of control power supply voltages. It is recommended to filter the control supply with a low-impedance electrolytic capacitor and a high-frequency decoupling capacitor connected at the V_{DD} pins of the module. Maximum ripple of the supply should be less than ± 1 V/µs to prevent the internal driver from creating incorrect signals due to high-frequency noise of the V_{DD} supply.

The potential at the module's COM terminal is different from that at the $V_{R(1-3)}$ power terminals by the voltage drop across the sensing resistor. All control circuits and power supplies should refer to this point and not to the $V_{R(1-3)}$ terminals. If the circuits are improperly connected, the additional current flowing through the sense resistor might cause improper operation of the short-circuit protection function. In designing the PCB, it is recommended to make the common reference (COM) a ground plane in the layout.

Key parameters: protection features

Table 6 CIPOS™ IPM versus control power supply voltage

Control voltage [V]	Functionality
0-2.5 V	Circuits are not operating, supply is not sufficient to have working active devices
2.5-11.1 V (positive going) 2.5-10.9 V(negative going)	Logic circuits are working, the IC is in UVLO, output off status is kept by active device (expected output resistance is higher, however, than what is specified at 15 V)
11.1-13.5 V	Conduction and switching losses will be higher than under normal conditions. High-side transistors may not operate after $V_{B(1-3)}$ initial charging, as the $V_{B(1-3)}$ voltage level may reach V_{BSUV+}.
13.5-16.5 for $V_{DD(1-3)}$ 12.5-17.5 for $V_{B(1-3)}$	Normal operation
16.5-20 for $V_{DD(1-3)}$ 17.5~20 for $V_{B(1-3)}$	Because the control supply voltage is above the recommended range, the transistor's switching will be faster, which will cause an increase in system noise. Peak short-circuit current might be too large for proper operation of short-circuit protection. (IRSM5xx series max $V_{CC(1-3)}$ is 25 V)
Over 20	Damage of module may occur (Over 25 V for IRSM5xx series)

3.2 Over-temperature protection

Many modules in the CIPOS™ Micro IPM portfolio have a negative-temperature coefficient (NTC) thermistor for temperature sensing. The NTC thermistor is integrated in the module with one terminal of the chip connected to COM, and the other to the VTH, which can be used to monitor the line temperature of the IPM. The resistance of the NTC can be calculated at any temperature as follows:

$$R_{TH} = R_{25} \cdot e^{[B\left(\frac{1}{T_{TH}} - \frac{1}{T_{25}}\right)]}$$

B (B-constant), R_{25} (resistance at 25 °C), and R_{125} (resistance at 125 °C) are given in the specific datasheet where an NTC is implemented. Characterization of the thermistor's resistance depending on temperature is also shown below.

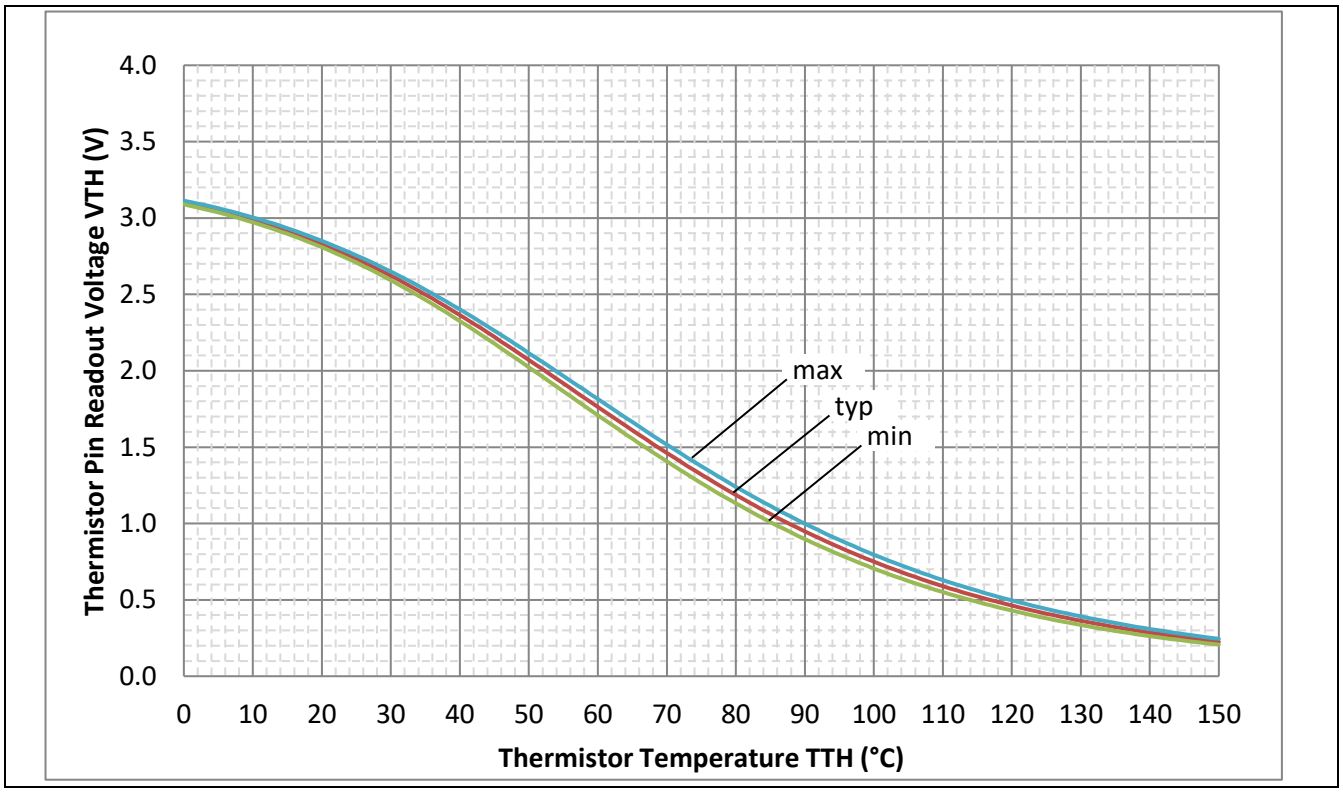


Figure 15 IM240 NTC thermistor resistance vs. thermistor temperature for 3.3 V pull-up resistor of 9.76 kOhm

An external resistor network should be connected to the NTC to provide temperature readings. When pulled up to a rail voltage such as V_{DD} or 3.3 V by a resistor, the VTH pin provides an analog voltage signal corresponding to the temperature of the thermistor. This circuit can be connected to the ADC terminal of the microcontroller to shut down the module if the temperature reading is too high. An example of this circuit is shown below in Figure 16.

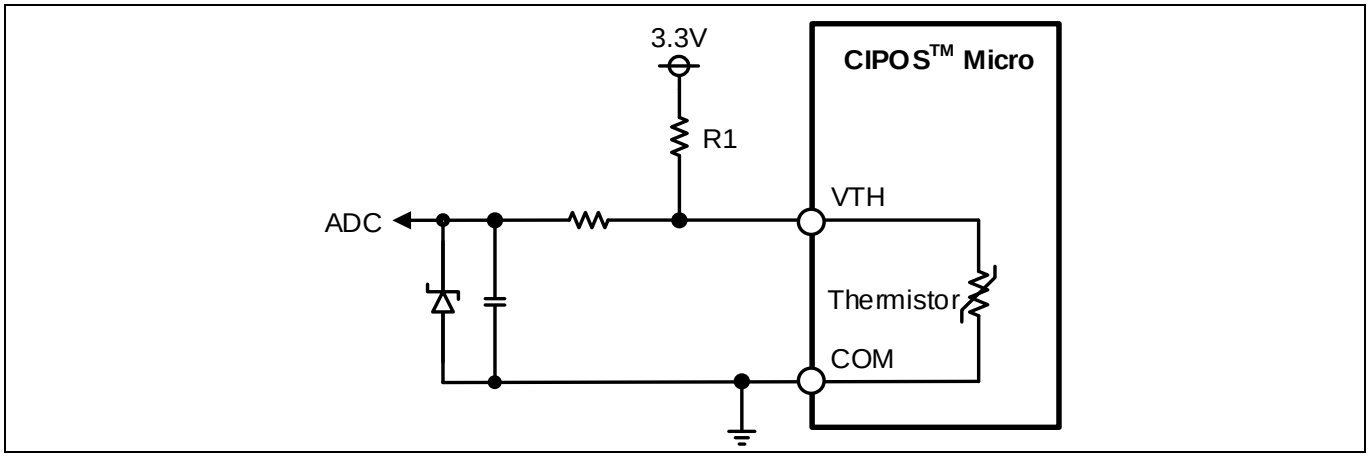


Figure 16 Example of over-temperature protection circuit

Thermistor readout voltage vs. thermistor temperature depends on the external circuit. Characterization of the thermistor based on a specific external circuit can be found in the part's datasheet.

Please note, it remains the responsibility of the system designer to implement protection strategies against overheating that are appropriate for the operating conditions. While the NTC provides temperature reading outputs, it is remote from the power switches, which are the major heat source inside the IPM. Because of this,

the NTC does not necessarily reflect the temperature of all internal components, as there will always be a timing and temperature difference. This needs to be considered when using the NTC to protect the IPM or the system. The actual NTC reading is affected by the thermal system design specificed by the system designer, so some calibration of readings and actual temperature may be required depending on the application.

3.3 Shoot-through protection

CIPOS™ Micro IPMs feature an integrated dead-time protection circuitry. The dead-time feature inserts a time period (minimum dead time) in which both the high- and low-side power switches are held off; this is done to ensure that the power switch being turned off has fully turned off before the second power switch is turned on. This minimum dead time is automatically inserted whenever the external dead time is shorter than DT; external dead times larger than DT are not modified by the module. Minimum dead time can be found in the specific datasheet.

3.4 Short-circuit SOA

CIPOS™ Micro IRSM5XX and IM240 have been designed to handle quick short-circuit situations without damage to the device. The IGBT-based IM240 have a defined short-circuit rating shown in datasheets (Tsc). MOSFETs do not typically have short-circuit ratings, however, in general MOSFET-based IRSM5x5 have better short-circuit handling capabilities than typical IGBT-based modules. There are two types of shorts that can occur to the module. These are a phase-to-phase short and a phase-to-ground short.

Both types were conducted on IRSM5x5 parts to show the short-circuit capabilities of the module. Please note this test was done for reference and was not tested in production.

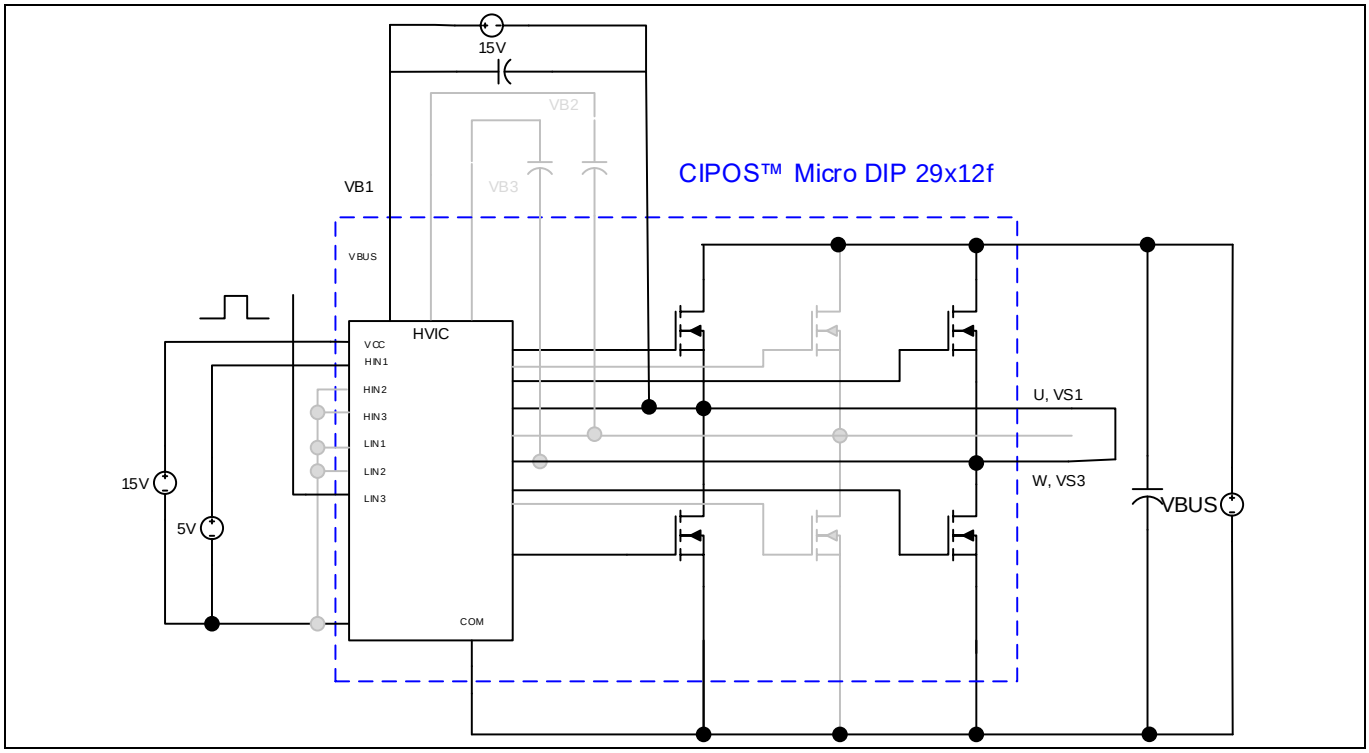


Figure 17 IRSM5x5 phase-to-phase short-circuit test setup

The phase-to-phase short-circuit test setup is shown in Figure 17 above. Phase VS1 and Phase VS3 are shorted together with a 1.02 mm diameter wire and length of 152.4 mm. VS1 high-side was kept on while VS3 low-side was pulsed on with increasing duration. This short-circuit test was done at two conditions: 125 °C with VBUS at 400 V and 150 °C with VBUS at 300 V. For the first condition (T_j=125 °C, VBUS=400 V), five parts were tested and

all parts passed at least 40 µs pulse width. For the second condition (T_j=150 °C, VBUS=300 V), three parts were tested and all passed at least 30 µs pulse width.

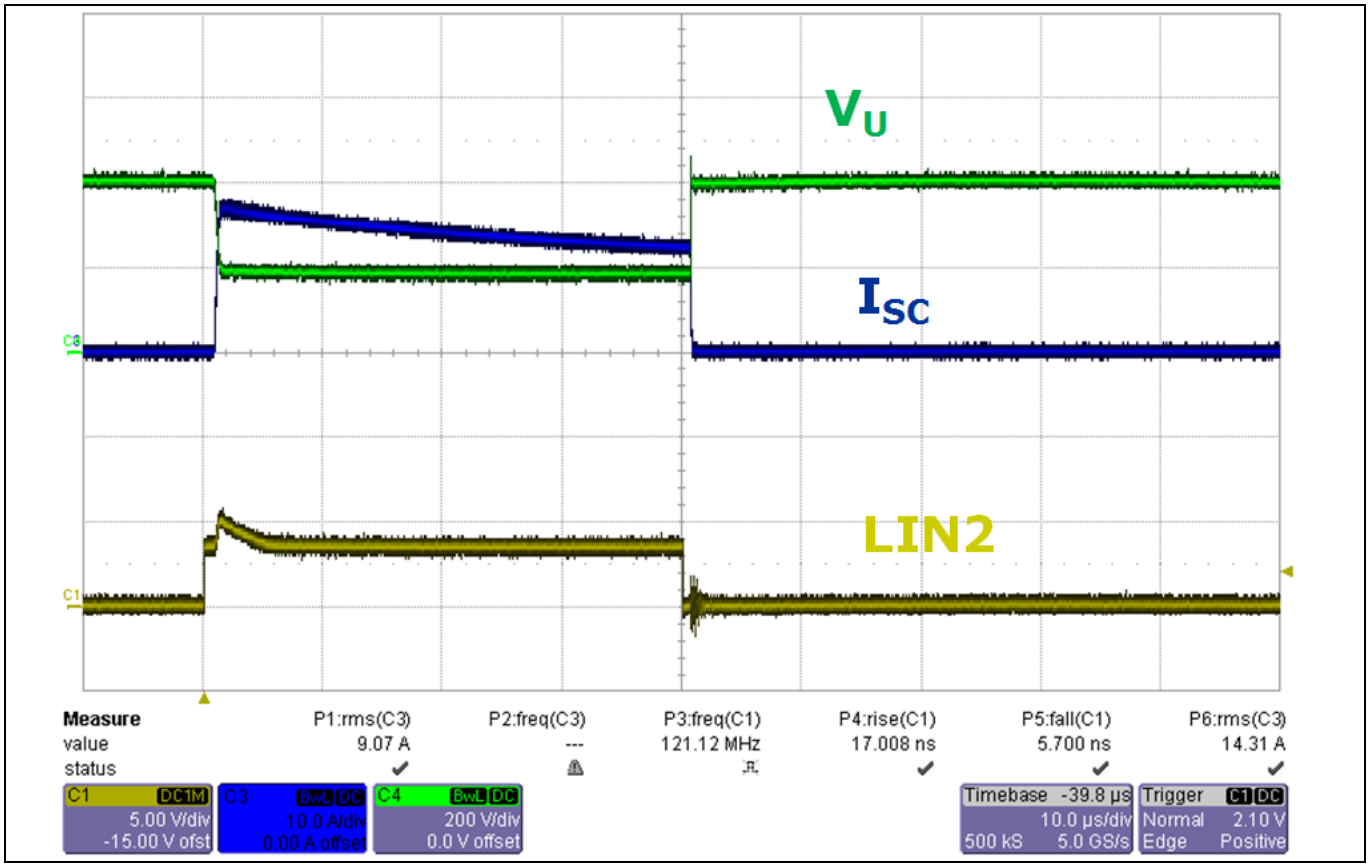


Figure 18 IRSM5x5 phase-to-phase short-circuit test example waveform (T_j=125 °C, VBUS=400 V)

An example waveform of phase-to-phase short-circuit test is shown above. As shown, LIN2 is pulsed on for approximately 40 µs, and the module was able to withstand this short with no damage to the device.

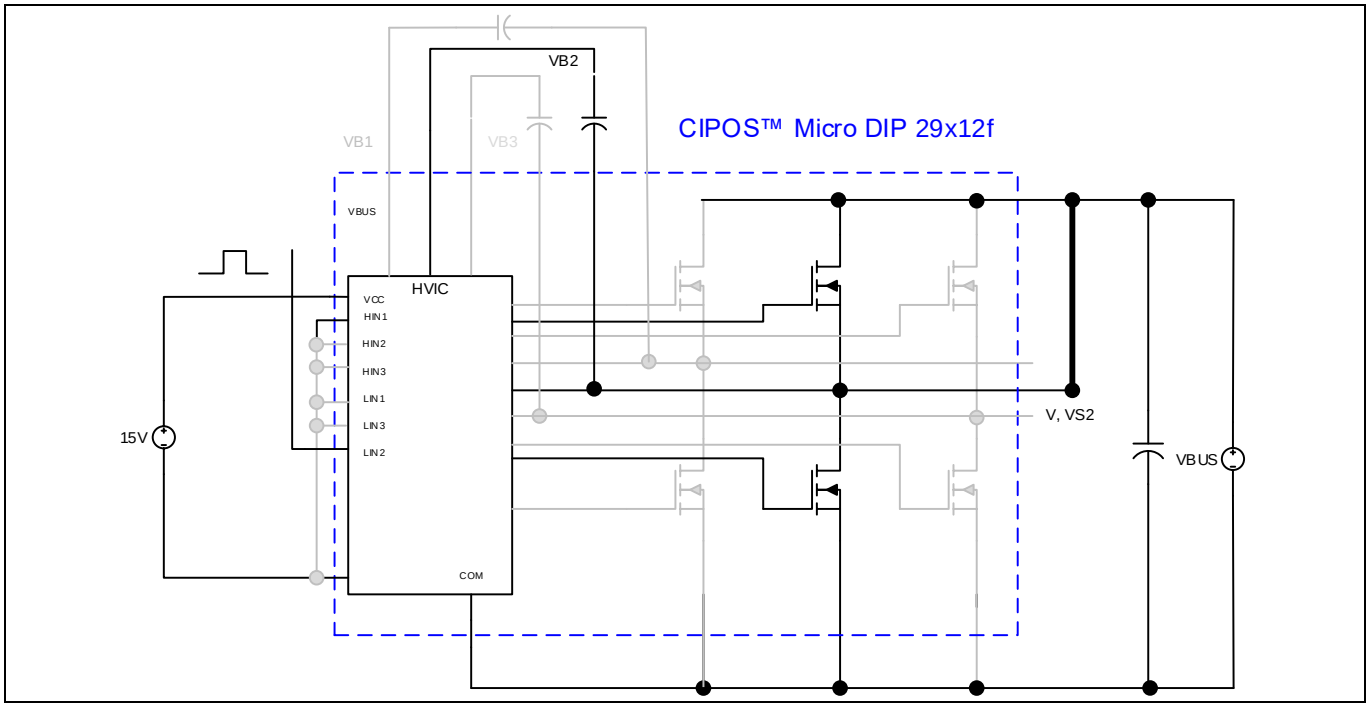


Figure 19 IRSM5x5 phase-to-ground short-circuit test setup

Key parameters: protection features

The phase-to-ground short-circuit test setup is shown above in Figure 19. Phase VS2 and V+ are shorted together with a 1.02 mm diameter wire and length of 152.4 mm.. VS2 low-side was pulsed on with increasing duration. This short-circuit test was done at 150 °C with VBUS at 400 V. Five parts were tested and all parts passed at least 10 µs pulse width.

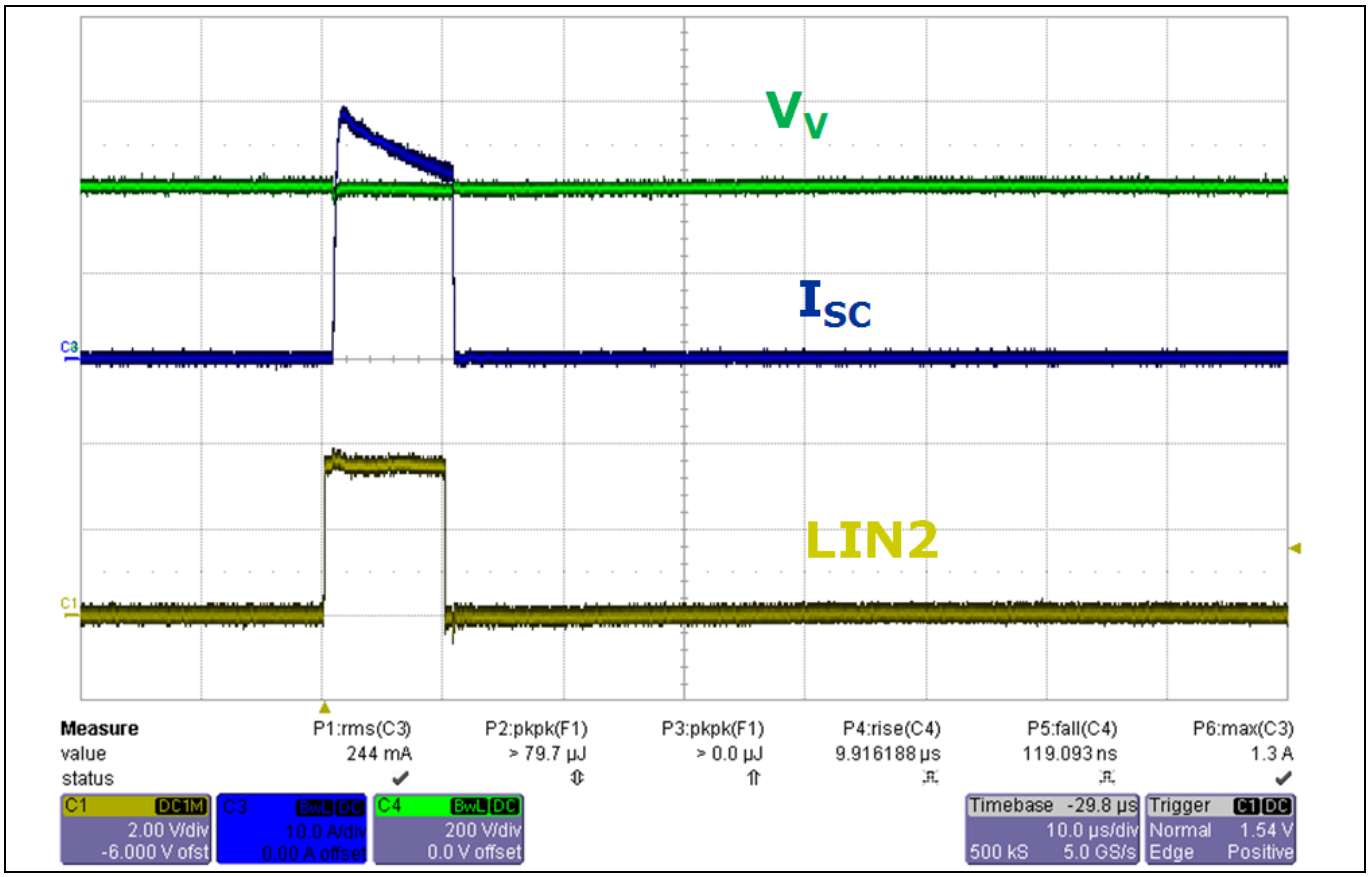


Figure 20 IRSM5x5 phase-to-ground short-circuit test example waveform

An example waveform of phase-to-ground short-circuit test is shown above. As shown, LIN2 is pulsed on for approximately 10 µs, and the module was able to withstand this short with no damage to the device.

4 Circuit interface and layout guide

4.1 Input and output signal connections

The following shows the I/O interface circuit between the microcontroller and the CIPOS™ Micro IRSM5XX and IM240 modules. The input logic is active high with weak 800 kΩ internal pull-down resistors. It is recommended to use external pull-down resistors on each PWM input pin.

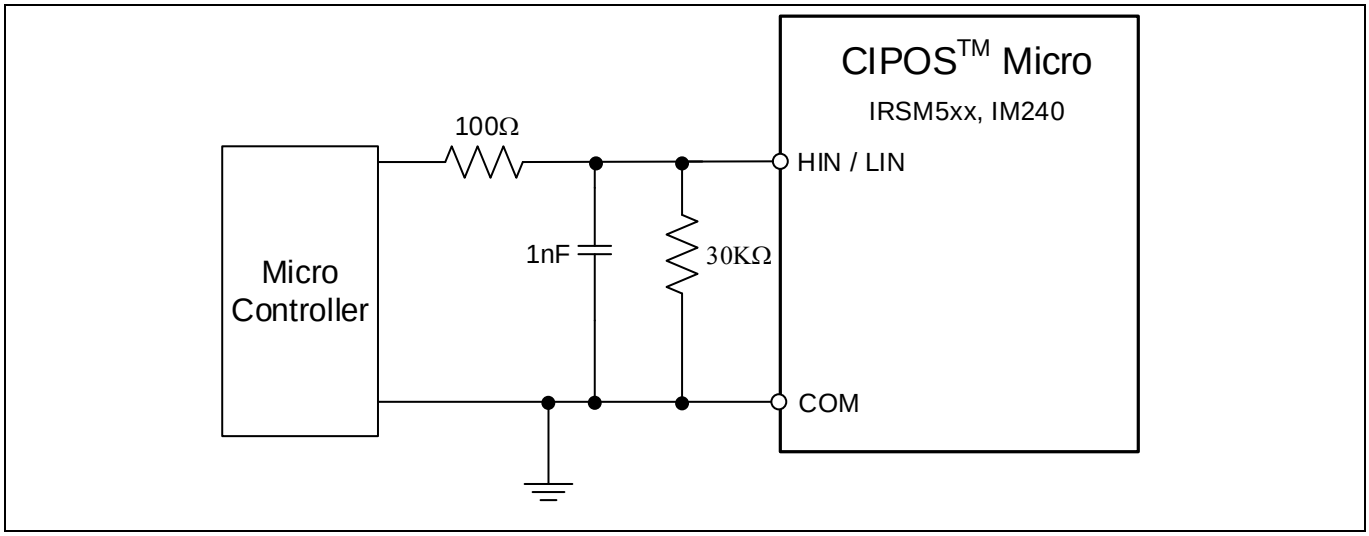


Figure 21 Recommended microcontroller I/O interface circuit

In addition, pull-down resistors are built into each input circuit. This reduces the required external component count. An input Schmitt trigger, noise filter, dead time and shoot-through prevention functions provide beneficial noise rejection to short input pulses. Furthermore, turn ON and turn OFF threshold voltages (shown in specific datasheet) is low enough where a direct connection to 3.3 V-class microcontroller or DSP is possible.

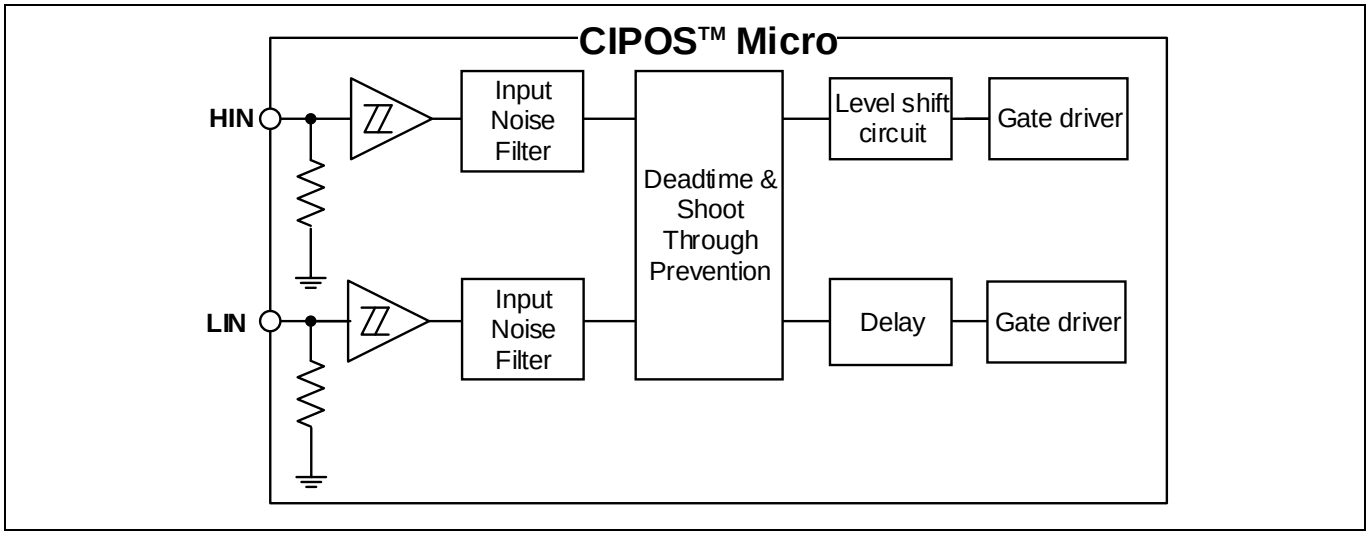


Figure 22 Internal structure of signal input terminals

As shown in Figure 22, the module's input signal integrates a pull-down resistor. Therefore, when using an external filtering resistor between the microcontroller output and IPM input, attention should be given to the signal voltage drop at the module's input terminal to satisfy the turn-on threshold voltage requirement.

4.2 General interface circuit example

Figure 23 shows a typical application diagram with a CIPOS™ Micro IPM. The diagram does not represent an actual recommended schematic, but serves as a guide to the usage of the IPM in an inverterized motor drive.

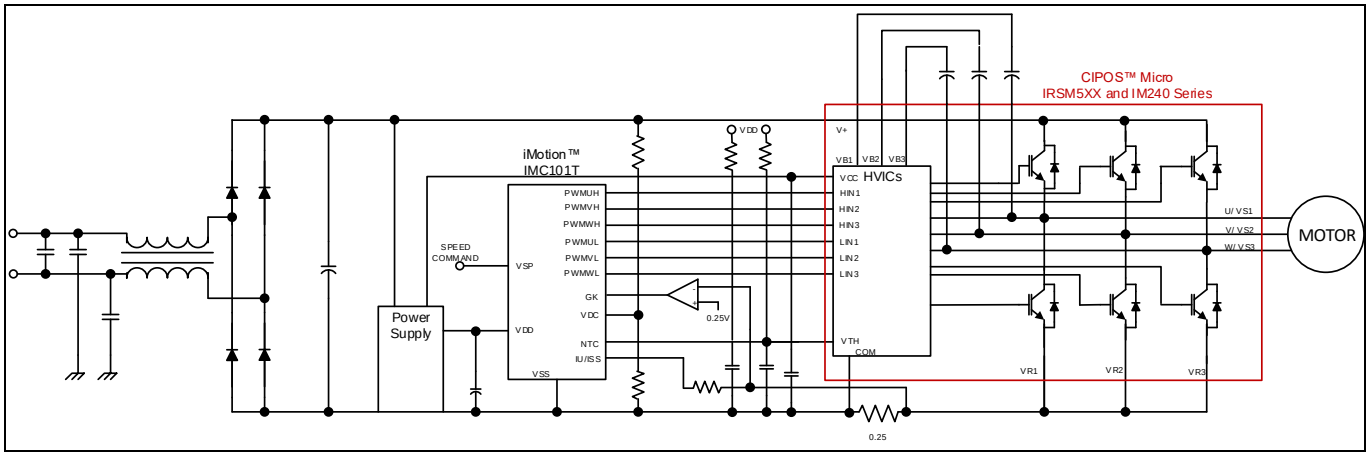


Figure 23 Basic application schematic

The following tips will help make the inverter design functionally robust and reliable:

1. Ceramic capacitors (rated >25 V and 0.1 – 1 µF) should be placed between each V_{DD} pin and COM, as close to the module as possible. These V_{DD} capacitors are required for a stable supply in addition to the larger, typically electrolytic, V_{DD} capacitor (>4.7 µF).
2. Bootstrap capacitors (rated >25 V and sized between 1 and 4.7 µF) should be placed as close to the module as possible. If electrolytic capacitors are used, it is recommended to place high-frequency decoupling ceramic capacitors in parallel to these.
3. As shown in Figure 24 below, snubber capacitors should be installed in the right location so as to suppress surge voltages effectively. Generally, a high-frequency non-inductive capacitor of around 0.1 ~ 0.22 µF is recommended. If the snubber capacitor is installed in the wrong location ‘1’ as shown in Figure 24, the snubber capacitor cannot suppress the surge voltage effectively. If the capacitor is installed in the location ‘2’, the charging and discharging currents generated by wiring inductance and the snubber capacitor will appear on the shunt resistor. This will impact the current-sensing signal and the SC protection level will be a little lower than the calculated design value. The ‘2’ position surge suppression effect is greater than the location ‘1’ or ‘3’. The ‘3’ position is a reasonable compromise with better suppression than in location ‘1’ without impacting the current-sensing signal accuracy. For this reason, the location ‘3’ is generally used.
4. The CIPOS™ Micro input logic is active-high with internal pull-down resistors of ~1 MΩ. It is recommended to have external pull-down resistors on each of the inputs (LIN, HIN) of ~10 kΩ.

4.3 Recommended circuit current of power supply

Control and gate driver power is normally provided by a single 15 V supply that is connected to the module V_{DD} pins. The circuit current of V_{DD} control supply is shown below in Table 7. Please note these values are for reference only and have not been tested in production.

Table 7 Current requirements of V_{DD} Power supply ($V_{DD(1-3)}$ shorted, unit:[mA])

Item		Static (Typ.)	Dynamic (Typ.)	Total (Typ.)
V_{DD} =15 V	F_{SW}=5 kHz	5.15	1.48	6.63
	F_{SW}=15 kHz		3.55	8.70

V_{DD} =20 V	F_{SW}=20 kHz	9.31	5.89	15.17

Finally, the recommended minimum current of the power supply is shown in Table 8 below. This value considers ripple and sufficient margins at given conditions.

Table 8 The recommended minimum circuit current of power supply (unit:[mA])

Item	The circuit current of +15 V control supply
V_{DD} =15 V F_{SW} ≤ 20 kHz	48.68

4.4 Recommended wiring of shunt resistor and snubber capacitor

External current-sensing resistors are applied to detect the overcurrent of phase currents. A long wiring pattern between the shunt resistors and CIPOS™ IPM will cause excessive surges that might damage the IPM's internal IC and current detection components. This may also distort the sensing signals that may lead to loss of control when driving a motor. To decrease the pattern inductance, the wiring between the shunt resistors and IPM should be as short as possible, and any loop should be avoided.

As shown in Figure 24, snubber capacitors should be installed in the right location so as to suppress surge voltages effectively. Generally a high-frequency non-inductive capacitor of around 0.1 ~ 0.22 µF is recommended. If the snubber capacitor is installed in the wrong location ('1' as shown in Figure 24), the snubber capacitor cannot suppress the surge voltage effectively. If the capacitor is installed in location '2', the charging and discharging currents generated by wiring inductance and the snubber capacitor will appear on the shunt resistor. This will impact the current-sensing signal and the SC protection level will be a bit lower than the calculated design value. The '2' position surge suppression effect is greater than in location '1' or '3'. The '3' position is a reasonable compromise with better suppression than location '1' without impacting the current-sensing signal accuracy. For this reason, the location '3' is generally used.

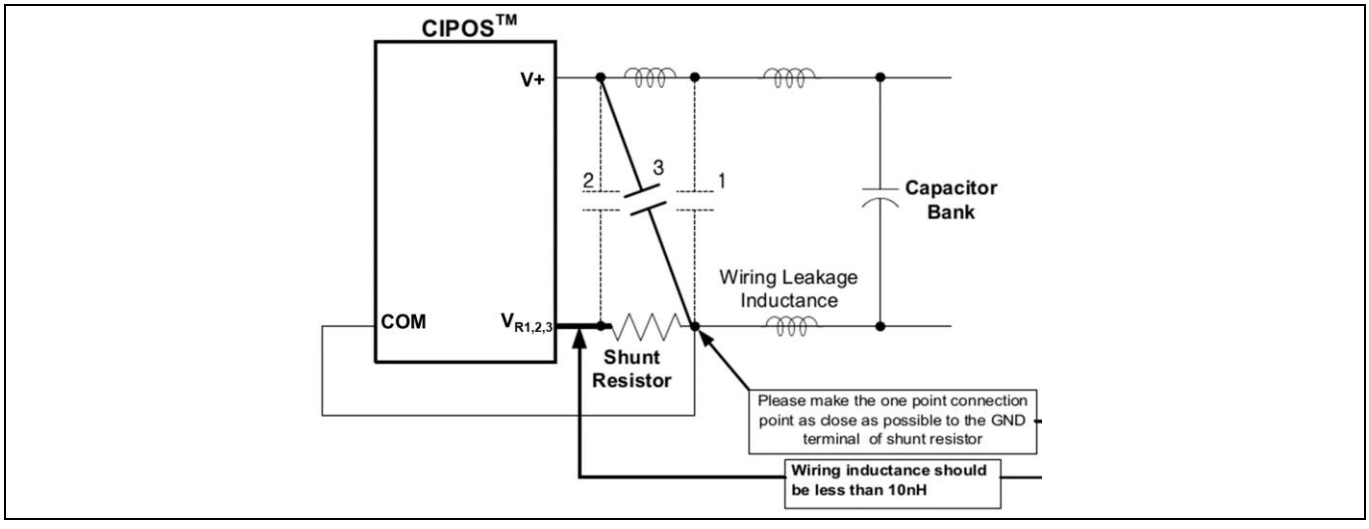


Figure 24 Proper snubber capacitor use

General suggestions:

- PCB traces should be designed as short as possible, and the area of the circuit (power or signal) should be minimized to avoid any noise.

- Make sure there is a good distance between switching lines with high di/dt and dV/dt and the signal lines, as the IPM is very sensitive to electrical noise. Specifically, the trace of each OUT phase carrying significant fast current and voltage transition should be separated from the logic lines and analog sensing circuit.
- Place shunt resistors as close as possible to the low-side pins of the IPM. Parasitic inductance should be as low as possible. Use of a low-inductance SMD resistor is recommended.
- Avoid any ground loops. Only a single path should connect to COM.
- Place each RC filter as close as possible to the IPM pins to increase efficiency.
- Fixed voltage traces such as GND and high-voltage lines can be used to shield the logic and analog lines from electrical noise produced by the switching lines.

4.5 Footprint and PCB design considerations

To help with PCB design, Infineon has made comprehensive PCB design libraries available on its website for CIPOS™ Micro IPM including footprints, symbols and 3D models of the parts. For example, model files for IRSM505-055DA can be accessed from its product page via the Boards and PCB Design Data menus. (https://www.infineon.com/cms/en/product/power/intelligent-power-modules-ipm/irsm505-055da/#!boards)

Libraries are available for EDA tools from Altium, Cadence, Mentor, and Eagle. Figure 25 shows a screenshot of the PCB model for IRSM505-055DA in Altium Designer.

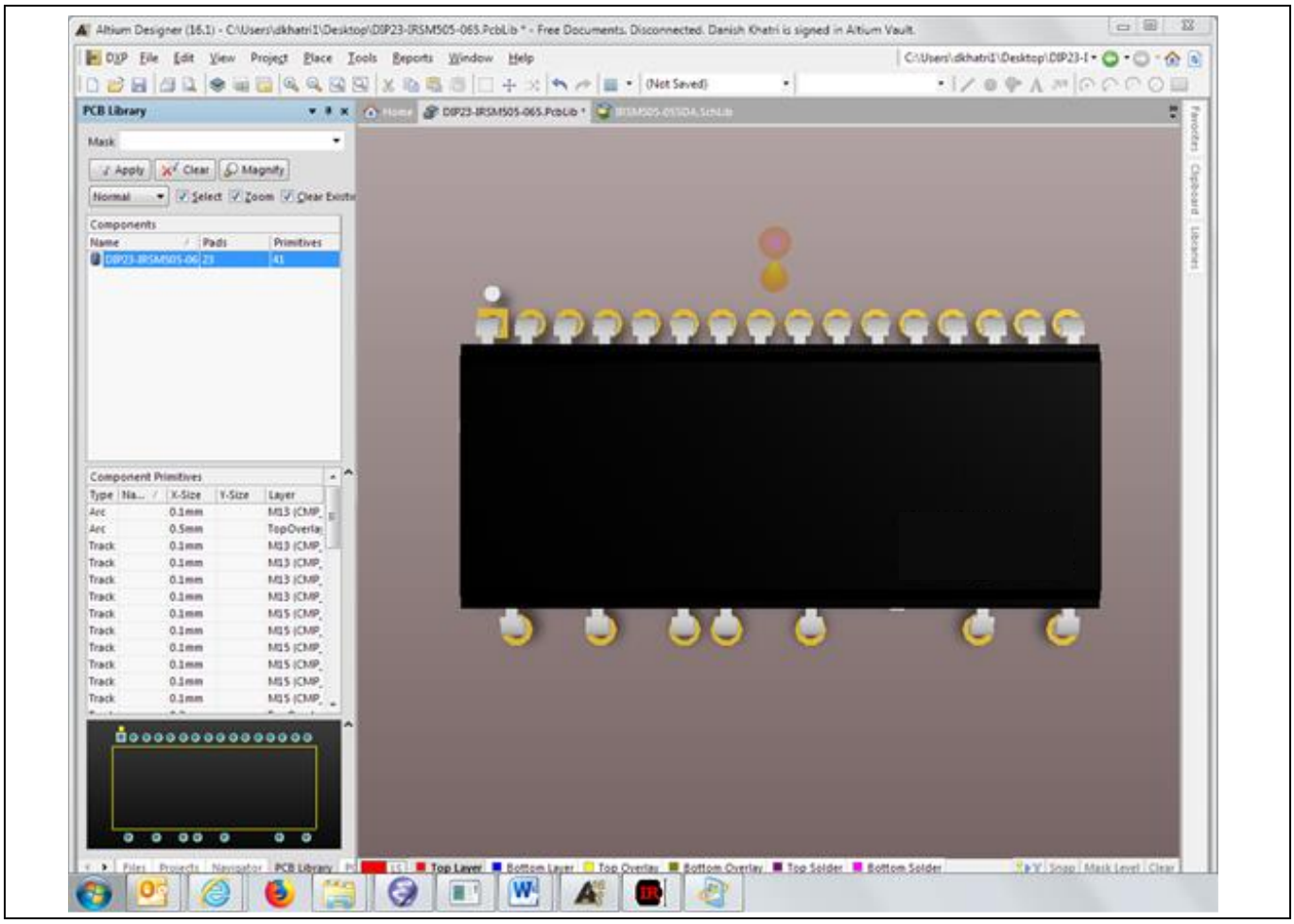


Figure 25 3D model of IRSM505-055DA in the PCB library for Altium Designer

5 Bootstrap circuit

5.1 Bootstrap circuit operation

The V_{BS} voltage, which is the voltage difference between V_B (1-3) and V_S (1-3), supplies voltage to the high-side circuitry of the gate driver, and must be in the range of 12.5~17.5 V. As described in Section 3.1, CIPOS™ Micro IPMs include an under-voltage protection function for V_{BS}.

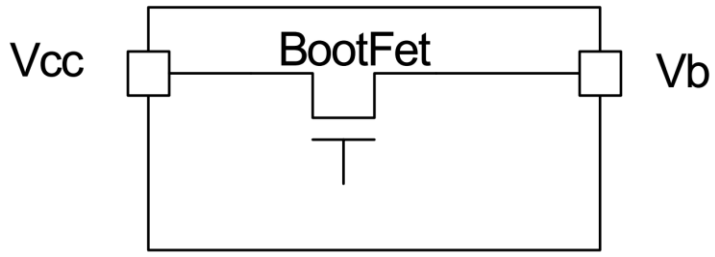


Figure 26 Simplified BootFET internal connection

Internal bootstrap circuitry consists of three high-voltage bootFETs that eliminate the need of any external diodes and resistance. One bootFET is integrated for each high-side output channel, and is connected between V_{DD} supply and its respective floating supply (V_{B1}, V_{B2}, V_{B3}) as shown in Figure 26. The integrated bootFET is turned ON during the time when LO is 'high', and has a limited source current due to R_{BS}. The V_{BS} voltage will be charged each cycle depending on the time of LO, value of the C_{BS} capacitor, the collector-emitter drop of external transistor and the low-side free-wheeling diode drop.

The bootFET of each channel follows the state of low-side output stage, i.e. the bootFET is ON when LO is high, unless the V_B voltage is higher than V_{DD}. In that case, the bootstrap FET is designed to remain off until V_B returns below that threshold. This concept is illustrated in Figure 27.

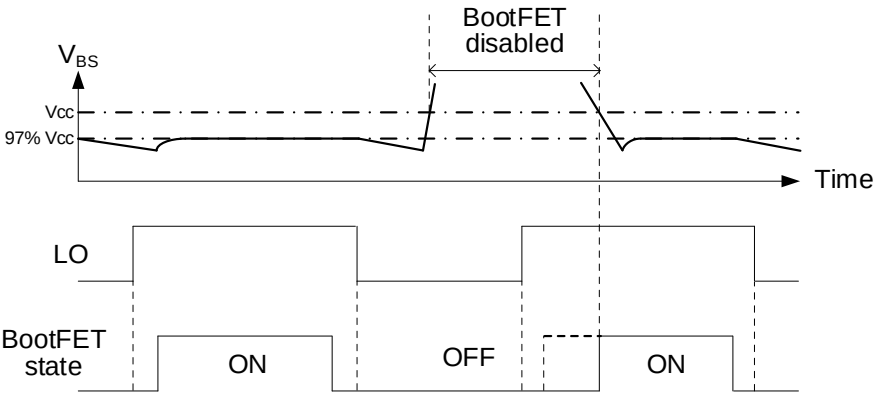


Figure 27 BootFET timing diagram

A bootFET is suitable for most PWM modulation schemes, and can be used either in parallel with an external bootstrap network (diode + resistor) or as replacement of it. The use of the integrated bootstrap as a replacement of the external bootstrap network may, however, have some limitations. An example of this limitation may arise when this functionality is used in non-complementary PWM schemes and at very high PWM duty-cycles. In these cases, superior performance can be achieved by using an external bootstrap diode and resistor in parallel with the internal bootstrap network.

5.2 Initial charging of bootstrap capacitor

To charge the bootstrap capacitor, a sufficient on-time duration of the low-side IGBT is required for initial bootstrap charging. The initial charging time (t_{charge}) can be calculated from the following equation:

$$t_{charge} \geq \frac{C_{BS} \cdot R_{BS}}{\delta} \cdot \ln\left(\frac{V_{DD}}{V_{DD} - V_{BS(\min)} - V_{LS}}\right)$$

Where,

- $V_{BS(min)}$ = The minimum value of the bootstrap capacitor voltage
- V_{LS} = Voltage drop across the low-side IGBT
- δ = Duty ratio of PWM

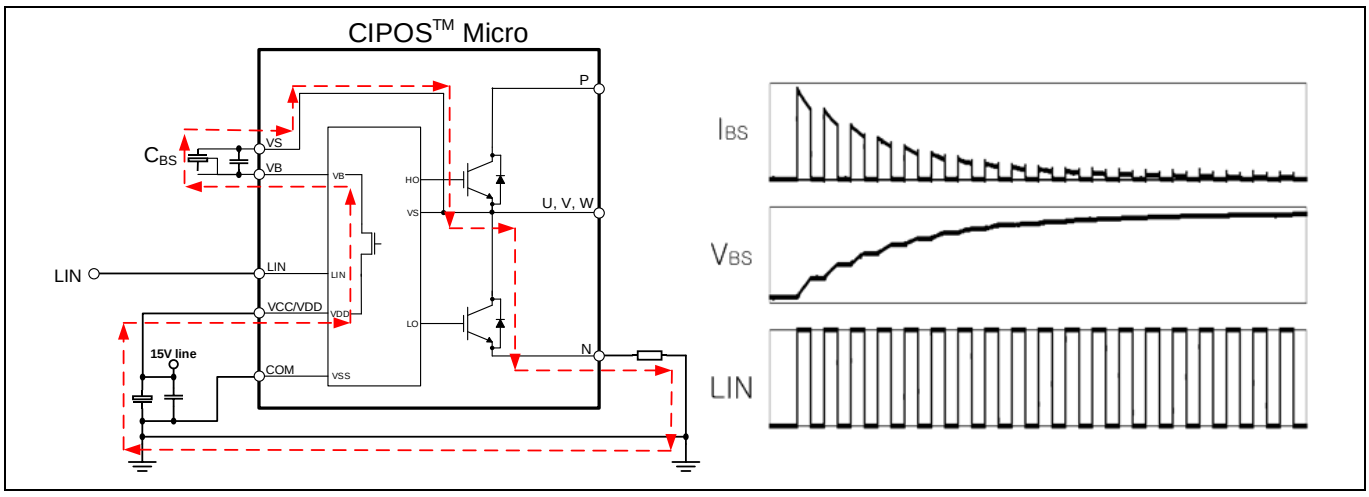


Figure 28 BootFET circuit operation and timing chart of initial FET charging

5.3 Bootstrap capacitor selection

The bootstrap capacitance can be calculated by:

$$C_{BS} = \frac{I_{leak} \cdot \Delta t}{\Delta V_{BS}}$$

Where,

- Δt = maximum ON pulse width of high-side IGBT
- ΔV_{BS} = the allowable discharge voltage of the C_{BS}
- I_{leak}= maximum discharge current of the C_{BS} mainly via the following mechanisms:
  - Gate charge for turning the high-side IGBT on
  - Quiescent current to the high-side circuit in the IC
  - Level-shift charge required by level-shifters in the IC
  - Leakage current in the bootstrap diode
  - C_{BS} capacitor leakage current (ignored for non-electrolytic capacitors)
  - Bootstrap-diode reverse-recovery charge

Bootstrap circuit

In practice a leakage current of 1 mA is recommended as a calculation basis. By taking in consideration dispersion and reliability, the capacitance is generally selected to be 2~3 times higher than the calculated one. The C_{BS} is only charged when the high-side IGBT is off and the VS voltage is pulled down to ground. Therefore, the on-time of the low-side IGBT must be sufficient to ensure that the charge drawn from the C_{BS} capacitor can be fully replenished. Hence, inherently there is a minimum on-time of the low-side IGBT (or off-time of the high-side IGBT).

The bootstrap capacitor should always be placed as close to the module pins as possible. At least one low ESR capacitor should be used to provide good local de-coupling. For example, a separate ceramic capacitor close to the IPM is essential if an electrolytic capacitor is used for the bootstrap capacitor. If the bootstrap capacitor is either a ceramic or tantalum type, it should be adequate for local decoupling.

5.4 Charging/ discharging of bootstrap capacitor during operation

The bootstrap capacitor C_{BS} charges through the bootFET from the V_{DD} supply when the high-side IGBT is off, and the VS voltage is pulled down to ground. It discharges when the high-side IGBT or diode are on.

5.4.1 Example 1: Selection of initial charging time

An example calculation of the minimum value of the initial charging time:

Conditions:

- C_{BS}=4. 7 µF, R_{BS} = 200 Ω, Duty Ratio (δ)= 0.5, V_{DD} = 15 V
- $V_{BS\,(min)}$ = 12.5 V
- V_{LS} = 0.1 V
- $t_{charge} \geq 4.7\mu F \times 200\Omega \times \frac{1}{0.5} \times \ln(\frac{15V}{15V-12.5V-0.1V})$

In order to ensure safety, it is recommended that the charging time must be at least three times longer than the calculated value.

5.4.2 Example 2: Minimum value of bootstrap capacitor

Based on the conditions given above, a minimum value of bootstrap capacitor can be chosen based on switching frequency.

Conditions:

- ΔV_{BS}=0.1 V, I_{leak}= 1 mA

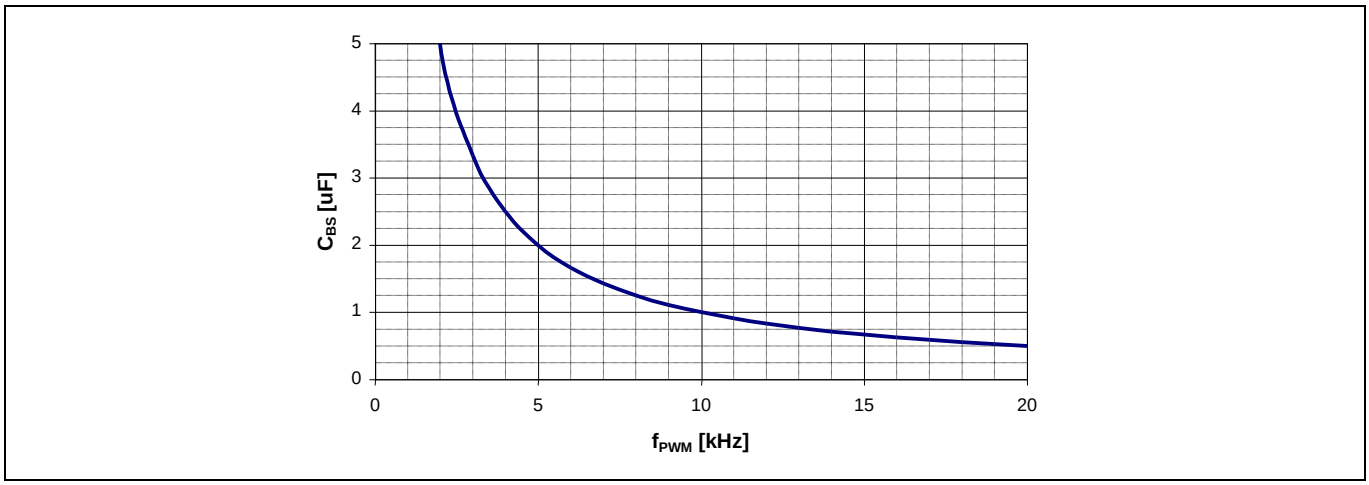


Figure 29 Bootstrap capacitance as a function of switching frequency

Bootstrap circuit

Figure 29 shows the curve for a continuous sinusoidal modulation if the voltage ripple (ΔV_{BS}) is 0.1 V. The recommended bootstrap capacitance for a continuous sinusoidal modulation method is therefore in the range of up to 4.7 µF for most switching frequencies. In other PWM methods, like a discontinuous sinusoidal modulation, the t_{charge} must be set to the longest low-side IGBT OFF period.

Note that this result is only an example. It is recommended that the system design considers the actual control pattern and lifetime of the used components.

6 Thermal system design

The thermal design of a system is a key issue included in electronic systems such as drives. In order to avoid overheating and /or to increase the reliability, two design criteria are of importance:

- Low power losses
- Low thermal resistance from junction to ambient

The first criterion is already fulfilled when choosing CIPOS™ Micro as an intelligent power module for the application. A good thermal design either allows the user to maximize the power or to increase the reliability of the system (by reducing the maximum temperature). This application note will give a short introduction to power losses and heatsinks, helping to understand the mode of operation, and to find the right heatsink for a specific application if needed.

For the thermal design, the following is required:

- The maximum power losses $P_{sw,i}$ of each power switch
- The maximum junction temperature $T_{J,\ max}$ of the power semiconductors
- The maximum allowable ambient temperature $T_{A,\ max}$
- The junction-to-ambient thermal resistance impedance $Z_{th,\ J\text{-}A}$
    - For steady-state considerations, the static thermal resistance $R_{th,J\text{-}A}$ is sufficient. This thermal resistance comprises the junction-to-case thermal resistance $Rth_{,J\text{-}C}$ as provided in datasheets, the case-to-heatsink thermal resistance $R_{th,C\text{-}HS}$ accounting for the heat flow through the thermal interface material between heatsink and the power module, and the heatsink-to-ambient thermal resistance $R_{th,HS\text{-}A}$. Each thermal resistance can be extended to its corresponding thermal impedance by adding the thermal capacitances.

6.1 Online motor-drive-simulation tool

CIPOS™ IPM Motor Drive Simulation Tool, which is available on Infineon's website (www.infineon.com/plex-ipm), offers help to users for part selection and design decisions. This tool allows the user to simulate and compare IPM parts using three-phase motor conditions to determine which module best suits their needs. The tool shows the expected temperature of the selected IPM, the approximate losses of the system, and also generates output voltage, current, junction temperature and loss waveforms. It is recommended to test parts with planned motor conditions in the simulation tool prior to physical design. A user manual and video tutorial to aid in tool use is provided on the webpage.

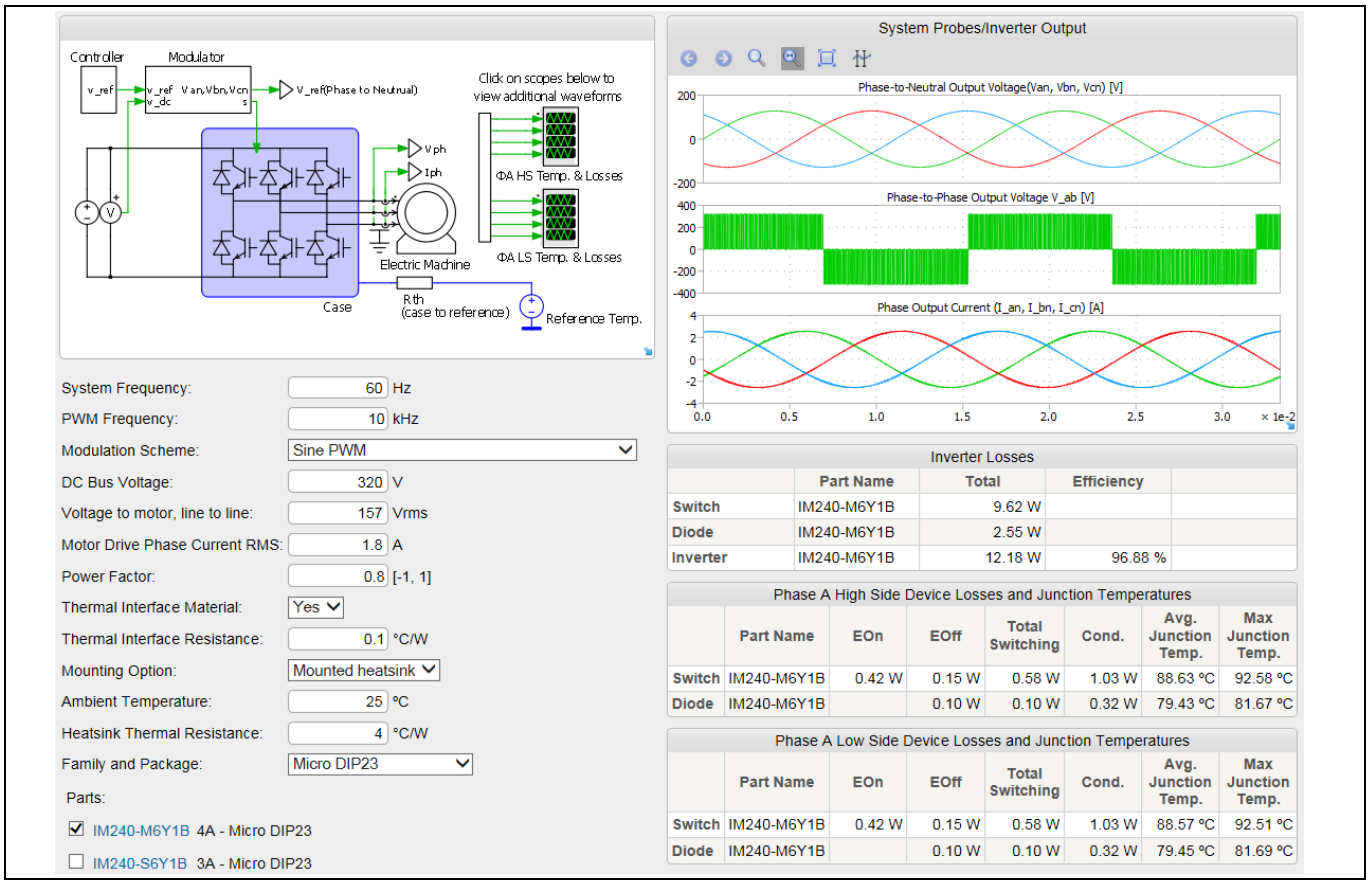


Figure 30 CIPOS™ IPM motor-drive-simulation tool example for IM240-M6Y1B

This tool provides a breakdown of losses, and can provide a glimpse of the tradeoff between switching and conduction losses in the module for given conditions and design. Alternatively, these losses can be calculated based on the formulas discussed in the next sections.

6.2 Power loss

Total power losses in the module are composed of conduction and switching losses in the power switch. The loss during the turn-off steady state can be ignored, asit is very small amount, and has little effect on increasing the temperature in the device.

Based on a PWM-inverter system for motor control applications, detailed equations are shown to calculate both conduction and switching losses of the module for a 3-phase continuous sinusoidal PWM. For other cases, like 3-phase discontinuous PWMs, please see Reference [4].

6.2.1 Conduction loss

Conduction losses depend on the DC electrical characteristics of the device, i.e., saturation voltage. Therefore, it is a function of the conduction current and the device's junction temperature.

6.2.1.1 IGBT, RC-IGBT and diode

The typical characteristics of forward drop voltage are approximated by the following linear equation for the IGBT and the diode, respectively:

$$V_{IGBT} = V_I + R_I \cdot i$$

$$V_{DIODE} = V_D + R_D \cdot i$$

Where,

- V_I=Threshold voltage of IGBT
- V_D= Threshold voltage of monolithic body diode
- R_I= On-state slope resistance of IGBT
- R_D=On-state slope resistance of monolithic body diode

Assuming that the switching frequency is high, the output current of the PWM inverter can be assumed to be sinusoidal, and can be calculated by:

$$i = I_{Peak} \cdot \cos(\theta - \varphi)$$

Where,

- φ = phase angle difference between output voltage and current.

Using the equations above, the conduction loss of one IGBT and its monolithic body diode can be obtained as follows:

$$P_{con.I} = \frac{1}{2\pi}\int_0^{\pi} \delta(V_{IGBT} \cdot i)d\theta = \frac{I_{peak}}{2\pi}V_I + \frac{I_{peak}}{8}V_I MI\cos\varphi + \frac{{I_{peak}}^2}{8}R_I + \frac{{I_{peak}}^2}{3\pi}R_I MI\cos\varphi$$

$$P_{con.D} = \frac{1}{2\pi}\int_0^{\pi} (1-\delta)(V_{DIODE} \cdot i)d\theta = \frac{I_{peak}}{2\pi}V_D - \frac{I_{peak}}{8}V_D MI\cos\varphi + \frac{{I_{peak}}^2}{8}R_D - \frac{{I_{peak}}^2}{3\pi}R_D MI\cos\varphi$$

$$P_{con} = P_{con.I} + P_{con.D}$$

Where,

- δ= duty cycle given in PWM method.

This can be calculated by:

$$\delta = \frac{1 + MI\cos(\theta)}{2}$$

Where,

- MI = PWM modulation index (MI, defined as the peak phase voltage divided by half of DC link voltage).

It should be noted that the total inverter conduction losses are six times that of P_{con}.

6.2.1.2 MOSFET

The typical characteristics of MOSFET's drain-to-source ON resistance and body-diode forward voltage are approximated by the following linear equations:

$$V_{DS} = V_M + R_M \cdot i$$

$$V_{SD} = V_{MD} + R_{MD} \cdot i$$

Where,

- V_M=Threshold voltage of MOSFET
- V_{MD}= Threshold voltage of MOSFET body diode
- R_M= On-state slope resistance of MOSFET
- R_{MD}=On-state slope resistance of MOSFET body diode

Thermal system design

Assuming that the switching frequency is high, the output current of the PWM inverter can be assumed to be sinusoidal, and can be calculated by:

$$i = I_{Peak} \cdot \cos(\theta - \varphi)$$

Where,

- φ = phase angle difference between output voltage and current.

Using the equations above, the conduction loss of one IGBT and its monolithic body diode can be obtained as follows:

$$P_{con.M} = \frac{1}{2\pi}\int_0^{\pi} \delta(V_{MOSFET} \cdot i)d\theta = \frac{I_{peak}}{2\pi}V_M + \frac{I_{peak}}{8}V_M MI\cos\varphi + \frac{{I_{peak}}^2}{8}R_M + \frac{{I_{peak}}^2}{3\pi}R_M MI\cos\varphi$$

$$P_{con.MD} = \frac{1}{2\pi}\int_0^{\pi} (1-\delta)(V_{MDIODE} \cdot i)d\theta = \frac{I_{peak}}{2\pi}V_{MD} - \frac{I_{peak}}{8}V_{MD} MI\cos\varphi + \frac{{I_{peak}}^2}{8}R_{MD} - \frac{{I_{peak}}^2}{3\pi}R_{MD} MI\cos\varphi$$

$$P_{con} = P_{con.M} + P_{con.MD}$$

Where,

- δ= duty cycle given in PWM method.

This can be calculated by:

$$\delta = \frac{1 + MI\cos(\theta)}{2}$$

Where,

- MI = PWM modulation index (MI, defined as the peak phase voltage divided by half of DC link voltage).

It should be noted that the total inverter conduction losses are six times of P_{con}.

6.2.2 Switching loss

Switching losses are determined by the dynamic characteristics like turn-on/off time and overvoltage/current. Hence, in order to obtain the accurate switching loss, the DC-link voltage of the system, the applied switching frequency and the power circuit layout, in addition to the current and temperature should be considered.

Different devices have different switching characteristics, and will vary according to the handled voltage/current and the operating temperature/frequency. However, the turn-on/off loss energy (Joule) can be measured by multiplying the current and voltage then integrating over time under a given circumstance.

6.2.2.1 IGBT, RC-IGBT and diode

Therefore the linear dependency of the switching energy loss on the switched-current is expressed during one switching period as follows:

$$E_I = E_{I.on} + E_{I.off}$$

$$E_D = E_{D.on} + E_{D.off}$$

Where,

- E_I = switching loss energy of the IGBT
- E_D= switching loss energy of monolithic diode

E_I and E_D can be considered a constant.

Thermal system design

As mentioned in conduction loss explanation, the output current can be considered a sinusoidal waveform, and the switching loss occurs every PWM period for the continuous PWM schemes. Therefore depending on the switching frequency, f_{sw}, the switching loss of one device is the following equation:

$$P_{sw} = \frac{1}{2\pi}\int_0^{\pi}(E_I + E_D)\cdot i \cdot f_{sw} d\varphi = \frac{(E_I + E_D)\cdot f_{sw}\cdot I_{peak}}{\pi}$$

These constants should be derived by experimental measurement. From the above equation, it should be noted that the switching losses are a linear function of current, and directly proportional to switching frequency.

6.2.2.2 MOSFET

Therefore the linear dependency of the switching energy loss on the switched current is expressed during one switching period as follows:

$$E_M = E_{M.on} + E_{M.off}$$

$$E_{MD} = E_{MD.on} + E_{MD.off}$$

Where,

- E_M = switching loss energy of the MOSFET
- E_{MD}= switching loss energy of MOSFET body diode

E_M and E_{MD} can be considered a constant.

As mentioned in the conduction loss explanation, the output current can be considered a sinusoidal waveform, and the switching loss occurs every PWM period for the continuous PWM schemes. Therefore depending on the switching frequency f_{sw}, the switching loss of one device has the following equation:

$$P_{sw} = \frac{1}{2\pi}\int_0^{\pi}(E_M + E_{MD})\cdot i \cdot f_{sw} d\varphi = \frac{(E_M + E_{MD})\cdot f_{sw}\cdot I_{peak}}{\pi}$$

These constants should be derived by experimental measurement. From the above equation, it should be noted that the switching losses are a linear function of current, and are directly proportional to the switching frequency.

6.3 Thermal impedance

During operation, power losses generate heat, which elevates the temperature in the semiconductor junctions. High junction temperatures limit the performance and the lifetime of the module. Thus, the thermal design of the package is a very important factor in the module development stage. Thermal design is also important in the development of the motor drive system. The heat generated from the module must be properly transferred to the environment using an adequate cooling system.

Thermal impedance qualifies the capability of a given thermal path to transfer heat in the steady state.

$$Z_{TH}(t) = \frac{\Delta T(t)}{P}$$

Thermal impedance is typically represented by an RC equivalent circuit as shown in Figure 31.

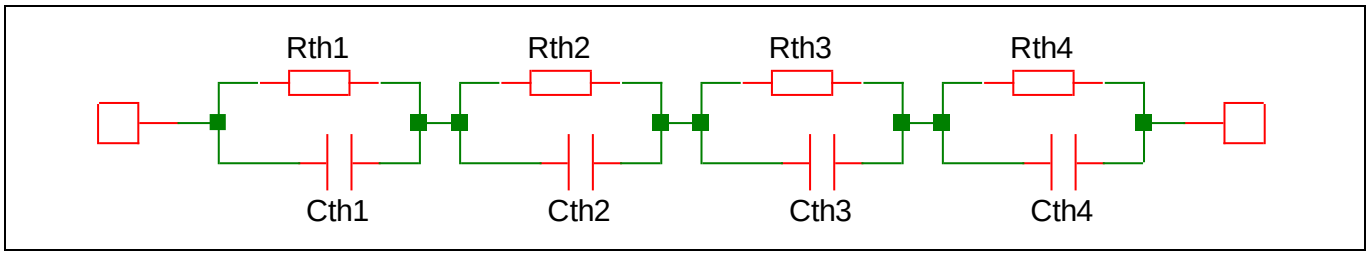


Figure 31 Thermal impedance RC equivalent circuit (Foster model)

Under sinusoidal modulation, the power loss has to be calculated in each switching cycle, as the device current changes within each half modulation cycle, as illustrated in Figure 32. The upper portion is the high-side switch current which is used to calculate E_{ON} and E_{OFF} of the switch. The lower portion in Figure 32 is the low-side diode current for E_{RR}.

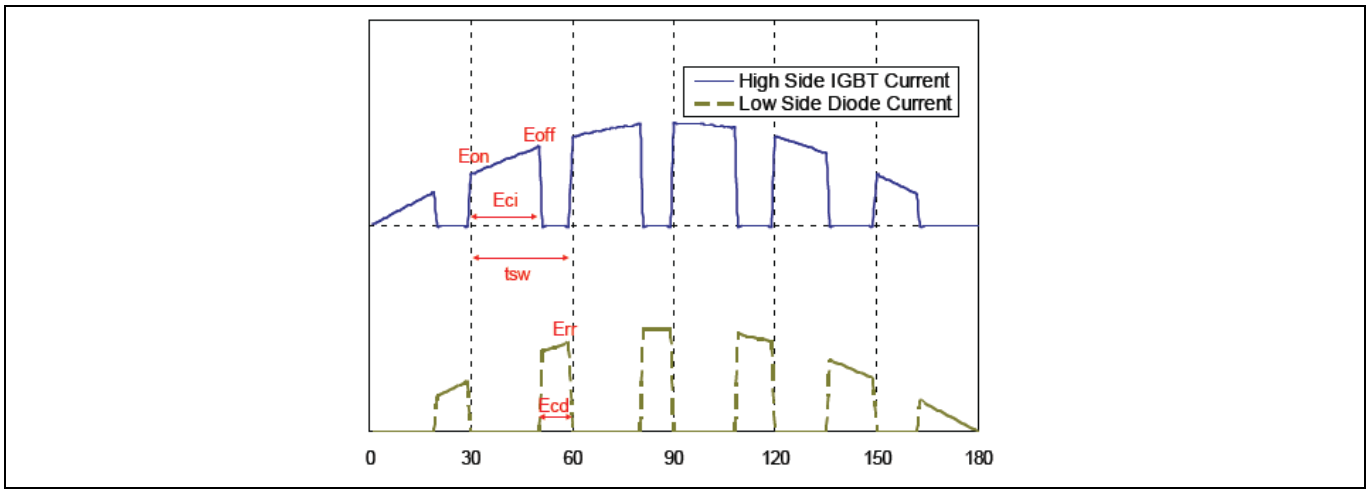


Figure 32 Loss calculation of sinusoidal modulation

Because the loss is not constant over time, its shape depends on current waveforms and device parameters. Figure 33 illustrates the power loss of a single switch in a typical case.



Figure 33 Junction-temperature calculations under sinusoidal modulation

6.4 Heatsink methods

While CIPOS™ Micro IRSM5xx and IM240 product portfolios are designed for non-heatsink use, there are methods that can be done to integrate a heatsink for higher power capability. Mass market heatsink assemblies designed for TO-220 and TO-247 packages can be used with CIPOS™ Micro IRSM5xx and IM240 which result in a very low-cost heatsinking solution. This section not only describes these methods, but also goes into detail about heatsink selection, characteristics, and mounting.

Some well-known methods to heatsink the module include:

- PCB as heatsink
- Screwed heatsink to PCB
- Sheet-metal heatsink to PCB
- Push-pinned heatsink to PCB
- TO-220 heatsink coupled with clip to PCB

6.4.1 PCB as heatsink

When using the PCB as a heatsink for the IPM, it is important to consider how the heat will flow across the PCB. For reference, thermal simulations of the CIPOS™ Micro showed that approximately 78.5% of the heat from the module travels through the PCB when no external heatsink is used. Because of this, the copper trace layouts of the PCB should be optimized to improve the junction-to-ambient thermal resistance $R_{th, J\text{-}A}$. Optimization of the PCB will of course vary per design, but this discussion should provide some insight into the topic.

Two thermal simulation results are shown below for CIPOS ™ Micro IPMs. Both simulations used the same conditions except for the size of the copper trace on the PCB to the signal pins of the module (pins 1-15). For Figure 34 (simulation results 1), a signal pin copper trace area of 44.8 mm^2 was used, and for Figure 35 (simulation results 2) a copper track of 68.8 mm^2 was used.

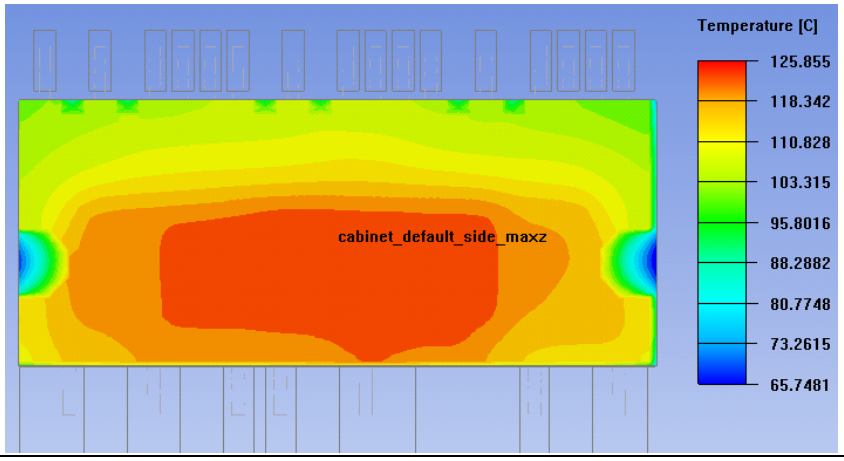


Figure 34 CIPOS™ Micro SOP thermal simulation results 1, signal PIN Cu trace area = 44.8 mm^2

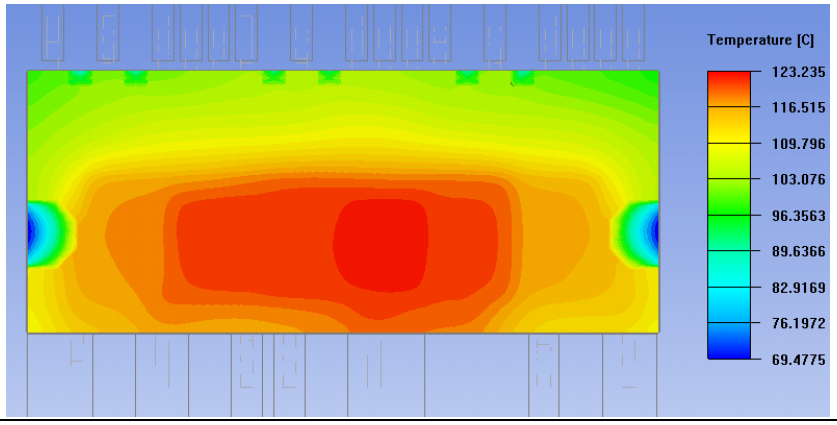


Figure 35 CIPOS™ Micro SOP thermal simulation results 2, signal PIN Cu track area = 68.8 mm^2

As shown in the figures above, increasing the surface area of the track lowered the maximum temperature of the module from 125.86 °C in simulation 1 to 123.24 °C in simulation 2, and also decreased the overall Rth_{J-A} from 42.25 °C/W to 41.15 °C/W. While this simulation only takes into consideration the area of the track, it is still important to consider the overall PCB design to guarantee optimal heat dissipation.

Since PCB substrate normally has very poor thermal conductivity, all copper features need to be considered to improve the thermal path of the IPM to ambient. Common copper features of a PCB include the amount and size of throughholes (vias), additional copper areas for heat spreading in the inner layers of the PCB, the thickness of these layers, and the design of the solder mask opening for the footprint. In general, increasing the amount and size of copper areas will increase the thermal dissipation of the modules.

When using surface-mount IPMs, the footprint design should also be optimized for thermal conductivitity. There are two main catagories of footprint design: non-solder-mask defined and solder-mask defined footprints.

A non-solder-mask pad is a metal pad that is surrounded by a solder-mask clearance. This clearance is specified by the designer to ensure that the mask does not overlap the solder pad. A solder-mask defined footprint is when the metal pad is larger than the solder-mask opening as shown in Figure 36. This allows for connection of the footprint to large copper areas of the PCB, and the option to increase the amount of thermal vias near or underneath the IPM, allowing for improved heat transfer. While this may be true, the solder-mask walls tend to prevent some air and gasses from escaping the solder joint during the reflow process.

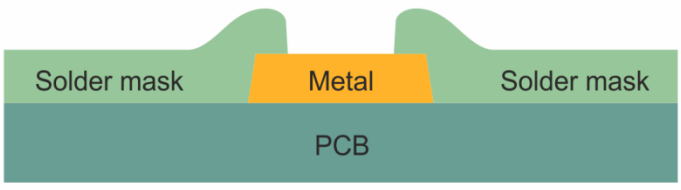


Figure 36 Solder-mask-defined pad

Even though the solder-mask-defined pad may have a small disadvantage compared to non-solder-mask pads during the reflow process, it is the design of choice when optimizing heat spreading of the PCB and using the PCB as a heatsink.

6.4.2 Screwed heatsink to PCB

While mounting the heatsink directly to the PCB is possible, issues may arise if it not mounted properly. Not only does the heatsink need to have proper contact to the module, but it also cannot be screwed on too tightly where the PCB may flex from the pressure. With proper torque, this issue can be avoided.

The PCB material, thickness and size must be considered along with the screw length and size for proper mounting. For example, Figure 37 shows a diagram of a heatsink mounted to a PCB for CIPOS™ Micro IPM with a M3 screw and a PCB thickness of 1.55 mm. Varying levels of torque were applied to the screws to measure the effects on performance and visual issues, i.e., cracks in solder, package, etc. Torque T_i was tested in a range from 0.1 Nm to 10 Nm.

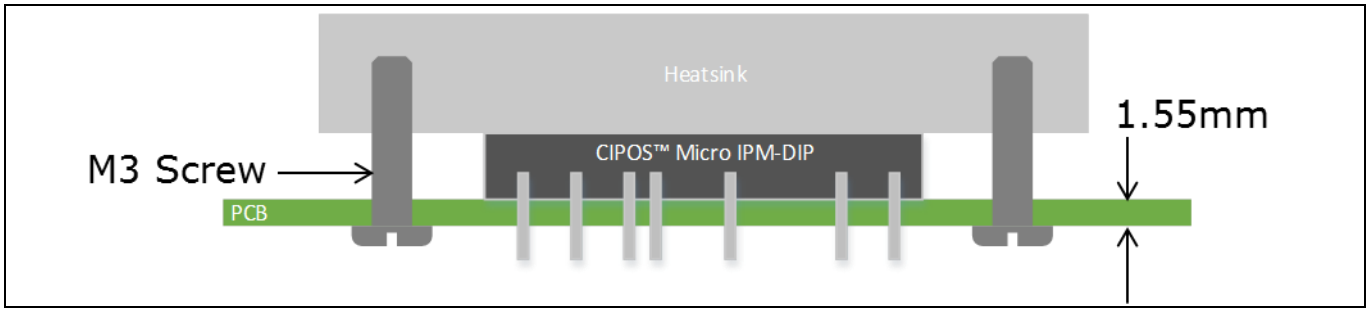


Figure 37 Screwed heatsink to PCB example

Results from this set-up showed that T_i greater than or equal to 0.7 Nm would cause major issues with performance, and would even cause the pins of the module to pull up from the PCB. It is recommended to assess the planned heatsink relative to the PCB design prior to use to ensure that the PCB does not warp from too much torque. Maximum contact force allowed for the modules is discussed in Section 6.4.9.

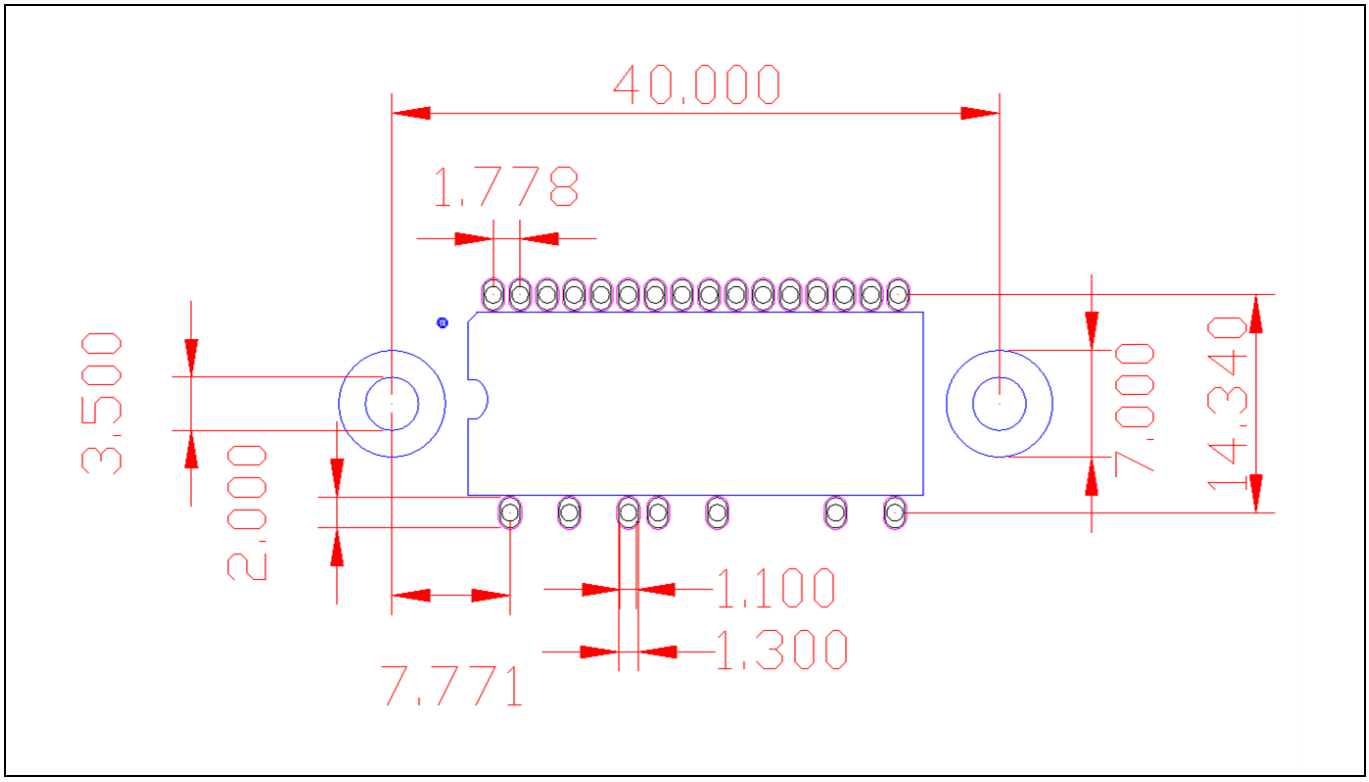


Figure 38 Screwed heatsink to PCB footprint example

6.4.3 Sheet metal heatsink to PCB

Similar to the heatsink design previously described, this method implements a heatsink that is connected directly to the PCB. Sheet metal with tabs is positioned with thermal grease across the module, and tabs are inserted through the PCB as shown in Figure 39.

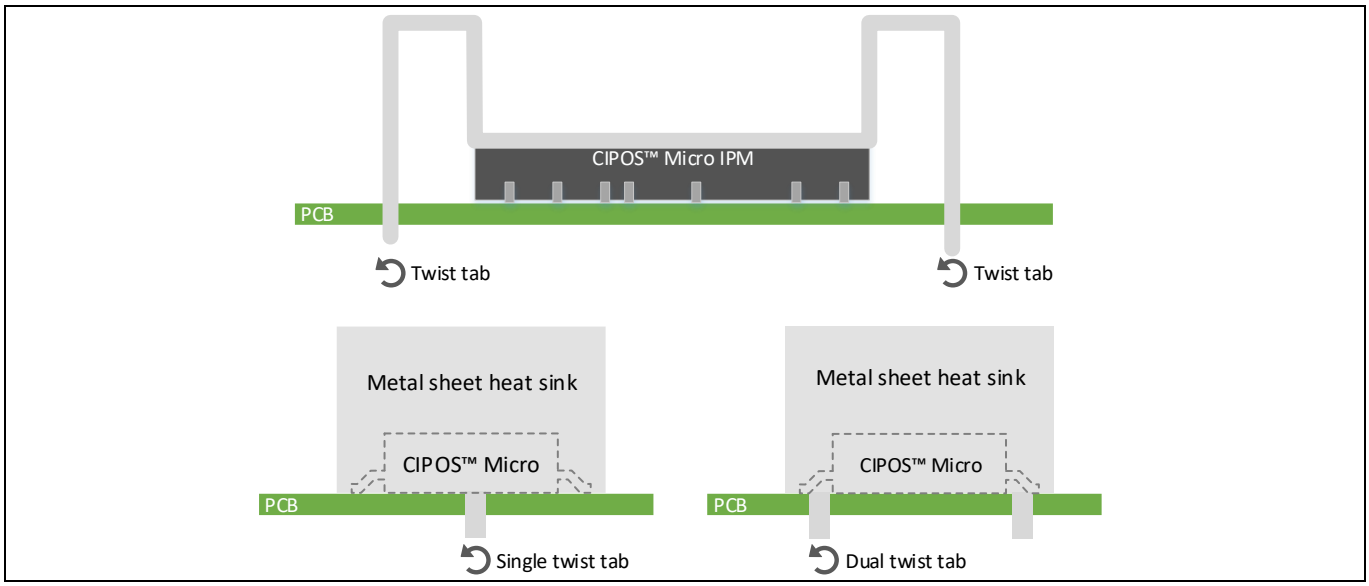


Figure 39 Sheet metal heatsink to PCB example

These tabs are twisted or soldered to secure the heatsink in place. This method has many different designs, two of which are shown above with single or dual-twist tabs. When using the tabs on the PCB, the PCB should not be allowed to warp. Warpage can result in cracking of the solder joints between the module pins and PCB pads, especially for SMD-type modules.

6.4.4 Push-pinned heatsink to PCB

This method is suitable for large heatsinks only, as too small of a heatsink may heat up the push-pins and cause structural issues. The push-pins are inserted in the corners of the heatsink, at a distance from the IPM. Figure 40 shows an example with two push-pins inserted diagonally across from each another to support the heatsink. Thermal grease should be applied between IPM and heatsink.

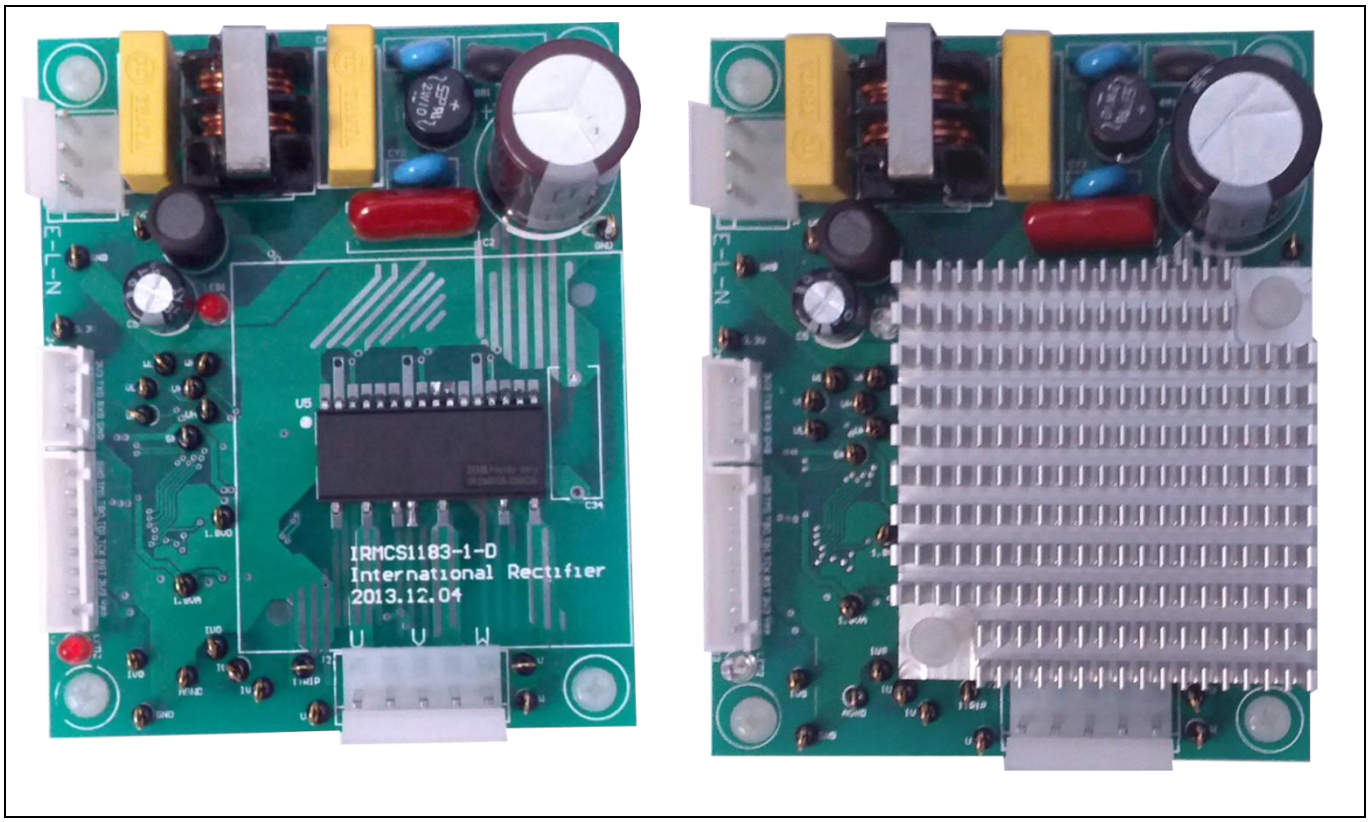


Figure 40 Push-pinned heatsink to PCB example

When using the push-pins on the PCB, the PCB should not be allowed to warp. Warpage can result in cracking of the solder joints between the module pins and PCB pads, especially for SMD-type modules. Maximum contact force allowed for modules is discussed in section 6.4.9.

6.4.5 TO-220 heatsink coupled with clip to PCB

Mass-market heatsink assemblies designed for TO-220 and TO-247 packages work very well with the CIPOS™ Micro IPM product series IRSM5xx and IM240. This is a very cost-effective heatsinking solution, while providing 30% higher power capability than without a heatsink.

One of the main designs uses a bolt-on TO-220 heatsink coupled with a commonly used clip. This is shown in Figure 41. The heatsink is placed across the IPM with thermal grease applied inbetween. The clip lies across the heatsink and attaches directly to the PCB.

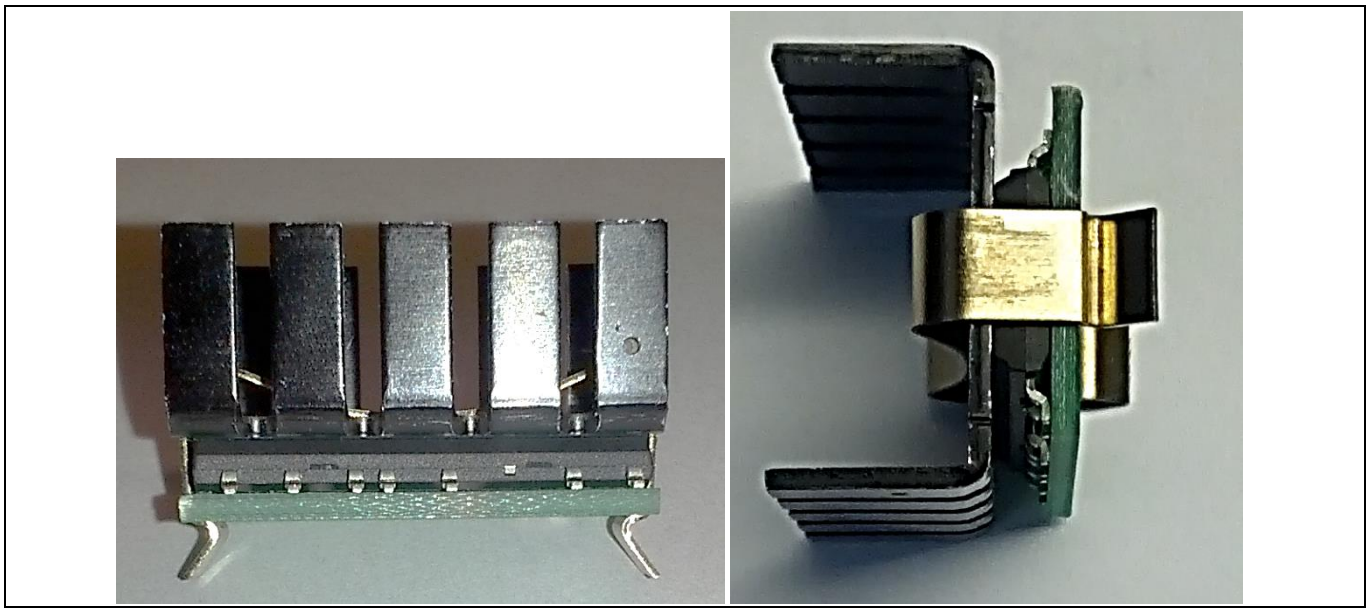


Figure 41 Heatsink coupled with clip to PCB example

PCB footprint for this method should include cutouts to accommodate clip. See example below. The universal footprint is shown (allows for mounting of SOP29x12F and DIP29x12F package options).

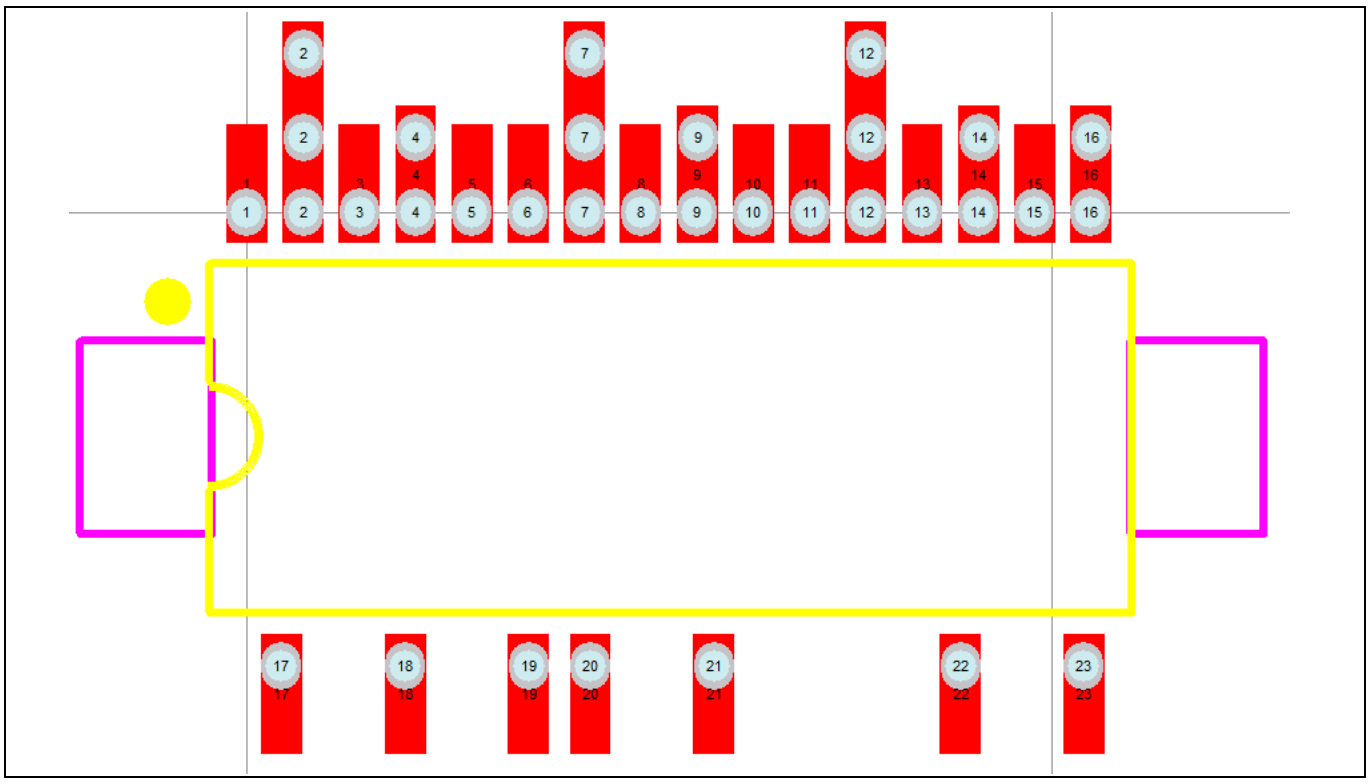


Figure 42 Heatsink coupled with clip to PCB footprint example

When implementing this method, the clip should not be too tight in the area where the PCB may warp. Warpage can result in cracking of the solder joints between the module pins and PCB pads, especially for SMD-type modules. Maximum contact force allowed for modules is discussed in Section 6.4.9.

Table 9 Heatsink suggestions

Heatsink type	Manufacturer	Part number	Clip part number
TO-220 Bolt-On	Aavid Thermalloy	530614B00000G	Kunze KU-SBK-0396-ES-ST-0.5 mm Assmann V22
	Wakefield Thermal Solutions	290-1AB	
	Assmann WSW Components	V2109B	

6.4.6 Required heatsink performance

If the power losses (P_{SW}), junction-to-case thermal resistance ($R_{th\,(J\text{-}C)}$), and maximum ambient temperature are known, the required heatsink thermal resistance and the thermal interface material can be calculated for the specific application. This can be done using the formula:

$$T_{J,max} = T_{A,max} + \sum_i P_{sw,i} \cdot R_{th,HS-A} + \sum_i P_{sw,i} \cdot R_{th,C-HS} + \max(P_{sw,i} \cdot R_{th,JC,i})$$

For three-phase IPMs, it can be assumed that all power switches dissipate the same power and have the same $Rth_{(J\text{-}C)}$ within reason. The required thermal resistance from case to ambient can then be calculated:

$$R_{th,C-A} = R_{th,C-S} + R_{th,HS-A} = \frac{T_{J,max} - P_{sw} \cdot R_{th,JC} - T_{A,max}}{\sum P_{sw}}$$

6.4.6.1 Calculating required heatsink performance example

The power switches of an outdoor fan drive dissipate 0.8 W maximum each. The maximum ambient temperature is 50°C, the maximum junction temperature is 150°C and $R_{th\,(J\text{-}C)}$ of the module is 6°K/W. With this information, $Rth_{(C\text{-}A)}$ can be calculated:

$$R_{th,C-A} \leq \frac{150°C - 0.8W \cdot 6\frac{°K}{W} - 50°C}{6 \cdot 0.8W} = 19.8\frac{°K}{W}$$

If the heatsink temperature is limited to 100 °C, an even lower thermal resistance is required:

$$R_{th,C-A} \leq \frac{100°C - 50°C}{6 \cdot 0.8W} = 10.4\frac{°K}{W}$$

Smaller heatsinks with higher thermal resistance may be acceptable if the maximum power is only required for a short time (times below the time constant of the thermal resistance and the thermal capacitance). However, this requires a detailed analysis of the transient power and temperature profiles. The larger the heatsink, the larger its thermal capacitance, i.e., the longer it takes to heat up.

6.4.7 Heatsink characteristics

Heatsinks are characterized by three parameters:

- Heat transfer from the power source to heatsink
- Heat transfer within the heatsink (to all the surfaces of the heatsink)
- Heat transfer from heatsink surfaces to ambient

6.4.7.1 Heat transfer from heat source to heatsink

There are two factors which need to be considered in order to provide a good thermal contact between power source and heatsink:

- Flatness of the contact area

  Due to the unevenness of surfaces, a thermal interface material needs to be supplied between heat source and heatsink. Such materials have a rather low thermal conductivity (<10 K/W), and therefore should be as thin as possible. The material still needs to fill out the space between heat source and heatsink, and an unevenness of the inserted material should be avoided. In addition, the particle size of the interface material must fit to the roughness of the module and the heatsink surfaces. Particles that are too large will unnecessarily increase the thickness of the interface layer, and increase the overall thermal resistance. Particles that are too small will not provide a good contact between the two surfaces, and will also lead to a higher thermal resistance.
- Mounting pressure

  The higher the mounting pressure, the better the interface material disperses. Excessive interface material is squeezed out resulting in a thinner interface layer with a lower thermal resistance.

6.4.7.2 Heat transfer within heatsink

The heat transfer within the heatsink is mainly determined by:

- Heatsink material

  The material needs to be a good thermal conductor. Most heatsinks are made of aluminum (λ ≈ 200 W/ (m·K)). Copper is heavier and more expensive but also nearly twice as efficient (λ ≈ 400 W/ (m·K)).
- Fin thickness

  If the fins are too thin, the thermal resistance from the heat source to each fin will be too high, and the efficiency of the fins reduced. Hence, it does not make sense to make the fins as thin as possible to increase the surface area by including more fins.

Please note that heatsinks have a thermal spreading resistance, in which not all points of the heatsink will be at the same temperature, which may lead to local hotspots at the center of the IPM. This must be considered in order to calculate heat transfer accurately.

6.4.7.3 Heat transfer from heatsink surface to ambient area

Heat transfers to ambient area mainly by convection. The corresponding thermal resistance is defined as:

$$R_{th,conv} = \frac{1}{\alpha \cdot A} V$$

Where,

- α = heat transfer coefficient
- A = surface area

This leads to two important factors:

- Surface area

  Heatsinks require a huge surface area in order to easily transfer the heat to ambient area. Since the heat source is assumed to be concentrated at one point, and not uniformly distributed, the total thermal resistance of a heatsink does not change linearly with length. Also, increasing the surface area by increasing the number of fins does not necessarily reduce the thermal resistance as discussed in Section 6.4.7.2.
- Heat transfer coefficient

  This coefficient is strongly dependent on the air flow velocity, as shown in Figure 43. If externally induced, air flow is used to aid in the transfer of heat; this is called forced convection. Otherwise, the transfer of heat

with no additional help is considered natural convection. Heatsinks with very small fin spacing do not allow a good air flow. If a fan is used (forced convection), then the fin gaps of the heatsink may be reduced, as the fan forces the air through the space between the fins.

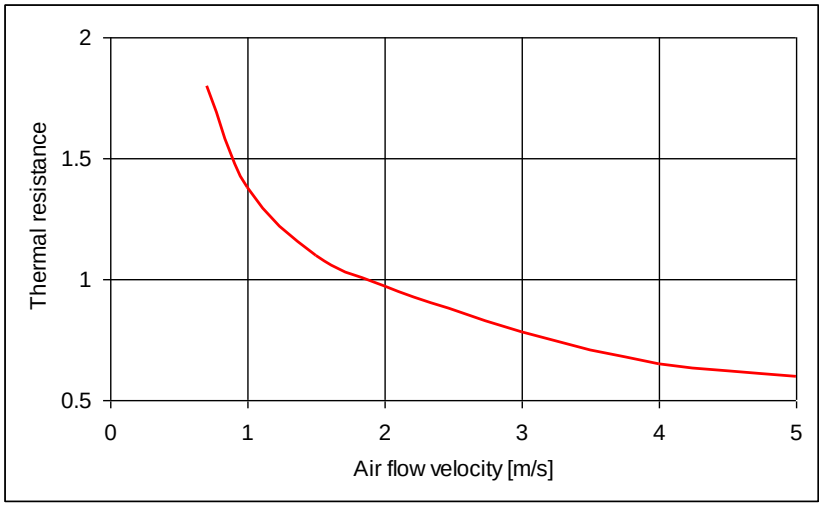


Figure 43 Thermal resistance vs. air flow velocity

In cases of natural convection, the heatsink efficiency depends on the temperature difference of heatsink and ambient area (i.e. on the dissipated power). Some manufacturers, like Aavid Thermalloy, provide a correction table which allows the calculation of thermal resistance dependent on the temperature difference. Figure 44 shows the heatsink efficiency degradation for natural convection as provided in the previous equation. Please note that the thermal resistance is 25% higher at 30 W than at 75 W.

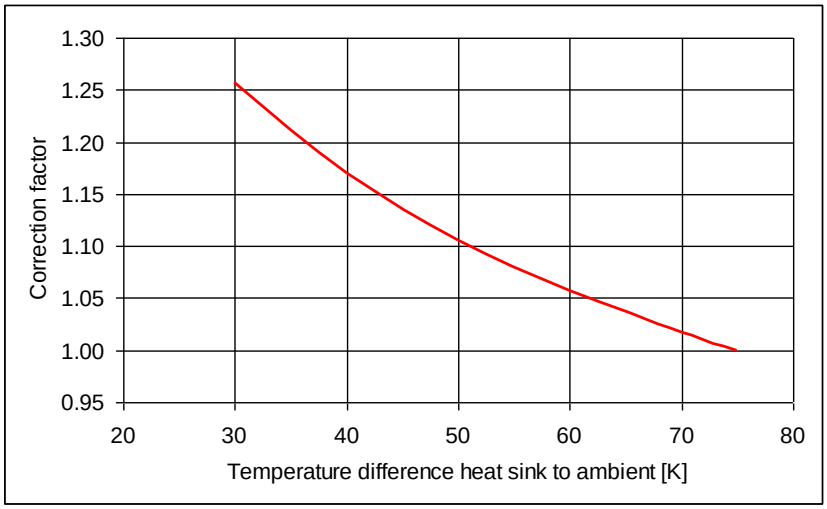


Figure 44 Correction factors for temperature

The positioning of the heatsink also plays an important role. In the case of natural convection, the best heatsink mounting position is with the fins of the heatsink mounted vertically, as the heated air tends to move upwards. Furthermore, one should make sure that there are no significant obstructions impeding the air flow.

Radiation occurs as well supporting the heat transfer from heatsink to ambient area. In order to increase the radiated heat, one can use anodized heatsinks with a black surface. While radiated heat is negligible in forced convection conditions, it does slightly decrease the thermal resistance of the heatsink in cases of natural convection. Therefore, blank heatsinks are preferable in natural convection conditions.

The discussions in this section clearly show that there cannot be only one thermal resistance value assigned to a certain heatsink.

6.4.7.4 Selecting a heatsink

Unfortunately, there is no straightforward method for selecting a heatsink. Finding a sufficient heatsink most likely will include an iterative process of choosing and testing heatsinks. In order to get a first rough estimation of the required volume of a heatsink, one can start with estimated volumetric thermal resistances, as given in Table 10 below (taken from [6]). This table only gives initial values, as the actual resistance varies for multiple parameters like dimensions, type, orientation, etc.

Table 7 Volumetric thermal resistance

Flow conditions [m/s]	Volumetric resistance [cm³ °C/W]
Natural convection	500~800
1.0	150~250
2.5	80~150
5.0	50~80

It can be roughly assumed that the volume of a heatsink needs to be quadrupled in order to halve its thermal resistance. This gives an idea about whether natural convection is sufficient for the available space, or forced convection is required.

In order to select an optimized heatsink for a given application, one needs to contact heatsink manufacturers or consultants.

When contacting heatsink manufacturers, please check the conditions under which the given thermal resistance values are valid. They might be given either for a point source or for a heat source which is evenly distributed over the entire base area of the heatsink. Also take care that the fin spacing is optimized for the corresponding flow conditions.

6.4.8 General mounting guidelines

An adequate heatsinking capability of an IPM is only achievable if it is suitably mounted. The following general points should be observed when mounting a heatsink in any of the methods previously described.

- There should be no burrs on aluminum or copper heatsinks
- Screw holes in heatsink should be countersunk
- There should be no unevenness or scratches in the heatsink
- The surface of the module should be completely in contact with the heatsink
- There should be no oxidation, stains or burrs on the heatsink surface

To improve the thermal conductivity, apply silicone grease to the contact surface between the IPM and heatsink. Spread a homogenous layer of the silicone grease with a thickness of 100 µm over the IPM's substrate surface. Non-planar surfaces of the heatsink may require a thicker layer of thermal grease. Please refer here to the specifications of the heatsink manufacturer. It is important to note that the heatsink should cover the complete backside of the module. There may be different functional behavior if a portion of the backside of the module is not in contact with the heatsink.

In general, if the heatsink surface roughness is greater than 3 µm Ra, the maximum roughness of CIPOS™ Micro IPM, it is recommended to use a thermal pad instead of grease. A heatsink with a surface roughness of 20 µm Ra or greater should not be used, as proper IPM heat dissipation and optimized $Rth_{C\text{-}A}$ cannot be ensured.

Thermal system design

To prevent a loss of heat dissipation effect due to warping of the substrate, tighten down the mounting screws gradually and sequentially while maintaining a left/right balance in pressure applied.

It should be assured by the design of the PCB application, that the plane of the back side of the module and the plane of the heatsink are parallel in order to achieve minimal tensions of the package and an optimal contact of the module with the heatsink. Please refer to the mechanical specifications of the module given in the datasheets.

It is considered the basics of good engineering to verify the function and thermal conditions by means of detailed measurements. It is best to use a final application inverter system, assembled with the final production process, to help achieve high-quality applications.

6.4.9 Contact force

Contact force to the module, especially when securing heatsinks, needs to be taken into consideration to ensure proper performance.

A contact force test was conducted for the CIPOS™ Micro SOP package to determine the amount of force the modules can withstand before damage. The modules were mounted to PCB DUT cards, and increasing contact force was applied over time. Test set-up is shown in Figure 45 below.

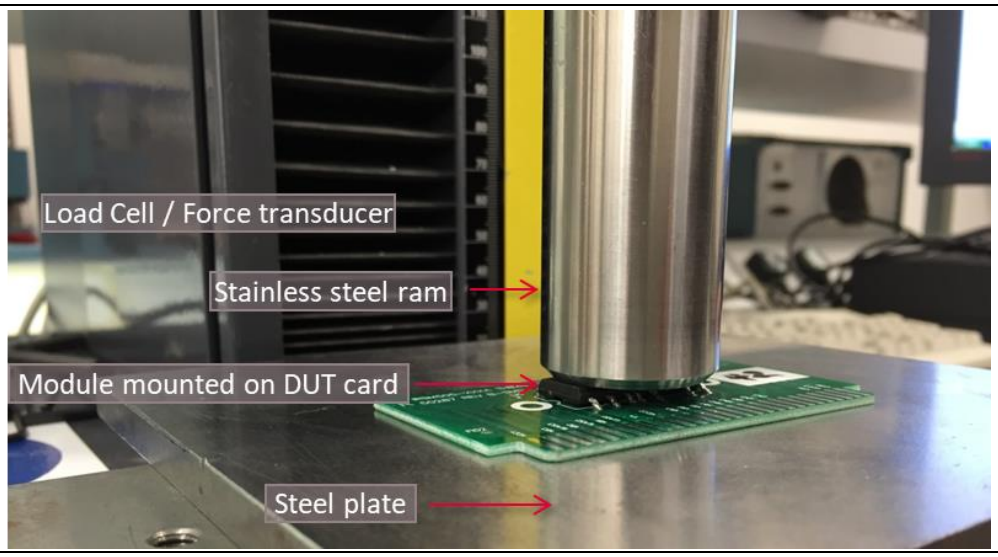


Figure 45 Contact force test set-up

During the test, two events were observed as the contact force was increased. The first event that occurred was the flattening of the PCB card. Some PCB DUT cards exhibit a convex warpage as illustrated below. A contact force of about 3 N is enough to change the shape, and flatten the PCB DUT card.

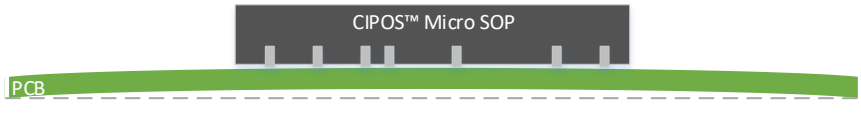


Figure 46 PCB warpage

Thermal system design

The second event observed during the test occurred around 100-200 N. Due to variations in the soldering process, some modules exhibit a small air gap between the bottom of the module and the PCB DUT as shown in Figure 47. On applying 100-200 N contact force, the gap is closed by deforming the module leads.

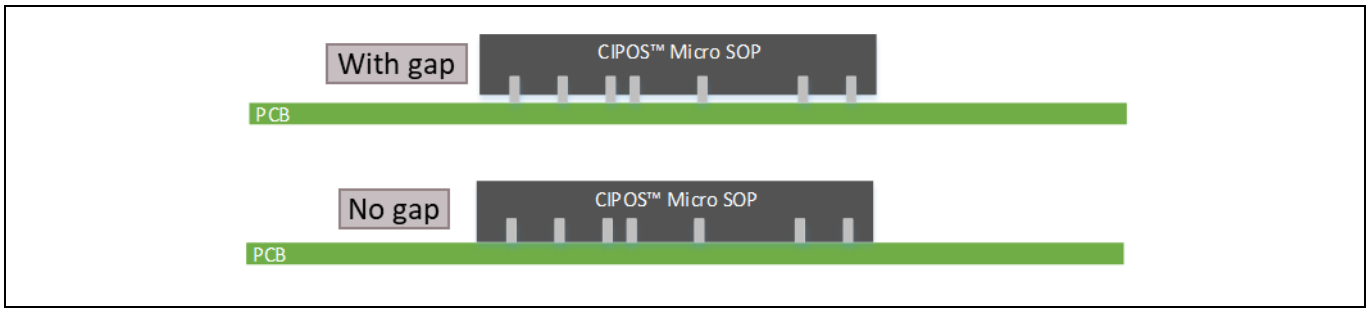


Figure 47 Lead deformation

Lastly, a force of 1000 N was applied to the modules four times. After applying this force, the modules were put through parametric testing to test for damage. All modules passed testing. A summary of the events are listed in the table below.

Table 11 Contact force test on CIPOS™ Micro SOP 29x12F

Force	Notes
3-5 N	PCB card is flattened
100-200 N	Leads are bent to flatten module against PCB
1000 N+	Functionality of module is not confirmed

As discussed previously, a force of over 100 N may deform modules by bending the leads so that the package body lays flat against the PCB. Care must be taken to inspect the leads and solder joints for any possible fractures. Bench tests have shown that 1000 N can be applied to CIPOS™ Micro IPM (package SOP 29x12F) without affecting functionality.

7 Additional guidelines

7.1 Handling

When installing a heatsink, excessive uneven tightening force might apply stress to inside chips, which will lead to breaking or deterioration of the device. To achieve effective heat dissipation, it is necessary to enlarge the contact area as much as possible, which minimizes the contact thermal resistance.

Apply thermal conductive grease properly over the contact surface between the module and the heatsink. This is also useful for preventing corrosion to the contact surface. The grease should be of stable quality and long-term durability within a wide operating temperature range. Ensure there is no debris remaining on the contact surface between the module and the heatsink. All equipment, which is used to handle or mount the module, should comply with the relevant ESD standards. This includes transportation, storage and assembly. The module itself is an ESD-sensitive device. It may therefore be damaged in the case of ESD shocks. Do not shake or handle by gripping only the heatsink, and in particular, do not cause shock to the PCB by grippng only the heatsink. This could cause package cracking or breaking.

7.2 Recommended storage conditions

Temperature: 5 ~ 35 °C

Relative humidity: 45 ~ 75%

- Avoid leaving module exposed to moisture or direct sunlight. Be particularly careful during periods of rain or snow
- Use storage areas where there is minimal temperature fluctuation

Rapid temperature changes can cause moisture condensation on the stored IPM, resulting in lead oxidation or corrosion, and eventually to degraded solderability.

- Do not allow the module to be exposed to corrosive gasses or dust
- Do not allow excessive external forces or loads to be applied to the module while in storage

8 References

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