PCB design guidelines for XENSIV™ 60 GHz Radar MMICs with AIP

Best practices and recommendations

About this document

Scope and purpose

This document provides PCB layout recommendations and best practices for XENSIV™ 60 GHz Radar MMICs with Antenna-in-Package (AIP) to achieve optimal radar performance.

Intended audience

The intended audiences for this document are design engineers, technicians, and developers of electronic systems working with radar technology. You are expected to interpret circuit schematics and understand fundamental PCB concepts, such as nets, components, vias, planes, and signal integrity concerns. While key concepts will be referenced, detailed explanations of basic electronics theory are not included.

Key points

- Describes PCB layout practices that mitigate RF sensitivity and layout-dependent performance variations in 60 GHz AIP radar designs
- Explains placement, routing, grounding, and stackup methods that ensure signal integrity and stable antenna behavior
- Provides practical design choices that reduce coupling, noise, and mechanical interference for reliable radar operation
- Highlights implementation options, such as EBG structures, triplet routing, and optimized keep-out zones for improved robustness
- Summarizes best-practice features that enhance layout consistency, manufacturability, and end-application performance

About this product family

Product family

Infineon's XENSIV™ 60 GHz radar MMICs with Antenna-in-Package (AIP) provide compact, high-precision, and low-power sensing solutions for IoT, smart home, and consumer applications.

Target applications

- Motion detection: Lighting, HVAC control, and security systems and intruder detection
- Gesture sensing: Smart speakers, TVs, and wearables
- Fall detection: for elderly care and privacy-focused monitoring (no camera image captured)
- Industrial automation: Level sensing and collision detection for robotics
- Presence sensing: Smart entrance counting and tracking

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1 Introduction

1.1 XENSIV™ 60 GHz Radar MMICs with AIP

Infineon's XENSIV™ 60 GHz Radar portfolio with Antenna-in-Package (AIP) technology offers a highly integrated and efficient solution for advanced radar sensing. These sensors are designed in both BiCMOS and CMOS technologies, ensuring exceptional RF performance, low power consumption, and compact designs suitable for a variety of applications.

Operating in the 60 GHz frequency range, these sensors deliver precise motion detection with high sensitivity that can detect even sub-millimeter movements. The Antenna-in-Package (AIP) design simplifies integration into space-constrained devices, while the portfolio supports both autonomous and SPI modes for flexible configurations and real-time data acquisition. With their advanced technology and versatility, the XENSIV™ 60 GHz radar sensors set a new benchmark for innovation in radar sensing.

1.2 Radar system design prerequisites

Familiarity with at least one PCB design software, such as Altium Designer, Allegro PCB, KiCAD, or Autodesk Eagle, is required, along with prior experience in PCB design, including schematics creation, layout design, and basic output file generation.

1.3 Software requirements

To review and work with PCB layouts, you must use PCB design software (SW), such as KiCAD, Altium Designer, Allegro PCB, and Autodesk Eagle. If a PCB review is submitted using other software, ensure that exported files are provided in one of the supported formats to facilitate Infineon's technical review process.

1.4 Infineon technical review requisites

For review purposes (e.g., for design support from Infineon or design-in activities), the bill of materials (BOM) must include Infineon components with a certain minimum value per PCB. This value depends on the project's quantity and customer profile. Compliance with this requirement ensures that the project qualifies for technical validation or feedback under Infineon's support framework. For additional details, contact Infineon support.

2 PCB design considerations for AIP radar

Consumer radar PCBs differ from generic digital or analog boards because of their high-frequency design challenges, compact integration, and sensitivity to layout. Consider the following key parameters to begin with:

- **Antenna type:** This document focuses on Integrated Antennas or Antenna-in-Package (AIP), included in most Infineon consumer and industrial radar MMICs

Note: External antennas design is out of scope for this document.

- **Power supply requirements:** Consider recommended radar power supply options
- **Communication interfaces:** SPI for data readout or control. For details, see Section 2.3.4
- **Form factor constraints:** Physical limits defined by the enclosure or mechanical housing
- **Radome:** If the radar is not exposed directly to the target, but hidden behind any enclosure, a radome is needed. Radome design is not in the scope of this document

Note: Ensure that you collect all component datasheets and interface specifications at this stage.

2.1 PCB material selection and layer stackup

Before starting the layout, check with the PCB manufacturer to see if they can produce the recommended layer stackup, available for each Infineon demo, evaluation, or reference design board.

To find recommended layer stackup, search on the Infineon website for any Infineon board-based on the selected radar MMIC. Download the design files and share the layer stackup file, which is always included inside the zip file, with your PCB manufacturer. Any modification to the layer stackup can have an impact on the final product performance so it is advised to use them as described.

On the other hand, if your requirements are lower than those specified on the datasheet, you may use a different layer stackup. For example, if in the MMIC datasheet, the maximum target detection range is 14 meters, but your application requires only 5 meters, then using a simpler layer stackup may fulfill your requirements.

A 4-layer FR-4 stackup is typically sufficient. See Section 6 for the optimized layer stackup for specific Infineon MMICs.

2.2 Radar MMIC placement

Many of Infineon's 60 GHz radar sensors feature an Antenna-in-Package (AIP) configuration where the complete RF radio system, consisting of silicon and antennas is integrated into a small package. This concept provides reduced sensor system size, facilitates sensor integration into an application, and does not demand RF knowledge to design external antennas and other RF structures.

However, to achieve optimum sensor performance, consider the impact of the PCB layout during the design.

2.2.1 Component height restrictions

Primarily, place the radar MMIC, as it is the core of the application and its position determines the antenna exclusion zone. As shown in Figure 1, the area is typically a 10 mm radius around the MMIC. Ensure that this area is kept free of tall components, vias, and copper pours. However, as with the PCB layer stackup, following this guidance is required to achieve maximum performance.

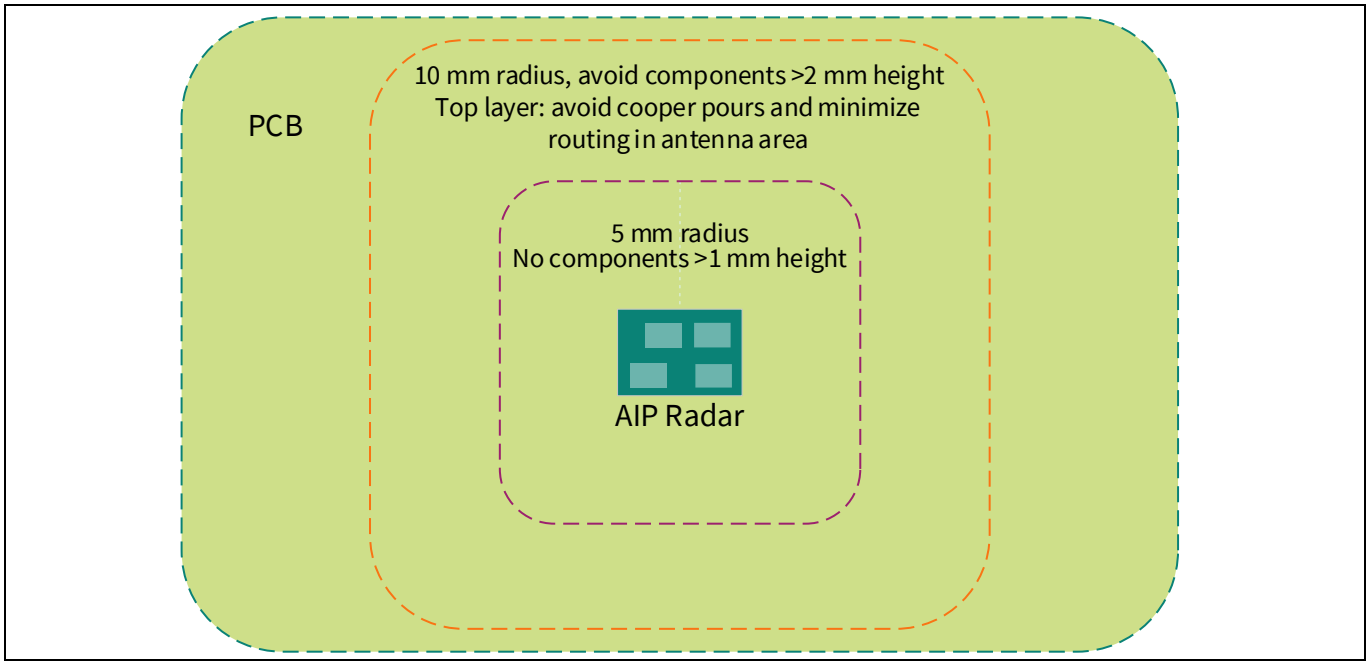

Figure 1 Antenna-in-Package (AIP) keep out zones

2.2.2 Radar PCB area keep-out zones

In addition to height, consider the top-layer copper and silk within the antenna keep-out zone:

- Avoid top-layer copper pours or traces in this region (unless required by the MMIC layout guide available from the MMIC datasheet)
- No test points, fiducials, or labels
- Avoid routed slots, cutouts, or mechanical features directly under or around the MMIC

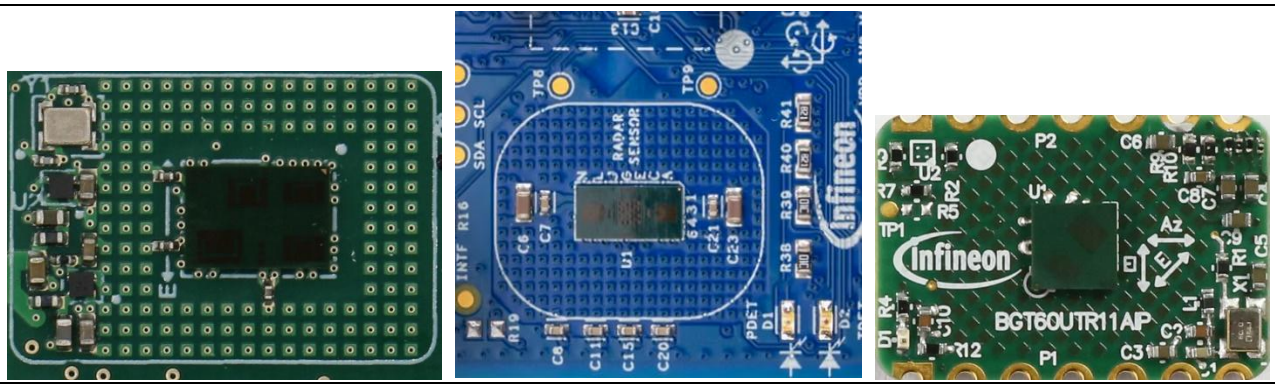

Figure 2 Radar placement using a keep out-zone and EBG structures around the radar MMIC

Figure 3 shows boards without enough space for a clear AIP radar keep out zone, making a compromise in component placement but still achieving good performance.

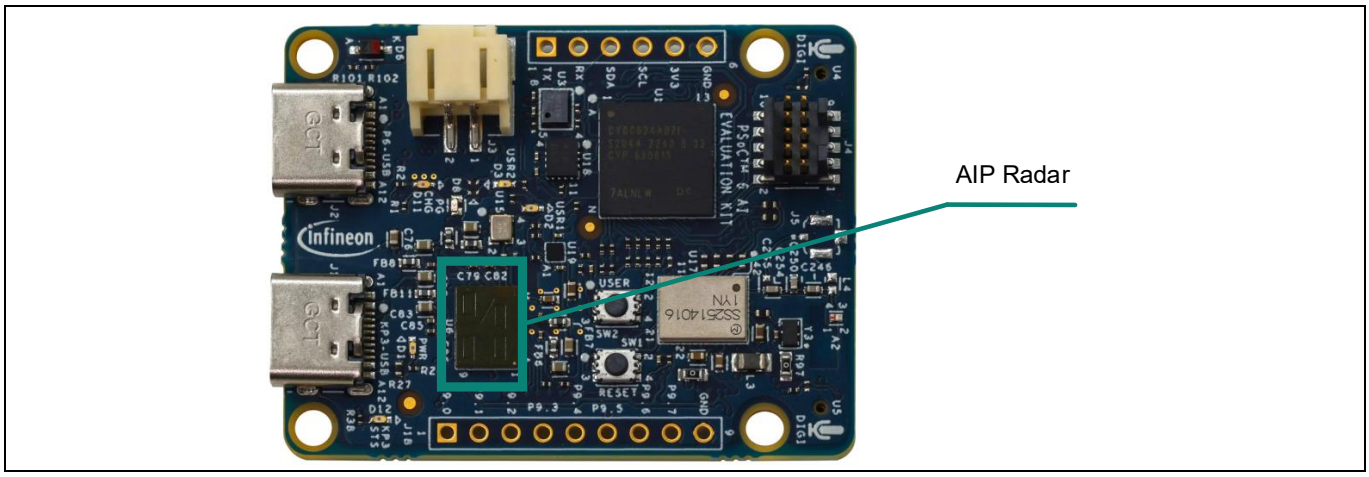

Figure 3 Radar placement on boards

2.2.3 Orientation of the radar MMIC

In radar systems with AIP technology, the orientation of the MMIC is non-rotational, which means the embedded antennas are fixed in direction. This makes the correct alignment of the MMIC on the PCB absolutely essential for achieving optimal signal coverage and directionality for your use case.

2.2.4 Direction considerations

- **Fixed antenna directions:** The antennas inside the MMIC package are physically aligned in specific directions, one for azimuth (horizontal field of view (FoV)) and one for elevation (vertical FoV). These cannot be changed by software or during runtime
- **Alignment to the application's field of view:** You must align the MMIC so that its Azimuth axis matches the expected horizontal scanning range, and its elevation axis matches the required vertical coverage. Misalignment (e.g., rotating the MMIC 90° or 270° from its intended orientation) will result in:
  - Poor signal gain in the desired direction
  - Incorrect object tracking performance
  - Reduced range and angular accuracy

Figure 4 shows portrait mode with wider E-plane in Azimuth orientation and landscape mode with wider E-plane in elevation orientation for the BGT60CUTR13AIP radar MMIC.

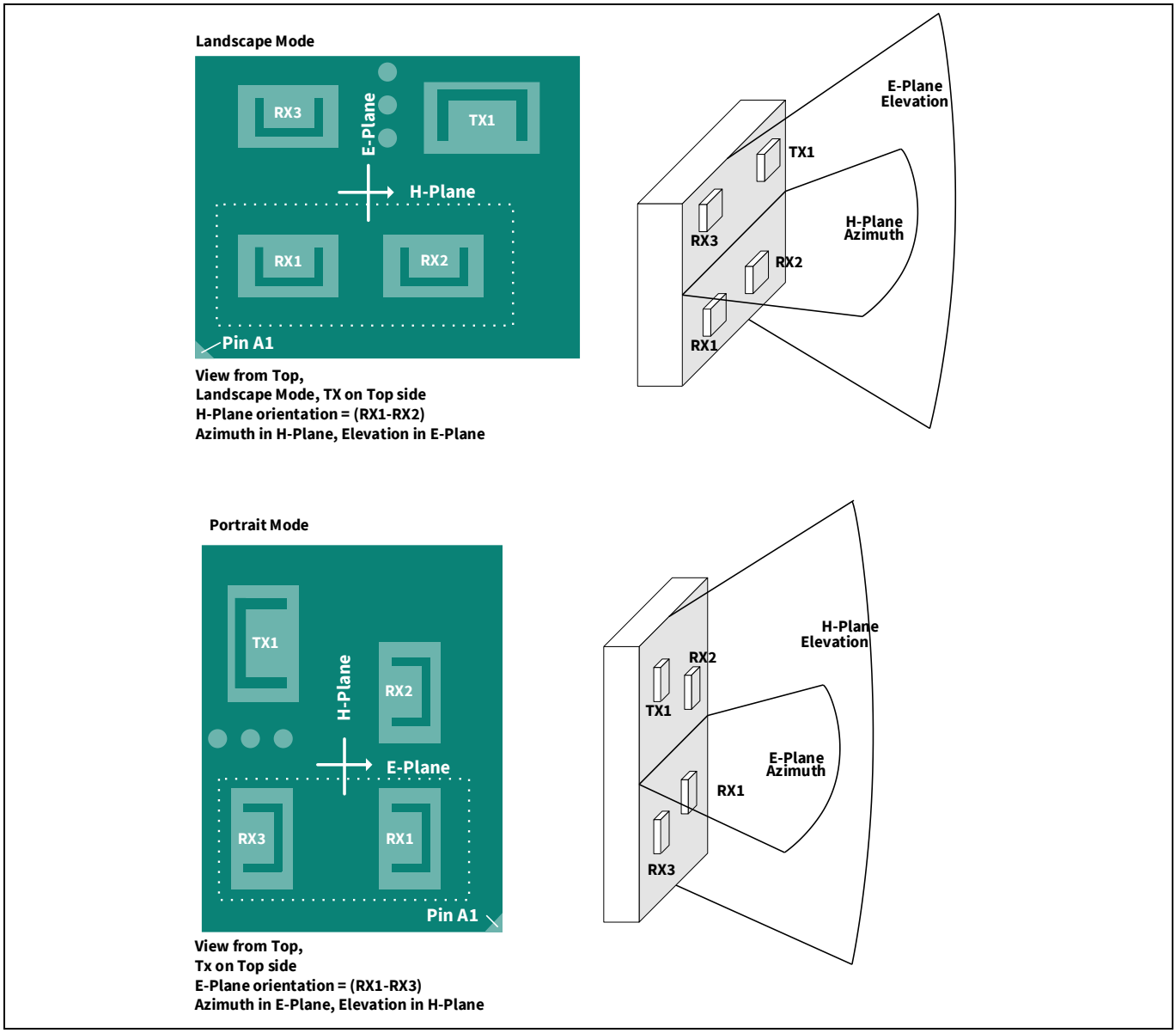

Figure 4 BGT60CUTR13AIP antenna naming and orientation

2.2.5 Orientation recommendations

- Clearly mark the azimuth and elevation axes in your layout with silkscreen, at least during the development phase
- See the chosen radar MMIC datasheet or reference design to confirm the package orientation and antenna field definitions
- Create a component height restriction zone in your PCB design
- Use 3D models to verify clearance during placement
- Consider the final product orientation when defining these zones

2.2.6 Housing and mechanical considerations

If the radar PCB is enclosed in a plastic housing:

- Ensure no metallic brackets, battery holders, shields, or casings sit above the MMIC's aperture
- Transparent or RF-friendly plastics are preferred for any material in front of the radar. Avoid foam pads or adhesives on the MMIC package lid
- Once all housing specifications are defined, make sure you run an EM Simulation to check the performance.
- **Mechanical enclosure and final product orientation:** Always consider how the entire module will be mounted in the final product (e.g., automotive bumper, smart door, appliance housing). Consider the design with the MMIC, which must be oriented according to the final mechanical orientation.

Note: For optimal performance, maintain an air gap between 2.4 mm to 2.7 mm above the PCB and leave room for beam propagation in your mechanical design. The exact air gap depends on the lens dielectric constants and other plastic parts in between.

Figure 5 shows the radome including the MCU board, shield PCB, and the radar sensor with radome thickness (T) and distance (airgap) between the shield PCB and the radome bottom surface.

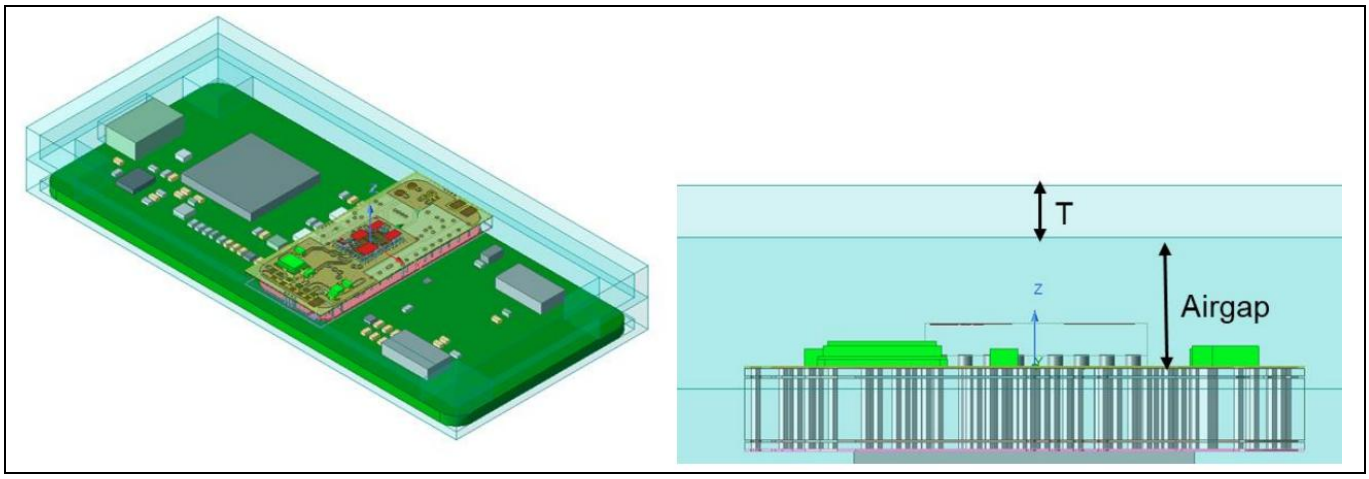

Figure 5 Radome with the MCU board

2.3 Placement considerations

Component placement is one of the most critical stages in radar PCB layout design. A well-planned placement ensures signal integrity, thermal efficiency, mechanical reliability, and simplifies routing.

A methodical component placement flow should follow a prioritized approach. After placing the radar MMIC, the following high priority functional blocks should be prioritized. The functional blocks priority will be enumerated and dissected in the following sections.

2.3.1 Critical analog or RF passive components

Place critical passives like feeding capacitors as close as possible to their associated MMIC pins. These must be compact and low profile, ideally 0201 or 0402 sizes. Use short, direct routing, keep impedance-controlled sections short, and use matched components.

2.3.2 Power management devices

- Place a low dropout (LDO) regulator as close as possible to the target device
- Ensure a clean power path from input connectors to radar power rails
- Keep noisy switching regulators as far as possible from the MMIC
- Consider placing ferrite beads in the power supply traces to reduce interference and noise from the power supply. Be aware that ferrite beads have certain DC resistance as well, which will introduce a voltage drop at high current
- Do not place a ferrite bead between the LDO output and MMIC, especially for fast short pulsing SRR systems (unwanted V-drop)
- Use wide traces or whole copper areas in a power plane for supply signals to reduce inductance

2.3.3 Oscillators, resonators

To avoid interference on the crystal oscillator from EMI, connect the quartz resonator GND pads directly to the GND plane via separate via holes, and do not connect it to other component GND connections on the component layer.

2.3.4 Control and communication interfaces

- Place microcontrollers, SPI/I^2C level shifters, EEPROMs, and debug headers
- Keep trace lengths short to the MMIC control pins
- Minimize coupling between digital control signals and RF routing by separating zones and using proper grounding

2.3.5 Low-priority components

Place general passives, indicators (LEDs), test points, and mechanical supports last. These components must not violate mechanical or RF clearance areas and should follow signal integrity and manufacturability guidelines.

2.3.6 Recommendations for placement review

- Use design rule checks (DRC) to enforce antenna exclusion zone and component height clearance
- Validate mechanical clearance with 3D models
- Keep sensitive analog and noisy digital domains isolated
- Ensure power integrity by minimizing loops and using solid planes beneath critical ICs

3 Routing guidelines

This section outlines techniques used for making high-speed PCBs with 60 GHz radar MMICs.

3.1 Decoupling capacitors

Radar sensors are very sensitive to noise and crosstalk on the supply domains. Therefore, decouple the different supply domains.

Decoupling capacitors are used to isolate or decouple two circuits. In other words, they decouple AC signals from DC signals or vice versa.

It is recommended to use decoupling capacitors on each supply domain (and the oscillator supply).

3.2 Minimize stub length

A stub is an unintended branch or leftover segment of a trace or via that does not follow the main signal path. The longer the stub, the more it can distort or reflect the signal.

At high frequencies, even small stubs act as resonant open circuits, reflecting signals back toward the source. These reflections cause signal degradation and timing errors.

3.2.1 Design recommendations to prevent signal reflections caused by stubs

- Keep the stub length shorter than one-quarter of the switching speed of the driver (the lumped distance). If possible, reduce stub length even further, ideally less than one-tenth of the wavelength for better signal integrity
- Use via-in-pad or back-drilling techniques to eliminate stubs
- Avoid T-branch connections (especially in differential pairs) and implement daisy-chain routing. However, consider that daisy-chain topologies are best suited for designs where tight signal timing is not a critical concern
- Pull-up or pull-down resistors on high-speed signals are common sources of stubs. If such resistors are necessary, route the signals as a daisy chain, as shown in Figure 6

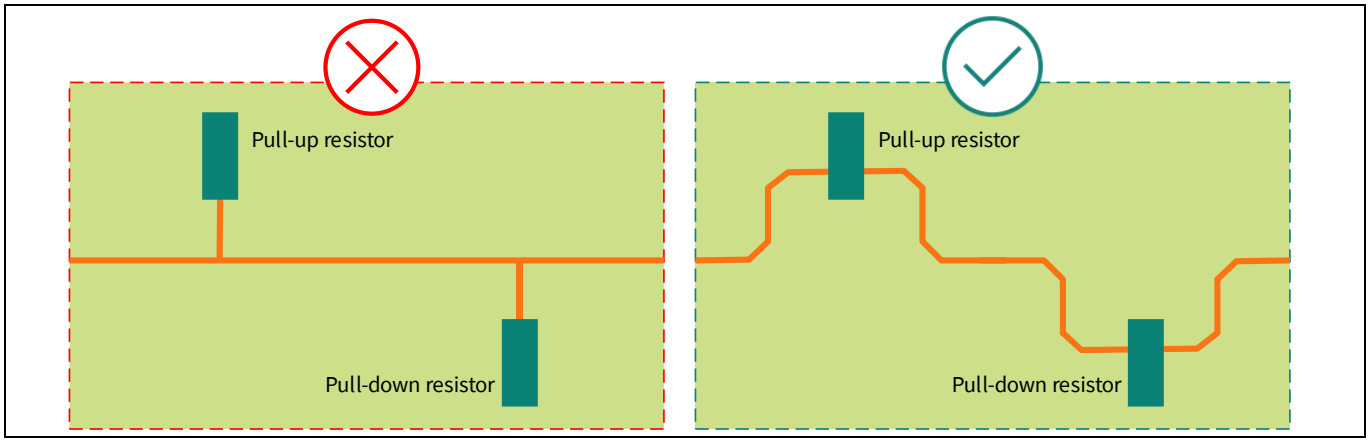

Figure 6 Implement daisy chain routing when using pull-up and pull-down resistors to avoid stubs

3.3 High-speed differential signal routing

This section provides guidance on high-speed differential signal routing.

3.3.1 Differential signal spacing

To minimize crosstalk in high-speed interfaces, the spacing between signals should be a minimum of two times and ideally five times the width of the trace. A PCB with a trace width of 6 mils requires a minimum of 12 mils but ideally 30 mils spacing between high-speed differential pairs.

3.3.2 High-speed differential signal routing recommendations

- Do not place probe or test points on any high-speed differential signal
- Keep the ground pours well away from differential pairs. If you must have them, use a clearance of three times the width of the trace
- Do not route high-speed traces under or near crystals, oscillators, clock signal generators, switching power regulators, mounting holes, magnetic devices, or ICs that use or duplicate clock signals
- If possible, route high-speed differential pair signals on the top or bottom layer of the PCB with an adjacent GND layer
- Ensure that high-speed differential signals are routed ≥90 mils from the edge of the reference plane
- Maintain a constant trace width after the SoC ball grid array (BGA) escape to avoid impedance mismatches in the transmission lines
- Maximize differential pair-to-pair spacing when possible

3.3.3 Trace length matching

- Keep total trace length for signal pairs to a minimum
- Match the etch lengths of the relevant differential pair traces
- Add serpentine routing to match lengths as close to the mismatched ends as possible
- No need to match the etch length of different differential pair groups (e.g., transmit pair length does not need to match receive pair length)
- Maintain symmetry in differential pair traces

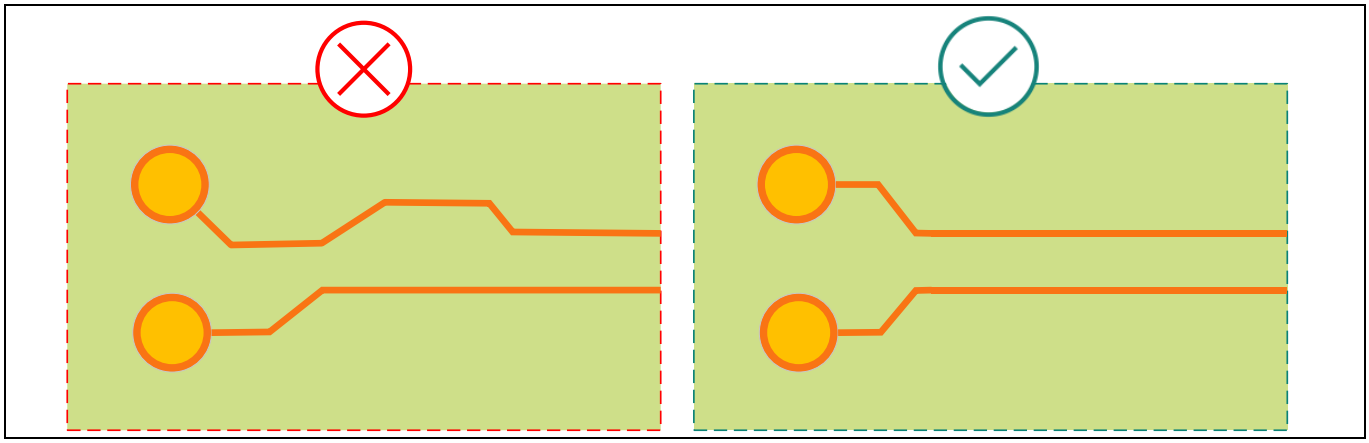

Figure 7 Route the differential pairs symmetrically and keep the signals parallel

- Route both traces on the same layer whenever possible to avoid differential impedance variation. When routing across layers, use vias of equal length and number in both traces to preserve timing and impedance

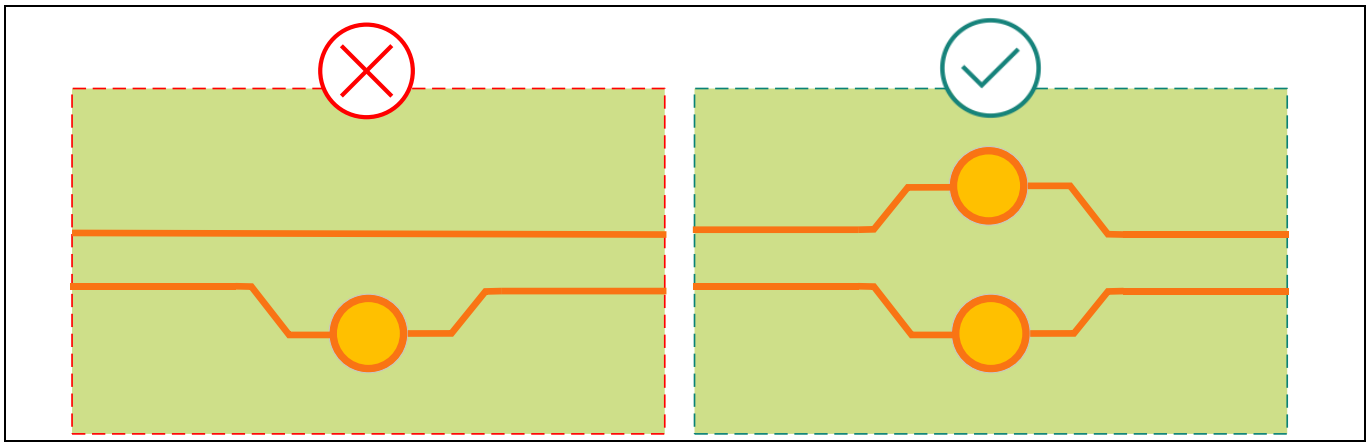

Figure 8 Route pairs on the same layer and place the same number of vias

- If differential pairs require serial coupling capacitors (AC coupling), place them symmetrically as shown in Figure 9. The capacitors create impedance discontinuities, so placing them symmetrically will reduce the risks of signal skew. Smaller component packages (like 0402) are preferable as they introduce less parasitic capacitance and inductance

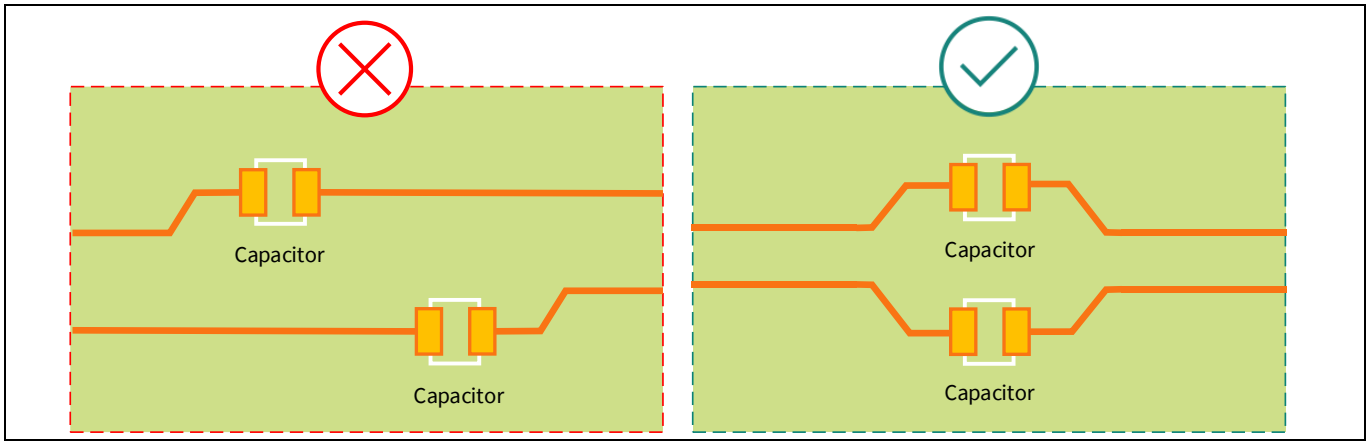

Figure 9 Place capacitors symmetrically to avoid discontinuities

- Use serpentine (accordion) routing to fine-tune shorter traces to match longer ones. This correction should be applied as close as possible to the point of mismatch (e.g., near a via or component) as shown in Figure 10. The mismatch occurs on the left set of vias, so add the serpentine on the left

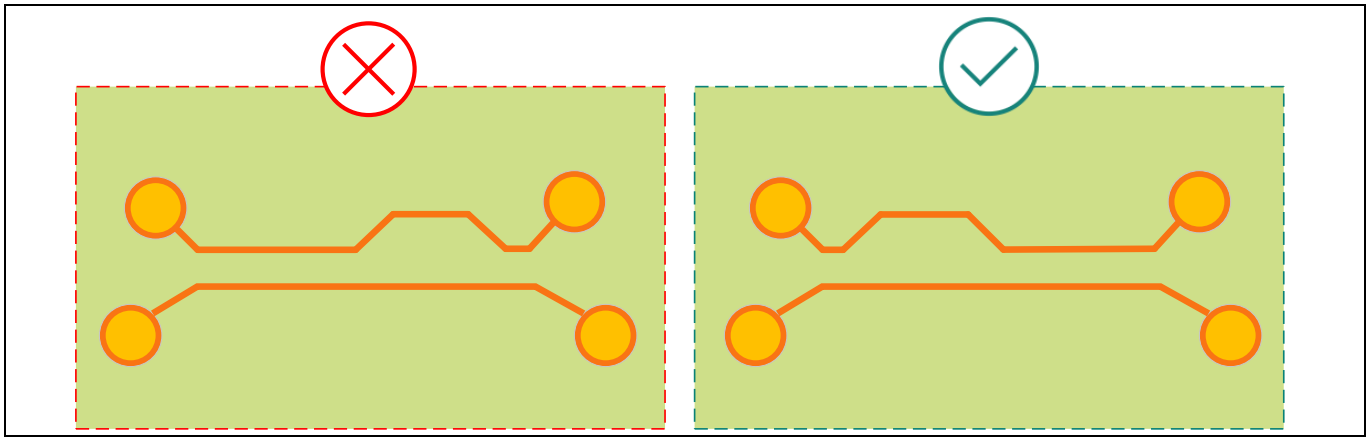

Figure 10 Add length correction near the mismatching point at the source

- Bends can also cause inconsistencies if the trace on the inner bend is smaller than the outer trace. In such cases, compensate the length close to the bend area as shown in Figure 11

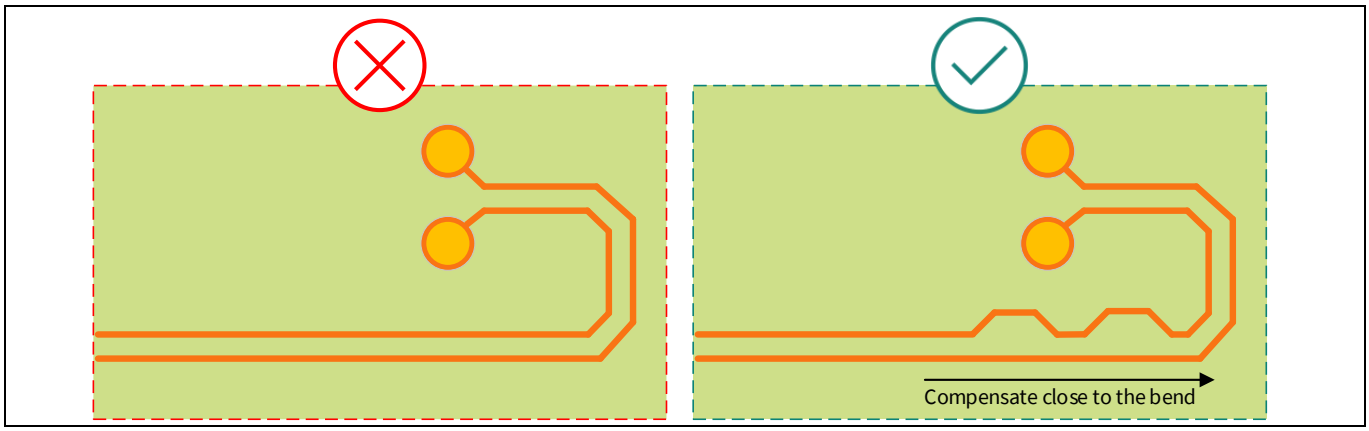

Figure 11 Place length compensation close to the bends

- Route both traces on the same layer to ensure equal signal speeds and a consistent dielectric constant. If a differential pair signal changes from one layer to another using vias and has a bend, each segment of the pair needs to be matched individually. In Figure 12, the vias separate the differential pair into two segments

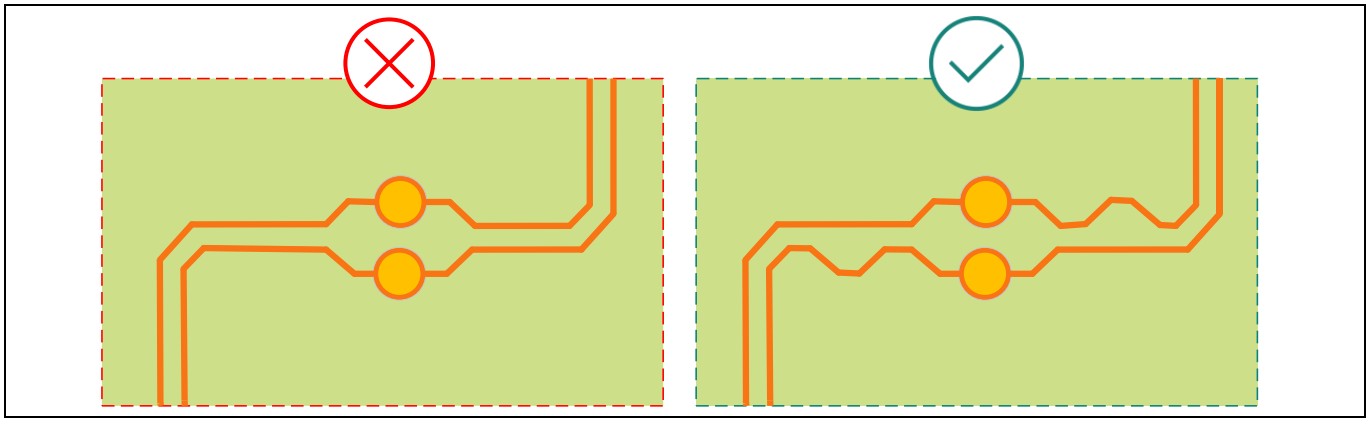

Figure 12 Compensate length differences in each segment of the trace

3.3.4 Reference planes

- Route the high-speed signals over a solid GND reference plane, as in Figure 13

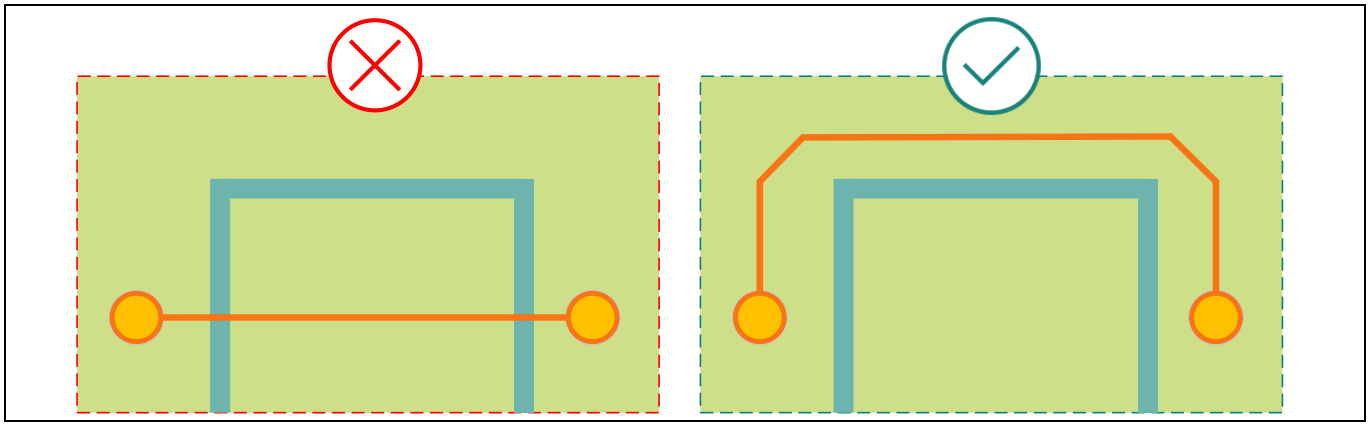

Figure 13 Avoid routing signals over split planes in high-speed PCBs

- If routing over a plane-split is unavoidable, place stitching capacitors (10 nF to 100 nF) across the split and place them as close as possible to the plane crossing, as in Figure 14

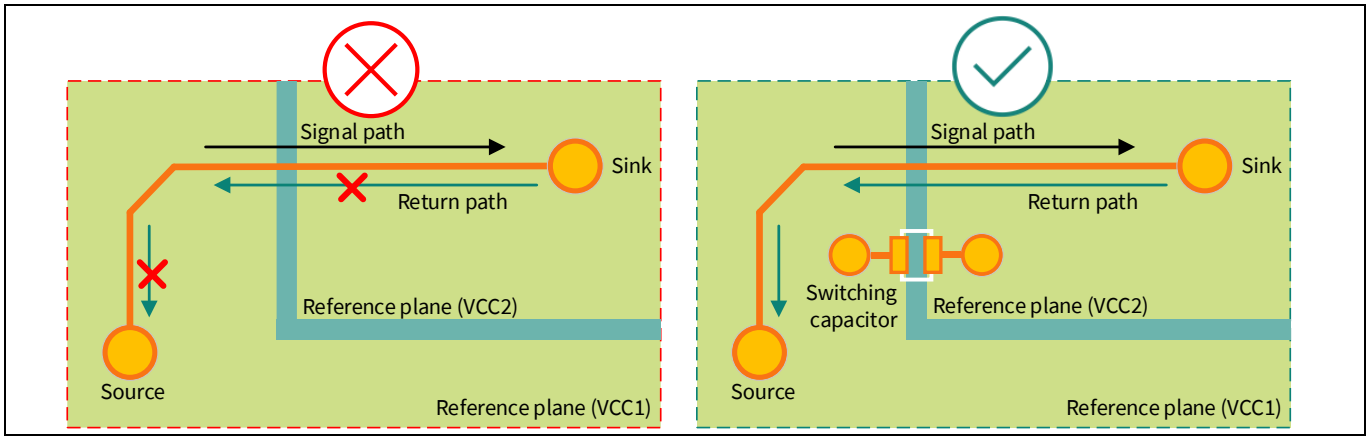

Figure 14 Use stitching capacitors when routing over a plane obstruction in high-speed PCBs

- Keep ground pours well away from differential pairs. If you must have them, use a clearance of three times the trace width
- Add dedicated ground vias close to the source and sink of the signal
  - Each signal via represents a discontinuity in the return path. Without a nearby ground via, the return current must take a long detour to reach the new reference plane

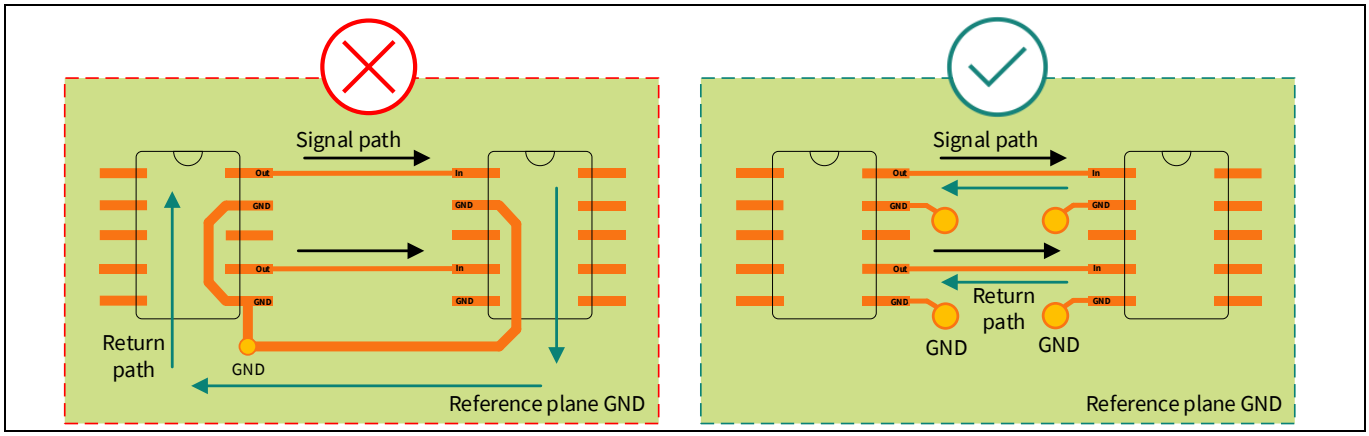

Figure 15 Consider the return path of the signals when placing ground vias

- To prevent unwanted capacitance, ensure planes that do not reference each other are not overlapped
- Use via-stitching for GND planes

3.4 Ground plane considerations

For radar PCBs using Infineon 60 GHz AIP MMICs, special attention must be paid to ground plane design. Every single-ended signal requires a GND reference.

3.4.1 Top layer ground pour

Attention: ***For radar AIP on the top side, it is better not to have any polygon pour there and minimize routing as much as possible. This differs from standard RF design practices where flooding everything with ground copper is common.***

3.4.2 Ground plane integrity

- Ensure solid ground reference planes for high-speed signals
- Avoid splits or voids in ground planes under signal traces
- Use stitching vias to connect ground planes when signals transition between layers
- Maintain ground plane continuity throughout the board
- No routing of any other signals should be implemented in a dedicated GND plane, typically layer 2
- Place multiple GND vias in larger GND areas
- Place GND vias along the PCB edges and RF traces for shielding

3.4.3 Ground return paths

- Keep ground return paths as short as possible
- Provide dedicated ground returns for critical signals
- Use ground vias near signal vias when transitioning between layers
- Consider the current return path for every signal trace

3.5 Power traces and planes

If there is enough space, use much wider traces, or whole copper areas in a power plane for supply signals to reduce inductance. This can be seen in all Infineon radar MMICs demo boards or reference designs PCBs.

3.6 Vias considerations

Improper via placement can disrupt current flow and create localized high-current density areas, known as “hot spots”. These regions increase impedance, generate heat, and impact power integrity.

To maintain an even current distribution, arrange vias in a uniform grid pattern rather than clustering them. A consistent via matrix allows current to flow continuously across the ground and power planes, minimizing voids and thermal buildup, as in Figure 16.

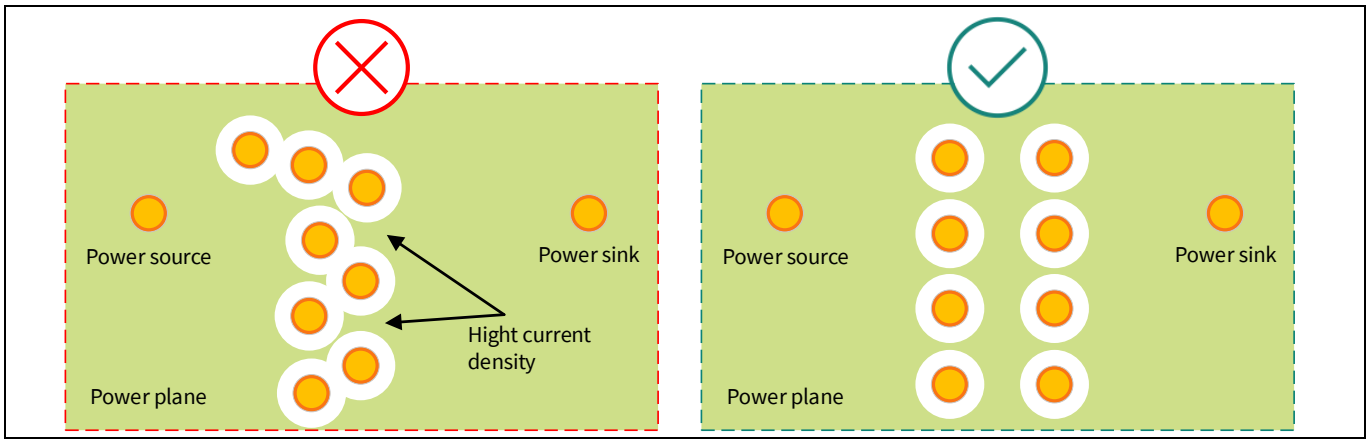

Figure 16 Place vias in a grid pattern to avoid hotspots

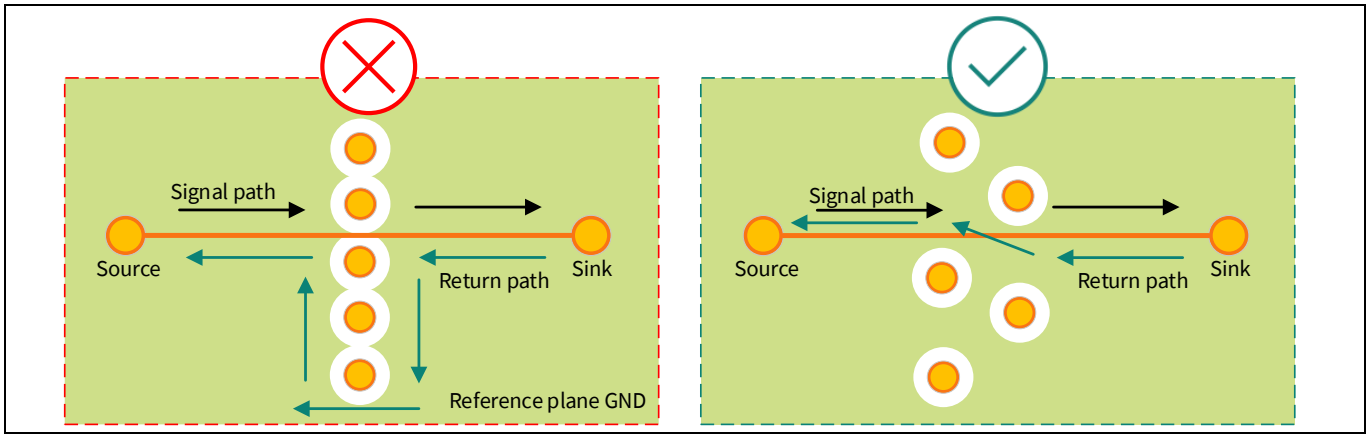

Figure 17 Maintain sufficient spacing between vias to avoid plane voids

4 Manufacturing considerations

Obtain the latest design rules document from your PCB manufacturer.

This document includes:

- Minimum trace width and spacing
- Minimum via and annular ring sizes
- Stackup availability and impedance tolerances
- Preferred materials (FR4, Rogers, Isola, etc.)

Note: For radar-frequency PCBs, choose a fabricator with RF expertise. Although it is not needed for Infineon AIP radar MMICs, the PCB manufacturer should support materials like Rogers RO4350B to make sure they have a higher quality standard.

4.1 Trace geometry

- **RF traces:** Target 50 Ω impedance (calculated from dielectric constant (Dk) and dielectric thickness)
- **Digital high-speed:** Differential pairs for SPI, I^2C, etc. (usually 100 Ω)
- **Power traces:** Short, wide paths with stitched ground return

4.2 Design for manufacturability

- Follow IPC Class 2 or Class 3 standards for high-reliability radar applications
- Maintain 100 µm minimum trace width and spacing or follow your manufacturer's recommendations
- Use standard drill sizes and via structures
- It is recommended to use as few different via sizes as possible. Using many different diameters can increase production time and cost, especially for blind vias
- Typical via sizes in Infineon AIP radar recommended boards are 0.4 mm diameter and 0.2 mm hole size. When possible, 0.6/0.3 mm is also used, especially for power and GND lines
- Consider panelization and breakaway tab placement

4.3 Design for testability

- Include test points for critical signals (outside of RF/antenna areas)
- Consider boundary scan or JTAG testing for complex designs
- Document test procedures and expected measurements
- Include power and ground test points

4.4 Final design review checklist

- Verify all MMIC AIP keep out zones are respected
- Confirm MMIC orientation matches intended field of view
- Check that all high-speed signals follow proper routing guidelines
- Verify power integrity with adequate decoupling
- Ensure mechanical fit with enclosure and mounting points
- Validate thermal management for all components

5 Electromagnetic (EM) simulations and FCC certification

5.1 EM simulations

Conducting 3D electromagnetic (EM) simulations of the PCB and housing is a useful step in verifying that the complete system meets its performance requirements. By examining the radiation pattern and gain, you can identify notches or gaps in the signal at specific field-of-view (FoV) angles. If the simulation results are not satisfactory, make minor adjustments to the PCB layout, such as relocating taller components further away from the AIP radar MMIC, which can be beneficial in mitigating these issues. Running a subsequent simulation can then confirm whether the modifications made to the PCB have effectively resolved the problems.

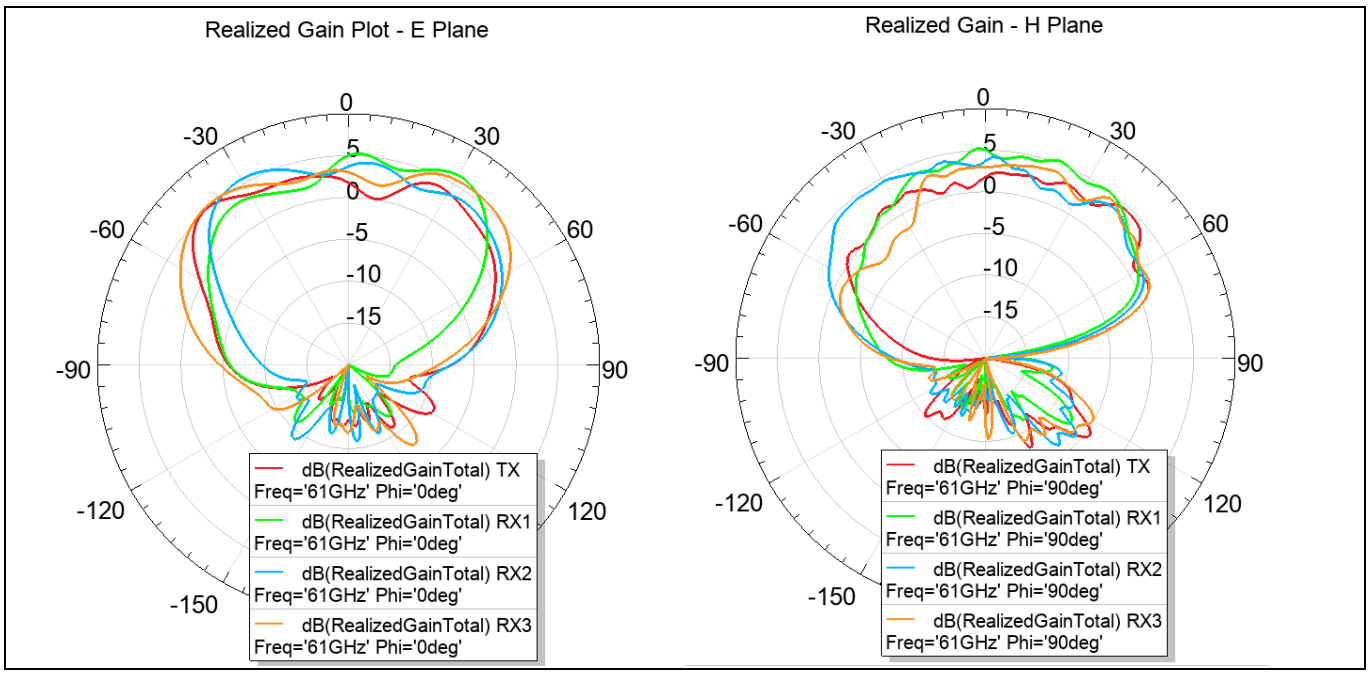

Figure 18 EM simulation on BGT60CUTR13AIP Wing board

5.2 FCC certification

Module certification is out of the scope of this document but see the EBG structures application note [1], which dives deep into this topic.

6 Infineon's XENSIV™ radar MMICs best practices

Infineon offers a range of boards and designs based on its radar MMIC. To select the right board, visit the product page of your selected MMIC and navigate to **Design resources** > **Boards and designs**. You will find demo boards, Wing boards, shields, or even reference designs. Select the board that best suits your application requirements, download the design files, and reuse them wherever possible. Ensure all BOM components are carefully chosen to maximize performance, particularly in critical areas like the power supply and oscillator sections. Using the same parts for these sensitive areas can help reduce development costs and accelerate time-to-market.

6.1 XENSIV™ BGT60CUTR13AIP radar

The XENSIV™ BGT60CUTR13AIP is an ultra-low-power 60 GHz radar sensor, manufactured with CMOS technology, offering a cost-effective solution compared to alternative technologies, making it ideal for budget-conscious consumer electronics.

6.1.1 Quick steps to improve the radar module

- Choose a PCB stack-up with a thin top prepreg to reduce the substrate modes
- Consider adding cutouts in the layout of the top metal to reduce the back-and-forth reflections in radar mode. Otherwise, use a complete top ground layer with shielding drills connecting all the metal layers on the PCB
- Reduce the components close to the radar chip
- Perform radar mode simulations to double check the linearity of the phase response in presence detection

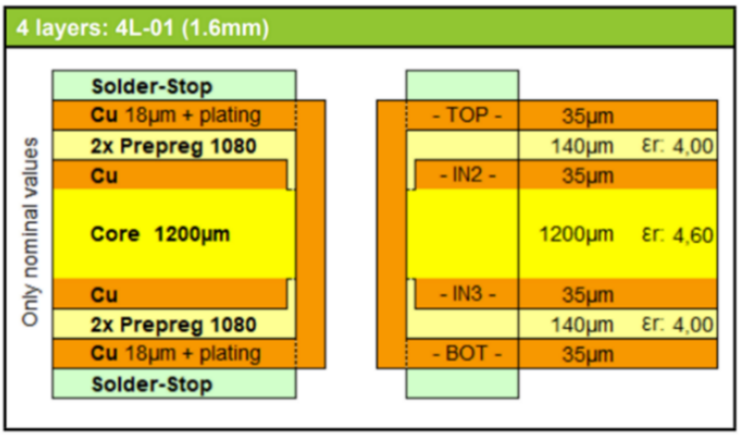

Figure 19 Layer stackup optimized for BGT60CUTR13AIP radar MMIC without EBG structures

6.1.2 Using electromagnetic bandgap (EBG) structures

To reduce the sensitivity of the radar sensor with integrated antennas towards the PCB design and to provide more consistent performance within a holder and radome, an EBG structure is adopted in the PCB layout. However, for ceiling mounted applications where the maximum FoV is preferred, like smart lighting, a PCB without EBG structures is preferred. The electromagnetic bandgap (EBG) is an RF structure tuned to the 60 GHz band, requiring a dedicated thickness and dielectric constant of the top dielectric layer. The EBG structure shown in Figure 20 has been optimized for the FR4 used PCB stackup. The top layer layout is shown in Figure 20, while the dimensions of the EBG structure are shown in detail in Figure 21.

The key dimensions of the EBG structure are as follows:

- Full through via hole size (d) of 0.2 mm (no blind vias)
- Distance between neighboring via center (p): 0.85 mm
- EBG pad dimension (w): 0.5 mm
- Layer thickness between top layer and ground layer beneath (l): 0.33 mm to 0.38 mm

For more information on electromagnetic bandgap, see the EBG structures application note [1].

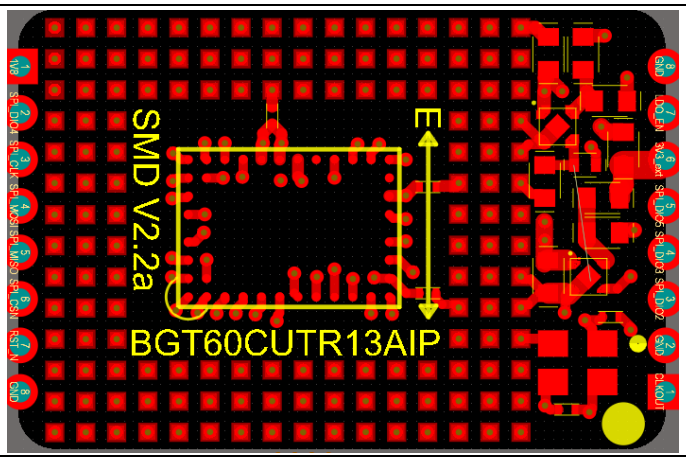

Figure 20 Top layer view of XENSIV™ BGT60CUTR13AIP SMD module layout

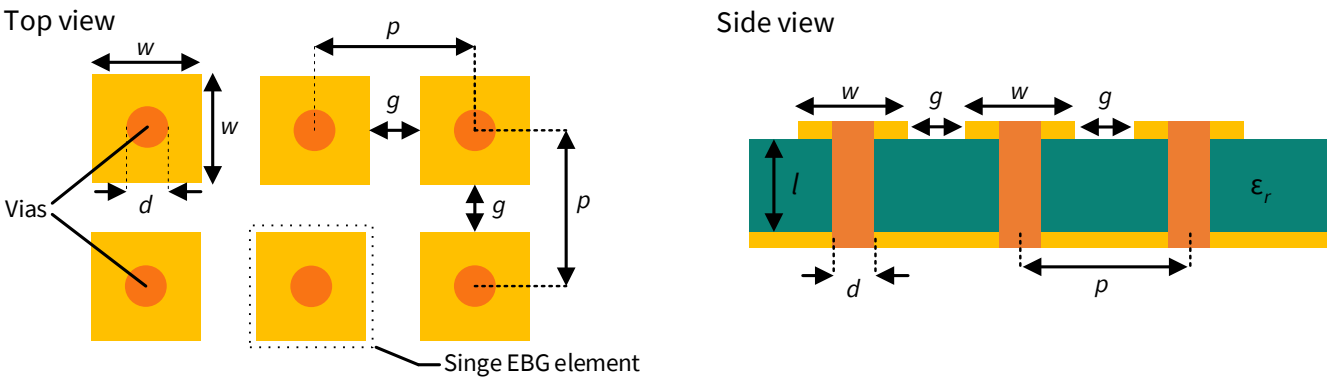

Figure 21 Grid of EBG elements with corresponding design parameters in top and side views

Note that the EBG design is only valid for a specific PCB layer stack defined by the substrate material underneath the EBG pads (described by its relative permittivity) and the thickness of this substrate layer. Deviations from one or both of these two parameters can impact the radiation characteristic of the individual antennas and overall sensor performance. The measured and demonstrated performance in this document can only be expected when using the identical PCB layer stack as shown in Figure 22.

The PCB layout consists of four metal layers. The top layer includes the radar MMIC together with the EBG structures. Layer 2 is mainly formed by a GND plane. Layer 3 is used for redistributing the signals and power supply. Layer 4 includes all other SMD components besides the radar MMIC. All vias are formed as through vias.

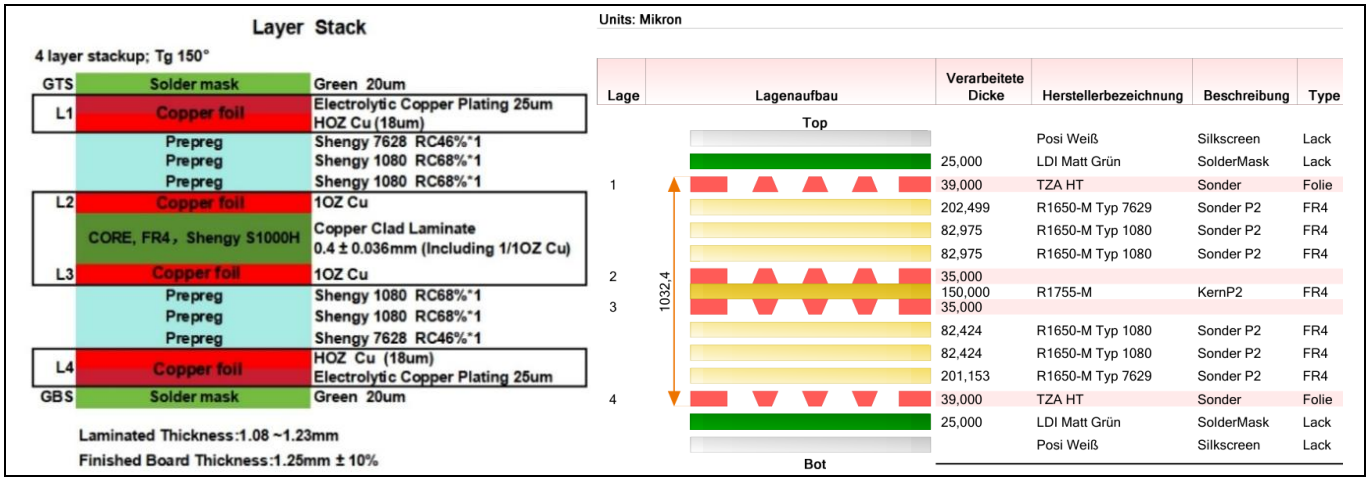

Figure 22 BGT60CUTR13AIP SMD module PCB layer stackup with EBG structures, with different laminates based on market availability and price

6.2 XENSIV™ BGT60UTR11AIP radar

The XENSIV™ BGT60UTR11AIP 60 GHz radar, with a total package size of only 4.05 mm², is very compact and comes integrated with 1 transmitter and 1 receiver antenna.

6.2.1 PCB design recommendations

The size of ground plane for the Antenna-in-Package (AIP) is limited by the BGT60UTR11AIP chip dimension. As a result, there will always be a portion of the RF signal interacting with the PCB structures around the BGT60UTR11AIP chip. In a few cases, this interaction will have an impact on the antenna radiation pattern. If it requires reducing this interaction, a special PCB design may be adopted, such as the EBG structure.

The structure of the EBG element design used for the RF shield can be seen in Figure 23. For more information about the EBG structures related to the BGT60UTR11AIP radar, see the shield user guide [2].

At least three rows of EBG elements in every direction around the sensor are recommended to provide a significant effect. Additional rows of EBG elements will further decrease the sensitivity of the radiation pattern towards the remaining PCB layout.

The EBG structure does not necessarily have to be part of every design. For many applications, reasonable performance has been demonstrated without EBG structures.

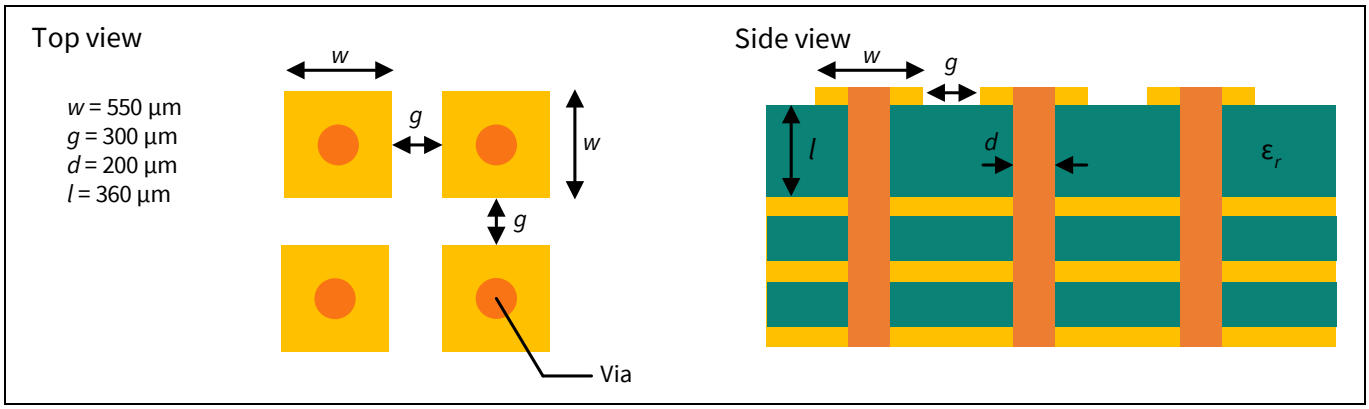

Figure 23 EBG geometry designed for 61 GHz on FR4 laminate

The transmitter antenna and the receiver antenna are located in a compact dimension of the radar package. A certain coupling level between the transmitter channel and the receiving channel usually cannot be avoided. Several measures can be implemented in the PCB design to further optimize the coupling behavior.

As shown in Figure 24, with the direct connections between PCB landing pads A1 and H8, together with the direct connection between pads A5 and D8, the Tx-Rx coupling of BGT60UTR11AIP shield V2.2 improves.

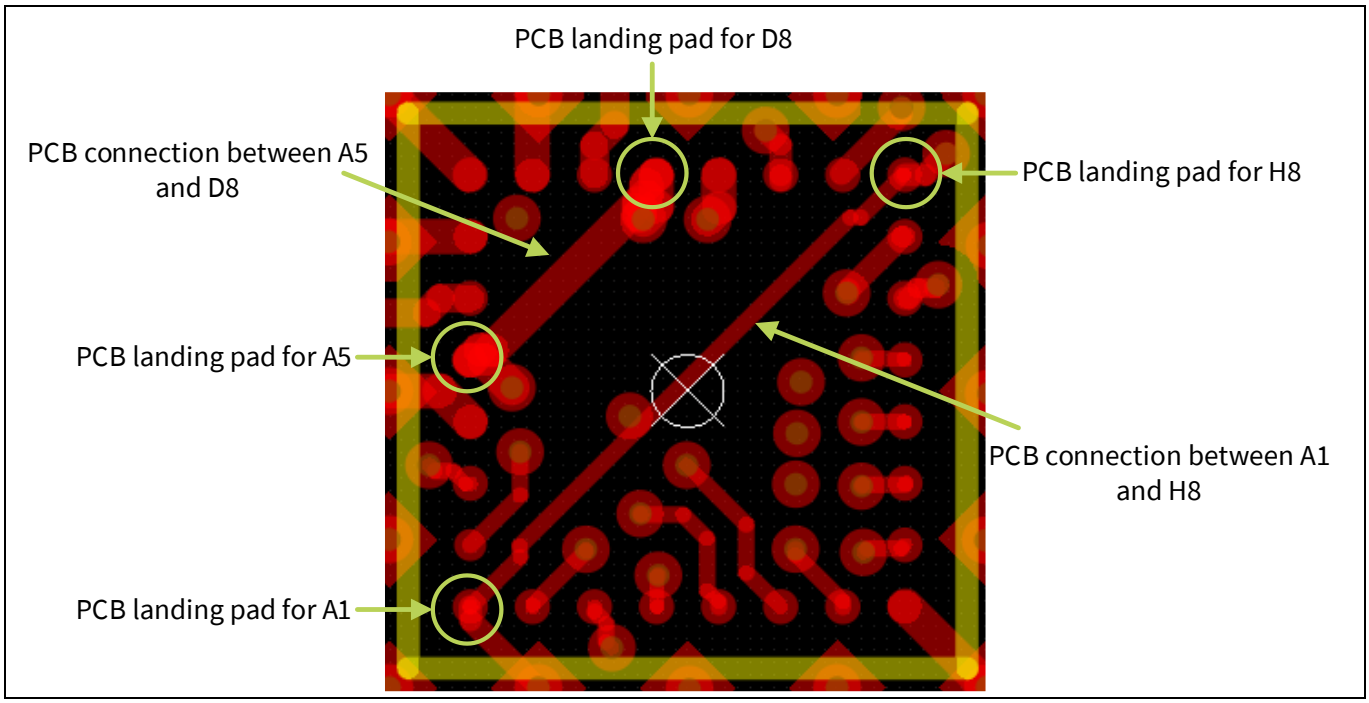

Figure 24 Ground landing pad connections underneath the BGT60UTR11AIP to improve Tx-Rx coupling

The cancellation of coupling relates to the inverted phase from different coupling paths. Hence, the variation in assembly and production may have an impact on the cancellation effect. The suggestion is to do pre-production evaluation to define the radar setting boundaries, such as the parameters of the high-pass filter and baseband gain.

6.3 XENSIV™ BGT60LTR11AIP radar

The XENSIV™ BGT60LTR11AIP is a fully integrated 60 GHz AIP radar with built-in motion and direction of motion detectors. It can operate autonomously, eliminating the need for an external microcontroller or additional signal processing. For longer range detection, adding a small M0 MCU can boost performance to achieve even better results.

6.3.1 PCB design recommendations

Depending on the use case, EBG structures are preferred. For example, for on-ceiling mounting scenarios, which are typically used for smart lighting. See the EBG structures application note [1] for more information on how to design the PCB with EBG structures for the BGT60LTR11AIP radar.

For other scenarios, a normal PCB without EBG structures is sufficient. For example, the BGT60LTR11AIP M0 reference design (REF_BGT60LTR11AIP_M0) is a good start for initial prototyping.

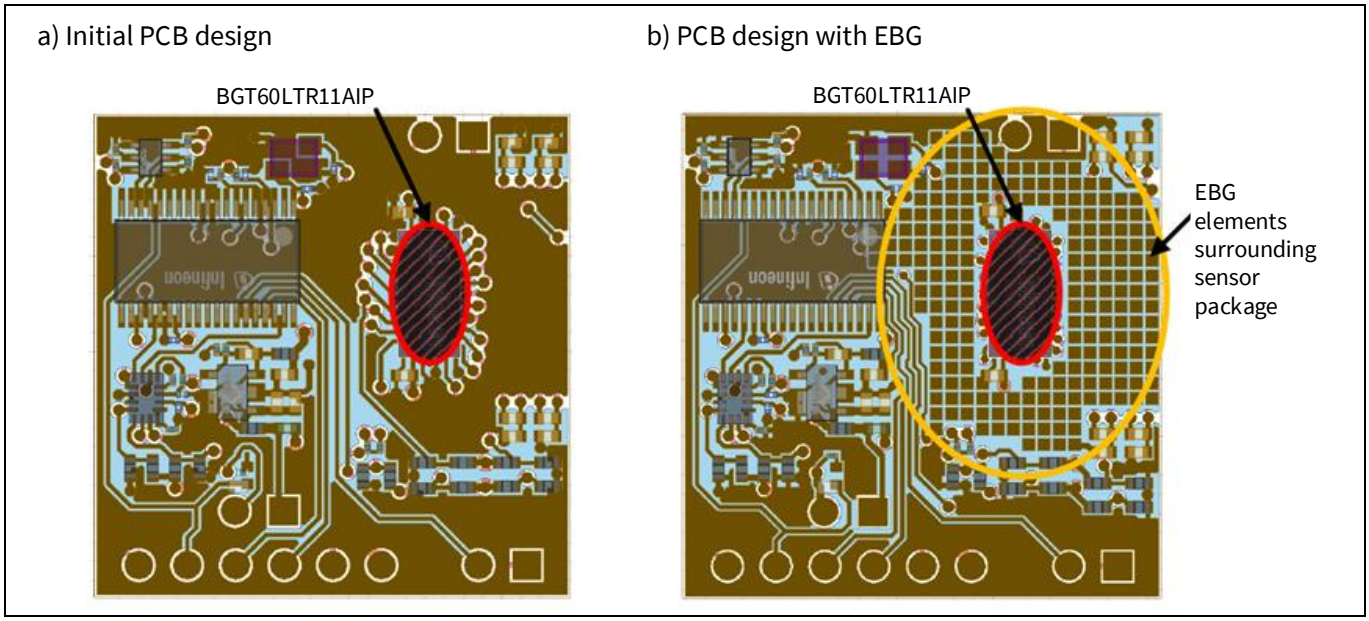

Figure 25 BGT60LTR11AIP M0 reference design with and without EBG structures

7 Related resources

- XENSIV™ 60 GHz radar sensors for IoT webpage
- Radar sensors developer community

References

[1] Infineon Technologies AG: *AN155366: Electromagnetic bandgap (EBG) structure application note;* Available online

[2] Infineon Technologies AG: *UG091947: BGT60UTR11AIP shield user guide;* Available online

[3] Texas Instruments: *High-Speed Interface Layout Guidelines (Rev. J); Dallas, TX; Texas Instruments; February 2023;* Available online

[4] Rahul Shashikanth: *10 Best High-Speed PCB Routing Practices; Sunnyvale, CA; Sierra Circuits; October 29, 2025*; Available online

[5] Infineon Technologies AG: *AN115231: FCC certification guide for radar modules application note;* Available online

[6] Infineon Technologies AG: *XENSIV™ BGT60CUTR13AIP MMIC user guide;* Available soon

Glossary

AIP
Antenna-in-Package (AIP)

Azimuth
horizontal field of view (Azimuth)

BGA
ball grid array (BGA)

BOM
bill of materials (BOM)

CMOS
complementary metal-oxide-semiconductor (CMOS)

Dk
dielectric constant (Dk)

DRC
design rules check (DRC)

EBG
electromagnetic bandgap (EBG)

Elevation
vertical field of view (Elevation)

EMI
electromagnetic interference (EMI)

ESD
electrostatic discharge (ESD)

FCC
Federal Communications Commission (FCC)

FoV
field of view (FoV)

FR4
glass epoxy laminate used in the fabrication of PCBs (FR4)

I^2C
Inter-Integrated Circuit communication protocol (I^2C)

MMIC
monolithic microwave integrated circuit (MMIC)

PCB
printed circuit board (PCB)

Radome
radar sensor enclosure or cover to protect the sensor or hide it from the product outlook (Radome)

Glossary

RF
radio frequency (RF)

RX
receive (RX)

S-G-S
signal-ground-signal (S-G-S)

Signal skew
time delay variation between multiple signals in a group (Signal skew)

SMD
surface-mount device (SMD)

SPI
Serial Peripheral Interface (SPI)

SRR
short-range radar (SRR)

SW
software (SW)

TX
transmit (TX)

XENSIV™
Infineon's broad portfolio of sensor solutions for automotive, industrial, and consumer applications (XENSIV™)

Revision history

Document revision	Date	Description of changes
1.00	2026-06-24	Initial release

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