Gate driving techniques for paralleling discrete SiC MOSFETs

Gate resistor configurations, switching-loss balancing, and oscillations

About this document

Scope and purpose

Driving paralleled discrete CoolSiC™ MOSFETs can be more complicated than driving single devices. Along with switching-losses or current imbalance, there can also be some severe oscillations. Additionally, paralleled devices offer more options to configure the gate resistors: for example, two paralleled devices can be driven either with a common gate resistor or with two individual resistors. This application note describes the key challenges like oscillations and gate resistor configurations and their solutions when driving paralleled devices.

Intended audience

This document is intended for power electronic engineers who are interested in driving paralleled CoolSiC™ MOSFETs with EiceDRIVER™ driver ICs, especially in terms of gate resistor configurations.

Keypoints

- Explains how gate-resistor configurations influence oscillations and switching-loss behavior in paralleled CoolSiC™ MOSFETs
- Describes measurement methods used to evaluate DM and CM oscillations and switching-loss imbalance mechanisms
- Highlights practical tradeoffs between DM oscillations and switching-loss imbalanceProvides design guidance for selecting R_i and R_c values to enable stable, low imbalance operation when driving paralleled CoolSiC™ MOSFETs with EiceDRIVER™ ICs

About this product family

Product family

EiceDRIVER™

Infineon's EiceDRIVER™ isolated gate drivers deliver high output current, fast and tightly matched propagation delays, and robust CMTI for demanding power applications. They support a wide gate-voltage range, enabling bipolar operation with negative gate voltages making them ideal for driving advanced SiC MOSFETs and GaN power switches.

Target applications

- Photovoltaic
- Solide-state transformer (SST)
- Uninterruptible power supplies (UPS)
- EV charging
- Server power supply units (PSU)

About this product family

Product family

CoolSiC™

Infineon's CoolSiC™ MOSFET offer exceptional performance in switching behavior and total losses. These devices are designed to offer high efficiency and optimal reliability, while also boasting a low on-resistance that remains stable and reproducible even in large-scale production. Its ability to turn off the device with zero gate bias makes the CoolSiC™ transistor concept the only true "normally-off" device.

Target applications

- Energy Storage Systems
- Industrial drives
- Motor control and drives
- Renewables
- UPS

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1 Introduction

1.1 Key challenges of paralleling CoolSiC™ MOSFETs

When paralleling discrete CoolSiC™ MOSFETs, it is crucial to have a good balance of the drain-source current and power losses among the devices. The drain current can be divided into two:

- **Static current**, primarily dependent on the on-state-resistance (R_{dson}) of CoolSiC™ MOSFETs
- **Dynamic current**, largely dependent on the dynamic parameters such as threshold voltage (V_{th}), gate capacitance (C_{gs}), and transconductance (g_{fs})

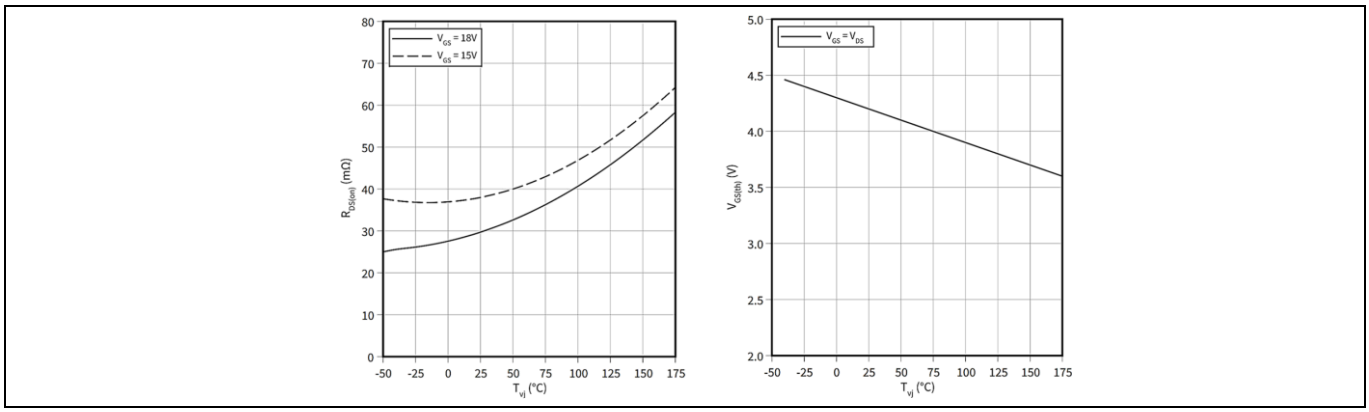

Figure 1 Typical temperature dependence of R_{dson} and V_{th} [1]

As shown in Figure 1, the R_{dson} shows a positive temperature coefficient (PTC), which enables the static current in paralleled devices to self-balance. However, the threshold voltage (V_{th}), which is a significant parameter of dynamic properties, has a negative temperature coefficient (NTC). This makes the dynamic current balancing more challenging. Moreover, if the circuits are not configured properly, there can be additional undesired oscillations leading to gate voltage instability and EMI problems.

Theoretically, each paralleled device can be driven by an individual gate driver, where all the driving circuits are independent. However, the propagation delay time of the gate drivers always vary from part to part, which could cause a timing mismatch and generate more imbalances in dynamic current and switching loss.

Therefore, it is recommended to drive the device with a single gate driver, where there could be different ways to configure the circuit. Figure 2 shows three methods to drive the gate of two paralleled devices, where the main difference is the resistance on the individual gate path [2].

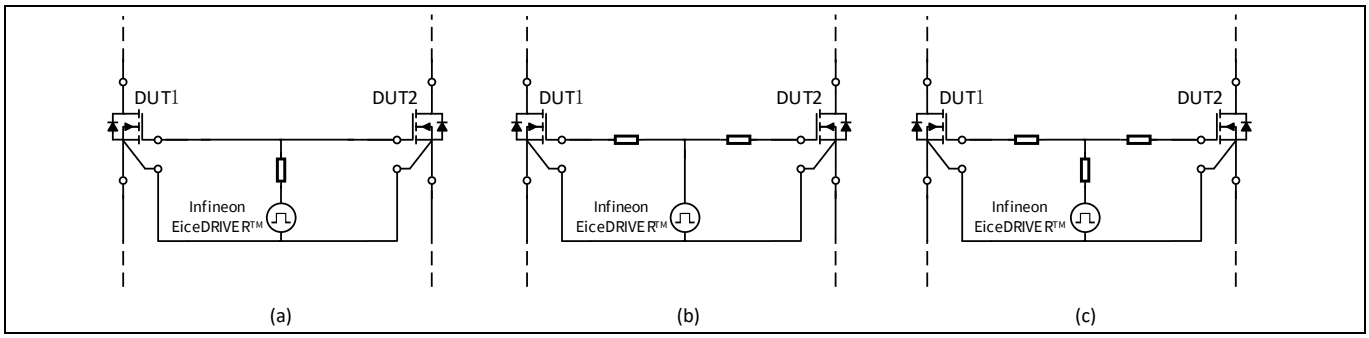

Figure 2 Three approaches to configure the gate resistors

1.2 Test and measurement details

To experimentally evaluate the current and switching-loss imbalance, a double-pulse-test platform for paralleled devices is developed, where waveforms of the paralleled devices can be measured at the same time.

To achieve faster switching and lower switching-losses, the 4-pin discrete device was selected. The chosen device is a 1.2 kV, 30 mΩ CoolSiC™ MOSFET, IMZA120R030M1H [1]. EiceDRIVER™ 1ED3124MU12F is a single-channel gate driver [2], which can supply up to 14 A peak output current to ensure more than sufficient driving current.

The PCB is designed with symmetric paths for paralleled devices to ensure that the layout is matched. The gate driver is designed on an individual board, which allows the gate resistors to change conveniently.

Figure 3 shows the test setup. All measurements were conducted at room temperature.

Note: Unless otherwise specified, the tests described in this application note were performed with V_{DC} = 800 V and I_{DC} = 70 A.

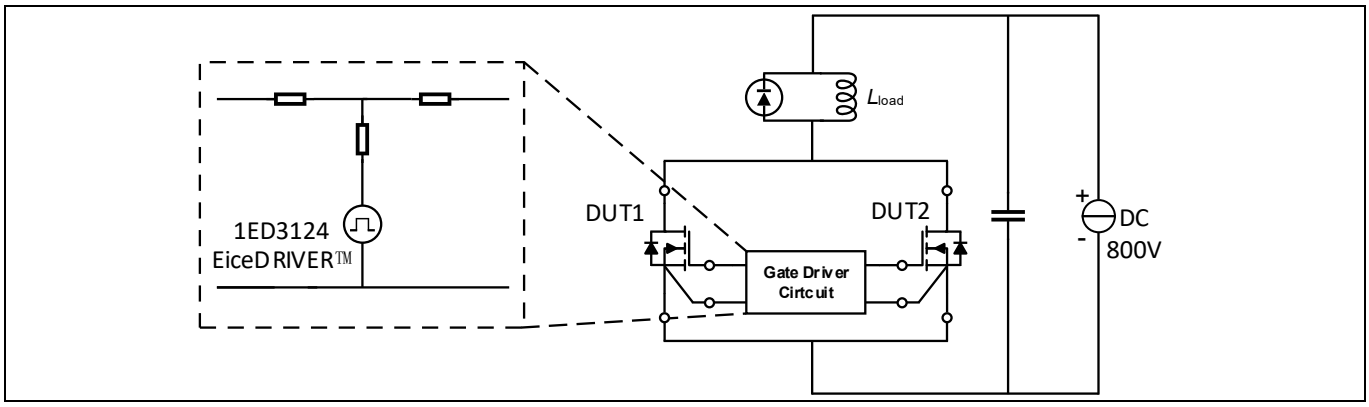

Figure 3 Double-pulse-test platform diagram

A hundred devices available from the market are characterized by the curve tracer to measure their transfer characteristics. The data is presented in Figure 4, which illustrates the spread of the measured transfer characteristics, providing a visual representation of the device-to-device variation.

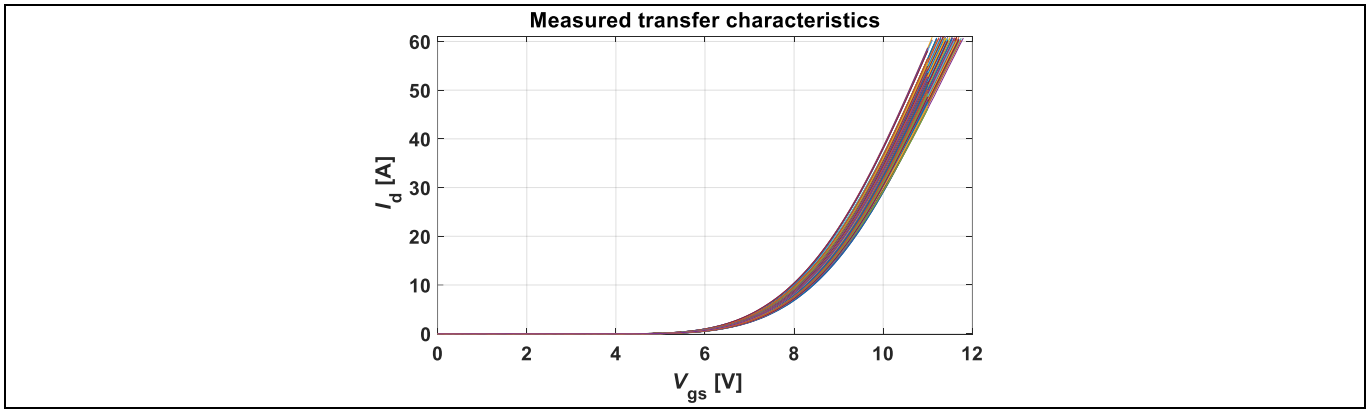

Figure 4 Spread of the transfer characteristics

The matched devices are selected by calculating the difference of their transfer curves, which is based on the method mentioned in paper [5].

2 Oscillations in paralleled discrete CoolSiC™ MOSFETs

2.1 Distinguishing two kinds of oscillations

When driving a single hard switching CoolSiC™ MOSFET, there could be oscillations during the turn-on as well as turn-off transients, which are mainly caused by the stray inductances and parasitic capacitances [7]. Usually, these oscillations are also called switching ringing. Figure 6 shows a typical waveform of the drain-source voltage and drain current during the switching transient, where oscillations can be seen after the rising or falling edges.

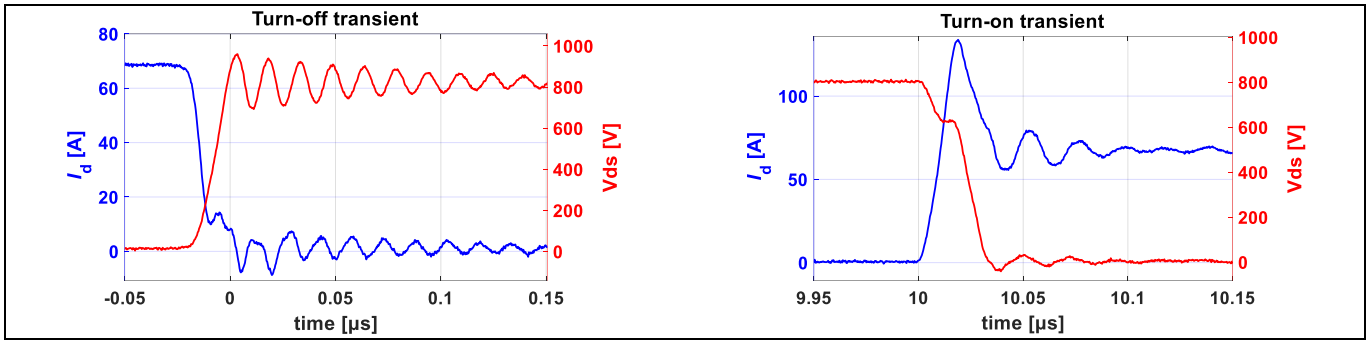

Figure 6 Measured switching waveforms during turn-on and turn-off for a single switch (R_g = 10 Ω)

The other kind of oscillation superposed on the switching ringing could lead to severe EMI and instability problems. Figure 7 (a) shows a case where oscillation occurs between the paralleled devices. The frequency is higher than the switching ringing mentioned above. Moreover, in extreme situations, as shown in Figure 7 (b), the gate voltage of both devices could become unstable and oscillate with a very large amplitude.

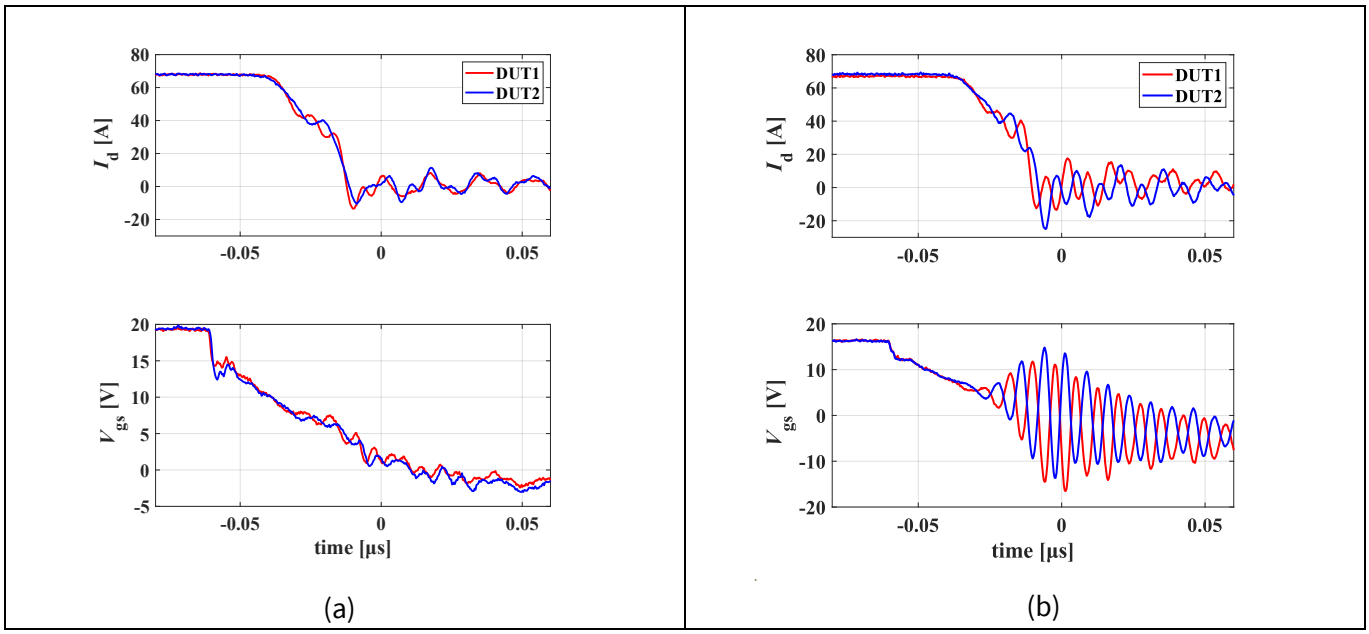

Figure 7 Measured waveforms in two different cases during turn-off for paralleled switches (R_g = 10 Ω per switch)

Furthermore, the drain-source currents though both devices can be decomposed into differential mode (DM) and common mode (CM) current by the following equations:

$$I_{\mathrm{d_CM}} = \frac{I_{\mathrm{d1}}+I_{\mathrm{d2}}}{2}, I_{\mathrm{d_DM}} = I_{\mathrm{d1}} - I_{\mathrm{d2}}$$

Equation 1

The CM current can be seen as the average of the drain-source current through both devices, where the DM current represents their difference. Figure 8 shows the extracted DM and CM components from Figure 7. It is clear that the CM current is similar to the switching ringing and contributes the main part of the transient current, whereas the differential mode current is oscillating near zero, meaning that there is an oscillation between the devices.

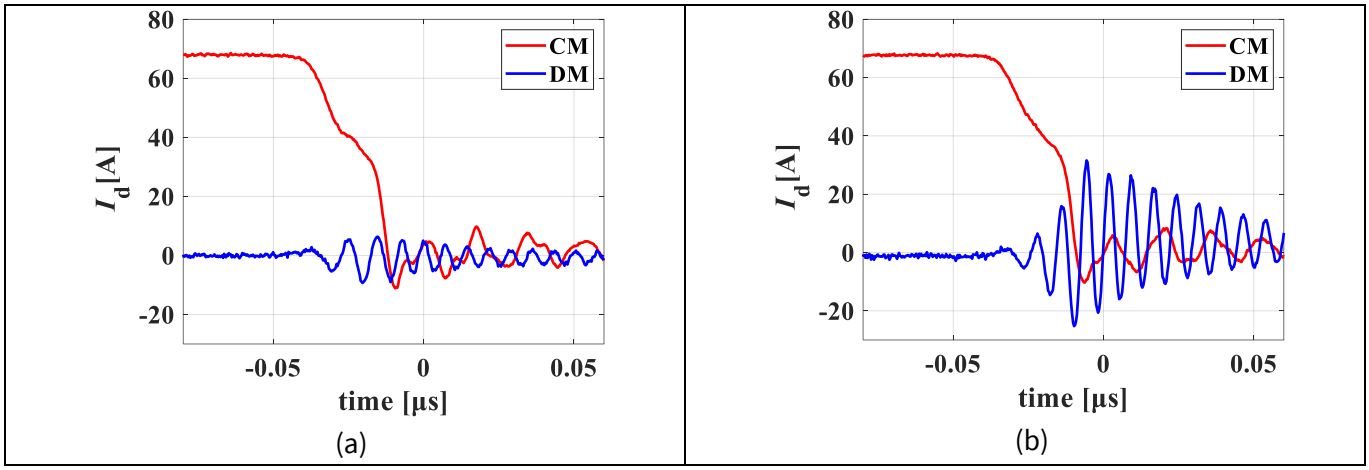

Figure 8 Extracted DM and CM current from Figure 7

2.2 Gate resistor configuration vs. switching oscillations

As mentioned in Section 2.1, the CM oscillation can be seen as switching ringing and is mainly caused by the loop stray inductance and the junction capacitance. On the other hand, according to [6], the DM oscillations arise from the unstable loop formed by the circuit parameters and can be mitigated by increasing the gate branch impedance or decreasing the source and Kelvin source branch impedance. Furthermore, DM oscillations are more prone to occur during turn-off than turn-on events, as a static current difference may already exist when the turn-off process starts. Figure 9 shows the comparison of two different gate resistor configurations. The measurements are done with matched device but with an asymmetric gate path created by bending the gate pin on one device.

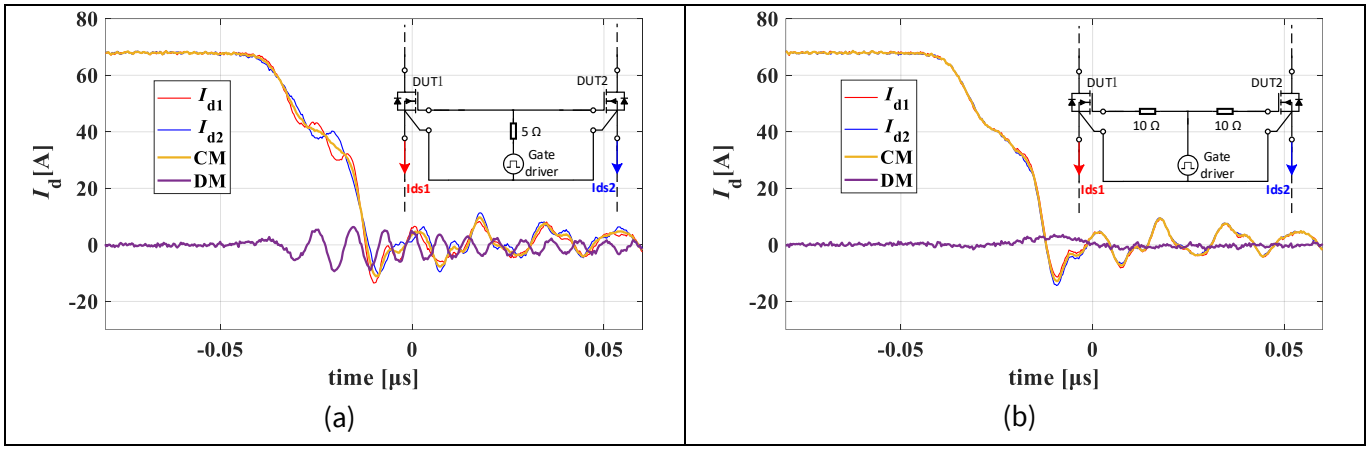

Figure 9 **Comparison of DM and CM oscillation with different gate resistor configurations (R_g = 10 Ω per switch)**

As shown in Figure 9, driving devices with individual gate resistors can damp the DM oscillation while the CM oscillation does not show an essential difference.

3 Switching-loss balancing in paralleled CoolSiC™ MOSFETs

This chapter presents a comparative analysis of the measurement results to show how different gate resistor configurations impact the imbalance in switching loss originating from various mismatches in the circuit such as stray inductance, device transfer characteristics, and gate-source capacitance (C_{gs}). Other parameters like gate-drain capacitance (C_{gd}) and drain-source capacitance (C_{ds}) are not considered in this work, because they normally don't exhibit a large variation [7].

3.1 Switching-loss imbalance caused by unmatched stray inductance

To emulate layout imbalances, the effective length of the device pin was increased by bending it. Figure 10 shows an example of this method, where the drain terminal of the device is bent to create extra stray inductance. This was applied individually to each pin of the DUT in the measurements.

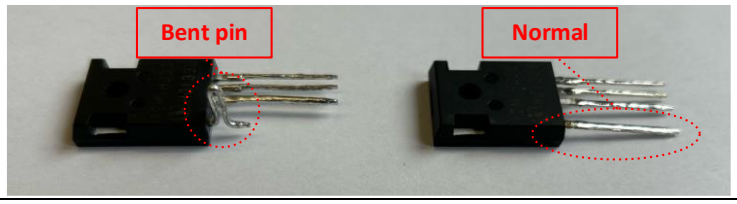

Figure 10 An example of a bent pin to add extra stray inductance in the loop

The extra stray inductance created by this method is extracted by Ansys Q3D. The estimated value is around 4.75 nH at 1 MHz for the drain and source pin, and 5.77 nH for the gate and Kelvin source pin as they are thinner. Figure 11 shows the diagram of the measurement in this section. The DUTs used in this section are matched devices. By bending different device pins, additional stray inductance is applied to different paths, allowing for the evaluation of their impact on the switching behavior.

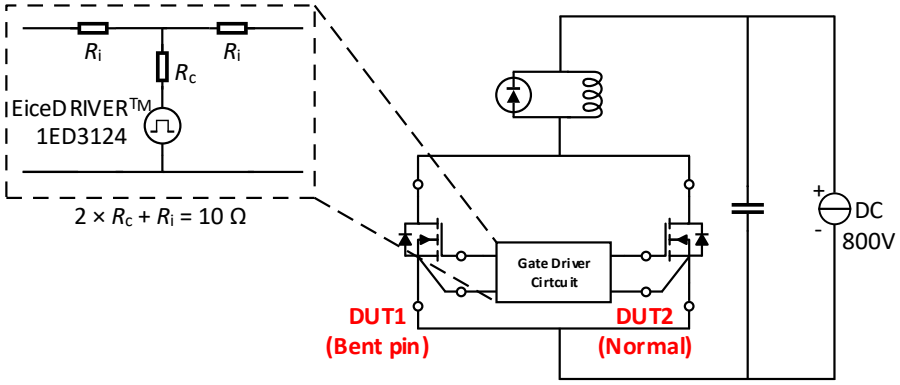

Figure 11 Diagram of the measurement with asymmetric stray inductance

Various gate resistor configurations are achieved by varying the value of R_i from 0 Ω to 10 Ω while keeping the total equivalent gate resistor value at 10 Ω per switch.

Figure 12 shows the relation of the extracted relative difference of the turn-on and turn-off losses between paralleled devices, where no evident correlations were found between R_i and imbalances in switching loss. This implies that using different gate resistor configurations does not essentially help in reducing the switching-loss imbalance caused by unmatched stray inductances.

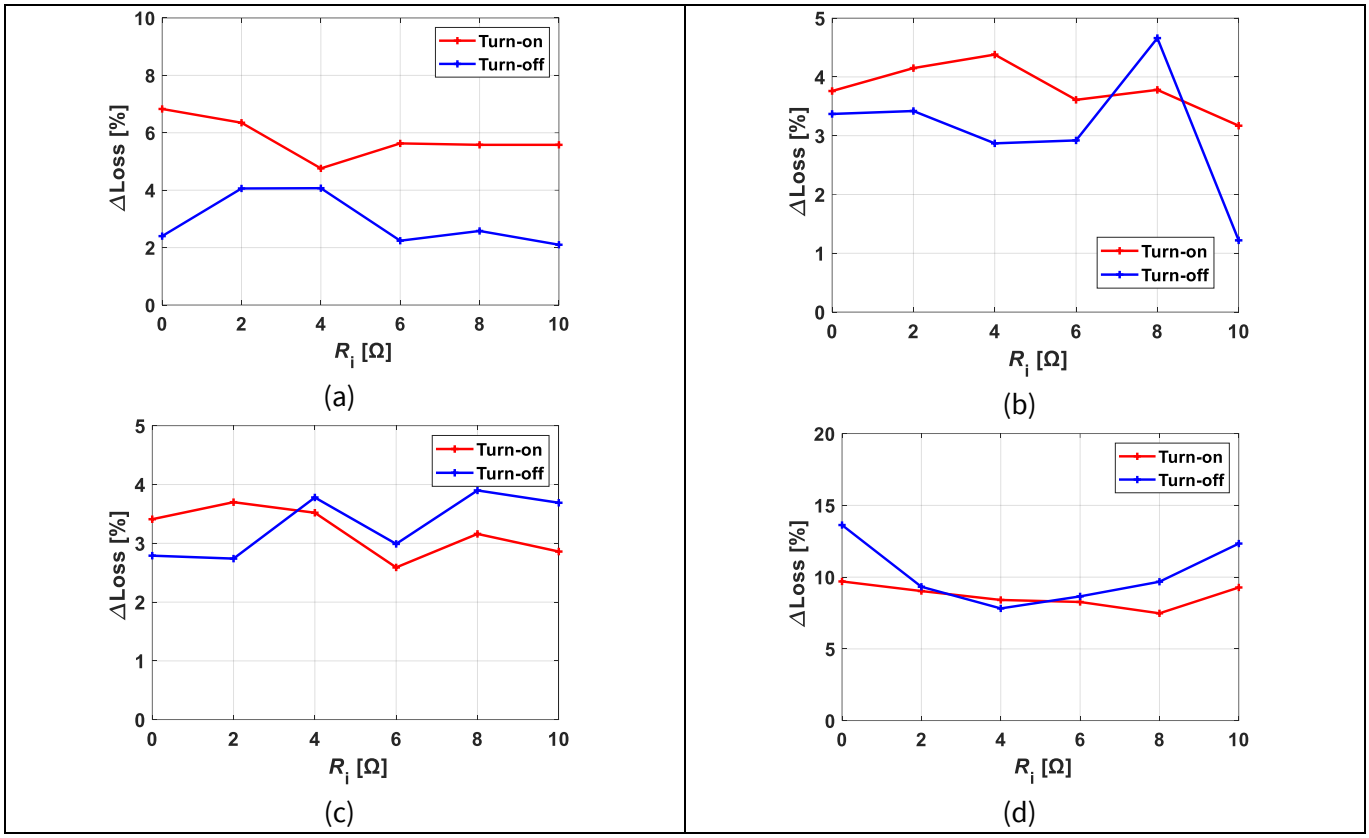

Figure 12 **Extracted relative switching-loss difference vs. R_i with: bent gate terminal (a), bent Kelvin source terminal (b), bent drain terminal (c), and bent power source terminal (d)**

3.2 Switching-loss imbalance caused by unmatched device transfer characteristics

In this part, the devices with different transfer characteristics are soldered onto the PCB. All other factors like PCB layout are kept symmetric. Figure 13 shows the diagram of the measurements in this section.

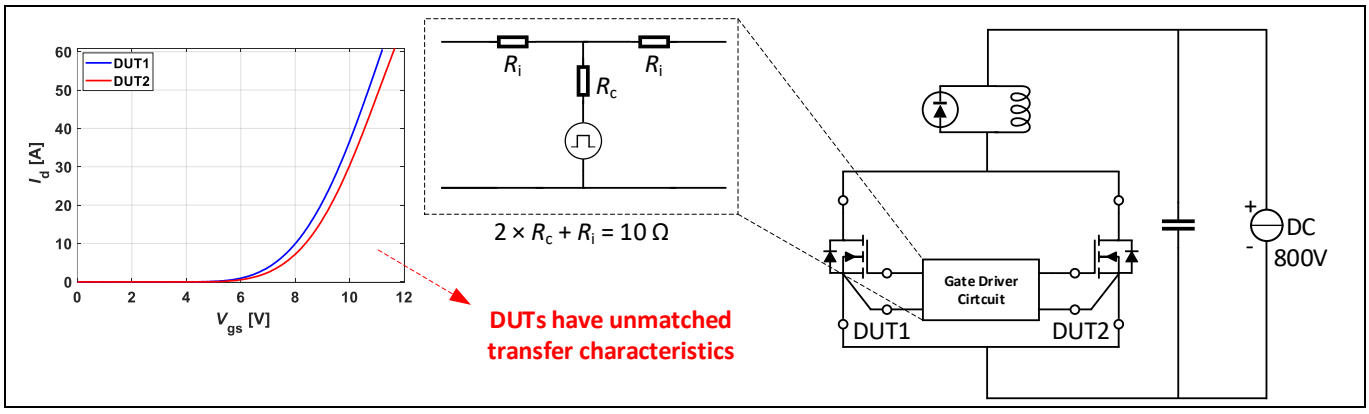

Figure 13 **Simplified diagram of the measurement with unmatched transfer characteristics**

The extracted results are presented in Figure 14. No evident correlations were found between R_i and switching-loss imbalances.

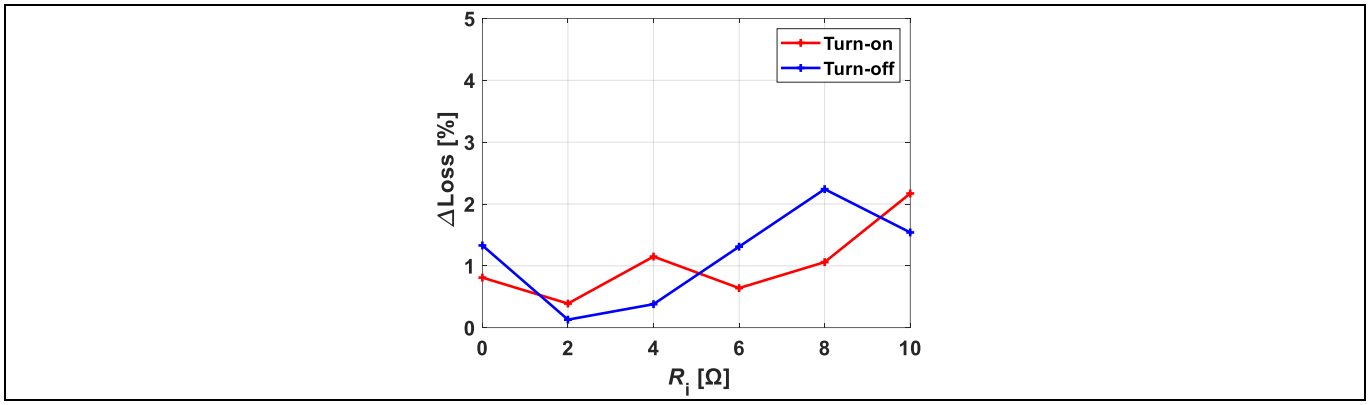

Figure 14 **Extracted relative switching-loss difference vs. R_i with unmatched device transfer characteristics**

3.3 Switching-loss imbalance caused by unmatched gate-source capacitance

To emulate imbalance on the gate capacitance, external SMD capacitors are directly soldered between gate and Kelvin source pin of pre-selected, matched devices. This allows a controlled introduction of capacitance mismatch. The measurement diagram is shown in Figure 15.

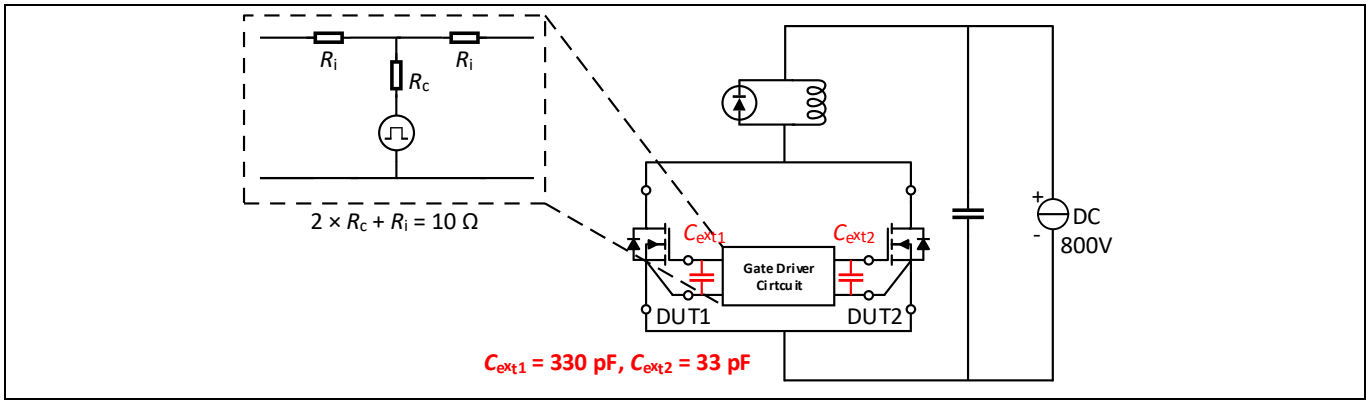

Figure 15 **Diagram of the measurement with unmatched gate capacitance**

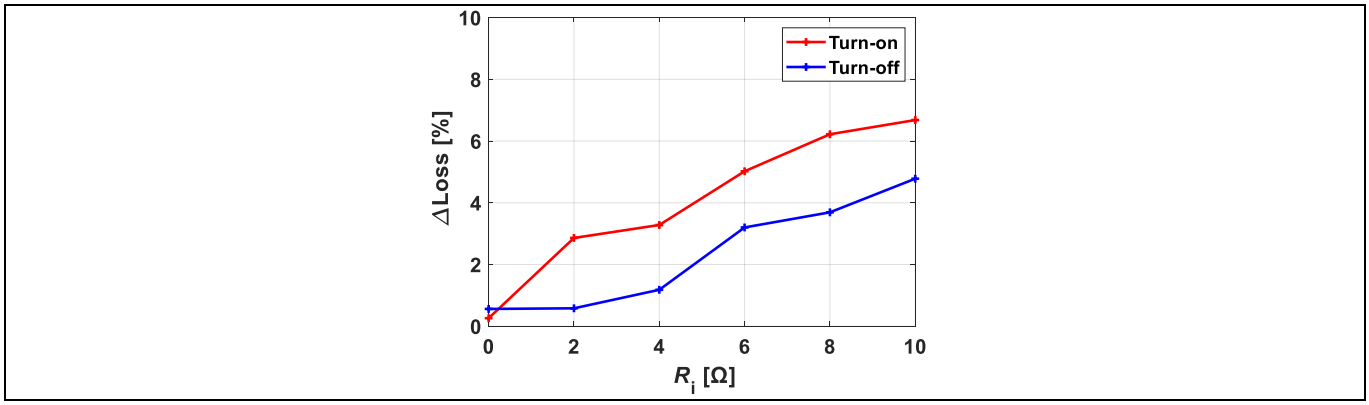

Figure 16 **Extracted relative switching-loss difference vs. R_i for different gate capacitances**

Figure 16 shows the extracted results. A positive correlation can be seen, which indicates that the higher R_i is, the more switching-loss imbalance is produced by unmatched C_{gs}.

This phenomenon is caused by the different time constants of the RC (R_i-C_{gs}) circuit. As shown in Figure 17, where the parasitic parameters are neglected, the switching transient can be simplified into two stages (blue paths and red arrows).

The first stage is to charge the gate capacitance, which results in the increase of the V_{gs}, while the second stage "maps" the V_{gs} into I_d. For a given difference on the gate capacitance, a higher R_i results in a greater difference in time constants, which leads to a more pronounced dynamic difference in $V_{gs.}$ As a result, this increased difference in V_{gs} causes a greater imbalance in current and subsequently, more imbalance in switching loss.

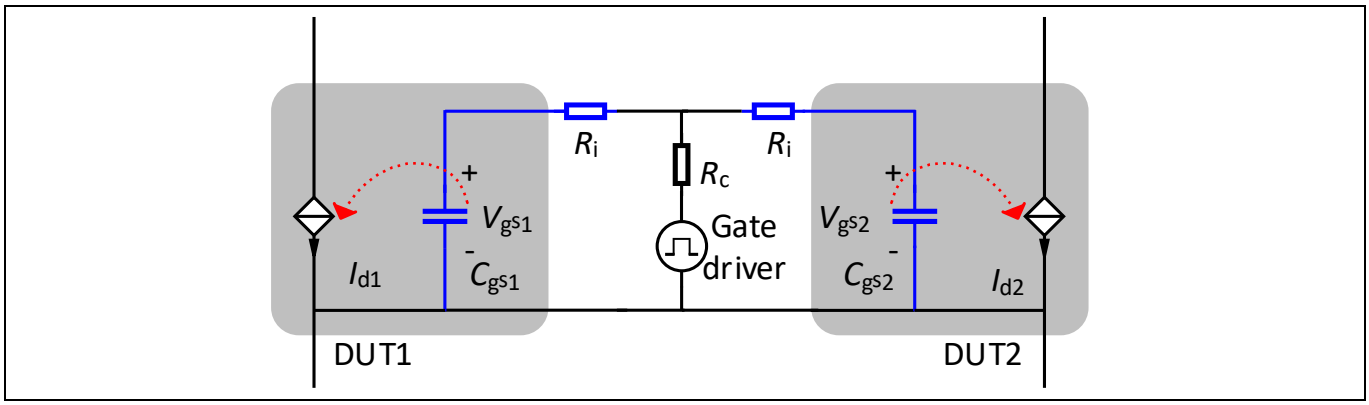

Figure 17 A simplified model of driving paralleled devices

4 Design recommendations for driving paralleled discrete CoolSiC™ MOSFETs with EiceDRIVER™ ICs

Based on the measurement and analysis presented above, recommendations can be concluded for configuring the gate resistors for paralleled CoolSiC™ MOSFETs.

When configuring the gate resistors to drive paralleled devices, the key consideration is the resistance on the individual gate path (R_i). Figure 18 shows the tradeoff when deciding the value of R_i.

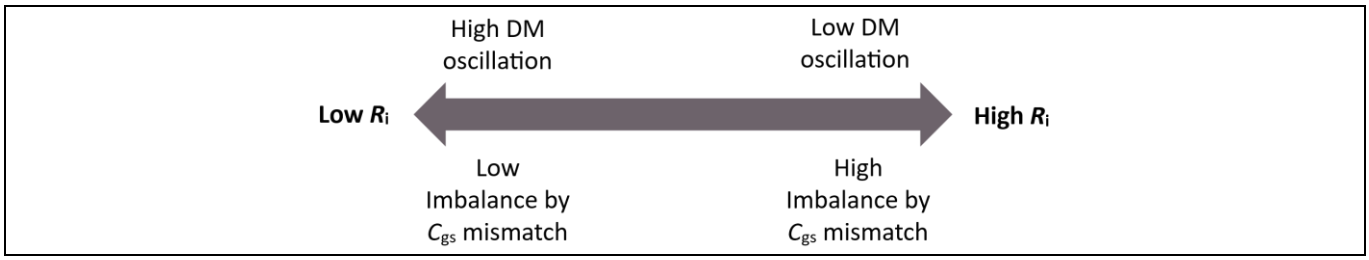

Figure 18 Tradeoff when setting the R_i value

A higher impedance on the gate path helps in suppressing the DM oscillations but could lead to more imbalance on switching losses caused by unmatched gate-source capacitance. On the other hand, a lower impedance on the gate path helps in mitigating the impact of difference in C_{gs} on the switching-loss imbalance but could introduce more DM oscillations into the circuit. Therefore, it is recommended to configure the gate resistors in a "hybrid" way, and to use the lowest R_i to damp the DM oscillations. The recommended procedure is shown in Figure 19.

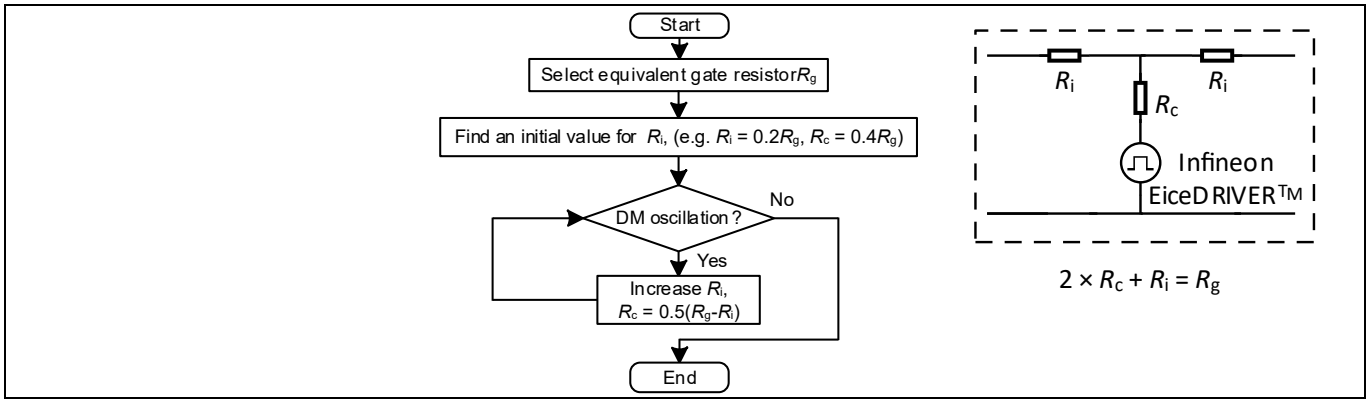

Figure 19 Recommended procedure to configure the gate resistors

In real applications, the paralleled devices should be pre-selected, and show "matched" characteristics, and the layout as well as the circuits should be as symmetrical as possible. An evident imbalance in the paralleled devices shouldn't exist initially. Therefore, after determining the equivalent gate resistance (R_g) per device, the first consideration is to minimize and suppress the possible DM oscillations.

As a rule of thumb, if $R_i > 0.2R_g$, the DM oscillation should be damped to a low enough level. However, DM oscillation is largely dependent on concrete circuit parameters such as stray inductance. It is still suggested to test the specific application and layout to find the optimal value. Then, the remaining resistance from R_g should be assigned to R_c to minimize the switching-loss imbalance caused by the potential mismatch such as difference on the C_{gs}.

5 Summary

This application note discussed the influence of the gate resistor configuration on driving paralleled discrete CoolSiC™ MOSFETs with the EiceDRIVER™ driver ICs. The key factor is the resistance on the individual gate path (R_i), where a tradeoff exits. A higher R_i helps to damp DM oscillations and hardly impact the CM oscillations. However, higher R_i makes the switching-loss imbalance more susceptible to mismatch like difference on C_{gs}. Therefore, after ensuring that DM oscillation is well suppressed, R_i is recommended to be as small as possible to mitigate the impact of possible mismatch on switching-loss imbalance.

6 Related resources

- EiceDRIVER™ gate driver IC webpage
- CoolSiC™ MOSFETs webpage
- Gate drive for power MOSFETs in switching applications application note

References

[1] Infineon Technologies AG: *IMZA120R030M1H CoolSiC™ 1200V SiC Trench MOSFET datasheet*; Available online

[2] Infineon Technologies AG: *EiceDRIVER™ 1ED312xMU12F Compact datasheet*; Available online

[3] Infineon Technologies AG: Gate drive for power MOSFETs in switching applications; Available online

[4] IEEE: *Impact of Gate Resistor Configurations on Current Balancing in Paralleled SiC MOSFETs*; Available online

[5] IEEE: *Influence of SiC MOSFET Gate Technologies on Imbalanced Performance in Hard Switching Parallel Operation*; Available online

[6] IEEE: *Mitigating Inter-Chip Oscillation of paralleled SiC MOSFETs*; Available online

[7] IEEE: *Influence of Parasitic Capacitances on Transient Current Distribution of Paralleled SiC MOSFETs*; Available online

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