Custom output voltage configuration in pin-strap mode using TDA38725 and TDA38740

OptiMOS™ iPOL TDA38740/25 40 A/25 A PMBus/I2C synchronous buck regulator

About this document

Scope and purpose

This application note proposes a method to configure various custom output voltages in pin-strap mode through practical implementation using OptiMOS™ iPOL TDA38740/25 PMBus/I2C synchronous buck regulators.

Intended audience

This document is intended for FAEs, customers, and application engineers who work on design and development of POL rails.

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1 Introduction

OptiMOS™ iPOL TDA38740/25 is an easy-to-use, fully integrated and highly efficient 40 A synchronous buck regulator. The onboard PWM controller and OptiMOS™ FETs with the integrated bootstrap diode make TDA38740/25 a small-footprint solution, providing highly efficient power delivery. The fast constant on-time (COT) control scheme simplifies design efforts and achieves fast control response. TDA38740/25 is available in both PMBus and pin-strap functionality.

- **PMBus/digital mode:** In this mode, the device configuration can be easily defined using Infineon's XDP™ Designer GUI and is stored in the on-chip memory. XDP™ Designer can be downloaded from Infineon Developer Center launcher.
- **Pin-strap/analog mode:** In this mode, TDA38740/25 devices provide the pin-strapping functionality to boot up the part with output voltage, current limit, switching frequency, forced continuous conduction mode (FCCM) or diode emulation mode (DEM), and address offset parameters to a value determined by the pin-strap resistors. In this mode, the output voltage is selected by connecting a resistor from the VBT pin to GND per a defined resistor table. This may be a limitation for some of the customers using an output voltage that is different from the available configurable options.

This document proposes a theoretical and practical implementation to configure the output voltage as close as possible to the actual requirements. Figure 1 shows the application circuit of the TDA38740/25 synchronous buck regulator.

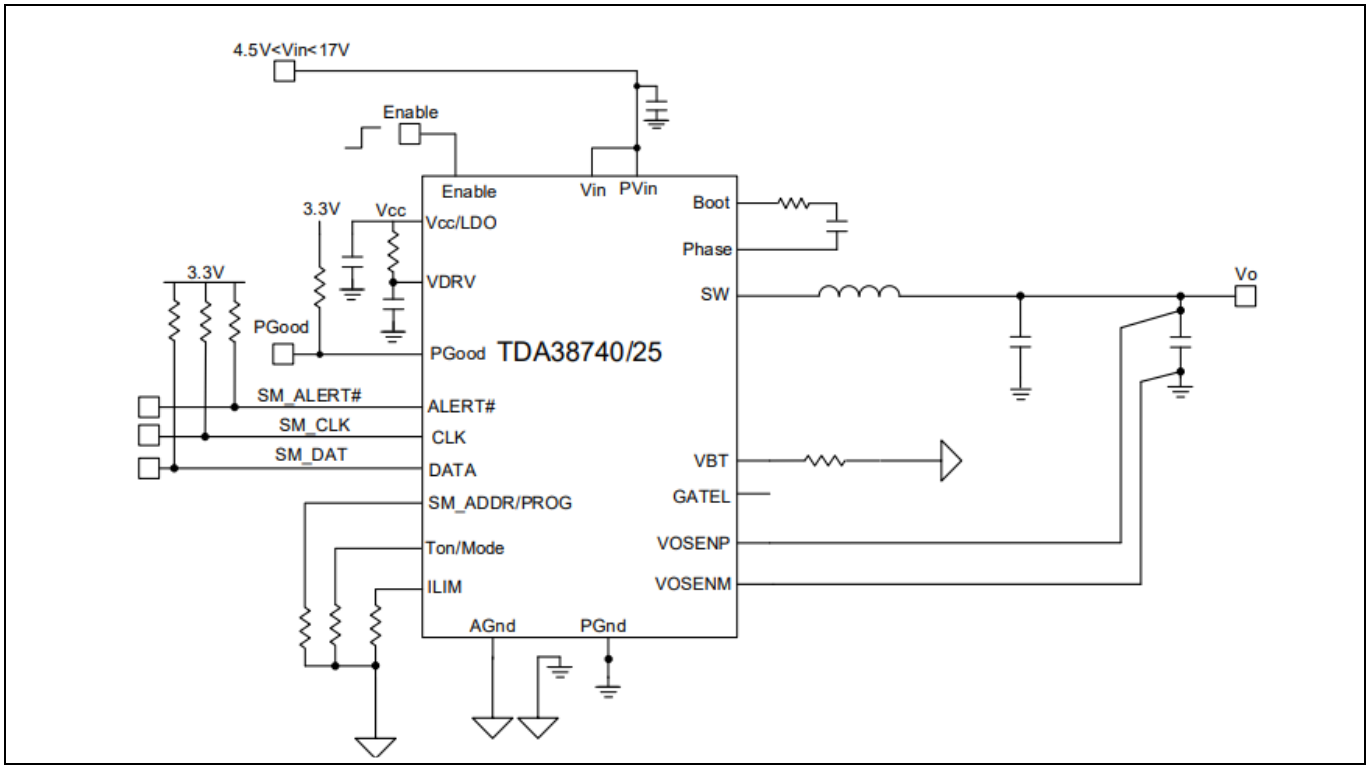

Figure 1 TDA38725/40 application diagram

1.1 TDA38740/25 features

- Single 5 V to 17 V application or wide input voltage range from 3.0 V to 17 V with external VCC
- Output voltage range: 0.25 V to 5.12 V with external feedback resistor divider
- Enhanced Fast COT engine stable with ceramic output capacitors without external compensation
- Optional forced continuous conduction mode (FCCM) and diode emulation (DEM) for enhanced light-load efficiency
- Pin programmable output voltage, switching frequency/mode selection with 16 unique selectable settings
- PMBus system interface for reporting of temperature, voltage, current, and power telemetry
- Single-image multiple-time programming (MTP) for the user section

Refer to the TDA38740/25 datasheet [2] for more details.

2 Pin-strap functionality

With the pin-strap functionality, TDA38740/25 operates as an analog IC with parameters such as output voltage, current limit, switching frequency, FCCM or DEM modes, and address offset determined by the pin-strap resistors. This is useful in applications which does not require any digital interface or telemetry information. In general, this device takes up two addresses: one for I2C and the other for PMBus. By default, the address offset functionality is enabled in the part to ensure unique identification of the device address.

2.1 Output voltage configuration

When operating in pin-strap resistor mode, the output voltage can be selected by connecting a resistor from the VBT pin to GND as highlighted in Table 1 and Table 2. The VBT pin can be used to set the output voltages in the range of 0.4 V to 2.5 V in VOUT_SCALE_LOOP 1:1 and from 0.8 V to 5 V in VOUT_SCALE_LOOP 1:2.

Section 3 proposes a method to set custom output voltage configurations in both 1:1 and 1:2 voltage scale loops (VSL) that are slightly out of the available range of output voltage settings.

Table 1 Output voltage and OVP limits for VOUT_SCALE_LOOP 1:1

VBT (kΩ)	Boot-up voltage (V)	Relative OVP/UVP (mV)	Fixed OVP
Short	0.4	150	0.8
5.62	0.5	150	1
9.53	0.6	150	1
14	0.7	150	1.2
21	0.8	200	1.2
30.1	0.9	200	1.2
36.5	1	200	1.35
43.2	1.05	200	1.35
51.1	1.1	200	1.35
61.9	1.2	200	1.5
75	1.25	250	1.8
88.7	1.35	250	1.8
105	1.5	300	2.2
127	1.65	300	2.2
147	1.8	300	2.2
Float	2.5	300	2.85

Table 2 Output voltage and OVP limits for VOUT_SCALE_LOOP 1:2

VBT (kΩ)	Boot-up voltage (V)	Relative OVP/UVP (mV)	Fixed OVP
Short	0.8	200	1.6
5.62	1.0	200	1.6
9.53	1.2	200	1.6
14	1.4	300	2.0
21	1.6	300	2.4
30.1	1.8	300	2.4
36.5	2.0	300	2.7
43.2	2.1	300	2.7
51.1	2.2	300	2.7
61.9	2.4	300	3.0
75	2.5	300	3.0
88.7	2.7	300	3.6
105	3.0	300	3.6
127	3.3	300	4.4
147	3.6	300	4.4
Float	5.0	300	5.7

2.2 Current limit configuration

The OCP limit can be selected by connecting a resistor from the ILIM pin to GND. Refer to the TDA38740/25 datasheet [2] for information about the current limit resistor settings. Loop compensation filter (LCF) zero selection is also available on ILIM pin; however, it does not affect the OCP operation and is part of the control loop tuning.

2.3 Mode and switching frequency configuration

The switching frequency and the operating mode can be set by connecting a resistor from the MODE/TON pin to GND. Refer to the TDA38740/25 datasheet [2] for information about the switching frequency and mode resistor settings.

3 Custom output voltage configuration

The TDA38740/25 part uses analog front end (AFE) to process the output voltage feedback of the point-of-load (POL) converter. This AFE block has a certain finite impedance at the feedback terminals. This finite impedance can be used as an advantage to create an offset to generate custom output voltages that are slightly out of the range of available options in pin-strap mode.

3.1 Analog front end output voltage equation

Consider the case of using a resistor divider in the feedback path to derive the output voltage equation including the impedance of AFE block as shown in Figure 2:

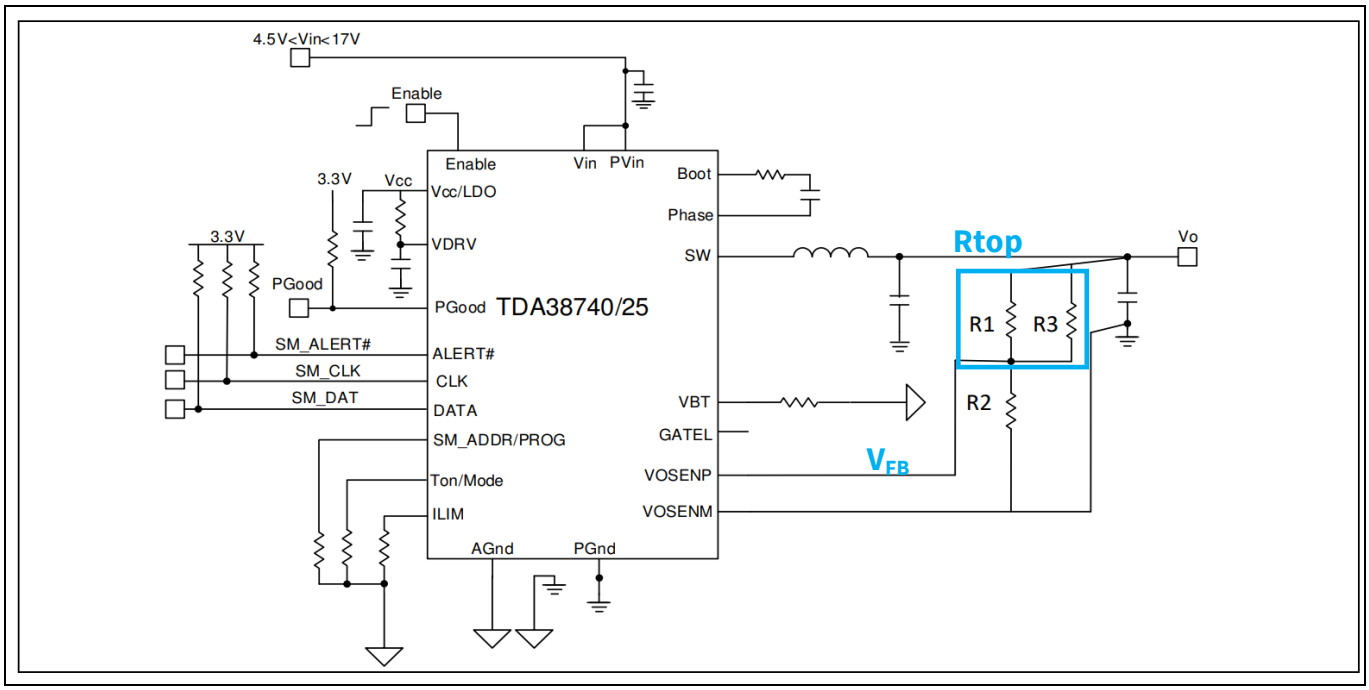

Figure 2 Application circuit used for calculations

The value of R_{top} in Figure 2 can be deduced by calculating the amount of current flowing in the feedback path as shown below:

$$R_{top} = \frac{(V_O - V_{fb})}{\frac{V_{fb}}{R2} + \frac{V_{fb}}{13570} - \frac{1.2}{20000}}$$

Equation 1 Equation for R_{top} calculations

Where,

V_{fb} = Feedback voltage

V_O = Output voltage

R2 = Bottom resistor of the feedback divider

R_{top} = Parallel combination of top feedback resistor R1 and offset compensation resistor R3; 13750 Ω and 20000 Ω are the internal resistances of the AFE block

Based on Equation 1, the equation of output voltage can be deduced as shown in Equation 2:

$$V_{out} = V_{fb}\left(1 + \frac{R_{top}}{R2} + \frac{R_{top}}{13750}\right) - \frac{1.2 * R_{top}}{20000}$$

Equation 2 Equation for output voltage

3.2 Configuration of output voltage to 0.92 V

Equation 2 can be used to configure the pin-strap versions of TDA38740/25 parts to generate the custom output voltage of 0.92 V. It is derived for both 1:1 and 1:2 voltage scale loop (VSL) applications. For output voltages < 2.5 V, 1:1 VSL can be used; for output voltages > 2.5 V, 1:2 VSL can be used.

3.2.1 VSL 1:1 application

In 1:1 VSL applications, the feedback resistor divider is not used; the output voltage is directly tied to the feedback terminals of TDA38740/25 parts. To ensure a higher accuracy of the calculations performed using Equation 1, the resistance of open components is considered as 100 MΩ. The nearest pin-strap option has been selected as 0.9 V output, which requires a boot resistor of 30.1 kΩ per Table 1. Calculations of the required feedback resistor used to generate 0.92 V is as shown below:

$$R_{top} = \frac{0.92-0.9}{\frac{0.9}{100M} + \frac{0.9}{13570} - \frac{1.2}{20000}} = 3170\ \Omega$$

Equation 3 R_{top} calculation for 0.92 V output

Selected R_{top} = R1 = 3300 Ω, R3 = NC, R2 = NC in the actual application because this provides an output voltage closer to 0.92 V per Equation 2. In 1:1 VSL applications, always select an available pin-strap voltage lower than the desired output voltage because the additional offset voltage is achieved using a series resistor in the feedback path.

Output undervoltage protection (UVP) and overvoltage protection (OVP) will be configured to relative UVP and OVP in the pin-strap part; these values are set based on the boot resistor value per Table 1. In this case with output voltage set to 0.9 V, the relative UVP and OVP will be 200 mV relative to 0.9 V resulting in 700 mV and 1100 mV. Calculations for UVP and OVP limits with R_{top} = R1 = 3300 Ω, R3 = NC, R2 = NC are shown below:

$$V_{uvp} = 0.7\left(1 + \frac{3300}{100M} + \frac{3300}{13750}\right) - 1.2 * \frac{3300}{20000} = 0.67\ V$$

Equation 4 Calculation of relative UVP for VSL 1:1

$$V_{ovp} = 1.1\left(1 + \frac{3300}{100M} + \frac{3300}{13750}\right) - 1.2 * \frac{3300}{20000} = 1.166\ \text{V}$$

Equation 5 Calculation of relative OVP for VSL 1:1

Considering the impact of R_{top} = R1 = 3300 Ω, the part will trigger UVP and OVP at 0.67 V and 1.166 V respectively per the calculations shown in Equation 4 and Equation 5.

3.2.2 VSL 1:2 application

In 1:2 VSL applications, it is recommended to use a 1:2 feedback resistor divider using 499 Ω, and directly tie the output voltage across the bottom feedback resistor divider to the feedback terminals of TDA38740/25. To ensure a higher accuracy of the calculations performed using Equation 1, the resistance of open components is considered as 100 MΩ. The nearest pin-strap option has been selected as 1.0 V output, which requires a boot resistor of 5.62 kΩ per Table 2. Use feedback voltage as 0.5 V during initial calculations to derive Rtop that could generate an output voltage of 0.92 V.

Calculations of the required feedback resistor used to generate 0.92 V are shown below. In 1:2 VSL applications, always select an available pin-strap voltage higher than the desired output voltage because the top resistor value of the feedback divider is reduced using a parallel resistor R3 to create the desired offset in the output voltage.

$$R_{top} = \frac{0.92-0.5}{\frac{0.5}{499}+\frac{0.5}{13570}+\frac{1.2}{20000}} = 429.95\ \Omega$$

Equation 6 R_{top} calculation for 1:2 VSL to generate 0.92 V

As R_{top} is the parallel combination of resistors R1 and R3 with R1 = 499 Ω, R_{top} can be calculated as follows:

$$R3 = \frac{R1*R_{top}}{R1-R_{top}} = \frac{499*429.95}{(499-429.95)} = 3107\ \Omega$$

Equation 7 R3 calculation

Used R1 = R2 = 499 Ω and R3 = 3.09 kΩ in actual application to generate 0.92 V output.

Output undervoltage protection (UVP) and overvoltage protection (OVP) will be configured to relative UVP and OVP in the pin-strap part; these values are set based on the boot resistor value per Table 2. In this case with output voltage set to 1.0 V, the relative UVP and OVP will be 200 mV relative to 1.0 V resulting in 800 mV and 1200 mV. Calculations for UVP and OVP limits with R1 = R2 = 499 Ω, R3 = 3.09 kΩ are shown below:

$$V_{uvp} = 0.4\left(1+\frac{430}{499}+\frac{430}{13750}\right) - 1.2 * \frac{430}{20000} = 0.735\ V$$

Equation 8 Calculation of relative UVP for VSL 1:2

$$V_{ovp} = 0.6\left(1+\frac{430}{499}+\frac{430}{13750}\right) - 1.2 * \frac{430}{20000} = 1.114\ V$$

Equation 9 Calculation of relative OVP for VSL 1:2

4 Bench results

Infineon evaluation boards EVAL_TDA38725A_1.1VOUT and EVAL_TDA38725A_3.3VOUT were used to generate an output voltage of 0.92 V using the theoretical analysis performed in Section 3 for both 1:1 and 1:2 VSL applications. The changes made in the schematics are shown below:

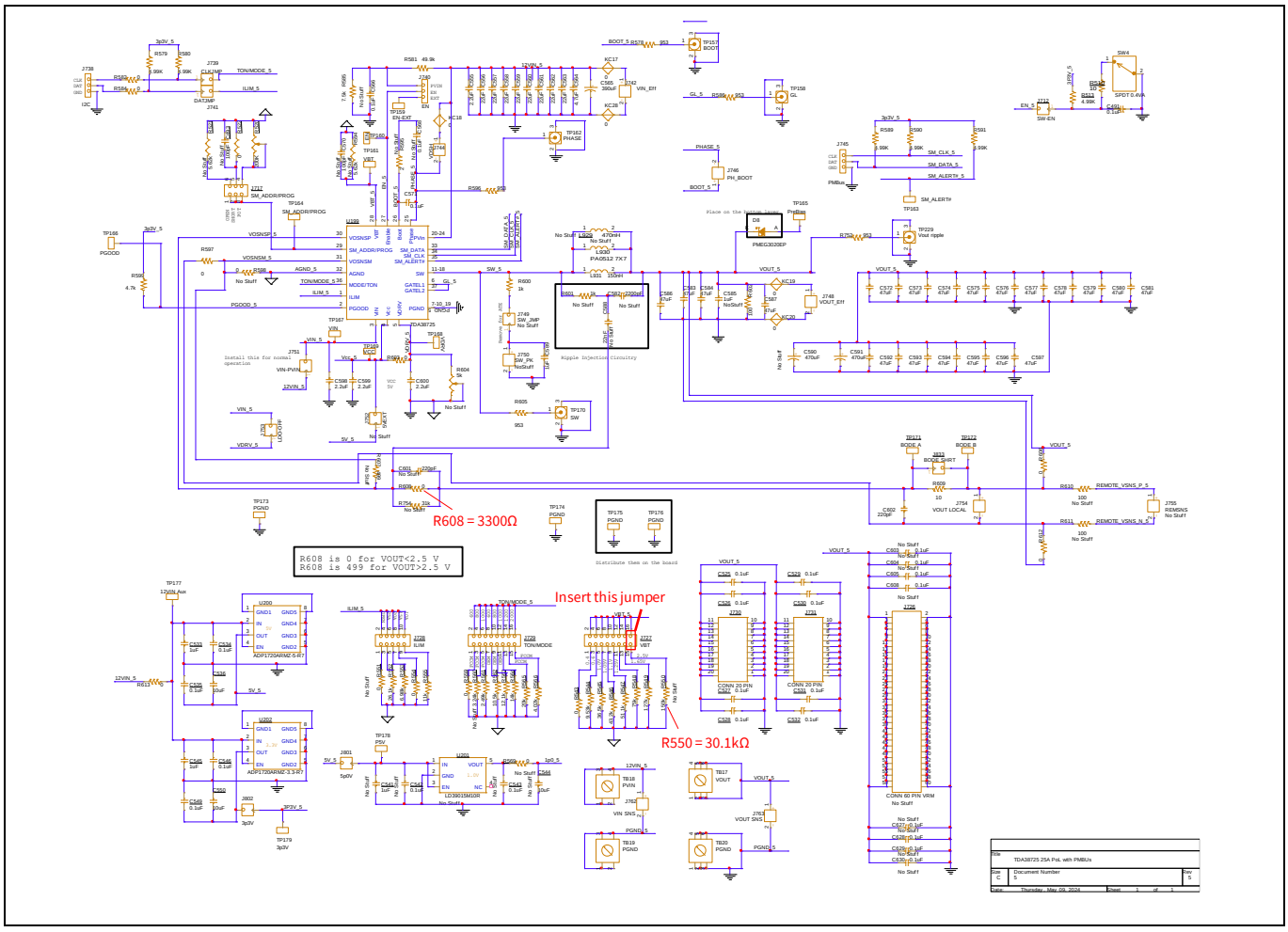

Figure 3 VSL 1:1 evaluation board schematics for V_O = 0.92 V

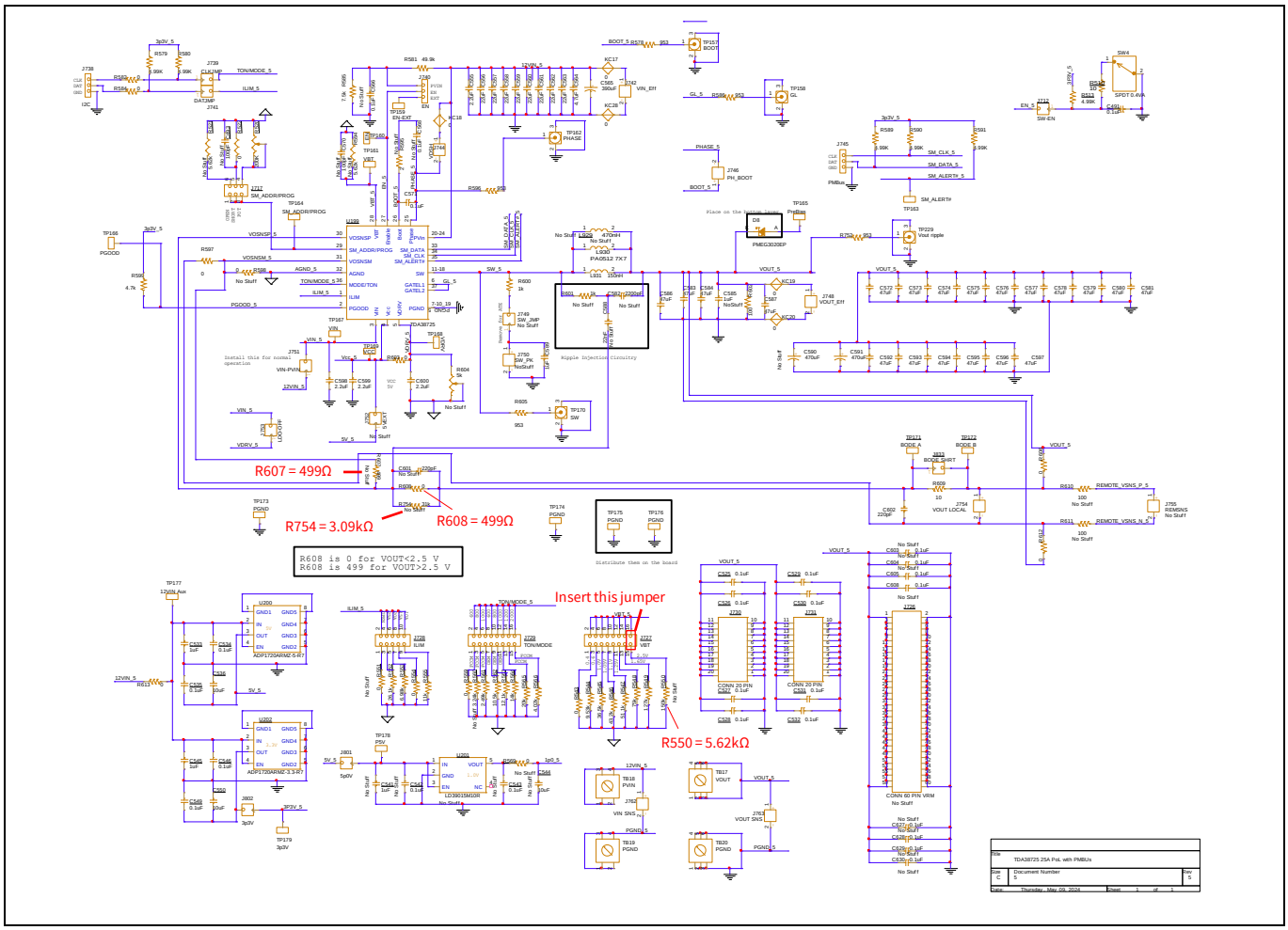

Figure 4 VSL 1:2 evaluation board schematics for V_o = 0.92 V

4.1 Start-up and steady-state waveforms

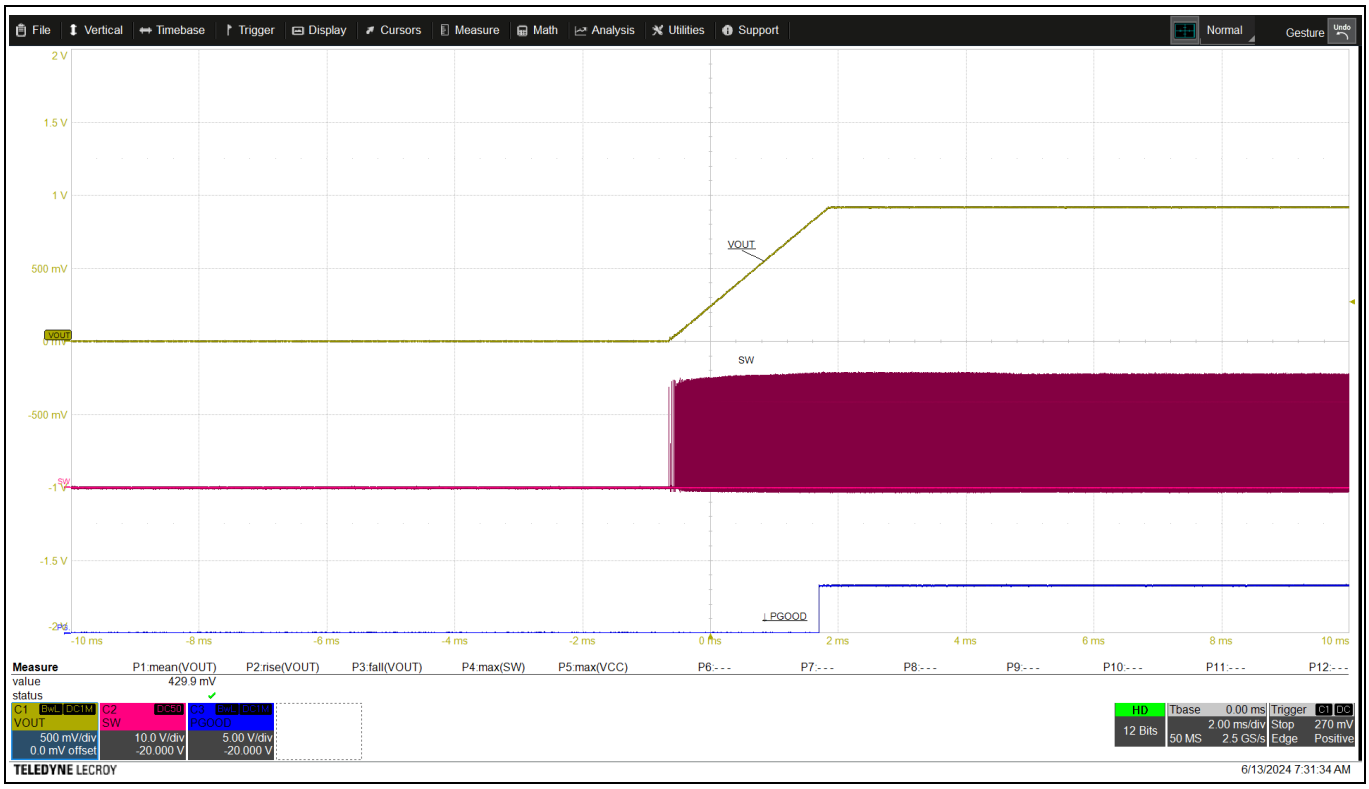

Figure 5 Start up with V_o = 0.92 V using VSL 1:1

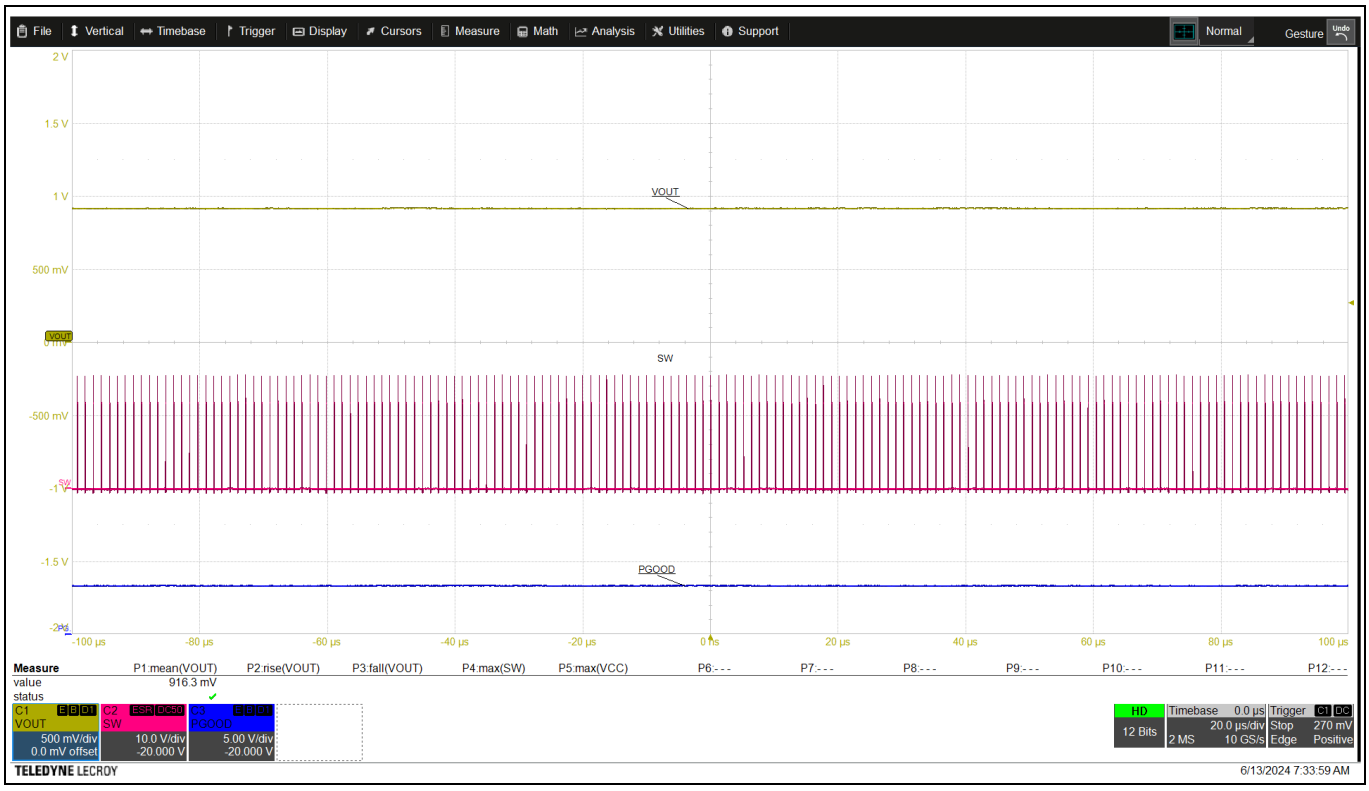

Figure 6 Steady state with V_o = 0.92 V using VSL 1:2

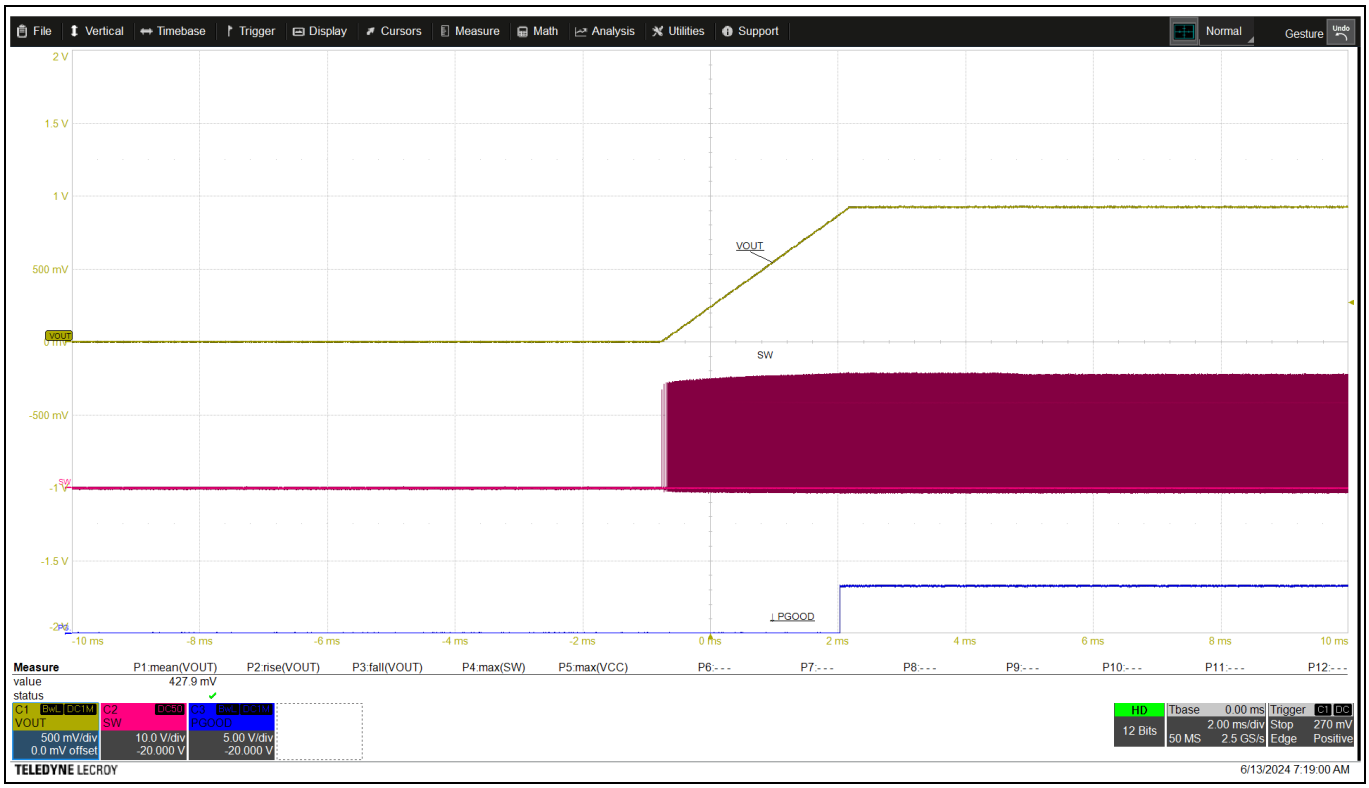

Figure 7 Start up with V_o = 0.92 V using VSL 1:2

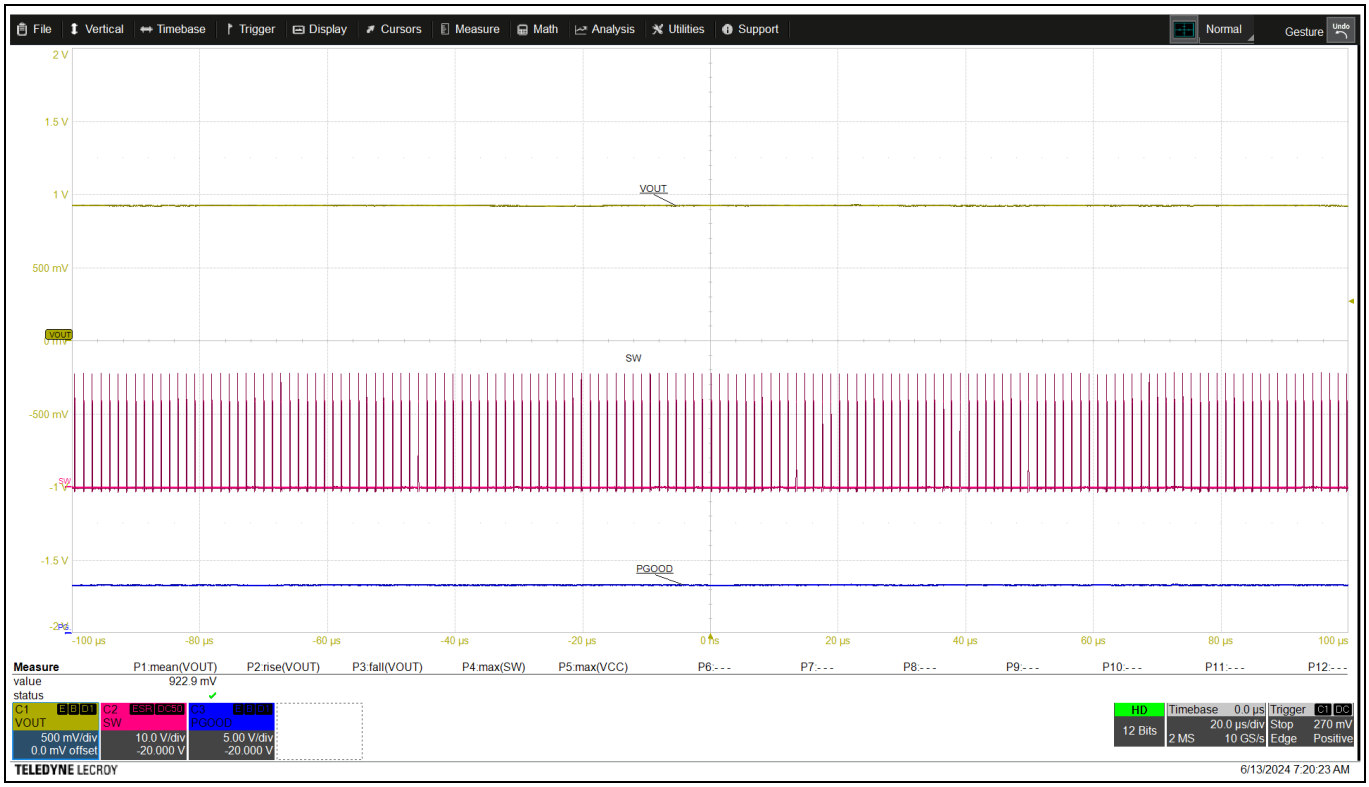

Figure 8 Steady state with V_o = 0.92 V using VSL 1:2

References

[1] Infineon Technologies AG: *Introduction of Fast COT*; Available online

[2] Infineon Technologies AG: *TDA38740/25 OptiMOS iPOL*; Available online

Revision history

Document revision	Date	Description of changes
V 1.0	2024-09-11	Initial release

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